國立交通大學

電子工程學系 電子研究所

博 士 論 文

矽奈米尺寸金氧半場效電晶體的載子傳輸與重要元件參數之實驗性的研究

Experimental Study of Carrier Transport and Important Device Parameters for Nanoscale Si MOSFETs

研 究 生：李維

指導教授：蘇彬 教授

中 華 民 國 九十八 年 二 月

矽奈米尺寸金氧半場效電晶體的載子傳輸與重要元件參數之實驗性的研究

Experimental Study of Carrier Transport and Important Device Parameters for Nanoscale Si MOSFETs

研 究 生：李維　　Student：Wei Lee

指導教授：蘇彬 博士　　Advisor：Dr. Pin Su

國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

A Dissertation
Submitted to Department of Electronics Engineering and
Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electronics Engineering

February 2009
Hsinchu, Taiwan, Republic of China

中華民國 九十八 年 二 月

矽奈米尺寸金氧半場效電晶體的載子傳輸與重要元件參數之實驗性的研究

研 究 生：李維　　指導教授：蘇彬 博士

國立交通大學 電子工程學系 電子研究所

摘要

本論文針對多閘極金氧半場效電晶體，比較其載子傳輸在重疊與非重疊閘源（汲）極結構中之差異，在具有重疊結構的元件中，我們觀察到次臨界電流特性依循波茲曼定律以及聲子為主要之載子碰撞特性，而在非具有重疊閘源（汲）極結構的元件中，我們發現次臨界區域與反轉區域之汲極電流對溫度並不敏感。我們的低溫量測結果指出，對於窄的重疊結構元件而言，載子在能階間碰撞是傳輸的主要機制，而對於非重疊結構元件而言，存在於非重疊區域的位能障會導致電導降低以及擾動。

此外，我們針對非具有重疊閘源（汲）極結構的多閘極金氧半場效電晶體，有系統地分析其可被控制的單電子效應與通道長、通道寬、閘極電壓、溫度之間的相依性。我們的研究指出，使用非重疊閘源（汲）極結構有助於實現單電子電晶體於金氧半場效電晶體，同時多閘極結構提供高閘極控制能力與高源（汲）極電阻的雙重優點，單電子效應被進一步地強化，目前的結果顯示，如果要實現室溫下可運作的單電子電晶體，除了元件尺寸必須要進一步維縮之外，穿隧位能障以及源（汲）極電阻必須要再進一步最佳化。由於單電子效應可被實現於最先進的金氧半場效電晶體，因此有助單電子電晶體整合於低功率互補式金氧半電路，

以達到高密度的目的。

另外，我們評估從實驗中萃取通道背向散射的可行性、限制因素以及應用範圍，我們的研究指出，其困難點在於是否能正確決定低電場載子遷移率（μ_0）、關鍵長度（l）與熱速度（v_{therm}）的溫度係數，透過我們所提出的自我相符萃取方法，我們不必預先假設：平均自由徑 $\lambda = (2k_BT\mu_0/qv_{therm})$，$l = k_BT$ 長，μ_0 =低電場載子遷移率，以及非退化極限。用這個廣義溫度相依性的萃取方法來分析應力效應對通道背向散射的影響，我發現 p 型金氧半場效電晶體之通道背向散射會因單軸壓縮應力增強而下降。至於應力效應與靜電位能的相關性，第一次透過實驗方法萃取出。我們還進一步證實應力作用能夠透過增強彈道傳輸效率進而抑制汲極電流的變異。

還有，我們針對具有超薄氧化層的金氧半場效電晶體，研究其漏電流所引起異常電容電壓特性的問題，我們提出用本質輸入阻抗來模擬長通道金氧半場效電晶體之電容衰減，並反向重建應有的電容電壓特性，透過 SPICE (Simulation Program with Integrated Circuit Emphasis)模擬，我們驗證本質輸入阻抗重建衰減電容的可靠度，而對於所重建的電容電壓特性，我們發現多晶矽閘極空乏效應可以被真實呈現，這個突破是有別於傳統使用頻率相依性所重建出的結果。由於重建方法的簡單性，因此適合作為大量製程觀察之用。

關鍵字：金氧半場效電晶體、量子干涉、單電子、彈道傳輸、背向散射、電容

Experimental Study of Carrier Transport and Important Device Parameters for Nanoscale Si MOSFETs

Student：Wei Lee Advisor：Dr. Pin Su

Department of Electronics Engineering and

Institute of Electronics

National Chiao Tung University

Abstract

This thesis provides a comparative study of carrier transport characteristics for multiple-gate silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistors (MOSFETs) with and without the non-overlapped gate to source/drain structure. For the overlapped devices, we observed the Boltzmann law in subthreshold characteristics and phonon-limited behavior in the inversion regime. For the non-overlapped devices, however, we found insensitive temperature dependence for drain current in both subthreshold and inversion regimes. Our low-temperature measurements indicate that the inter-subband scattering may be the dominant carrier transport mechanism for narrow overlapped multiple-gate SOI MOSFETs (MuGFETs). For the non-overlapped MuGFETs, the voltage-controlled potential barriers in the non-overlapped regions are crucial and may give rise to the conductance reduction and fluctuation.

Besides, we systematically present controlled single-electron effects in the non-overlapped MuGFETs with various gate length, fin width, gate bias and temperature. Our study indicates that using the non-overlapped gate to source/drain

structure as an approach of the single-electron transistor (SET) in MOSFETs is promising. Combining the advantage of gate control and the constriction of high source/drain resistances, single-electron effects are further enhanced using the multiple-gate architecture. From the presented results, downsizing MuGFETs is needed for future room-temperature SET applications. Besides, the tunnel barriers and access resistances may need to be further optimized. Since single-electron effects can be achieved in state-of-the-art MOSFETs, it is beneficial to build SETs in low-power complementary metal-oxide-semiconductor (CMOS) circuits for the ultrahigh-density purpose.

In addition, we have assessed the validity, limitation, and application of experimental channel backscattering extraction. Our study indicates that the difficulty of the temperature-dependent method lies in accurate determination of the temperature sensitivity of low-field mobility (μ_0), critical length (l) and thermal velocity (υ_{therm}). Through our proposed self-consistent approach, channel backscattering can be extracted without assuming $\lambda = (2k_BT\mu_0/q\upsilon_{therm})$, $l = k_BT$ length, μ_0 = low-field mobility, and the non-degenerate limit. Using the generalized temperature-dependent method, we have clarified that channel backscattering of nanoscale p-type MOSFETs can be reduced by the uniaxially compressive strain. Moreover, we have experimentally extracted the electrostatic potential of the source-channel junction barrier with accurate strain and gate voltage dependence. We have demonstrated that the strain technology can improve the drain current variation as well as the mismatch properties through the enhanced ballistic efficiency.

Moreover, we have investigated anomalous inversion capacitance-voltage (C–V) attenuation for MOSFETs with leaky dielectrics. We propose to reconstruct the inversion C–V characteristic based on long-channel MOSFETs using the concept of

intrinsic input resistance (R_{ii}). The concept of R_{ii} has been validated by segmented SPICE (Simulation Program with Integrated Circuit Emphasis) simulation. Our reconstructed $C-V$ characteristics show poly-depletion effects, which are not visible in the two-frequency three-element method, and agree well with the NCSU CVC ($C-V$ analysis software developed by the North Carolina State University) simulation results. Due to its simplicity, our proposed R_{ii} approach may provide an option for regular process monitoring purposes.

Keywords: MOSFET, Quantum interference, single-electron, ballistic transport, backscattering, capacitance

誌 謝

本論文的完成，首先我要感謝我的指導教授 蘇彬 博士，蘇老師在過去五年半的時間裡，給予我許多的指導與鼓勵，我也在這五年半的時間從老師身上學到做研究的態度與方法。也感謝老師安排我進台積電實習，讓我在學校學習理論的同時，有更多的機會可以務實驗證，使我對於元件特性與物理有更深地了解。

另外，我也要感謝台積電 SPICE 部門所有長官與同仁，特別是長時間帶我的老闆 蘇芻暐 博士，由於有他的指點，我可以更快進入對超薄氧化層之相關研究軌道，另外我還要特別感謝 SPICE 實驗室的管理者 林忠凱 博士、彭琴嬌 助理工程師，讓我有充分的空間可以使用最先進的量測機台。

還有，我也要感謝曾經麻煩過的學長林宏年、葉冠麟、李耀仁、盧文泰、李明賢、余正明，還有現在的學弟妹 陳柏年、王生圳、吳育昇、郭俊延、胡璧合、范銘隆、呂昆諺、謝欣原，由於有他們的幫助，讓我在研究上能更順利。

在這我也要感謝我的家人，特別是我的母親，由於有她的默默鼓勵與祝福，讓我能夠在心情沮喪時得到安慰，我還要感謝我的女友，陪我一起度過這快兩年的研究時間，有你們的關心與照顧，讓我有讀博士班、做研究的動力。

最後，謹以此論文獻給我的家人，以及所有關心我的朋友。

李維

誌于 交大-台積電

2009/1

Contents

Abstract (Chinese) i
Abstract (English) iii
Acknowledgement (Chinese) v
Contents vi
Table captions x
Figure captions xi

Chapter 1 Introduction

1.1 Background and motivation 1
1.2 Organization 5

Chapter 2 Comparison of Carrier Transport for Overlapped and Non-overlapped Multiple-Gate SOI MOSFETs

2.1 Introduction 12
2.2 Overlapped and non-overlapped device structures 13
2.3 Experimental comparison 13
2.3.1 Classical characteristics 13
2.3.2 Mesophysical characteristics 14
2.4 Interpretation 16
2.4.1 Intersubband scattering effects 16
2.4.2 Single-electron effects 16
2.4.3 Variable range hopping conductance 17
2.4.4 Universal conductance fluctuations 17
2.4.5 Quantum interference effects 17
2.5 Application to effective channel length extraction 20
2.6 Conclusion 23

Chapter 3 Single-Electron Effects of Non-overlapped Multiple-Gate SOI MOSFETs

3.1 Introduction 48
3.2 Coulomb blockade oscillation 50
3.3 Experimental measurement of single-electric effects 51
3.3.1 Devices 51
3.3.2 Single-electric effects in multiple-gate devices 52
3.3.3 L_g & W_{fin} dependence 53
3.3.4 V_{GS} dependence 54

3.3.5 N_B dependence 55
3.4 Discussion 55
3.4.1 Quantum mechanical effects 56
3.4.2 Multiple-dot system 57
3.4.3 Gate-dot coupling strength 57
3.5 Application to capacitance extraction 58
3.6 Conclusion 59

Chapter 4 Ballistic Transport Characteristics of Nanoscale MOSFETs

4.1 Introduction 86
4.2 Channel backscattering theory 89
4.3 A new self-consistent temperature-dependence extraction method..... 91
4.3.1 $I_{d,sat}$ and $V_{T,sat}$ 92
4.3.2 β..... 93
4.3.3 γ..... 94
4.3.4 Experimental guidelines 95
4.4 Experimental investigation of Coulomb scattering effects on channel backscattering characteristics 96
4.4.1 Impact of body doping 96
4.4.2 Impact of high-k dielectrics 97
4.5 Experimental investigation of impacts of process induced uniaxial strain on channel backscattering characteristics 97
4.5.1 Devices 97
4.5.2 Channel backscattering characteristics 98
4.6 Experimental investigation of channel backscattering for SOI MOSFETs 100
4.6.1 Extraction method with self-heating correction 100
4.6.2 Impact of floating-body and self-heating effects 101
4.7 Application of ballistic efficiency to suppression of drain current variation 102
4.8 Conclusion 103

Chapter 5 Gate-Tunneling Current Induced Capacitance-Voltage Problems

5.1 Introduction 136
5.2 Devices and measurements 138
5.3 BSIM4-based macro model and SPICE simulation 139

5.3.1 Short-channel device 140
5.3.2 Long-channel device 140
5.4 Intrinsic input resistance model 141
5.5 Experimental reconstruction 142
5.6 Conclusion 144

Chapter 6 Conclusions 162

Vita (Chinese) 167
Publication list 168

Table Captions

Chapter 3

Table 3.1 Several studies on single-electron effects in Si-based MOS structures……64
Table 3.2 A list of devices studied in this work……..65

Figure Captions

Chapter 2

Fig. 2.1 (a) Multiple-gate FinFET SOI structure investigated in this work and its cross-sectional AA' view along the channel direction showing (b) the non-overlapped gate to source/drain structure and (c) the overlapped gate to source/drain structure……28

Fig. 2.2 Measured I_{DS} vs. V_{GS} characteristics at V_{DS} = 50 mV under T = 300 to 56 K for the overlapped FinFET Device 1 with W_{fin} = 25 nm and L_g = 80 nm……..29

Fig. 2.3 Measured I_{DS} vs. V_{GS} characteristics at V_{DS} = 50 mV under T = 300 to 56 K for the non-overlapped FinFET Device 2 with W_{fin} = 25 nm and L_g = 30 nm…….…….30

Fig. 2.4 Measured channel conductance (G_{DS}) vs. (V_{GS}-V_T) characteristics for the overlapped Device 3 with L_g = 60 nm and W_{fin} = 10 nm at various V_{DS} under (a) T = 56 K and (b) T = 223 K……...31

Fig. 2.5 Measured G_{DS} vs. (V_{GS}-V_T) characteristics for the non-overlapped Device 2 with L_g = 30 nm and W_{fin} = 25 nm at various V_{DS} under (a) T = 56 K and (b) T = 223 K……32

Fig. 2.6 Calculated electronic potential for the non-overlapped gate to source/drain structure at V_{GS} = 0 to 1 V. V_p: peak potential value in the non-overlapped region. V_c: potential value at the channel center. E: carrier energy. d: width of the effective quantum well. I_a: direct tunneling through the potential barrier of the non-overlapped region. I_b: thermally-associated tunneling. I_c: thermionic emission……..33

Fig. 2.7 Measured temperature sensitivity of drain current ($\Delta\log(I_{DS})/\Delta T$) vs. ($V_{GS}$-$V_T$) characteristics for overlapped and non-overlapped devices under (a) high temperature, T = 300 to 250 K and (b) low temperature, T = 223 to 56 K……...34

Fig. 2.8 Calculated transmission probability Tr vs. V_{GS} for d = 30 nm and E-eV_p = 0~5, 5~10 and 10~15 meV……35

Fig. 2.9 Measured G_{DS} and G_m'/V_{DS} vs. $(V_{GS}-V_T)$ characteristics for the non-overlapped Device 2 with L_g = 30 nm and W_{fin} = 25 nm at V_{DS} = 1 and 50 mV under T = 56 and 300 K. (G_m' = $\partial G_m/\partial V_{GS}$ and G_m = $\partial I_{DS}/\partial V_{GS}$)……...36

Fig. 2.10 Calculated transmission probability Tr vs. V_{GS} and E for d = 30 nm……37

Fig. 2.11 Fermi wavelength as a function of $(V_{GS}-V_T)$. The location at which the quantum interference occurs is indicated for d = 30 nm……...38

Fig. 2.12 Fermi wavelength as a function of $(V_{GS}-V_T)$. The location at which the quantum interference occurs is indicated for d = 40 nm……...39

Fig. 2.13 Calculated transmission probability Tr vs. V_{GS} and E for d = 40 nm……40

Fig. 2.14 Measured G_m'/V_{DS} vs. $(V_{GS}-V_T)$ characteristics for the Device 6 with L_g = 40 nm and W_{fin} = 25 nm…….....41

Fig. 2.15 Illustration of the quantum interference effect on I_D–V_{GS}, G_m–V_{GS}, and $\partial G_m/\partial V_{GS}$ vs. V_{GS} characteristics……42

Fig. 2.16 AC G_m measurement used in this work (freq. = 2 MHz). Note that the trapping/de-trapping mechanisms can be suppressed by the AC method……...43

Fig. 2.17 DC and AC measurement results of $\partial G_m/\partial V_{GS}$ vs. V_{GS}-V_T for the Device 4 with L_g = 30 nm and W_{fin} = 25 nm. We can determine the $(V_{GS}-V_T)$ at which quantum interference occurs for each n (indicated by arrows)…...44

Fig. 2.18 DC and AC measurement results of $\partial G_m/\partial V_{GS}$ vs. V_{GS}-V_T for the Device 5 with L_g = 30 nm and W_{fin} = 25 nm…….……45

Fig. 2.19 Extracted V_{GS}-dependent L_{eff} for the non-overlapped multiple-gate FinFETs with L_g = 30 nm and W_{fin} = 25 nm…….….46

Fig. 2.20 A schematic carrier density plot along the channel between source and drain for the non-overlapped gate to source/drain structure at V_{GS} = 0 to 1 V. L_{eff} is determined based on the inversion-layer sheet conductivity……...47

Chapter 3

Fig. 3.1 Schematic of a quantum dot, in the shape of an island, connected to source and drain electrodes by tunnel barriers and to a gate by a capacitor (C_g)……66

Fig. 3.2 An illustration of Coulomb blockade oscillations, the effect of single electron charges on the conductance vs. V_G characteristics. The period in gate voltage V_G is about e/C_g. $V_{G3} > V_{G2} > V_{G1}$……..…..67

Fig. 3.3 An example of Coulomb blockade oscillations in G_{DS} vs. V_G characteristics. The conductance G_{DS} is the ratio I_{DS}/V_{DS} and the period ΔV_G is about e/C_g……...68

Fig. 3.4 Multiple-gate Fin-FET SOI structure investigated in this work and (b) its cross-sectional view along A-A' view showing the non-overlapped gate to source/drain regions. (c) A schematic electronic potential plot along the channel between source and drain for the FinFET with non-overlapped regions……..69

Fig. 3.5 Periodic oscillations occur in G_m/V_{DS} vs. V_{GS} characteristics for (a) the Device 1 and (b) the Device 2 with L_g = 30 nm and W_{fin} = 25 nm at T = 293K……..70

Fig. 3.6 Periodic oscillations occur in dG_m (= G_m-<G_m>) vs. V_{GS} characteristics for the Device 1 at (a) T = 293 K and (b) T = 233 K. <G_m> is the long-range average……..71

Fig. 3.7 Both (a) the FFT and (b) the histogram of the directly counted peak-to-peak spacing (ΔV_G) confirm that the period (<ΔV_G>) in Fig. 3.6 is 17 mV……72

Fig. 3.8 Periodic oscillations occur in G_m/V_{DS} vs. V_{GS} characteristics for the Device 3 with L_g = 40 nm and W_{fin} = 25 nm at T = 20 °C. Smaller peak-to-peak spacing (ΔV_G = 15 mV) from the FFT can be seen……...73

Fig. 3.9 Periodic oscillations occur in dG_m vs. V_{GS} characteristics for the Device 4 with L_g = 40 nm and W_{fin} = 15 nm at (a) V_{GS} = 0~0.2 V, (b) V_{GS} = 0.2~0.4 V and (c) V_{GS} = 0.4~0.6 V. (d) The FFT of periodic oscillations in different V_{GS} regimes……74

Fig. 3.10 V_{GS} dependence of $1/\langle \Delta V_G \rangle$ can be observed for the Device 1 and 4. $\langle \Delta V_G \rangle$ is extracted from the FFT in different V_{GS} regimes……..…..75

Fig. 3.11 An illustration of the V_{GS}-modulated tunnel barriers…….76

Fig. 3.12 Periodic oscillations occur in dG_m vs. V_{GS} characteristics for the Device 5 with L_g = 30 nm, W_{fin} = 25 nm and $N_B = 3\times10^{18}$ cm^{-3} at (a) V_{GS} = -0.8~-0.6 V and (b) V_{GS} = -0.6~-0.4 V. (c) The FFT of periodic oscillations in different V_{GS} regimes…….77

Fig. 3.13 Periodic oscillations occur in dG_m vs. V_{GS} characteristics for the Device 6 with L_g = 40 nm, W_{fin} = 25 nm and $N_B = 3\times10^{18}$ cm^{-3} at V_{GS} = 0~0.3 V. (b) The FFT of periodic oscillations in different V_{GS} regimes…….…..78

Fig. 3.14 Periodic oscillations occur in dG_m vs. V_{GS} characteristics for the Device 7 with L_g = 30 nm and W_{fin} = 25 nm at (a) T = 293 K and (b) T = 56 K……79

Fig. 3.15 Schematic energy diagram of a SET. The quantum energy levels are discrete with each quantum-level spacing defined as $\Delta\varepsilon$. ΔE is the charging energy e^2/C_Σ……....80

Fig. 3.16 Periodic oscillations occur in dG_m vs. V_{GS} characteristics for the Device 8 with L_g = 40 nm and W_{fin} = 25 nm at (a) V_{DS} = 0.3 mV and (b) V_{DS} = 10 mV under T = 56 K……81

Fig. 3.17 (a) Rhombus diagram for the Device 2. (b) dG_m vs. V_{GS} characteristics at V_{DS} = 2 mV. The conductance peaks (dots) correspond to the dots at V_{DS} = 2 mV in (a)…….82

Fig. 3.18 Rhombus diagram for the Device 3 with L_g = 40 nm and W_{fin} = 25 nm…….…….83

Fig. 3.19 Measured junction capacitance C_j per unit width vs. V_{BS} characteristics for planar SOI NMOSFET with high and low doping……....84

Fig. 3.20 C_g vs. L_g characteristics for different extraction methods……..…85

Chapter 4

Fig. 4.1 Schematic diagram illustrating the backscattering theory [1]. Carrier in the critical length l is with a backscattering ratio r_{sat}. The average injection velocity υ_{inj} is determined the equilibrium thermal velocity υ_{therm} and r_{sat} as $\upsilon_{inj} = \upsilon_{therm}(1-r_{sat})/(1+r_{sat})$ ……110

Fig. 4.2 Calculated ballistic efficiency B vs. L_g based on the results of [20] showing the need of accurate $V_{T,sat}$ and $(\beta_\mu-\beta_l)$ ……...111

Fig. 4.3 Measured $I_{d,sat}$ and $V_{T,sat}$ vs. T characteristics for the NMOSFET with L_g = 120 nm. Linear dependence of $I_{d,sat}$ and $V_{T,sat}$ on T is shown for T = 233 ~ 373 K. $V_{T,sat}$ is determined by maximum transconductance method with *DIBL* considered, i.e., $V_{T,sat} = V_{T,lin}$-*DIBL*……...112

Fig. 4.4 Different estimations of $-(\partial V_T/\partial T)/(V_{gs}-V_T)$. $V_{T,lin}$ is extrapolated from the maximum transconductance. *DIBL* is the gate-voltage difference between gate voltages at I_d = 100 nA/μm for V_{ds} = 0.05 and 1.5 V……...113

Fig. 4.5 λ/l vs. T characteristics shows the need of self-consistent β for the backscattering coefficient extraction. In [7]-[15], β = -1.5 from β = $1+(\beta_\mu-\beta_l)$, β_μ = -1.5 and β_l = 1. Note that different values of $I_{d,sat}$ and $V_{T,sat}$ are considered in (4) at the corresponding temperature……..114

Fig. 4.6 Extracted β and β_μ vs. V_{gs} characteristics for the NMOSFET with L_g = 120 nm. β_μ (–□–) is observed based on the effective mobility μ, which is extracted at different temperature by the split *C–V* method with R_{sd} correction……..115

Fig. 4.7 Extracted β vs. L_g characteristics for NMOSFETs at $V_{GS}-V_{T,sat}$ = 0.9 V. The self-consistently extracted β shows significant L_g dependence…..…….116

Fig. 4.8 Extracted r_{sat} and the effective mobility μ vs. V_{gs} characteristics for the NMOSFET with L_g = 120 nm……117

Fig. 4.9 Extracted r_{sat} vs. V_{gs} characteristics for the NMOSFET with L_g = 120 nm with different $\Delta\gamma$ corrections……...118

Fig. 4.10 (a) Extracted β and (b) r_{sat} vs. $(V_{gs}-V_{T,sat})$ characteristics for 100-nm-L_g NMOSFETs with high and low body-doping N_a……....119

Fig. 4.11 (a) Extracted β and (b) r_{sat} vs. (V_{gs}-$V_{T,sat}$) characteristics for 100-nm-L_g NMOSFETs with HfO_2 and SiO_2 gate dielectrics……..120

Fig. 4.12 Measured drain-current vs. gate voltage characteristics for 50-nm-L_g PMOSFETs with and without uniaxially compressive strain at T = 233, 298, 373 K for (a) $|V_{ds}|$ = 0.05 V and (b) $|V_{ds}|$ = 1.3 V……....121

Fig. 4.13 (a) Extracted β and (b) r_{sat} vs. $|V_{gs}$-$V_{T,sat}|$ characteristics for 50-nm-L_g PMOSFETs with and without uniaxially compressive strain [23][24]. The R_{sd} effect has been corrected. (R_{sd} ~ 125 Ω/um for the strained device and 214 Ω/um for the unstrained device)……..122

Fig. 4.14 Extracted (a) thermal velocity v_{therm}, (b) mean-free path λ and (c) effective mobility μ vs. $|V_{gs}$-$V_T|$ characteristics for 50-nm-L_g PMOSFETs with and without uniaxially compressive strain at T = 298 K. λ is extracted from the slop of $I_{d,lin}$–V_{ds} characteristics at V_{ds} = -20 ~ 20 mV. Effective mobility is extracted from the split C–V method at V_{ds} = 50 mV with R_{sd} correction [2]……123

Fig. 4.15 Extracted potential -k_BT/q vs. (l_T-l_{233K}) characteristics for (a) strained and unstrained PMOSFETs with L_g = 50 nm at $|V_{gs}$-$V_{T,sat}|$ = 0.8 V and $|V_{ds}|$ = 1.3 V, and (b) the strained PMOSFET with L_g = 50 nm at $|V_{gs}$-$V_{T,sat}|$ = 0.4 ~ 0.8V and $|V_{ds}|$ = 1.3 V……..124

Fig. 4.16 Our self-consistent method considering accurate temperature dependence of carrier mobility and self-heating effects……125

Fig. 4.17 Self-heating induced ΔT vs. ambient temperature T_0 for the SOI MOSFET with L_g = 63 nm. R_{th} (= 67064 K/W) is extracted by the method presented in [34]……..126

Fig. 4.18 λ/l vs. T characteristics for (a) the constant β = -1.5 (i.e., β_μ = -1.5 and β_l = 1) and the self-consistent β, and (b) the self-consistent β with and without the correction of self-heating……...127

Fig. 4.19 r_{sat} vs. V_{gs} characteristics for SOI NMOSFETs with L_g = 216 nm and 63 nm using the conventional method (i.e., assuming β = -1.5 in (10))……128

Fig. 4.20 r_{sat} vs. V_{gs} characteristics for SOI NMOSFETs with L_g = 216 nm and 63 nm using the self-consistent method with and without self-heating corrections……129

Fig. 4.21 G_{ds} and the extracted β vs. V_{ds} characteristics for SOI NMOSFET with L_g = 216 nm and 63 nm. The floating-body effects can be seen in both G_{ds} and the self-consistently extracted β……130

Fig. 4.22 Comparison of $\sigma(V_T)$ and $\sigma(V_T)/V_T$ for strained and unstrained PFETs……..131

Fig. 4.23 $\sigma(I_{d,sat})/I_{d,sat}$ vs. $\sigma(\mu_0)/\mu_0$ characteristics for strained and unstrained PFETs with L_g = 50 ~ 500 nm at V_{ds} = 1.3 V……..132

Fig. 4.24 B_{sat} enhancement and μ enhancement vs. L_g characteristics for strained and unstrained PFETs. B_{sat}: ballistic efficiency B in saturation region……...133

Fig. 4.25 V_{ds} dependence of the ballistic-efficiency enhancement. B is near $\lambda/(2l+\lambda)$ for high V_{ds} and $\lambda/(L_g+\lambda)$ for low V_{ds}……...134

Fig. 4.26 $\sigma(I_d)/I_d$ vs. $\sigma(\mu_0)/\mu_0$ characteristics for strained and unstrained PFETs with L_g = 50 ~ 500 nm at V_{ds} = 0.3 V……..135

Chapter 5

Fig. 5.1 (a) Inversion MOS capacitance (C_{gc}) for the short-channel (L_g = 0.24μm) device. C_0: true capacitance for L_g = 10 μm. (b) The variation of C_m increases as L_g decreases. C_m: measured capacitance. $<C_m>$: C_m mean……148

Fig. 5.2 (a) The impact of cable inductance, L_s, on C_{gc}. (b) Frequency dependence of the measured C_{gc}……149

Fig. 5.3 (a) BSIM4-based macro model. C_f: fringing capacitance. $R_4 = 1\text{x}10^9$ Ω, $C_4 = 1\text{x}10^{-9}$ F. (b) Our BSIM4 extraction methodology of the inversion MOS capacitance……..150

Fig. 5.4 (a) Merely considering R_{ge} and R_{sd} without taking L_i into account cannot model the C_{gc} characteristics in the high gate bias regime. (b) In the same MOS array of short-channel devices, the impact of on-chip inductance (L_i) depends on the measurement configuration. (For the SD-G case, the Hi port is connected to source/drain, while the Lo port to the gate

electrode.)……152

Fig. 5.5 The segmented SPICE simulation reveals the importance of calibrations and the distributed effect for the long channel device……153

Fig. 5.6 The cable inductance L_s vs. frequency characteristics. ~1μH L_s can be excluded after performing the SHORT calibration……154

Fig. 5.7 (a) DC and (b) AC verification of the segmented SPICE simulation for the distributed effect……155

Fig. 5.8 (a) The gate-tunneling induced *C–V* attenuation due to de-biasing effect can be simulated by BSIM4/SPICE simulation. (b) The gate currents simulated by the segmented simulation and the R_{ii} lumped simulation are nearly identical. (c) Segmented SPICE simulation with each sub-transistor modeled by the BSIM4 MOSFET model. (d) Single-transistor SPICE simulation with R_{ii} added to the gate terminal in addition to R_{ge}……156

Fig. 5.9 (a) R_{ii} for L_g = 10 μm device can be extracted from the DC output characteristics. (b) R_{ii} as a function of V_{GS} and L_g……...158

Fig. 5.10 Small-signal equivalent models for MOS capacitor. (a) Three-element model. (b) Two-element parallel model……..159

Fig. 5.11 Reconstructed *C–V* characteristics for (a) NMOS and (b) PMOS with and without considering R_{ii}. The results agree well with the simulation results of NCSU CVC. (T_{OX} = 1.15 nm. NMOS : N_{Bulk} = 3E17 cm^{-3}, N_{Gate} = 1.8E20 cm^{-3}, $R_{ge}+R_{sd}/2$ = 40 Ω. PMOS : N_{Bulk} = 2.5E17 cm^{-3}, N_{Gate} = 8.5E19 cm^{-3}, $R_{ge}+R_{sd}/2$ = 180 Ω.)……160

Fig. 5.12 The contribution of intrinsic input resistance in the overall gate-current induced de-biasing effect. $R_s = R_{ii}+R_{ge}+R_{sd}/2$……161

Chapter 1

Introduction

1.1 Background and motivation

Regarding conventional silicon metal-oxide-semiconductor field-effect transistors (MOSFETs), the device size is scaled in all dimensions, resulting in smaller oxide thickness, channel length, and channel width. Currently, 45 nm (with a physical gate length ~30 nm) is the state-of-the-art process technology, but even smaller dimensions are expected in the future [1]. For example, bulk silicon MOSFETs with the 10-nm physical gate length have been demonstrated by the Intel Corporation [2]. As the device size is scaled, not only device speed (i.e., circuit performance) is enhanced but also the cost and the consuming power can be reduced. To continue the scaling trend, multiple-gate silicon-on-insulator (SOI) MOSFETs are considered as a promising candidate for ultra-scaled complementary metal-oxide-semiconductor (CMOS) devices [3]. It has been reported that excellent subthreshold characteristics can be achieved in the nanowire FinFET with the 5-nm physical gate length [4].

It is important to point out that the exponential growth in integrated circuit complexity, which has seen a hundred-million-fold increase in transistor count per chip over the past forty years, will be finally facing its limits. One reason is that critical dimensions, such as transistor gate length L_g and oxide thickness t_{ox}, are reaching physical limitations. Besides, maintaining dimensional integrity at the limits of scaling is also a challenge. Although these manufacturing issues may be overcome by introducing novel materials (e.g., high-k dielectric, germanium channel) or state-of-the-art technologies (e.g., process induced uniaxial strain) for continual

performance enhancement, fundamental device-physics issues may still restrict the device performance enhancement [5]. Several examples are listed as follows:

First, it has been presented in [6] that quantum-mechanical tunneling current from the source to the drain may limit the device performance for ultra-scaled-L_g devices. The insensitive temperature dependence of subthreshold characteristics indicating the tunneling current between the source to the drain was observed for the 8-nm-L_g MOSFET [6]. Such a tunneling current is starting to dominate instead of the thermal current and makes it difficult to obtain sufficiently high on/off current ratio when L_g is reduced.

Besides, significant quantum-mechanical tunneling current through the gate dielectric drastically increases with thinning oxide thickness [6]. The consequences are not only the increasing stand-by power dissipation but also the distorted capacitance-voltage (C–V) characteristics [7]. Note that C–V measurements are a fundamental characterization technique for MOS devices. Accurate determination of device capacitance is critical for oxide thickness extraction [8], metallurgical channel length determination [9], mobility measurement [10] and interface trap characterization [11].

Quantum-mechanical confinement effects are expected for the size smaller than 15 nm and may impact carrier transport. In [12], evidence of one-dimensional subband formation was observed at low temperature in tri-gate SOI MOSFETs, resulting in oscillations of current-voltage characteristics. It is worth noting that such quantum-mechanical effects on current-voltage characteristics can directly impact carrier mobility at room temperature [13]. The inter-subband scattering significantly affects the carrier mobility and results in the negative resistance and the dynamic mobility behavior.

For nanoscale MOSFETs with effective channel length so short comparable to de Broglie wavelength, the quantum interference phenomenon stemmed from the wave nature of channel electrons can occur and impact the transistor characteristics [14]. Strictly speaking, quantum interference occurs when device size and elastic scattering length are smaller than or approximately equal to the "phase coherence length" (i.e., inelastic scattering length) of carriers. This phase coherence length is the distance a carrier travels before it encounters a phase-randomizing collision, which effectively destroys its quantum mechanical wave nature and restores classical (particle-like) behavior [15]. The wave nature of carriers will give rise to conductance fluctuation due to the elastic scattering center, such as trapped charges [14], ionized atoms [16], electric potential barriers [17]. Besides, when the quantum interference prevails, the Anderson localization effect can result in conductance loss [18].

Moreover, the single-electron effect due to Coulomb blockade may also become increasingly significant with scaling CMOS devices because the number of charges in such small size is rare [19]. The phenomenon of single-electron tunneling was first predicted by Russians scientist Likharev in 1986 for a small tunnel junction, which is essentially a small capacitor with a capacitance C. For the small capacitor, the charge Q and the corresponding charging energy ΔE are discrete and relate to C as $\Delta E = Q^2/2C$ [20]. Carrier transport through such a small capacitor is determined by the discrete ΔE and shows periodic oscillations in current-voltage characteristics. Due to the innovation of semiconductor technology, the studies of single-electron phenomena associated with tunneling in semiconductor nanostructures [21], bulk CMOS devices [22], SOI MOSFETs [23] and nano dots [24] have emerged.

Furthermore, the continuous scaling down of MOSFETs has made possible to realize devices with L_g comparable to the carrier transport mean-free-path. In these

structures, carrier motion can be ballistic [25][26], i.e., a carrier can traverse the entire structure from one end to the other without suffering any collision with other carriers, elastic centers, and inelastic phonon. When this happens, the motion of carriers can not be described adequately by the concept of the effective mobility. In [27], the convenience of the effective mobility was challenged especially for a nanoscale MOSFET under high drain bias where off-equilibrium transport dominates. Besides, the performance of nano-scaled devices becomes more complicated to predict just relying on the concept of the effective mobility [28].

From the above examples one may say that the amazing progress of CMOS technology leads to a significant evolution of the mechanisms of carrier transport in nanoscale MOSFETs, and may also affect the basic principles of device scaling and optimization. Therefore, the purpose of this thesis is to explore further into mechanisms of carrier transport in nanoscale MOSFETs as well as to investigate innovative applications based on state-of-the-art CMOS devices.

In addition to manufacturing and fundamental device-physics issues, there is still a challenging task to characterize important device parameters (e.g., L_g and gate capacitance C_g) of nanoscale MOSFETs using conventional extraction methods (top-down approaches). For example, the applicability of conventional effective channel length L_{eff} extraction methods [29][30] is questioned because of the non-ohmic gate-underlap [31]. Moreover, the geometry-dependent parasitics associated with the 3-D topography of nonplanar devices [32] may result in difficulty in the observation of intrinsic C_g by traditional C–V based measurements. Therefore, the feasibility of using the mesoscopic phenomena (buttom-up approaches) to determine important device parameters for nanoscale MOSFETs merits investigation.

1.2 Organization

This dissertation includes six chapters.

In Chapter 1, the background and the motivation of this thesis are reviewed.

In Chapter 2, we conduct a systematic comparison of carrier transport between overlapped and non-overlapped multiple-gate SOI MOSFETs (MuGFETs). The classical current-voltage and mesophysical characteristics have been investigated for devices with effective channel length L_{eff} = 50 to 60 nm and fin width W_{fin} = 5 to 25 nm at T = 300 to 56 K. Several mesophysical characteristics, including quantum-mechanical confinement effects [12][13], quantum-mechanical interference effects [33], single-electron effects [34], variable range hopping conductance [25] and universal conductance fluctuations [35], are systematically examined. In addition, a new approach of L_{eff} extraction is developed based on the quantum-mechanical interference effects.

In Chapter 3, we further demonstrate controlled single-electron effects in the non-overlapped MuGFETs [34] through a comprehensive investigation for the observed single-electron effects. Then, we systematically present single-electron effects for devices with various gate length (L_g), fin width (W_{fin}), gate bias (V_{GS}), body doping (N_B) and temperature [36]. The impact of access resistances [23], the estimation of gate-dot coupling strength [37] and phenomena of split-peak separations [38] are discussed. Besides, we demonstrate that the gate capacitance as well as source/drain capacitance can be extracted with an aF-scale resolution by single-electron effects.

In Chapter 4, we report a generalized temperature-dependent channel backscattering extraction method that can self-consistently determine the temperature sensitivity of low-field mobility (μ_0) and the critical length (l) in nanoscale MOSFETs [39]-[40]. The validity of our method for the process monitoring purpose is assessed based on various types of devices: high vs. low body-doping, HfO_2 vs. SiO_2 dielectric,

and unstrained vs. uniaxially strained devices. Through the extracted channel backscattering coefficients, we investigate the impacts of the Coulomb scattering, the uniaxial strain, the self-heating effect and the floating-body effect on ballistic efficiency. Finally, we propose that the drain current variation can be suppressed through enhanced ballistic efficiency.

In Chapter 5, we systematically examine the gate tunneling current induced $C-V$ distortion from measurements to simulations. Through the BSIM4-based macro model, different mechanisms of $C-V$ distortion can be characterized for short and long channel devices. Then, we investigate the validity of the concept of intrinsic input resistance [41] in the characterization of the distributed channel RC effects [42]. Finally, we assess the feasibility of using the intrinsic input resistance approach for the inversion $C-V$ reconstruction [43].

Chapter 6 summarizes essential research results and contributions of this dissertation work.

References

[1] International Technology Roadmap for Semiconductors, 2007, [Online]. Available: http://www.itrs.net/Links/2007ITRS/Home2007.htm.

[2] R. Chau, B. Boyanov, B. Doyle, M. Doczy, S. Datta, S. Hareland, B. Jin, J. Kavalieros, and M. Metz, "Silicon nano-transistors for logic applications," *Physica E: Low-dimensional Systems and Nanostructures*, vol. **19**(1–2), pp. 1–5, July 2003.

[3] Z. Krivokapic, C. Tabery, W. Maszara, Q. Xiang, and M.-R. Lin, "High performance 45 nm CMOS technology with 20 nm multi-gate devices" *2003 Int. Conf. Solid State Devices Materials,* pp. 760–61, 2003

[4] F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-X. Chung, H.-W. Chen, C.-C. Huang, Y.-C. Yeo, Y.-M. Li, J.-W. Lee, P. Chen, M.-S. Liang, and C. Hu, "5nm-Gate Nanowire FinFET," *Symp. VLSI Tech. Dig.*, pp. 196–197, June 2004.

[5] H.-S. Philip Wong, "Beyond the conventional transistor," *IBM J. of Research and Development*, vol. **46**(2–3), pp. 133–168, 2002.

[6] M. Fukuma, "New Frontiers of Sub-100nm VLSI Technology - Moving toward Device and Circuit Co-design," *Symp. VLSI Tech. Dig.*, pp. 4–5, 2000.

[7] K. J. Yang and C. Hu, "MOS Capacitance Measurements for High-Leakage Thin Dielectrics," *IEEE Trans. on Electron Devices*, vol. **46**(7), pp.1500–1501, July 1999.

[8] S.-H. Lo, D.A. Buchanan, Y. Taur, and W. Wang, "Quantum mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's," *IEEE Electron Device Letters*, vol. **18**(5), pp. 209–211, May 1997.

[9] S.-W. Lee, "A capacitance-based method for experimental determination of metallurgical channel length in submicron LDD MOSFET's," *IEEE Trans. on Electron Devices*, vol. **41**(3), pp. 403–412, Mar. 1994.

[10] C.-L. Huang, J.V. Faricelli, and N.D. Arora, "A new technique for measuring MOSFET inversion layer mobility," *IEEE Trans. on Electron Devices*, vol. **40**(6), pp. 1134–1139, June 1993.

[11] A. Koukab, A. Bath, and E. Losson, "An improved high-frequency C–V method for interface state analysis on MIS structures," *Solid-State Electron.*, vol. **41**(4), pp. 634–641, 1997.

[12] J.-P. Colinge, A.J. Quinn, L. Floyd, G. Redmond, J.C. Alderman, W. Xiong, C.R. Cleavelin, T. Schulz, K. Schruefer, G. Knoblinger, and P. Patruno,

"Low-temperature electron mobility in Trigate SOI MOSFETs," *IEEE Electron Device Letters*, vol. **27**(2), pp. 120–122, Feb. 2006.

[13] J.-P. Colinge, W. Xiong, C.R. Cleavelin, T. Schulz, K. Schrufer, K. Matthews, and P. Patruno, "Room-Temperature Low-Dimensional Effects in Pi-Gate SOI MOSFETs," *IEEE Electron Device Letters*, vol. **27**(9), pp. 775–777, Sept. 2006.

[14] A. Ohata, A. Toriumi, and J. Koga, "A study of quantum interference fluctuations in deep sub-μm MOSFET's under cryogenic conditions", *IEEE Trans. on Electron Devices*, vol. **41**(11), pp. 2107–2111, Nov. 1994.

[15] M. Cahay and S. Bandyopadhyay, "Semiconductor quantum devices," *IEEE Potentials*, vol. **12**(1), pp. 18–23, Feb. 1993.

[16] M.J. Gilbert and D.K. Ferry, "Quantum interference in fully depleted tri-gate quantum-wire transistors-the role of inelastic scattering," *IEEE Trans. on Nanotechnology*, vol. **4**(5), pp. 599–604, Sept. 2005.

[17] H. Ueno, M. Tanaka, K. Morikawa, T. Takahashi, M. Miura-Mattausch, and Y. Omura, "Origin of transconductance oscillations in silicon-on-insulator metal-oxide-semiconductor field-effect transistors with an ultrathin 6-nm-thick active Si layer," *J. Applied Physics*, vol. **91**(8), pp. 5360–5364, Apr. 2002.

[18] P.W. Anderson, "Absence of Diffusion in Certain Random Lattices," *Phys. Rev.*, vol. **109**(5), pp. 1492–1505, 1958.

[19] K.K. Likharev, "Single-Electron Devices and Their Applications", *Proceedings of The IEEE*, vol. **87**(4), pp.606–632, April 1999.

[20] I.G. Neizvestnyi, O.V. Sokolova, and D.G. Shamiryan, "Single electronics," *Russian Microelectronics*, vol. **28**(2), pp. 67–88, 1999.

[21] U. Meirav and E.B. Foxman, "Single-electron phenomena in semicoductors," *Semicond. Sci. Technol.*, vol. **11**, pp. 255–284, 1996.

[22] F. Boeuf, X. Jehl, M. Sanquer and T. Skotnicki, "Controlled Single-Electron Effects in Nonoverlapped Ultra-Short Silicon Field Effect Transistors," *IEEE Trans. on Nanotechnology*, vol. **2**(3), pp.144–148, Sept. 2003.

[23] X. Jehl, M. Sanquer, G. Bertrand, G. Guégan, S. Deleonibus, and D. Fraboulet "Silicon Single Electron Transistors With SOI and MOSFET Structures: The Role of Access Resistances," *IEEE Trans. on Nanotechnology*, vol. **2**(4), pp.308–313, Dec. 2003.

[24] L. Zhuang, L. Guo, and S. Y. Chou, "Silicon single-electron quantum-dot transistor switch operating at room temperature," *Appl. Phys. Letters*, vol. **72**(10), pp.1205–1207, March 1998.

[25] K. Natori, "Ballistic metal-oxide-semiconductor field effect transistor," *J. Appl. Phys.*, vol. **76**(8), pp. 4879–4890, Oct. 1994.

[26] M.S. Lundstrom, "Elementary scattering theory of the Si MOSFET," *IEEE Electron Device Letters*, vol. **18**(7), pp. 361–363, July 1997.

[27] M.S. Lundstrom, "On the mobility versus drain current relation for a nanoscale MOSFET," *IEEE Electron Device Letters*, vol. **22**(6), pp. 293–295, June 2001.

[28] M.-H. Liao, C.-W. Liu, Lingyen Yeh, T.-L. Lee, and M.-S. Liang, "Gate width dependence on backscattering characteristics in the nanoscale strained complementary metal-oxide-semiconductor field-effect transistor," *Appl. Phys. Letters*, vol. **92**(6), p. 063506, Feb. 2008.

[29] D.J. Mountain, "Application of electrical effective channel length and external resistance measurement techniques to a submicrometer CMOS process," *IEEE Trans. on Electron Devices*, vol. **36**(11), pp. 2499–2505, Nov. 1989.

[30] G.J. Hu, C. Chang, and Y.-T. Chia, "Gate-voltage-dependent effective channel length and series resistance of LDD MOSFET's," *IEEE Trans. on Electron*

Devices, vol. **34**(12), pp. 2469–2475, 1987.

[31] J.G. Fossum, M.M. Chowdhury, V.P. Trivedi, T.-J. King, Y.-K. Choi, J. An, and B. Yu, "Physical insights on design and modeling of nanoscale FinFETs," *IEDM Tech. Dig.*, pp. 29.1.1–29.1.4, 2003.

[32] W. Wu and M. Chan, "Analysis of Geometry-Dependent Parasitics in Multifin Double-Gate FinFETs," *IEEE Trans. on Electron Devices*, vol. **54**(4), pp. 692–698, April 2007.

[33] W. Lee and P. Su, "A Comparative Study of Carrier Transport for Overlapped and Non-overlapped Multiple-Gate SOI MOSFETs," *IEEE Trans. on Nanotechnology*, 2009, to be published.

[34] W. Lee, P. Su, H. Chen, C. Chang, K. Su, S. Liu, and F. Yang, "An Assessment of Single-Electron Effects in Multiple-Gate SOI MOSFETs with 1.6-nm Gate Oxide near Room Temperature," *IEEE Electron Device Letters*, vol. **27**(3), pp. 182–184, March 2006.

[35] G. Wirth, U. Hilleringmann, J. T. Horstmann, and K. Goser, "Mesoscopic transport phenomena in ultrashort channel MOSFETs," *Solid-State Electronics*, vol. **43**(7), pp. 1245–1250, July 1999.

[36] W. Lee and P. Su, "Single-electron effects in non-overlapped multiple-gate silicon-on-insulator metal-oxide-semiconductor field-effect transistors," *Nanotechnology*, vol. **20**, p. 065202, Feb. 2009.

[37] Y.-M. Wan, K.-D. Huang, C.-L. Sung, and S.-F. Hu, "Transport properties of ultra thin oxide gated Si SET near room temperature," *Proc. 5th IEEE Conf. Nanotechnology*, vol. **2**, pp.750–753, July 2005.

[38] F.R. Waugh, M.J. Berry, D.J. Mar, and R.M. Westervelt, "Single-electron charging in double and triple quantum dots with tunable coupling," *Phys. Rev. Letters*, vol.

75(4) pp.705–708, July 1995.

[39] W. Lee and P. Su, "Investigation of Channel Backscattering Characteristics in Nanoscale Uniaxial Strained PMOSFETs," *IEEE Trans. on Nanotechnology*, 2009, to be published.

[40] W. Lee and P. Su, "Investigation of Channel Backscattering Characteristics for Nanoscale SOI MOSFETs Using a New Temperature-Dependent Method," *Proc. 2008 IEEE Int. SOI Conf.,* New York, USA, pp. 73–74, Oct. 2008.

[41] X. Jin, J.-J. Ou, C.-H. Chen, W. Liu, M. J. Deen, P. R. Gray, and C. Hu, "An Effective Gate Resistance Model for CMOS RF and Noise Modeling", *IEDM Tech. Dig.*, p.961, 1998.

[42] D.W. Barlage, J.T. O'Keeffe, J.T. Kavalieros, M.M. Nguyen, and R. S. Chau, "Inversion MOS Capacitance Extraction for High-Leakage Dielectrics Using a Transmission Line Equivalent Circuit," *IEEE Electron Device Letters*, vol. **21**(9), pp.454–456, Sept. 2000.

[43] W. Lee, P. Su, K. Su, C. Chiang, and S. Liu, "Investigation of Anomalous Inversion C-V Characteristics for Long-Channel MOSFETs with Leaky Dielectrics: Mechanisms and Reconstruction," *IEEE Trans. on Semiconductor Manufacturing*, vol. **21**(1), pp. 104–109, Feb. 2008.

Chapter 2

Comparison of Carrier Transport for Overlapped and Non-overlapped Multiple-Gate SOI MOSFETs

2.1 Introduction

Multiple-gate silicon-on-insulator (SOI) MOSFET (MuGFET) structures provide superior electrostatic integrity needed for complementary metal-oxide-semiconductor (CMOS) scaling entering the deca-nanometer regime [1]. The benefits of MuGFET have been extensively investigated regarding issues of short-channel effects (SCE), leakage current, threshold voltage (V_T) fluctuations, mobility, and so on [2].

For MuGFET design, source/drain engineering is crucial because of the parasitic drain/source resistance [3] and the parasitic fringing/overlap capacitance that may limit circuit performance [4]. Two options in the source/drain engineering are the overlapped structure with light-doping drain/source (LDD/LDS) and the non-overlapped structure. The LDD/LDS implantation has been widely used in state-of-the-art CMOS devices for suppressing source and drain resistances. On the other hand, transistor optimization for peak circuit performance within leakage current constraints (i.e., minimum *CV*/*I* delay) may dictate the non-overlapped gate to source/drain structure to minimize the fringing/overlap capacitance. Whether the various source/drain engineering will impact the carrier transport in nanoscale MuGFETs merits examination. In this chapter, we conduct a systematic comparison of carrier transport between overlapped and non-overlapped MuGFETs. The classical current-voltage and mesophysical characteristics have been investigated for devices with effective channel length L_{eff} = 50 to 60 nm at T = 300 to 56 K.

2.2 Overlapped and non-overlapped device structures

The process flow for fabricating MuGFETs is similar to that reported in [32]. Fig. 2.1(a) shows a schematic view of the MuGFET investigated in this study [31]. Our devices were fabricated on SOI wafers using standard CMOS optical lithography [5]. The Si-body thickness, H_{fin}, was thinned down to about 40 nm by thermal oxidation. The fin-width, W_{fin}, was defined by wet etching. After W_{fin} was developed, the Si-body fin was doped with BF_2 implantation and annealed. Using optical lithography and anisotropic reactive ion etching, the gate length, L_g, was defined. Note that the LDD/LDS implantation was performed for the overlapped structure (Fig. 2.1(c)) and was skipped for the non-overlapped structure (Fig. 2.1(b)) before developing the composite spacer of silicon oxide and nitride. Finally, heavily-doped N^+ source/drain was made. In this study, we compare these two types of devices based on the same effective source-drain length L_{eff}.

2.3 Experimental comparison

2.3.1 Classical characteristics

Current-voltage measurements (I_{DS}–V_{GS}) at V_{DS} = 50 mV under T = 300 to 56 K were performed with a 25-mV V_{GS} step for the overlapped Device 1 with W_{fin} = 25 nm and L_g = 80 nm (Fig. 2.2), and for the non-overlapped Device 2 with W_{fin} = 25 nm and L_g = 30 nm (Fig. 2.3). Fig. 2.2 shows that the subthreshold swing S for the overlapped Device 1 decreases with temperature. We have confirmed that the S–T characteristic follows the Boltzmann law $S = n(k_BT/q)\ln(10)$ with the body effect coefficient $n \approx 1.16$. The linear temperature dependence of S is a feature of fully depleted SOI [8], and has also been observed in tri-gate SOI MOSFETs [13].

For the non-overlapped Device 2, however, the linear temperature dependence of S can only be seen when temperature is larger than 223 K (Fig. 2.3). For temperature

below 223 K, S is a constant and does not follow the Boltzmann law. This suggests that for the non-overlapped Device 2, tunneling current dominates the fundamental limitation of leakage current instead of the thermal current [12]. We have noted that similar S behavior has been reported at $T < 100$ K for the planar non-overlapped NMOSFET in [12]. It implies that the leakage current associated with thermionic emission is suppressed in our MuGFET.

The insensitive temperature dependence of I_{DS} can also be found in the strong inversion region for the non-overlapped Device 2 (Fig. 2.3). In contrast to that of the overlapped Device 1 (Fig. 2.2), the I_{DS} for $V_{GS} > 0.6$ V is nearly independent on temperature. These results indicate that carrier transport in the strong inversion region is determined by the phonon-limited mobility for the overlapped Device 1, but not for the non-overlapped Device 2.

2.3.2 Mesophysical characteristics

To further compare the carrier transport characteristics for overlapped and non-overlapped devices, we have investigated channel conductance ($G_{DS} = I_{DS}/V_{DS}$) with low V_{DS}. Fig. 2.4 shows the measured G_{DS} versus V_{GS} characteristics for the overlapped Device 3 with W_{fin} = 10 nm and L_g = 60 nm. Significant G_{DS} fluctuations can be seen at T = 56 K (Fig. 2.4(a)). Similar G_{DS} fluctuations have been reported in [6] and attributed to the intersubband scattering. While the number of populated subbands increases with increasing V_{GS}, the intersubband scattering also increases with each new subband [7]. In other words, when V_{GS} increases, the G_{DS} increases due to new populated subbands and then decreases due to the mobility reduction (i.e., the increase of intersubband scattering). Thus, fluctuations can be seen in the G_{DS}–V_{GS} characteristics. We have noted that the G_{DS} fluctuations almost occur at the same V_{GS}, such as the spike at V_{GS}-V_T = 0.425 V (Fig. 2.4(a)). We have also noted that for the wider overlapped devices (i.e.,

Device 1) with negligible subband splitting, the G_{DS} fluctuations can not be found.

One important criterion to observe the intersubband scattering effect is that the qV_{DS} and k_BT are not significantly larger than the subband energy split ΔE [7]. It is worth noting in Fig. 2.4(a) that the G_{DS} fluctuations can be observed at V_{DS} = 50 mV under T = 56 K. Considering the voltage drop across the access resistances (i.e., source/drain resistances, contact resistance and back-end metal resistance), the effective qV_{DS} over the channel and therefore ΔE may be about 20 to 30 meV. This is also consistent that with the observed G_{DS} fluctuations at V_{DS} = 1 mV under T = 223 K shown in Fig. 2.4(b). Besides, we have noted in our process that the final minimum W_{fin} at the channel center is smaller than the mask-defined 10-nm W_{fin} (final minimum W_{fin} ~5 nm) due to over etching [31].

An important signature for intersubband scattering is that conductance reductions (i.e., mobility reduction) occur as V_{DS} increases [6]. This is because the drain bias forces electrons to jump from higher to lower subbands, and thus enhances intersubband scattering and reduces the carrier mobility [7]. It is worth noting that the reductions in G_{DS} due to mobility reduction can also be observed at V_{DS} = 1 mV when temperature increases from 56 to 223 K. Similar V_{DS} and temperature dependence in G_{DS} has also been observed for trigate SOI MOSFETs in [6]-[7].

For the non-overlapped Device 2 in the high V_{GS} regime, the G_{DS} increases with V_{DS} and temperature as can be observed in Fig. 2.5(a) and Fig. 2.5(b), respectively. Such V_{DS} and temperature dependence of G_{DS} is completely opposite to that of the overlapped Device 3 (Fig. 2.4) and can not be ascribed to the intersubband scattering effect. In addition, Fig. 2.5 also shows interesting fluctuations with negative differential resistance in the G_{DS}. Although the G_{DS} fluctuations in Fig. 2.5 were observed in the same measurement conditions as Fig. 2.4, one can safely state that it does not result

from the intersubband scattering. In the next section, we shall give more discussions for the anomalous G_{DS} behavior of the non-overlapped Device 2.

2.4 Interpretation

2.4.1 Intersubband scattering effects

As described above, the V_{DS} and temperature dependence of G_{DS} in Fig. 2.5 for the non-overlapped Device 2 is completely opposite to characteristics of intersubband scattering effect. Therefore, the G_{DS} fluctuations in Fig. 2.5 can not be ascribed to the intersubband scattering effect. Besides, we have also noted that for the overlapped Device 1 with the same W_{fin} (i.e., W_{fin} = 25 nm), the G_{DS} fluctuations can not be found.

2.4.2 Single-electron effects

Coulomb blockade is expected to be important as the charging energy e^2/C_g of the device becomes large [18][19]. With scaling of devices, it is expected that Coulomb blockade oscillation (CBO) occurs in I_D–V_{GS} characteristics [20]. Although the multiple-gate SOI structure with adequate source/drain engineering presents a very promising scheme to build room-temperature SETs [21], we have confirmed in Fig. 2.5 that the physical mechanism described for the non-overlapped device is not due to the CBO. Regarding single-electron effects in the non-overlapped multiple-gate device, we have presented our research results in Chapter 3.

If the G_{DS}–V_{GS} characteristics shown in Fig. 2.5(a) were due to CBO, the V_{GS} period of CBO can be related to the gate capacitance by e/C_g as well as gate effective area (A_{eff}) by $C_g = A_{eff} \times \varepsilon_{SiO2}/EOT$. Since the effective oxide thickness (EOT) is about 2.6 nm for our device, from $e/C_g \approx 75$ mV (Fig. 2.5(a)), A_{eff} is estimated ~1.6×10^{-12} cm^2 for our MuGFET. However, such A_{eff} is about 15 times smaller than $2H_{fin}L_g = 2.4\times10^{-11}$ cm^2. This indicates that the G_{DS} oscillations in Fig. 2.5(a) can not be attributed to CBO. Besides, the G_{DS} oscillations in Fig. 2.5(a) become significant with increasing G_{DS},

which is not the signature of CBO.

2.4.3 Variable range hopping conductance

Charged centers in the oxide, interfaces or bulk Si can result in random potential fluctuation [22][23]. In the limit of zero temperature, electron transport is characterized by hopping certain charged centers. When the energy of carriers is increased with temperature or V_{DS}, hopping processes determined by the activation energy may change. In other words, conductance fluctuations may change with temperature or V_{DS}. This phenomenon is an origin of the variable range hopping (VRH) itself. In our experimental results, however, the anomalous conductance fluctuations are present at the same (V_{GS}-V_T) values for the same device with various temperature and V_{DS} (Fig. 2.9). Besides, if electron transport is limited by the VRH, the tunneling conductance must be less than e^2/h [22][23]. That the G_{DS} in Fig. 2.5 is several times e^2/h may exclude the possibility of the VRH. Furthermore, if we assume the anomalous conductance fluctuations are caused by trapping and de-trapping mechanisms, a dependence of fluctuations on the measurement frequency is expected. This could not be observed in our AC G_m measurements in Fig. 2.16 to 2.18.

2.4.4 Universal conductance fluctuations

Due to the two voltage-controlled potential barriers, the universal conductance fluctuations (UCF) [24], as have been predicted by Lee and Stone [25] for disordered systems, are also not expected to be responsible for our observed conductance fluctuations. In addition, to the best our knowledge, the UCF are easily smeared by temperature and may not be easily observed for our devices at $T > 4.2$ K [26].

2.4.5 Quantum interference effects

Fig. 2.6 shows the electronic potential calculated using ISE device simulation [16] for our non-overlapped device. The non-overlapped gate to source/drain regions act

as the voltage-controlled potential barriers along the channel. Therefore, carrier transport from source to drain is significantly influenced by the barriers as illustrated in Fig. 2.6: directly tunneling (I_a), thermally-associated tunneling (I_b), and thermionic emission (I_c). The contribution of these three mechanisms to I_{DS} depends on V_{GS} and temperature. For high V_{GS}, I_a is dominant. With decreasing V_{GS}, increased electronic potential diminishes I_a, and thus I_b and I_c become important. In other words, I_{DS} in the subthreshold region results mainly from I_b and I_c for the non-overlapped device. It is worth noting that carrier transport by I_c requires more thermal energy and may be suppressed under low temperature.

Figure 2.7 shows the temperature sensitivity of I_{DS} ($\partial\log(I_{DS})/\partial T$) vs. V_{GS} characteristics extracted from Fig. 2.2 and Fig. 2.3 under high and low temperatures. For the non-overlapped device in the strong inversion region, the insensitive temperature dependence manifests the importance of I_a. On the other hand, the negative temperature dependence for the overlapped device in the strong inversion region indicates phonon scattering. In addition, it can be noted in Fig. 2.7(a) that $\partial\log(I_{DS})/\partial T$ significantly increases with decreasing V_{GS} for both overlapped and non-overlapped devices. This suggests that in the high temperature regime the subthreshold current of the non-overlapped device is dominated by I_c, similar to the overlapped device. When temperature decreases, however, the thermionic emission I_c is suppressed and the I_b component with weak temperature dependence becomes dominant. In other words, the suppression of I_c under low temperature is the main reason of S saturation for the non-overlapped device. It should be noted that such mechanism of S saturation is different from lateral tunneling through the channel, as presented for ultra-short devices in [12] and [17].

Figure 2.6 also shows an equivalent quantum well under the gate in the

non-overlapped device [12]. It is worth noting that the height of the voltage-controlled potential barriers in the non-overlapped regions increases with V_{GS}. The consequence is the plausibility of electron-wave confined between the barriers. When the length of the quantum well, d, is smaller than the inelastic-scattering (e.g., phonon scattering) length, the phase-coherent electron wavefunction over the entire channel as well as quantum interference between coherent electron waves occur. The quantum interference enhances the electron backscattering probability [9]-[10] and thereby reduces the conductivity expected classically. Such quantum correction to the conductivity is the weak localization effect [9]-[10] and logarithmically dependent on temperature as $\Delta\sigma = (pe^2/\pi h)\ln(T)$, where the value of p depends on the scattering process. When T = 56 K, the carriers at V_{DS} = 50 mV experience more heating (more phonon scattering) and thus less localization effect than those at V_{DS} = 1 or 2 mV. Therefore, the G_{DS} measured at V_{DS} = 50 mV is larger than that at V_{DS} = 1 or 2 mV (Fig. 2.5). From the G_{DS} data at V_{DS} = 2 mV under T = 56 K and 223 K in Fig. 2.5, we can estimate that $p \approx 1$, which is close to the results in [11] for the 2DEG in Si MOSFETs.

The quantum-mechanical interference for an electron wave passing through a quantum well also results in oscillating transmission probability, Tr, as [14][31]

$$Tr = \left| \frac{\exp(-ik_1 d)}{\cos(k_2 d) - i(\omega/2)\sin(k_2 d)} \right|^2, \tag{1}$$

where $\omega = k_1/k_2 + k_2/k_1$, k_1 and k_2 are the wave vectors in the non-overlapped region and in the quantum well, respectively. The wave vectors are determined from

$$k_1 = \sqrt{2m(E - eV_p)}/\hbar, \tag{2}$$

$$k_2 = \sqrt{2m(E - eV_c)}/\hbar, \tag{3}$$

where m and E are the effective mass and energy of the electron. Fig. 2.8 shows the calculated Tr for the quantum well in Fig. 2.6. The values of d and (E-eV_p) used in Fig.

2.8 are based on our experiments. It is worth noting that the *Tr* oscillation becomes obvious with increasing V_{GS} as well as the depth of the quantum well. From the *Tr* calculation based on d = 30 nm and (E-eV_p) = 0~5 meV (Fig. 2.8), we can observe three transmission maxima due to constructive interference (i.e., Tr = 1) at $V_{GS} \approx$ 0.2, 0.43 and 1 V. When (E-eV_p) increases, we observed smaller *Tr* oscillations and shifts in the corresponding transmission maximum. In other words, the electron energy distribution may result in group-like *Tr* oscillations as shown in the Groups 1 to 3 of Fig. 2.8. We found that such group-like fluctuations can also be seen in the G_m' ($G_m' = \partial G_m/\partial V_{GS}$, $G_m = \partial I_{DS}/\partial V_{GS}$) characteristics in Fig. 2.9 as well as in the G_{DS} characteristics shown in Fig. 2.5(a). We have noted that nearly every peak in G_m' (Fig. 2.9) can correspond to the peak in G_{DS} (Fig. 2.5(a)). It is worth noting that the G_m' oscillation of Group 3 is more significant and wider than that of Groups 1 and 2, which is consistent with the simulation results in Fig. 2.8. Remind that both the potential barrier height in Fig. 2.6 and G_{DS} fluctuations in Fig. 2.5 and Fig. 2.9 increase with V_{GS}. For devices with the same size, similar G_m' oscillations can also be observed and have been presented in our previous study [15].

2.5 Application to effective channel length extraction

The physical mean of (1) can be understood from *Tr* versus *E* characteristics in Fig. 2.10. For a fixed V_{GS}, the perfect transmission (Tr = 1) occurs at specific values of E, whcih can be predicted by [14]

$$E_n - eV_c = \frac{n^2\pi^2\hbar^2}{2md^2}, \tag{4}$$

where n is any integer corresponding to the scattering states E_n. Since the wavevector k is defined as $k \equiv 2\pi/\lambda$ for a wave of wavelength λ, from (3) and (4) we can observed

$$d = n\frac{\lambda}{2}. \tag{5}$$

(5) means that the perfect transmission of carriers occur when the width of the quantum well d is a half integer multiple of the wavelength of electrons. As λ is taken as Fermi wavelength (λ_F), the wavelength of electrons can be estimated by $\lambda = (4\pi/n_s)^{0.5}$ for the 2DEG [27][28], where the inversion carrier density $n_s = (C_g/eA_{eff})(V_{GS}-V_T)$. Since the gate capacitance per area $C_g/A_{eff} = \varepsilon_{SiO2}/EOT$ ($\approx 1.33\times10^{-6}$ F/cm^2), the perfect transmission is observed as [8][9]

$$V_{GS} - V_T = \frac{\pi e n^2 EOT}{d^2 \varepsilon_{SiO2}}. \tag{6}$$

Fig. 2.11 shows the calculated λ_F versus (V_{GS}-V_T) characteristics and the predicted maximum transmission for d = 30 nm by (5). We have noted that the perfect transmissions are predicted at 0.17, 0.38 and 0.68 V for n = 2 to 4, respectively, which are fairly corresponding to the simulated *Tr* oscillations in Fig. 2.10 and the Groups 1 to 3 of the measured oscillations in Fig. 2.9. Besides, the proportion of n^2 in (6) explains the dense *Tr* oscillations. For d = 40 nm, the maximum transmission has also been predicted in Fig. 2.11. Due to the inverse proportion of d^2 in Eq. (6), the density of the predicted interference occurrence increases. Such result is consistent with the simulated *Tr* oscillations in Fig. 2.13 and can explain the measured oscillations in Fig. 2.14. Fig. 2.14 shows the measured $\partial G_m/\partial V_{GS}$ versus (V_{GS}-V_T) characteristics for the Device 6 with L_g = 40 nm (i.e., d = 40 nm). We have noted that the observed $\partial G_m/\partial V_{GS}$ fluctuations can be predicted by the model (Fig. 2.11) for n = 4 to 6 fairly well.

(5) and (6) reveal an opportunity to extract effective channel length (i.e., d) based on the quantum interference measurement. For a given value of (V_{GS}-V_T) at which quantum interference occurs, d can than be calculated from (5) and (6). To clearly identify what the (V_{GS}-V_T) value occurs enhanced G_{DS}, the $\partial G_m/\partial V_{GS}$ characteristics may

be helpful to be analyzed. Fig. 2.15 shows an illustration of the quantum interference effect on G_{DS}, G_m and $\partial G_m/\partial V_{GS}$. When constructive interference occurs, the enhanced transmission probability is responsible for the enhanced G_{DS}, and results in the G_m humps and peaks in the corresponding $\partial G_m/\partial V_{GS}$ vs. V_{GS} characteristic. Note that the valley in $\partial G_m/\partial V_{GS}$ occurs when the G_{DS} as well as the transmission probability is enhanced, and can be an index of the quantum interference.

In addition, we have also employed the AC G_m measurement to exclude the background noise effects on the $\partial G_m/\partial V_{GS}$ characteristics. Fig. 2.16 shows the AC G_m measurement used in this work. We found that by tuning the AC small signal to larger values (~20 mV), the short-range fluctuation resulted from background noises (e.g., low-frequency noise, thermal noise, Coulomb blockade oscillation…) can be averaged out and suppressed. Therefore, the long-range $\partial G_m/\partial V_{GS}$ fluctuation caused by the quantum interference can be clearly observed. In other words, the AC measurement has a better resolution in the characterization of quantum interference. Fig. 2.17 shows AC and DC measurement results of the $\partial G_m/\partial V_{GS}$ for the non-overlapped Device 4 with L_g = 30 nm and W_{fin} = 25 nm. It is worth noting that not only the main $\partial G_m/\partial V_{GS}$ valleys at n = 1, 3 and 4 can be reproduced for AC and DC measurements, but also the absent peak at n = 2 in the DC measurement can be clearly observed by the AC measurement. To further confirm the validity of our measurements, we performed the same AC and DC measurements on the Device 5 with the same size. As shown in Fig. 2.18, the main $\partial G_m/\partial V_{GS}$ valleys for n = 1 to 4 can be clearly observed from our measurements.

Based on both AC and DC measurements, we can determine the (V_{GS}-V_T) value at which quantum interference occurs for each n. The L_{eff} can then be determined from (6). The extracted L_{eff} values are about 30 and 27 nm for the Device 4 and 5, respectively. The 3-nm L_{eff} difference may be resulted from the process variations. Fig. 2.19 shows

the extracted L_{eff} for the non-overlapped multiple-gate MOSFETs with L_g = 30 nm and W_{fin} = 25 nm. The V_{GS} dependences of the extracted L_{eff} can be seen in the simulation result and the extracted values. Fig. 2.20 shows the charge density calculated using ISE device simulation [16] for our non-overlapped device. It is worth noting that our extracted L_{eff}, based on the wave nature of electrons, agrees with the simulation result (in Fig. 2.20) that is based on the inversion-layer sheet conductivity. In addition, we have note that for non-overlapped devices, the applicability of conventional L_{eff} extraction methods [29][30] is questioned because of the non-ohmic non-overlapped regions.

2.6 Conclusion

We have conducted a comparative study of carrier transport characteristics for MuGFETs with and without the non-overlapped source/drain structure. For the overlapped devices, we observed Boltzmann law in subthreshold characteristics and phonon-limited behavior in the inversion regime. For the non-overlapped devices, however, we found insensitive temperature dependence of I_{DS} in both subthreshold and inversion regimes. Our low-temperature measurements indicate that the inter-subband scattering may be the dominant carrier transport mechanism for narrow overlapped MuGFETs. For the non-overlapped MuGFETs, the voltage-controlled potential barriers in the non-overlapped regions may give rise to the weak localization effect (conductance reduction) and the quantum interference fluctuations. In addition, we have developed a novel approach to obtain the V_{GS}-dependent L_{eff} for MuGFETs with non-overlapped gate to source/drain structure. The extracted L_{eff}, based on the wave nature of channel electrons, agrees with the simulation result that is based on the inversion-layer sheet conductivity.

References

[1] International Technology Roadmap for Semiconductors, 2007, [Online]. Available: http://www.itrs.net/Links/2007ITRS/Home2007.htm.

[2] N. Collaert, A. De Keersgieter, A. Dixit, I. Ferain, L.-S. Lai, D. Lenoble, A. Mercha, A. Nackaerts, B.J. Pawlak, R. Rooyackers, T. Schulz, K.T. Sar, N.J. Son, M.J.H. Van Dal, P. Verheyen, K. von Arnim, L. Witters, K.D. Meyer; S. Biesemans, and M. Jurczak "Multi-gate devices for the 32nm technology node and beyond," *European Solid-State Device Research*, pp. 143–146, Sept. 2007.

[3] A. Dixit, A. Kottantharayil, N. Collaert, M. Goodwin, M. Jurczak, and K.D. Meyer, "Analysis of the parasitic S/D resistance in multiple-gate FETs," *IEEE Trans. on Electron Devices*, vol. **52**(6), pp. 1132–1140, June 2005.

[4] A. Bansal, B.C. Paul, and K. Roy, "Modeling and optimization of fringe capacitance of nanoscale DGMOS devices," *IEEE Trans. on Electron Devices*, vol. **52**(2), pp. 256–262, Feb. 2005.

[5] F.-L. Yang, H.-Y. Chen, and C.-Y. Chang, "SOI Transistor/Power Scaling and Scaling-Strengthened Strain" *Int. Conf. Solid State Devices and Materials*, pp. 772–773, Sept. 2004.

[6] J.-P. Colinge, A.J. Quinn, L. Floyd, G. Redmond, J.C. Alderman, W. Xiong, C.R. Cleavelin, T. Schulz, K. Schruefer, G. Knoblinger, and P. Patruno, "Low-temperature electron mobility in Trigate SOI MOSFETs," *IEEE Electron Device Letters*, vol. **27**(2), pp. 120–122, Feb. 2006.

[7] J.-P. Colinge, W. Xiong, C.R. Cleavelin, T. Schulz, K. Schrufer, K. Matthews, and P. Patruno, "Room-Temperature Low-Dimensional Effects in Pi-Gate SOI MOSFETs," *IEEE Electron Device Letters*, vol. **27**(9), pp. 775–777, Sept. 2006.

[8] M. Lemme, T. Mollenhauer, W. Henschel, T. Wahlbrink, H. Gottlob, J. Efavi, M.

Baus, O. Winkler, B. Spangenberg, and H. Kurz, “Subthreshold characteristics of p-type triple-gate MOSFETs,” *European Solid-State Device Research*, pp. 123–126, Sept. 2003.

[9] V. Renard, Z.D. Kvon, O. Estibals, J.C. Portal, A.I. Toropov, A.K. Bakarov, and M.N. Kostrikin, “Negative parabolic magneto-resistance induced by electron-electron interaction in two-dimensional electron gas with diffusive transport,” *Physica E*, vol. **22**(1-3), pp. 328–331, 2004.

[10] P.M. Mensz and R.G. Wheeler, “Magnetoconductance due to parallel magnetic fields in silicon inversion layers,” *Phys. Rev. B*, vol. **35**(6), pp. 2844–2853, Feb. 1987.

[11] D.J. Bishop, R.C. Dynes, and D.C. Tsui, “Magnetoresistance in Si metal-oxide-semiconductor field-effect transistors: Evidence of weak localization and correlation,” *Phys. Rev. B*, vol. **26**(2), pp. 773–779, July 1982.

[12] F. Boeuf, T. Skotnicki, S. Monfray, C. Julien, D. Dutartre, J. Martins, A. Mazoyer, P. Palla, R. Tavel, B. Ribot, P. Sondergard, and E. Sanquer, “16 nm planar NMOSFET manufacturable within state-of-the-art CMOSprocess thanks to specific design and optimisation,” *IEDM Tech. Dig.*, pp. 29.5.1–29.5.4, Dec. 2001.

[13] J.-P. Colinge, L. Floyd, A.J. Quinn, G. Redmond, J.C. Alderman, W. Xiong, C.R. Cleavelin, T. Schulz, K. Schruefer, G. Knoblinger, and P. Patruno, “Temperature effects on trigate SOI MOSFETs,” *IEEE Electron Device Letters*, vol. **27**(3), pp. 172–174, Mar. 2006.

[14] D. J. Griffiths, *Introduction to Quantum Mechanics*, Prentice Hall, Upper Saddle River, New Jersey, 1994, p. 60, ISBN 0-13-124405-1.

[15] W. Lee, P. Su, H.-Y. Chen, C.-Y. Chang, K.-W. Su, S. Liu, and F.-L. Yang, “An experimental assessment of quantum interference in uultiple-gate SOI nMOSFETs

with non-overlapped gate to source/drain structure near room temperature," *Proc. IEEE Silicon Nanoelectronics Workshop*, Kyoto, Japan, p. 15, June 2007.

[16] "ISE TCAD Rel. 10.0," *DESSIS*, 2004.

[17] M. Fukuma, "New Frontiers of Sub-100nm VLSI Technology - Moving toward Device and Circuit Co-design," *Symp. VLSI Tech. Dig.*, pp. 4–5, 2000.

[18] K.K. Likharev, "Single-Electron Devices and Their Applications", *Proceedings of The IEEE*, vol. **87**(4), pp.606–632, April 1999.

[19] S.M. Goodnick and J. Bird, "Quantum-effect and single-electron devices," *IEEE Trans. on Nanotechnology*, vol. **2**(4), pp. 368–385, 2003.

[20] F. Boeuf, X. Jehl, M. Sanquer, and T. Skotnicki, "Controlled Single-Electron Effects in Nonoverlapped Ultra-Short Silicon Field Effect Transistors," *IEEE Trans. on Nanotechnology*, vol. **2**(3), pp.144–148, Sept. 2003.

[21] W. Lee, P. Su, H. Chen, C. Chang, K. Su, S. Liu, and F. Yang, "An Assessment of Single-Electron Effects in Multiple-Gate SOI MOSFETs with 1.6-nm Gate Oxide near Room Temperature," *IEEE Electron Device Letters*, vol. **27**(3), pp. 182–184, March 2006.

[22] G. Wirth, U. Hilleringmann, J. T. Horstmann, and K. Goser, "Mesoscopic transport phenomena in ultrashort channel MOSFETs," *Solid-State Electronics*, vol. **43**(7), pp. 1245–1250, July 1999.

[23] A. Ohata, A. Toriumi, and J. Koga, "A study of quantum interference fluctuations in deep sub-μm MOSFET's under cryogenic conditions," *IEEE Trans. on Electron Devices*, vol. **41**(11), pp. 2107–2111, Nov. 1994.

[24] C.P. Umbach, S. Washbun, R.B. Laibowitz, and R.A. Webb, "Magnetoresistance of small, quasi-one-dimensional, normal-metal rings and lines," *Phys. Rev.*, vol. **B30**, pp. 4048-4051, 1984.

[25] P.A. Lee and A. Douglas Stone, “Universal Conductance Fluctuations in Metals,” *Phys. Rev. Letters*, vol. **55**(15), pp. 1622–1625, 1985.

[26] S. Datta, *Electronic Transport in Mesoscopic Systems*, Cambridge University Press, 1995, p. 215.

[27] Y. Omura, K. Kurihara, Y. Takahashi, T. Ishiyama, Y. Nakajima, and K. Izumi, “50-nm channel nMOSFET/SIMOX with an ultrathin 2- or 6-nm thick silicon layer and their significant features of operations,” *IEEE Electron Device Letters*, vol. **18**(5), pp. 190–193, May 1997.

[28] T. Takahashi, M. Miura-Mattausch, and Y. Omura, “Transconductance oscillations in metal-oxide-semiconductor field-effect transistors with thin silicon-on-insulator originated by quantized energy levels,” *Appl. Phys. Letters*, vol. **75**(10), pp. 1458–1460, Sept. 1999.

[29] G.J. Hu, C. Chang, and Y.-T. Chia, “Gate-voltage-dependent effective channel length and series resistance of LDD MOSFET's,” *IEEE Trans. on Electron Devices*, vol. **34**(12), pp. 2469–2475, Dec. 1987.

[30] D.J. Mountain “Application of electrical effective channel length and external resistance measurement techniques to a submicrometer CMOS process,” *IEEE Trans. on Electron Devices*, vol. **36**(11), pp. 2499–2505, Nov. 1989.

[31] W. Lee and P. Su, “A Comparative Study of Carrier Transport for Overlapped and Non-overlapped Multiple-Gate SOI MOSFETs,” *IEEE Trans. on Nanotechnology*, 2009, to be published.

[32] F.-L. Yang, H.-Y. Chen, F.-C. Chen, C.-C. Huang, C.-Y. Chang, H.-K. Chiu, C.-C. Lee, C.-C. Chen, H.-T. Huang, C.-J. Chen, H.-J. Tao, Y.-C. Yeo, M.-S. Liang, and C. Hu, “25nm CMOS Omega FETs,” *IEDM Tech. Dig.*, pp. 255–258, Dec. 2002.

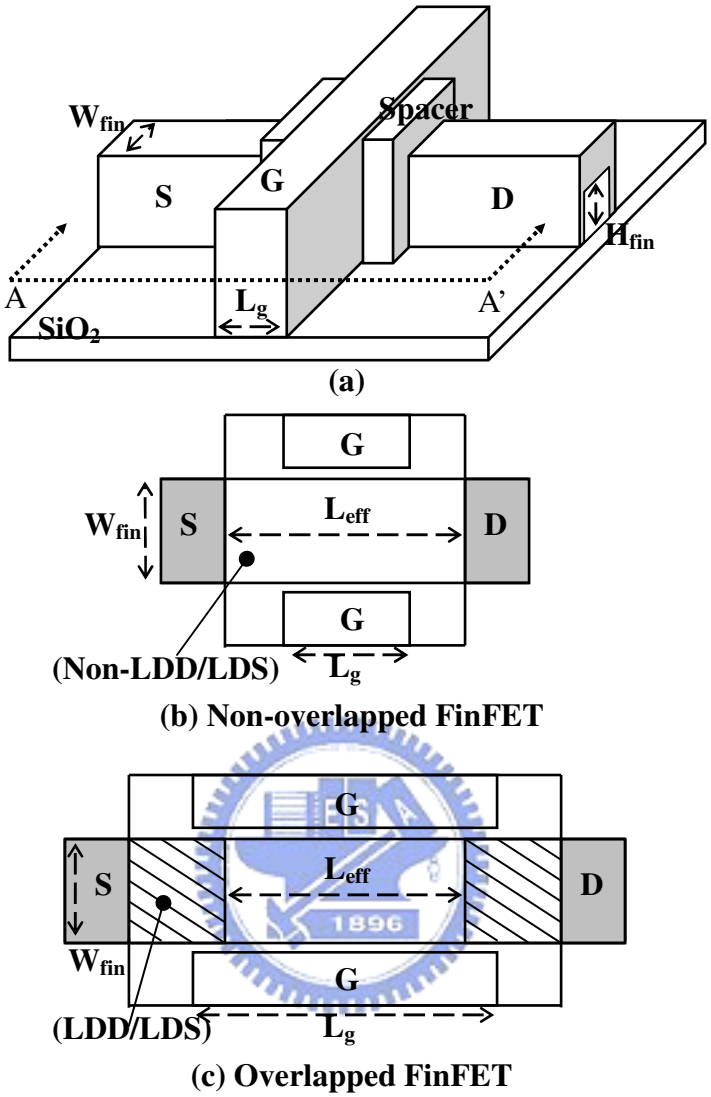


Fig. 2.1. (a) Multiple-gate FinFET SOI structure investigated in this work and its cross-sectional AA' view along the channel direction showing (b) the non-overlapped gate to source/drain structure and (c) the overlapped gate to source/drain structure.

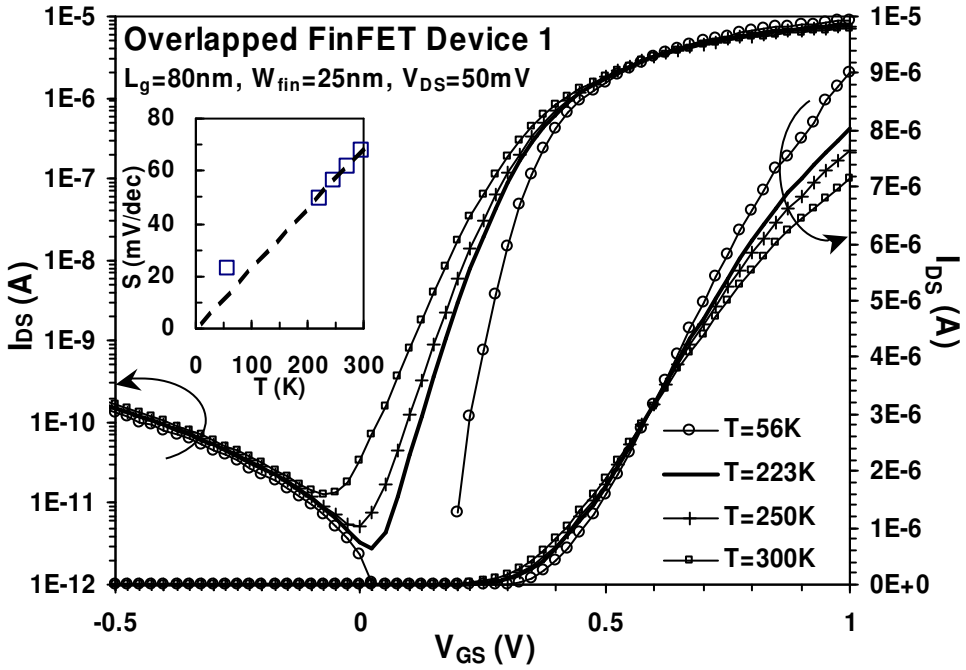


Fig. 2.2. Measured I_{DS} vs. V_{GS} characteristics at V_{DS} = 50 mV under T = 300 to 56 K for the overlapped FinFET Device 1 with W_{fin} = 25 nm and L_g = 80 nm.

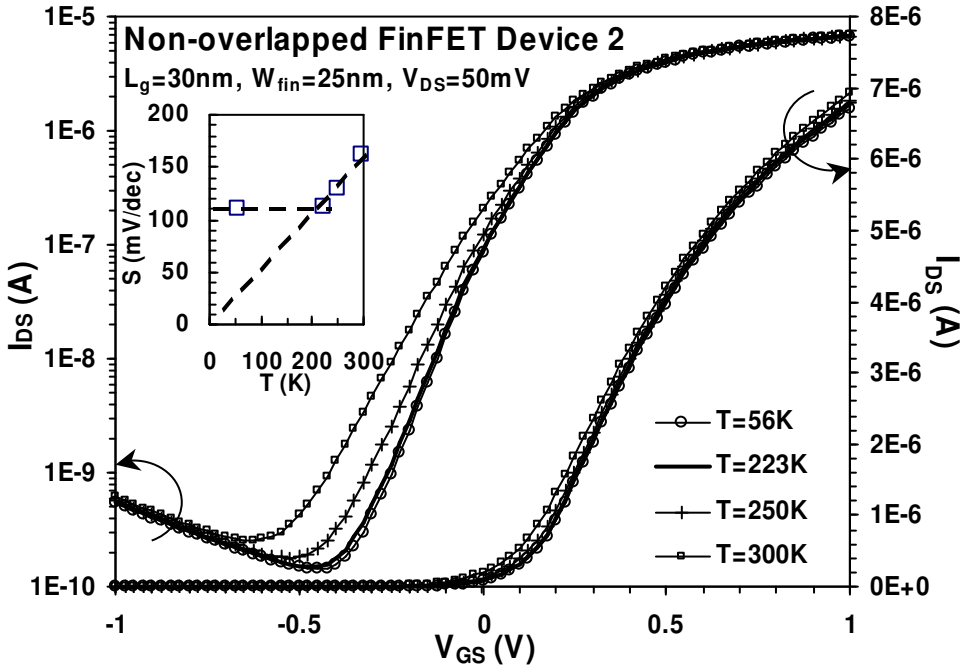


Fig. 2.3. Measured I_{DS} vs. V_{GS} characteristics at V_{DS} = 50 mV under T = 300 to 56 K for the non-overlapped FinFET Device 2 with W_{fin} = 25 nm and L_g = 30 nm.

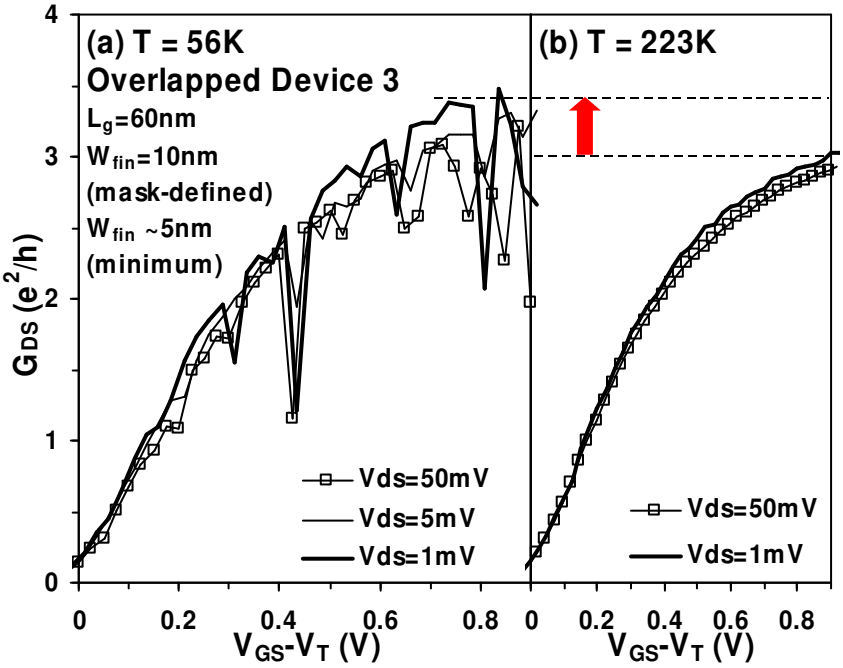


Fig. 2.4. Measured channel conductance (G_{DS}) vs. (V_{GS}-V_T) characteristics for the overlapped Device 3 with L_g = 60 nm and W_{fin} = 10 nm at various V_{DS} under (a) T = 56 K and (b) T = 223 K.

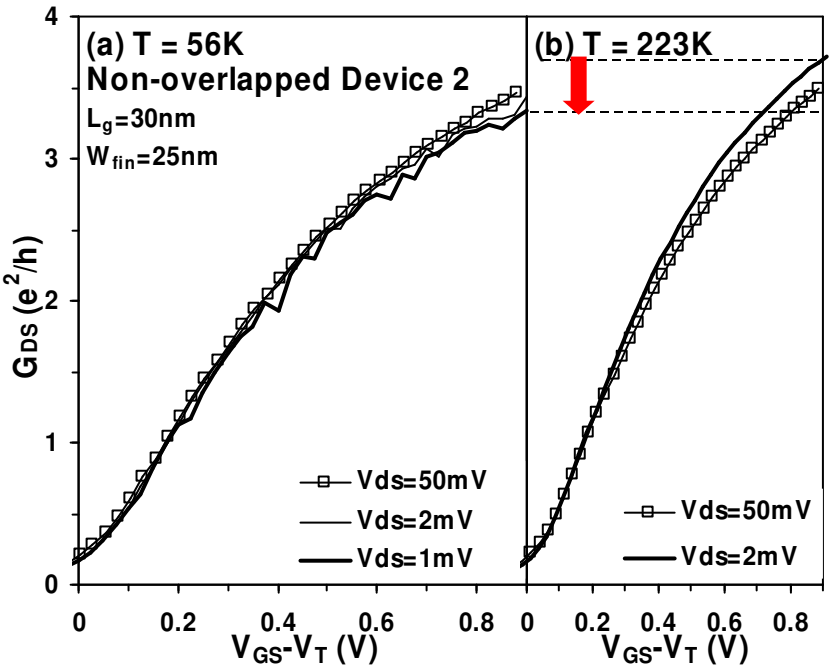


Fig. 2.5. Measured G_{DS} vs. (V_{GS}-V_T) characteristics for the non-overlapped Device 2 with L_g = 30 nm and W_{fin} = 25 nm at various V_{DS} under (a) T = 56 K and (b) T = 223 K.

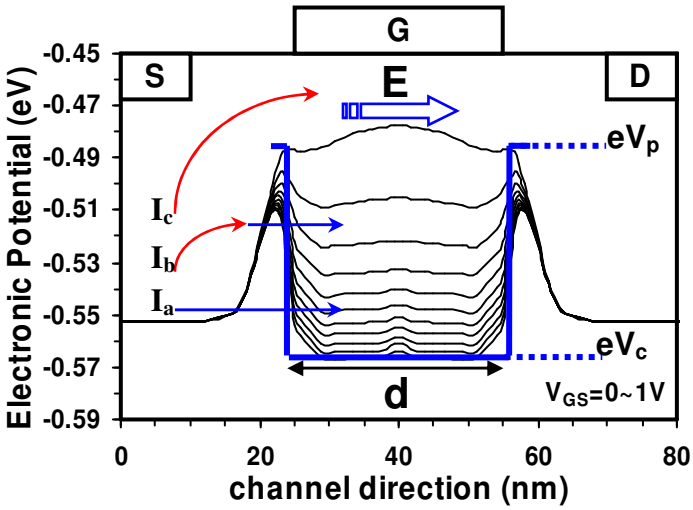


Fig. 2.6. Calculated electronic potential for the non-overlapped gate to source/drain structure at V_{GS} = 0 to 1 V. V_p: peak potential value in the non-overlapped region. V_c: potential value at the channel center. E: carrier energy. d: width of the effective quantum well. I_a: direct tunneling through the potential barrier of the non-overlapped region. I_b: thermally-associated tunneling. I_c: thermionic emission.

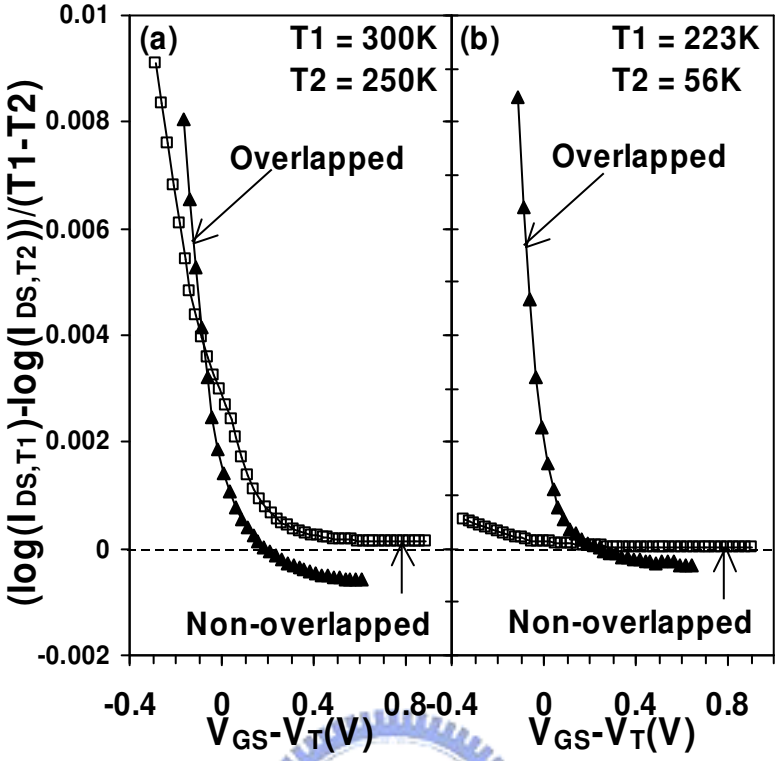


Fig. 7. Measured temperature sensitivity of drain current ($\Delta\log(I_{DS})/\Delta T$) vs. ($V_{GS}$-$V_T$) characteristics for overlapped and non-overlapped devices under (a) high temperature, T = 300 to 250 K and (b) low temperature, T = 223 to 56 K.

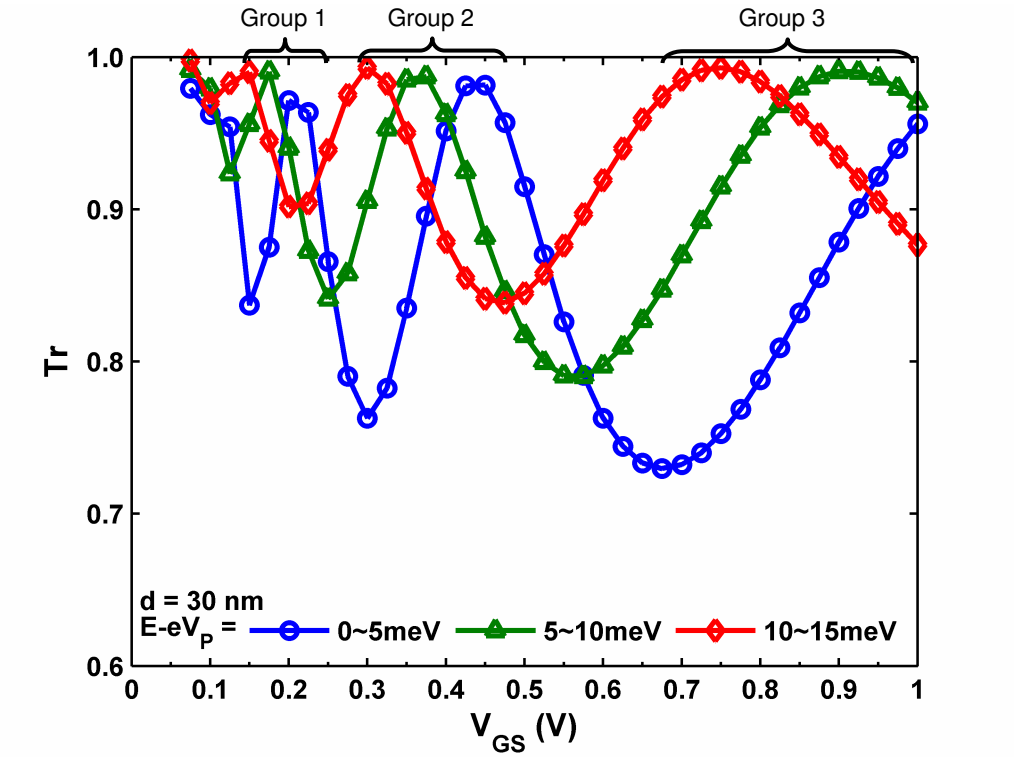


Fig. 2.8. Calculated transmission probability Tr vs. V_{GS} for d = 30 nm and E-eV_p = 0~5, 5~10 and 10~15 meV.

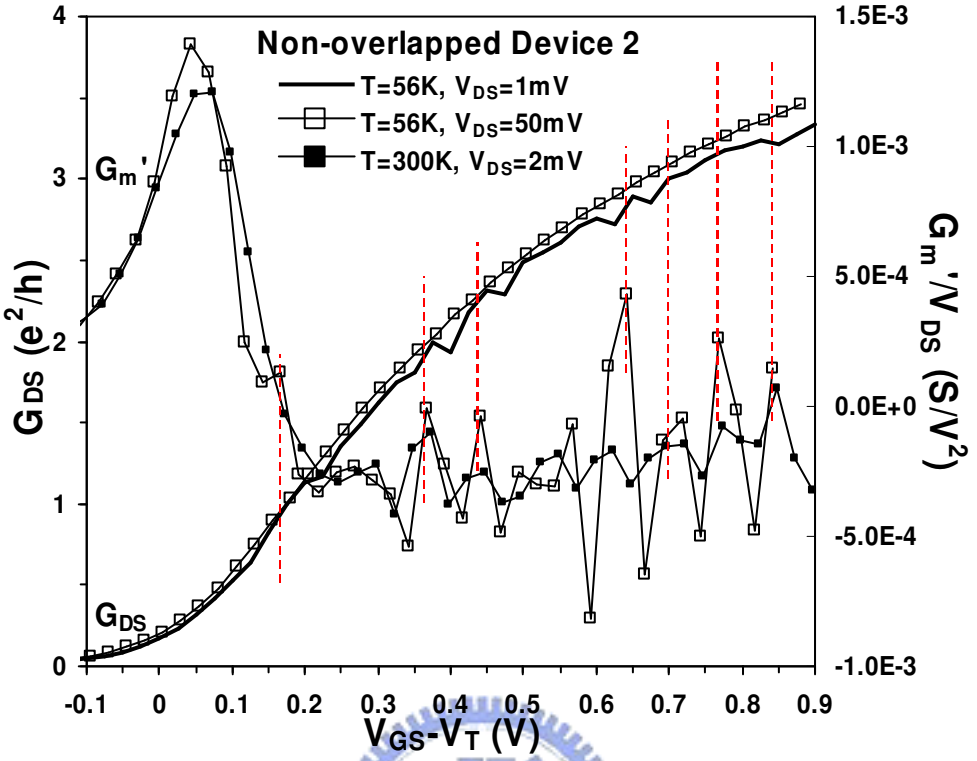


Fig. 2.9. Measured G_{DS} and G_m'/V_{DS} vs. $(V_{GS}-V_T)$ characteristics for the non-overlapped Device 2 with L_g = 30 nm and W_{fin} = 25 nm at V_{DS} = 1 and 50 mV under T = 56 and 300 K. ($G_m' = \partial G_m/\partial V_{GS}$ and $G_m = \partial I_{DS}/\partial V_{GS}$).

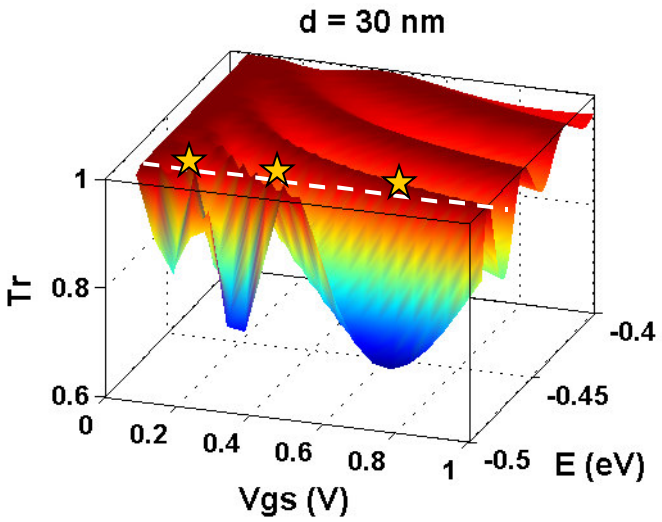


Fig. 2.10. Calculated transmission probability *Tr* vs. V_{GS} and *E* for *d* = 30 nm.

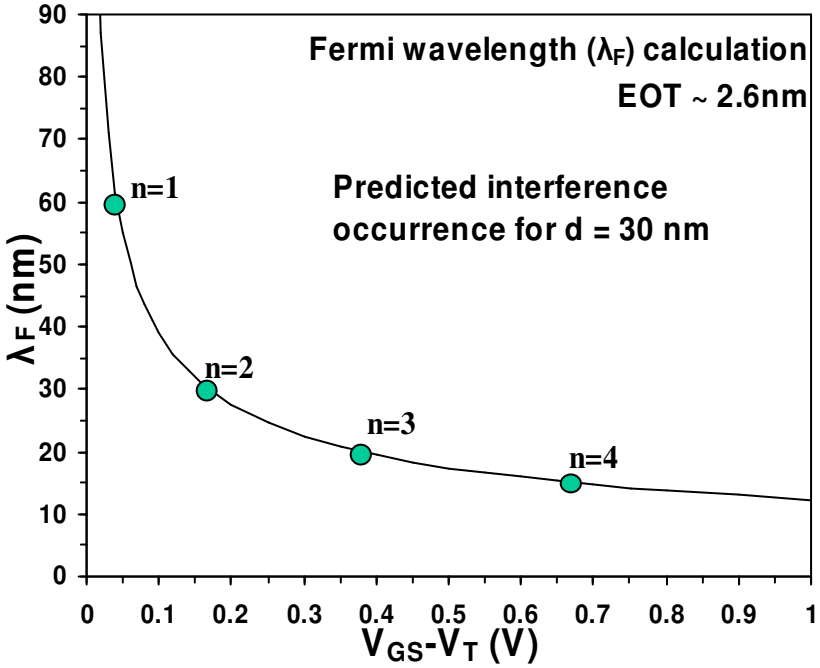


Fig. 2.11. Fermi wavelength as a function of (V_{GS}-V_T). The location at which the quantum interference occurs is indicated for d = 30 nm.

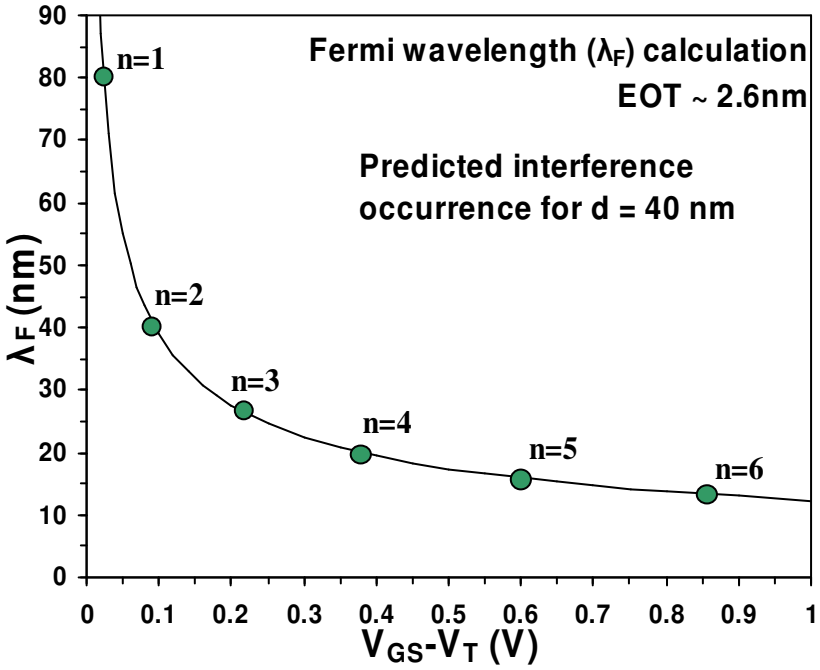


Fig. 2.12. Fermi wavelength as a function of (V_{GS}-V_T). The location at which the quantum interference occurs is indicated for d = 40 nm.

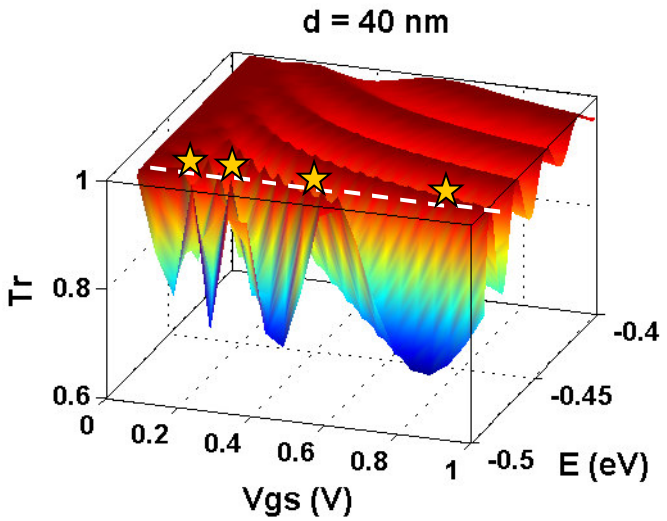


Fig. 2.13. Calculated transmission probability *Tr* vs. V_{GS} and *E* for *d* = 40 nm.

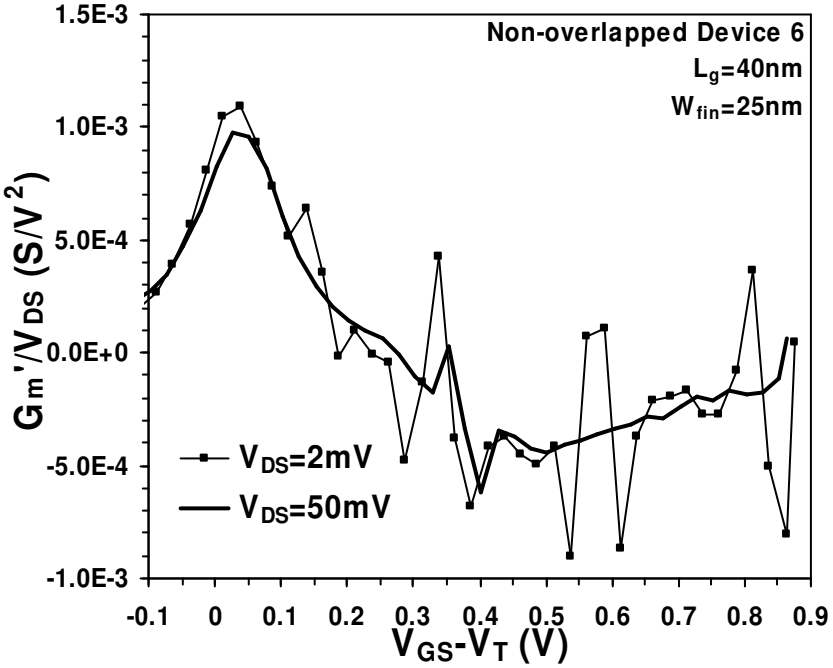


Fig. 2.14. Measured G_m'/V_{DS} vs. $(V_{GS}-V_T)$ characteristics for the Device 6 with L_g = 40 nm and W_{fin} = 25 nm.

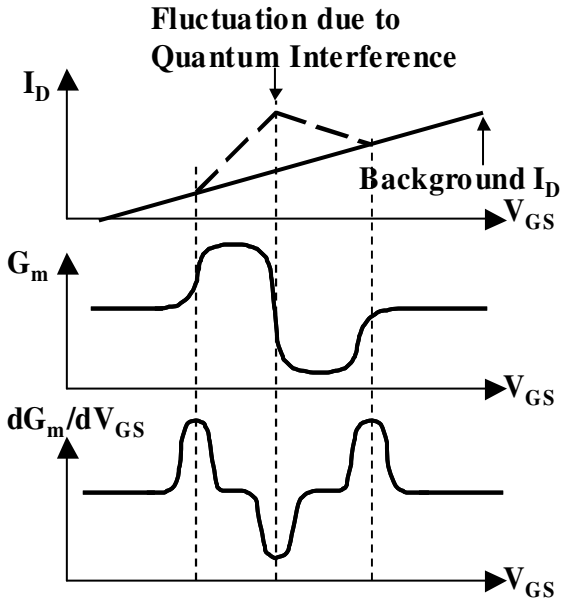


Fig. 2.15. Illustration of the quantum interference effect on I_D–V_{GS}, G_m–V_{GS}, and $\partial G_m/\partial V_{GS}$ vs. V_{GS} characteristics.

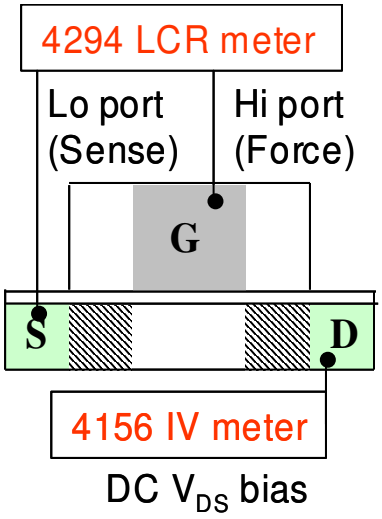


Fig 2.16. AC G_m measurement used in this work (freq. = 2 MHz). Note that the trapping/de-trapping mechanisms can be suppressed by the AC method.

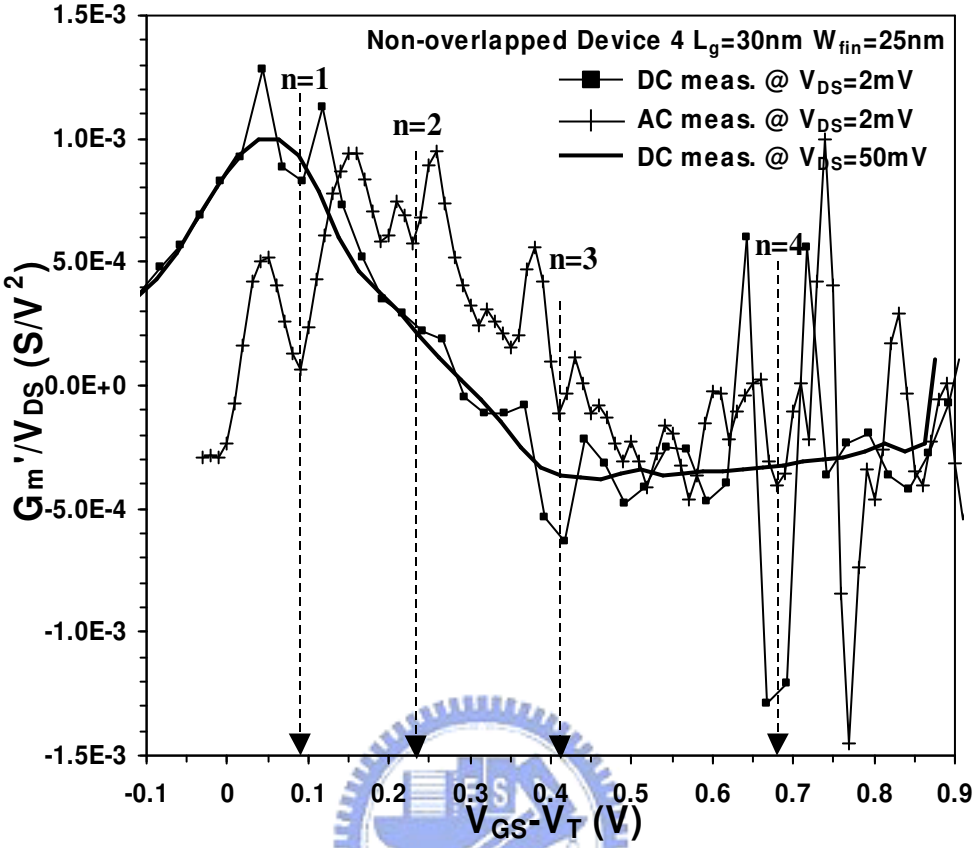


Fig. 2.17. DC and AC measurement results of $\partial G_m/\partial V_{GS}$ vs. V_{GS}-V_T for the Device 4 with L_g = 30 nm and W_{fin} = 25 nm. We can determine the (V_{GS}-V_T) at which quantum interference occurs for each n (indicated by arrows).

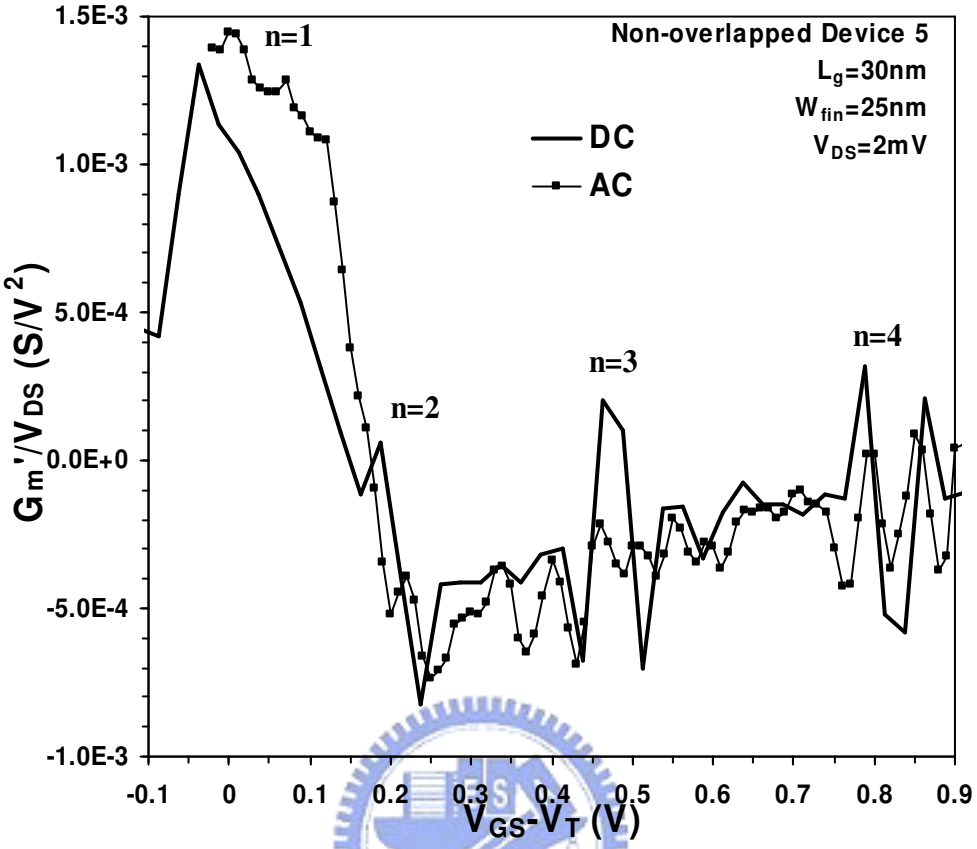


Fig. 2.18. DC and AC measurement results of $\partial G_m/\partial V_{GS}$ vs. V_{GS}-V_T for the Device 5 with L_g = 30 nm and W_{fin} = 25 nm.

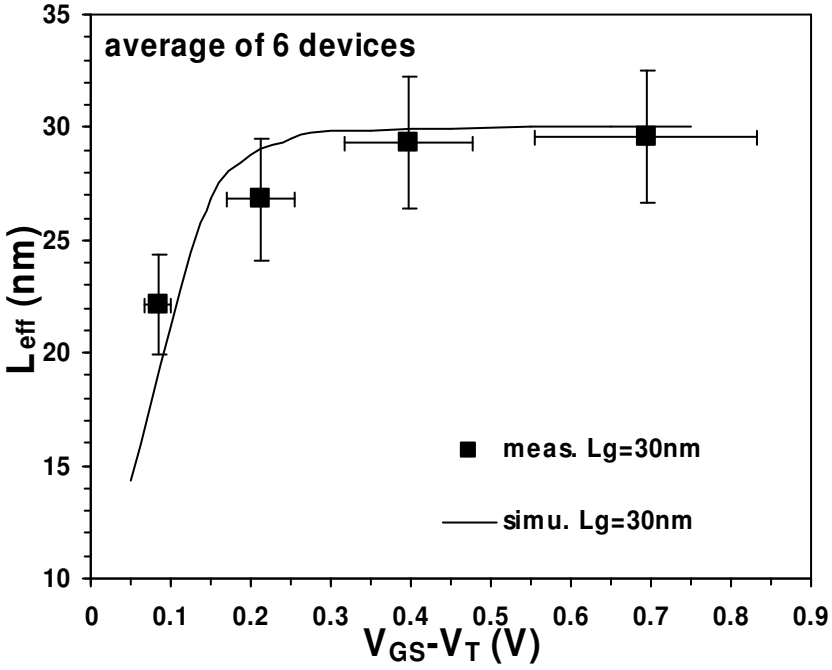


Fig. 2.19. Extracted V_{GS}-dependent L_{eff} for the non-overlapped multiple-gate FinFETs with L_g = 30 nm and W_{fin} = 25 nm.

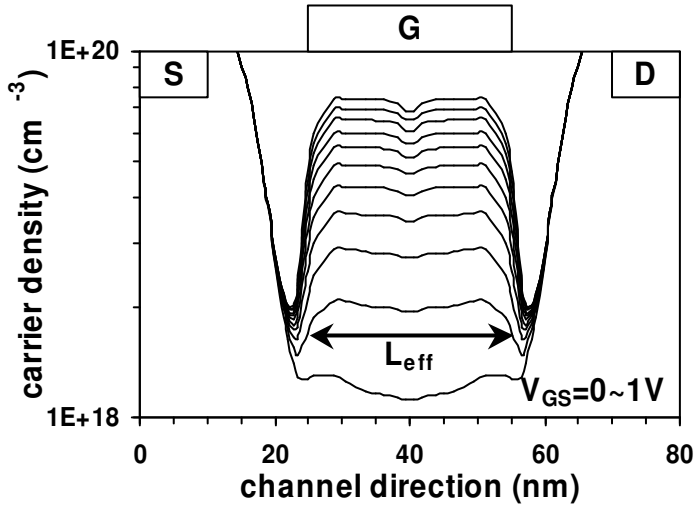


Fig. 2.20. A schematic carrier density plot along the channel between source and drain for the non-overlapped gate to source/drain structure at V_{GS} = 0 to 1 V. L_{eff} is determined based on the inversion-layer sheet conductivity.

Chapter 3

Single-Electron Effects of Non-overlapped Multiple-Gate SOI MOSFETs

3.1 Introduction

A single-electron transistor (SET) consists of a conducting island connected to two electron reservoirs through tunnel barriers [1]. When the size of the island as well as its capacitances is scaled sufficiently small, the conductivity is determined by single charge and shows periodicity. Many studies in the past [1]-[7] have pointed out that SET is a promising candidate for ultralow-power and ultrahigh-density circuit systems in the next generation [2]-[3]. Especially, the SET with standard silicon nano-electronics process and compatible with existing complementary metal-oxide-semiconductor (CMOS) device architectures is very attractive. Although various novel silicon-based SETs have been reported for superior room-temperature performance and functionality [4]-[6], it is difficult for these SETs to be compatible with state-of-the-art CMOS devices.

A direct way to realize CMOS-compatible SETs is raising Coulomb blockade effects [7] in real CMOS devices. Table 3.1 lists several studies of silicon-based SETs with MOS structures, and reveals that downsizing the SET is essential to achieving the Coulomb blockade oscillation (CBO). The key parameter is the constriction of carriers (i.e., the control of tunnel barriers and the suppression of short-channel effects). In [8], one approach of electronic confinement, using the non-overlapped-gate architecture as tunnel barriers, has been employed to produce controlled single-electron effects in real planar MOSFETs. In [9], electronic confinement by means of high access resistances

(i.e., source/drain resistances) yields CBO in ultra-thin silicon-on-insulator (SOI) MOSFETs. In [20], using the multiple-gate structure to overcome the short-channel effect, significant CBO has been shown. Although these studies represent attractive schemes to build SETs on large-scale wafers, charging energy is small (less then about 6 mV) and is not suitable for room-temperature applications. To allow high-temperature operation, the size of dots needs to be reduced. Therefore, the purpose of this work is to explore further into combining more than one approach in ultra-scaled CMOS devices.

Since multiple-gate SOI MOSFETs are considered as a promising candidate for ultra-scaled CMOS [10], we have conducted an assessment of single-electron effects in these devices near room temperature [11][32]. The single-electron effects reported in [11] and [32] is associated with the presence of tunnel barriers in spacer-defined non-overlapped gate to source/drain regions. Besides, high source/drain resistances in narrow multiple-gate devices further facilitate the constriction of carriers. To the best of our knowledge, it is the first demonstration of single-electron effects in multiple-gate SOI MOSFETs with non-overlapped gate to source/drain structure at room temperature. We have also noted that similar ideas have been reported in [23] and [24] after our study [11] [32].

We further demonstrate controlled single-electron effects in these devices through a comprehensive investigation on the observed single-electron effects, which can be modulated by geometry and applied bias. Moreover, the role of access resistances [9] and the gate-dot coupling strength [12] are assessed. The organization of this chapter is as follows. In Section 3.2, the theory of CBO is presented. In Section 3.3, we describe our device structure that features the non-overlapped architecture. Then, we systematically present single-electron effects for devices with various gate length (L_g), fin width (W_{fin}), gate bias (V_{GS}), body doping (N_B) and temperature. The impact of

access resistances [9], the estimation of gate-dot coupling strength [12] and phenomena of split-peak separations are discussed in Section 3.4. In Section 3.5, a new approach of capacitance extraction is presented. Finally, the conclusion will be drawn in Section 3.6.

3.2 Coulomb blockade oscillation

In this section we examine the circumstances under which Coulomb charging effects are important. Considering the electronic properties of the small island depicted in Fig. 3.1, charge exchange can occur only with source and drain terminals. The gate electrode provides an electrostatic or capacitive coupling through the gate capacitance C_g. The number of charges on this island is an integer with a quantized number N. When source-island (or drain-island) tunneling occurs, the charge on the island suddenly changes by the quantized amount e. The associated change in the Coulomb energy ΔE is expressed in terms of the capacitance C_g of the island as $\Delta E \sim e^2/C_g$. This charging energy becomes important when it exceeds the thermal energy k_BT, i.e., $e^2/C_g > k_BT$ [25]. A second requirement is that the barriers are sufficiently opaque such that the electrons are located either in the source, in the drain, or on the island. This means that over a time scale of Δt, changing of the charge number on the island is much less than one. Typically, $\Delta t \approx R_{barrier}C_g$, where $R_{barrier}$ represents the tunnel resistance of the barrier. From the Heisenberg uncertainty relation, $\Delta E \Delta t > h$, we can obtain $R_{barrier} > h/e^2$ [25], which implies that for an ideal tunnel barrier, $R_{barrier}$ should be much larger than the resistance quantum $h/e^2 = 25813\ \Omega$.

Under these two criterions (i.e., $e^2/C_g > k_BT$ and $R_{barrier} > h/e^2$), the conductance of the island is determined by serially discrete energy levels, which can be modulated by the gate voltage V_{GS}. Fig. 3.2 shows that while V_{GS} increases the island's electrostatic energy through C_g, the tunneling of charges can compensate the increased energy state with a discrete integer. In other words, there is the energy competition between V_{GS} and

the induced charge, which leads to so-called Coulomb blockade. Note that only when the increased energy state is charged, the island is conductive. With continually increasing V_{GS}, discrete energy levels sequentially contribute discontinuous conductance at the corresponding V_{GS} and thus result in conductance oscillations, that is, Coulomb blockade oscillation.

3.3 Experimental measurement of single-electric effects

In this section we analyze the features of periodic oscillations in G_m (= $\partial I_D/\partial V_{GS}$). DC current-voltage measurements (I_D–V_{GS}) were carefully performed using the Agilent 4156C precision semiconductor parameter analyzer in low-noise probe stations. In Section 3.3.1, we present the multiple-gate MOSFET with the non-overlapped structure. Experiments on the multiple-gate device with L_g = 30 nm and W_{fin} = 25 nm at different temperatures are described in Section 3.3.2. The geometry dependence, the V_{GS} dependence and the N_B dependence are analyzed in Sections 3.3.3 to 3.3.5, respectively.

3.3.1 Devices

The process flow for fabricating MuGFETs is similar to that reported in [33]. Fig. 3.4(a) shows the schematic view of the multi-gate SOI MOSFETs investigated in this study. Our devices were fabricated on separation by implantation of oxygen (SIMOX) SOI wafers using standard CMOS optical lithography [13]. The Si-body thickness, H_{fin}, was thinned down to about 40 nm by thermal oxidation. The fin width, W_{fin}, was defined by wet-etching and is about 15 and 25 nm. After W_{fin} was developed, the Si-body fin was doped with B^+ with doping concentration, N_B, about 6×10^{18} and 3×10^{18} cm^{-3}. Afterward the 1.6-nm gate oxide was thermally grown. The ultra-thin gate oxide contributes to not only the suppression of short-channel effects, but also the gate-dot coupling strength of the SET [12]. The *in-situ* heavily-doped N^+ poly-silicon was subsequently deposited. Using optical lithography and anisotropic reactive ion etching,

the gate length, L_g, was defined and ranges from 30 to 40 nm. Without the light-doping-drain/source (LDD/LDS) implantation, the composite spacer of silicon oxide and nitride was deposited and anisotropically etched. Finally, heavily-doped N^+ source/drain was made. It is worth noting that all the processes are essentially the same as traditional CMOS technologies.

Table 3.2 lists the information of tested devices in this work. The main feature of our device structure is the non-overlapped gate to source and drain regions, which are defined by spacers, as depicted in Fig. 3.4(b). With increasing the gate voltage, there is larger carrier concentration under the gate electrode than in the non-overlapped regions (Fig. 3.4(c)). In other words, the non-overlapped regions separate inversed carriers from source/drain and act as the electrostatic tunnel barriers of the single-electron tunneling [8]. It is worth noting that the size of tunnel barriers depends on the non-overlapped regions as well as the spacers. Optimum tunnel barriers can be controlled through modulating the width of spacers. In addition, the high source/drain resistances that are intrinsic to the multiple-gate SOI structure are useful for the constriction of carriers [9].

3.3.2 Single-electric effects in multiple-gate devices

Figure 3.5(a) shows the G_m–V_{GS} characteristics measured at room temperature (T = 20 ^{o}C) for the Device 1 with L_g = 30 nm and W_{fin} = 25 nm. Periodic oscillations, an indication of the CBO [14], in the G_m–V_{GS} characteristics can be seen. Such periodic oscillations in G_m can be reproduced for the Device 2 with the same size, as shown in Fig. 3.5(b). It is worth noting that the peaks of each period may be repeated at the same gate bias. For devices with large dimensions under the same measurement system, nevertheless, only the thermal noise can be seen. Therefore, the effect of equipments, such as the effect of source accuracy [15], is not responsible for the observed periodic oscillations. We have also noticed that the channel conductance ($G_{DS} = \partial I_D/\partial V_{DS}$) is on

the same order of magnitude as e^2/h (~3.87×10^{-5} S), which has been considered as one of the most important criteria for the CBO [1][9].

Figure 3.6(a) shows the oscillating components, G_m-<G_m>, for the data in Fig. 3.5(a). The period, ΔV_G, can be observed to be ~17 mV. When the temperature decreases from 293 to 233 K, as shown in Fig. 3.6(b), the oscillations are reproducible with the same period. To further analyze the periodic oscillations, both the discrete fast Fourier transform (FFT) [16] and the histogram of the directly counted peak-to-peak spacing (ΔV_G) [8,9] can be applied. It can be confirmed from Fig. 3.7 that the observed conductance oscillations in Fig. 3.5 follow Gaussian distribution [8,17-19] with a mean period (<ΔV_G>) ~17 mV and a standard deviation (*sd*) ~3.5 mV. The normalized width of the distribution [8], *sd*/<ΔV_G>, is about 0.2. Similar results have also been obtained in [8] for single-electron effects in planar bulk MOSFETs with the non-overlapped-gate architecture. The Gaussian shape of the ΔV_G distribution has been explained in terms of the charging energy level dynamics due to shape deformation of the quantum dot [17,18]. In other words, the shape of the quantum dot in our device is not fixed and is deformed by V_{GS}, which can be understood from the simulated V_{GS}-controlled tunnel barriers shown in Fig. 3.4(c).

3.3.3 L_g & W_{fin} dependence

The period of G_m oscillations, <ΔV_G>, represents the charging energy and is related to the gate capacitance by e/C_g [1]. For our multiple-gate devices, the gate capacitance C_g is associated with the effective gate area A_{eff} (i.e., $2H_{fin}L_g$). Therefore, we expect that the period <ΔV_G> decreases as L_g increases. Fig. 3.8 shows the G_m–V_{GS} characteristics for the Device 3 with L_g = 40 nm and W_{fin} = 25 nm at T = 20 °C. The phenomenon of G_m oscillation can still be observed with <ΔV_G> ~15 mV. Compared with the 17-mV period for the Device 1 and 2 with L_g = 30 nm, the decreased <ΔV_G>

represents the C_g dependence of single-electron effects. Furthermore, such L_g dependence indicates that the quantum dot in our devices is determined by the tunnel barriers of the non-overlapped regions rather than the disordered potential landscape demonstrated in the multi-gate SOI structures of [20].

Figs. 3.9(a)-(c) show oscillating components corresponding to V_{GS} = 0–0.2, 0.2–0.4 and 0.4–0.6 V, respectively, for the Device 4 with L_g = 40 nm and W_{fin} = 15 nm. From the FFT shown in Fig. 3.9(d), we obtain the period ranging from 13 to 10 mV. It is interesting that although the period is smaller as compared with the 15-mV period for the Device 3 with W_{fin} = 25 nm, the phenomenon of G_m oscillation is clearer than that of the Device 3 (Fig. 3.8). The decreased $<\Delta V_G>$ for W_{fin} = 15 nm may be attributed to the increase of the gate-dot coupling strength, α, which is the ratio between the gate capacitance and the total capacitance, C_g/C_Σ, and accounts for a portion of the period as [2]

$$\Delta V_G = \frac{C_\Sigma}{C_g}\left(\frac{\Delta\varepsilon}{e}\right) + \frac{e}{C_g} \quad (1),$$

where $\Delta\varepsilon$ is an average discrete energy spacing in the semiconductor. The stronger gate-dot coupling strength [12] can also further control the leakage current and thus make the conductance oscillations more distinguishable. In addition, when the W_{fin} of multiple-gate devices reduces, the source/drain resistances increase. Therefore, the carrier is further constricted [9].

3.3.4 V_{GS} dependence

It is also worth noting in Fig. 3.9 that the period of G_m oscillation decreases from 13 to 10 mV when V_{GS} increases from 0 to 0.6 V. For other devices, we can also observe the decreased period with increasing V_{GS}. Fig. 3.10 shows the extracted $1/<\Delta V_G>$ versus V_{GS} for the Devices 1 and 4. We can clearly see that $1/<\Delta V_G>$ increases with V_{GS}. From

(1), we know that ΔV_G is inversely proportional to the gate capacitance C_g, which is associated with the size of dots. Therefore, such V_{GS} dependence of ΔV_G (i.e., ΔV_G decreases as V_{GS} increases) indicates that the size of the quantum dot increases with V_{GS}. We have noted that the result in Fig. 3.10 is consistent with the V_{GS}-dependent L_{eff} in Fig. 2.19 extracted from the simulation and the quantum interference method. This indicates that the V_{GS} modulated tunnel barriers (Fig. 3.11) may account for the V_{GS} dependence of ΔV_G. It is noteworthy that the V_{GS} dependence of the period reveals a possibility of single SET with multiple periods, which may enhance the functionality of SETs.

3.3.5 N_B dependence

Fig. 3.12(a) and Fig. 3.12(b) show the oscillating components for the Device 5 with L_g = 30 nm, W_{fin} = 25 nm and $N_B = 3\times10^{18}$ cm^{-3}. The mean period, $<\Delta V_G>$, is about 18.5 mV (Fig. 3.12(c)), which is larger than the 17-mV $<\Delta V_G>$ for the Device 1 and 2 with higher N_B ($N_B = 6\times10^{18}$ cm^{-3}) (Figs. 3.5 to 3.7). The increase in $<\Delta V_G>$ can still be observed for the device with different size. Fig. 3.13(a) shows the oscillating components for the Device 6 with L_g = 40 nm, W_{fin} = 25 nm and $N_B = 3\times10^{18}$ cm^{-3}. $<\Delta V_G>$ is about 16 mV (Fig. 3.13(b)). Compared with the 15-mV $<\Delta V_G>$ for the Device 3 shown in Fig. 3.8, the $<\Delta V_G>$ for the Device 6 with lower N_B is larger. From Fig. 3.11, we know that tunnel barriers in the non-overlapped regions and body potential define the quantum dots in the multi-gate SOI MOSFETs. Therefore, the body doping concentration, N_B, should affect the periodicity because of different capacitive coupling between these electrostatic potential barriers. Note that light N_B may result in lower barrier height and enhanced short-channel effects. The situation is similar to the short-channel device without halo or pocket implants. In other words, the capacitive coupling strength from the drain side is increased. Consequently, the gate-dot coupling

strength becomes weaker and thus $<\Delta V_G>$ increases.

3.4 Discussion

3.4.1 Quantum mechanical effects

We have noted in Fig. 3(a) that the fine structure of split-peak phenomena occurs at G_m oscillating peaks. As the temperature is decreased from 293 to 233 K, the fine structure becomes clear and almost reproduces at all peaks (Fig. 3(b)). To investigate these split-peak phenomena, we performed low temperature measurements (T = 56 K) for the Device 7 with L_g = 30 nm and W_{fin} = 25 nm (Figs. 3.14(a) and 3.14(b)). Compared with the high-temperature results in Fig. 3.14(a), the fine structure can be clearly seen at T = 56 K and V_{DS} = 0.2 mV in Fig. 3.14(b). One model with considering quantum mechanical effects in the SET operation [3] may explain the fine structure. Fig. 3.15 shows several excitation energy levels with average energy spacing, $\Delta\varepsilon$, for a small dot. For the $(n+1)$th electron, the first excited state can be available as long as the carrier energy is larger than the discrete energy spacing $\Delta\varepsilon$ (i.e., $eV_{DS} + k_BT > \Delta\varepsilon$) [21]. An important characteristic for the effect of excitation energy levels is that the number of splitting peaks increases with V_{DS} [21]-[22]. To verify this feature, we measured G_m oscillations for the Device 8 with L_g = 40 nm and W_{fin} = 25 nm at V_{DS} = 0.3 and 10 mV, respectively, under T = 56 K. For V_{DS} = 0.3 mV in Fig. 3.16(a), the fine structure can be seen on a limited number of oscillating peaks. When V_{DS} increases to 10 mV in Fig. 3.16(b), we can observe the fine structure for each peak. It is worth noting in Fig. 3.16(b) as well as in Fig. 3.14(b) that single peak may develop into triple peaks for our measurements. It implies that three excitation energy levels are observed [21]-[22]. When the carrier energy is further increased by k_BT, however, thermal fluctuation smears out the fine structure, as shown in Fig. 3.14(a), Fig. 3.5 and Fig. 3.6. It is also worth noting in Fig. 3.9 that the fine structure can be clearly observed at room

temperature for the Device 4 with narrow W_{fin}. This result demonstrates that both the gate-dot coupling strength and the access resistances (i.e., source/drain resistance) are important for enhancing the control of single-electron effects and thus for the realization of room-temperature operation SETs.

3.4.2 Multiple-dot system

The excitation energy levels may also result from the coupling effect between dot arrays [29]. In [29], it has been shown that Coulomb blockade conductance peaks split into two (double dots) or three (triple dots) peaks each. The reason is attributed to the degenerated energy levels for the coupled dots. For our devices with the multiple-gate structure, multiple dots may be defined in each surface channel and may be coupled to each other when volume inversion occurs. It is worth noting in Figs. 3.12 and 3.13that split-peak separation (the fine structure) becomes more significant for the Devices 5 and 6 with light N_B than in Figs. 3.5 to 3.8. This is because light N_B decreases body potential and enhances the coupling effects.

3.4.3 Gate-dot coupling strength

From (1), we know that the gate-dot coupling strength α is an important parameter to determining periodicity of single-electron effects. Besides, α represents the efficiency of converting electrical voltage on the gate into the dot and the capability to trigger oscillations [12]. To determine the gate-dot coupling strength α of the SET, Coulomb blockade rhombus diagram can be used. The slopes of the diamond-shape contours are given by $C_g/(C_g+C_s)$ and $-C_g/C_d$, respectively [8]. Fig. 3.17 shows the rhombus diagram for the Device 2 with L_g = 30 nm and W_{fin} = 25 nm. From the slops in Fig. 3.17 (black lines), we obtain C_g:C_d:C_s = 9:16:13. For the other Device 3 with L_g = 40 nm and W_{fin} = 25 nm (Fig. 3.18), we obtain C_g:C_d:C_s = 11:9:9. We then calculate α = $C_g/(C_g+C_d+C_s)$ = 0.2 ~ 0.3. Similar results have been reported in [8] and [9]. In addition,

from $mL_gC_g/A_{eff} = C_d/W_{eff}$ (= C_s/W_{eff}), where $m = C_d/C_g$ (= C_s/C_g) and $C_g/A_{eff} = \varepsilon_{SiO2}$/EOT ~ 1.33×10^{-6} F/cm^2, we estimate C_d/W_{eff} (C_s/W_{eff}) to be about 0.71 ~ 0.44 (0.58 ~ 0.44) fF/μm. These extracted values are on the same order of magnitude as the measured junction capacitance data, as shown in Fig. 3.19.

3.5 Application to capacitance extraction

For nanoscale multi-gate devices, using top-down approaches to determine device capacitances is a challenging task. For example, the geometry-dependent parasitics associated with the 3-D topography of nonplanar devices [30] may result in difficulty in the observation of intrinsic gate capacitance (C_g) by traditional C-V based measurements. However, the occurrence of periodic Coulomb blockade in multiple-gate MOSFETs allows to extract the capacitances between the channel and the gate, source, and drain. Recently, M. Hofheinz *et al.* [31] have demonstrated that the Coulomb blockade phenomenon can be used to characterize capacitances of multiple-channel devices. In here, we extract capacitances for our multiple-gate MOSFETs.

Also shown in Fig. 3.7 is that a 17-mV period of the oscillating component can be observed for the Device 1 with L_g = 30 nm and W_{fin} = 25 nm. From $\langle \Delta V_G \rangle = e/C_g$ and the gate capacitance per unit area C_g/A_{eff} (=1.33×10^{-6} F/cm^2), we can deduce an effective area of the device, $A_{eff} \approx 7.1\times10^{-12}$ cm^2, which is about a factor of 3 smaller than the total gate area of our FinFET device ($2H_{fin}L_g$ = 24×10^{-12} cm^2). Besides uncertainties of process control in very small geometries, the discrepancy may stem mainly from the impact of excitation energy levels (Fig. 3.15), in which the degenerated energy spacing $\Delta\varepsilon$ accounts for a portion of the period of CBO as the first term in Eq. (1), $(1/\alpha)(\Delta\varepsilon/e)$. It is worth noting that the period of the fine structure (i.e., the split-peak phenomena) is near $(1/\alpha)(\Delta\varepsilon/e)$ and can be observed in the FFT. In Fig. 3.14, the fine structure is clear and responsible for the 4.3-mV period. From $\langle \Delta V_G \rangle$ = 11.7 mV and

$(1/\alpha)(\Delta\varepsilon/e)$ = 4.3 mV, we can deduce C_g ~ 21.6 aF and A_{eff} ~ 16.2×10^{-12} cm^2, which is much closer to the expected total gate area 24×10^{-12} cm^2. For the Devices 4 (Fig. 3.16) and 8 (Fig. 3.9), C_g can be extracted ~26.6 aF and ~29.6 aF, respectively. Fig. 3.20 shows the extracted C_g values from Eq. (1) and $\langle\Delta V_G\rangle = e/C_g$. It is worth noticing that the extracted values of C_g are linearly proportional to L_g for Eq. (1). In addition, the values of C_d and C_s can then be calculated for the extracted C_g and the capacitance ration in Coulomb blockade rhombus characteristics (see Section 3.4.3). The extracted values of C_d and C_s are about 21.8 ~ 38.4 aF and 21.8 ~ 31.2 aF, respectively.

3.6 Conclusion

In summary, we have systematically investigated controlled single-electron effects in multiple-gate SOI MOSFETs with various L_g, W_{fin}, V_{GS}, N_B and temperature. Our study indicates that using the non-overlapped gate to source/drain structure as an approach of the SET in MOSFETs is promising. Combining the advantage of gate control and the constriction of high source/drain resistances, single-electron effects are further enhanced using the multiple-gate architecture. From the presented results, downsizing multiple-gate SOI MOSFETs is needed for future room-temperature SET applications. Besides, the tunnel barriers and access resistances may need to be further optimized. Since single-electron effects can be achieved in state-of-the-art CMOS devices, it is beneficial to built SETs in low-power CMOS circuits for the ultrahigh-density purpose. In addition, the occurrence of periodic oscillation in multiple-gate MOSFETs allows extracting the aF-scale capacitances.

References

[1] K.K. Likharev, "Single-Electron Devices and Their Applications", *Proceedings of The IEEE*, vol. **87**(4), pp. 606–632, April 1999.

[2] S.M. Goodnick and J. Bird, "Quantum-Effect and Single-Electron Devices," *IEEE Trans. on Nanotechnology*, vol. **2**(4), pp. 368–385, Dec. 2003.

[3] K. Miyaji, M. Saitoh, and T. Hiramoto, "Compact analytical model for room-temperature-operating silicon single-electron transistors with discrete quantum energy levels," *IEEE Trans. on Nanotechnology*, vol. **5**(3), pp. 167–173, May 2003.

[4] C.S. Lent, P.D. Tougaw, W. Porod, and G.H. Bernstein, "Quantum cellular automata," *Nanotechnology*, vol. **4**, pp. 49–57, 1993.

[5] M. A. Nielsen and I. L. Chuang, *Quantum Computation and Quantum Information* (Cambridge: Cambridge University) 2000.

[6] K. Uchida, J. Koga, R. Ohba, and A. Toriumi, "Room-temperature operation of multifunctional single-electron transistor logic," *IEDM Tech. Dig.*, pp. 863–865, 2000.

[7] C.W.J. Beenakker, "Theory of Coulomb-blockade oscillations in the conductance of a quantum dot," *Phys. Rev. B*, vol. **44**(4), pp. 1646–1656, July 1991.

[8] F. Boeuf, X. Jehl, M. Sanquer, and T. Skotnicki, "Controlled Single-Electron Effects in Nonoverlapped Ultra-Short Silicon Field Effect Transistors," *IEEE Trans. on Nanotechnology*, vol. **2**(3), pp. 144–148, Sept. 2003.

[9] X. Jehl, M. Sanquer, G. Bertrand, G. Guégan, S. Deleonibus, and D. Fraboulet, "Silicon Single Electron Transistors With SOI and MOSFET Structures: The Role of Access Resistances," *IEEE Trans. on Nanotechnology*, vol. **2**(4), pp. 308–313, Dec. 2003.

[10] Z. Krivokapic, C. Tabery, W. Maszara, Q. Xiang, and M.-R. Lin, "High performance 45 nm CMOS technology with 20 nm multi-gate devices," *2003 Int. Conf. Solid State Devices Materials*, pp. 760–761, 2003.

[11] W. Lee, P. Su, H.-Y. Chen, C.-Y. Chang, K.-W. Su, S. Liu, and F.-L. Yang, "An assessment of single-electron effects in multiple-gate SOI MOSFETs with 1.6-nm gate oxide near room temperature," *IEEE Electron Device Letters*, vol. **27**(3), pp. 182–184, Mar. 2006.

[12] Y.-M. Wan, K.-D. Huang, C.-L. Sung, and S.-F. Hu, "Transport properties of ultra thin oxide gated Si SET near room temperature," in *Proc. 5th IEEE Conf. Nanotechnology*, vol. **2**, pp. 750–753, July 2005.

[13] F.-L. Yang, H.-Y.Chen, F.-C. Chen, Y.-L. Chan, K.-N. Yang, C.-J. Chen, H.-J. Tao, Y.-K. Choi, M.-S. Liang, and C. Hu, "35nm CMOS FinFETs," *Symp. VLSI Tech. Dig.*, pp.104–105, 2002.

[14] L. Zhuang, L. Guo, and S. Y. Chou, "Silicon single-electron quantum-dot transistor switch operating at room temperature," *Appl. Phys. Letters*, vol. **72**(10), pp. 1205–1207, March 1998.

[15] KEITHLEY Instruments, Inc., Overcoming the Measurement Challenges of Advanced Semiconductor Technologies – DC, Pluse, and RF-From Modeling to Manufacturing (1st Edition), 2005, p. 102, (http://www.keithley.com/wb/201)

[16] J.H.P. Scott-Thomas, S.B. Field, M.A. Kastner, H.I. Smith, and D.A. Antoniadis, "Conductance Oscillations Periodic in the Density of a One-Dimensional Electron Gas," *Phys. Rev. Letters*, vol. **62**(5), pp. 583–586, January 1989.

[17] F. Simmel, D. Abusch-Magder, D.A. Wharam, M.A. Kastner, and J.P. Kotthaus, "Statistics of the Coulomb-blockade peak spacings of a silicon quantum dot", *Phys. Rev. B*, vol. **59**(16), pp. 10441–10444, April 1999.

[18] R.O. Vallejos, C.H. Lewenkopf, and E.R. Mucciolo, “Coulomb Blockade Peak Spacing Fluctuations in Deformable Quantum Dots: A Further Test of Random Matrix Theory”, *Phys. Rev. Letters*, vol. **81**(3), pp. 677–680, July 1998.

[19] R. Berkovits, “Absence of Bimodal Peak Spacing Distribution in the Coulomb Blockade Regime”, *Phys. Rev. Letters*, vol. **81**(10), pp. 2128–2131, Sept. 1998.

[20] M.G. Peters, S.G. den Hartog, J.I. Dijkhuis, O.J.A. Buyk, and L.W. Molenkamp, “Single electron tunneling and suppression of short-channel effects in submicron silicon transistors,” *J. Appl. Phys.*, vol. **84**(9), pp. 5052–5056, Nov. 1998.

[21] L.L. Sohn, L.P. Kouwenhoven, and G. Schön, “Mesoscopic Electron Transport,” *NATO Science Series E: Applied Sciences*, Vol. **345**, Springer, Sept. 30, 1997.

[22] A.T. Johnson, L.P. Kouwenhoven, W. de Jong, N.C. van der Vaart, C.J.P.M. Harmans, and C.T. Foxon, “Zero-dimensional states and single electron charging in quantum dots,” *Physical Review Letters*, vol. **69**(10), pp. 1592-1595, July 1992

[23] M. Hofheinz, X. Jehl, M. Sanquer, G. Molas, M. Vinet, and S. Deleonibus, “Simple and controlled single electron transistor based on doping modulation in silicon nanowires,” *Appl. Phys. Lett.*, vol. **89**, p. 143504,Oct. 2006.

[24] H. Sellier, G.P. Lansbergen, J. Caro, S. Rogge, N. Collaert, I. Ferain, M. Jurczak, and S. Biesemans, “Transport Spectroscopy of a Single Dopant in a Gated Silicon Nanowire,” *Phys. Rev. Lett.*, vol. **97**, p. 206805 ,Nov. 2006.

[25] L.P. Kouwenhoven, C.M. Marcus, P.L. McEuen, S. Tarucha, R.M. Westervelt, and N.S. Wingreen, “Electron Transport in Quantum Dots,” *proc. Nato ASI conference*, ed. by L.P. Kouwenhoven, G. Schön, and L.L. Sohn (Kluwer, Dordrecht, 1997).

[26] Y. Takahashi, H. Namatsu, K. Kurihara, K. Iwadate, M. Nagase, and K. Murase, “Size Dependence of the Characteristics of Si Single-Electron Transistors on SIMOX Substrates,” *IEEE Trans. on Electron Devices*, vol. **43**(8), p. 1213, 1996.

[27] M. Sanquer, M. Specht, and L. Ghenim, "Coulomb blockade in low-mobility nanometer size Si MOSFET's," *Phys. Rev. B*, vol. **61**(11), p. 7249, 2000.

[28] H. Matsuoka, T. Ichiguchi, T. Yoshimura, and E. Takeda, "Coulomb blockade in the inversion layer of a Si metal-oxide-semiconductor field-effect transistor with a dual-gate structure," *Appl. Phys. Letter*, vol. **64**(5), p. 586, 1994.

[29] F.R. Waugh, M.J. Berry, D.J. Mar, and R.M. Westervelt, "Single-Electron Charging in Double and Triple Quantum Dots with Tunable Coupling," *Phys. Rev. Letters*, vol. **75**(4) pp. 705–708, July 1995.

[30] W. Wu, M. Chan, "Analysis of Geometry-Dependent Parasitics in Multifin Double-Gate FinFETs," *IEEE Trans. on Electron Devices*, vol. **54**(4), pp. 692–698, April 2007.

[31] M. Hofheinz, X. Jehl, M. Sanquer, R. Cerutti, A. Cros, P. Coronel, H. Brut, and T. Skotnicki, "Measurement of Capacitances in Multigate Transistors by Coulomb Blockade Spectroscopy," *IEEE Trans. on Nanotechnology*, vol. **7**(1), pp. 74–78, Jan. 2008.

[32] W. Lee and P. Su, "Single-electron effects in non-overlapped multiple-gate silicon-on-insulator metal-oxide-semiconductor field-effect transistors," *Nanotechnology*, vol. **20**, p. 065202, Feb. 2009.

[33] F.-L. Yang, H.-Y. Chen, F.-C. Chen, C.-C. Huang, C.-Y. Chang, H.-K. Chiu, C.-C. Lee, C.-C. Chen, H.-T. Huang, C.-J. Chen, H.-J. Tao, Y.-C. Yeo, M.-S. Liang, and C. Hu, "25nm CMOS Omega FETs," *IEDM Tech. Dig.*, pp. 255–258, Dec. 2002.

Table 3.1. Several studies on single-electron effects in Si-based MOS structures.

	this work	[20]	[12]	[26]	[14]	[9]	[8]	[27]	[28]
type	N-Fin	N-Fin	N-SET	SET	N-SEQDT	Acc-SET	NP-Bulk	N-bulk	N-DGbulk
T_{ox} (nm)	**1.6**	25	**6**	30	25	10	**2~3**	**2.4~3.8**	10
L (nm)	**30**	200	**40**	**50~200**	**dot**	~100	**16~27**	**50~100**	~5000
W (nm)	**25**	100~500	**15**	**20**	**16**	>50	280	1000~400	130
H (nm)	**40**	100	**25**	**30**	**32**	**10**			
C_g (aF)	20~30	5.2	2	3~5	1.7	27	66	46~80	>46
ΔV_g (mV)	17	~31	400	50~30	1400	6	9~6	3.5~2	16~17
Temp. (K)	**<300**	1.8	**<250**	**300**	**300**	<10	<5	<5	<1
lithography	**optical**	E-beam	E-beam	E-beam	E-beam	E-beam	**optical**		E-beam

Table 3.2. A list of devices studied in this work.

Device	W_{fin} (nm)	L_g (nm)	N_B (10^{18} cm^{-3})	T (K)	Figure
1	25	30	6	233, 293	3.5(a), 3.6, 3.7
2	25	30	6	293	3.5(b), 3.17
3	25	40	6	293	3.8, 3.18
4	15	40	6	293	3.9
5	25	30	3	223	3.12
6	25	40	3	223	3.13
7	25	30	6	56, 293	3.14
8	25	40	6	56	3.16

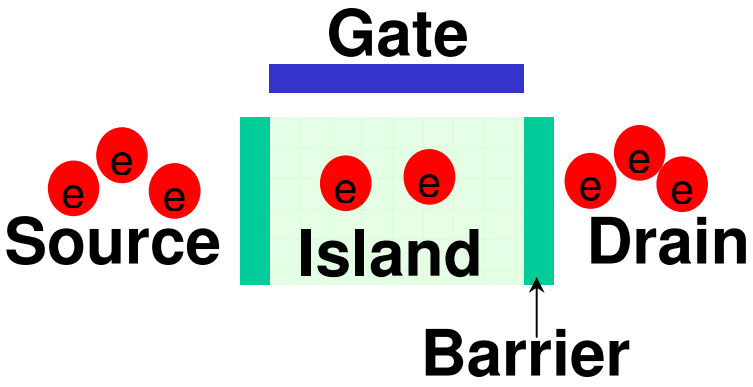


Fig. 3.1. Schematic of a quantum dot, in the shape of an island, connected to source and drain electrodes by tunnel barriers and to a gate by a capacitor (C_g).

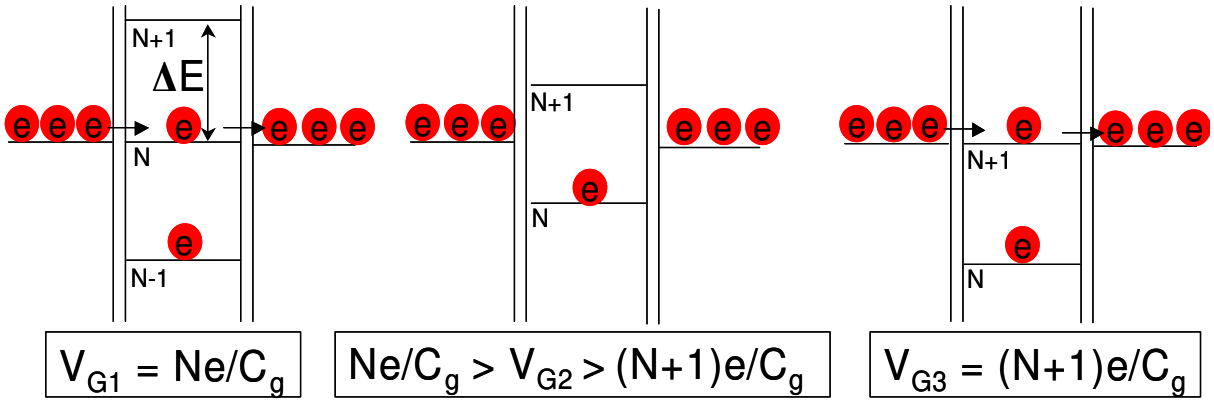


Fig. 3.2. An illustration of Coulomb blockade oscillations, the effect of single electron charges on the conductance vs. V_G characteristics. The period in gate voltage V_G is about e/C_g. $V_{G3} > V_{G2} > V_{G1}$.

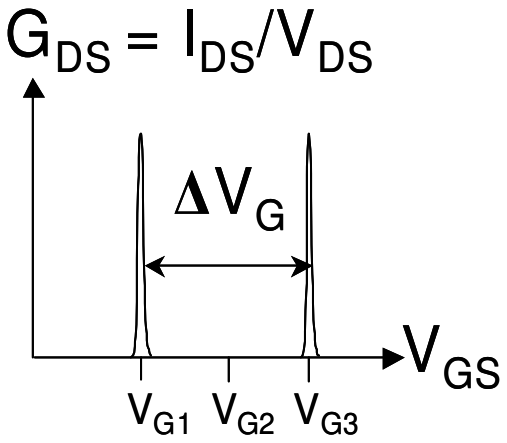


Fig. 3.3. An example of Coulomb blockade oscillations in G_{DS} vs. V_G characteristics. The conductance G_{DS} is the ratio I_{DS}/V_{DS} and the period ΔV_G is about e/C_g.

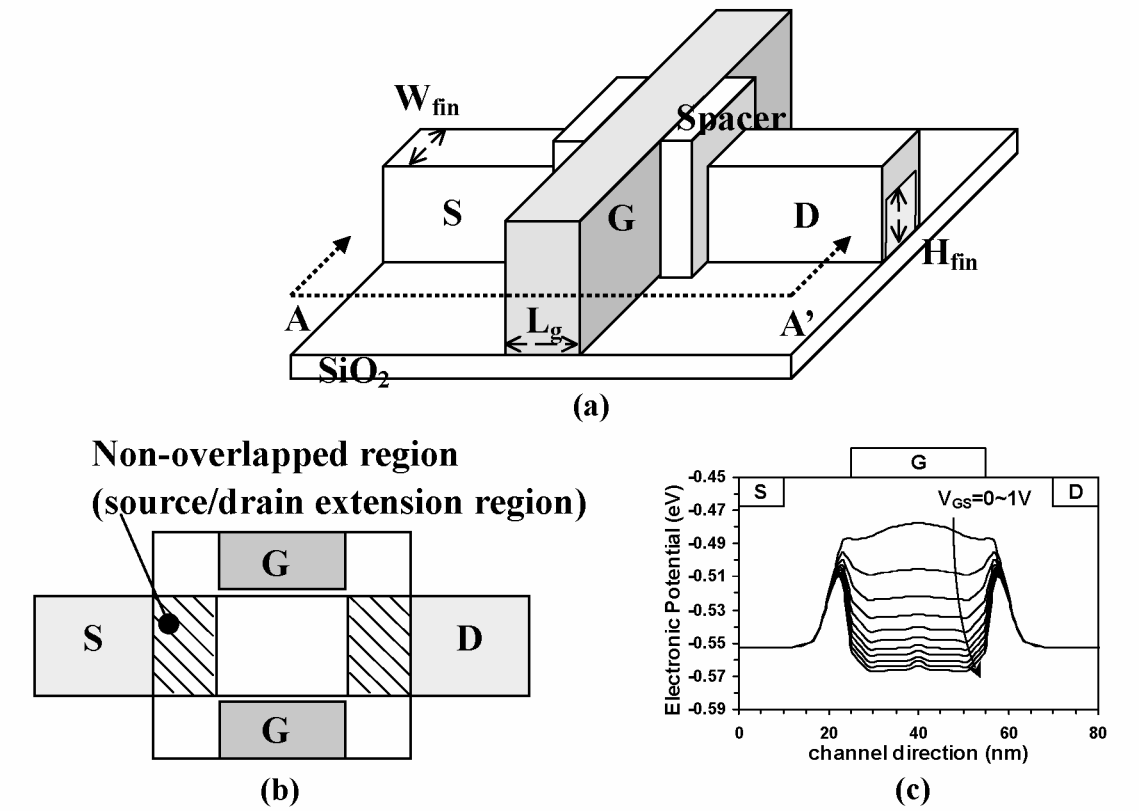


Fig. 3.4. Multiple-gate Fin-FET SOI structure investigated in this work and (b) its cross-sectional view along A-A' view showing the non-overlapped gate to source/drain regions. (c) A schematic electronic potential plot along the channel between source and drain for the FinFET with non-overlapped regions.

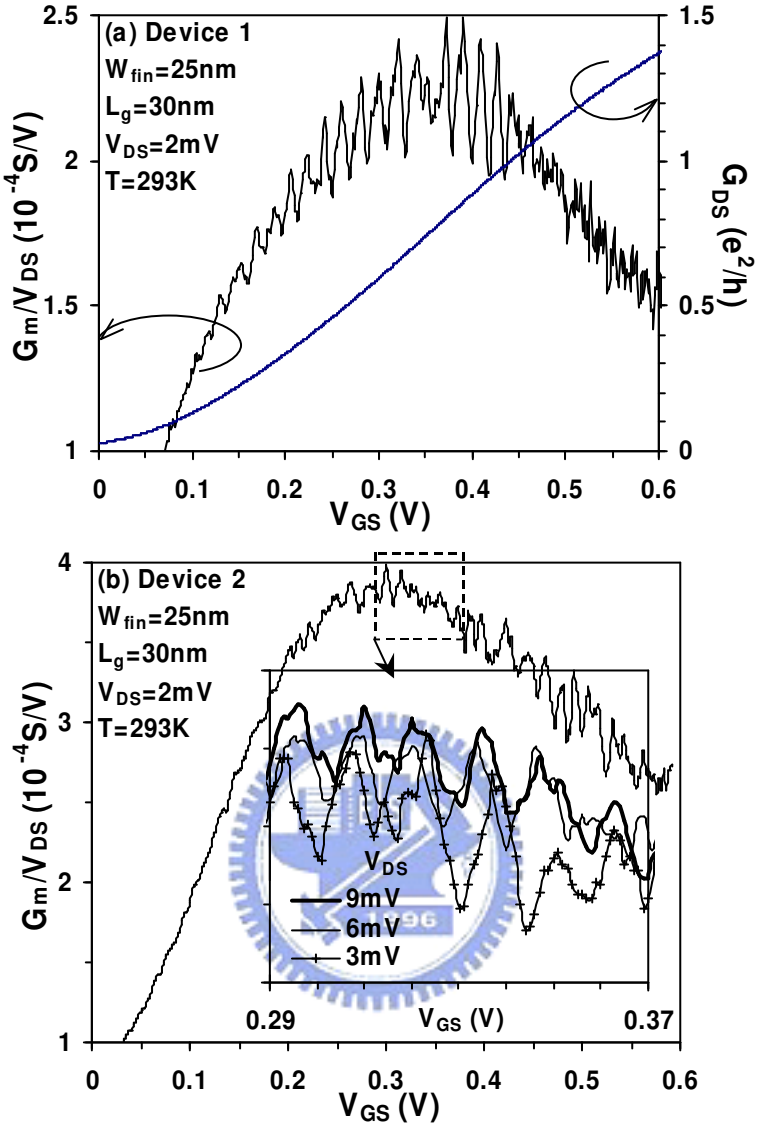


Fig. 3.5. Periodic oscillations occur in G_m/V_{DS} vs. V_{GS} characteristics for (a) the Device 1 and (b) the Device 2 with L_g = 30 nm and W_{fin} = 25 nm at T = 293K.

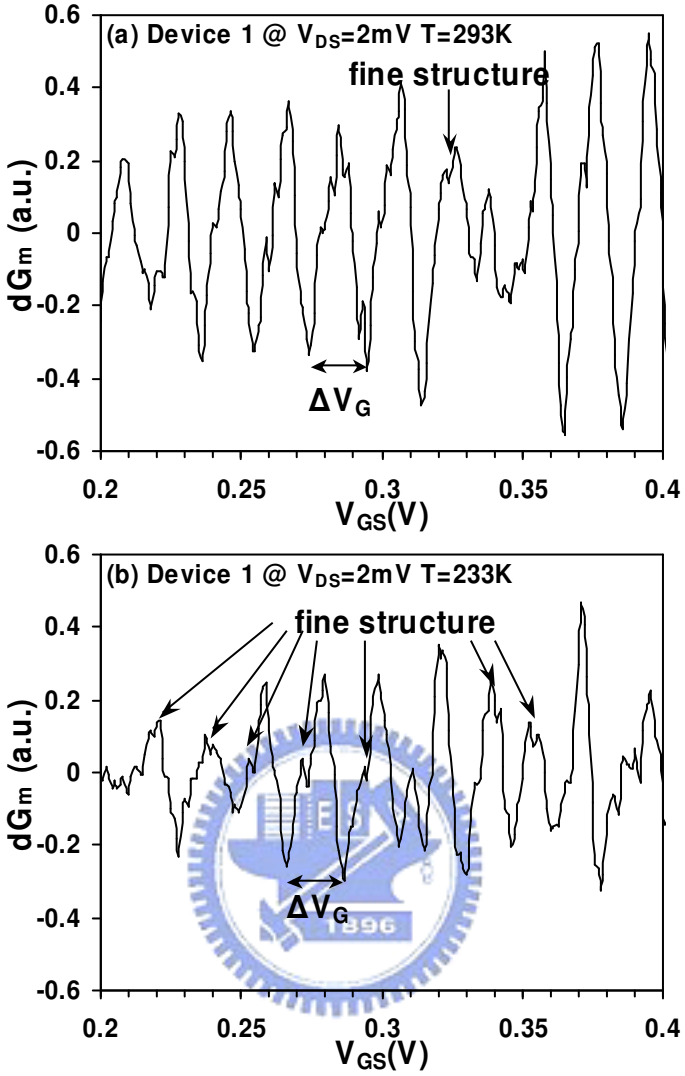


Fig. 3.6. Periodic oscillations occur in dG_m (= G_m-<G_m>) vs. V_{GS} characteristics for the Device 1 at (a) T = 293 K and (b) T = 233 K. <G_m> is the long-range average.

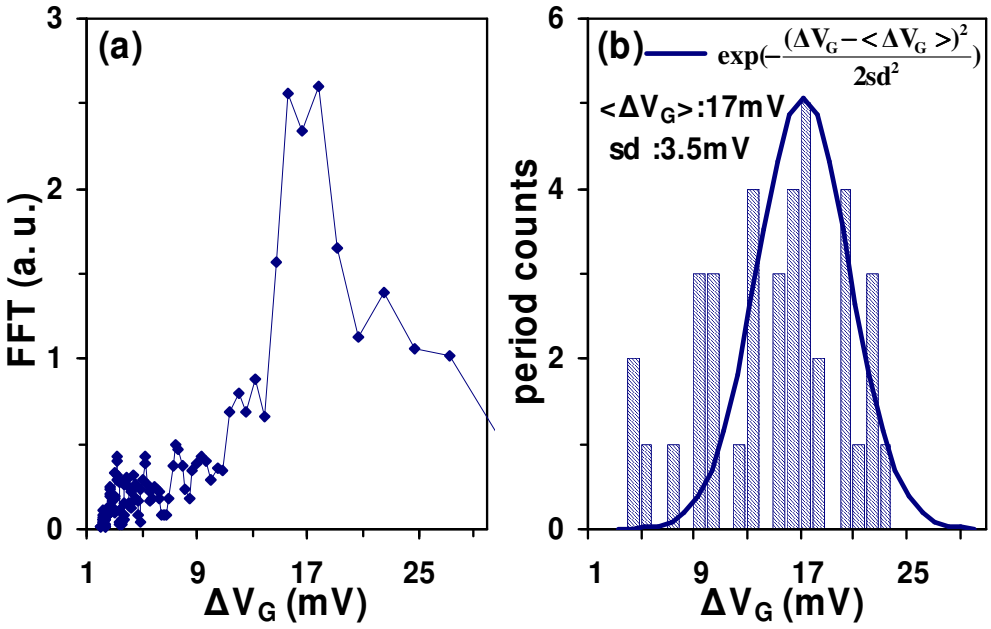


Fig. 3.7. Both (a) the FFT and (b) the histogram of the directly counted peak-to-peak spacing (ΔV_G) confirm that the period ($<\Delta V_G>$) in Fig. 3.6 is 17 mV.

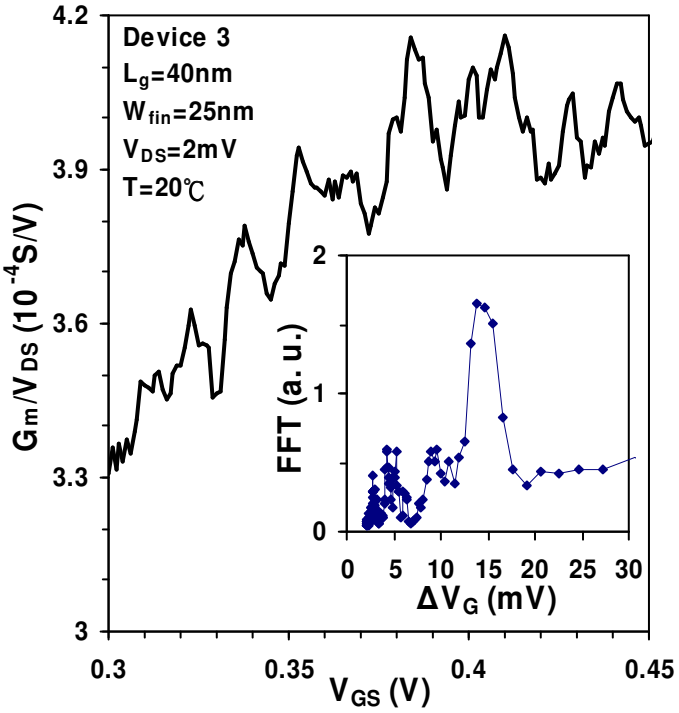


Fig. 3.8. Periodic oscillations occur in G_m/V_{DS} vs. V_{GS} characteristics for the Device 3 with L_g = 40 nm and W_{fin} = 25 nm at T = 20 °C. Smaller peak-to-peak spacing (ΔV_G = 15 mV) from the FFT can be seen.

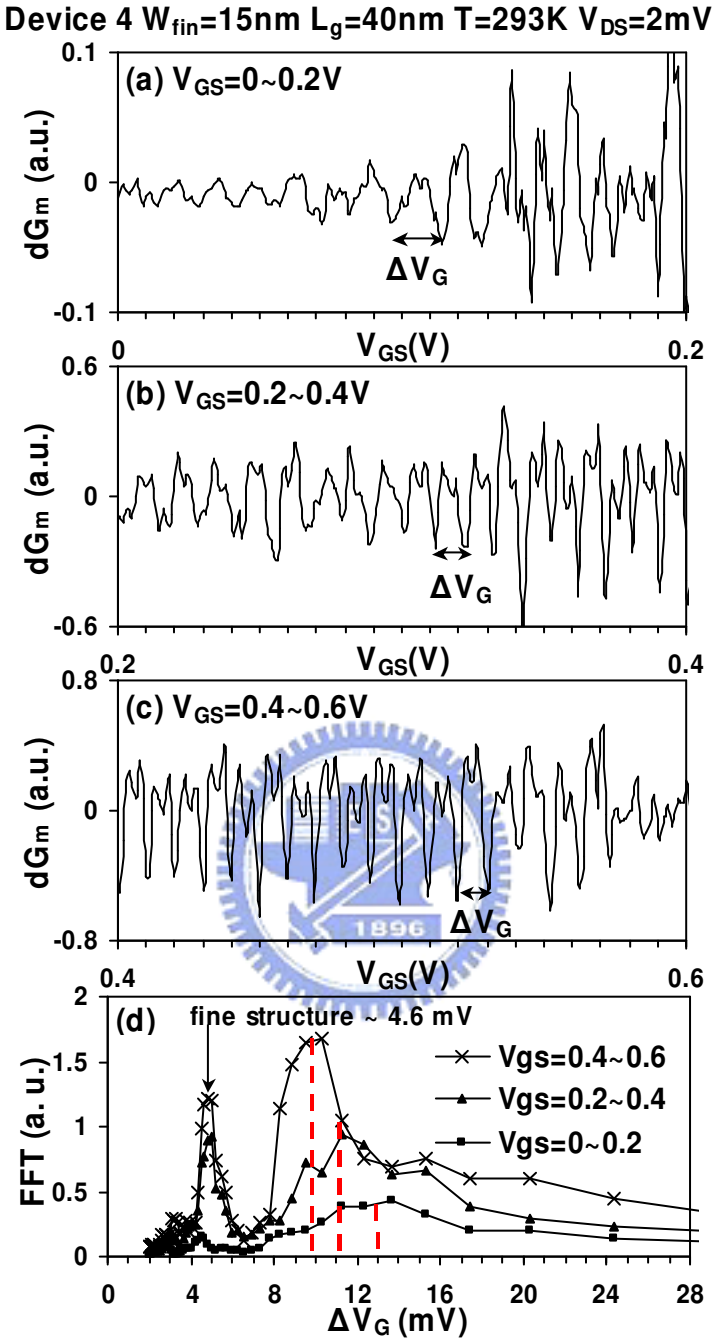


Fig. 3.9. Periodic oscillations occur in dG_m vs. V_{GS} characteristics for the Device 4 with L_g = 40 nm and W_{fin} = 15 nm at (a) V_{GS} = 0~0.2 V, (b) V_{GS} = 0.2~0.4 V and (c) V_{GS} = 0.4~0.6 V. (d) The FFT of periodic oscillations in different V_{GS} regimes.

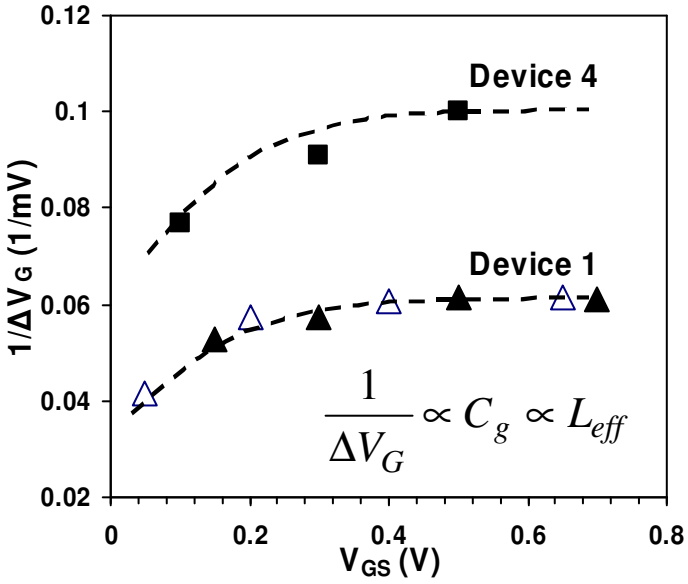


Fig. 3.10. V_{GS} dependence of $1/\langle \Delta V_G \rangle$ can be observed for the Device 1 and 4. $\langle \Delta V_G \rangle$ is extracted from the FFT in different V_{GS} regimes.

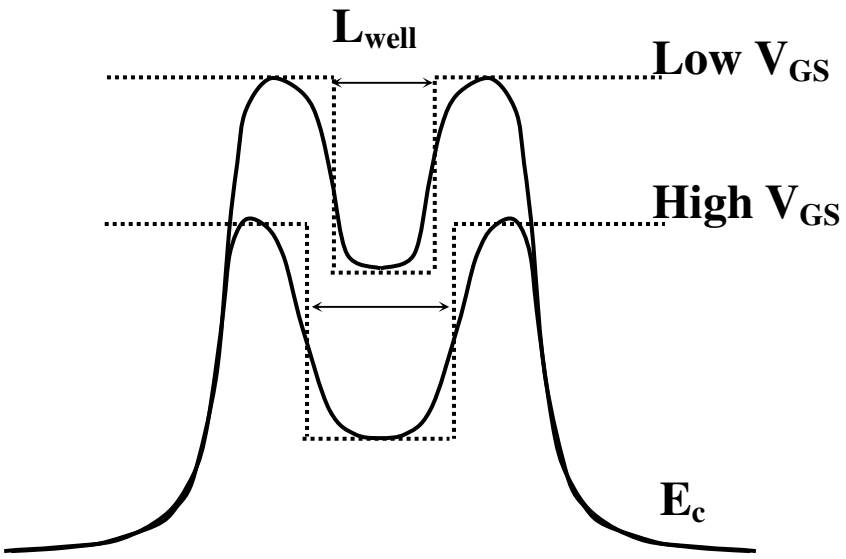


Fig. 3.11. An illustration of the V_{GS}-modulated tunnel barriers.

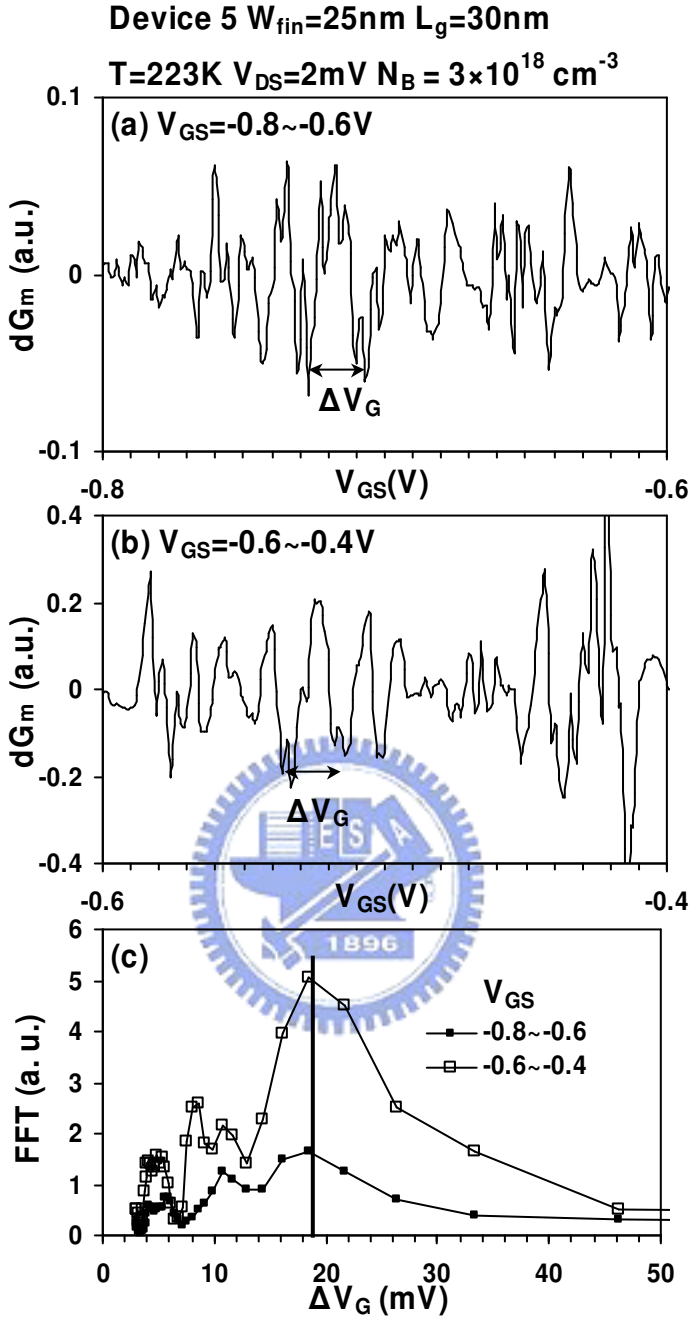


Fig. 3.12. Periodic oscillations occur in dG_m vs. V_{GS} characteristics for the Device 5 with L_g = 30 nm, W_{fin} = 25 nm and $N_B = 3\times10^{18}$ cm^{-3} at (a) V_{GS} = -0.8~-0.6 V and (b) V_{GS} = -0.6~-0.4 V. (c) The FFT of periodic oscillations in different V_{GS} regimes.

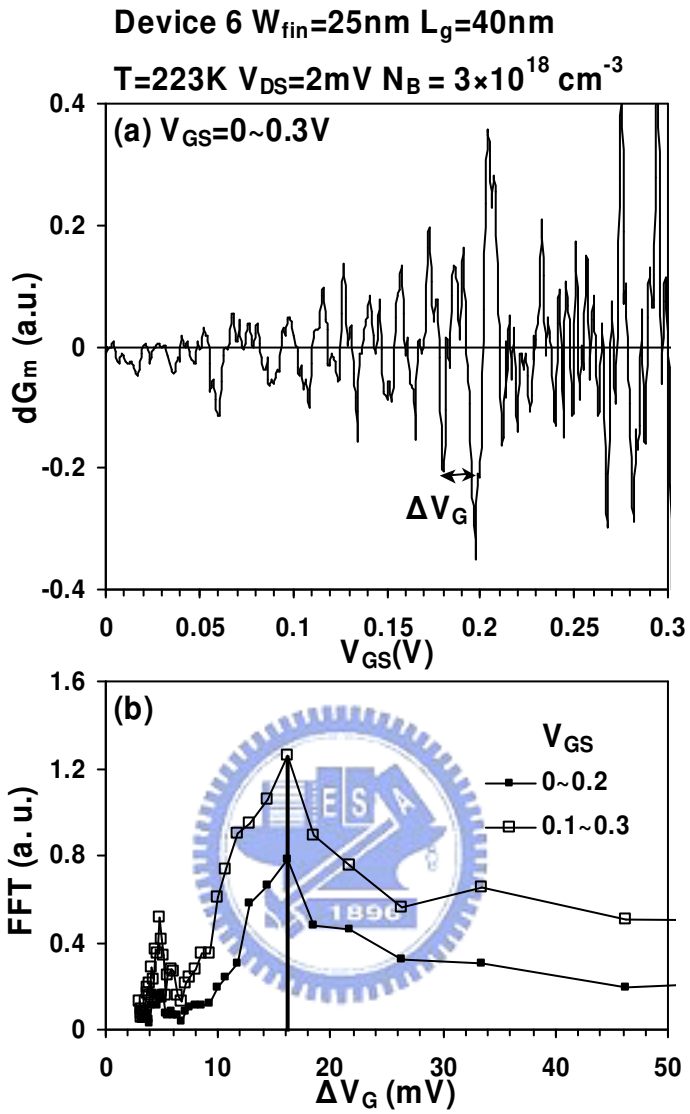


Fig. 3.13. (a) Periodic oscillations occur in dG_m vs. V_{GS} characteristics for the Device 6 with L_g = 40 nm, W_{fin} = 25 nm and N_B = 3×10^{18} cm^{-3} at V_{GS} = 0~0.3 V. (b) The FFT of periodic oscillations in different V_{GS} regimes.

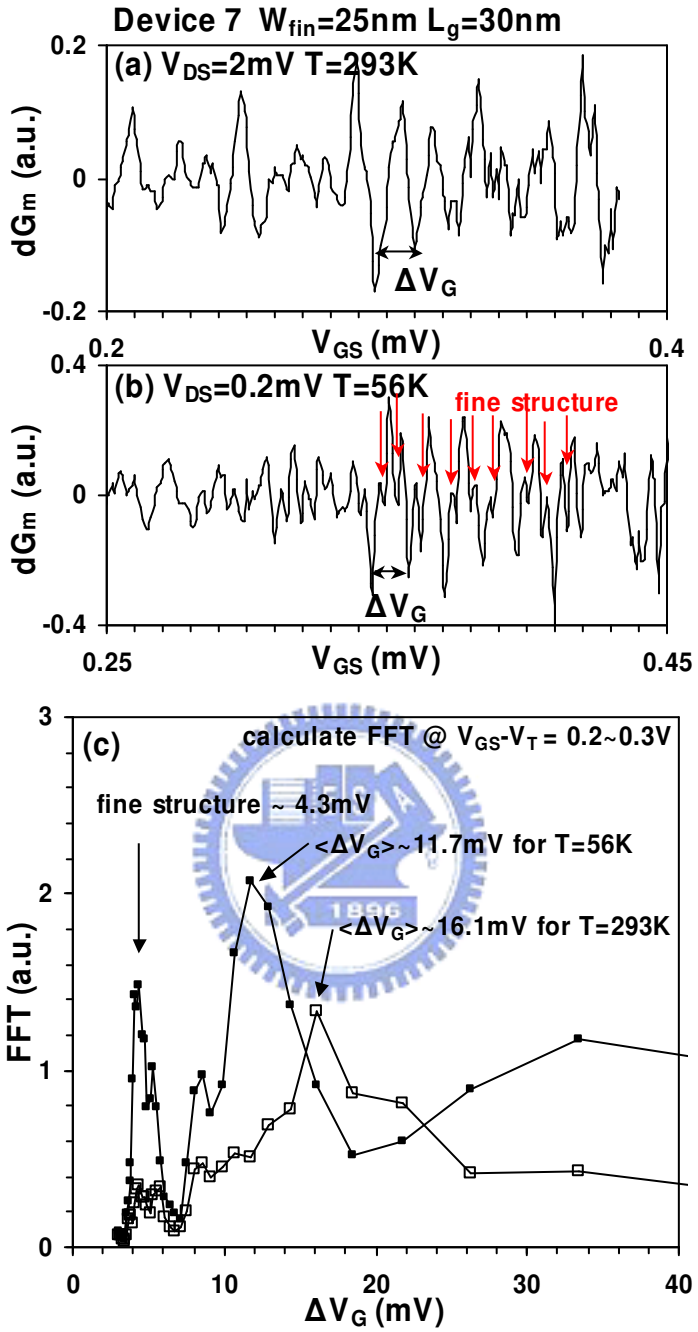


Fig. 3.14. Periodic oscillations occur in dG_m vs. V_{GS} characteristics for the Device 7 with L_g = 30 nm and W_{fin} = 25 nm at (a) T = 293 K and (b) T = 56 K.

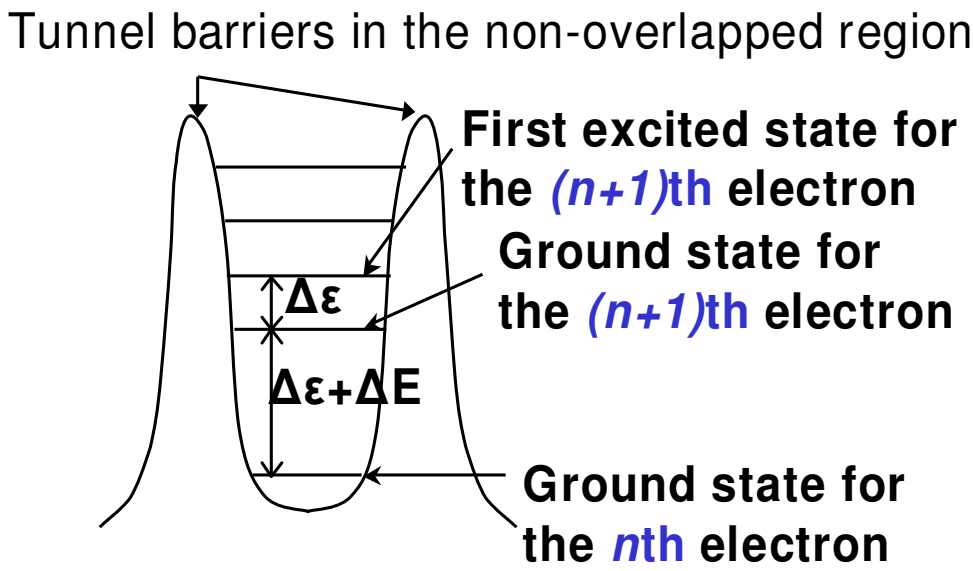


Fig. 3.15. Schematic energy diagram of a SET. The quantum energy levels are discrete with each quantum-level spacing defined as $\Delta\varepsilon$. ΔE is the charging energy e^2/C_Σ.

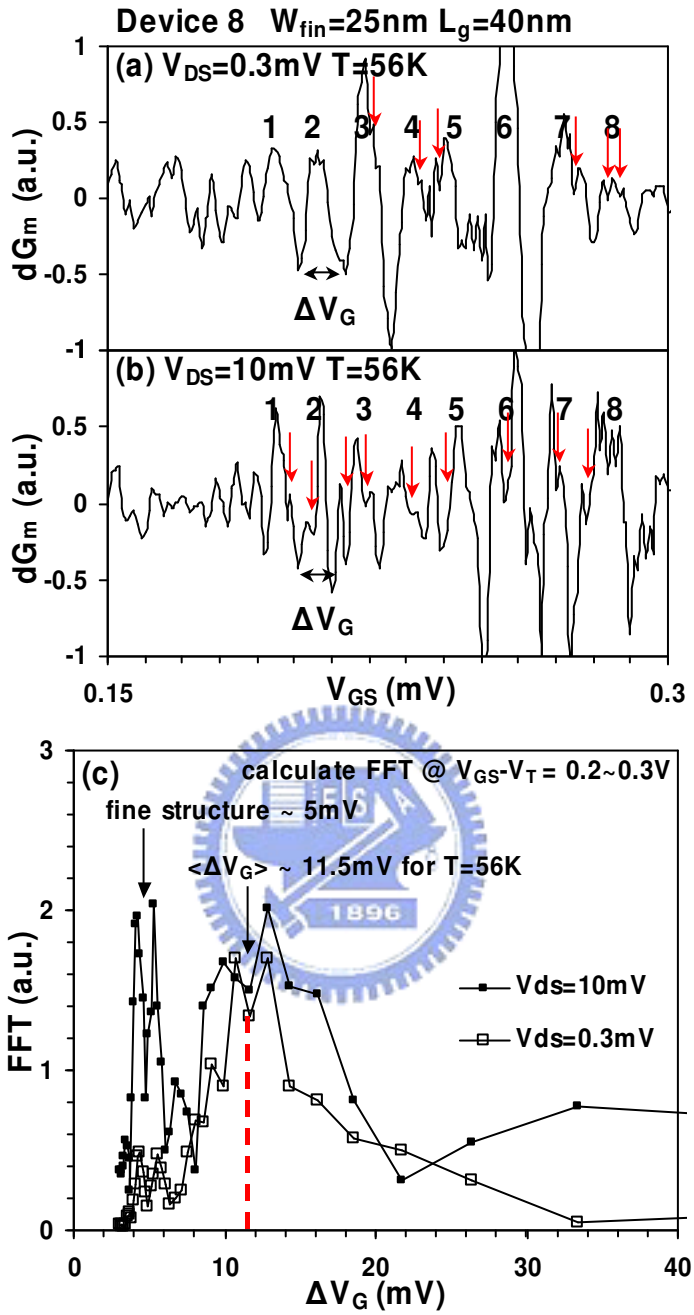


Fig. 3.16. Periodic oscillations occur in dG_m vs. V_{GS} characteristics for the Device 8 with L_g = 40 nm and W_{fin} = 25 nm at (a) V_{DS} = 0.3 mV and (b) V_{DS} = 10 mV under T = 56 K.

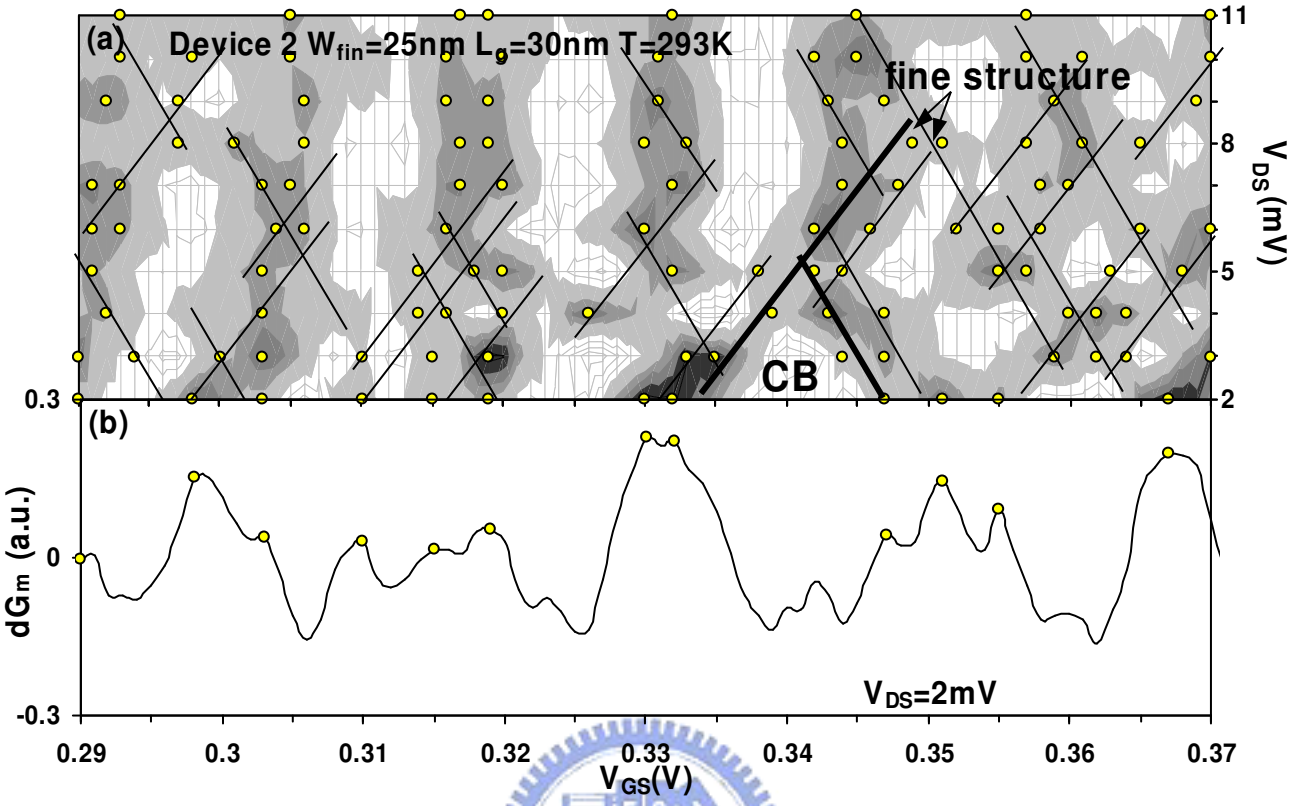


Fig. 3.17. (a) Rhombus diagram for the Device 2. (b) dG_m vs. V_{GS} characteristics at V_{DS} = 2 mV. The conductance peaks (dots) correspond to the dots at V_{DS} = 2 mV in (a).

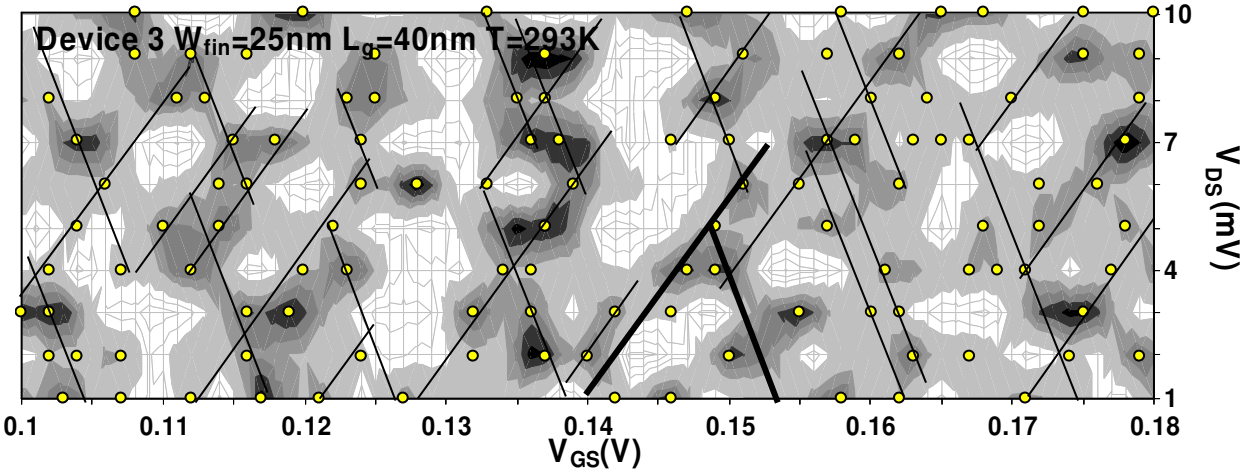


Fig. 3.18. Rhombus diagram for the Device 3 with L_g = 40 nm and W_{fin} = 25 nm.

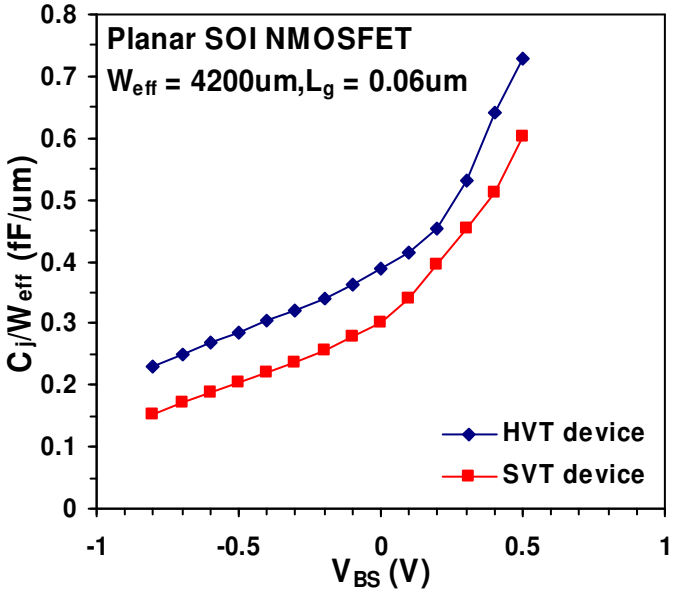


Fig. 3.19. Measured junction capacitance C_j per unit width vs. V_{BS} characteristics for planar SOI NMOSFET with high and low doping.

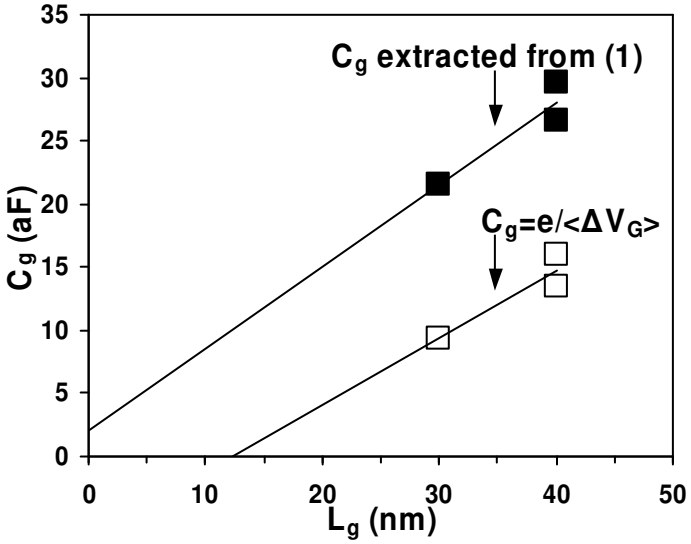


Fig. 3.20. C_g vs. L_g characteristics for different extraction methods.

Chapter 4

Ballistic Transport Characteristics of Nanoscale MOSFETs

4.1 Introduction

Since the introduction of channel backscattering theory [1][2], there has been great interest in determining how close to the ballistic limit the CMOS device can be operated using backscattering coefficient (r_{sat}). Indeed, the 2007 edition of the international technology roadmap of semiconductors (ITRS) has reported that to attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal velocity (υ_{therm}) and injection efficiency (i.e., ballistic efficiency $B = (1-r_{sat})/(1+r_{sat})$) at the source end (Fig. 4.1) appears to be needed [3]. In addition, the continued aggressive scaling of CMOS is driving the industry toward a number of major technological innovations such as high-k dielectrics and uniaxial-strain technologies. Therefore, there is a strong motivation on developing techniques to experimentally estimate backscattering coefficient r_{sat} for providing guidelines in CMOS processes and determining the impacts of modern technologies on the ballistic efficiency.

To this purpose, A. Lochtefeld and D. A. Antoniadis [4] have proposed a technique to determine the thermal limit (i.e., the ballistic limit) by comparing the measured effective velocity to the simulated injection velocity. Besides, V. Barral *et al.* [5][6] presented an r_{sat} extraction methodology with considering multi-subband population based on the simulated correction factor. However, relying on simulation in extraction procedures is inconvenient to be routinely used in technology development. So far, to the best of our knowledge, the only fully experimental method [7][8]

evaluates r_{sat} from the mean free path λ and the critical length l as

$$r_{sat} = \frac{l}{l+\lambda} \tag{1}.$$

Based on the temperature-dependent characteristics of drain current, the value of λ/l can be obtained by [7][8]

$$\frac{\lambda}{\ell} = \frac{-2\left(1+\left(\beta_\mu - \beta_l\right)-\gamma\right)}{\gamma - \left(\frac{\partial I_{d,sat}}{I_{d,sat}\partial T} + \frac{\partial V_{T,sat}}{(V_{gs}-V_{T,sat})\partial T}\right)T} - 2 \tag{2},$$

where β_μ, β_l and γ are defined as the temperature sensitivity of the low-field mobility μ_0, the critical length l and the thermal velocity υ_{therm}, respectively. $V_{T,sat}$ and $I_{d,sat}$ are saturated threshold voltage and drain current.

Recently, this method has been examined by [20] and concluded that the accuracy of (2) is quite modest due to the inaccurate inversion charge (Q_{inv}). However, we found that the error was originated from estimating Q_{inv} by the linear threshold voltage $V_{T,lin}$ instead of $V_{T,sat}$ for $I_{d,sat}$. Moreover, a constant (β_μ-β_l) (e.g., (β_μ-β_l) = -2.5 or -2.23 [20]) was used for devices with different gate length (L_g). Fig. 4.2 shows that after considering accurate $V_{T,sat}$ and L_g-dependence of (β_μ-β_l) in (2), the observed ballistic efficiency presents the same L_g dependence as the Multi-Subband-Monte-Carlo results in [20]. Besides, this result indicates that the accuracy of this temperature-dependent backscattering extraction method (i.e., (2)) lies in accurate $V_{T,sat}$, β_μ, β_l and γ.

In previous studies [9]-[15], β_μ = -1.5 (i.e., phonon-limited mobility $\propto T^{-1.5}$), β_l = 1 (i.e., l = the k_BT length $\propto T$) and γ = 0.5 (i.e., $\upsilon_{therm} = \sqrt{2k_BT/\pi m^*}$ for the non-degenerate limit) have been assumed. However, these assumptions are questionable for state-of-the-art nanoscale MOSFETs [18]-[20]. For example, Z. Ren *et al.* [19] have shown that the electron mobility in high–k (HfO_2) devices is relatively insensitive to temperature, i.e., $\mu_0 \propto T^{-1}$. In addition, the temperature dependence of the critical length

l (i.e., β_l) may not equal to 1 because the critical length l may not equal to the k_BT length (i.e., the distance over which the potential drops by k_BT/q (Fig. 4.1)) [29][30][36]. It has been shown in [36] that the "critical" length l is several times larger than the k_BT length and may change with L_g, channel electric field and scattering mechanisms. Moreover, the temperature dependence of the thermal velocity υ_{therm} (i.e., γ) decreases from 0.5 (non-degenerate limit) to 0 (degenerate limit) with increasing V_{gs} [21]. All these facts indicate that the β_μ, β_l and γ can not be assumed constants and the difficulty of the temperature-dependent backscattering extraction method lies in accurate determination of β_μ, β_l and γ. Therefore, a physically accurate backscattering extraction method considering accurate β_μ, β_l and γ is needed.

In this work, we report a new temperature-dependent channel backscattering extraction that can self-consistently determine (β_μ-β_l) and r_{sat} for nanoscale MOSFETs. Under the self-consistent framework, several assumptions in the original method (e.g., μ_0 = the low-field mobility, l = the k_BT length, $\lambda = 2k_BT\mu_0/q\upsilon_{therm}$, and the non-degenerate limit) are no longer needed. The validity and the limitation of our method are discussed. Applications for the process monitoring purpose are experimentally assessed based on various types of devices such as: high vs. low body-doping, and HfO_2 vs. SiO_2 dielectric. The impacts of the strain effect, the self-heating effect and the floating-body effect on r_{sat} are investigated [37].

The organization of this chapter is as follows. In Section 4.2, the channel backscattering theory is briefly presented. In Section 4.3, we present our self-consistent temperature-dependent extraction method. Then, we study the limitations of the method and propose guidelines for utilizing our self-consistent method. Experimental investigation of the Coulomb scattering effects and the uniaxial strain effects on extracted backscattering coefficients are discussed in Section 4.4 and Section 4.5,

respectively. For SOI devices, the extraction with self-heating corrections and the floating-body effects are presented in Section 4.6. In Section 4.7, we further propose using enhanced ballistic efficiency to suppress the drain current variation for nanoscale MOSFETs. Finally, the conclusion will be drawn in Section 4.8.

4.2 Channel backscattering theory

Figure 4.1 illustrates the physical picture of flux treatment of carrier transport in nanoscale MOSFETs [1][2]. We focus on the fluxes at the source-channel junction barrier. Carriers injected from the thermal equilibrium source and drain populate the top of this barrier. Appling a high drain bias, carriers injected from the drain to the source need not to be considered, because there is a significant potential barrier ~qV_{DS} for carriers in the drain. Therefore, carriers in the source play an important role. A fraction of carriers injected from the source into the channel is scattered back to the source. Others flow out the drain and comprise the steady-state drain current I_d. The density of carriers at the top of the source-channel junction barrier is controlled by MOS capacitance, that is, gate capacitance C_g. Generally, the inversion carriers Q_{inv} can be computed from

$$Q_{inv} \approx C_g \left(V_{gs} - V_T\right) \tag{3},$$

where V_T is the threshold voltage. Because of current continuity, the steady-state drain current I_d may be evaluate from Q_{inv} of the source-channel junction barrier as

$$I_d = WQ_{inv}\upsilon_{inj} \approx WC_g \left(V_{gs} - V_T\right)\upsilon_{inj} \tag{4},$$

where υ_{inj} is the average velocity of carriers at the beginning of the channel. The maximum value of υ_{inj} is approximately the equilibrium uni-directional thermal velocity υ_{therm}, because all carriers with the positive velocity (i.e., flux from source to drain) were injected from the thermal equilibrium source [1][2]. Backscattering from the channel determines how close to this upper limit the device operates. According to the

derivation in [21], υ_{inj} in saturation region can be related to the channel backscattering coefficient r_{sat} as

$$\upsilon_{inj} \approx \left(\frac{1-r_{sat}}{1+r_{sat}}\right)\upsilon_{therm} \tag{5}.$$

Besides, υ_{therm} with degenerate consideration is expressed as [21]

$$\upsilon_{therm} = \sqrt{\frac{2k_BT}{\pi m^*}}\left(\frac{\Im_{1/2}(\eta_F)}{\Im_0(\eta_F)}\right) \tag{6},$$

where $\Im_n(\eta_F)$ is the Fermi-Dirac integral of order n and is function of the Fermi level E_F normalized to k_BT (i.e., $\eta_F = (E_F\text{-}E_i)/k_BT$). Finally, using (4), (5) and (6), we obtain

$$\frac{I_{d,sat}}{W} = Q_{inv}\left(\frac{1-r_{sat}}{1+r_{sat}}\right)\left\{\sqrt{\frac{2k_BT}{\pi m^*}}\left(\frac{\Im_{1/2}(\eta_F)}{\Im_0(\eta_F)}\right)\right\} \tag{7}.$$

Note that (7) is derived for the saturation condition, i.e., $qV_{ds} >> k_BT$. The V_{ds} dependence factor is approximated to 1 [21]. Besides, the saturation threshold voltage ($V_{T,sat}$) is required to consider accurate Q_{inv} in (7), that is, $Q_{inv} \approx C_{ox}(V_{gs}\text{-}V_{T,sat})$.

In the ballistic case $r_{sat} = 0$, ballistic efficiency $B = (1\text{-}r_{sat})/(1+r_{sat}) = 1$, and the drain current $I_{d,sat}$ has its thermal limited maximum. From (1), we know that the channel backscattering coefficient r_{sat} depends on the mean free path λ and the critical length l [2]. In the scattering theory [2], λ and l are physically referred to the low-field mobility μ_0 (i.e., $\lambda = 2k_BT\mu_0/q\upsilon_{therm}$) and the k_BT length (i.e., l = the k_BT length = the distance over which the potential drops by k_BT/q (Fig. 4.1)), respectively. However, these expressions were challenged as a phenomenological one that is useful for physical understanding, but not quantitatively [29][30][32][33][36]. The reasons are listed: The concept of the carrier mobility is derived from the drift diffusion model and is applicable to long channel devices. The role of scattering in nanoscale transistors is more complicate and is not straightforward to determine without considering redistribution of scattered carriers [29]. Besides, the redistributed carriers, the corresponding λ, and the potential

profile play an important role in determining the *relative* importance of scattering at different locations along the channel [29]. In other words, the "critical" length l changes with different scattering conditions and may not be merely defined as the k_BT length [36].

Experimentally, r_{sat} extraction has been developed based on several assumptions (i.e., $\lambda = 2k_BT\mu_0/q\upsilon_{therm}$, l = the k_BT length, μ_0 = the low-field mobility, and the non-degenerate limit) in (7) [7]-[10]. To fulfill the role of scattering in nanoscale transistors (descriptions above), these assumptions can not be allowed. In the next section, we will present a self-consistent technique, in which these assumptions are not needed.

4.3 A new self-consistent temperature-dependence extraction method

The temperature-dependent analytic model can been derived from (7) as [10]

$$\frac{\partial I_{d,sat}}{I_{d,sat}\partial T} = \left[-\frac{\partial V_{T,sat}}{(V_{gs}-V_{T,sat})\partial T} - \left(\frac{1}{1+r_{sat}} + \frac{1}{1-r_{sat}} \right) \frac{\partial r_{sat}}{\partial T} + \frac{1}{\upsilon_{therm}} \frac{\partial \upsilon_{therm}}{\partial T} \right] \tag{8}.$$

Note that $\partial r_{sat}/\partial T = -[(\beta-\gamma)r_{sat}(1-r_{sat})]/T$ and $\partial \upsilon_{therm}/\partial T = (\upsilon_{therm}\gamma)/T$ can be observed from the temperature dependence of λ/l and υ_{therm} [21][22]:

$$\upsilon_{therm} \propto T^{\gamma} \tag{9a},$$

and

$$\frac{\lambda}{\ell} = \frac{A}{\upsilon_{therm}} \propto T^{\beta-\gamma} \tag{9b},$$

where β and γ account for the temperature sensitivity of A and υ_{therm}, respectively. Finally, (8) can be expressed as follows:

$$\frac{\lambda}{\ell} = \frac{-2(\beta-\gamma)}{\gamma - \left(\frac{\partial I_{d,sat}}{I_{d,sat}\partial T} + \frac{\partial V_{T,sat}}{(V_{gs}-V_{T,sat})\partial T} \right) T} - 2 \tag{10}.$$

Note that (10) is derived without the following assumptions: $\lambda = (2k_BT\mu_0/q\upsilon_{therm})$, l = the

k_BT length $\propto (k_BT)^{\beta_l}$, μ_0 = the low-field mobility $\propto T^{\beta_\mu}$, and the non-degenerate limit. When these assumptions are made, A can be expressed as [21]

$$A = \frac{2k_BT\mu_0}{q}\left(B\frac{q}{k_BT}\right)^{\beta_l} \propto T^{1+(\beta_\mu-\beta_l)} \quad (11),$$

and (10) reduces to (2). When β_μ = -1.5, β_l = 1and γ = 0.5, we obtain β = -1.5 and (10) reduces to the original model used in [7]-[15] as

$$\frac{\lambda}{\ell} = \frac{-4}{0.5-\left(\frac{\partial I_{d,sat}}{I_{d,sat}\partial T}+\frac{\partial V_{T,sat}}{(V_{gs}-V_{T,sat})\partial T}\right)T} - 2 \quad (12).$$

From the results of Fig. 2, we know ballistic efficiency B as well as r_{sat} can be accurately obtained as long as using accurate parameters. In the following sections, we will examine each parameter separately.

4.3.1 $I_{d,sat}$ and $V_{T,sat}$

Figure 4.3 shows measured $I_{d,sat}$ and $V_{T,sat}$ versus temperature characteristics for the NMOSFET with L_g = 120 nm. Linear temperature dependence of $I_{d,sat}$ and $V_{T,sat}$ can be observed for T = 233 ~ 373 K. From the slope, $\partial I_{d,sat}/\partial T$ and $\partial V_{T,sat}/\partial T$ can then be determined. $V_{T,sat}$ was calculated from the linear threshold voltage $V_{T,lin}$, which was determined by the maximum transconductance method at V_{ds} = 0.05 V, with drain-induced barrier lowering (*DIBL*) consideration, i.e., $V_{T,sat} = V_{T,lin}$ - *DIBL*. Using $V_{T,sat}$ instead of $V_{T,lin}$ in estimating Q_{inv} is important to accurately account for the *DIBL* effect on the reduction of threshold voltage. Fig. 4.4 shows the calculated $-(\partial V_T/\partial T)/(V_{gs}-V_T)$ with and without *DIBL* consideration. Significant discrepancy can be seen as L_g reduces. We have noted that the estimated $-(\partial V_T/\partial T)/(V_{gs}-V_T)$ with *DIBL* consideration shows the same L_g dependence as the simulated $(\partial Q_{inv}/\partial T)/Q_{inv}$ in [20]. Besides, to exclude the doping effect [20] and the non-equilibrium effect [28] for ultra-short channel devices, which may result in Q_{inv} variation, we have confirmed the

validity of $Q_{inv} \approx C_{ox}(V_{gs}\text{-}V_T)$ from capacitance-voltage (C–V) measurements in this study.

4.3.2 β

From (9b) and (11), we know that the physical meaning of β is referred to the mean-free-path λ, the low-field mobility μ_0, and the critical length l. However, the backscattering extraction in previous studies [7]-[15] involves constant β (i.e., β = -1.5 from (11), β_μ = -1.5 and β_l = -1.5) that is not necessarily correct in state-of-the-art MOSFETs with technology innovations (such as halo implantation, high-k dielectric, strain technologies). There are evidences in plenty to show that carrier scattering mechanisms may change from phonon scattering (β_μ = -1.5 [25]) to Coulomb scattering ($\beta_\mu > 0$) for devices with different size and processes [17]-[19]. In addition, in a short channel where the transport is nonstationary we can not consider λ to be independent of the carrier energy [30]. Besides, it has been suggested that the entire channel or a more significant part of channel may participate in the backscattering and thus the critical length l does not follow the concept of the k_BT layer [29][30][32][33][36]. In other words, it is difficult to predict an accurate value of β for nanoscale state-of-the-art MOSFETs. Therefore, we propose to use (9b) and (10) to determine β and λ/l self-consistently. Note that $\lambda = (2k_BT\mu_0/qv_{therm})$, l = the k_BT length $\propto (k_BT)^{\beta_l}$, μ_0 = the low-field mobility $\propto T^{\beta_\mu}$, and the non-degenerate limit need not to be assumed in the self-consistent framework. Fig. 4.5 shows the extracted λ/l versus temperature characteristics for self-consistent β and β = -1.5, respectively. Although the difference between the self-consistently determined β and -1.5 is only 0.315, significant discrepancy in λ/l can be seen. It is worth noting that the temperature dependent of λ/l can satisfy the constraint of (9b) for self-consistent β, but not for β = -1.5.

To further verify the self-consistently determined β, we have directly extracted β_μ

based on the effective mobility μ, which was measured by the split C–V method with the R_{sd} correction [31]. Fig. 4.6 shows the comparison of self-consistent β and β_μ for the device with L_g = 120 nm. Although the effective mobility μ may not be identical to the low field mobility μ_0 (as defined by λ [2][21]), similar V_{gs} dependence can be seen for the self-consistently determined β and the obtained β_μ. The increased β_μ as well as β with decreasing V_{gs} manifests the importance of Coulomb scattering in the weak inversion region [31]. Besides, we have note that the self-consistently determined β shows significant L_g dependence, as shown in Fig. 4.7. It is clear that the self-consistently determined β increases with decreasing L_g. The increased β is attributed to the importance of halo implant and thus Coulomb scattering in short-channel devices [31]. Fig. 4.7 also indicates that the L_g dependence of β needs to be considered in estimating the L_g dependence of ballistic efficiency (Fig. 4.2).

Figure 4.8 shows the extracted r_{sat} and μ for the NMOSFET with L_g = 120 nm. It can be seen that the assumption of β = -1.5 results in insensitive r_{sat}–V_{gs} dependence. On the other hand, the r_{sat} value extracted by the self-consistent β shows significant V_{gs} dependence. The increased r_{sat} with decreasing V_{gs} results from the decreased μ (through λ) and manifests the importance of Coulomb scattering in the weak inversion region [31]. Besides, the decreased potential gradient of the source-channel junction barrier (i.e., increased l) with decreasing V_{gs} may also account for such V_{gs} dependence of the self-consistently extracted r_{sat} [8].

4.3.3 γ

This self-consistent temperature-dependent method still has limitations because of the uncertainty in γ. From (6), we know that γ ranges from 0.5 (non-degenerate limit: $\eta_F \rightarrow 0$) to 0 (degenerate limit: $\eta_F \rightarrow \infty$). In other words, γ may decrease from 0.5 to 0 with increasing V_{gs}. Therefore, we propose using γ = 0.5 as a first approximation and

then estimating the impact of the $\gamma = 0.5$ assumption on the extracted r_{sat}. For example, we extracted r_{sat} based on $\gamma = 0.5$ in Fig. 4.8. To further consider the impact of the $\gamma = 0.5$ assumption on the extracted r_{sat}, we can derive $\partial r_{sat}/\partial\gamma$ (from (1) and (10)) as

$$\frac{\partial r_{sat}}{\partial \gamma} = \frac{r_{sat}(1-r_{sat})}{\gamma - \left(\frac{\partial I_{d,sat}}{I_{d,sat}\partial T} + \frac{\partial V_{T,sat}}{(V_{gs}-V_{T,sat})\partial T} \right) T} \quad (13).$$

Since the right-hand-side (RHS) value of (13) is positive, an overestimated γ ($\Delta\gamma$) results in an overrated r_{sat} (Δr_{sat}). Based on (13), we can calculate Δr_{sat} for the extracted r_{sat} in Fig. 4.8. Fig. 4.9 shows the corrected r_{sat} vs. V_{gs} characteristics for $\Delta\gamma = 0 \sim 0.5$. It can be see that r_{sat} is insensitive to $\Delta\gamma$ in the weak inversion region. Besides, it should be noticed that γ is near 0.5 (i.e., $\Delta\gamma \rightarrow 0$) with decreasing V_{gs}. In other words, the extracted r_{sat} in the weak inversion region is more accurate than in the strong inversion region. Although $\Delta\gamma$ as well as Δr_{sat} may be significant in the strong inversion region, the maximum error of $\Delta\gamma$ (i.e., $\Delta\gamma = 0.5$, $\gamma = 0$ for the degenerate limit) is not expected for present devices with multi-subband population of carriers. For example, it has been observed for the multi-gate 12-nm-Si-thickness SOI MOSFET that $\gamma \approx 0.2$ (i.e., $\Delta\gamma = 0.3$) based on Multi-Subband-Monte-Carlo simulations [20]. In addition, we propose several experimental guidelines in the following section to increase accuracy of r_{sat} extraction.

4.3.4 Experimental guidelines

1. As revealed from (13), to reduce the impact of $\Delta\gamma$, one can reduce the RHS value of (13) by increasing the measurement temperature.
2. $\Delta\gamma$ can also be reduced when temperature increases because the degenerate effect is reduced and $\eta_F \rightarrow 0$ (i.e., $\gamma \rightarrow 0.5$).
3. To keep the same baseline and minimize possible errors due to different η_F, comparison under the same gate overdrive is needed.

4. For the extracted r_{sat} at the same gate overdrive, its Δr_{sat} may be of similar magnitude. Therefore, Δr_{sat} may not be important for comparative purposes because similar Δr_{sat} can be canceled out.
5. Since the extracted r_{sat} is more accurate in the weak inversion region, comparing from the weak inversion region to the strong inversion is suggested.
6. Once γ can be exactly observed by other method, such as Monte-Carlo simulations [20], one can use (13) to estimate and correct Δr_{sat}.
7. In case the Q_{inv} is different from $C_{ox}(V_{gs}\text{-}V_T)$, one can directly obtain $(\partial Q_{inv}/\partial T)/Q_{inv}$ from the C–V measurement instead of using $-(\partial V_T/\partial T)/(V_{gs}\text{-}V_T)$ in (10).
8. Since the critical length l can be determined by the channel potential [33], r_{sat} should be extracted at the same V_{ds}/L_g to keep the same baseline especially for the L_g-dependent comparison.

Following the above guidelines, several examples of technology comparison for the process monitoring purposes are presented.

4.4 Experimental investigation of Coulomb scattering effects on channel backscattering characteristics

4.4.1 Impact of body doping

Figure 4.10 shows the extracted β and r_{sat} versus $(V_{gs}\text{-}V_{T,sat})$ characteristics for the 100-nm-L_g NMOSFETs with high and low body-doping, N_a. It is clear that the self-consistently determined β really presents the increased β_μ due to increased Coulomb scattering for the high N_a device. Besides, the impact of increasing N_a on r_{sat} can be observed through comparing the extracted r_{sat} at the same gate over drive. In contrast to the result for β = -1.5, the r_{sat} extracted by the self-consistent β is increased for the high N_a device. The increased r_{sat} is consistent with the prediction in [26] and is attribute to increased Coulomb scattering and the reduced carrier mobility [24].

4.4.2 Impact of high-k dielectrics

Co-processed NMOSFETs with HfO_2 and SiO_2 dielectrics were implanted by the same N_a condition and showed similar *DIBL* characteristics. Fig. 4.11 shows the extracted β and r_{sat} versus (V_{gs}-$V_{T,sat}$) characteristics for the 100-nm-L_g NMOSFETs with HfO_2 and SiO_2 dielectrics. It is worth noting that the self-consistently determined β is increased for the HfO_2 dielectric. The result is consistent with the simulation predictions in [19] and can be explained by the active low-energy interfacial phonons [19] and excess Coulomb scattering [27]. Besides, reduced carrier mobility has been reported for high-k devices [19] and was expected to reduce λ as well as increase r_{sat}. On the other hand, as shown in Fig. 4.11(b), the extracted r_{sat} can not respond to the reduced mobility unless the self-consistent β is applied.

4.5 Experimental investigation of impacts of process induced uniaxial strain on channel backscattering characteristics

4.5.1 Devices

P-channel MOSFETs with channel direction <110> were manufactured based on state-of-the-art CMOS technology on 300-mm p-type (100) silicon substrate. Process-induced uniaxial strained-silicon technologies featuring compressive SiGe source/drain and compressive contact etch stop layer (CESL) were employed in this study [9][10][23][24]. Co-processed strained and unstrained PMOSFETs were implanted by the same pocket condition and showed similar drain-induced barrier lowering (*DIBL*) characteristics. Devices with L_g = 50 nm were characterized at T = 223, 298 and 373 K. As shown in Fig. 4.12, the saturated drain current ($I_{d,sat}$) and the linear drain current ($I_{d,lin}$) of the 50-nm-L_g strained device are improved by about 2.1X and 2.9X as compared with its unstrained counterpart, respectively. The threshold voltage of $I_{d,lin}$, $V_{T,lin}$, was determined by the maximum transconductance method. The

threshold voltage of $I_{d,sat}$, $V_{T,sat}$, was calculated from $V_{T,lin}$ with *DIBL* consideration, i.e., $V_{T,sat} = V_{T,lin}$ - *DIBL*. *DIBL* was characterized from the subthreshold characteristics. In order to exclude the parasitic source/drain series resistance (R_{sd}) effect, the constant-mobility method is adopted [18]. The extracted R_{sd} values are about 125 Ω/μm and 214 Ω/μm for strained and unstrained devices, respectively. Based on the measured $I_{d,sat}$–T and $V_{T,sat}$–T characteristics, the following backscattering extraction can be carried out.

4.5.2 Channel backscattering characteristics

Figure 4.13 shows the extracted β and r_{sat} versus $|V_{gs}$-$V_{T,sat}|$ characteristics for the unstrained and strained PMOSFETs with L_g = 50 nm, respectively. It can be seen that the self-consistently determined β is far from -1.5, especially for the unstrained device. Besides, significant V_{gs} dependence of β and r_{sat} can be observed for both devices. It is worth noting that the value of β for the strained PFET is smaller than that of the unstrained one. This result is consistent with the measured $I_{d,sat}$–V_{gs} characteristics, in which the $I_{d,sat}$ of the strained device shows more phonon-limited behavior (i.e., $I_{d,sat}$ decreases as temperature increases) and thus β decreases. Moreover, r_{sat} is actually reduced in the compressive-strained PFET, which is contrary to previous studies [9][10] using β = -1.5.

It must be noticed that strain effects may impact the subband population of carriers and thus the fairness of comparison based on the γ = 0.5 assumption. From (13), we know that an overestimated γ ($\Delta\gamma$) results in an overrated r_{sat}. Since the degenerate effect increases with V_{gs} and is enhanced by strain effects, γ decreases faster for the strained device than that for the unstrained one. In other words, γ as well as r_{sat} is more overestimated in Fig. 4.13(b) for the strained device. Note that the extracted r_{sat} (with self-consistent β in Fig. 4.13(b)) for the strained device is already smaller than that of

the unstrained one. Therefore, the γ = 0.5 assumption will result in underestimation of the impact of compressive strain on the reduction of r_{sat}. In other words, the γ = 0.5 assumption does not change the fact that r_{sat} is actually reduced in the compressive-strained PFET.

To further understand the strain effect, we have investigated υ_{therm}, λ and effective mobility μ for both strained and unstrained PFETs. Based on the self-consistent extracted r_{sat} (Fig. 4.13(b)) and the measured $I_{d,sat}$ (Fig. 4.12(a)), υ_{therm} was calculated from $I_{d,sat} = WC_{ox}(V_{gs}-V_{T,sat})\upsilon_{therm}(1-r_{sat})/(1+r_{sat})$. In addition, λ can be extracted from [35]

$$\frac{I_{d,lin}}{V_{ds}I_{d,sat}} = \frac{(V_{gs}-V_{T,lin})(q/2k_BT)(\lambda/(\lambda+L_g))}{(V_{gs}-V_{T,sat})((1-r_{sat})/(1+r_{sat}))} \quad (14),$$

where the ratio of $I_{d,lin}/V_{ds}$ is determined from the slope of $I_{d,lin}$–V_{ds} characteristics at V_{ds} = 0 V. The effective mobility μ was measured using the split C–V method with R_{sd} correction, as presented in our previous study [24]. Fig. 4.14 shows the extracted υ_{therm}, λ and μ versus V_{gs} characteristics, respectively. It can be seen that the strain-reduced conductivity effective mass m^* leads to an increase of υ_{therm}, λ and μ. Although the effective mobility μ extracted from the split C–V method may not be exactly equivalent to the low field mobility μ_0 as the definition of λ [2][21][35], it is worth noting that the enhancement of backscattering coefficients follows the relation of $\lambda \propto (2k_BT\mu_0/q\upsilon_{therm})$, i.e., 1.9X ($\lambda$ enhancement) ~ 3.3X (μ enhancement) / 1.5X (υ_{therm} enhancement). The strain effect on the enhancement of $1/m^*$ and the relaxation time τ can also be obtained ~2.3X from (υ_{therm} enhancement)^2 and ~1.3X from (λ enhancement)/(υ_{therm} enhancement), respectively. Besides, the λ enhancement is the main reason for the reduction of r_{sat} and pushes the transport of carriers closer to the ballistic regime. Contrary to previous reports [9][10], our study indicates that the ballistic efficiency can

be enhanced by compressive strain for nanoscale PFETs.

From the extracted r_{sat} and λ, the critical length l can be calculated through (1). Since r_{sat} and λ are strongly dependent on V_{gs}, l is extracted under the same gate overdrive for strained and unstrained PFET at different temperatures. Fig. 4.15(a) shows the potential $-k_BT/q$ versus (l_T-l_{233K}) characteristics, which can be viewed as the potential gradient of the source-channel junction barrier (Fig. 4.1). It can be seen that the potential gradient is smaller for the unstrained device. Similar variation in electrostatic potential has been simulated by A. Svizhenko *et al.* [29] for different scattering conditions. It can be understood that more backscattering events for the unstrained device with smaller λ raise the electrostatic potential to higher energy to maintain the same carrier density. Our experimentally observed backscattering effect on the electrostatic potential supports the prediction in [29]. It is, to the best of our knowledge, the first experimental demonstration. In addition, the V_{gs} dependence of the potential gradient is shown in Fig. 4.15(b). It is clear that the potential gradient decreases with decreasing V_{gs}. The decreased potential gradient of the source-channel junction barrier (i.e., increased l) can explain the V_{gs} dependence of r_{sat} for the self-consistent (β_μ-β_l) in Fig. 4.13(b).

4.6 Experimental investigation of channel backscattering for nanoscale SOI MOSFETs

4.6.1 Extraction method with self-heating correction

For silicon-on-insulator (SOI) devices, the self-heating effect significantly influences device temperature and is not considered in this self-consistent temperature-dependent extraction method (Section 4.3). Therefore, a correct backscattering extraction method considering accurate temperature dependence is needed for the characterization of nanoscale SOI devices. According to (10), the

self-heating induced drain current loss can be extracted by

$$\Delta I_{d,sat} = I_{d,sat}\Delta T\left(\frac{\gamma - \frac{2(\beta-\gamma)}{2+\lambda/l}}{T} - \frac{\frac{\partial V_{T,sat}}{\partial T}}{(V_{gs}-V_{T,sat})}\right) \quad (15).$$

The temperature rise $\Delta T = R_{th}I_{d,sat}V_{ds}$, where R_{th} is the thermal resistance [34]. Fig. 4.16 shows the procedure of the extraction with the correction of self-heating effects. After β and λ/l are self-consistently extracted from (9b) and (10), the heating-free drain current ($I_{d,sat}$ + $\Delta I_{d,sat}$) can be obtained from (15) and then is used again to solve the new β and λ/l. This loop is repeated until the true temperature and current are obtained self-consistently. Finally, we can obtain the heating-free coefficients.

The extracted heating-free $I_{d,sat}$ has been confirmed form the measured $I_{d,sat}$–T characteristics. Fig. 4.17 shows that the extracted ΔT is a function of ambient temperature T_0. It means that the ΔT correction is important for the temperature-dependence-based extraction. Note that the T_0 sensitivity of ΔT increases with device power as well as V_{ds}. Fig. 4.18(a) shows the first step (without heating corrections) for the self-consistent determination of β and λ/l. Fig. 4.18(b) shows the extracted λ/l with and without the self-heating correction. It can be seen that after performing the self-heating correction, λ/l increases (i.e., r_{sat} decreases) (Fig. 4.18(b)).

4.6.2 Impact of floating-body and self-heating effects

Figure 4.19 shows the extracted r_{sat}–V_{gs} characteristics for the SOI MOSFETs with L_g = 216 nm and 63 nm using the conventional method (i.e., (12)). Anomalous crossover behavior in the high V_{gs} regime for both devices can be seen. It is worth noting that the V_{ds} dependence of r_{sat} is completely opposite to the backscattering theory, in which r_{sat} decreases with increasing V_{ds} due to reduced l [2].

After considering self-consistent β and self-heating corrections (Fig. 4.20), we can observe accurate V_{gs} and V_{ds} dependence in r_{sat} for both devices. Such V_{gs}

dependence of r_{sat} has been observed in previous Section for the bulk MOSFETs and can be explained by the Coulomb scattering effect and the potential gradient of the source-channel junction barrier (i.e., decreased l) [8]. Note that the self-heating correction is significant with increasing V_{gs} and V_{ds}. It is also worth noting that r_{sat} is more sensitive to V_{ds} in the low V_{gs} regime than in the high V_{gs} regime. In addition, compared to bulk devices with similar size and *DIBL*, we can find that the SOI device has a smaller r_{sat}. The reduced r_{sat} may result from the impact-ionization induced floating-body effect. In other words, the decreased threshold voltage due to floating-body effects results in additional gate overdrive and thus further reduces r_{sat}.

Figure 4.21(a) and 4.12(b) show the extracted β versus V_{ds} characteristics with various V_{gs} for the device with L_g = 216 nm and 63 nm, respectively. At V_{ds} = 0.6 V, it can be seen that $|\beta|$ decreases with decreasing V_{gs}. Since the temperature sensitivity of the l is nearly unchanged for the same device [20], the decreased $|\beta|$ is mainly due to the decreased $|\beta_\mu|$ and can be attributed to the Coulomb scattering in the weak inversion region. When V_{ds} increases, however, the reduction of threshold voltage (due to floating-body effects) pushes the SOI device toward strong inversion. Therefore, the scattering mechanism of carriers becomes more phonon-limited and $|\beta_\mu|$ increases. It is worth noting in Fig. 4.20 that $|\beta|$ increases with V_{ds} especially for low V_{gs}. Besides, we can see that $|\beta|$ is a function of V_{gs} and V_{ds}, similar to the channel conductance G_{ds} (= dI_d/dV_{ds}) that is determined by floating body effects.

4.7 Application of ballistic efficiency to suppression of drain current variation

A simple expression relating I_d of nanoscale MOSFETs to μ_0 has been derived by Lundstrom [35] as

$$\delta I_d / I_d = (\delta\mu_0 / \mu_0)(1 - B) \quad (16),$$

in which the sensitivity of I_d to μ_0 is determined by the ballistic efficiency B. Eq. (16) reveals that the impact of the μ_0 variation, $\sigma(\mu_0)/\mu_0$, on the $I_{d,sat}$ variation, $\sigma(I_{d,sat})/I_{d,sat}$, can be suppressed when the ballistic efficiency B is enhanced. To ensure that the V_T variation does not affect the following analysis, we have confirmed in Fig. 4.22 that the standard deviation of V_T, $\sigma(V_T)$, as well as the V_T variation, $\sigma(V_T)/V_T$, are similar between strained and unstrained devices. The linear dependence of $\sigma(I_{d,sat})/I_{d,sat}$ on $\sigma(\mu_0)/\mu_0$ presented in Fig. 4.23 follows the prediction of Eq. (16), in which the slope represents the degree of ballistic efficiency B. The reduced slope for strained PFETs (Fig. 4.23) can be explained by the B_{sat} enhancement ($B_{sat,strained}$-$B_{sat,unstrained}$) (Fig. 4.24). It is worth noting that the suppression of $\sigma(I_{d,sat})/I_{d,sat}$ (Fig. 4.23), the B_{sat} enhancement (Fig. 4.24) and the μ enhancement (Fig. 4.24) are more significant with decreasing L_g. Besides, we found that the B enhancement decreases with decreasing V_{ds} (Fig. 4.25), which may be referred to the relation of $B \sim \lambda/(L+\lambda)$ for low V_{ds}, i.e., the λ enhancement is not important for $\lambda/(L+\lambda)$ as $L >> \lambda$. Such V_{ds} dependence of the B enhancement results in the weak suppression in the $\sigma(I_d)/I_d$ vs. $\sigma(\mu_0)/\mu_0$ characteristics measured at V_{ds} = 0.3 V as shown in Fig. 4.26.

4.8 Conclusion

We have reported a generalized temperature-dependent channel backscattering extraction method that can self-consistently determine β in nanoscale MOSFETs. Through comparing the V_{gs} and temperature dependence, we have shown that assuming β_μ and β_l constants will result in unphysical backscattering characteristics. We have also investigated the limitation in the self-consistent approach and proposed guidelines for experimental extraction. Using an generalized temperature-dependent method, we have shown that the r_{sat} of nanoscale PMOSFETs can be reduced by the uniaxially

compressive strain. Besides, r_{sat} is increased for NMOSFETs with higher N_a and HfO_2 dielectric. In addition, our results indicate that both self-heating and floating-body effects are important in the determination of backscattering coefficients. On one hand the floating-body effect may decrease channel backscattering in high drain bias regime, and on the other hand the self-heating effect may increase channel backscattering. We further demonstrate that the strain technology can improve the drain current variation through the enhanced ballistic efficiency. Moreover, the improvement shows L_g and V_{ds} dependence. Since β and r_{sat} can be physically determined by our developed program, the generalized self-consistent temperature-dependent method is competent to be routinely used in technology development for the process monitoring purpose.

References

[1] K. Natori, "Ballistic metal-oxide-semiconductor field effect transistor," *J. Appl. Phys.*, vol. 76(**8**), pp. 4879–4890, Oct. 1994.

[2] M.S. Lundstrom, "Elementary scattering theory of the Si MOSFET," *IEEE Electron Device Letters*, vol. 18(**7**), pp. 361–363, July 1997.

[3] International Technology Roadmap for Semiconductors, 2007, [Online]. Available: http://www.itrs.net/Links/2007ITRS/Home2007.htm.

[4] A. Lochtefeld and D.A. Antoniadis, "On experimental determination of carrier velocity in deeply scaledNMOS: how close to the thermal limit?," *IEEE Electron Device Letters*, vol. 22(**2**), pp. 95–97, Feb. 2001.

[5] V. Barral, T. Poiroux, F. Rochette, M. Vinet, S. Barraud, O. Faynot, L. Tosti, F. Andrieu, M. Casse, B. Previtali, R. Ritzenthaler, P. Grosgeorges, E. Bernard, G. LeCarval, D. Munteanu, J.L. Autran, and S. Deleonibus, "Will strain be useful for 10nm quasi-ballistic FDSOI devices? An experimental study," *Symp. VLSI Tech.*,

pp. 128–129, 2007.

[6] E. Bernard, T. Ernst, B. Guillaumot, N. Vulliet, V. Barral, V. Maffini-Alvaro, F. Andrieu, C. Vizioz, Y. Campidelli, P. Gautier, J.M. Hartmann, R. Kies, V. Delaye, F. Aussenac, T. Poiroux, P. Coronel, A. Souifi, T. Skotnicki, and S. Deleonibus, "Novel integration process and performances analysis of Low STandby Power (LSTP) 3D multi-channel CMOSFET (MCFET) on SOI with metal / high-K gate stack," *Symp. VLSI Tech.*, pp. 17–19, 2008.

[7] M.-J. Chen, H.-T. Huang, K.-C. Huang, P.-N. Chen, C.-S. Chang, and C.-H. Diaz, "Temperature dependent channel backscattering coefficients in nanoscale MOSFETs," *IEDM Tech. Dig.*, pp. 39–42, Dec. 2002.

[8] M.-J. Chen, H.-T. Huang, Y.-C. Chou, R.-T. Chen, Y.-T. Tseng, P.-N. Chen, and C.-H. Diaz, "Separation of channel backscattering coefficients in nanoscale MOSFETs," *IEEE Trans. on Electron Devices*, vol. 51(**9**), pp. 1409–1415, Sept. 2004.

[9] H.-N. Lin, H.-W. Chen, C.-H. Ko, C.-H. Ge, H.-C. Lin, T.-Y. Huang, and W.-C. Lee, "Channel backscattering characteristics of strained PMOSFETs with embedded SiGe source/drain," *IEDM Tech. Dig.*, pp. 141–144, Dec. 2005.

[10] H.-N. Lin, H.-W. Chen, C.-H. Ko, C.-H. Ge, H.-C. Lin, T.-Y. Huang, and W.-C. Lee, "Channel backscattering characteristics of uniaxially strained nanoscale CMOSFETs," *IEEE Electron Device Letters*, vol. 26(**9**), pp. 676–678, Sept. 2005.

[11] K.-W. Ang, K.-J. Chui, H.-C. Chin, Y.-L. Foo, A. Du, W. Deng, M.-F. Li, G. Samudra, N. Balasubramanian, and Y.-C. Yeo, "50 nm Silicon-On-Insulator N-MOSFET Featuring Multiple Stressors: Silicon-Carbon Source/Drain Regions and Tensile Stress Silicon Nitride Liner," *Symp. VLSI Tech.*, pp. 66–67, 2006.

[12] K.-W. Ang, H.-C. Chin, K.-J. Chui, M.-F. Li, G. Samudra, and Y.-C. Yeo, "Carrier

Backscattering Characteristics of Strained N-MOSFET Featuring Silicon-Carbon Source/Drain Regions," *Proc. ESSDERC*, pp. 89–92, 2006.

[13] M.H. Liao, C.W. Liu, L. Yeh, T.-L. Lee, and M.-S. Liang, "Gate width dependence on backscattering characteristics in the nanoscale strained complementary metal-oxide-semiconductor field-effect transistor," *Appl. Phys. Letters*, vol. 92(**6**), p. 063506, Feb. 2008.

[14] V. Barral, T. Poiroux, M. Vinet, J. Widiez, B. Previtali, P. Grosgeorges, G. Le Carval, S. Barraud, J.L. Autran, D. Munteanu, and S. Deleonibus, "Experimental determination of the channel backscattering coefficient on 10–70 nm-metal-gate Double-Gate transistors," *Solid-State Electronics*, vol. 51(**4**), pp. 537–542, April 2007.

[15] S.S. Chung, Y.J. Tsai, P.W. Liu, C.H. Tsai, Y.H. Lin, C.T. Tsai, G.H. Ma, S.C. Chien, and S.W. Sun "A Roadmap of Backscattering for the Strained CMOS Devices in the Ballistic Regime," *Proc. Silicon Nanoelectronics Workshop*, Kyoto, Japan, pp. 19–20, June 2007.

[16] W. Lee and P. Su, "Investigation of channel backscattering characteristics for nanoscale SOI MOSFETs using a new temperature-dependent method," *IEEE Int. SOI Conf.*, 2008.

[17] A. Cros, K. Romanjek, D. Fleury, S. Harrison, R. Cerutti, P. Coronel, B. Dumont, A. Pouydebasque, R. Wacquez, B. Duriez, R. Gwoziecki, F. Boeuf, H. Brut, G. Ghibaudo, T. Skotnicki, "Unexpected mobility degradation for very short devices : A new challenge for CMOS scaling," *IEDM Tech. Dig.*, Dec. 2006.

[18] A. Khakifirooz, and D.A. Antoniadis, "MOSFET Performance Scaling—Part I: Historical Trends," *IEEE Trans. on Electron Devices*, vol. 55(**6**), pp. 1391–1400, June 2008.

[19] Z. Ren, M.V. Fischetti, E.P. Gusev, E.A. Cartier, and M. Chudzik, "Inversion channel mobility in high-k high performance MOSFETs," *IEDM Tech. Dig.*, pp. 33.2.1–33.2.4, Dec. 2003.

[20] M. Zilli, P. Palestri, D. Esseni, L. Selmi, "On the experimental determination of channel back-scattering in nanoMOSFETs," *IEDM Tech. Dig.*, pp. 105–108, Dec. 2007.

[21] A. Rahman and M.S. Lundstrom, "A Compact Scattering Model for the Nanoscale Double-Gate MOSFET," *IEEE Trans. on Electron Devices*, vol. 49(**3**), pp. 481–489, March 2002.

[22] E. Pop, C.O. Chui, S. Sinha, R. Dutton, and K. Goodson, "Electron-thermal comparison and performance optimization of thin-body SOI and GOI MOSFETs," *IEDM Tech. Dig.*, Dec. 2004.

[23] P. Su and J.-Y. Kuo, "On the Enhanced Impact Ionization in Uniaxial Strained p-MOSFETs," *IEEE Electron Device Letters*, vol. 28(7), pp. 649–651, July 2007.

[24] W. P.-N. Chen, P. Su, and K.-I. Goto, "Investigation of Coulomb Mobility in Nanoscale Strained PMOSFETs," *IEEE Trans. on Nanotechnology*, vol. 7(**5**), pp. 538–543, Sep. 2008.

[25] D.S. Jeon and D.E. Burk, "MOSFET Electron Inversion Layer Mobilities–A Physically Based Semi-Empirical Model for a Wide Temperature Range," *IEEE Trans. on Electron Devices*, vol. 36(**8**), pp. 1456–1463, Aug. 1989.

[26] T. Skotnicki, C. Fenouillet-Beranger, C. Gallon, F. Boeuf, S. Monfray, F. Payet, A. Pouydebasque, M. Szczap, A. Farcy, F. Arnaud, S. Clerc, M. Sellier, A. Cathignol, J.-P. Schoellkopf, E. Perea, R. Ferrant, and H. Mingam, "Innovative Materials, Devices, and CMOS Technologies for Low-Power Mobile Multimedia," *IEEE Trans. on Electron Devices*, vol. 55(**1**), pp. 96–130, Jan. 2008.

[27] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, H. Satake, and N. Fukushima, "Additional Scattering Effects for Mobility Degradation in Hf-silicate Gate MISFETs," *IEDM Tech. Dig.*, p.621, Dec. 2002.

[28] M.V. Fischetti, L. Wang, B. Yu, C. Sachs, P.M. Asbeck, Y. Taur, and M. Rodwell, "Simulation of Electron Transport in High-Mobility MOSFETs: Density of States Bottleneck and Source Starvation," *IEDM Tech. Dig.*, pp.109–112, Dec. 2007.

[29] A. Svizhenko and M. P. Anantram, "Role of Scattering in Nanotransistors," *IEEE Trans. on Electron Devices*, vol. **50**(6), pp. 1459–1466, June 2003.

[30] E. Fuchs, P. Dollfus, G. Le Carval, S. Barraud, D. Villanueva, F. Salvetti, H. Jaouen, and T. Skotnicki, "A new backscattering model giving a description of the quasi-ballistic transport in nano-MOSFET," *IEEE Trans. Electron Devices*, vol. **52**(10), pp. 2280–2289, Oct. 2005.

[31] W. P.-N. Chen, P. Su, and K.-I. Goto, "Impact of Process-Induced Strain on Coulomb Scattering Mobility in Short-Channel n-MOSFETs," *IEEE Electron Device Letters*, vol. 29(7), pp. 768–770, July 2008.

[32] P. Palestri, R. Clerc, D. Esseni, L. Lucci, and L. Selmi, "Multi-subband-monte-carlo investigation of the mean free path and of the kT layer in degenerated quasi ballistic nanoMOSFETs," *IEDM Tech. Dig.*, Dec. 2006.

[33] R. Clerc, P. Palestri, and L. Selmi, "On the physical understanding of the kT-layer concept in quasi-ballistic regime of transport in nanoscale devices," *IEEE Trans. on Electron Devices*, vol. 53(**7**), pp. 1634–1640, July 2006.

[34] L.T. Su, J.E. Chung, D.A. Antoniadis, K.E. Goodson, and M.I. Flik, "Measurement and Modeling of Self-Heating in SOI NMOSFET's," *IEEE Trans. on Electron Devices*, vol. 41(**1**), pp. 69–75, Jan. 1994.

[35] M.S. Lundstrom, "On the Mobility Versus Drain Current Relation for a Nanoscale

MOSFET," *IEEE Electron Device Letters*, vol. 22(**6**), pp. 293–295, June 2001.

[36] R. Kim and M.S. Lundstrom, "Physics of carrier backscattering in one- and two-dimensional nanotransistors," *IEEE Trans. on Electron Devices*, vol. 56(**1**), pp. 132–139, Jan. 1994.

[37] W. Lee and P. Su, "Investigation of Channel Backscattering Characteristics in Nanoscale Uniaxial Strained PMOSFETs," *IEEE Trans. on Nanotechnology*, 2009, to be published.

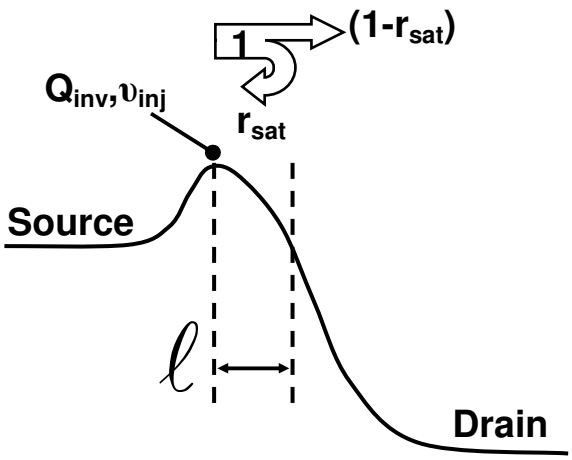


Fig. 4.1. Schematic diagram illustrating the backscattering theory [1]. Carrier in the critical length l is with a backscattering ratio r_{sat}. The average injection velocity υ_{inj} is determined the equilibrium thermal velocity υ_{therm} and r_{sat} as $\upsilon_{inj} = \upsilon_{therm}(1-r_{sat})/(1+r_{sat})$.

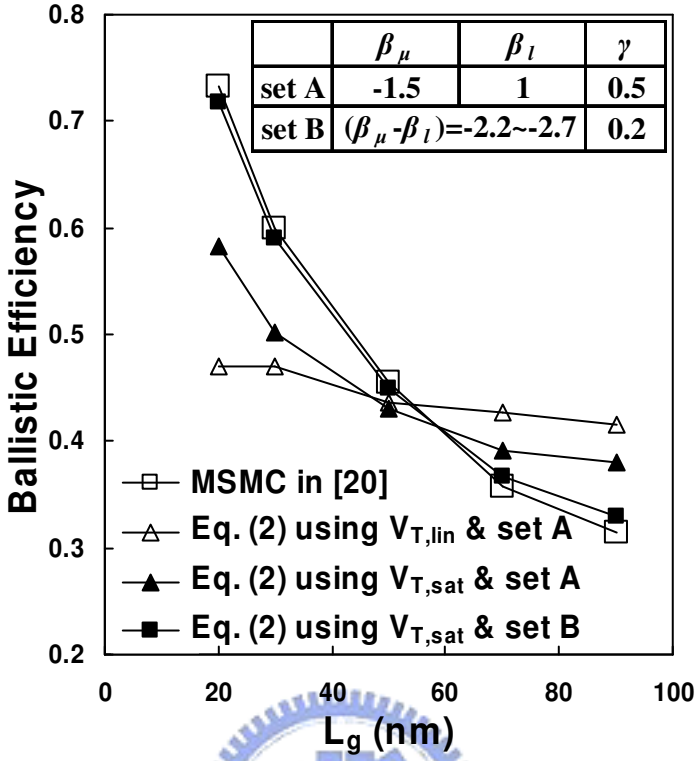


Fig. 4.2. Calculated ballistic efficiency B vs. L_g based on the results of [20] showing the need of accurate $V_{T,sat}$ and $(\beta_\mu$-$\beta_l)$.

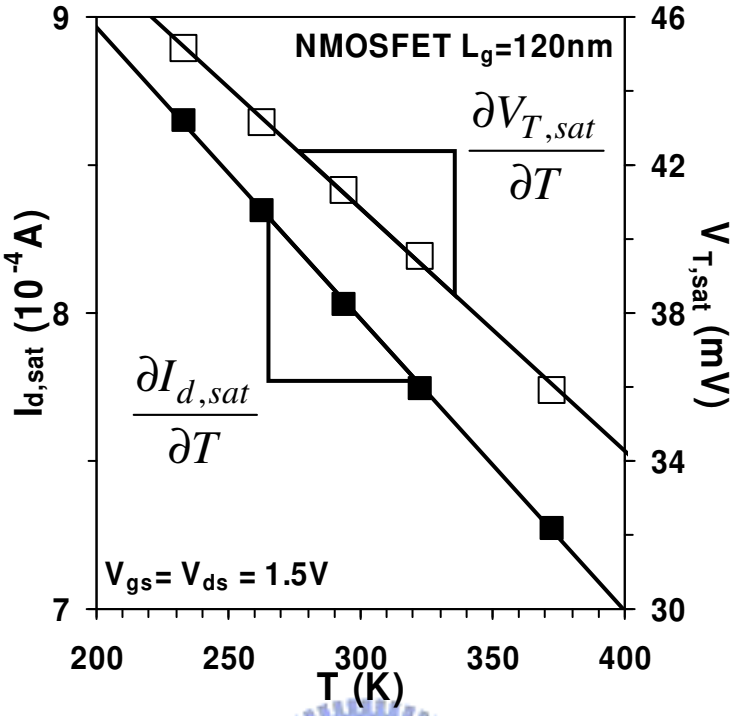


Fig. 4.3. Measured $I_{d,sat}$ and $V_{T,sat}$ vs. T characteristics for the NMOSFET with L_g = 120 nm. Linear dependence of $I_{d,sat}$ and $V_{T,sat}$ on T is shown for T = 233 ~ 373 K. $V_{T,sat}$ is determined by maximum transconductance method with *DIBL* considered, i.e., $V_{T,sat}$ = $V_{T,lin}$-*DIBL*.

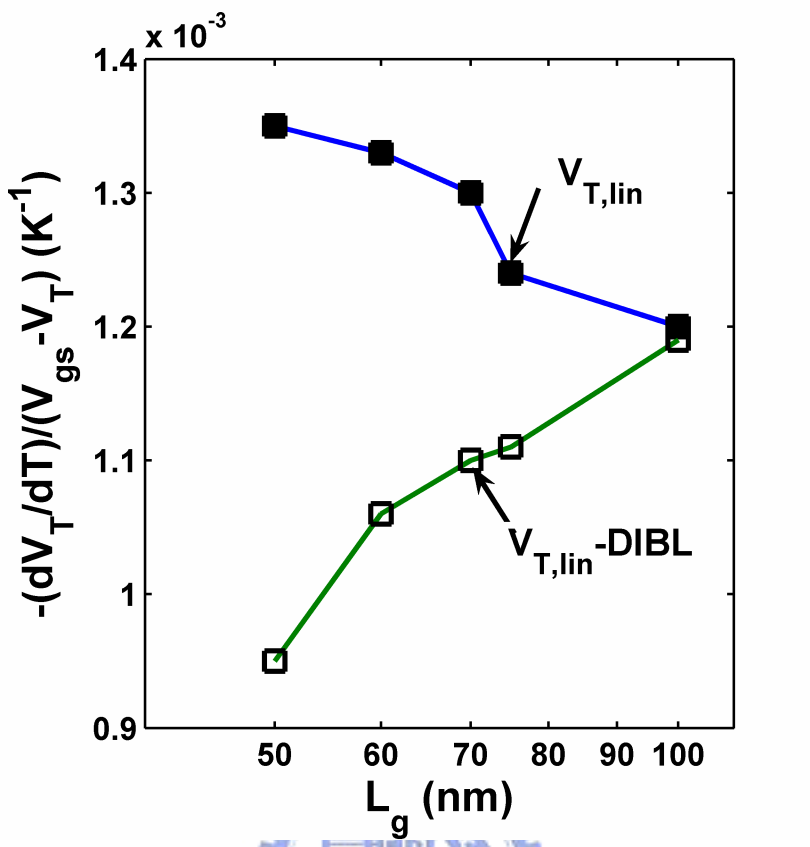


Fig. 4.4. Different estimations of $-(\partial V_T/\partial T)/(V_{gs}-V_T)$. $V_{T,lin}$ is extrapolated from the maximum transconductance. *DIBL* is the gate-voltage difference between gate voltages at I_d = 100 nA/μm for V_{ds} = 0.05 and 1.5 V.

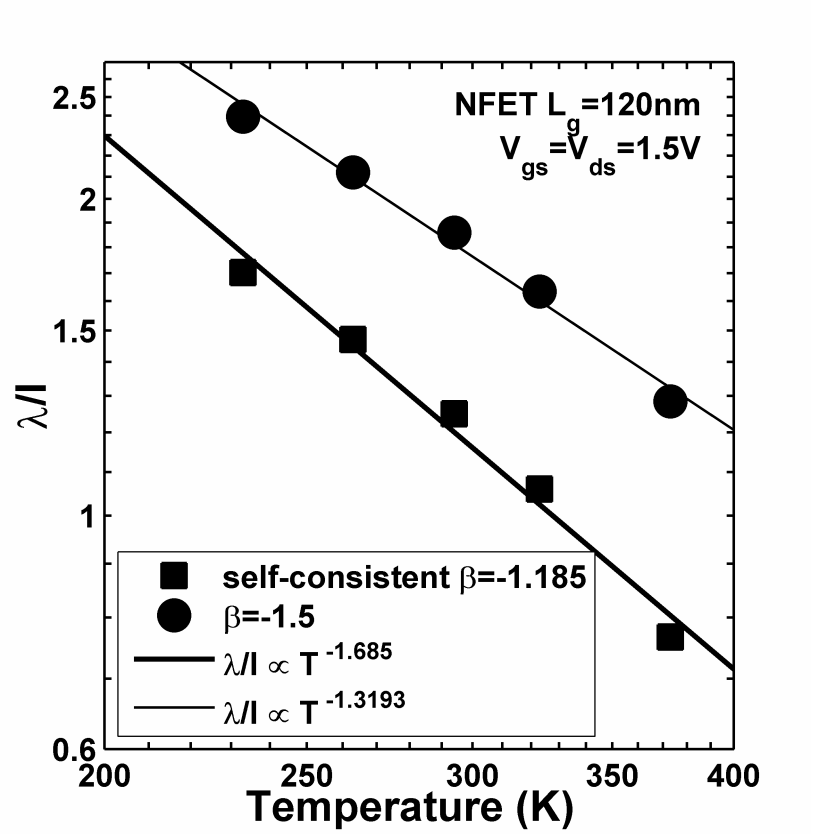


Fig. 4.5. λ/l vs. T characteristics shows the need of self-consistent β for the backscattering coefficient extraction. In [7]-[15], β = -1.5 from $\beta = 1+(\beta_\mu-\beta_l)$, β_μ = -1.5 and β_l = 1. Note that different values of $I_{d,sat}$ and $V_{T,sat}$ are considered in (4) at the corresponding temperature.

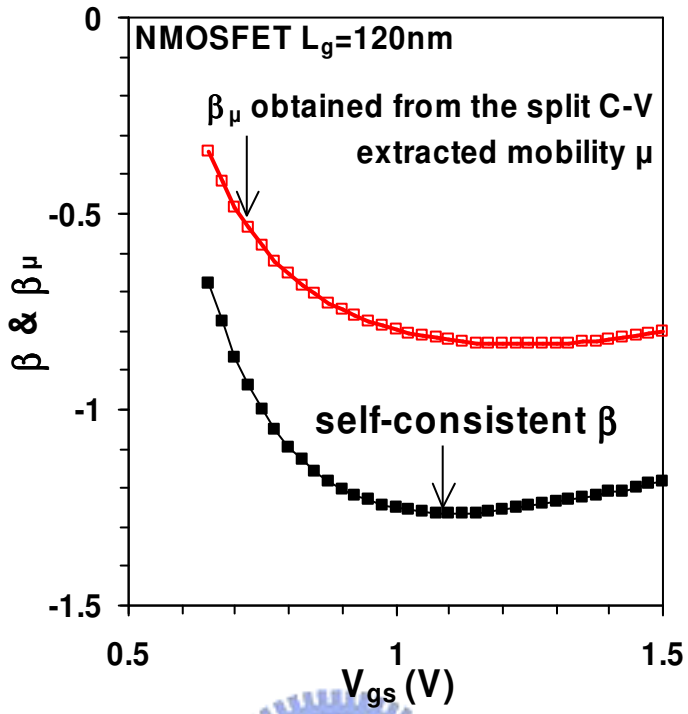


Fig. 4.6. Extracted β and β_μ vs. V_{gs} characteristics for the NMOSFET with L_g = 120 nm. β_μ (–□–) is observed based on the effective mobility μ, which is extracted at different temperature by the split C–V method with R_{sd} correction.

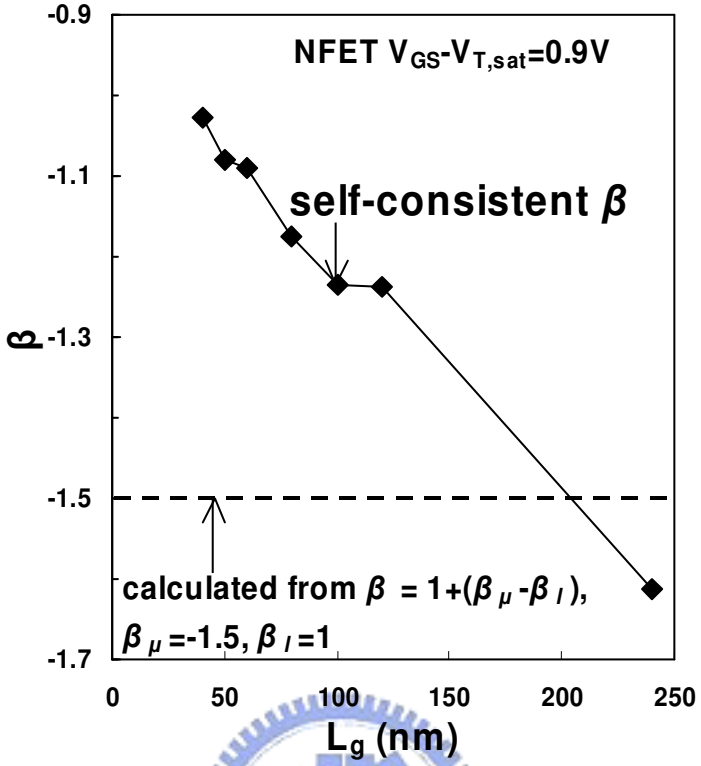


Fig. 4.7. Extracted β vs. L_g characteristics for NMOSFETs at V_{GS}-$V_{T,sat}$ = 0.9 V. The self-consistently extracted β shows significant L_g dependence.

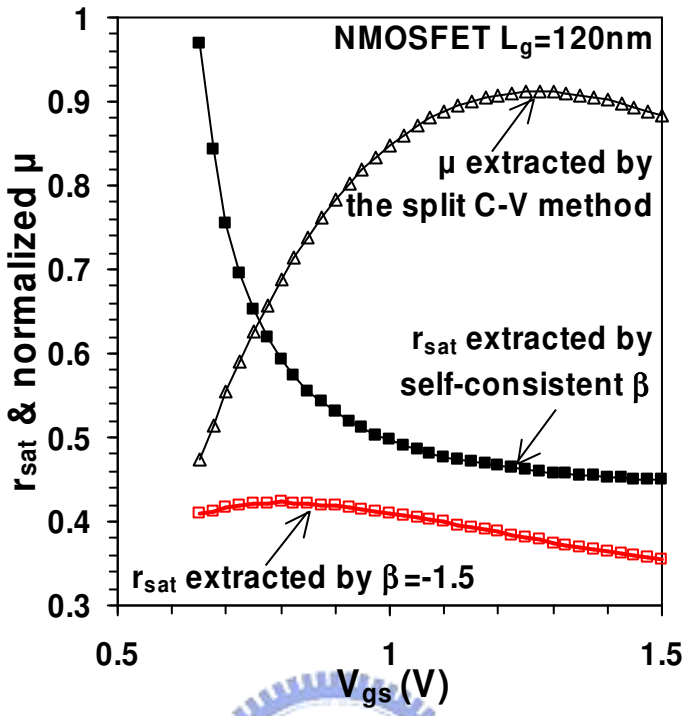


Fig. 4.8. Extracted r_{sat} and the effective mobility μ vs. V_{gs} characteristics for the NMOSFET with L_g = 120 nm.

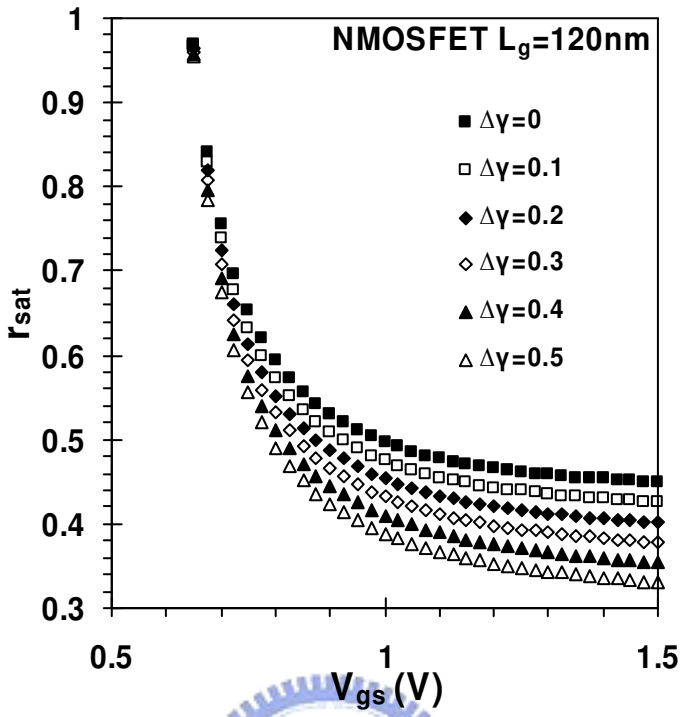


Fig. 4.9. Extracted r_{sat} vs. V_{gs} characteristics for the NMOSFET with L_g = 120 nm with different $\Delta\gamma$ corrections.

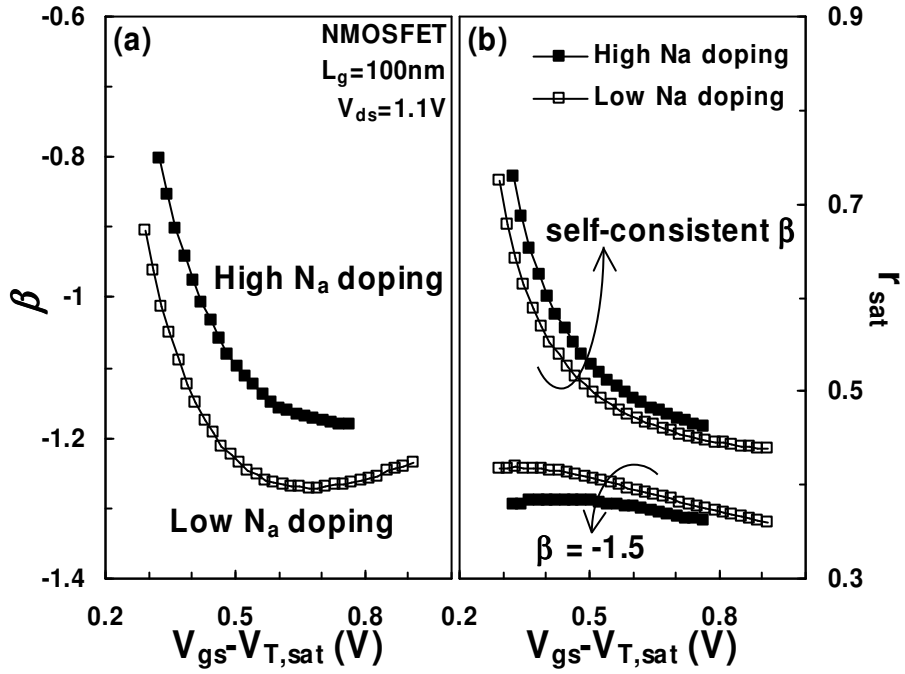


Fig. 4.10. (a) Extracted β and (b) r_{sat} vs. (V_{gs}-$V_{T,sat}$) characteristics for 100-nm-L_g NMOSFETs with high and low body-doping N_a.

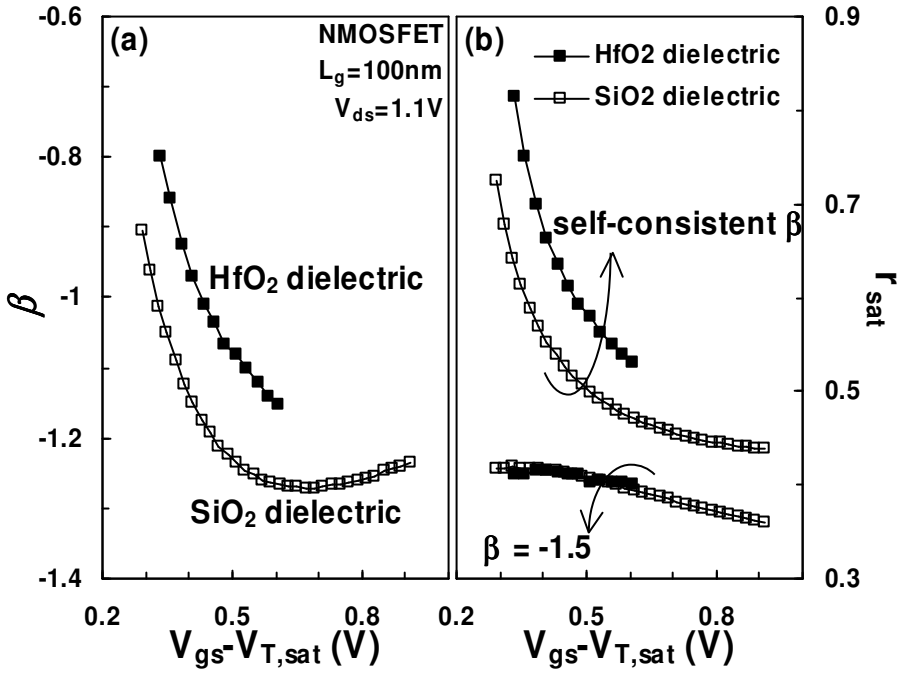


Fig. 4.11. (a) Extracted β and (b) r_{sat} vs. (V_{gs}-$V_{T,sat}$) characteristics for 100-nm-L_g NMOSFETs with HfO_2 and SiO_2 gate dielectrics.

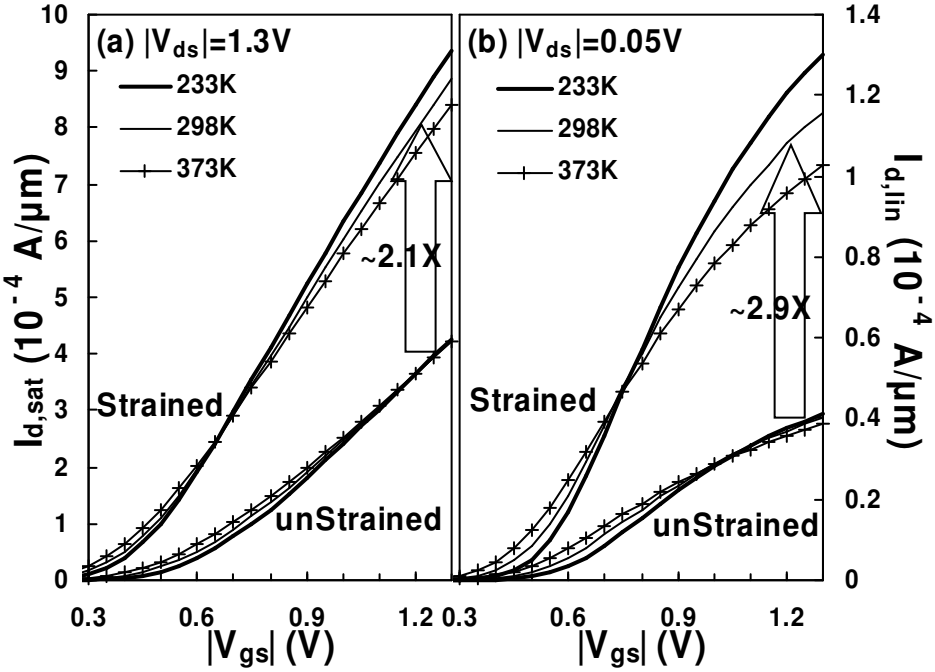


Fig. 4.12. Measured drain-current vs. gate voltage characteristics for 50-nm-L_g PMOSFETs with and without uniaxially compressive strain at T = 233, 298, 373 K for (a) $|V_{ds}|$ = 0.05 V and (b) $|V_{ds}|$ = 1.3 V.

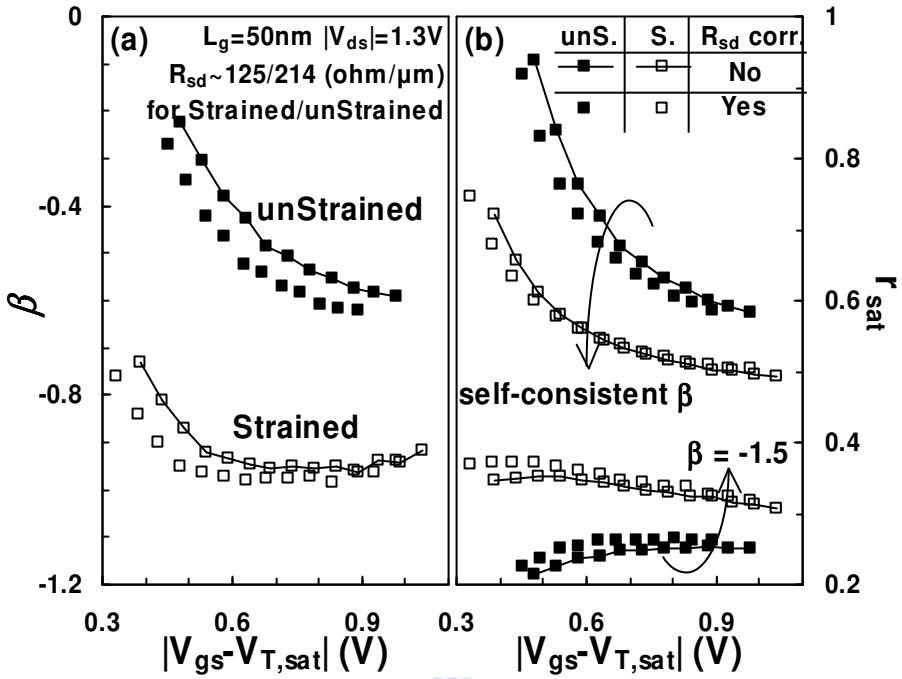


Fig. 4.13. (a) Extracted β and (b) r_{sat} vs. $|V_{gs}-V_{T,sat}|$ characteristics for 50-nm-L_g PMOSFETs with and without uniaxially compressive strain [23][24]. The R_{sd} effect has been corrected. (R_{sd} ~ 125 Ω/um for the strained device and 214 Ω/um for the unstrained device).

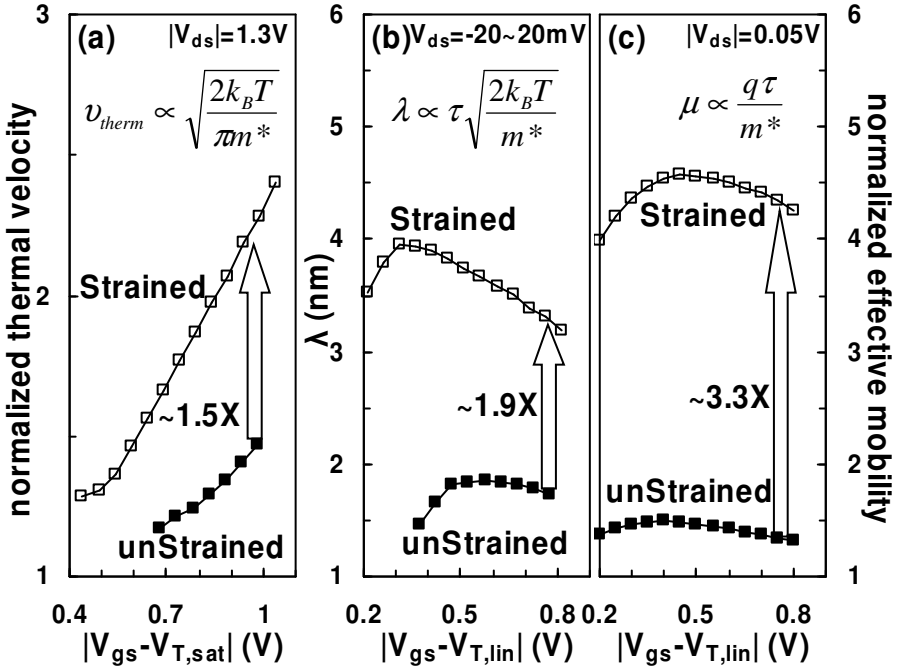


Fig. 4.14. Extracted (a) thermal velocity v_{therm}, (b) mean-free path λ and (c) effective mobility μ vs. $|V_{gs}-V_T|$ characteristics for 50-nm-L_g PMOSFETs with and without uniaxially compressive strain at T = 298 K. λ is extracted from the slop of $I_{d,lin}$–V_{ds} characteristics at V_{ds} = -20 ~ 20 mV. Effective mobility is extracted from the split C–V method at V_{ds} = 50 mV with R_{sd} correction [2].

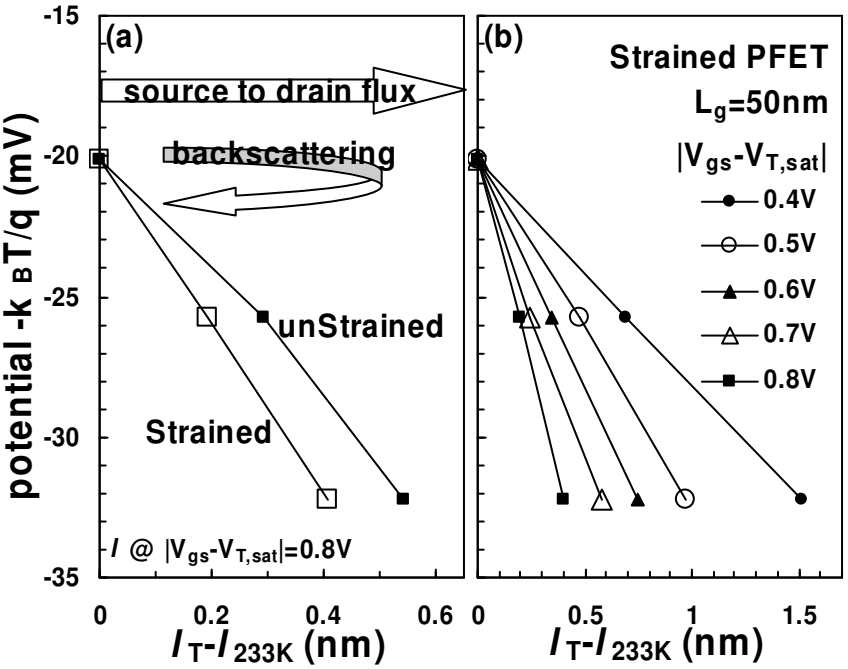


Fig. 4.15. Extracted potential $-k_BT/q$ vs. (l_T-l_{233K}) characteristics for (a) strained and unstrained PMOSFETs with L_g = 50 nm at $|V_{gs}\text{-}V_{T,sat}|$ = 0.8 V and $|V_{ds}|$ = 1.3 V, and (b) the strained PMOSFET with L_g = 50 nm at $|V_{gs}\text{-}V_{T,sat}|$ = 0.4 ~ 0.8V and $|V_{ds}|$ = 1.3 V.

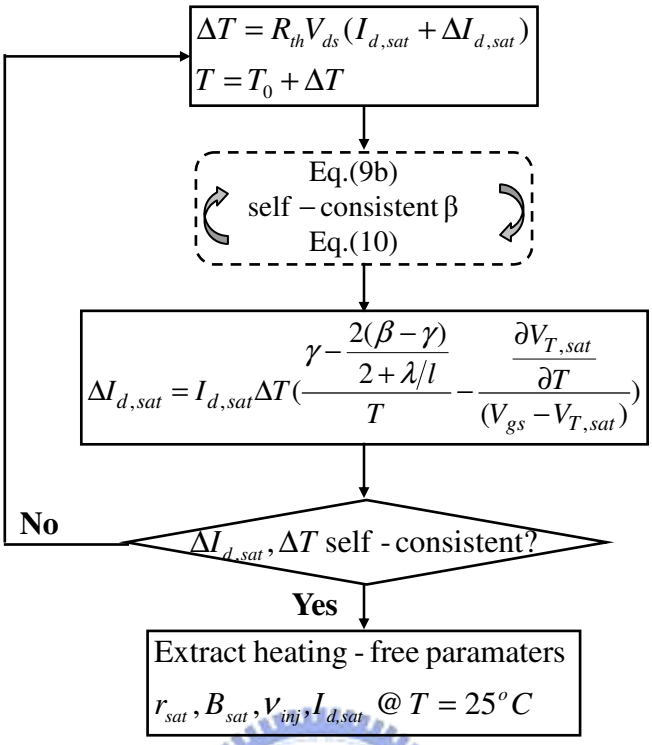


Fig. 4.16. Our self-consistent method considering accurate temperature dependence of carrier mobility and self-heating effects.

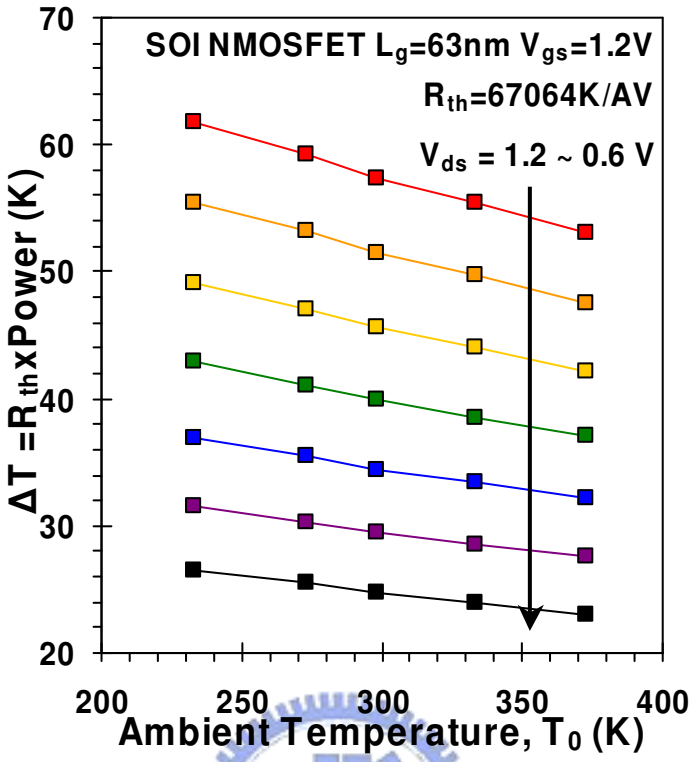


Fig. 4.17. Self-heating induced ΔT vs. ambient temperature T_0 for the SOI MOSFET with L_g = 63 nm. R_{th} (= 67064 K/W) is extracted by the method presented in [34].

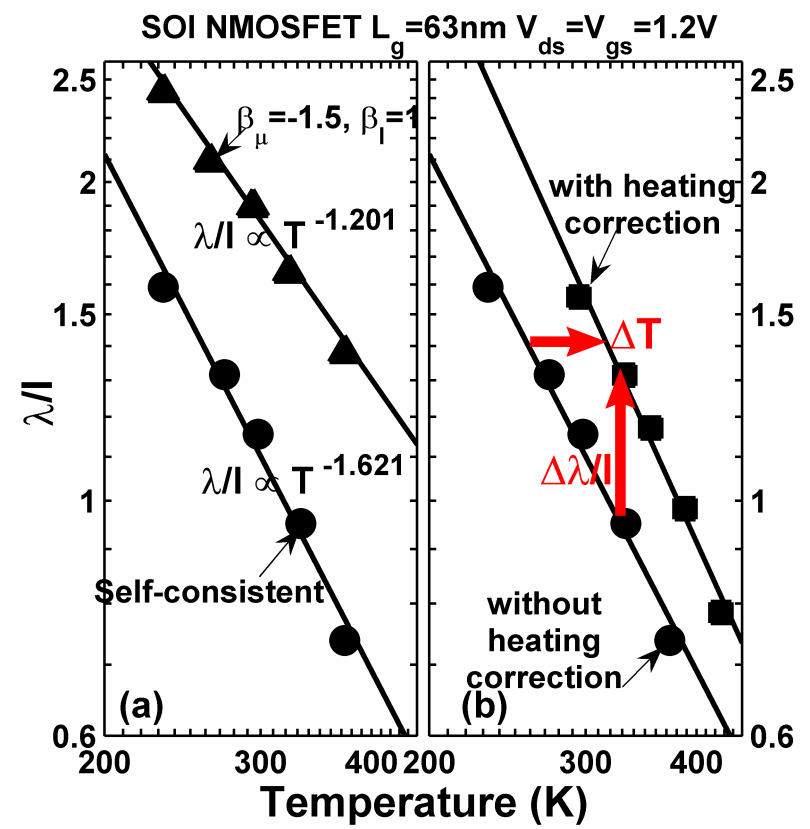


Fig. 4.18. λ/l vs. T characteristics for (a) the constant β = -1.5 (i.e., β_μ = -1.5 and β_l = 1) and the self-consistent β, and (b) the self-consistent β with and without the correction of self-heating.

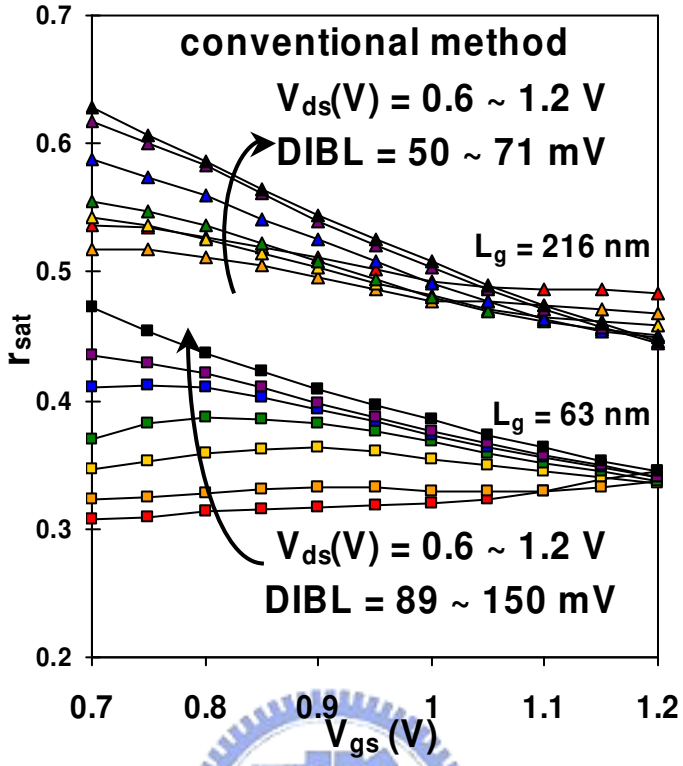


Fig. 4.19. r_{sat} vs. V_{gs} characteristics for SOI NMOSFETs with L_g = 216 nm and 63 nm using the conventional method (i.e., assuming β = -1.5 in (10)).

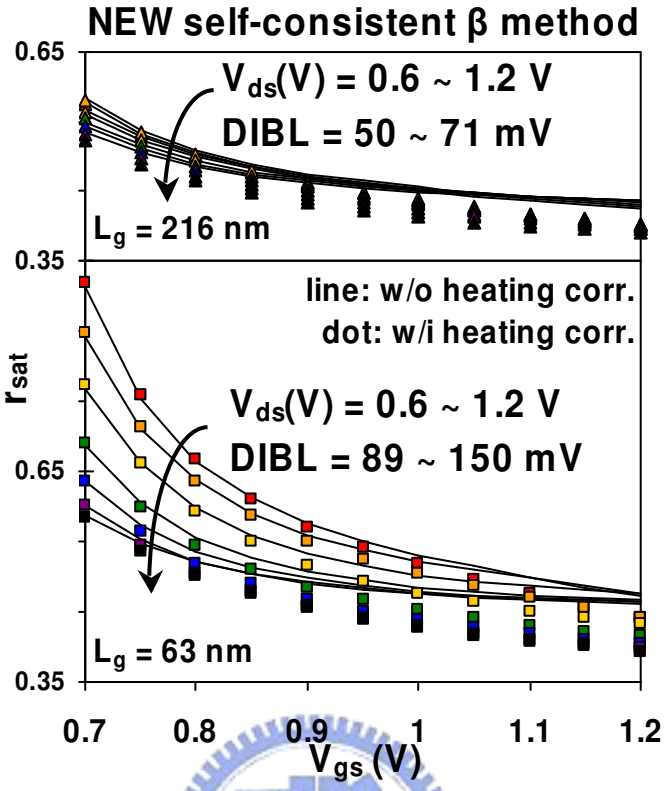


Fig. 4.20. r_{sat} vs. V_{gs} characteristics for SOI NMOSFETs with L_g = 216 nm and 63 nm using the self-consistent method with and without self-heating corrections.

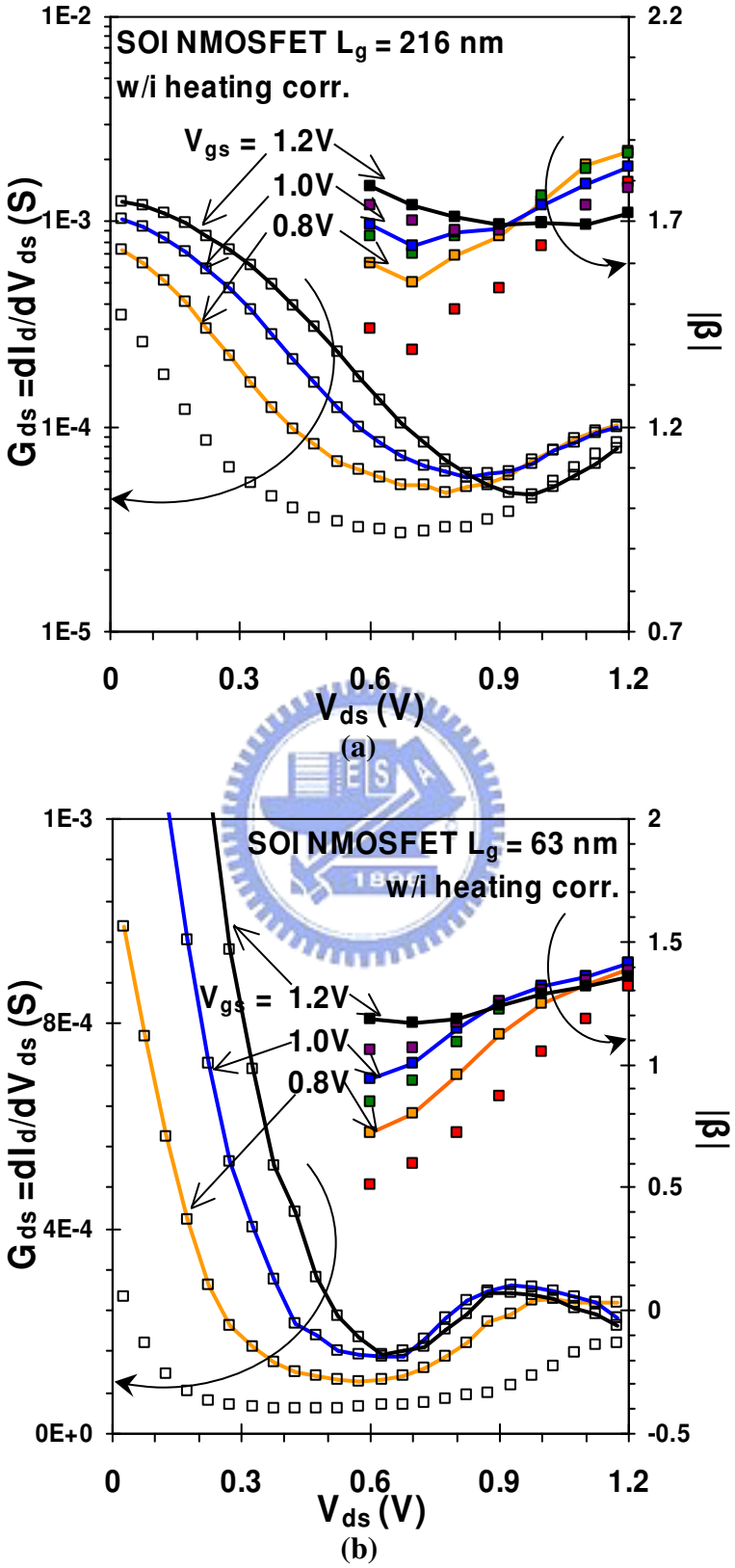


Fig. 4.21. G_{ds} and the extracted β vs. V_{ds} characteristics for SOI NMOSFET with L_g = 216 nm and 63 nm. The floating-body effects can be seen in both G_{ds} and the self-consistently extracted β.

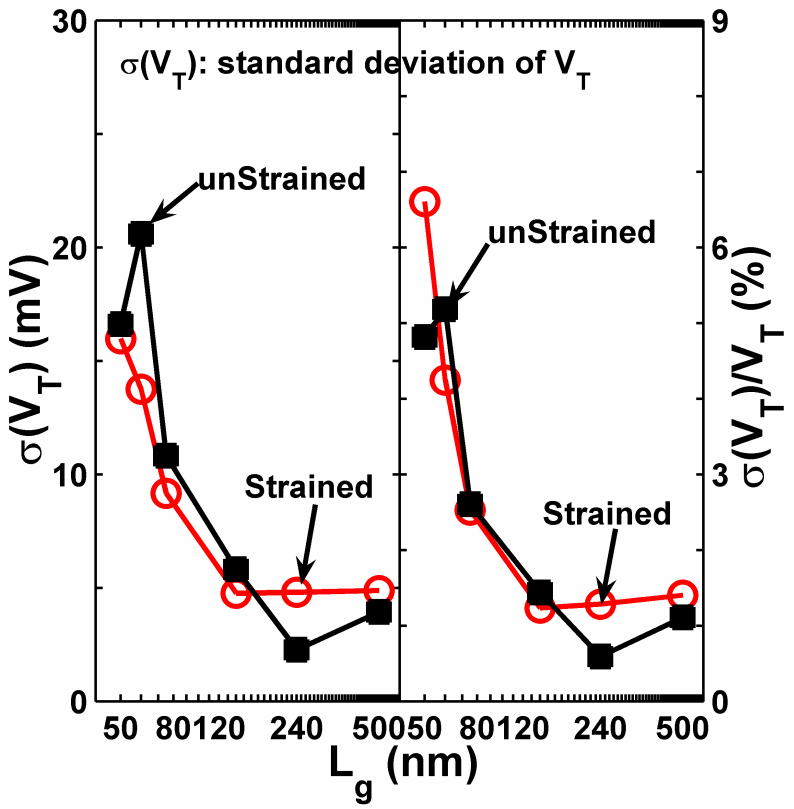


Fig. 4.22. Comparison of σ(V_T) and σ(V_T)/V_T for strained and unstrained PFETs.

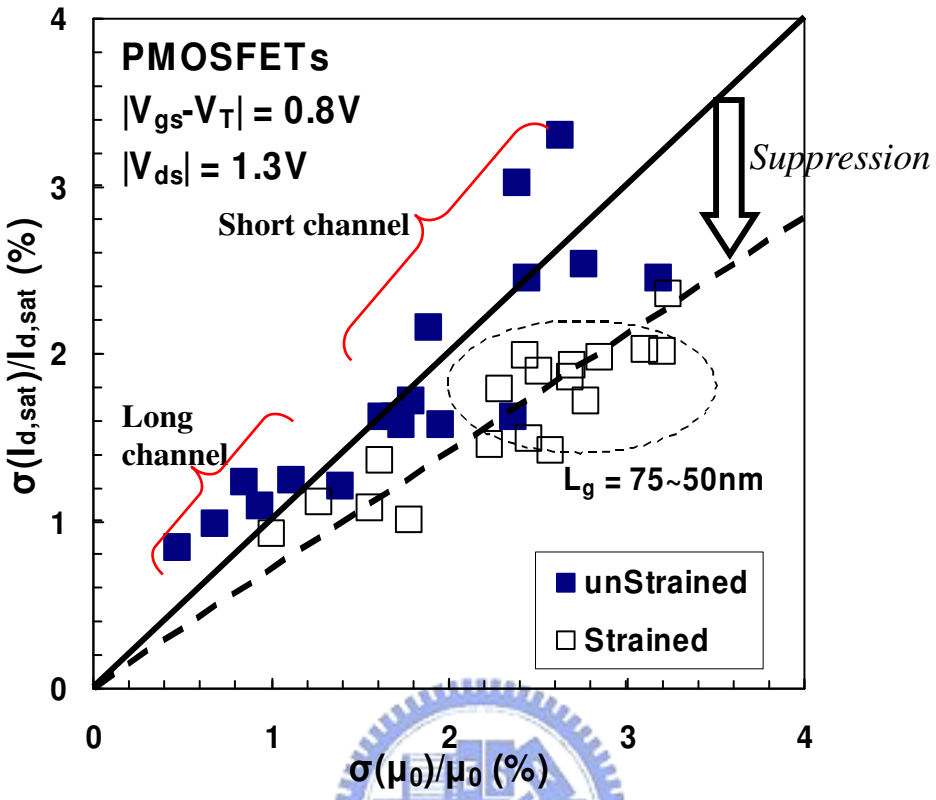


Fig. 4.23. $\sigma(I_{d,sat})/I_{d,sat}$ vs. $\sigma(\mu_0)/\mu_0$ characteristics for strained and unstrained PFETs with L_g = 50 ~ 500 nm at V_{ds} = 1.3 V.

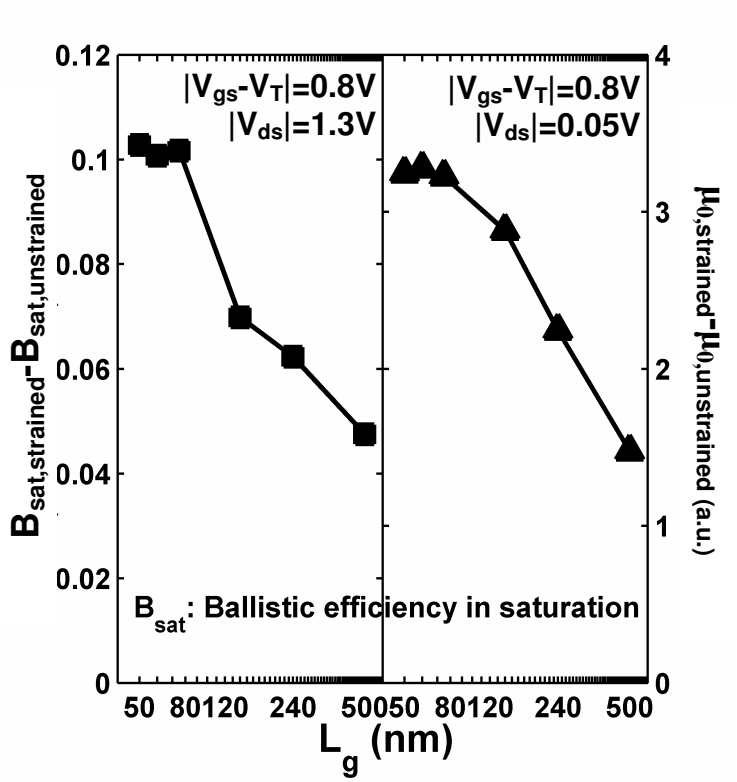


Fig. 4.24. B_{sat} enhancement and μ enhancement vs. L_g characteristics for strained and unstrained PFETs. B_{sat}: ballistic efficiency B in saturation region.

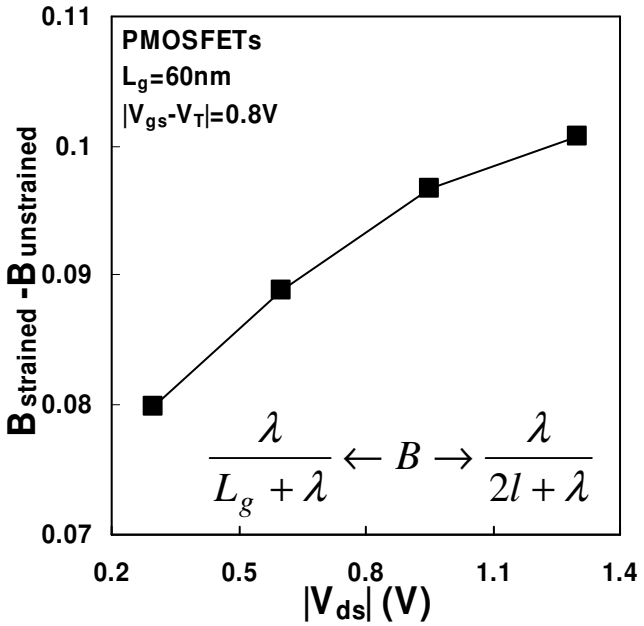


Fig. 4.25. V_{ds} dependence of the ballistic-efficiency enhancement. B is near $\lambda/(2l+\lambda)$ for high V_{ds} and $\lambda/(L_g+\lambda)$ for low V_{ds}.

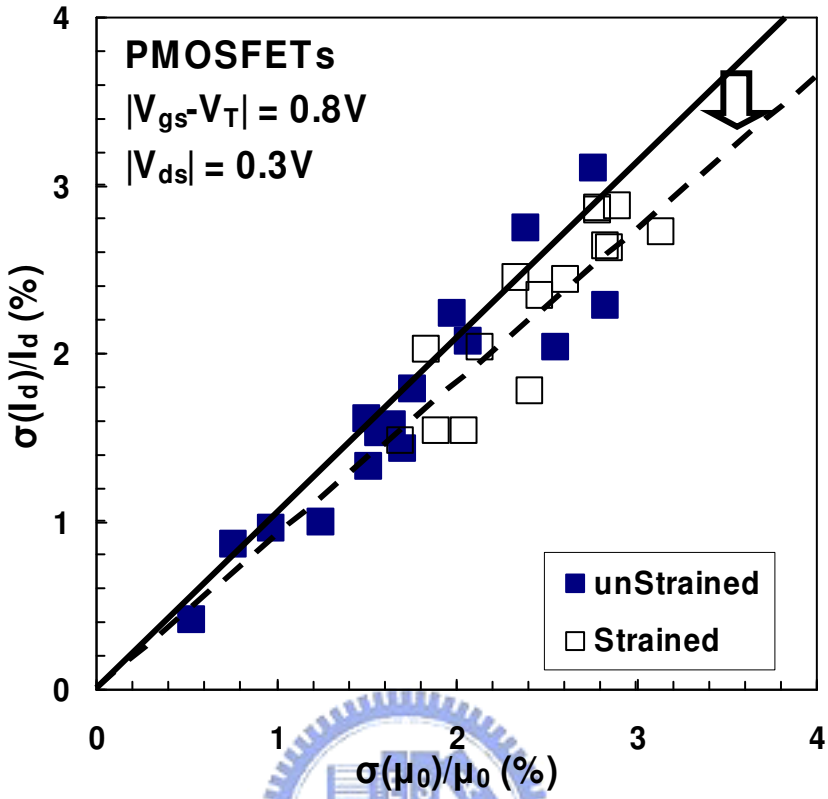


Fig. 4.26. $\sigma(I_d)/I_d$ vs. $\sigma(\mu_0)/\mu_0$ characteristics for strained and unstrained PFETs with L_g = 50 ~ 500 nm at V_{ds} = 0.3 V.

Chapter 5

Gate-Tunneling Current Induced Capacitance-Voltage Problems

5.1 Introduction

The gate capacitance-voltage (C–V) characteristic is fundamental to CMOS technology development because it plays an important role in oxide thickness extraction [21], carrier mobility calculation, interface trap characterization, and so on. As the gate dielectric thickness is reduced (below 20 Å), the inversion C–V characteristic is distorted due to direct tunneling current [1]-[9], [14]-[19]. Since the gate-tunneling current in metal oxide semiconductor (MOS) test structures may result in significant distributed channel resistance effect [5]-[9], several studies proposed conducting C–V measurements using short-channel devices [14]-[18]. Fig. 5.1(a) shows the observed inversion C–V characteristic with adequate calibrations for short-channel devices. Although the inversion C–V characteristic is acceptable for gate bias (V_{GS}) smaller than 1 V, there still is significant C–V distortion for $V_{GS} > 1$ V. One general way to solve this problem is to increase the C–V measurement frequency [14]-[18]. Based on the frequency dependent characteristics, parasitic component effects can be excluded and true C–V characteristics can then be calculated by a certain model of choice. For example, Pantisano *et al.* [15] proposed a C–V measurement from 1 kHz to 100 MHz and an extraction methodology using the three-element model [3]-[4], [22-23]. However, C–V measurements in the high frequency range require high frequency probes (Ground Signal Ground - GSG) and RF (radio frequency) test structures. Moreover, the calibration procedures in high frequency measurements and model-data fitting make the

C–V reconstruction rather time consuming for regular product monitoring. Besides, using these short-channel devices in *C–V* measurements has several drawbacks such as small intrinsic capacitance, large parasitic components and uncertainty in the physical gate length. In other words, the variation of measured capacitance increases as channel length decreases (Fig. 5.1(b)). Therefore, the reconstruction of *C–V* characteristics from long-channel devices is still a crucial issue.

Several studies have constructed the *C–V* characteristics for long-channel devices using distributed circuit approaches [5]-[9]. For example, Barlage *et al*. [7] proposed using a transmission line concept to extract the inversion MOS capacitance. In [5], we employed segmented SPICE simulation with each sub-transistor modeled by the BSIM4 MOSFET model to simulate the anomalous *C–V* curves due to gate tunneling. Although these methods may provide well-restored characteristics, the implementation is too complicated to be routinely used in a technology development. To develop a simple method for the inversion *C–V* reconstruction, the challenge lies in capturing the distributed nature of the gate capacitance and the channel resistance in a compact way. This is analogous to the gate input impedance modeling in the compact model development for RF CMOS, where an intrinsic input resistance has been introduced [10] as a major part of the gate input resistance. In this chapter, we investigate the inversion *C–V* reconstruction and assess the feasibility of the concept of intrinsic input resistance for long-channel MOSFETs.

This chapter is organized as follows. In Section 5.2, devices and measurements in this work are presented. In Section 5.3, we describe BSIM4-based macro model using in this study, and identify mechanisms responsible for the inversion *C–V* attenuation in short-channel as well as long-channel devices. In Section 5.4, we investigate the validity of the concept of intrinsic input resistance. In Section 5.5, we assess the feasibility of

the intrinsic input resistance approach for the inversion *C–V* reconstruction. The conclusion will be drawn in Section 5.6.

5.2 Devices and measurements

Standard MOSFETs with doped poly-Si gate electrode were fabricated and tested in this study. The equivalent oxide thickness (EOT) is about 11 Å. The transistor gate length (L_g) ranges from 0.24 to 10 μm with 10-μm width (W). For the short-channel device with L_g = 0.24 μm, we employed a test structure with 15-array devices in parallel. Our *C–V* measurement was carried out using the impedance analyzer Agilent 4294A and the Cascade Microtech probe system (S300 series) with DCP 100 probes. Under the RC parallel mode, the Hi port of Agilent 4294A was connected to source/drain, while the Lo port was connected to the gate electrode (SD-G case). The measurement principle of Agilent 4294A is the Four-Terminal Pair (4TP) configuration with Auto-Balancing-Bridge (ABB) method [13]. In the 4TP configuration, the outer shield of leads of Agilent 4294A needs to be connected together to provide a current return path to cancel the magnetic field generated by the inner current loop [13]. Besides, the whole system of the *C–V* measurement needs to be isolated from actual ground to exclude complicated coupling effects from the ground path and maintain stability of the *C–V* measurement.

Although the cable inductance, L_s, can be removed to a certain extent in the 4TP configuration [13], residual inductance may result in negative capacitance. Fig. 5.2(a) shows the measured inversion MOS capacitance, C_{gc}, with and without an adequate SHORT calibration. Without performing the SHORT calibration, C_{gc} dramatically drops as V_{GS} increases. By an adequate SHORT calibration, the residual L_s (~1 μH in series, Fig. 5.2(a) inset) can be compensated. In addition, L_s and stray capacitances may induce a resonance when the measurement frequency increases [13]. As shown in the Fig.

5.2(b), a resonance at ~30 MHz can be seen. The resonance leads to not only accuracy degradation but also very unstable measurement. To avoid the impact of the resonance, we performed *C–V* measurements in the frequency independent region (Fig. 5.2(b)). It is worth noting that the instrumentation error [19] and the impact of extrinsic capacitances and resistances [1]-[3] are frequency dependent. Therefore, measuring C_{gc} in the frequency independent region may avoid these two mechanisms. In other words, the attenuation in C_{gc} measured in the frequency independent region with adequate calibrations (Δ in Fig. 5.2(a)) can be attributed to mechanisms of the intrinsic device part. After excluding the influences from the extrinsic components in the measurement setup, the C_{gc} data was then used in the following BSIM4-based extraction methodology.

5.3 BSIM4-based macro model and SPICE simulation

Figure 5.3(a) shows the BSIM4-based macro model we used in the simulation of C_{gc}. Segmented SPICE simulation that divides the transistor along the length direction with 10 sub-transistors in series was utilized and the BSIM4 device model parameters were calibrated through our extraction methodology (Fig. 5.3(b)). Our C_{gc} extraction methodology considers both DC and AC characteristics of devices. Basic device DC parameters such as threshold voltage (V_T), gate tunneling current (I_g), mobility (μ) and source/drain resistance (R_{sd}) need to be first determined and used in the AC analysis of SPICE. The oxide thickness, effective channel length, gate electrode resistance (R_{ge}) and the parasitic inductance within the test structure itself (L_i) can then be extracted based on a comparison between the C_{gc} data and the simulation results. The true inversion MOS capacitance can be obtained by the gate-tunneling-free simulation. In the following sections, we discuss various mechanisms associated with the intrinsic device responsible for the anomalous *C–V* characteristics.

5.3.1 Short-channel device

Fig. 5.4(a) shows significant capacitance attenuation in the C_{gc} measurement for the device with L_g = 0.24 μm. The parasitic effects caused by R_{ge}, R_{sd} and L_i are responsible for the attenuation. Note that the impact of source/drain resistance, R_{sd}, and gate electrode resistance, R_{ge}, increases as L_g decreases. In addition, the short-channel test structure is usually designed as a multi-array type to increase the impedance of the capacitor. As a result, the residual on-chip inductance, L_i, may become significant in the multi-array test structure when large current exists. By comparing the C_{gc} measurement data with the L_i-free simulation (Fig. 5.4(a)), it can be seen that the L_i effect is significant in the high gate bias (i.e., high gate tunneling) regime. Moreover, the L_i-induced C_{gc} attenuation depends on the measurement configuration. As shown in Fig. 5.4(b), various measurement configuration may result in various C_{gc} attenuation due to different current direction. In other words, different C–V characteristics may be observed for the multi-array test structure with the same size but different layout. Therefore, the L_i effect increases the uncertainty in the C–V measurement for short-channel devices.

5.3.2 Long-channel device

Fig. 5.5 shows the comparison between simulation and data for the device with L_g = 10 μm. The negative capacitance value results from the cable inductance L_s. Fig. 5.6 shows that the measured L_s is about ~1 μH. After performing the SHORT calibration, we can exclude the L_s effect and observe positive capacitance value (Fig. 5.5). The simulation in Fig. 5.5 reveals that the impact of the gate-tunneling-induced distributed effect is crucial for the long-channel device. Because of the IR drop caused by gate-tunneling current, the channel potential is a distribution instead of a constant. Moreover, this potential distribution depends on V_{GS}, L_g and measurement configuration.

Fig. 5.7(a) shows the channel potential distribution at V_{GS} = 1.5 V for the device with L_g = 10 μm. For the SD-G case (Hi port to Source/Drain, Lo port to Gate), the maximum potential, ~0.17 V, occurs at the center of the channel, because of the symmetric gate-tunneling current from gate to source/drain. For the D-G case (the Hi port to the drain electrode only), however, the maximum potential, ~0.34 V, occurs at the floating side (source side). It is worth noting that both the maximum IR drop and the capacitance attenuation (Fig. 5.7(b)) are enhanced in the D-G case. The excellent model-data fit in Fig. 5.7(b) shows the accuracy of our BSIM4-based segmented SPICE simulation.

5.4 Intrinsic input resistance model

Fig. 5.8(a) shows BSIM4/SPICE-simulated *C–V* characteristics for devices with leaky dielectrics. The BSIM4 device model parameters are the same as those used in Fig. 5.4, Fig. 5.5 and Fig. 5.7. As shown in Fig. 5.8(a), a substantial attenuation in the inversion capacitance for long-channel MOSFETs can be seen. The attenuation results mainly from the gate tunneling induced de-biasing effect. Also shown in Fig. 5.8(a) is that a single-transistor simulation with an intrinsic input resistance, R_{ii}, added to the gate terminal in addition to gate electrode resistance (Fig. 5.8(d)) yields nearly identical results as those of segmented simulation with sufficient (e.g. 30) sub-transistors (Fig. 5.8(c)). Besides, the gate currents (I_g) simulated by segmented simulation and the single-transistor simulation with R_{ii} are nearly identical for the devices with L_g = 0.24 to 10 μm (Fig. 5.8(b)). It indicates that the tunneling resistance $(\partial I_g/\partial V_{gs})^{-1}$ of a single-transistor simulation with R_{ii} is nearly identical to that of segmented simulation.

R_{ii} represents a channel-reflected gate resistance and can be thought of as an equivalent resistance accounting for the first-order non-quasi-static effect in the channel [10][12]. R_{ii} is proportional to the total channel resistance with a proportional constant α, which accounts for the distributed effect of the complex RC network constructed by the

gate capacitance and the channel resistance. Since this RC network has a short termination at both source and drain nodes in the C–V measurement, α can be approximated as 1/12 because the location at which the gate current equals zero occurs at $L_g/2$ [12]. The channel resistance and R_{ii} have been modeled through channel integration in BSIM4 [10][12] and can be extracted from the measured I–V (Fig. 5.9(a)). Fig. 5.9(b) shows that R_{ii} depends on V_{GS} and L_g. As L_g increases, R_{ii} increases.

Figure 5.8 indicate that the R_{ii} approach is accurate and efficient in simulating the distributed effect in long-channel MOSFETs. For the device with L_g = 10 μm, it can be seen from Fig. 5.8(a) that 10 sub-transistors are enough to capture the distributed effect. For the device with L_g = 20 μm, however, 10 sub-transistors are not sufficient to gain satisfactory accuracy. There is significant discrepancy between the two C_{gc} curves with 10 and 20 sub-transistors. It is worth noting that as the number of sub-transistors increases, the C_{gc} curves of the segmented simulation are close to that of the R_{ii} lumped simulation. In other words, the uncertainty in selecting the number of sub-transistors to simulate the distributed effect can be avoided by the R_{ii} lumped simulation. Therefore, using the R_{ii} approach in the inversion C–V reconstruction for long-channel MOSFETs is more accurate and efficient than the segmented-simulation approach.

5.5 Experimental reconstruction

In this section, we demonstrate that the concept of R_{ii} can be used to develop a simple method for the inversion C–V reconstruction for long-channel devices. As the conventional three-element model (Fig. 5.10(a)) is used to represent the small-signal equivalent model of a leaky MOS capacitor, the total series resistance, R_s, can be calculated by $R_{ii} + R_{ge} + R_{sd}/2$. The factor of 1/2 accounts for the R_{sd} induced de-biasing effect caused by one half of I_g. The inversion C–V may then be reconstructed by [20], [23]:

$$C_{OX} = \frac{C_m}{(1 - G_m R_s)^2 + \omega^2 C_m{}^2 R_s{}^2} \quad (1)$$

where C_m and G_m represent the measured capacitance and conductance, respectively, using the parallel circuit model of the LCR meter (Fig. 5.10(b)). The value of R_{ii} can be extracted from the channel resistance (Fig. 5.9(a)). The values of R_{ge} and R_{sd} can also be measured by standard procedures.

Fig. 5.11(a) and Fig. 5.11(b) show the measured inversion capacitance and our reconstructed *C–V* characteristics for NMOS and PMOS with L_g = 10 μm and W = 10 μm, respectively. The impact of R_{ii} on the reconstructed results can be seen. Moreover, the correction for PMOS is larger because the lower PMOS channel mobility may result in a higher channel resistance and R_{ii}. Besides, the reconstructed *C–V* characteristics show a slight decrease in the high gate bias regime. This can be attributed to poly-depletion effects. Also shown in Fig. 9 are the theoretical characteristics provided by the NCSU CVC (*C–V* analysis software developed by the North Carolina State University) [14]. Note that merely using the two-frequency three-element method [3]-[4], [22]-[23] has been known [7][14] to be unable to show the poly-depletion effect because of the limited number of elements. Using the R_{ii} approach to fully account for the distributed effect together with the three-element model, however, our reconstructed *C–V* curves show poly-depletion effects and agree with the NCSU-CVC simulation results well.

To assess the importance of intrinsic input resistance to the overall gate-current induced de-biasing effect, Fig. 5.12 shows R_{ii}/R_s as a function of L_g. it can be seen that the impact of R_{ii} increases with L_g. For the device with L_g = 10 μm, R_{ii}/R_s is ~80%. For L_g = 20 μm, the R_{ii}/R_s ratio can reach as high as 95%. In other words, the inversion *C–V* can be reconstructed by (1) with $R_s \approx R_{ii}$, which can be obtained from the channel resistance extraction shown in Fig. 5.9(a).

5.6 Conclusion

We have investigated the inversion *C–V* reconstruction and assessed the feasibility of the concept of intrinsic input resistance for long-channel MOSFETs. The concept of R_{ii} has been validated by segmented BSIM4/SPICE simulation. Using the R_{ii} approach in the inversion *C–V* reconstruction is more accurate and efficient than the segmented simulation approach. Our reconstructed *C–V* characteristics show poly-depletion effects and agree well with the NCSU-CVC simulation results. The intrinsic input resistance dominates the overall gate-current induced de-biasing effect (~95% for L_g = 20 μm) and can be extracted directly from the *I–V* characteristics. Due to its simplicity, our proposed R_{ii} approach may provide an option for regular process monitoring purposes.

References

[1] P.A. Kraus, K.Z. Ahmed, and J.S. Williamson Jr., "Elimination of Chuck-Related Parasitics in MOSFET Gate Capacitance Measurements," *IEEE Trans. Electron Devices*, vol. **51**(8), p. 1350, Aug. 2004.

[2] Z. Luo and T.P. Ma, "A New Method to Extract EOT of Ultrathin Gate Dielectric With High Leakage Current," *IEEE Electron Device Letters*, vol. **25**(9), p. 655, Sept. 2004.

[3] K.J. Yang and C. Hu, "MOS Capacitance Measurements for High-Leakage Thin Dielectrics," *IEEE Trans. Electron Devices*, vol. **46**(7), p. 1500, July 1999.

[4] A. Nara, N. Yasuda, H. Satake, and A. Toriumi, "Applicability Limits of the Two-Frequency Capacitance Measurement Technique for the Thickness Extraction of Ultrathin Gate Oxide," *IEEE Trans. Semiconductor Manufacturing*, vol. **15**(2), p. 209, May 2002.

[5] W. Lee, K.-W. Su, C.-S. Chiang, S. Liu, and P. Su, "Inversion MOS Capacitance Extraction for Ultra-Thin Gate Oxide using BSIM4," *Proc. IEEE 2005 VLSI-TSA Int. Symp. VLSI Technology*, p. 62, April 2005.

[6] C.-H. Choi, Y. Wu, J.-S. Goo, Z. Yu, and R.W. Dutton, "Capacitance Reconstruction from Measured *C-V* in High Leakage, Nitride/Oxide MOS," *IEEE Trans. Electron Devices*, vol. **47**(10), p. 1843, Oct. 2000.

[7] D.W. Barlage, J.T. O'Keeffe, J.T. Kavalieros, M.M. Nguyen, and R.S. Chau, "Inversion MOS Capacitance Extraction for High-Leakage Dielectrics Using a Transmission Line Equivalent Circuit," *IEEE Electron Device Letters*, vol. **21**(9), p. 454, Sep. 2000.

[8] D. Rideau, P. Scheer, D. Roy, G. Gouget, M. Minondo, and A. Juge, "Series Resistance Estimation and C(V) Measurements on Ultra Thin Oxide MOS Capacitors," *IEEE Int. Conf. Microelectronic Test Structures*, p. 191, March 2003.

[9] K. Ahmed, E. Ibok, G. C.-F. Yeap, Q. Xiang, B. Ogle, J. J. Wortman, and J. R. Hauser, "Impact of Tunnel Currents and Channel Resistance on the Characterization of Channel Inversion Layer Charge and Polysilicon-Gate Depletion of Sub-20-Å Gate Oxide MOSFETs," *IEEE Trans. Electron Devices*, vol. **46**(8), p. 1650, Aug. 1999.

[10] X. Jin, J.-J. Ou, C.-H. Chen, W. Liu, M. J. Deen, P. R. Gray, and C. Hu, "An Effective Gate Resistance Model for CMOS RF and Noise Modeling," *IEDM Tech. Dig.*, p. 961, 1998.

[11] W. Lee, P. Su, K.-W. Su, C.-S. Chiang, and S. Liu, "Investigation of Inversion C-V Reconstruction for Long-Channel MOSFETs with Leaky Dielectrics using Intrinsic Input Resistance Approach," *Int. Conf. Solid State Devices and Materials*, p. 416, Sept. 2006.

[12] W. Liu, *MOSFET Models for SPICE Simulation including BSIM3v3 and BSIM4*, John Wiley & Sons, 2001.

[13] *Evaluation of MOS Capacitor Gate Oxide C-V Characteristics Using the Agilent 4294A*, Agilent Technologies Application Note PN4294-3.

[14] J.-S. Goo, T. Mantei, K. Wieczorek, W.G. En, and A.B. Icel, "Extending Two-Element Capacitance Extraction Method Toward Ultraleaky Gate Oxides Using a Short-Channel Length," *IEEE Electron Device Letters*, vol. **25**(12), p. 819, Dec. 2004.

[15] L. Pantisano, J. Ramos, E.S. A. Serrano, Ph. J. Roussel, W. Sansen, and G. Groeseneken, "A comprehensive model to accurately calculate the gate capacitance and the leakage from DC to 100 MHz for ultra thin dielectrics," *IEEE Int. Conf. Microelectronic Test Structures*, p. 222, March 2006.

[16] J. Schmitz, F.N. Cubaynes, R.J. Havens, R. de Kort, A.J. Scholten, and L.F. Tiemeijer, "Test Structure Design Considerations for RF-CV Measurements on Leaky Dielectrics," *IEEE Trans. Semiconductor Manufacturing*, vol. **17**(2), p. 150, May 2004.

[17] J. Schmitz, F.N. Cubaynes, R.J. Havens, R. de Kort, A.J. Scholten, and L.F. Tiemeijer, "RF Capacitance-Voltage Characterization of MOSFETs With High Leakage Dielectrics," *IEEE Electron Device Letters*, vol. **24**(1), p. 37, January 2003.

[18] C. Yu, J. Zhang, J.S. Yuan, F. Duan, S.K. Jayanarananan, A. Marathe, S. Cooper, V. Pham, and J.-S. Goo, "Evaluation of RF Capacitance Extraction for Ultrathin Ultraleaky SOI MOS Devices," *IEEE Electron Device Letters*, vol. **28**(1), p. 45, January 2007.

[19] W.K. Henson, K.Z. Ahmed, E.M. Vogel, J.R. Hauser, J.J. Wortman, R.D.

Venables, M. Xu, and D. Venables, "Estimating Oxide Thickness of Tunnel Oxides Down to 1.4nm Using Conventional Capacitance-Voltage Measurements on MOS Capacitors," *IEEE Electron Device Letters*, vol. **20**(4), p. 179, April 1999.

[20] E.M. Vogel, W.K. Henson, C.A. Richter, and J.S. Suehle, "Limitations of Conductance to the Measurement of the Interface State Density of MOS Capacitors with Tunneling Gate Dielectrics," *IEEE Trans. Electron Devices*, vol. **47**(3), p. 601, March 2000.

[21] G. Ghibaudo, S. Bruyère, T. Devoivre, B. DeSalvo, and E. Vincent, "Improved Method for the Oxide Thickness Extraction in MOS Structures with Ultrathin Gate Dielectrics," *IEEE Trans. Semiconductor Manufacturing*, vol. **13**(2), p. 152, May 2000.

[22] D.K. Schroder, *Semiconductor Material and Device Characterization*, 3rd Edition (John Wiley & Sons, Inc., New York).

[23] A.M. Goodman, "Metal-Semiconductor Barrier Height Measurement by the Differential Capacitance Method-One Carrier System," *J. Appl. Phys.*, **34**(2), p. 329, Feb. 1963.

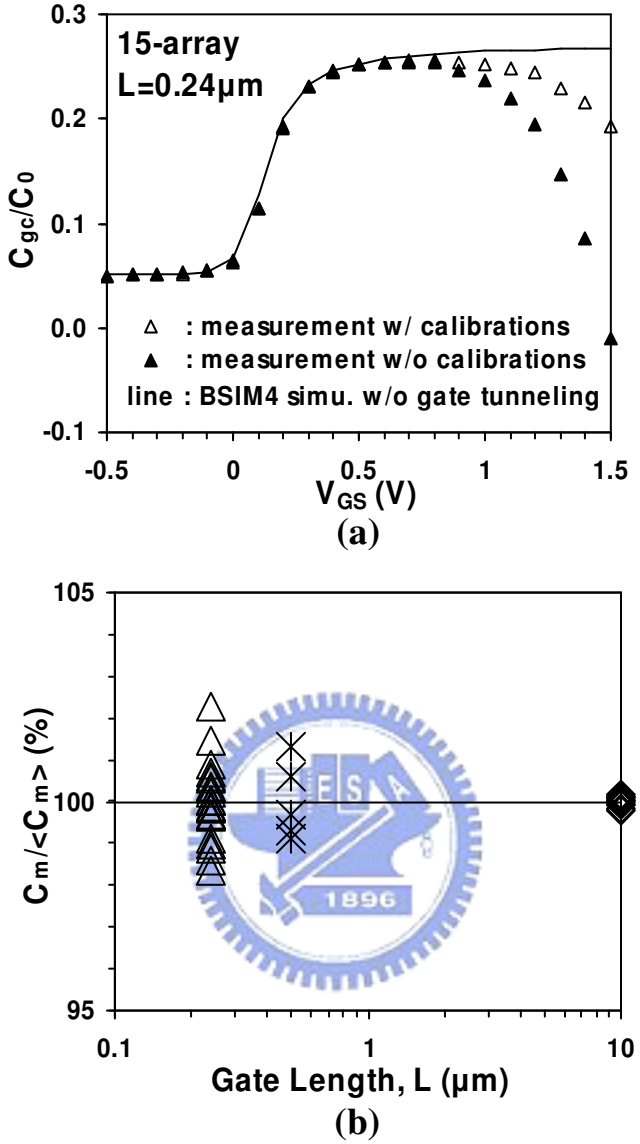


Fig. 5.1. (a) Inversion MOS capacitance (C_{gc}) for the short-channel (L_g = 0.24μm) device. C_0: true capacitance for L_g = 10 μm. (b) The variation of C_m increases as L_g decreases. C_m: measured capacitance. <C_m>: C_m mean.

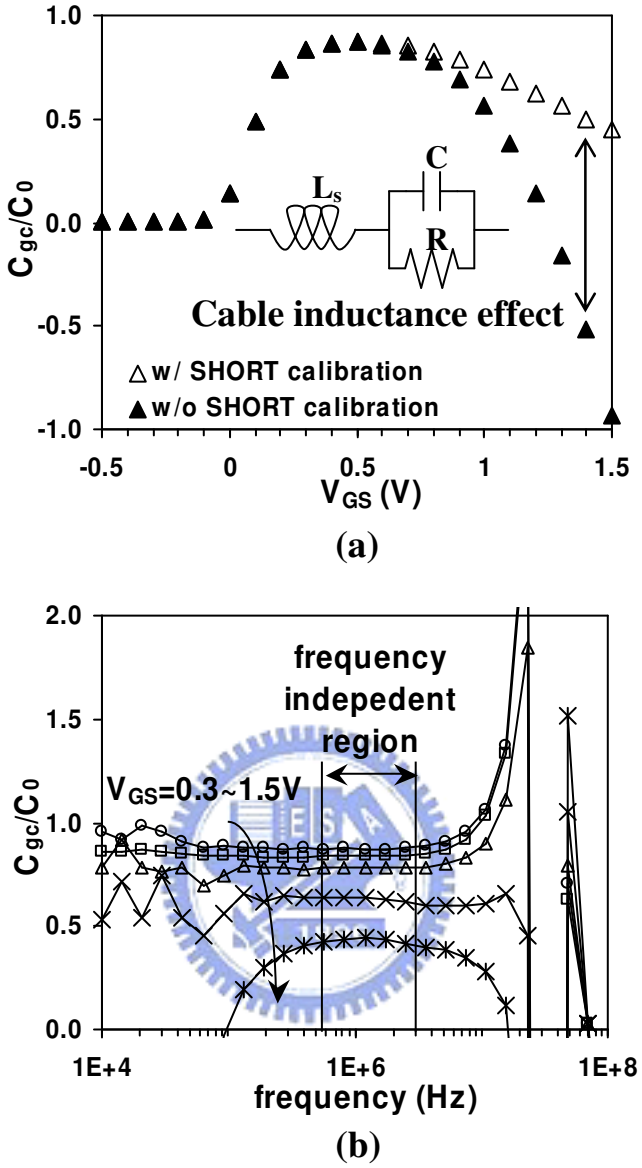


Fig. 5.2. (a) The impact of cable inductance, L_s, on C_{gc}. (b) Frequency dependence of the measured C_{gc}.

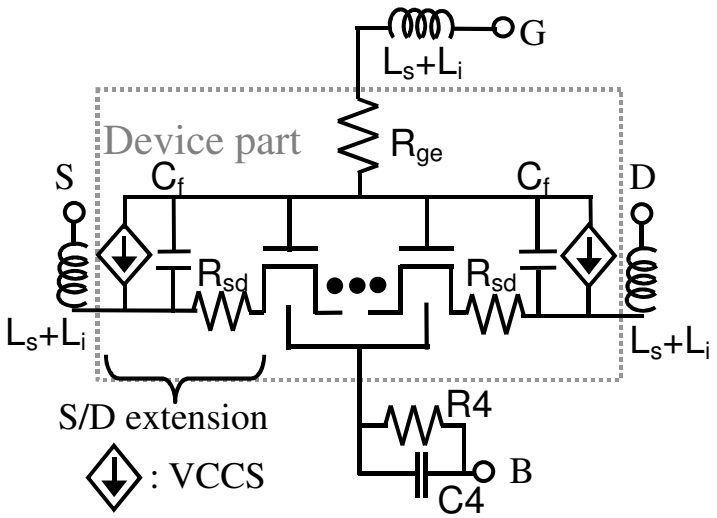


Fig. 5.3. (a) BSIM4-based macro model. C_f: fringing capacitance. R_4 = 1x10^9 Ω, C_4 = 1x10^{-9} F.

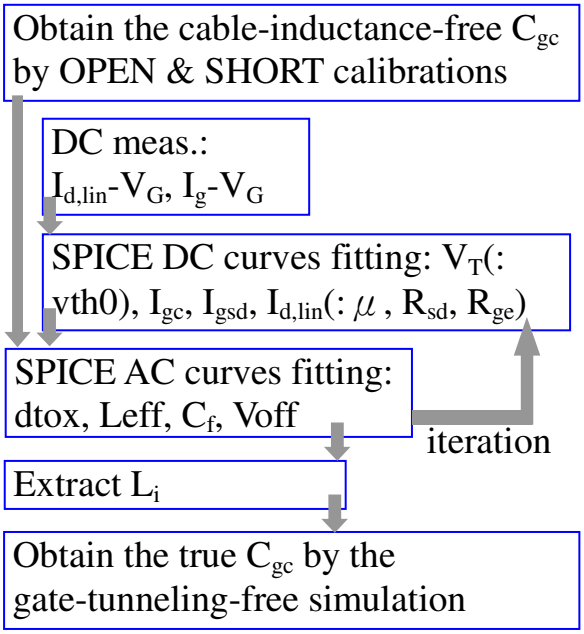


Fig. 5.3. (b) Our BSIM4 extraction methodology of the inversion MOS capacitance.

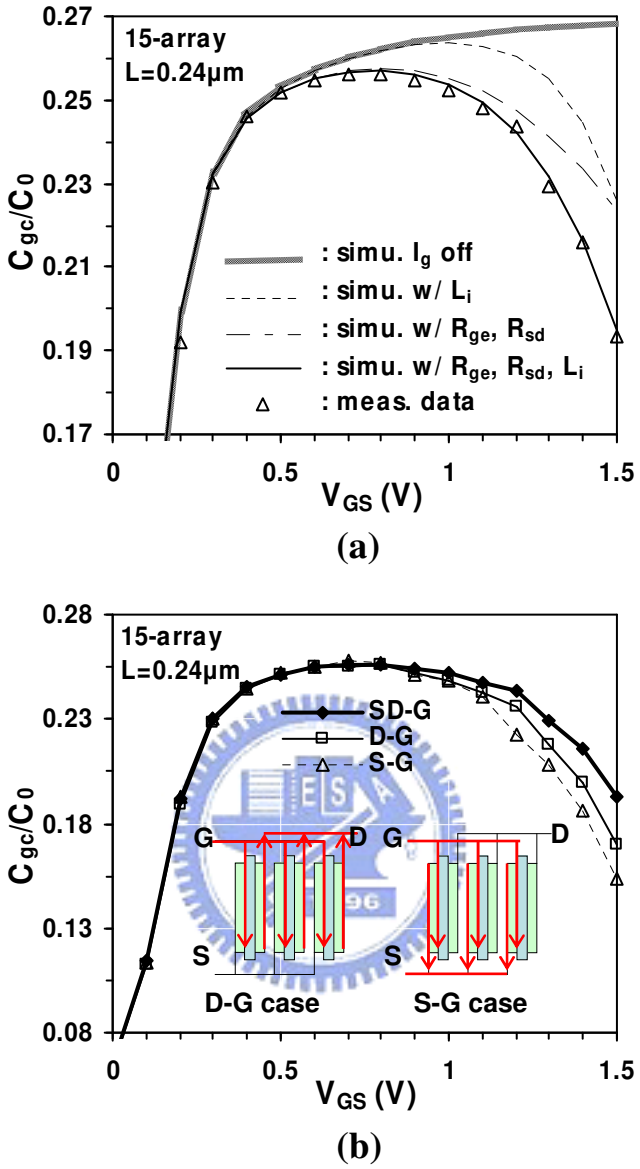


Fig. 5.4. (a) Merely considering R_{ge} and R_{sd} without taking L_i into account cannot model the C_{gc} characteristics in the high gate bias regime. (b) In the same MOS array of short-channel devices, the impact of on-chip inductance (L_i) depends on the measurement configuration. (For the SD-G case, the Hi port is connected to source/drain, while the Lo port to the gate electrode.)

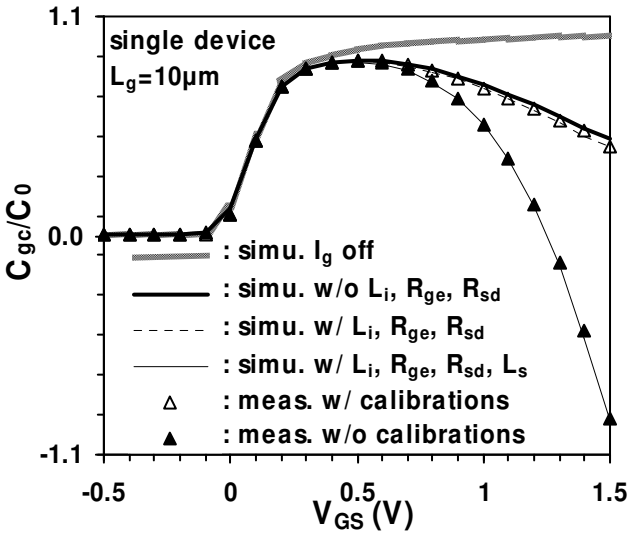


Fig. 5.5. The segmented SPICE simulation reveals the importance of calibrations and the distributed effect for the long channel device.

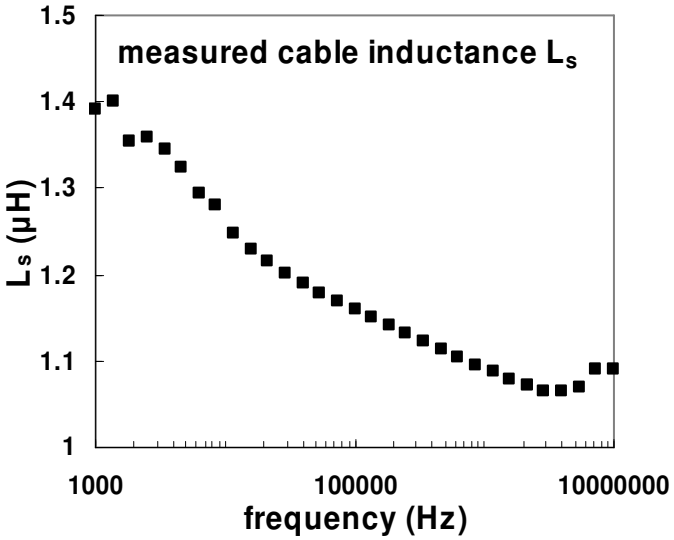


Fig. 5.6. The cable inductance L_s vs. frequency characteristics. ~1μH L_s can be excluded after performing the SHORT calibration.

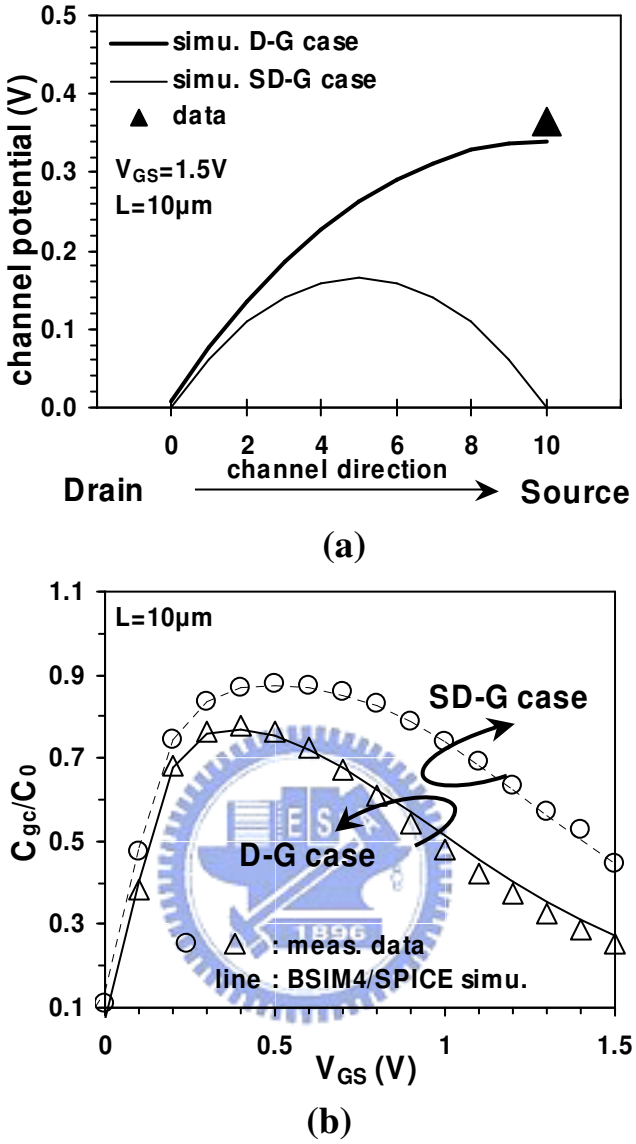


Fig. 5.7. (a) DC and (b) AC verification of the segmented SPICE simulation for the distributed effect.

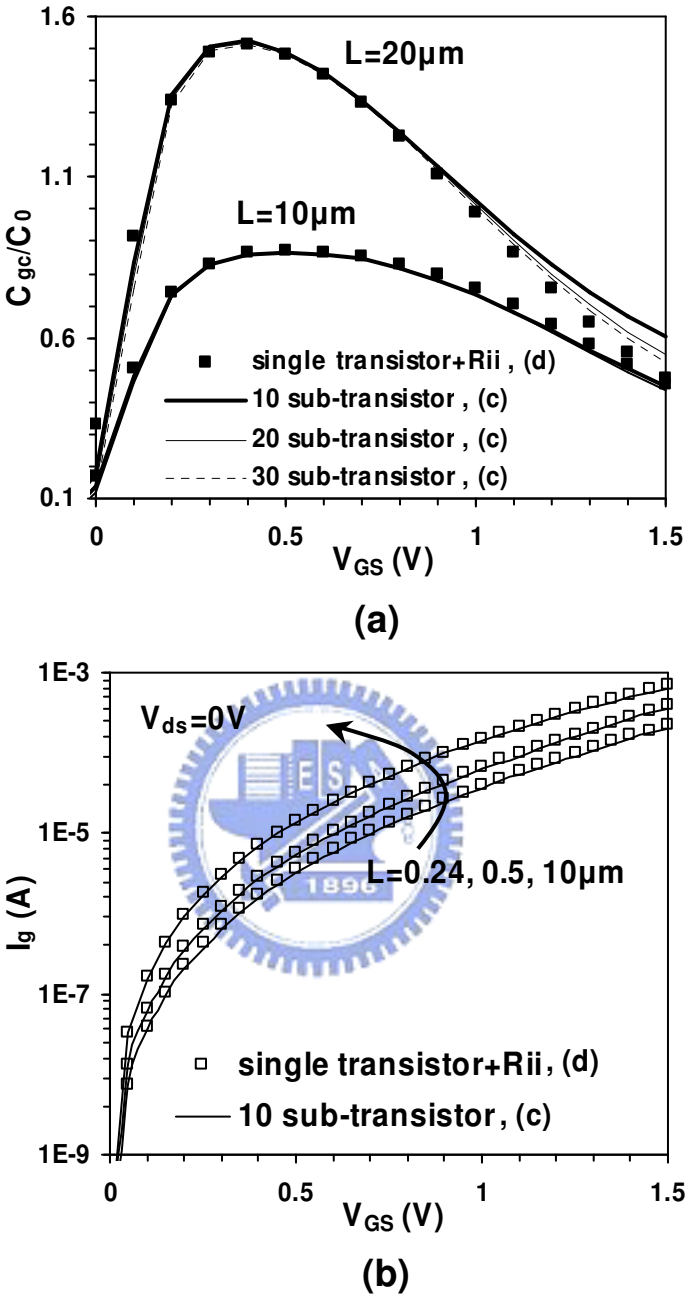


Fig. 5.8. (a) The gate-tunneling induced *C–V* attenuation due to de-biasing effect can be simulated by BSIM4/SPICE simulation. (b) The gate currents simulated by the segmented simulation and the R_{ii} lumped simulation are nearly identical.

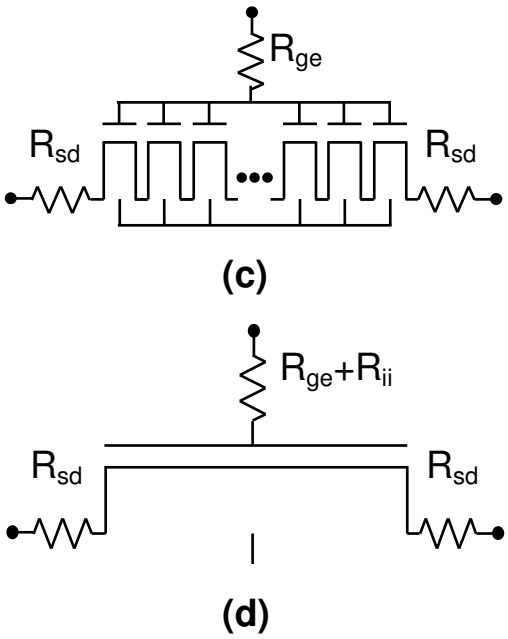


Fig. 5.8. (c) Segmented SPICE simulation with each sub-transistor modeled by the BSIM4 MOSFET model. (d) Single-transistor SPICE simulation with R_{ii} added to the gate terminal in addition to R_{ge}.

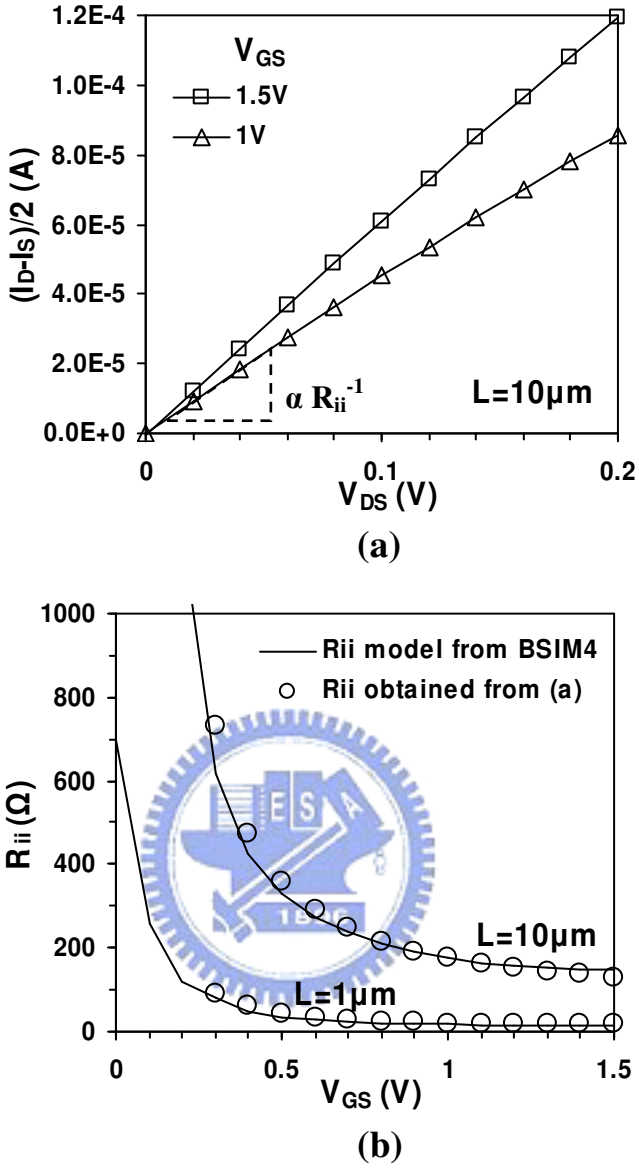


Fig. 5.9. (a) R_{ii} for L_g = 10 μm device can be extracted from the DC output characteristics. (b) R_{ii} as a function of V_{GS} and L_g.

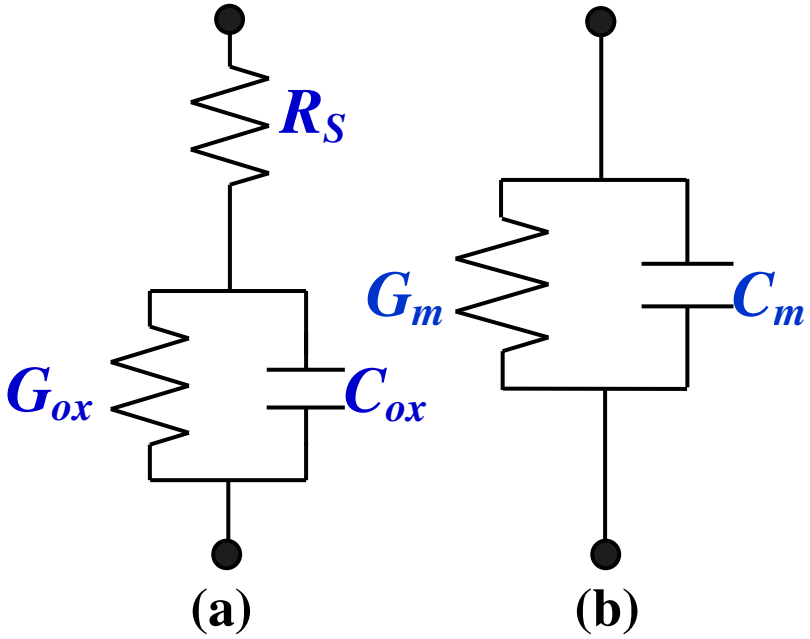
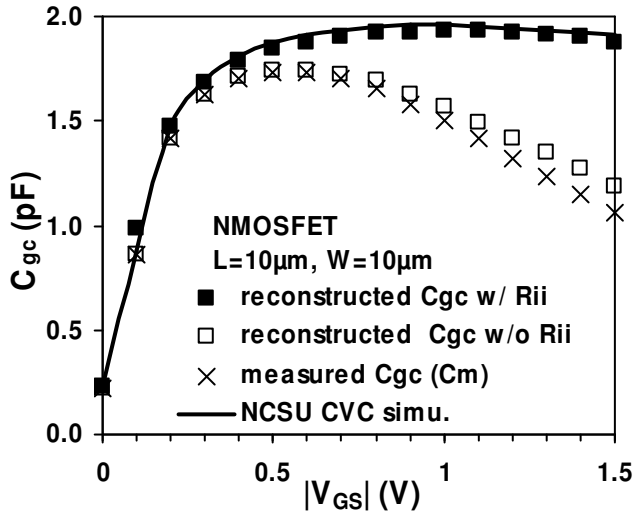
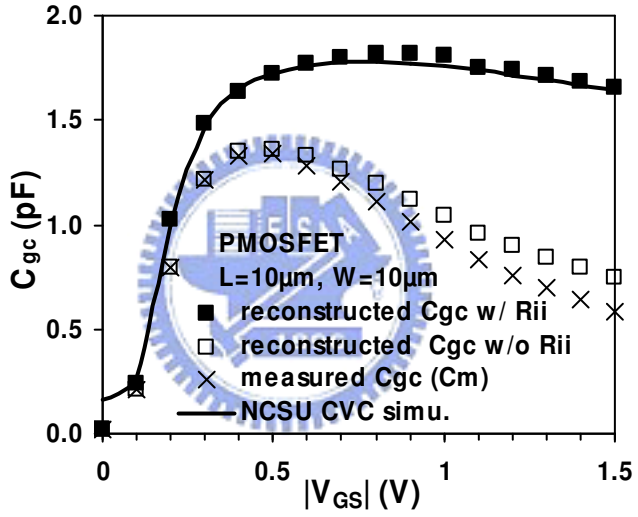


Fig. 5.10. Small-signal equivalent models for MOS capacitor. (a) Three-element model. (b) Two-element parallel model.



(a)



(b)

Fig. 5.11. Reconstructed *C–V* characteristics for (a) NMOS and (b) PMOS with and without considering R_{ii}. The results agree well with the simulation results of NCSU CVC. (T_{OX} = 1.15 nm. NMOS : N_{Bulk} = 3E17 cm^{-3}, N_{Gate} = 1.8E20 cm^{-3}, R_{ge}+R_{sd}/2 = 40 Ω. PMOS : N_{Bulk} = 2.5E17 cm^{-3}, N_{Gate} = 8.5E19 cm^{-3}, R_{ge}+R_{sd}/2 = 180 Ω.)

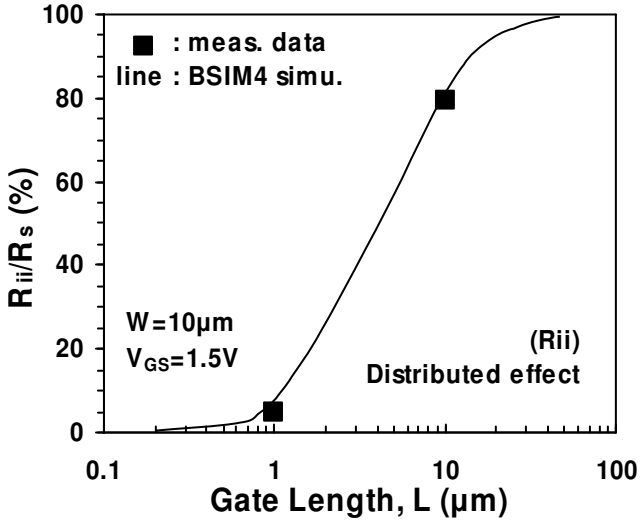


Fig. 5.12. The contribution of intrinsic input resistance in the overall gate-current induced de-biasing effect. $R_s = R_{ii}+R_{ge}+R_{sd}/2$.

Chapter 6

Conclusions

In this dissertation, we have systematically performed comparative investigation for various kinds of nanoscale MOSFETs including the overlapped vs. non-overlapped multiple-gate SOI MOSFETs, the strain vs. unstrained planar MOSFETs, the SiO_2 vs. HfO_2 dielectrics, the high vs. low body doping, the SOI vs. bulk MOSFETs, and ultra-thin gate dielectrics. For multiple-gate SOI MOSFETs, quantum-mechanical confinement effects and quantum-mechanical interference effects may prevail in the narrow overlapped devices and the non-overlapped devices, respectively [1]-[2]. Besides, controlled single-electron effects have also been observed in the non-overlapped devices especially for smaller gate length and fin width [3]-[5]. In addition, channel backscattering characteristics have been successfully, physically and experimentally extracted through the newly developed self-consistence temperature-dependence extraction method [6]-[7]. We found that ballistic efficiency can be enhanced by compressive strain for PMOSFETs and is degraded by high body doping and high-k dielectric. Moreover, for the gate-tunneling current induced capacitance-voltage problem, we have proposed a simple reconstruction method [8]. Several important results were obtained and summarized as follows:

1. In Chapter 2, we have conducted a comparative study of carrier transport characteristics for multiple-gate SOI MOSFETs with and without the non-overlapped source/drain structure. For the overlapped devices, we observed *Boltzmann law* in subthreshold characteristics and *phonon-limited behavior* in the inversion regime. For the non-overlapped devices, however, we found insensitive temperature dependence of drain current in both subthreshold and inversion

regimes. Our low-temperature measurements indicate that the *inter-subband scattering* (i.e., *quantum-mechanical confinement effects*) may dominate carrier transport mechanism for narrow overlapped multiple-gate devices. For the non-overlapped multiple-gate devices, the voltage-controlled potential barriers in the non-overlapped regions may give rise to the *weak localization effect* (conductance reduction) and the *quantum interference fluctuations*. Based on the wave nature of channel electrons, we have experimentally obtained the gate-voltage-dependent effective channel length for the non-overlapped multiple-gate SOI MOSFETs, which agrees with the simulation results.

2. In Chapter 3, we have systematically investigated controlled single-electron effects in multiple-gate SOI MOSFETs with various *gate length*, *fin width*, *gate voltage*, *body doping* and *temperature*. Our study indicates that using the non-overlapped gate to source/drain structure as an approach of the single-electron transistor (SET) in MOSFETs is promising. Combining the advantage of gate control and the constriction of high source/drain resistances, single-electron effects are further enhanced using the multiple-gate architecture. From the presented results, downsizing multiple-gate SOI MOSFETs is needed for future room-temperature SET applications. Since single-electron effects can be achieved in state-of-the-art CMOS devices, it is beneficial to built SETs in low-power CMOS circuits for the ultrahigh-density purpose. In addition, we have analyzed gate capacitance as well as source/drain capacitance of multiple-gate SOI MOSFETs.
3. In Chapter 4, we have reported a *generalized self-consistent temperature-dependent channel backscattering extraction method*. We have also investigated the limitation of this self-consistent method and proposed guidelines for experimental extraction. Using the generalized temperature-dependent method, we have shown that the

channel backscattering of nanoscale PMOSFETs can be reduced by the uniaxially compressive strain. Besides, channel backscattering is increased for NMOSFETs with higher body doping and HfO_2 dielectric. In addition, our results indicate that on one hand the floating-body effect may decrease the channel backscattering in high drain bias regime, and on the other hand the self-heating effect may increase channel backscattering. We further demonstrate that the strain technology can improve the drain current variation through the enhanced ballistic efficiency. We believe that the generalized temperature-dependent extraction method is competent to be routinely used in technology development for the process monitoring purpose.

4. In Chapter 5, we have investigated the *inversion C−V reconstruction* and assessed the feasibility of the concept of *intrinsic input resistance* (R_{ii}) for long-channel MOSFETs. The concept of R_{ii} has been validated by segmented BSIM4/SPICE simulation. Using the R_{ii} approach in the inversion C–V reconstruction is more accurate and efficient than the segmented simulation approach. Our reconstructed C–V characteristics show poly-depletion effects and agree well with the NCSU-CVC simulation results. Due to its simplicity, our proposed R_{ii} approach may provide an option for regular process monitoring purposes.

Finally, it is worth noting that we have proposed an effective channel length extraction in Chapter 2 using the quantum interference effects. Similar ideas have been developed to determine the Si/SiO_2 interface roughness for bulk MOSFETs [10] and the diameter of the nanowire devices [11]. In Chapter 3, we have demonstrated that the single-electron effect is competent to be used in the aF-scale capacitance extraction. Recently, this concept has been employed in [12] for the nanoscale multi-channel devices. We believe that the feasibility of using mesophysics (buttom-up approaches) to determine important device parameters for nanoscale MOSFETs is promising.

References

[1] W. Lee and P. Su, "A Comparative Study of Carrier Transport for Overlapped and Non-overlapped Multiple-Gate SOI MOSFETs," *IEEE Trans. on Nanotechnology*, 2009, to be published.

[2] W. Lee, P. Su, H. Chen, C. Chang, K. Su, S. Liu, and F. Yang, "An Experimental Assessment of Quantum Interference in Multiple-Gate SOI nMOSFETs with Non-Overlapped Gate to Source/Drain Structure near Room Temperature," *Proc. of the 2007 Silicon Nanoelectronics Workshop*, Kyoto, Japan, p. 15, June 2007.

[3] W. Lee and P. Su, "Single-electron effects in non-overlapped multiple-gate silicon-on-insulator metal-oxide-semiconductor field-effect transistors," *Nanotechnology*, vol. **20**, p. 065202, Feb. 2009.

[4] W. Lee, P. Su, H. Chen, C. Chang, K. Su, S. Liu, and F. Yang, "An Assessment of Single-Electron Effects in Multiple-Gate SOI MOSFETs with 1.6-nm Gate Oxide near Room Temperature," *IEEE Electron Device Letters*, vol. **27**(3), pp. 182–184, March 2006.

[5] W. Lee and P. Su, "A Comprehensive Study of Single-Electron Effects in Multiple-Gate MOSFETs," *Proc. of the 2008 Silicon Nanoelectronics Workshop*, Honolulu, Hawaii, USA, June 2008.

[6] W. Lee and P. Su, "Investigation of Channel Backscattering Characteristics in Nanoscale Uniaxial Strained PMOSFETs," *IEEE Trans. on Nanotechnology*, 2009 (conditionally accepted)

[7] W. Lee and P. Su, "Investigation of Channel Backscattering Characteristics for Nanoscale SOI MOSFETs Using a New Temperature-Dependent Method," *Proc. of the 2008 IEEE International SOI Conference*, New York, USA, pp. 73–74, October 2008.

[9] W. Lee, P. Su, K. Su, C. Chiang, and S. Liu, "Investigation of Anomalous Inversion C-V Characteristics for Long-Channel MOSFETs with Leaky Dielectrics : Mechanisms and Reconstruction," *IEEE Trans. on Semiconductor Manufacturing*, vol. **21**(1), pp. 104–109, Feb. 2008.

[10] W. R. Anderson, D. R. Lombardi, R. G. Wheeler, and T.-P. Ma, "Determination of Si/SiO_2 interface roughness using weak localization," *IEEE Electron Device Letters*, vol. **14**(7), pp. 351–353, July 1993.

[11] A.T. Tilke, F.C. Simmel, H. Lorenz, R.H. Blick, and J.P. Kotthaus, "Quantum interference in a one-dimensional silicon nanowire," *Phys. Rev. B*, vol. **68**, p. 075311, 2003.

[12] M. Hofheinz, X. Jehl, M. Sanquer, R. Cerutti, A. Cros, P. Coronel, H. Brut, and T. Skotnicki, "Measurement of capacitances in multigate transistors by coulomb blockade spectroscopy," *IEEE Trans. on Nanotechnology*, vol. **7**(1), pp. 74–78, 2008.

簡 歷

姓名： 李維

性別： 男

生日： 68 年 6 月 24 日

籍貫： 台北市

通訊地址: 112　台北市 北投區吉利街 257 巷 4 弄 10 號 5 樓

學歷:

Grade	Name of School, Major	Year
High School	師大附中	1994~1997
College	清華大學 工程與系統科學系	1997~2001
Master	交通大學 電子研究所	2001~2003
Ph.D.	交通大學 電子研究所	2003~2009

博士論文題目:

矽奈米尺寸金氧半場效電晶體的載子傳輸與

重要元件參數之實驗性的研究

Experimental Study of Carrier Transport and

Important Device Parameters for Nanoscale Si MOSFETs

著 作 目 錄

A. International Journal

1. **W. Lee** and P. Su, "Single-electron effects in non-overlapped multiple-gate silicon-on-insulator metal-oxide-semiconductor field-effect transistors," *Nanotechnology*, vol. **20**, p. 065202, Feb. 2009. (A 類期刊—**SCI**)

2. **W. Lee**, P. Su, H. Chen, C. Chang, K. Su, S. Liu, and F. Yang, "An Assessment of Single-Electron Effects in Multiple-Gate SOI MOSFETs with 1.6-nm Gate Oxide near Room Temperature," *IEEE Electron Device Letters*, vol. **27**(3), pp. 182–184, March 2006. (A 類期刊—**SCI**)

3. **W. Lee** and P. Su, "A Comparative Study of Carrier Transport for Overlapped and Non-overlapped Multiple-Gate SOI MOSFETs," *IEEE Trans. on Nanotechnology*, 2009, to be published. (A 類期刊—**SCI**)

4. **W. Lee** and P. Su, "Investigation of Channel Backscattering Characteristics in Nanoscale Uniaxial Strained PMOSFETs," *IEEE Trans. on Nanotechnology*, 2009. (A 類期刊—**SCI**) (conditionally accepted)

5. **W. Lee**, P. Su, K. Su, C. Chiang, and S. Liu, "Investigation of Anomalous Inversion C-V Characteristics for Long-Channel MOSFETs with Leaky Dielectrics : Mechanisms and Reconstruction," *IEEE Trans. on Semiconductor Manufacturing*, vol. **21**(1), pp. 104–109, Feb. 2008. (A 類期刊—**SCI**)

6. P. Su and **W. Lee**, "On the Prediction of Geometry-Dependent Floating-Body Effect in SOI MOSFETs," *IEEE Trans. on Electron Devices*, vol. 52(7), pp. 1662–1664, July 2005. (A 類期刊—**SCI**)

7. P. Su and **W. Lee**, "Modeling Geometry-Dependent Floating-Body Effect Using Body-Source Built-In Potential Lowering for SOI Circuit Simulation," *Jpn. J. Appl. Phys.*, vol. **44**(4B), pp. 2366–2370, April 2005. (B 類期刊—**SCI**)

8. **W. Lee**, P. Su, K. Su, C. Chiang, and S. Liu, "Investigation of Inversion C-V Reconstruction for MOSFETs with Leaky Dielectrics using BSIM4/SPICE and Intrinsic Input Resistance Model," *Jpn. J. Appl. Phys.*, vol. **46**(4B), pp. 1870–1873, April 2007. (B 類期刊—**SCI**)

9. **W. Lee** and P. Su, "On the Experimental Determination of Channel Backscattering Characteristics – Limitation and Application for the Process Monitoring Purpose," *IEEE Trans. on Electron Device*. (投稿中)

B. International Conference

10. P. Su and **W. Lee**, "Modeling Geometry-Dependent Floating-Body Effect using Body-Source Built-In Potential Lowering for Scaled SOI CMOS," *2004 Int. Conf. Solid State Devices and Materials (SSDM)*, Tokyo, Japan, pp. 510–511. Sept. 2004. (研討會論文—國際)

11. **W. Lee**, K. Su, C. Chiang, S. Liu, and P. Su, "Inversion MOS Capacitance Extraction for Ultra-Thin Gate Oxide using BSIM4," *Proc. of the IEEE 2005 VLSI-TSA Int. Symp. VLSI Technology*, Hsinchu, Taiwan, pp. 62−63, April 2005. (研討會論文—國際) (**Oral presentation**)

12. **W. Lee**, P. Su, H. Chen, C. Chang, K. Su, S. Liu, and F. Yang, "An Assessment of Single-Electron Effects in Multiple-Gate SOI MOSFETs with 1.6-nm Gate Oxide near Room Temperature," *Proc. of 2005 Int. Semiconductor Device Research Symposium (ISDRS)*, Washington D.C., USA, pp.175−176, Dec. 2005. (研討會論文—國際) (**Oral presentation**)

13. **W. Lee**, P. Su, K. Su, C. Chiang, and S. Liu, "Investigation of Inversion C-V Reconstruction for Long-Channel MOSFETs with Leaky Dielectrics using Intrinsic Input Resistance Approach," *2006 Int. Conf. Solid State Devices and Materials (SSDM)*, Yokohama, Japan, Sept. 2006. (研討會論文—國際)

14. **W. Lee**, P. Su, H. Chen, C. Chang, K. Su, S. Liu, and F. Yang, "Controlled Single-Electron Effects in Multiple-Gate SOI MOSFETs near Room Temperature," *Proc. of the 2006 IEEE Int. SOI Conf.*, Niagara Falls, New York, USA, Oct. 2006. (研討會論文—國際)

15. **W. Lee**, P. Su, H. Chen, C. Chang, K. Su, S. Liu, and F. Yang, "An Experimental Assessment of Quantum Interference in Multiple-Gate SOI nMOSFETs with Non-Overlapped Gate to Source/Drain Structure near Room Temperature," *Proc. of the 2007 Silicon Nanoelectronics Workshop*, Kyoto, Japan, p. 15, June 2007. (研討會論文—國際) (**Oral presentation**)

16. **W. Lee** and P. Su, "A Comprehensive Study of Single-Electron Effects in Multiple-Gate MOSFETs," *Proc. of the 2008 Silicon Nanoelectronics Workshop*, Honolulu, Hawaii, USA, June 2008. (研討會論文—國際) (**Oral presentation**)

17. **W. Lee** and P. Su, "Investigation of Channel Backscattering Characteristics for Nanoscale SOI MOSFETs Using a New Temperature-Dependent Method," *Proc. of the 2008 IEEE Int. SOI Conf.*, New York, USA, pp. 73−74, October 2008. (研討會論文—國際)

18. **W. Lee**, J. J.-Y. Kuo, W. P.-N. Chen, P. Su, and M.-C. Jeng, "Impact of Uniaxial Strain on Channel Backscattering Characteristics and Drain Current Variation for Nanoscale PMOSFETs," *Symp. on VLSI*, 2009. (投稿中)

19. **W. Lee**, P. Su, and M.-C. Jeng, "On the Experimental Determination of Channel Backscattering Characteristics – Limitation and Application for the Process Monitoring Purpose," *Symp. on VLSI*, 2009. (投稿中)