高介電係數介電質與金屬閘極製程技術應用在

金屬-氧化層-氮化層-氧化層-矽結構之非揮發性記憶體

研究生：賴軍宏　　指導教授：荊鳳德教授

國立交通大學

電子工程學系暨電子研究所

摘要

近年來，在半導體產業中，記憶體元件的發展已成為另一主流。其中，屬於非揮發性型態的快閃式記憶體因其具有高密度特性、良好的資料保存能力和重複抹寫功能而被廣泛地使用在個人行動電子產品，例如手機或數位相機。隨著這些電子產品的普及化，對快閃式記憶體的需求也快速增加。因此，快閃式記憶體的發展和技術已成為重要的研究之一。

隨著元件尺寸持續縮微，快閃式記憶體主要的製程技術關鍵為其具有導電性的多晶矽浮停閘。基於非揮發性記憶體基本的需求，以多晶矽材料當作電荷儲存層的快閃式記憶體需要厚度至少約6-7奈米的穿遂氧化層來防止儲存電荷遺失以增加資料儲存能力。其主要原因為反覆的編碼和抹除過程將會對穿遂氧化層造成應力而產生缺陷，這些缺陷可能形成漏電路徑而導致多晶矽全面性的漏電。然而，較厚的穿遂氧化層不僅需要較大的操作電壓也增加元件製程縮微的困難度。為了解決此問題，多晶矽材料將被氮化矽所取代。由氮化矽電荷儲存層所形成的多晶矽或金屬閘極-氧化矽-氮化矽-氧化矽-矽結構記憶體元件可以解決平面微

縮的問題且同時具有良好電荷儲存能力、低工作電壓特性和符合目前互補式金氧半場效電晶體元件的製程，因此已開始受到大家的關注。

在此論文中，我們使用全新的高介電係數介電質材料氮化鋁（介電係數約10）和氧化鉿鋁（介電係數約 17）分別取代傳統的氮化矽電荷捕獲層及氧化矽阻擋層。高介電係數介電質的使用，不僅可以有效降低操作電壓，同時也可以將電壓有效的跨在薄二氧化矽穿遂層以增加編碼和抹寫速度。此外，應用具高功函數的金屬閘極氧化銥替代傳統多晶矽閘極可以防止在抹除狀態時電荷從閘極端注入並增加抹除效率。此非揮發性記憶體元件展現出非常大的記憶視窗（3.7伏）、快速（100 微秒）、低電壓（13 伏）操作和良好的資料儲存特性。

為了更進一步的降低記憶體元件操作電壓使其達到嵌入式單一晶片系統的應用。我們使用具有更高介電係數的介電質材料-氮氧化鉿（介電係數約 22）當作元件的電荷捕獲層。此氮氧化鉿記憶體元件展現出快速（100 微秒）和超低電壓（8 伏）操作特性。同時具有良好的資料儲存特性。另外，設計一簡單的電路可將此記憶體元件之操作電壓減少一半以達到單一晶片系統的應用。

Process and Technology for High-κ Metal Gate MONOS Structured Non-volatile Memory

Student: C. H. Lai **Advisor: Dr. Albert Chin**

Department of Electronics Engineering

& Institute of Electronics

National Chiao Tung University

Abstract

Recently, the Flash memory is commonly used in portable electronic products, such as cell phone, MP3 player and USB Flash. However, with the increase in requirements for products, the technology and process must be still improved.

The key issue for poly-Si floating gate non-volatile memory is the electrically conductive charge storage layer, where the programmed electrons will leak out through the single oxide defect. Such oxide defects are generated by the program and erase stress operation. In order to maintain the data retention, the thick tunnel oxide (6-7 nm) is required. That is opposite to the VLSI scaling trend. In addition, the memory device with thick tunnel oxide requires a higher operation voltage. To overcome this problem, the conductive poly-Si is replaced by discrete trapping nitride to form the [poly-Si or metal gate]-SiO_2-SiN-SiO_2-Si SONOS or MONOS memory. The isolated charges stored in discrete traps can prevent complete charge leakage. Therefore, a thinner tunnel oxide can be used. This in turn yields lower voltage and

faster speed for program and erase.

In this dissertation, we demonstrated a low voltage, fast speed and good data retention MONOS memory device with high work function IrO_x metal gate, novel high-κ AlN trapping layer and HfAlO blocking layer. At 13 V and 100 μs program and -13 V 100 μs erase, we found a large threshold voltage shift (ΔV_{th}) of 3.7 V that extrapolated to 1.9 V for 10-year retention at 85°C. This 100 μs speed, low operation voltage of 12-13 V, withstand above 10 k cycles and 1.9 V 10-year memory retention window at 85°C meet all the non-volatile memory requirements simultaneously.

Using the same concept, we further provide the TaN-HfAlO-HfON-SiO_2-Si MONOS device to operate at only 8 V under faster 100 μs. Such low P/E voltage is achieved by using novel HfON trapping layer with very high κ of 22 beyond AlN (κ~10). Under fast 100 μs at ±8 V for P/E, the device exhibits a large initial ΔV_{th} (memory window) of 2.5 V and the 10-years extrapolated retention window of 1.0 V at even 125°C. Using a simple voltage inverter circuit, the P/E voltage can further be reduced to nearly half: by applying 4.5 V and -3.5 V for the same ±8 V gate-channel bias. This is useful for embedded SoC under a single 5 V voltage source.

Acknowledgement

First, I would like to thank my advisor Prof. Albert Chin for his fruitful discussion and illuminative comment. I am also grateful to all ED633 group members, Dr. C. Y. Lin, Dr. S. B. Chen, Dr. M. Y. Yang, Dr. C. H. Huang, Dr. D. S. Yu, Dr. C. C. Chen, Dr. H. L. Kao, C. H. Wu, B. F. Hung, K. C. Chiang, Terry Wang, Z. W. Lin and W. L. Huang, for their enthusiastic assistance and cooperation. Moreover, I thank for my girl friend Miss Chan, Hui-Ting. Finally, I deeply appreciate my family and parents' endless encouragement and spiritual support. Without them, I can't finish this dissertation.

Contents

Figure Caption

Chapter 1 Introduction

Chapter 2 A Novel Program-erasable High-κ AlN/Si MIS Capacitor

Large ΔV_{th} and Good Retention

Table Caption