Chapter 1

Introduction

1.1 Motivation to study high-κ dielectrics

Along of the improvement of the semiconductor processing technology, the scaling trend of MOSFETs devices will produce the large gate leakage current due to thinner gate oxide [1.1]-[1.2]. The MOSFETs exhibit significant leakage current more than 1 A/cm^2 when the thickness of ultra-thin silicon gate oxide (SiO_2) is less than 2 nm. To reduce the leakage current related higher power consumption in highly integrated circuit and overcome the physical thickness limitation of silicon dioxide, the conventional SiO_2 will be replaced with high dielectric constant (high-κ) materials as the gate dielectrics beyond the 0.1 μm technology node [1.3]-[1.8]. Therefore, the engineering of high-κ gate dielectrics have attracted great attention and played an important role in technology pull for VLSI. Although high-κ materials often exhibit smaller bandgap and higher defect density than conventional silicon dioxide, using the high-κ gate dielectric can increase efficiently the physical thickness in the same effective oxide thickness (EOT) that shows lower leakage characteristics than silicon dioxide by several orders without the reduction of capacitance density [1.4]-[1.7]. Recently, some high-κ materials have been widely studied and successfully intergraded in advanced MOSFETs or semiconductor devices, such as DRAMs or Flash memory and RF metal-insulator-metal (MIM) capacitors [1.9]-[1.10]. According to the ITRS (International Technology Roadmap for Semiconductor) [1.11], the suitable gate dielectrics must have κ value more than 8 for 50-70 nm technology nodes and that must be more than 15 when the technology dimension less than 50 nm. Fig. 1-1 shows the evolution of MOSFET technology requirement. Moreover, the useful gate dielectrics should meet the following fundamental requirements:

- Thermodynamic stability on silicon with respect to formation of SiO_2 and MSi_x.
- Amorphous after device integration, implies that the dielectrics should remain amorphous after S/D or elevated temperature activation.
- Low conduction for low leakage and low power consumption. For metal oxides (MO_x), it is well known that bandgap is inversely related to κ value (the aluminum oxide as an exception). Low leakage current implies large band-offset for electrons and holes.
- High carrier mobility at the dielectric/Si interface. Therefore, the low D_{it} and low bulk charges (low effective fixed charges) are requirements.
- High breakdown strength and acceptable reliability. The breakdown strength is inversely related to κ value for metal oxides.

The most popular high-κ materials which are studied extensively nowadays are metal oxides (MO_x), such as Ta_2O_5, TiO_2, HfO_2, ZrO_2, Al_2O_3 and La_2O_3 which have the higher κ values ranging from 9 to 80. However, the most metal oxides will have the characteristics of crystallization at elevated temperature which cause devices generate non-uniform leakage distribution and give large statistical variation for nano-meter devices across the chip. Therefore, replacement gate strategies have been proposed to prevent crystallization and deleterious effects of mass and electrical transport along grain boundaries. Figs. 1-2 and 1-3 summarize the κ value and band offset for popular high-κ dielectric candidates.

1.2 Motivation to study metal gate

Metal gate is required for advanced CMOS transistors to eliminate poly gate depletion [1.12]-[1.19]. Since the EOT target prescribed by the ITRS roadmap in years 2018 is only 0.5 nm for 7 nm CMOS [1.11], any depletion of the poly-Si gate electrode will be unacceptable. To overcome this problem, the metal gate electrode will be required to make poly-depletion free due to the poly depletion will reduce the capacitance and contribute a degradation to EOT in inversion state [1.12]-[1.24], is shown in Fig. 1-4. The work function (Φ_B) of metal (in Fig. 1-5) play an important role for metal-gate/high-κ MOSFET. The preferred work function of the metals are ~5.1 eV for p-MOSFETs and ~4.2 eV for n-MOSFETs. However, one of the difficult challenges for metal-gate/high-κ CMOS devices is large threshold voltage (V_{th}) due to

Fermi-level pinning effect. This is especially difficult for p-MOSFET [1.12] since only Ni (5.15 eV), Ir (5.27 eV) and Pt (5.65 eV) in the Periodic Table have work function close to the desired 5.2 eV used in conventional p^+ poly-Si gated p-MOS (in Fig. 1-5). In addition, thermal stability of the effective metal electrode and metal diffusion are also important considerations. Recently, lots of metal or metal-nitride materials have been widely researched and successfully intergraded in advanced CMOSFET's, such as TiN, TaN, Pt, Mo and Ir [1.12]-[1.24]. Tantalum (Ta) has a work-function close to n^+ poly-Si. Tantalum nitride (TaN) is quite stable (to maintain thermal stability up to a 1000°C RTA) because the activation energy of metal and nitrogen is relatively low. Tantalum is bonded tightly within nitride and no obvious diffuse was observed in fabricated devices. However, TaN gate on high-κ HfO_2 shows a significant shift of flat band voltage (V_{FB}) toward the mid-gap of Si due to the interface reaction between the TaN and HfO_2 at the high temperature. This is called the "Fermi-level pinning effect." Therefore, the Fermi-level pinning effect needs to be avoided by selecting suitable metal gate and high-κ materials for advanced MOSFETs.

For MONOS structured non-volatile memory device, the metal electrode with high work function is needed. The metal gate with higher work-function can prevent the electron injection from electrode in erase operation [1.25]. That improves efficiently erase speed.

1.3 Motivation to study MONOS memory

The semiconductor memory can be divided into volatile and non-volatile memory (Fig. 1-6). For volatile memory such as Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), the stored information will lose when the power is off. On the contrary, the non-volatile memory could hold its data stored in off-power state. In addition, the one transistor (1T) structure of non-volatile memory can save more cell area than 1T1C DRAM with high cell density. Recently, the non-volatile memory is also important for mobile or portable electronic products, especially the conventional poly-Si floating gate Flash memory devices (Fig. 1-6). However, the key issue for electrical-conductive poly-Si is the scaling of tunnel oxide since the storage charges will discharge at very thin tunnel oxide. Moreover, the poly-Si floating gate Flash memory device also need long erase time and thicker tunneling oxide to maintain good charge retention because of hot carrier problems in the floating gate (the reason is shown in Fig. 1-7). Therefore, the thickness of tunnel oxide can only be scaled down to 6-7 nm. This causes the Flash memories need to operate at higher program and erase voltage (the electric field is more than 6 MV/cm). To solve these problems and realize vertical scaling, the conductive poly-Si floating gate is replaced by Si_3N_4 to form the [poly-Si/metal]-SiO_2-Si_3N_4-SiO_2-Si structure; we call the SONOS or MONOS memory devices (the structure is shown in Fig. 1-8). The SONOS/MONOS device is a potentially important non-volatile memory suitable for downscaling below 20 nm [1.26]-[1.30] since the discrete traps in the silicon nitride can prevent complete charge leakage out through single oxide defects, which gives better data retention and useful for 2 bits/cell. Thus a thinner tunnel oxide (<5 nm) can be used in a SONOS/MONOS memory compared with that in a conventional poly-Si floating gate device. This yields lower voltage and faster speed for operation. According to International Technology Roadmap for Semiconductors (ITRS) [1.11], at 2018, the SONOS non-volatile memory will continue down-scaling the thickness of tunnel oxide to 2 nm and program/erase (P/E) voltage to 4.0-4.5 V (the table is shown in Fig. 1-9) with faster speed while maintaining good data retention at elevated temperature. Such low voltage operation under 5 V is also important for embedded system-on-chip (SoC).

1.4 The measurement of the devices

To investigate the electrical characteristics of devices, we measured the I_g-V_g curves for gate leakage current and I_d-V_g for transistor characteristics by using HP 4156A semiconductor parameter analyzer. Besides, HP4284A precision LCR meter was used to evaluate the gate capacitance and the conductance ranging from 100 kHz to 1 MHz. For memory measurement, the fabricated MONOS devices were characterized by program and erase measurements, as well as cycling and retention tests at 85°C and 125°C using an HP4156A Semiconductor Parameter Analyzer and HP8110A 150 MHz Pulse Pattern Generator. In addition, to investigate the RF characteristics (at the frequency above 1 MHz) of AlN single layer memory capacitors, we measured the scattering parameter by using HP8510C network analyzer and the test set. The measurement set-up for S-parameter is shown in Fig. 1-10. Network analyzer generates a calibrated RF signal and has three input measuring channels. These are commonly called the R, the A, and the B channels. The R channel is used to measure the incident voltage, and the A and B channels measure reflected and transmitted voltages. Then, we can obtain S_{11} and S_{21} by calculating A/R and B/R in polar form, respectively. The S_{12} and S_{22} can also be obtained using the same way except changing the input voltage channel. The noise figure and associated gain were measured by HP85122A and ATN-NP5B noise parameter extraction system up to 6 GHz. There are three major categories of measurement type that the system can supply: DC, S-parameters, and noise parameters. The first two categories mainly support the noise parameter measurement.

1.5 Innovation and contribution

One of the difficult challenges for DRAM technology is the charge loss in the storage capacitor. This problem may be overcome by using high capacitor density and frequent refreshing but become more difficult as scaling down due to the limited available high-κ dielectric. Although the phase change memory (PCM) or ferroelectric material may provide an alternative solution with additional non-volatile function, the density of available PCM or FeRAM is still relatively low [1.31]. In this dissertation, we propose a new approach using the AlN capacitor for 1T1C memory such as DRAM that has good data retention and program-erase function by charge trapping or de-trapping in the high trap density AlN. Although the charge trapping mechanism is similar to MONOS memory, the erase mechanism in single layer AlN is fundamentally different from the multi-layer MONOS. The programmed charges can be erased by a small voltage of -4 V for 1 ms; this is impossible for single layer Al_2O_3 or other known high-κ dielectric where continuously increasing V_{th} and charge trapping are found. In addition, the AlN has unique merit of higher trap density than Al_2O_3 similar to that of Si_3N_4 than SiO_2, which is confirmed by the larger V_{th} shift at the same electric field. The possible erase mechanism may be due to the smaller bandgap (E_G ~6.0 eV) or ΔE_V than Al_2O_3 (E_G ~9.0 eV) with additional higher trap density that allows hole injection or electron tunnel out from these high trap density states. Another merit of this capacitor is the long retention time and evident to the small V_{th} variation of 0.06 V after program or erase for 10^4 s and the potential of extended long memory time. This program-erasable high-κ AlN capacitor with good data retention provides an alternative solution to 1T1C memory.

The [poly-Si/metal]-SiO_2-Si_3N_4-SiO_2-Si (SONOS/MONOS) memory devices are potentially important because the discrete traps permit 2 bits of charge storage in the nitride. The isolated charges stored in discrete traps can prevent complete charge leakage out through single oxide defects. This is the primary failure mechanism for electrical-conductive poly-Si floating gate Flash memory. Thus a thinner bottom oxide (<4 nm) can be used in a SONOS/MONOS memory compared with that in a conventional poly-Si floating gate device. This, in turn, yields faster program and erase (P/E) functions. Furthermore, the MONOS may be even better than SONOS for erase due to additional work-function control by metal-gate [1.28]. According to International Technology Roadmap for Semiconductors (ITRS) at year 2018 [1.11], the SONOS NVM may continue down-scaling the tunnel oxide to 2 nm with very low program/erase (P/E) voltage to 4.0-4.5 V and fast speed while maintaining good data retention of >10 years at elevated temperature. Such low voltage operation < 5 V is also important for embedded system- on-chip (SoC).

However, the MONOS memory with thinner tunnel oxide may result in relative poor data retention and therefore a better trapping layer is needed [1.30]. In this dissertation, we first compare the trapping capability between normally used Si_3N_4 with novel AlN dielectric. Significant better charge trapping is measured in AlN than

Si_3N_4, where good P/E and retention characteristics can be achieved even in single layer AlN. Such excellent performance is further evident from the much better memory integrity in IrO_x-HfAlO-AlN-SiO_2-Si device with lower operation voltage, faster P/E speed and good retention than the best reported SONOS data using Si_3N_4 trapping layer. At 13 V and 100 μs program and -12 V 100 μs erase, we found a large threshold voltage shift (ΔV_{th}) of 3.1 V that extrapolated to 1.4 V for 10-year retention at 85°C. These values increased to 3.7 V for the initial ΔV_{th} and 1.9 V for the 10 year case at ±13 V and 100 μs P/E. This 100 μs speed, low operation voltage of 12-13 V, withstand above 10 k cycles and 1.9 V 10-year memory retention window at 85°C meet all the non-volatile memory requirements simultaneously [1.26].

Using the same concept, we further provide the TaN-HfAlO-HfON-SiO_2-Si MONOS device to operate at only 8 V under faster 100 μs. Such low P/E voltage is achieved by using novel HfON trapping layer with very high κ of 22 beyond AlN (κ~10). Under fast 100 μs at ±8 V for P/E, the device exhibits a large initial ΔV_{th} (memory window) of 2.5 V and the 10-years extrapolated retention window of 1.0 V at even 125°C. The good high temperature data retention is also due to the deep trapping of HfON similar to AlGaN [1.31]. Using a simple voltage inverter circuit, the P/E voltage can further be reduced to nearly half: by applying 4.5 V and -3.5 V for the same ±8 V gate-channel bias. This is useful for embedded SoC under a single 5 V voltage source. Fig. 1-11 shows the summary and structure of this dissertation.

		2003	2005	2007	2009	2012	2015	2018
Gate Length (nm)		107	80	65	50	30	25	18
EOT (nm)	**High Speed**	1.3	1.2	0.9	0.8	0.7	0.6	0.5
	Low Power	1.6	1.4	1.2	1.0	0.9	0.8	0.7
S/D Junction Depth (X_j, nm)*		49.5	35.2	27.5	NA	NA	NA	NA
Interconnect Levels		9	11	11	12	12	13	14
Logic V_{DD} (V)	**High Speed**	1.2	1.1	1.1	1.0	0.9	0.8	0.7
	Low Power	1.0	0.9	0.8	0.8	0.7	0.6	0.5

Source: International Technology Roadmap for Semiconductor (ITRS 2003)

Fig. 1-1 The evolution of MOS technology requirement.

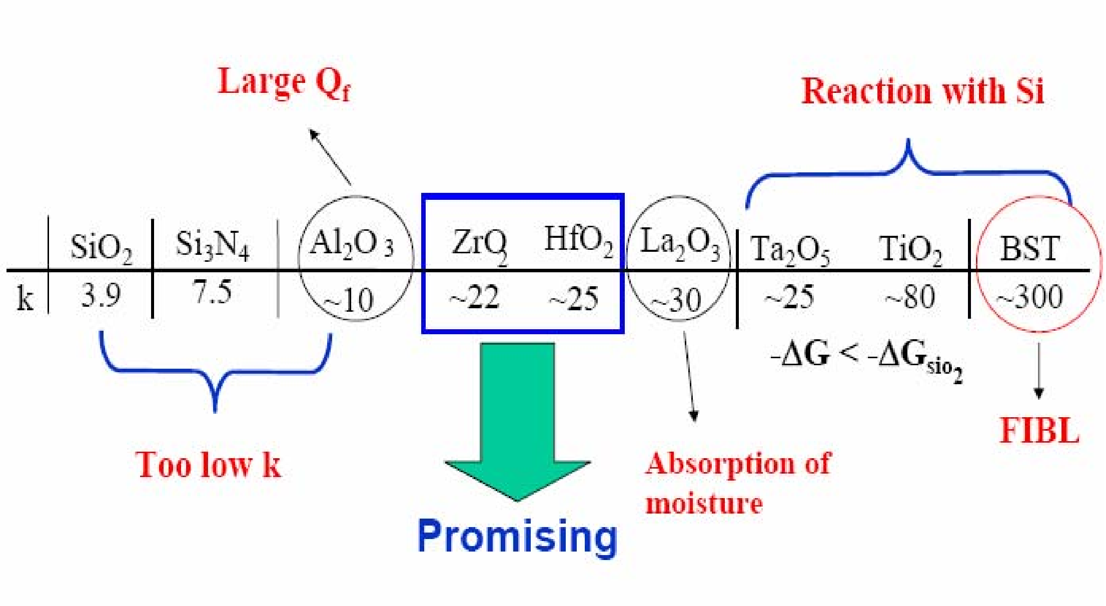


Fig. 1-2 The κ value of high-κ materials.

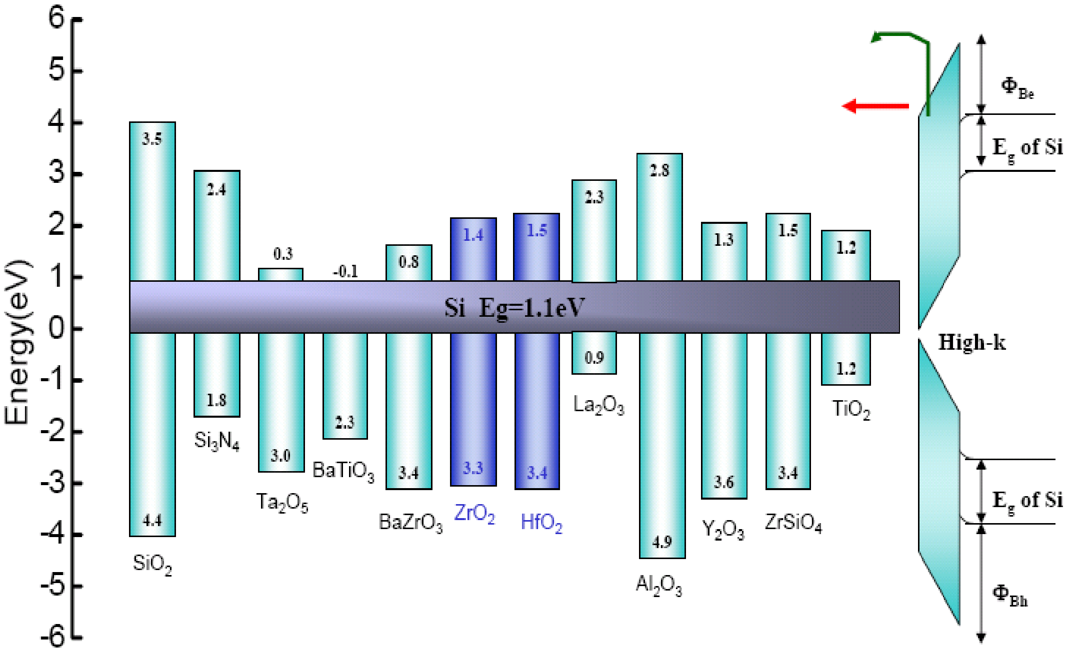
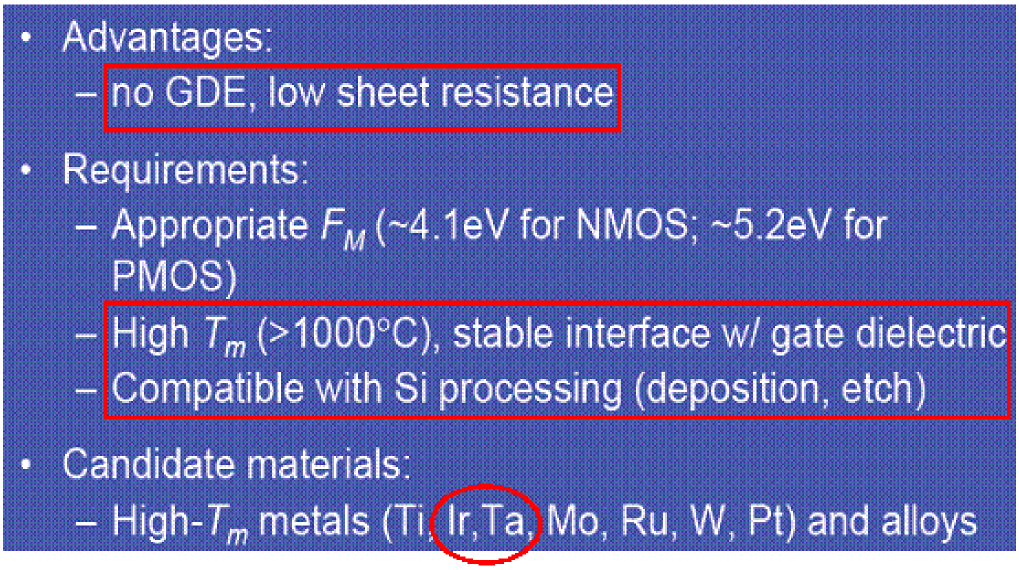


Fig. 1-3 The band offset of popular high-κ materials.



- Advantages:
  - no GDE, low sheet resistance
- Requirements:
  - Appropriate F_M (~4.1eV for NMOS; ~5.2eV for PMOS)
  - High T_m (>1000°C), stable interface w/ gate dielectric
  - Compatible with Si processing (deposition, etch)
- Candidate materials:
  - High-T_m metals (Ti, Ir,Ta, Mo, Ru, W, Pt) and alloys

Fig. 1-4 The advantages and requirements of metal gate technology.

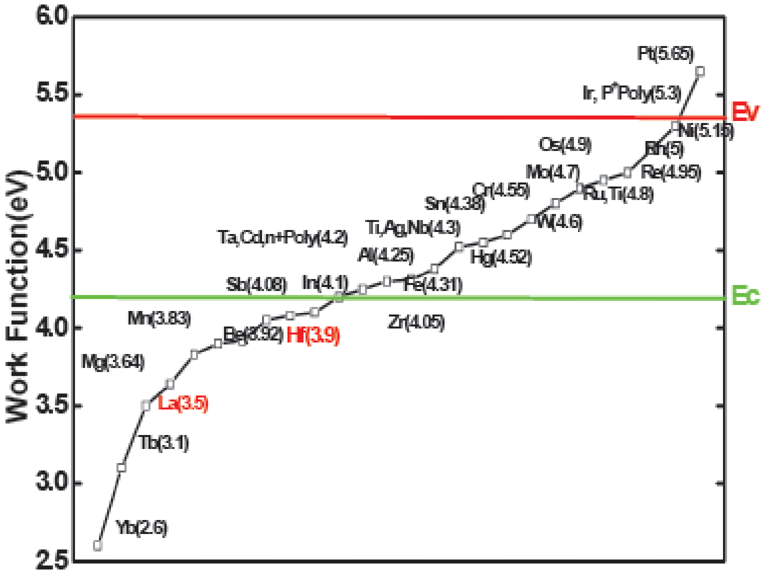
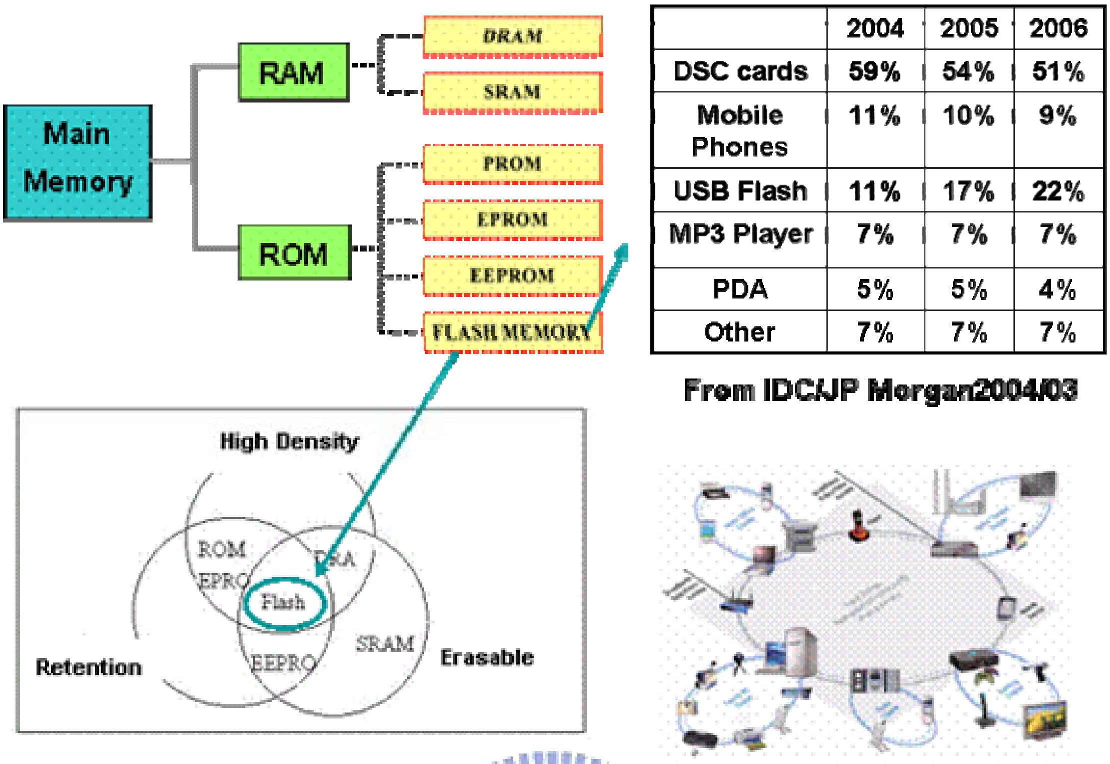


Fig. 1-5 The values of work function for different metal materials.



	2004	2005	2006
DSC cards	59%	54%	51%
Mobile Phones	11%	10%	9%
USB Flash	11%	17%	22%
MP3 Player	7%	7%	7%
PDA	5%	5%	4%
Other	7%	7%	7%

From IDC/JP Morgan2004/03

Fig. 1-6 The advantages and functions of non-volatile Flash memory.

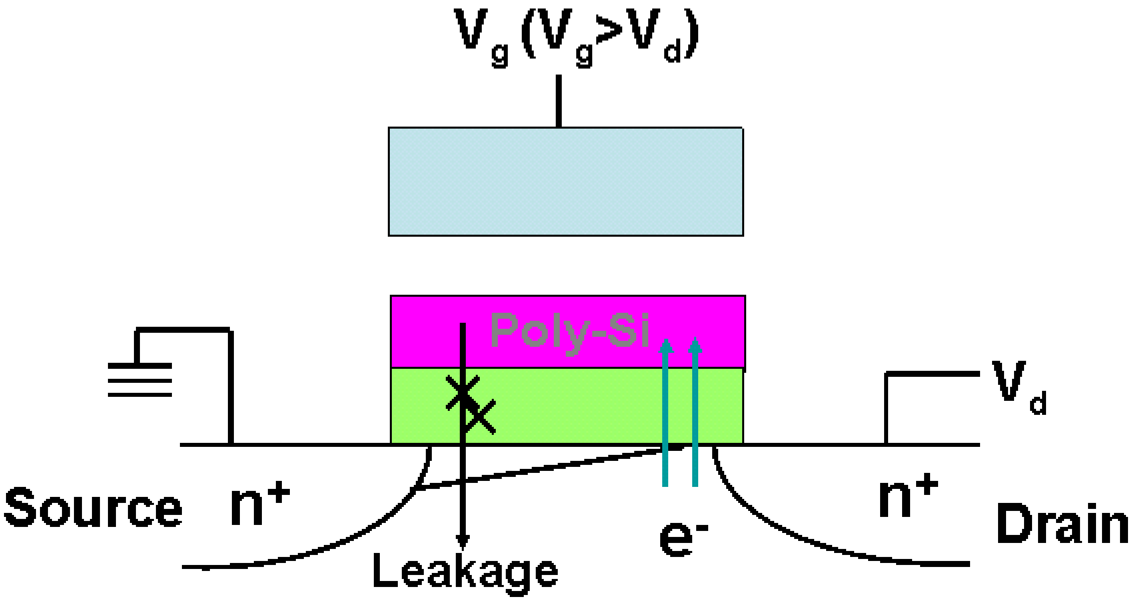


Fig. 1-7 Hot carrier problems in the electrically conductive poly-Si floating gate Flash memory.

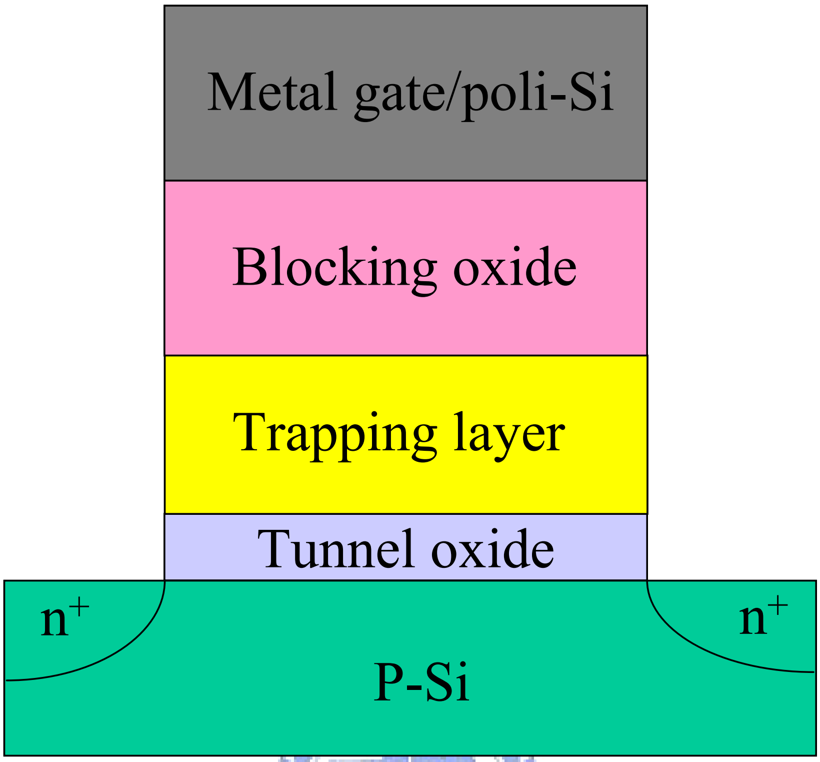
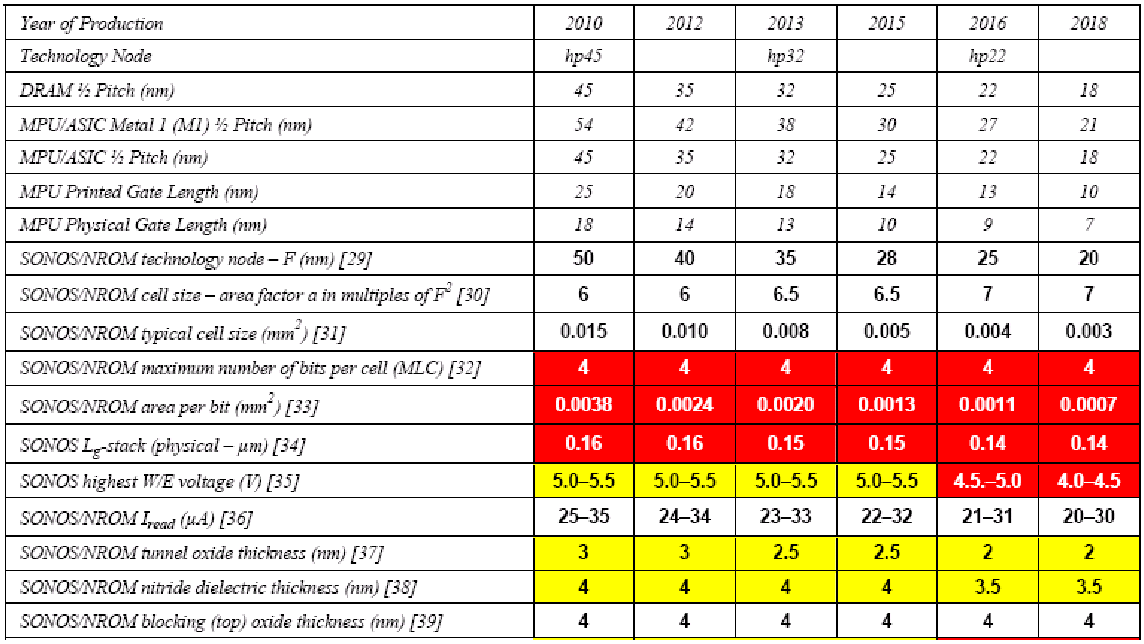


Fig. 1-8 The cross section of metal [gate/poly-Si]-SiO_2-Si_3N_4-SiO_2-Si memory



Year of Production	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Technology Node	*hp45*		*hp32*		*hp22*	
DRAM ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*54*	*42*	*38*	*30*	*27*	*21*
MPU/ASIC ½ Pitch (nm)	*45*	*35*	*32*	*25*	*22*	*18*
MPU Printed Gate Length (nm)	*25*	*20*	*18*	*14*	*13*	*10*
MPU Physical Gate Length (nm)	*18*	*14*	*13*	*10*	*9*	*7*
SONOS/NROM technology node – F (nm) [29]	50	40	35	28	25	20
SONOS/NROM cell size – area factor a in multiples of F^2 *[30]*	6	6	6.5	6.5	7	7
SONOS/NROM typical cell size (mm^2) *[31]*	0.015	0.010	0.008	0.005	0.004	0.003
SONOS/NROM maximum number of bits per cell (MLC) [32]	**4**	**4**	**4**	**4**	**4**	**4**
SONOS/NROM area per bit (mm^2) *[33]*	**0.0038**	**0.0024**	**0.0020**	**0.0013**	**0.0011**	**0.0007**
SONOS L_g*-stack (physical – µm) [34]*	**0.16**	**0.16**	**0.15**	**0.15**	**0.14**	**0.14**
SONOS highest W/E voltage (V) [35]	5.0–5.5	5.0–5.5	5.0–5.5	5.0–5.5	**4.5.–5.0**	**4.0–4.5**
SONOS/NROM I_{read} *(µA) [36]*	25–35	24–34	23–33	22–32	21–31	20–30
SONOS/NROM tunnel oxide thickness (nm) [37]	3	3	2.5	2.5	2	2
SONOS/NROM nitride dielectric thickness (nm) [38]	4	4	4	4	3.5	3.5
SONOS/NROM blocking (top) oxide thickness (nm) [39]	4	4	4	4	4	4

Fig. 1-9 The requirements for SONOS memory from ITRS.

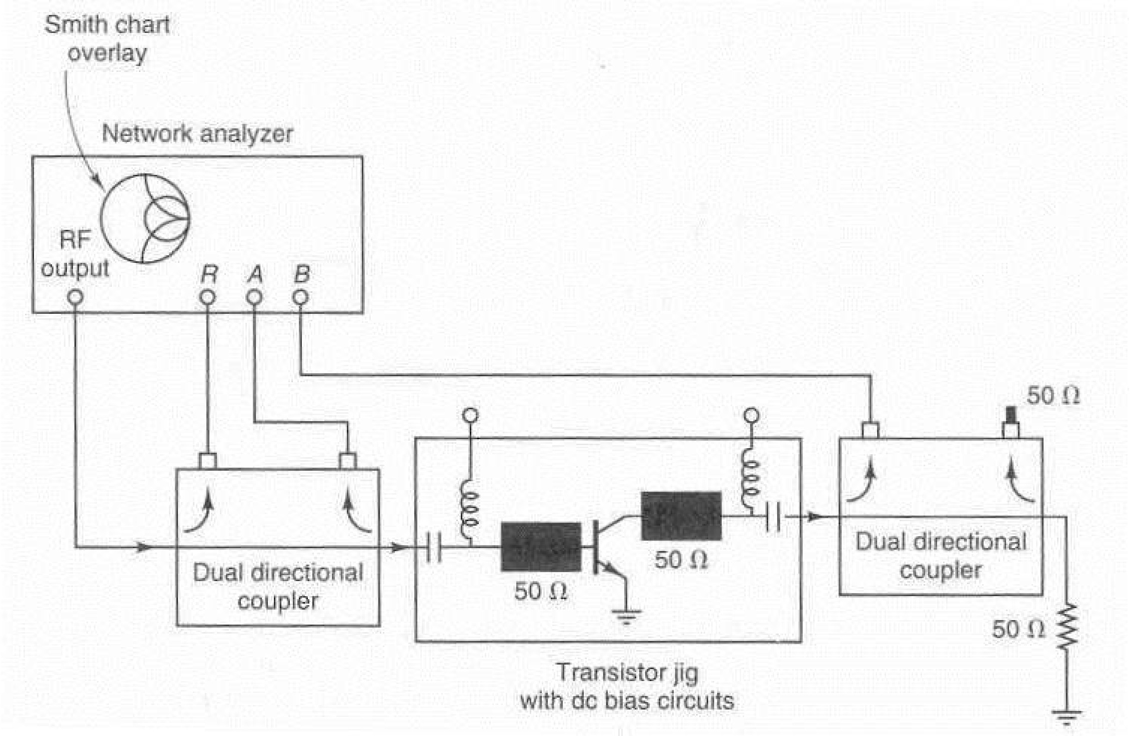


Fig. 1-10 The measurement set-up for S-parameter.

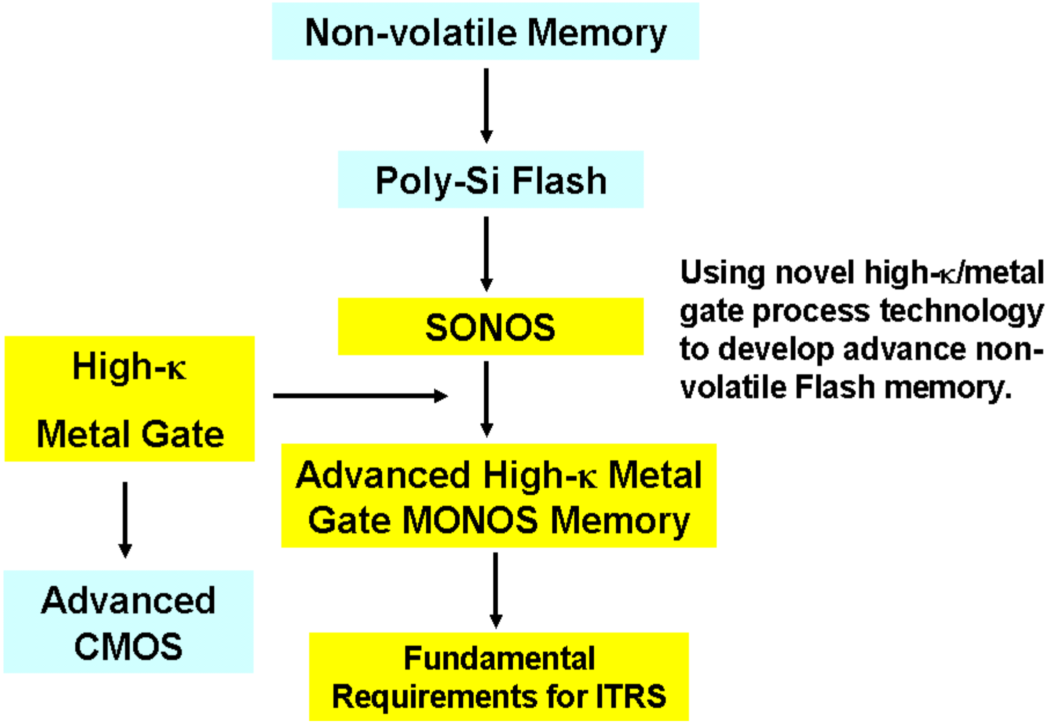


Fig. 1-11 The summary and structure of this dissertation.

Chapter 2

A Novel Program-erasable High-κ AlN/Si MIS Capacitor

2.1 Introduction

For analog and RF [2.1]-[2.8] ICs and memory applications, capacitors with a high capacitance density are preferred. It is also desirable to have a program-erasable capability. This is especially important for RF ICs where process variations can shift the resonance frequency of LC tank away from designed values, creating impedance mismatches and bandpass frequency differences [2.8]. Program-erasable capacitors can also extend the data retention for DRAMs leading to less frequent re-flashing cycles. In this work, we propose and demonstrate a MIS capacitor on Si using a single layer of high-κ AlN dielectric, which exhibits the program-erase function as well as good data retention. The single layer high-κ capacitor has a programmable C-V, which can be erased by -4 V bias for 1ms. In contrast, this does not occur for high-κ Al_2O_3 [2.1]-[2.3] or AlON capacitors. The possible erase mechanism may be due to the smaller bandgap (E_G ~6.0 eV) or ΔE_V (valance band offset) of AlN compared with Al_2O_3 (E_G ~9.0 eV) [2.1]-[2.3], which could permit hole injection or electron tunneling out of high density of trap states. After 10^4 s, the program-erase cycle showed good retention of threshold voltage (V_{th}) shift of only 0.06 V.

2.2 Experimental

The MIS capacitors were fabricated using low temperature high-κ dielectric process [2.1]-[2.15] on 4-in 5-10 Ω-cm p-type Si wafer. After standard pre-gate clean, an AlN dielectric of 16 nm was deposited by physical vapor deposition (PVD) system [2.1]-[2.5] and annealed at 400°C for 5 min in a furnace under N_2 ambient. Finally, Al metal was deposited by PVD and then patterned by photo lithography to form top electrode with capacitor area of 100 μm×100 μm. (Note that the processing at low temperature of 400 °C would permit integration into the back end of a VLSI fabrication line.) The resulting structure is shown in Fig. 2-1. For comparison, we also fabricated single layer Al_2O_3, AlON and Si_3N_4 capacitors. All the C-V characteristics were measured by HP4284A at 1 MHz, and a pulse generator was used for the program and erase study.

2.3 Results and discussion

Figs. 2-2(a) and 2-2(b) show the measured C-V hysteresis of Al/AlN/Si MIS capacitors. The high-κ AlN/Si capacitors with as-deposited AlN dielectric show large memory window of 2 V after -5~10 V sweep. After 400°C and 5 min PDA, the memory window of 1.5 V was still measured. The XRD measurement of high-κ AlN dielectrics is displayed in Fig. 2-3. The high-κ AlN dielectrics are still amorphous after 400^{o}C and 20 min annealing. Next, we apply a positive voltage on Al electrode and program the high-κ AlN/Si MIS capacitors from 4~11 V for 1 ms. The threshold voltage has significant shift after 4 V and 1 ms program (in Fig. 2-4). Figs. 2-5(a) and 2-5(b) show the measured C-V characteristics and time-dependence of the V_{th} shift for a high-κ AlN MIS capacitor. The capacitor was measured under applied ±2 to ±4 V voltages for times from 0.1 to 100 ms. The V_{th} shifts increase with increasing applied voltage. The V_{th} of 0.24 V for +4 V and of -0.27 V for -4 V applied for 1 ms shows that the AlN capacitor can be programmed or erased, similar to SONOS memory [2.16]-[2.19]. In sharp contrast (shown in Fig. 2-6), only a few mV of V_{th} changes are measured in Si_3N_4/Si capacitor fabricated by VLSI backend process with close capacitance density. The larger hysteresis of C-V curve indicates the stronger carrier trapping (higher density and/or deeper energy of traps) in the AlN device than that of Si_3N_4 capacitor. The $|V_{th}|$ increase largely with increasing program-erase time from 0.1 ms to 1 ms and gradually saturates from 1 ms to 100 ms, suggesting a switching speed of ~1 ms at 4 V bias. The feature of nearly symmetrical positive and negative V_{th} for program and erase functions is important for low voltage applications. In addition, high capacitance density of ~5 fF/μm^2 and low leakage current of 6×10^{-8} A/cm^2 at -2.5 V (shown in Fig. 2.9) are measured in high-κ AlN dielectric capacitor, which are close to those for high-κ Al_2O_3 MIM capacitors reported before [2.1]-[2.2]. The high capacitor density is especially important for backend capacitor [2.1]-[2.5] due to the very thick equivalent-oxide thickness (EOT) > 5 nm and hence the low leakage current. On the other hand, low leakage current is one of the most important factors for high-κ gate dielectric with typical EOT ≤1.5 nm [2.9]-[2.15]. The capacitor density of AlN/Si device is also much higher than that for SONOS capacitors [2.17]-[2.19].

Figs. 2-7 and 2-8 show C-V characteristics of the high-κ Al_2O_3 and AlON capacitors, respectively. The Al_2O_3 capacitor has nearly the same capacitance density and the close V_{th} shift with AlN capacitor. However, continuous increasing V_{th} with increasing applied negative voltage at top Al electrode is measured without erase function, which may be due to increasing trapped negative charges in the high-κ dielectric [2.17]. Similar features, without the erase function, are found in the AlON capacitor, even for -10 V applied voltages. No such erase function is reported for other known high-κ SiN dielectric and it seems to be unique for high-κ AlN dielectrics. Fig. 2-9 shows the leakage current and the fast decreasing J-V slope at high current level may be due to charge trapping to decrease the following carriers' tunnel rate. Figs. 2-10 and 2-11 show the schematic band diagram of metal-gate/high-κ/Si capacitor and Al/AlN/Si, respectively. The possible erase mechanism may arise from the smaller bandgap (E_G~6.0 eV) or ΔE_V for AlN compared with Al_2O_3 (E_G~9.0 eV). This could permit hole injection or electron tunneling out from the high density of trap states, which is less possible for large E_G Al_2O_3.

We show the retention behavior of the AlN capacitor in Fig. 2-12(a). Good program-erase retention properties are evident from the small shift of the C-V curves at up to 10,000 s after removing the 1 ms program-erase voltage. To evaluate the program-erase retention property further, Fig. 2-12(b) shows V_{th} as a function of time, as derived from the measured C-V curves in Fig. 2-12(a). The extended time retention is preserved with only a small V_{th} change of only 0.06 V, after removing the write voltage for 10,000 s. However, the memory window is closed quickly at a raised temperature of 100°C. Figure 2-13 shows the cycling property. The memory window remains almost unchanged although a V_{th} shift of 0.15 V is measured for both on- and off-state. Further improvement is required to extend the high temperature retention and cycling, although these results are already useful for DRAM improvement.

2.4 Conclusion

We have demonstrated a program-erasable high-κ AlN/Si MIS capacitor with good retention. This novel program-erasable capacitor with high capacitance density of ~5 fF/μm^2, low voltage of ±4 V operation, good retention property and low temperature process compatible with VLSI backend line should find wide applications for 1T1C static-dynamic memory and program-erasable varactor for RF ICs.

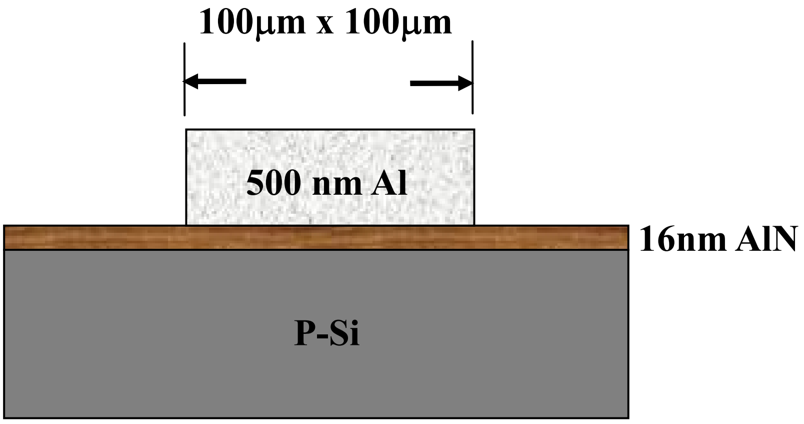
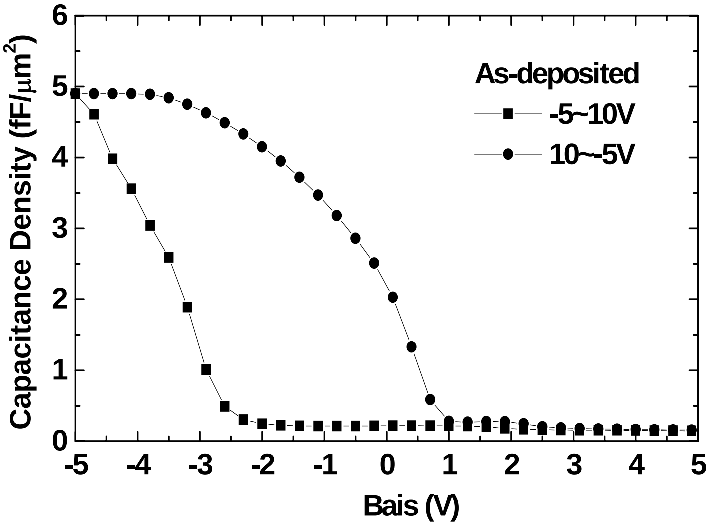
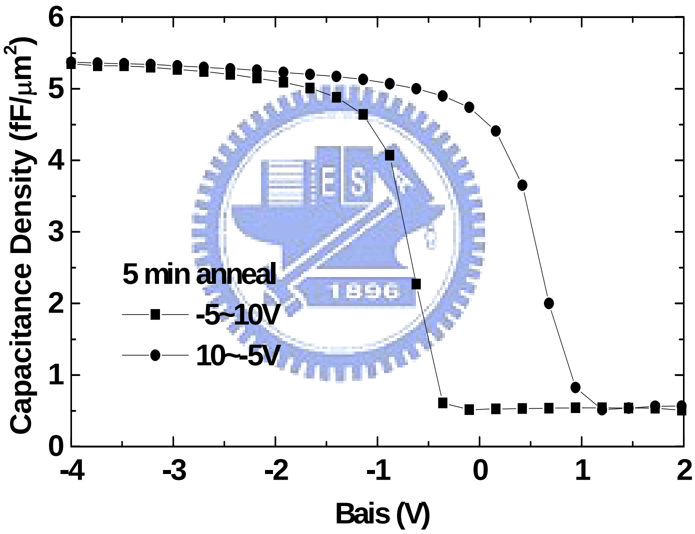


Fig. 2-1 Cross section view of novel program-erasable high-κ AlN MIS capacitors.



(a)



(b)

Fig. 1-12 The measured C-V hysteresis of 16 nm AlN/Si MIS capacitors after (a) as-deposited and (b) 400°C 5 min PDA process.

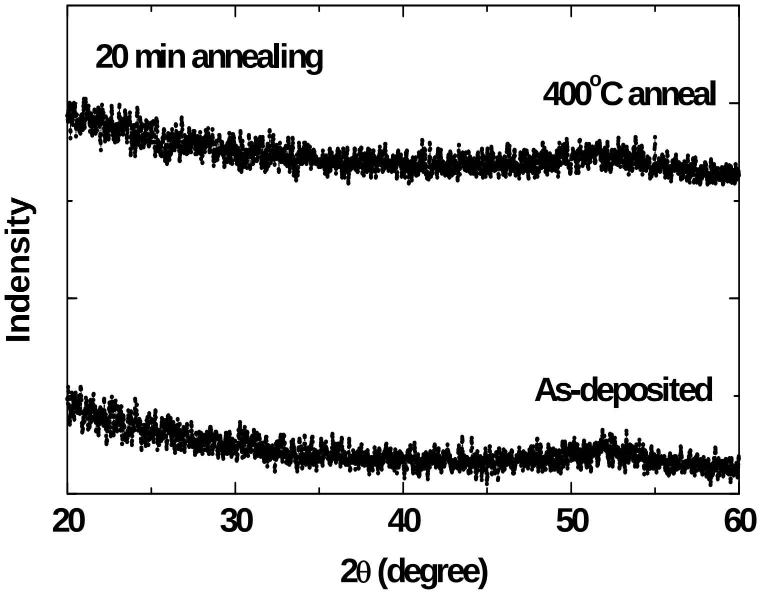


Fig. 2-3 The XRD measurement of as-deposited and 400°C PDA AlN dielectrics. The high-κ AlN dielectrics are amorphous after 400°C and 20 min annealing.

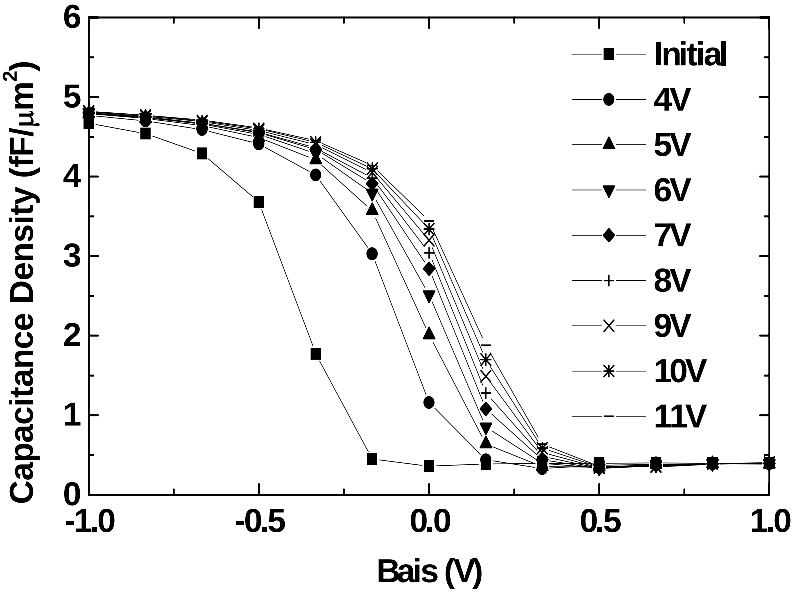
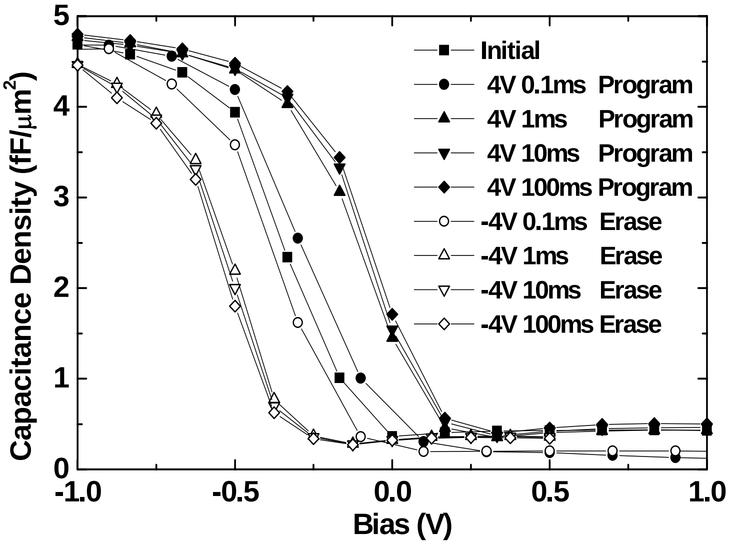
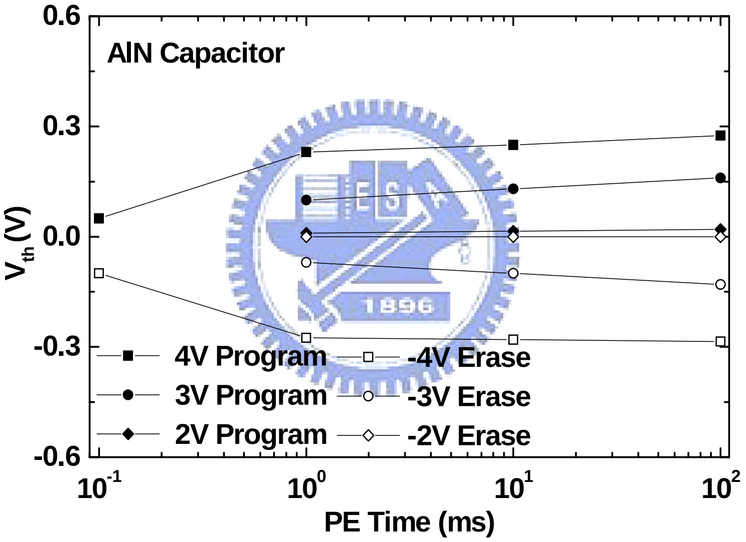


Fig. 2-4 The high-κ AlN single layer MIS capacitor behaves program characteristics under 4 V~11 V for 1 ms.



(a)



(b)

Fig. 2-5 (a) The measured C-V characteristics, and (b) the threshold V_{th} as a function of the duration of the applied voltage, for a single layer high-κ AlN/Si MIS capacitor. The program and erase properties were obtained by applying voltages from ±2 V to ±4 V respectively.

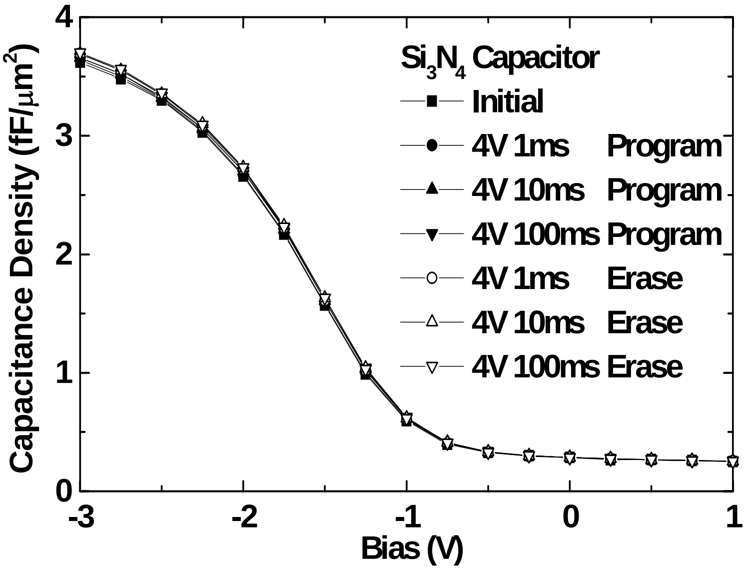


Fig. 2-6 C-V characteristics of an Al/Si_3N_4/Si MIS capacitor. In contrast, a small C-V shift was shown after applying voltages of +4 and -4 V, which suggests shallower trap energy or lower trap density in the Si_3N_4 MIS device.

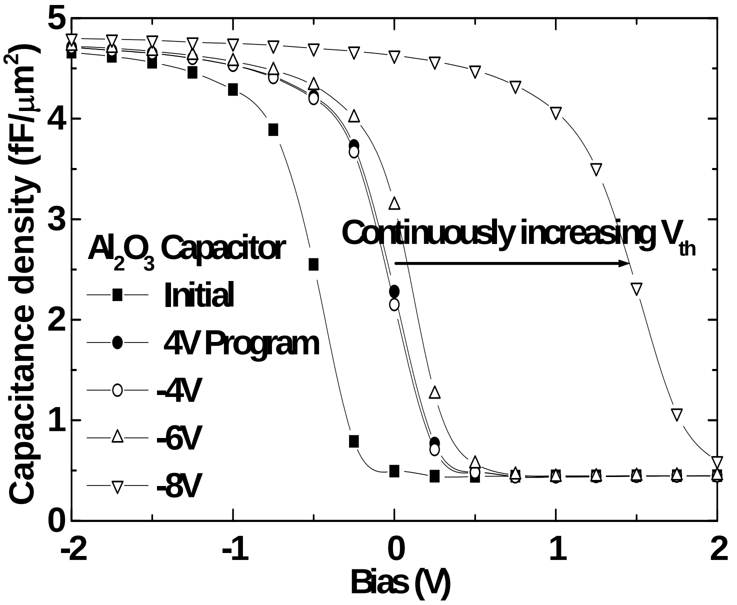


Fig. 2-7 The measured C-V characteristics of high-κ single layer Al_2O_3 MIS capacitors. Continuously increasing V_{th} is observed and can not be erased by negative voltage.

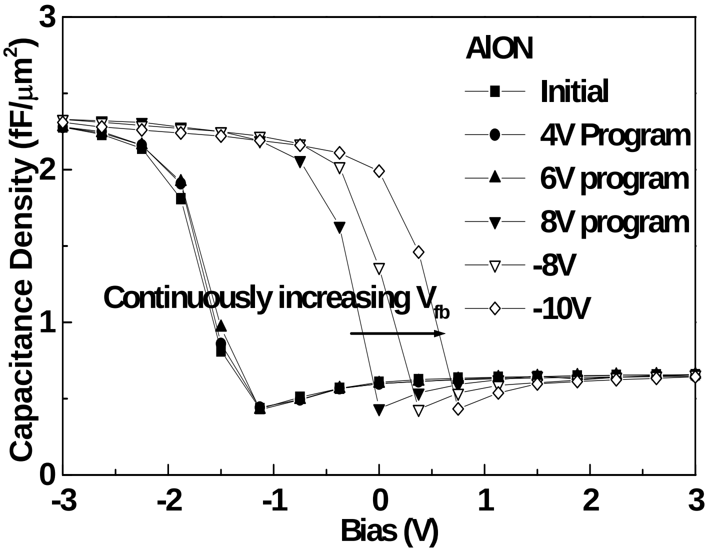


Fig. 2-8 The measured C-V characteristics of high-κ single layer AlON MIS capacitors. Continuously increasing V_{th} is observed at negative voltage without the erase function.

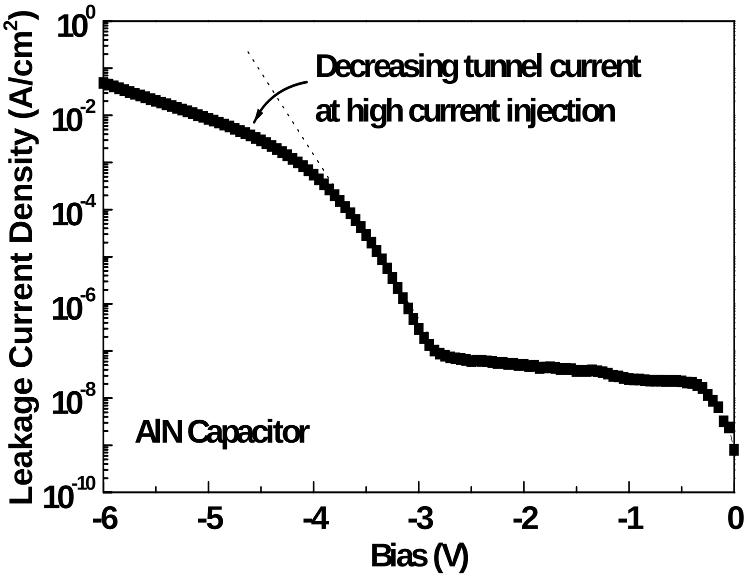


Fig. 2-9 The measured J-V characteristics of AlN capacitor. The fast decreasing slope may be due to charge trapping in AlN and decrease the subsequent carriers' tunnel rate.

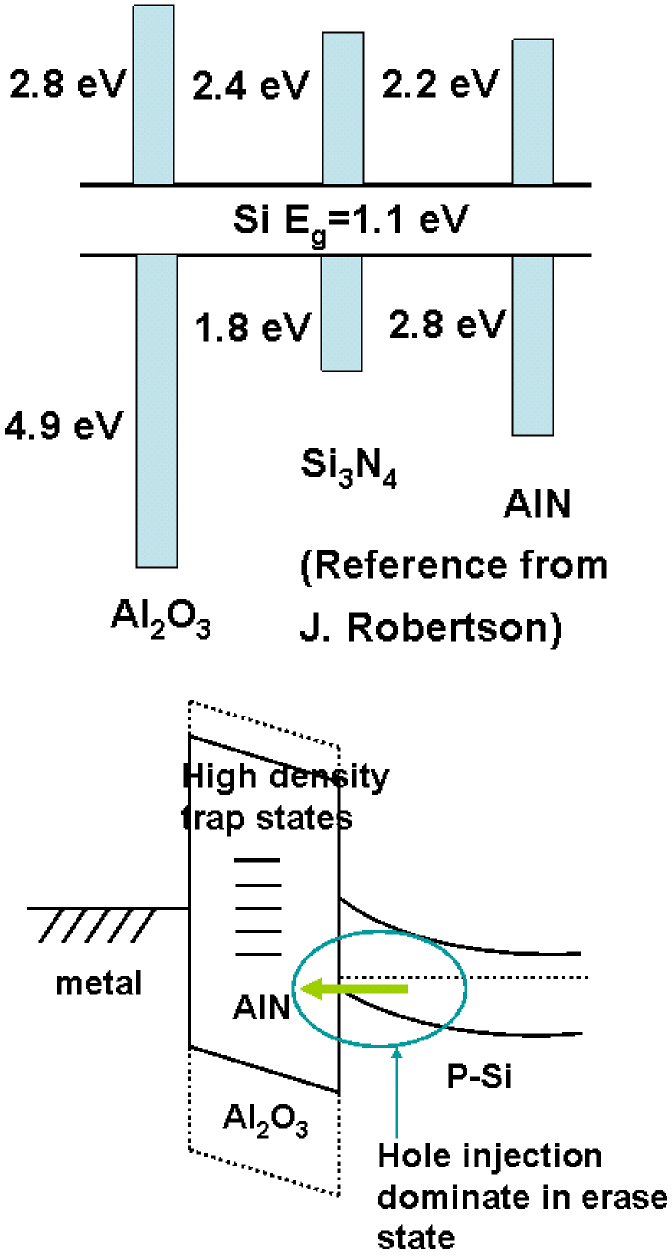


Fig. 2-10 The schematic band diagram of the metal-gate/high-κ dielectric/Si MIS capacitor in erase state.

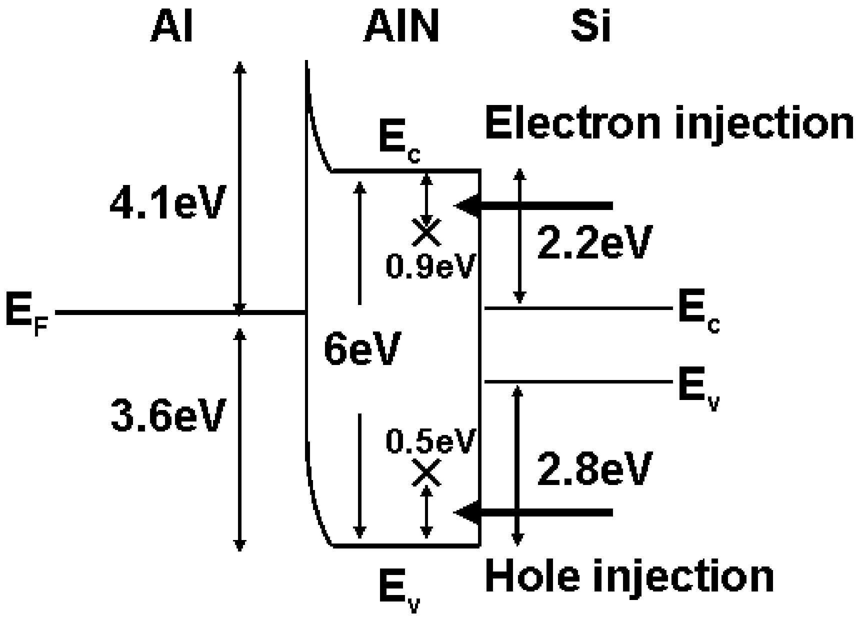
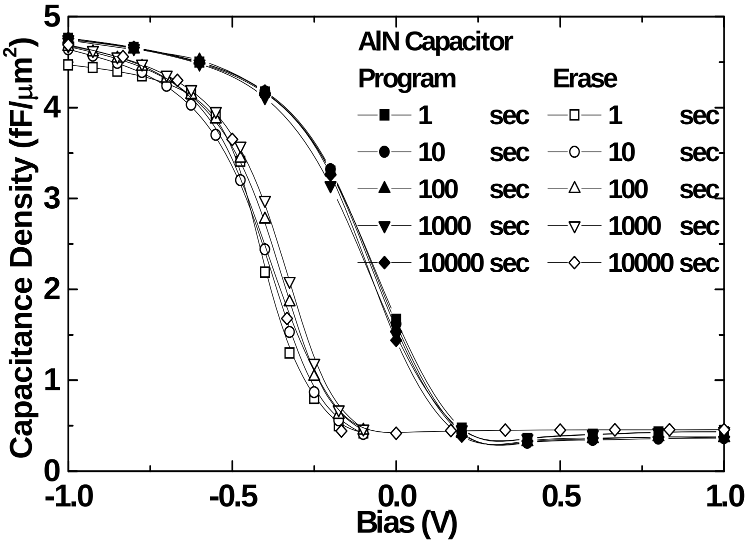
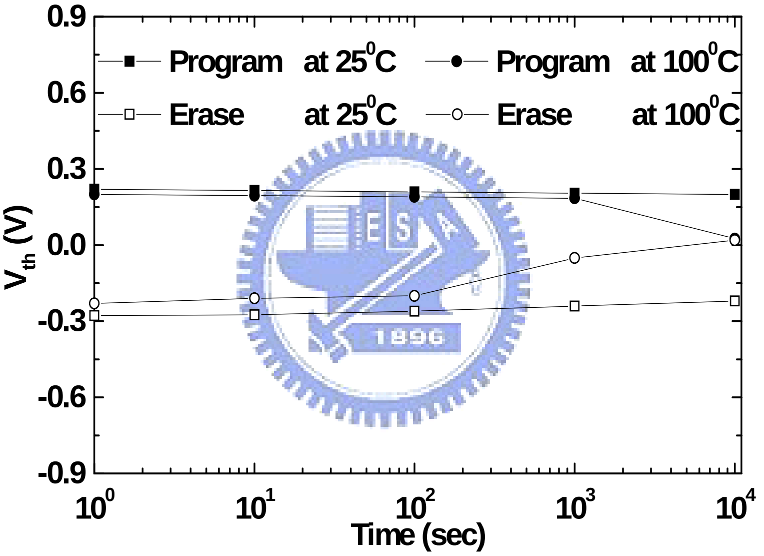


Fig. 2-11 The schematic band diagram of the Al metal gate/high-κ AlN/Si MIS capacitor.



(a)



(b)

Fig. 2-12 (a) The C-V characteristics of an AlN MIS capacitor used for retention, measured from 10 s to 10000 s after removing the 1 ms +4 V program or -4 V erase voltage; (b) the threshold V_{th} as a function of retention time, derived from (a).

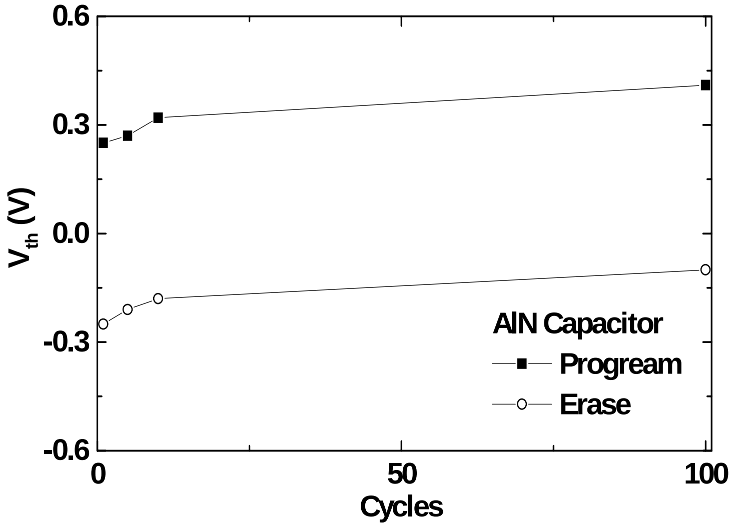


Fig. 2-13 The cycling property of Al/AlN/Si MIS capacitor.

Chapter 3

The Tunable and Program-erasable RF MIS Capacitor with Long Tuning Memory

3.1 Introduction

When designing RF ICs it is desirable to have a tuning capability within the RF circuit. This is because process variations shift the resonance frequency of LC tank circuits away from their modeled values, creating impedance mismatches and bandpass frequency differences from those simulated. The tuning capability may arise from changing the L or C value inside the circuit, however changing inductance is still not simple, even using MEMS technology. In contrast, tunable capacitors, or varactors, are used to tune the resonance frequency of VCOs, although an additional voltage bias circuit has to be used. In this research, we propose and demonstrate a new tunable high-κ capacitor [3.1]-[3.6] similar to a varactor [3.7]-[3.8], which has an additional function of having long program-erase retention. It is thus capable of retaining the tuned capacitor value without always being connected to the bias circuit.

The novel program-erasable feature of the capacitor arises from injected carriers being trapped and de-trapped in an AlN capacitor and shifting the C-V curve permanently. This charge trapping mechanism has been successfully applied to form semi-insulating Si for RF passive devices, giving performance close to those on GaAs [3.9]-[3.10]. The trapped charges can only be removed by applying an erase voltage, to regain the original C-V characteristic. Although the program and erase function is similar to a non-volatile Si/oxide/nitride/oxide/Si (SONOS) memory [3.11]-[3.12], the mechanism is different since only a single trapping AlN layer is used, rather than the complicated SONOS structure [3.11]-[3.12]. In addition, the capacitance density of a single layer high-κ AlN capacitor is much higher than the SONOS device and is comparable with a high-κ Al_2O_3 capacitor [3.1]-[3.2] – this is important to reduce the capacitor area and die size of RF ICs. This simple varactor, with a program-erasable function and long tuning memory capability, should find wide applications to tune the impedance mismatching and resonance frequency offset, without requiring that the voltage bias circuit be connected always. This feature should also permit RF IC design with fewer design cycles. Fig. 3-1 shows the application of such a non-volatile capacitor.

3.2 Experimental

The MIS capacitors were fabricated using an advanced high-κ dielectric process [3.1]-[3.6], [3.17]-[3.20]. The device layout is similar to the varactors used in RF circuits [3.1]-[3.5], where the n^+ source-drain is used to connect the bottom of the MIS capacitors (similar to source-drain to connect channel). After defining and opening the active capacitor area, a thin AlN layer was deposited on the Si, and then annealed at $400^{o}C$ to form the high-κ AlN dielectric. Finally, the top capacitor electrode and transmission line were defined with patterned Al. The resulting structure is shown in Fig. 3-2. The high-κ MIM capacitors were characterized using an HP4284A LCR meter to 1 MHz, for tuning capability measurements. The S-parameters were measured, up to 20 GHz, to characterize the RF performance using an HP8510C VNA. Additional 'through' transmission lines [3.9] were measured to de-embed the parasitic inductance in the RF layout of the MIM capacitors. A similar method has been used for RF noise analysis of 0.18 to 0.13 μm MOSFETs [3.13].

3.3 Results and discussion

A. *Tuning and program-erase performance:*

Fig. 3-3 shows the measured C-V characteristics of a high-κ MIS tunable capacitor. The large tunability of 12 in C_{max}/C_{min} is due to the high capacitance density ($\varepsilon_0 k/t_k$) arising from the high-κ gate dielectric. The capacitance density of 4.8 $fF/\mu m^2$ is close to that for high-κ Al_2O_3 MIM capacitors, reported previously [3.1]-[3.2]. In additional to the large tunability, this high-κ MIS capacitor has unique program and erase functions that can shift the flat band voltage (V_{FB}) of the capacitance by applying $+V_g$ and $-V_g$ voltages, respectively. The reason for this is that electrons can be injected and holes may also be injected into the AlN MIS capacitor during the $+V_g$

and -V_g bias causing the stored charge to decrease, because of the relatively smaller E_G or ΔE_V in AlN (~6.0 eV). To the best of our knowledge, this is the first report that a single layer high-κ dielectric can have the program-erase function with high capacitance density.

B. Program-erase retention characteristics:

It is important that the long retention of the shifted C-V be preserved after removing the applied voltage. Fig. 3-4 shows the measured C-V characteristics of an AlN MIS capacitor after applying respective program or erase voltages of +4 V or -4 V for 1 ms. The C-V measurements were done after the program-erase, from 10 s to 10,000 s. Good program-erase retention is evident from the small shift of the C-V characteristics or the V_{FB}, even after removing the write voltage for 10,000s. To evaluate the program-erase retention further, we have plotted the threshold voltage (V_{th}) from the measured C-V curves as a function of time in Fig. 3-5. The almost symmetrical + V_{th} for program and - V_{th} for erase, is important for low voltage applications. The small variation in ± V_{th} with time suggests excellent memory characteristics. This may be useful for long retention after removing the program-erase voltage, similar to the feature of a non-volatile memory.

C. RF characteristics:

To investigate the RF characteristics of this tunable and program-erasable AlN capacitor, we first establish an equivalent circuit model. As shown in Fig. 3-6, the parallel C and R_p are the basic models for the high-κ capacitor, whereas additional small series R_s and L_s are the parasitic resistance and inductance in the coplanar transmission line. The R and C shunt pass to ground is the transmission line loss to the ground [3.9]. The intrinsic RF characteristics of an AlN MIS capacitor can be obtained by de-embedding the through line [3.3], [3.13] in additional to the open pad.

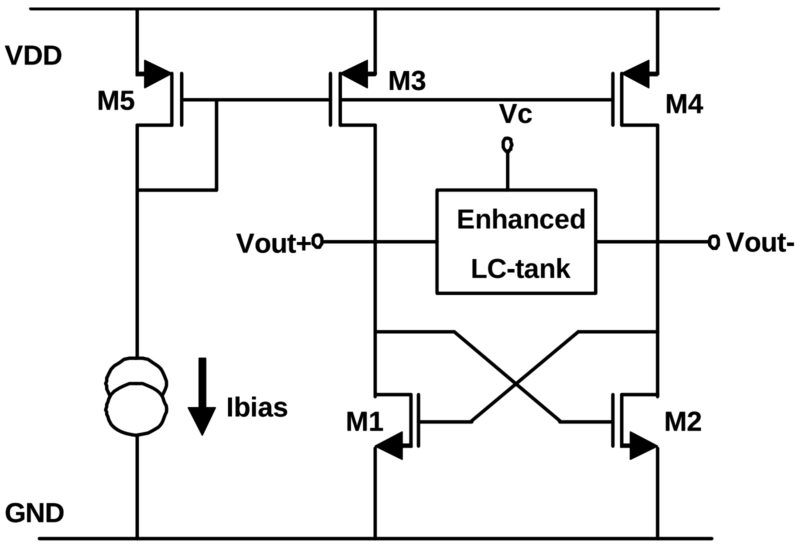
The S-parameters for an AlN MIS capacitor are shown in Fig. 3-7. For comparison, the simulated results using equivalent circuit model in Fig. 3-6 are also included. The good agreement between the measured and simulated data over the wide frequency range from 200 MHz to 20 GHz suggests that the equivalent circuit model shown in Fig. 3-6 is appropriate for capacitance extraction.

The frequency dependence of the AlN MIS capacitance, as extracted from the measured and simulated S-parameters, is shown in Fig. 3-8. The high capacitance value can be maintained until the frequency approaches the resonance frequency of 9.7 GHz. This feature is due to the small parasitic inductance in the transmission line even after de-embedding. The relatively low resonance frequency ($1/2\pi\sqrt{LC}$) arises from the large capacitance and high-κ dielectric properties of AlN.

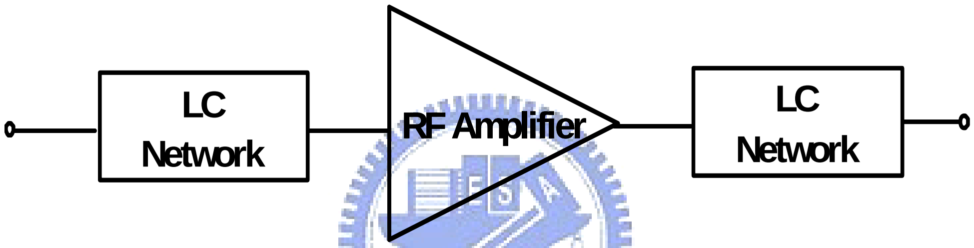
We have also determined the Q-factor for the AlN MIM capacitor, which is shown in Fig. 3-9. The good RF performance is exemplified by a Q-factor of 65 at the frequency of 6 GHz. The Q-factor decreases rapidly as the frequency nears the resonance frequency and the parasitic inductance from the transmission line dominates.

3.4 Conclusion

We have developed a novel program-erasable high-κ AlN MIS capacitor which has long tuning memory. High capacitance density of ~5 fF/μm^2 was obtained with a large C_{max}/C_{min} tunability of 12. Good tuning memory was shown by the small V_{th} variation, after programming or erasing at ± 4 V, for 10,000 s and the potentially long extrapolated memory time of years.

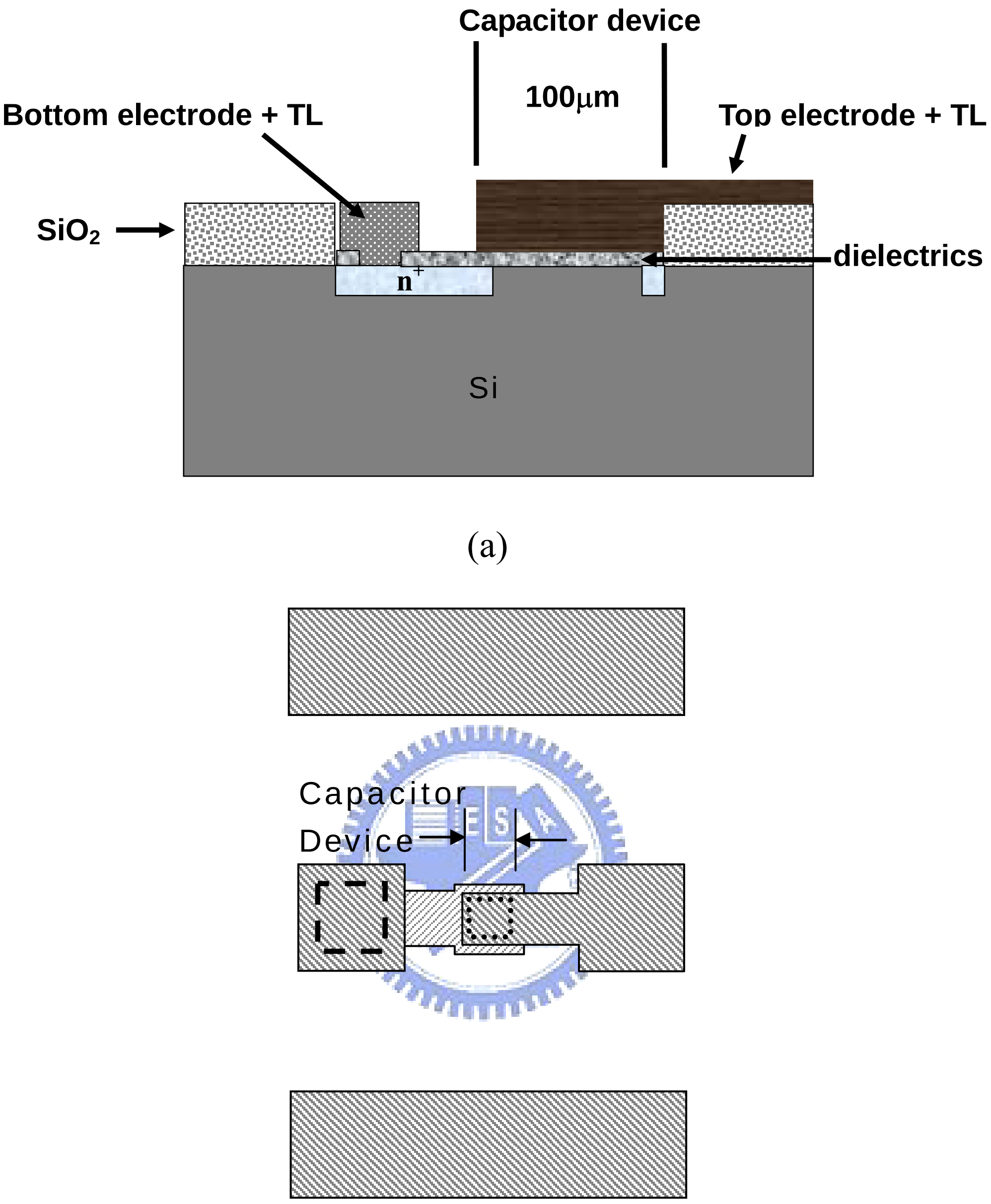


(a)



(b)

Fig. 3-1 The application of a program-erasable high-κ tunable capacitor for (a) VCO and (b) RF amplifier. The tuning memory of the device can greatly simply the VCO by eliminating an external voltage bias circuit and reducing the design turn-around time that may involve correcting the impedance mismatch in I/O LC networks of an RF amplifier.



(a)

(b)

Fig. 3-2 (a) Cross section and (b) top cell view of the RF AlN MIS capacitors.

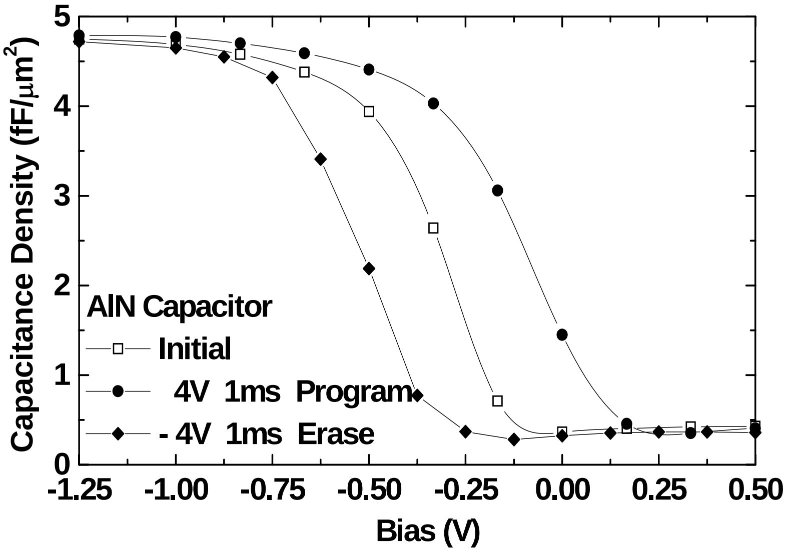


Fig. 3-3 Measured C-V characteristics of a high-κ AlN MIS capacitor. A large tuning range can be obtained in these high density capacitors using a high-κ gate dielectric. The shift of V_{FB} in the C-V curves is achieved by $+V_g$ and $-V_g$ for applied program and erase voltages, respectively.

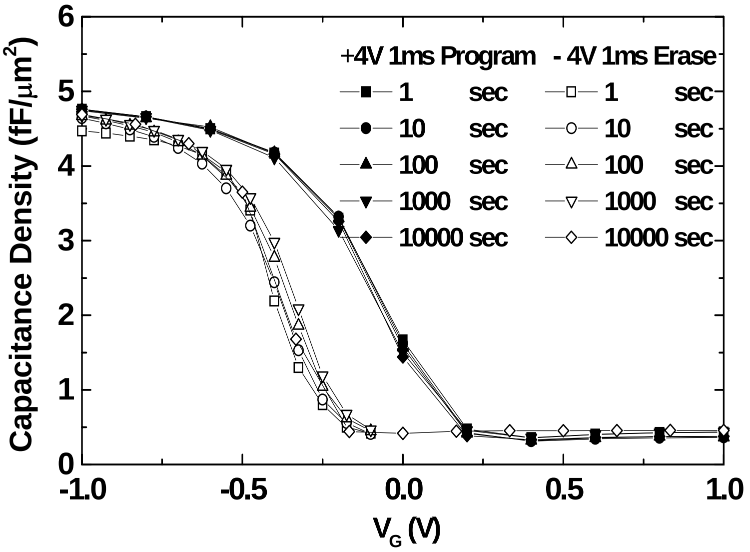


Fig. 3-4 The measured C-V characteristics of an AlN MIS capacitor after a + 4 V program or a -4 V erase for 1 ms. The retention property was obtained by measuring the C-V, after removing the program or erase voltage, for 10 s to 10,000 s.

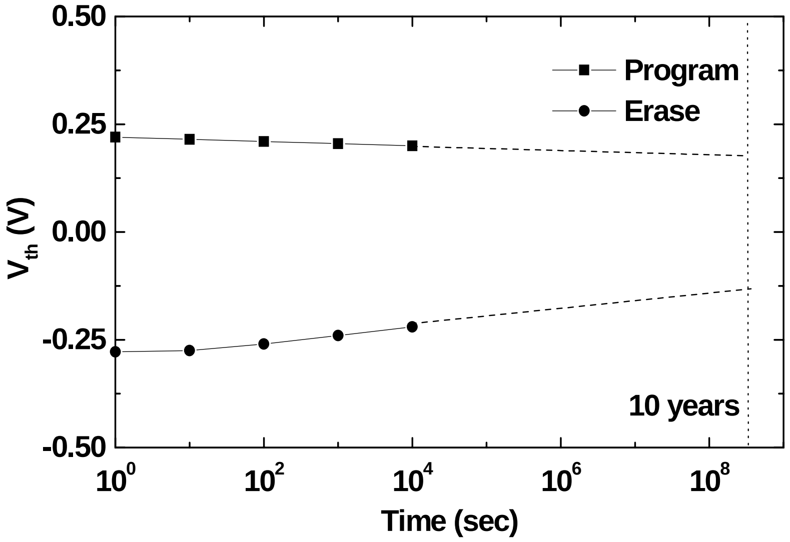


Fig. 3-5 The retention characteristics of + V_{th} and - V_{th} from the C-V curves in Fig. 4 for an AlN MIS capacitor programmed or erased at +4 V or -4 V for 1 ms. Excellent memory characteristics are shown, such as the small V_{th} variation and extrapolated long memory time.

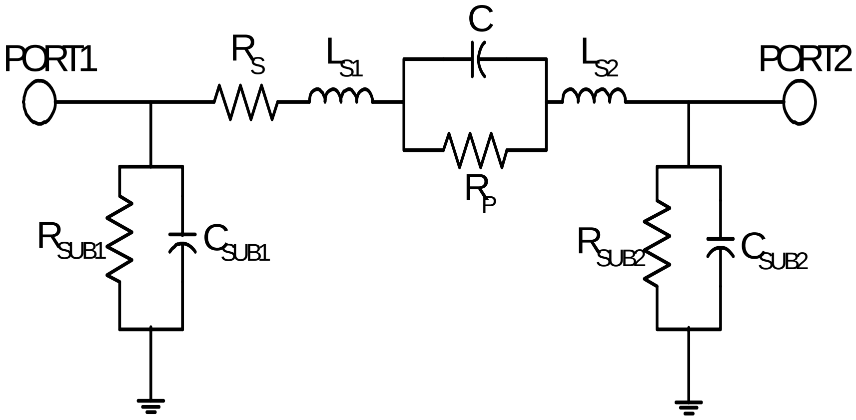


Fig. 3-6 The equivalent circuit model for an AlN capacitor simulation in the RF regime.

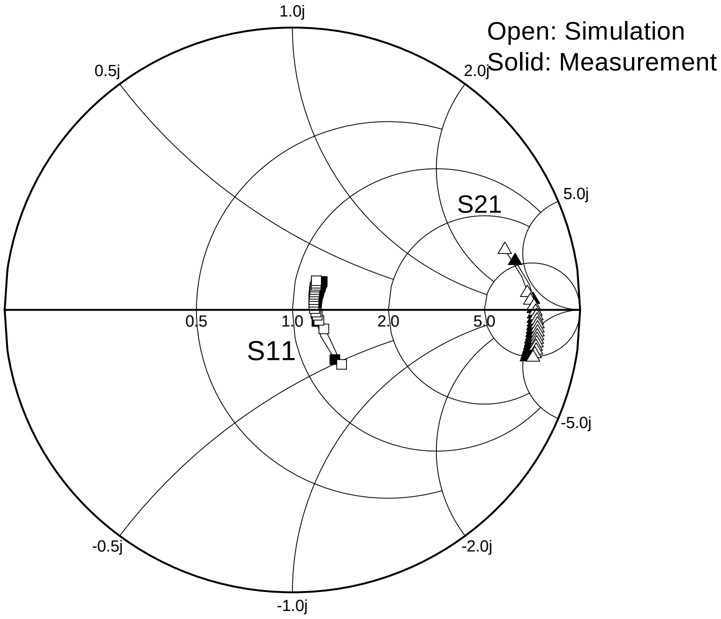


Fig. 3-7 The measured and simulated S-parameters of program-erasable AlN MIS capacitors.

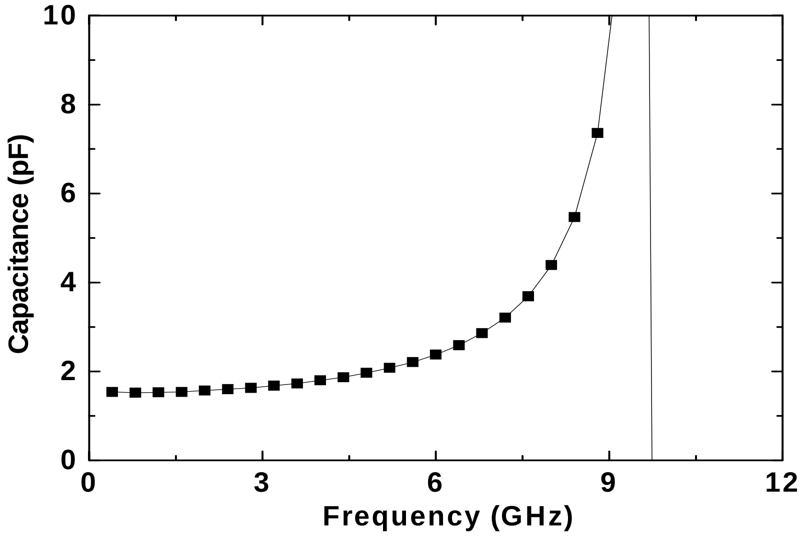


Fig. 3-8 The frequency-dependent capacitance for the program-erasable AlN MIS capacitor.

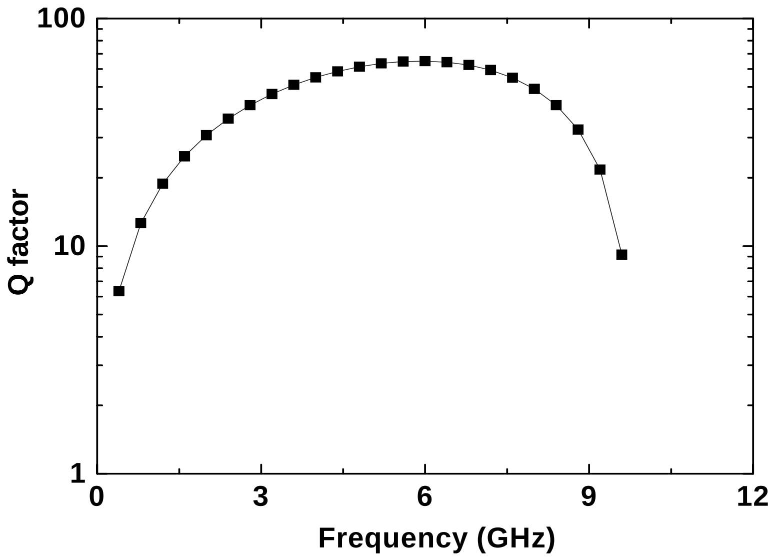


Fig. 3-9 The Q-factor of a 4.8 fF/μm^2 AlN MIS capacitor as a function of frequency.

Chapter 4

Novel SiO_2/AlN/HfAlO/IrO_x Memory with Fast Erase, Large ΔV_{th} and Good Retention

4.1 Introduction

Fundamental challenges for advanced non-volatile memory are the continuous down-scaling program/erase (P/E) time and operation voltage, while still maintaining good 10 years data retention [4.1]. Although the SOMOS/MONOS memory [4.1]-[4.8] provides a potential solution for down-scaling the gate oxide beyond conventional floating gate memory, further performance improvements with larger memory window (ΔV_{th}) of charge-tapping in nitride and faster erase time at low voltage and are required [4.1]-[4.8]. Of the known high-κ dielectrics, AlN has a better charge-trapping capability than Si_3N_4 and Al_2O_3 as well as unique P/E memory characteristics [4.9]-[4.12]. In this work, we report the memory performance of novel IrO_x-HfAlO-AlN-SiO_2-Si MONOS device. At ±13 V and fast 100 μs P/E, we found a large ΔV_{th} of 3.7 V that extrapolated to 1.9 V for 10-year retention at 85°C. The 85°C initial ΔV_{th} and 10-year retention window further increase to 5.5 V and 3.4 V for 1ms erase. Such fast P/E also gives large 10^5-cycled ΔV_{th} window due to small stress on tunnel SiO_2. The good retention is due to the strong Al-N ionic bond related higher trapping capability. The very fast 100 μs erase is owing to the high electric field (*E*) over tunnel SiO_2 from D ($\varepsilon_0\kappa E$) continuity of high-κ AlN (κ=10) trapping layer [4.9]-[4.12] and HfAlO (κ=17) barrier [4.13]-[4.14]. The low P/E voltage is from the efficient charge-trapping AlN, very high 3.5 fF/μm^2 capacitance density for charge storage, large electric field in SiO_2 and high workfunction Iridium oxide (IrO_x) metal gate [4.15]-[4.16] for low gate carrier injection during erase. These results are among the best reported data [4.4]-[4.7] summarized in Table 4-1.

4.2 Experimental

The IrO_x-HfAlO-AlN-SiO_2-Si MONOS memory devices were fabricated on a p-type Si wafer with resistivity of 5-10 Ω-cm. After a standard pre-gate clean, the 2.8 nm tunnel SiO_2 was formed by thermal oxidation at 850°C for 2 min, using diluted O_2. Then the 12 nm and 16nm AlN dielectric charge-trapping layers were formed by PVD, and a post- deposition RTA at 400°C for 1 min under N_2 ambient [4.9]-[4.12]. The high-κ HfAlO (Hf:Al=1:1) barrier layer [4.13]-[4.14], 13 nm thick, was deposited by Atomic Layer CVD and finally the 50 nm IrO_x [4.15]-[4.16] was deposited by PVD to form the MONOS structure. After standard lithography and gate patterning by RIE, a self-aligned arsenic (As^+) ion-implantation, followed by a 900°C and 30 sec RTA process, was used and to form the source-drain region. The resulting structure of the IrO_x-HfAlO-AlN-SiO_2-Si MONOS device is shown in Fig. 4-1. The fabricated devices were characterized by P/E measurements, as well as cycling and retention tests at 85°C using an HP4156A Semiconductor Parameter Analyzer and HP8110A 150 MHz Pulse Pattern Generator.

4.3 Results and discussion

A. P/E characteristics:

Fig. 4-2 shows the characteristics of leakage current for Ir and IrO_2 high-κ/metal gate PMOS [4.15]. The gate leakage current is one order of magnitude lower using IrO2 than Ir. Lower dielectric leakage current is most probably due to small metal diffusion in more thermal dynamic stable IrO_2 than pure Ir. In addition, the work function of IrO_2 is ~ 5.1 eV. Fig. 4-3 is the SIMS depth profiles of O and Ir in the IrO_x layer. The existence of oxygen in IrO_x layer is clearly shown. Fig. 4-4 shows the schematic band diagram of SiO_2/AlN/ HfAlO/IrO_x devices. The strong trapping AlN can reduce the P/E voltage even for thin AlN. The 5.1 eV high workfunction [4.15]-[4.16] is important to scale down the HfAlO thickness and erase voltage. This is evidenced from the 1 order of magnitude lower J_g in Fig. 4-5 than a previous report of a similar structure [4.6] also under -10 to -15 V erase operation. This is consistent with the>10X lower J_g in IrO_x/high-κ PMOS than mid-gap metal-gate device [4.15]-[4.16]. The C-V hysteresis curves, in Fig. 4-6, show very large ΔV_{th} shifts of 7-10 V. The capacitance further increases to 3.5 fF/μm^2 for 12 nm AlN MONOS to give large charge storage at low voltage. Figure 4-7 shows the I_d-V_g characteristics of 12 nm AlN MONOS device with 10 μm gate length. A large memory window of 2.3V to 3.7V was measured at fast 100 μs P/E voltages from ±12 V to ±13 V. The detailed P/E characteristics (time-dependence of ΔV_{th} from the peak g_m of the linear I_d-V_g) are shown in Fig. 4-8 for thicker 16 nm AlN MONOS. A fast P/E time of 100 μs-1 ms are measured at ±13 V, with a large ΔV_{th} shift. The ΔV_{th} and P/E speed are increased using the thinner 12 nm AlN MONOS. As shown in Figs. 4-9, the 13 V 100 μs program gives 3.3 V ΔV_{th} change and the -13 V 100 μs erase has -3.7 V ΔV_{th}. Even a ΔV_{th} shift of 2.1 V and -1.8 V is obtained at 10 μs and ±13 V P/E. Such very fast erase is ~10X better than published data [4.4]-[4.7] with larger ΔV_{th}. It arises from the higher electric field in thin 2.8 nm SiO_2 due to a smaller voltage drop in small EOT high-κ HfAlO (κ=17) barrier and trapping AlN (κ=10) from $\varepsilon_o \kappa E$ continuity. The high work-function IrO_x gate [4.15]-[4.16] also helps the erase by largely reducing charge injection from gate with thin HfAlO.

B. Retention and cycling:

Figs. 4-10, 4-11 and 4-12 show the retention characteristics. The 10-year retention ΔV_{th} is larger for 12 nm than and 16 nm AlN devices with only slightly faster decay rate. The extrapolated 10-year memory window at 25°C, for 12 nm AlN device, increases from 2.4 to 4.1 V with increasing erase time from 0.1 to 1 ms. Still a large

10-year window at 85°C of 1.9 or 3.4 V was obtained for 100 μs or 1 ms erase and 100 μs program at ±13 V. This is above the best reported data [4.4]-[4.7] in Table 4-1. Besides, the 85°C high- and low-level retention decay rate of 120 and only 64 mV/dec are comparable with published data [4.4]-[4.7], with added merit of the largest initial ΔV_{th} of 5.5 V (3.7 V) at 1ms (0.1 ms) -13 V erase. This large memory window is arose form the strong Al-N ionic bond to give better trapping capability than Al_2O_3 and Si_3N_4 [4.9]-[4.12]. Good endurance is also obtained in Figs. 4-13 and 4-14. At 85°C and ±13 V, big 10^5-cycled memory window of 2.9 or 4.6 V and 10 k-cycled 10-year retention window of 1.6 or 2.7 V are obtained at 0.1 ms or 1 ms erase. Such excellent endurance is due to the fast P/E time with less stress to tunnel SiO_2. Table 4-1 summarizes the important memory data. At 85°C and ±13 V P/E, good memory integrity of fast 100 to 1000 μs erase time, large ΔV_{th} of 3.7 or 5.5 V, big 10^5-cycled ΔV_{th} of 2.9 or 4.6 V, and good retention of large 10-year memory window of 1.9 or 3.4 V are obtained at the same time in this MONOS device.

4.4 Conclusion

We have demonstrated a novel AlN MONOS memory device which uses the IrO_x metal gate and shows a large initial memory window of 3.7 V at ±13 V and 100 μs P/E, 1.9 V extrapolated ΔV_{th} for 10-year data retention and the 10% ΔV_{th} degradation after 10^4 P/E cycles at 85°C.

	P/E condition for retention & cycling	Initial ΔV_{th} (V) @85^{o}C	10-year retention @85^{o}C	85^{o}C-P/E decay rate (mV/dec)	ΔV_{th} @Cycles 85^{o}C
This Work	**13V 100μs/ -13V 100μs**	**3.7**	**1.9**	**120 / 52**	**2.9 @ 10^{5}**
	13V 100μs/ -13V 1ms	**5.5**	**3.4**	**120 / 64**	**4.6 @ 10^{5}**
Tri-gate [4.4] $SiO_2/Si_3N_4/$ SiO_2/poly	11.5V 3ms/ -11.5V100ms	1.2	1.1 (25^{o}C only)	12.5 /12.5 (25^{o}C only)	1.5 @ 10^{4} (25^{o}C only)
FinFET [4.5] $SiO_2/Si_3N_4/$ SiO_2	13V 10μs/ -12V 1ms	5	2.9	60 / 150	4.2 @ 10^{4}
$SiO2/Si_3N_4/$ Al_2O_3/TaN [4.6]	13.5V100μs/ -13V 10ms	4.4	2.07	140 / 75	4 @ 10^{5}
$SiO_2/Al_2O3/$ SiO_2/poly [4.7]	9V >1ms/ no data	0.9	0.9	No charge loss	No data

Table 4-1 Comparisons of P/E speed, ΔV_{th} window (extrapolated for 85^{o}C 10-years retention), retention decay rate and endurance.

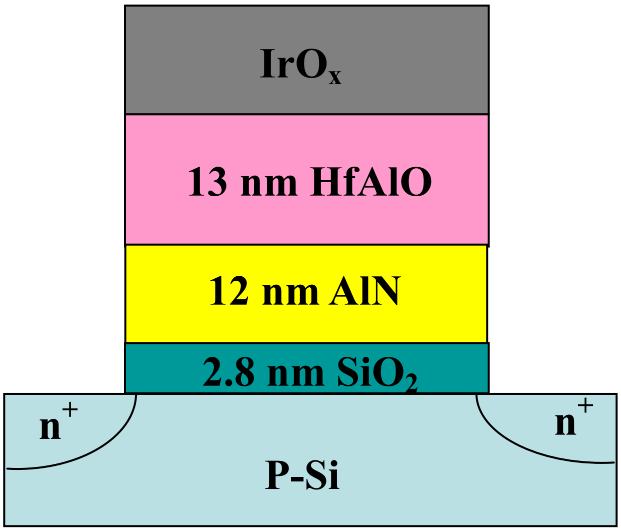
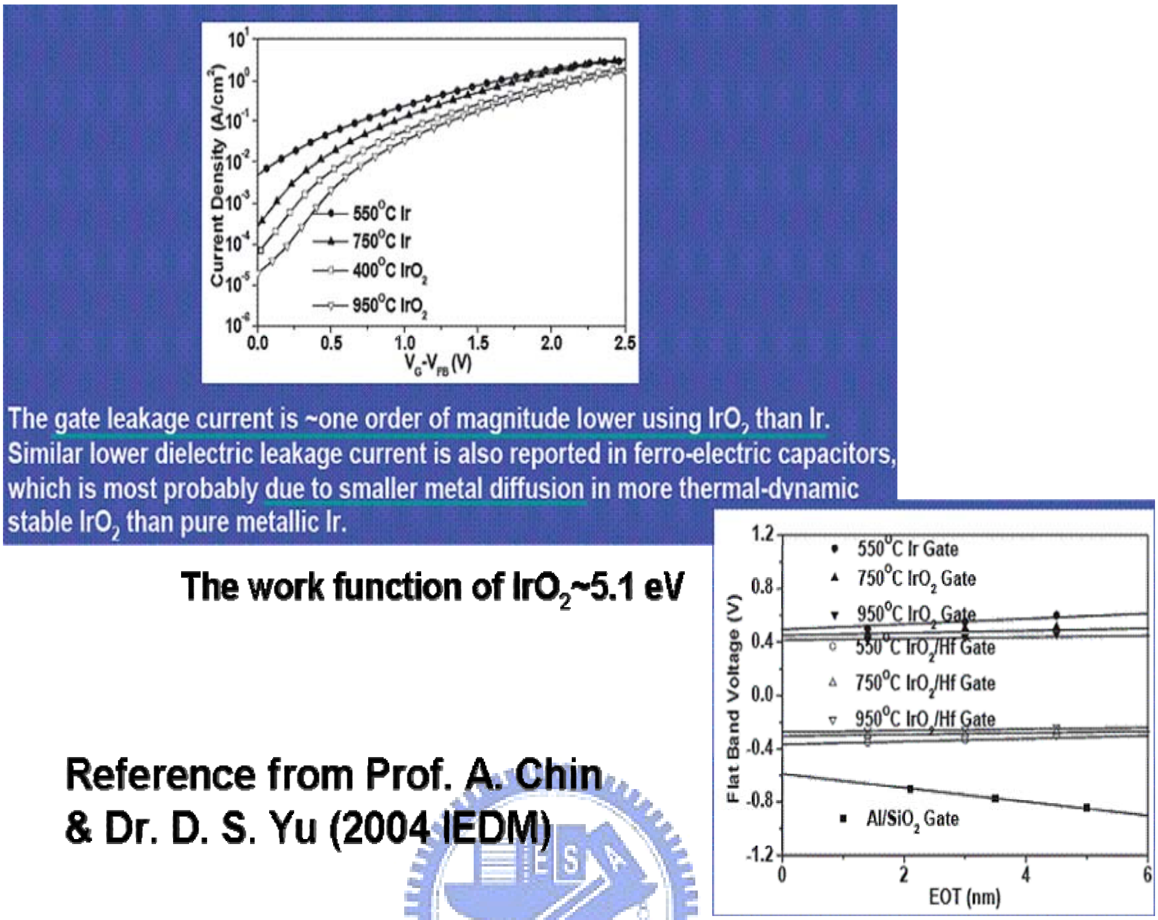


Fig. 4-1 The cross-section view of Si/SiO_2/AlN/HfAlO/IrO_x MONOS memory device.



The gate leakage current is ~one order of magnitude lower using IrO$_2$ than Ir. Similar lower dielectric leakage current is also reported in ferro-electric capacitors, which is most probably due to smaller metal diffusion in more thermal-dynamic stable IrO$_2$ than pure metallic Ir.

The work function of IrO$_2$~5.1 eV

Reference from Prof. A. Chin & Dr. D. S. Yu (2004 IEDM)

Fig. 4-2 The J-V characteristics of Ir/IrO$_2$ high-κ metal gate PMOS.

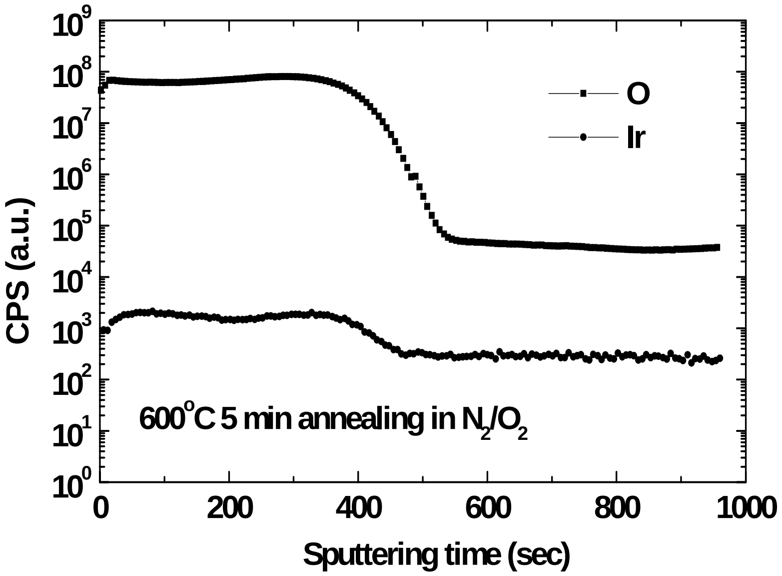


Fig. 4-3 The SIMS measurement of IrO_x film.

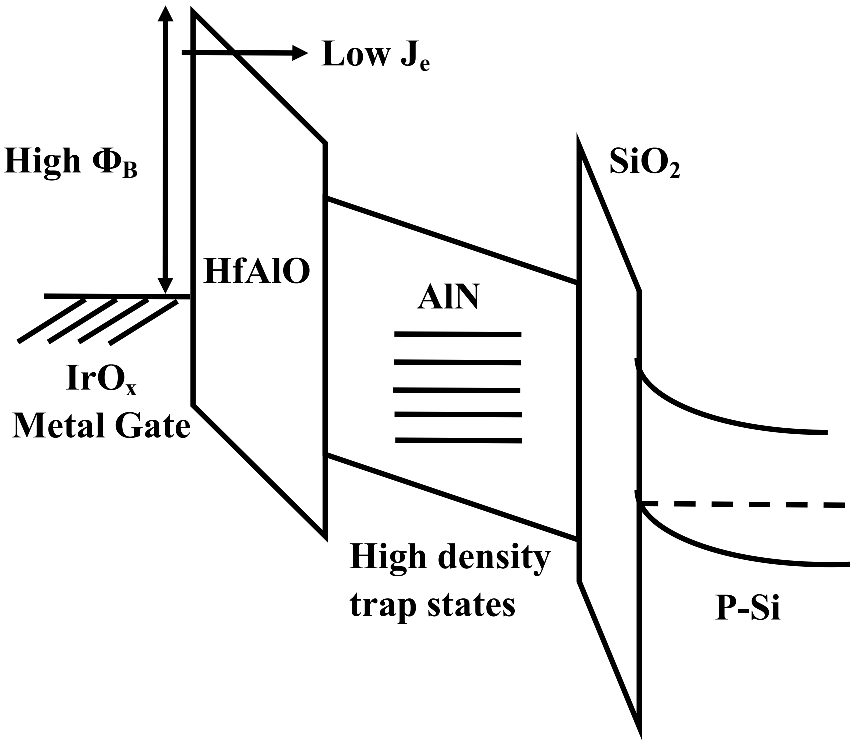


Fig. 4-4 The band diagram of an IrO_x-HfAlO-AlN-SiO_2-Si MONOS device in the erase state. The AlN has a strong trapping capability and the high work-function IrO_x metal gate decreases the charge injection into the thin HfAlO blocking layer.

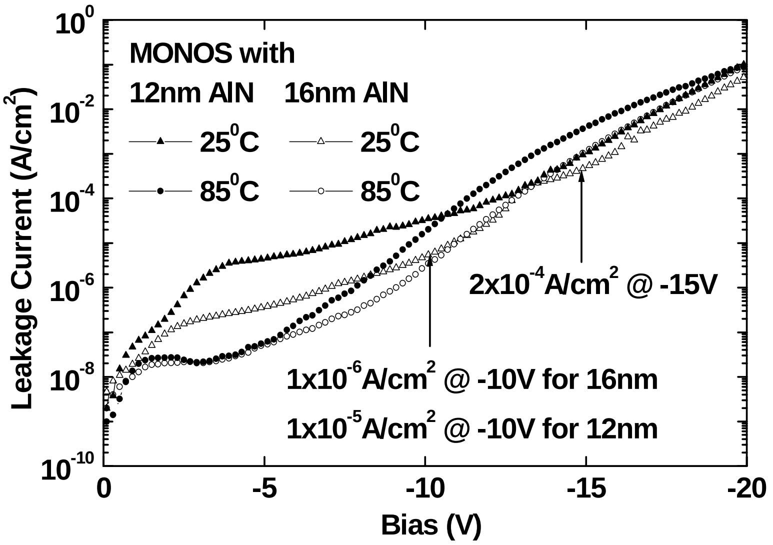


Fig. 4-5 J_g-V_g curves of MONOS memory with 12 nm and 16 nm AlN at 25 and 85^{o}C. The J_g is 1 order of magnitude lower than the data from [4.6] due to higher work function of IrO_x.

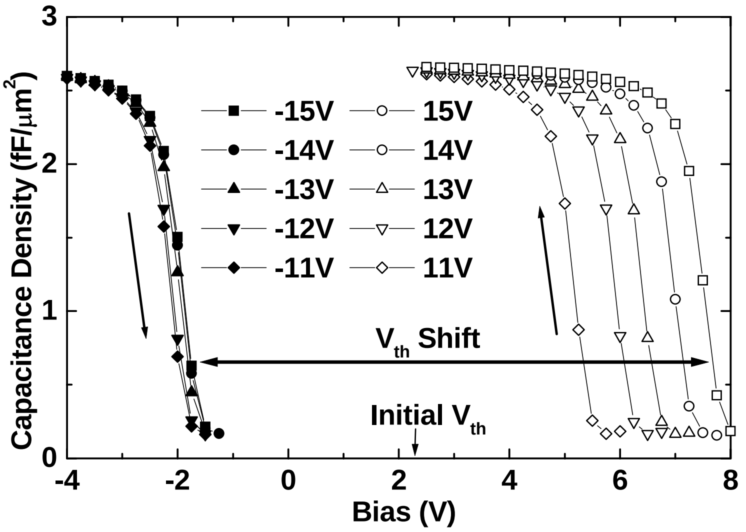


Fig. 4-6 C-V hysteresis curves of MONOS capacitor with 16 nm AlN for various V_g. The capacitance density increases to 3.5 fF/μm^2 for 12 nm AlN device.

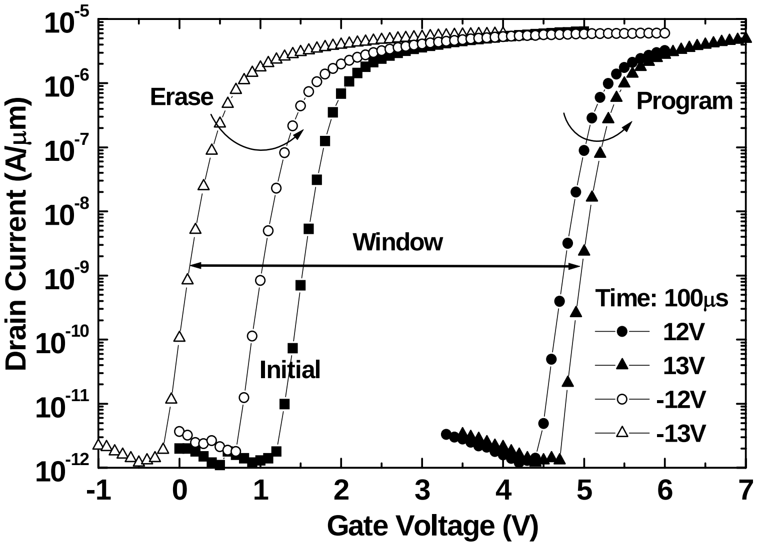
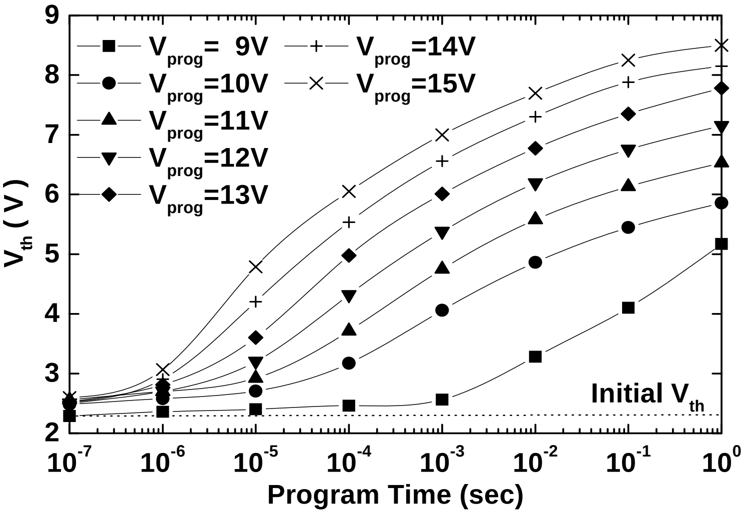
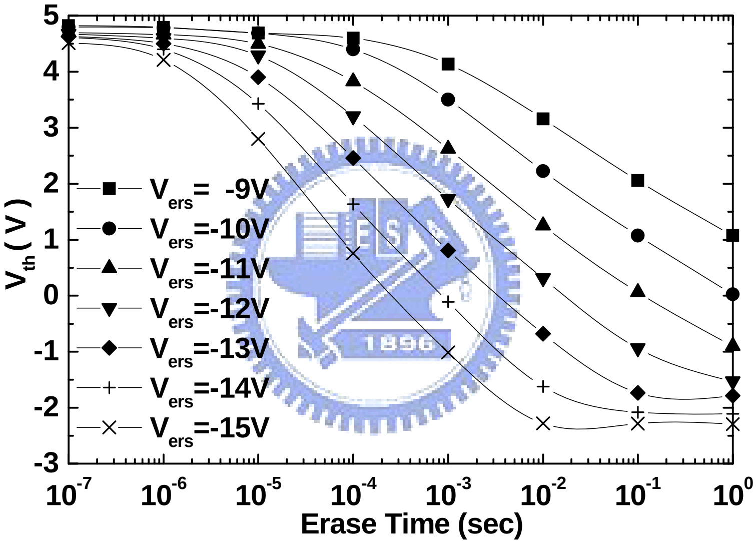


Fig. 4-7 The measured I_d-V_g characteristics of IrO_x-HfAlO-12 nm AlN-SiO_2-Si MONOS device.

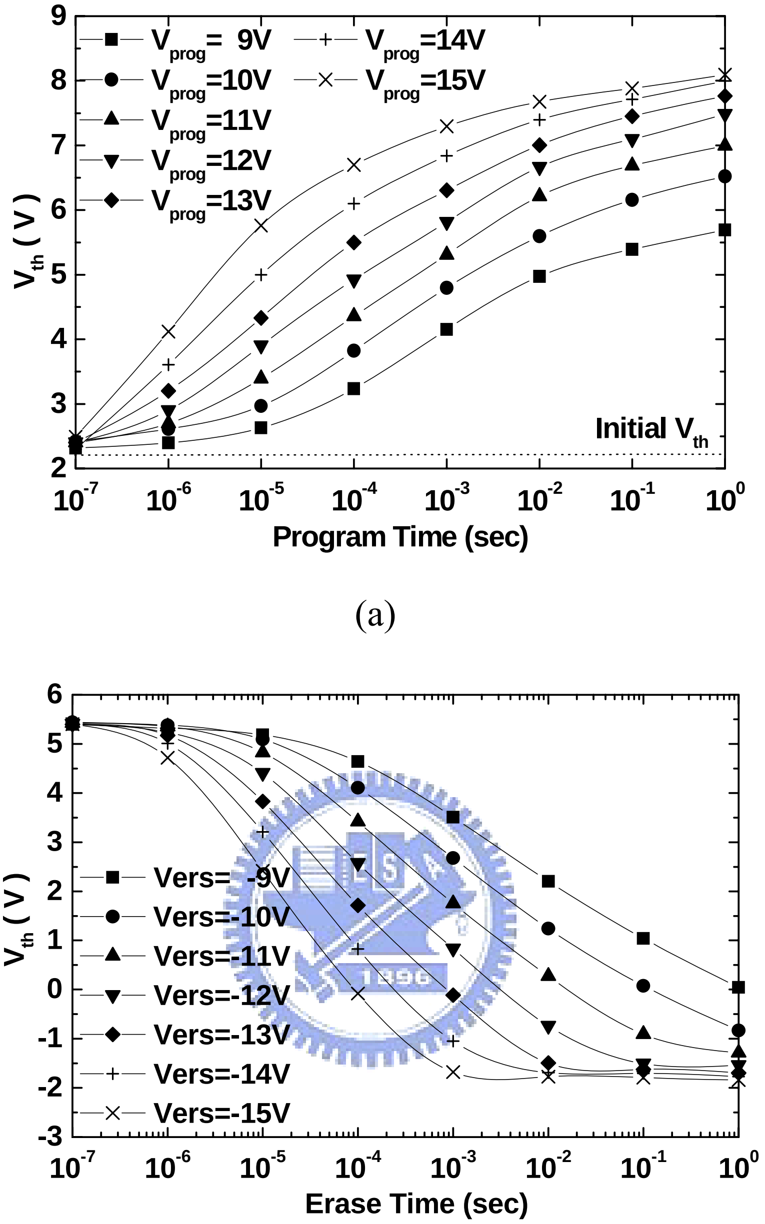


(a)



(b)

Fig. 4-8 The measured (a) program and (b) erase characteristics from I_d-V_g for 16 nm AlN MONOS devices 10 μm gate length. The device was initially programmed at 13 V for 100 μs.



(a)

(b)

Fig. 4-9 The measured (a) program and (b) erase characteristics from I_d-V_g for 12 nm AlN MONOS devices 10 μm gate length. The device was initially programmed at 13 V for 100 μs.

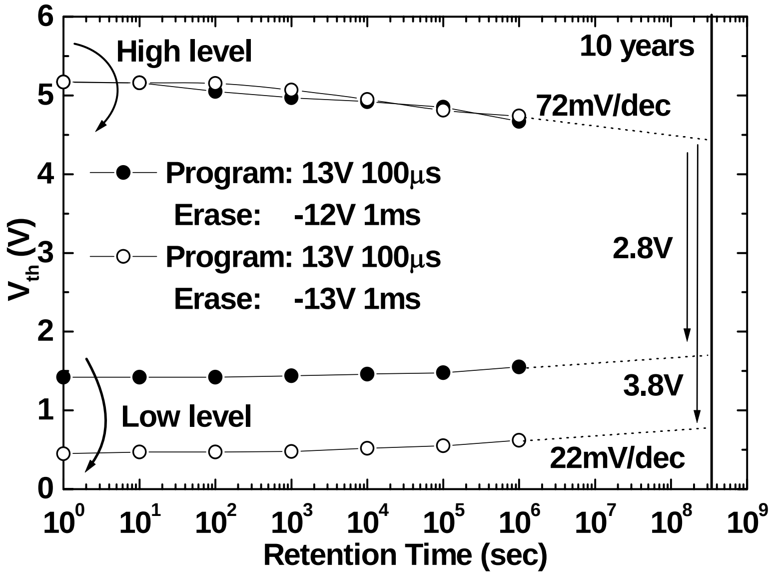


Fig. 4-10 Retention of MONOS devices with 16 nm AlN at 25°C. The P/E decay rates are only 72/22 mV/dec.

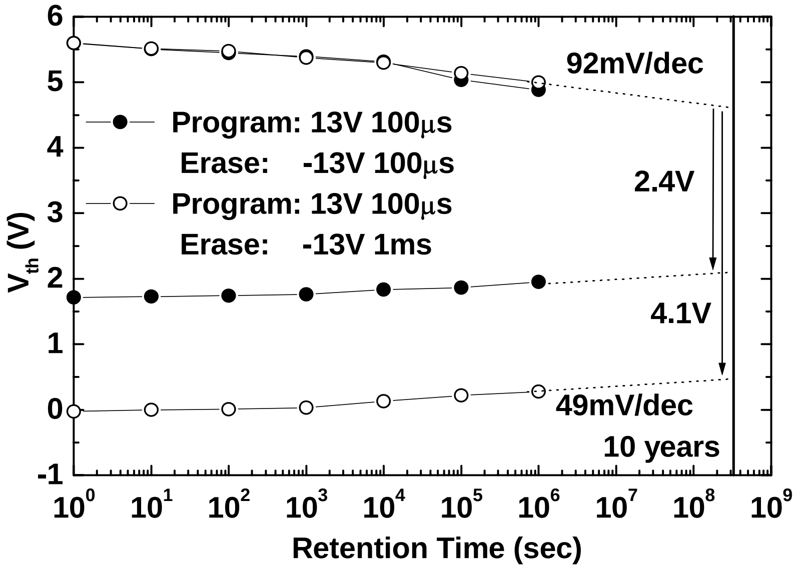


Fig. 4-11 Retention of MONOS devices with 12nm AlN at 25°C. The P/E decay rates are 92/49 mV/dec.

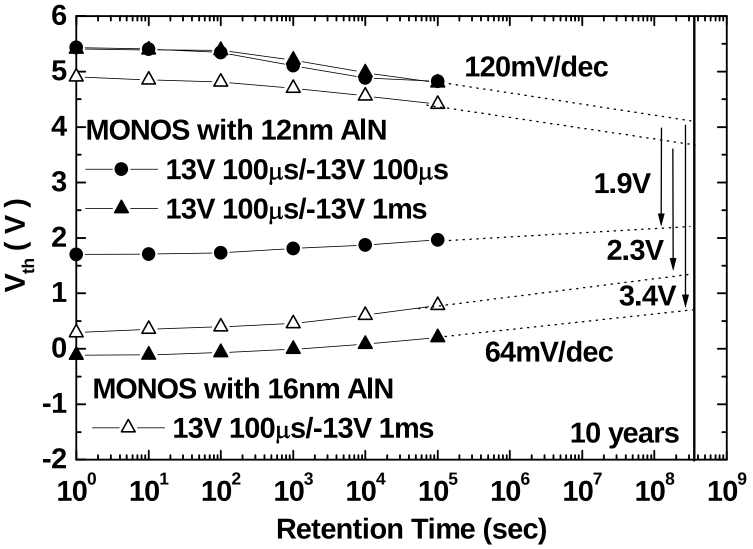
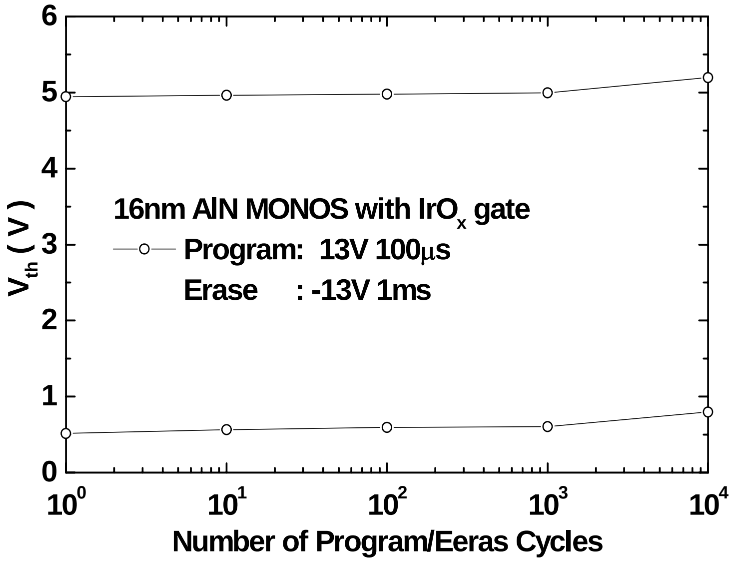
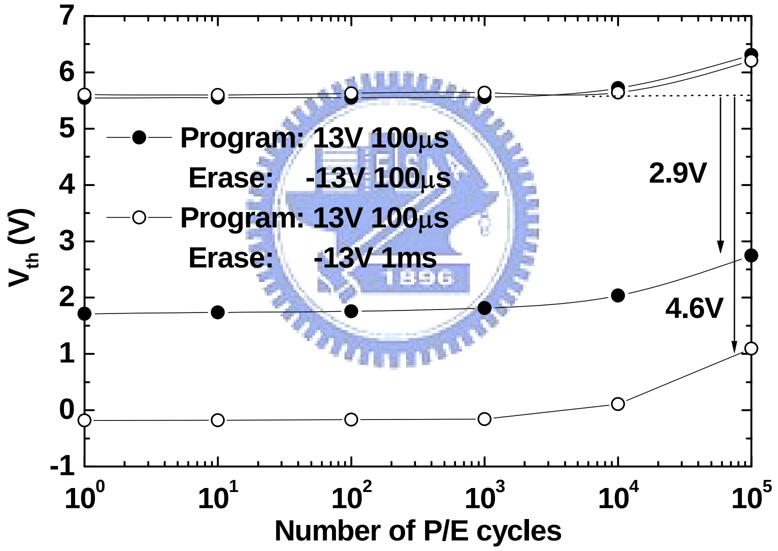


Fig. 4-12 Retention of MONOS devices with 12 nm and 16 nm AlN at 85°C. The P/E decay rates are 120/64 mV/dec.

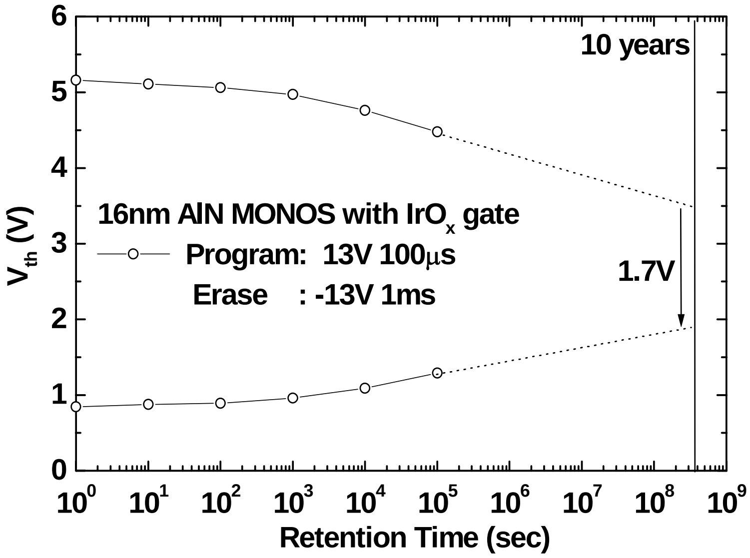


(a)

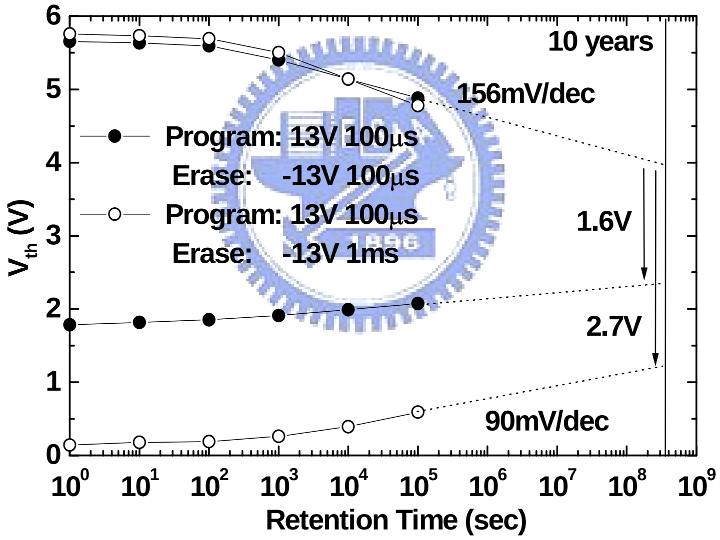


(b)

Fig. 4-13 Endurance of MONOS memory with (a) 16 nm and (b) 12 nm AlN at 85°C. High ΔV_{th} can be maintain up to 10^4 or 10^5 P/E.



(a)



(a)

Fig. 4-14 Retention of 10 k P/E-cycled MONOS devices with (a) 16 nm and (b) 12 nm AlN at 85°C. Large ΔV_{th} of 1.6 and 2.7 V are still obtained in 12 nm AlN MONOS device.

Chapter 5

Very Low Voltage SiO$_2$/HfON/HfAlO/TaN Memory with Fast Speed and Good Retention

5.1 Introduction

According to ITRS roadmap, the SONOS non-volatile memory (NVM) will continue down-scaling program/erase (P/E) voltage to 4.0-4.5 V with faster speed while maintaining good retention [5.1]-[5.10]. Such low voltage operation is also important for embedded SoC application. In chapter 4, we showed [metal-gate]-[high-κ]-AlN-SiO$_2$-Si MONOS devices to operate at 13 V with fast 100 µs~1 ms P/E and good 10-year extrapolated retention at 85^{o}C [5.3]. In this chapter, we further develop the MONOS structured memory by using novel HfON trapping layer [5.11]-[5.13] to form the TaN-HfAlO-HfON-SiO$_2$-Si MONOS and operate at only P/E voltage of 8 V (between gate and channel) under faster 10 µs~ 100 µs P/E with good extrapolated 10-year retention of 1.0 V even at 125^{o}C. Using a simple voltage inverter circuit, the P/E voltage can further be reduced to nearly half: by applying 4.5 V and -3.5 V for the same ±8 V gate-channel bias. This is useful for embedded SoC under a single 5 V voltage source. Such low P/E voltage is achieved by using novel HfON trapping layer with very high-κ value (κ~22) beyond previous AlN (κ=10) [5.3] or

Si_3N_4 (κ=7), in addition to use the same high-κ blocking oxide of HfAlO (κ=17) [5.3], [5.14]-[5.16]. This is evident from the higher gate capacitance density of 4 fF/μm^2. The very low P/E voltage is due to the small voltage drop in high-κ trapping HfON and blocking HfAlO to give high electric field over the thin tunnel oxide. The high field in tunnel oxide also in turn gives fast P/E speed. The good 125°C retention is due to the deep E_{vac}-E_c energy (χ) of HfON similar to Al(Ga)N [5.17], even at low ±8 V fast 100 μs P/E speed using thin tunnel SiO_2. These results compare well with reported data [5.3]-[5.6] in Table 5-1, with added merits of much lower P/E voltage for embedded SoC, faster speed and using existing dielectric materials available in IC fabs.

5.2 Experimental

The TaN-HfAlO-HfON-SiO_2-Si MONOS memory devices were fabricated on a p-type Si wafer with resistivity of 5-10 Ω-cm. After a standard pre-gate clean, the 2.8 nm thermal SiO_2 was grown as the tunnel oxide at 850°C for 2 min under diluted O_2 condition. Then 10 nm HfON dielectric charge trapping layer was formed by Hf sputtering using mixed Ar/N_2/O_2 ambient (Ar/N_2/O_2=20:5:5 sccm) at 3 mTorr pressure, followed by post-deposition anneal (PDA) process at 650°C for 30 sec in N_2 environment by RTA. The formed HfON was further characterized by secondary ion-mass spectroscopy (SIMS) and x-ray photoelectron spectra (XPS). The high-κ

HfAlO (Hf:Al=1:1) barrier layer of 12 nm thick was deposited by similar reactive co-sputter of Hf and Al targets under mixed Ar/O_2 (Ar/O_2=25:5 sccm). A 650°C and 30 sec in N_2 PDA process was also applied after HfAlO deposition. Then 100 nm TaN metal gate was deposited by sputter to form the MONOS structure. After standard lithography and gate patterning by reactive ion etching (RIE), the self-aligned arsenic (As^+) ion-implantation and followed 900°C/30 sec RTA were applied to form the source-drain (S/D) region. The resulting structure is shown in Fig. 5-1. The fabricated MONOS devices were characterized by P/E measurements, as well as cycling and retention tests at 85°C and 125°C using an HP4156A Semiconductor Parameter Analyzer and HP8110A 150MHz Pulse Pattern Generator.

5.3 Results and discussion

A. HfON characterization and band diagrams of MONOS devices

Fig. 5-2 indicates SIMS depth profiles of oxygen and nitrogen in the HfON and control HfO_2 layers. The existence of nitrogen in HfON layer is clearly shown. The additional nitrogen incorporation is beneficial for improved high temperature thermal stability [5.11]-[5.13]. Besides, the nitrogen in HfON may increase the trapping capability similar to AlN [5.3] and Si_3N_4 cases, which are much better than their oxide counterparts of Al_2O_3 and SiO_2.

Fig. 5-3 shows the X-ray photoelectron survey spectra of the HfON film. It is clearly shown that all the features of the X-ray photoelectron peaks are almost identical to the spectrum of the HfON bulk power, indicating the formation of HfON film. There are 5.8% nitrogen and 55.6% oxygen in the HfON dielectric film deposited by PVD. Figs. 5-4(a) and 5-4(b) show Hf_{4f} and N_{1s} XPS spectra respectively, for HfON and control HfO_2 dielectrics. There are two peaks in Hf_{4f} spectra according to spin-orbit splitting into $Hf_{4f5/2}$ and $Hf_{4f7/2}$. In the HfO_2, the binding energies of $Hf_{4f5/2}$ and $Hf_{4f7/2}$ were located at 18.8 eV and 17.4 eV, respectively. An obvious peak shift of 0.58 eV in the HfON to HfO_2 is observed, where the lower energy implies the presence of Hf-N bonds in the HfON after PDA process. In addition, the HfO_2 dielectric showed no peaks for N_{1s}, while the HfON showed noticeable high intensity at binding energy of 397.8 eV.

Since the HfN is known to be metallic, the HfON may have smaller energy bandgap (E_G) than HfO_2. This is shown in the schematic band diagrams of TaN-HfAlO-[high-κ/HfON]-SiO_2-Si MONOS structure of Fig. 5-5(a), according to published data [5.18]. The better trapping capability and possibly small energy bandgap in HfON than HfO_2 [5.11]-[5.13] can give larger memory window and maintain long time data retention even using thin tunnel oxide. In addition, the larger E_{vac}-E_c energy (χ) of 2.6 eV for HfON also gives better retention than traditional

Si_3N_4 (1.7 eV) and AlN (1.82 eV) [5.3]. Moreover, the HfON has higher κ than Si_3N_4 (κ=7) and AlN (κ=10) that can lower the P/E voltage. The using high-κ blocking HfAlO (κ=17) rather than conventional SiO_2-Si_3N_4-SiO_2 (ONO) further reduces the P/E voltage. The TaN metal gate is also important for better erase function. As shown in the energy band diagram of MONOS under erase state (Fig. 5-5(b)), the TaN metal gate provided a 4.65 eV high work-function by Fermi-level pinning to high-κ than self-aligned n^+-poly gate (4.1 eV), which can reduce the electrons injection from the gate and allows the thickness of the HfAlO barrier to be scaled down.

Fig. 5-6 shows the C-V hysteresis curves. Large V_{FB} shift is obtained at low P/E voltage. The high gate capacitance density of 4 $fF/\mu m^2$ is better than IrO_2-HfAlO-AlN-SiO_2-Si MONOS device [5.3] due to the higher κ of 22 in HfON than 10 in AlN. Fig. 5-7 shows the gate leakage current (J_g) of TaN-HfAlO-HfON-SiO_2-Si MONOS device during erase measured from 25 to 125 °C. At -8 V erase condition, a low leakage current of 5×10^{-5} A/cm^2 is measured at 25°C, which increases slightly to 3×10^{-4} A/cm^2 at 125°C. These low measured leakage currents, from using high work function TaN gate, are important to prevent electron injection from gate into trapping layer during erase.

B. Program and erase characteristics

Fig. 5-8 shows the I_d-V_g curves of TaN-HfAlO-HfON-SiO_2-Si MONOS device with 5 μm gate length. A large memory window of 2.5V was measured under rapid 100 μs at ±8 V P/E voltages. The detail program and erase transients (time-depended threshold voltages from the peak g_m of the linear I_d-$V_{g,}$) are shown in Figs. 5-9(a) and 5-9(b), respectively. The V_{th} increases monotonically with increasing program time and decreases with increasing erase time. In programming, the V_{th} starts to shift from 10 μs at 7-9 V gate pulse. The V_{th} even changes from 1 μs at very low -6 V gate pulse after initial program for the erase operation. The MONOS memory device shows extremely high program/erase speed. We can get a threshold voltage shift of 1.4 V at 100 μs and 8 V for program operation and -2.5 V shift at 100 μs and -8 V for erase (2.5 V initial memory window is measured under fast 100 μs and low ±8 V P/E voltage). Such fast high P/E speed at low operation voltage is due to the high electric field (E) in the thin 2.8 nm SiO_2 tunnel layer, which is originated from the small voltage drop in high-κ HfAlO and HfON by $\varepsilon_o \kappa E$ continuity. The fast erase is also attributed to the high work-function TaN gate (4.65 eV) that reduces the charge injection through the thin HfAlO blocking oxide [5.3]. The large ΔV_{th} under fast 100 μs and low ±8 V P/E voltage indicates the efficient charge trapping in HfON that is related to the deeper trapping energy than Si_3N_4. The large erase ΔV_{th} is due to the hole injection from accumulation region of Si body. From T-Supreme & Medici

(TMA) analysis (the simulation is shown in Fig. 5-10 and parameters in Table 5-2), the measured erase J-V current at low voltage is mainly from hole current rather than gate electron current [5.17], which is due to the high work-function TaN (4.7eV) than n^+-Si (4.1 eV). This efficient and fast erase by hole injection is a special merit for MONOS device using thin tunnel oxide.

For integrated logic and memory SoC application, it is desirable to reduce the P/E voltage under a simple 5 V supply voltage. We have designed a simple voltage inverter circuit in Fig. 5-11 (a) that can generate a -3.5 V from a 4.5 V voltage source which is shown in Fig. 5-11 (b). Therefore, the P/E voltage of 8 V can be further reduced to nearly half by applying 4.5 V and -3.5 V for the same gate-body bias. Such low P/E voltage can improve the die area and energy efficiency beyond the using high voltage charge pumping circuit.

C. Retention and cycling

A good non-volatile memory device requires withstanding P/E operation up to 10^4-10^5 cycles with good 10-years memory retention at evaluated temperatures [5.1]. Figure 5-12 shows the P/E endurance characteristics of metal-gate/high-κ MONOS device with HfON trapping layer. Under ±8 V and 100 μs P/E condition, an initial memory window 2.5 V is obtained that can be maintained after 10 k P/E cycles with only 12% degradation. Such good endurance is due to the fast P/E time of 100 μs which gives less stress in the 2.8 nm thin tunnel oxide. From the increasing V_{th} after P/E cycling, the dominant degradation mechanism is due to the electron trapping. However, such electron trapping did not result in a closed memory window by charge loss.

Figs. 5-13(a) and 5-13(b) show the retention behavior of the Flash MONOS device. The fresh device exhibits a good extrapolated 10-years memory window of 1.45 and 1.0 V at 85 and 125^{o}C respectively, under ±8 V 100 μs P/E operation. The memory window decay rate from initial 2.5 V to 1.45 V at 10-years is 42% at 85^{o}C, that is comparable with or better than published data [5.3]-[5.6] summarized in Table 5-1. The 10-years retention memory window decreased slightly to 1.3 V after 1k cycling with increasing decay rate to 48% (shown in Fig. 5-14). Such good retention behavior is due to the deep trapping level in HfON shown in Fig. 5-15 and the small stress on the tunnel oxide by fast 100 μs switching speed. The metal-gate/high-κ HfON trapping MONOS device shows a very fast P/E speed of 100 μs, very low 8 V operation, a good 10-years retention memory window of 1.45 V (or 42% decay) at 85^{o}C and good endurance characteristics of 2.2 V memory window after 10 k cycling. These excellent memory device performances integrities are comparable well with best published data shown in Table 5-1, which are due to the high-κ HfON with deep trapping, low voltage drop high-κ HfAlO barrier, high work-function TaN metal gate and thinner 2.8 nm tunnel oxide.

5.4 Conclusion

We have demonstrated a novel TaN-HfAlO-HfON-SiO_2-Si MONOS memory device which shows a large initial memory window of 2.5V at ±8V and fast 100μs P/E. 1.45V extrapolated ΔV_{th} for 10-year data retention was measured at 85°C, which further gives good 1.0V 10-year memory window even at 125°C. In addition, the only 12% ΔV_{th} degradation was obtained after 10^3 P/E cycles. Using a simple voltage inverter circuit, the P/E voltage can further be reduced to nearly half: by applying 4.5 V and -3.5 V for the same ±8 V gate-channel bias. This is useful for embedded SoC under a single 5 V voltage source.

	P/E condition for retention & cycling	Initial ΔV_{th} (V)	10-year retention @85^{o}C	85^{o}C-decay rate	ΔV_{th} @Cycles
This Work	**8V 100μs/ -8V 100μs**	**2.5**	**1.45**	**42%**	**2.1@ 10^5**
SiO_2/AlN/ HfAlO/IrO_x [5.3]	13V 100μs/ -13V 100μs	3.7	1.9	48%	2.9 @ 10^5
SiO_2/Si-NC/ SiO_2 [5.4]	14V 10ms/ -14V 100ms	4	3.5	12.5%	4.5 @ 10^5
Tri-gate SiO_2/Si_3N_4/ SiO_2 [5.5]	11.5V 3ms/ -11.5V 100ms	1.2	1.1 (@25^{o}C)	8.3% (@25^{o}C)	1.5 @ 10^4
FinFET SiO_2/Si_3N_4/ SiO_2 [5.6]	13V 10μs/ -12V 1ms	4.5	2.4	47%	3.5 @ 10^4

Table 5-1 Comparisons of P/E condition, ΔV_{th} and reliability of TaN-HfAlO-HfON-SiO_2-Si MONOS memory with published data.

	Thickness (nm)	Work-function (eV)	Band gap (eV)	k-value
TaN	**150**	**4.65**	／	／
HfAlO	**12**	／	**5.9**	**17**
HfON	**10**	／	**5.6**	**22**
SiO_2	**2.8**	／	**9**	**3.9**

Table 5-2 The device parameters used for TMA simulation.

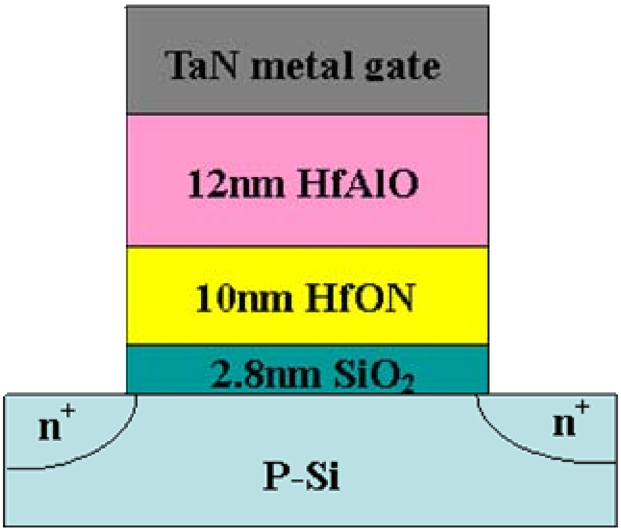


Fig. 5-1 The structure of TaN-HfAlO-HfON-SiO_2-Si MONOS memory device.

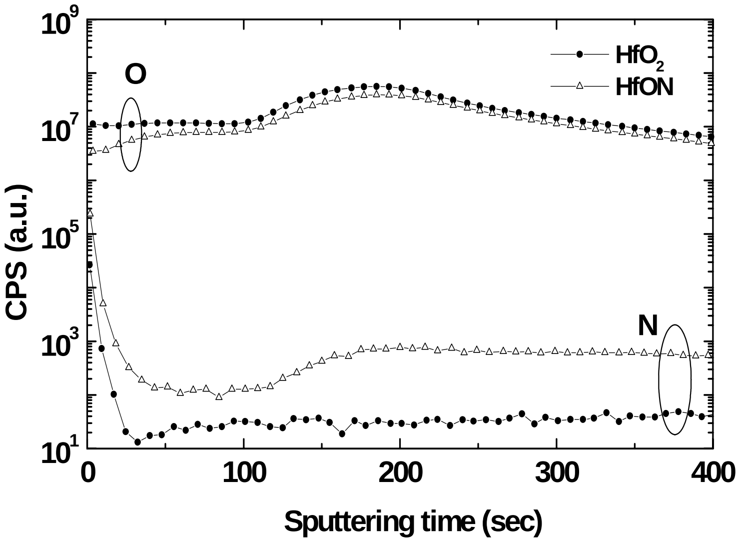


Fig. 5-2 The SIMS profiles of oxygen and nitrogen in the HfO_2 and HfON layers.

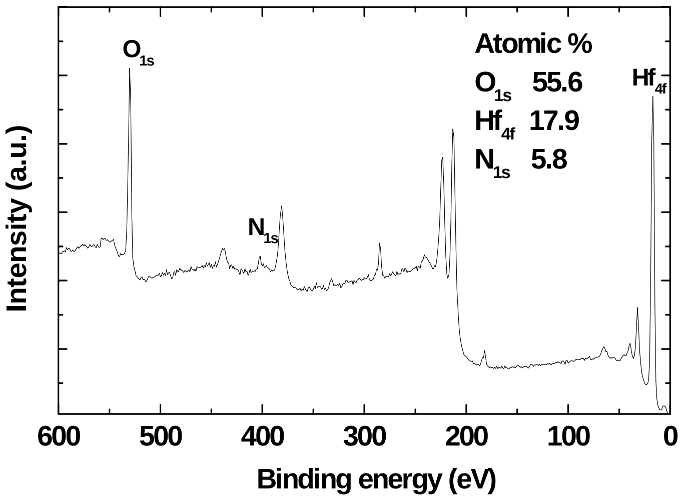
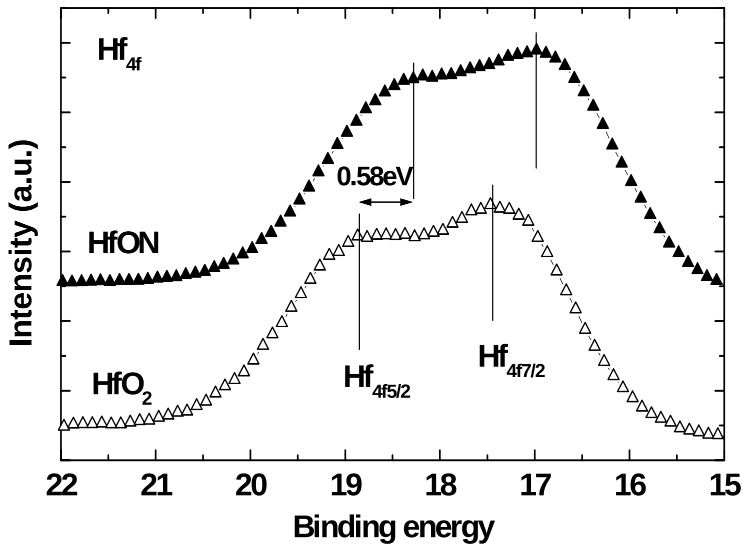
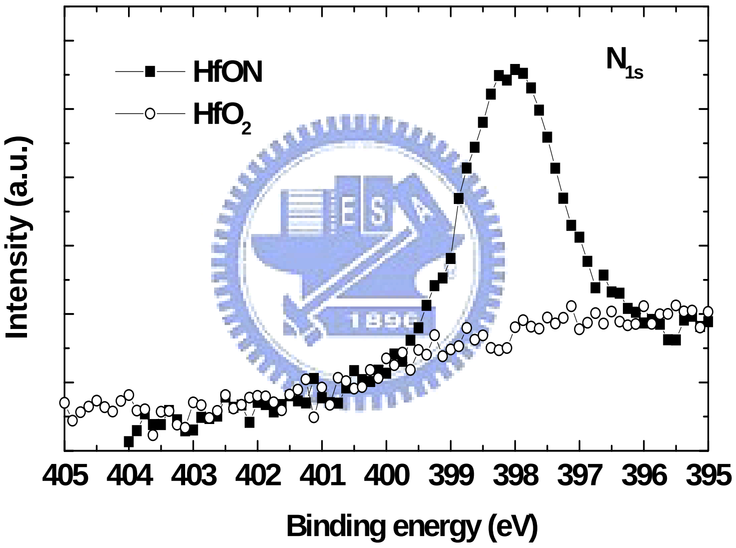


Fig. 5-3 X-ray photoelectron survey spectra of the HfON high-κ dielectric.

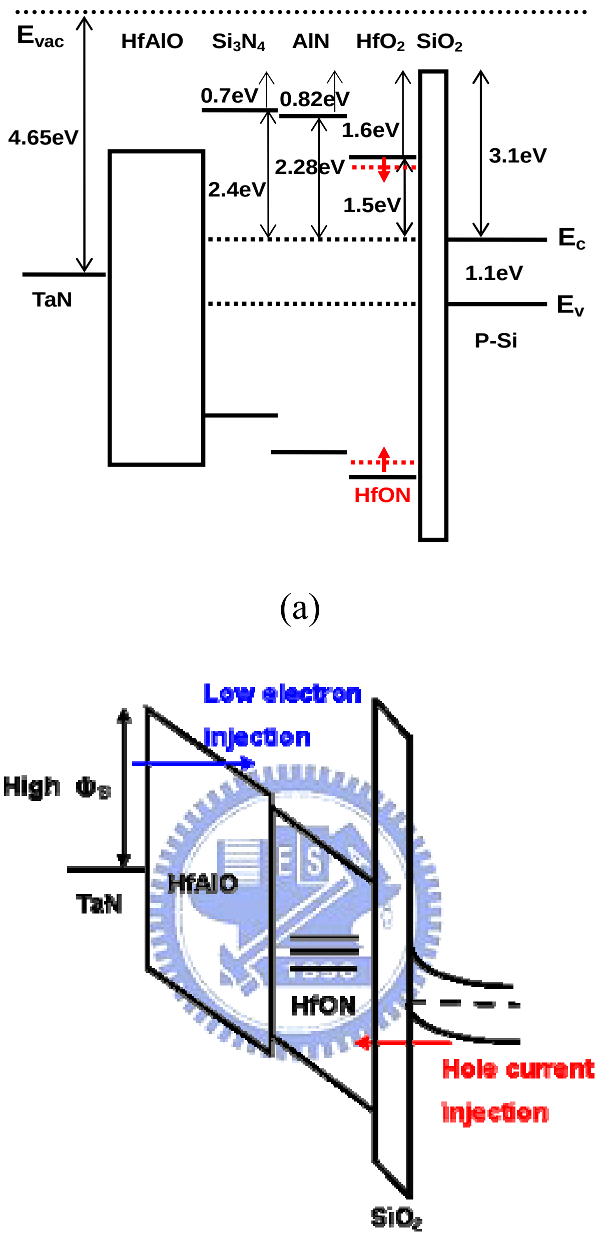


(a)



(b)

Fig. 5-4 XPS characteristics of (a) Hf_{4f} spectra and (b) N_{1s} spectra of HfON and control HfO_2 dielectrics.



(a)

(b)

Fig. 5-5(a) Energy band diagram of TaN-HfAlO-[trapping layer]-SiO_2-Si MONOS device with different Si_3N_4, AlN or HfON high-κ trapping layer; (b) energy band diagram of MONOS under erase function.

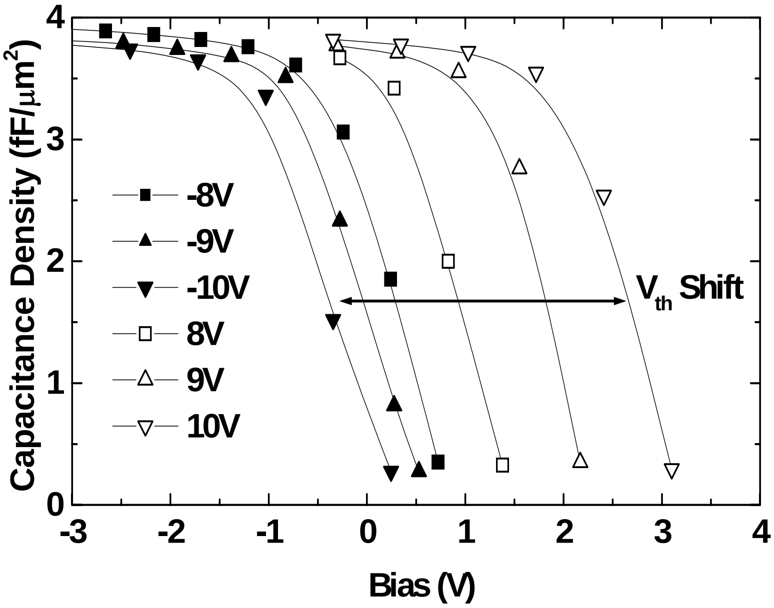


Fig. 5-6 C-V hysteresis curves of HfON MONOS capacitor. Very high capacitance density ~4 fF/μm^2 is obtained.

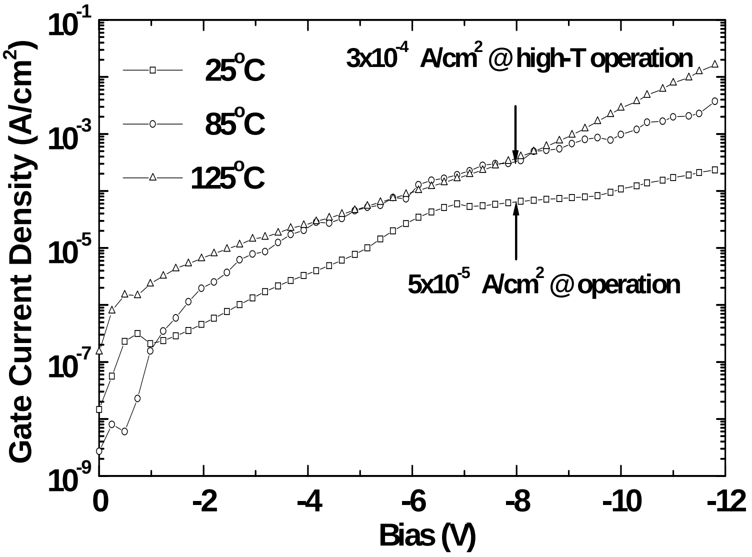


Fig. 5-7The J_g-V_g characteristics of TaN-HfAlO-HfON-SiO_2-Si MONOS under erase at 25-125°C.

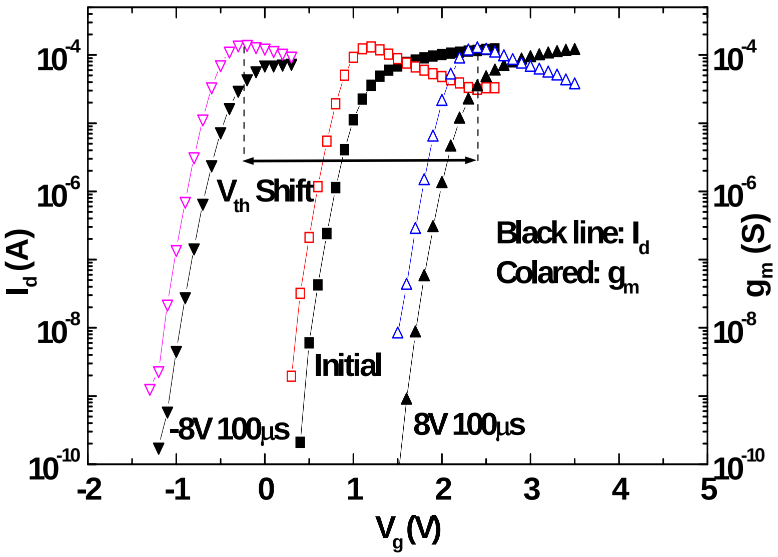
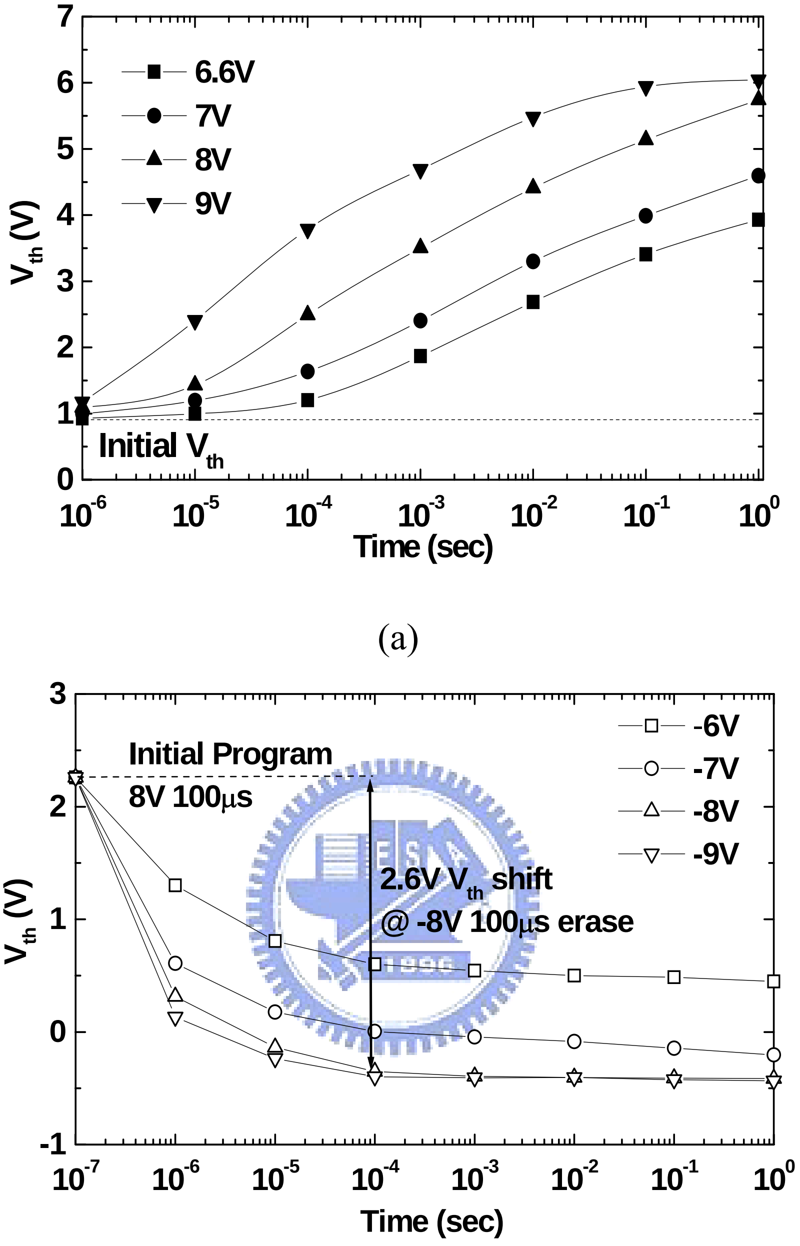


Fig. 5-8 The I_d-V_g and gm curves of HfON MONOS transistors.



(a)

(b)

Fig. 5-9 The P/E characteristics of HfON MONOS device. (a) The measured program characteristics from I_d-V_g of transistors (b) The measured erase characteristics from I_d-V_g of transistors.

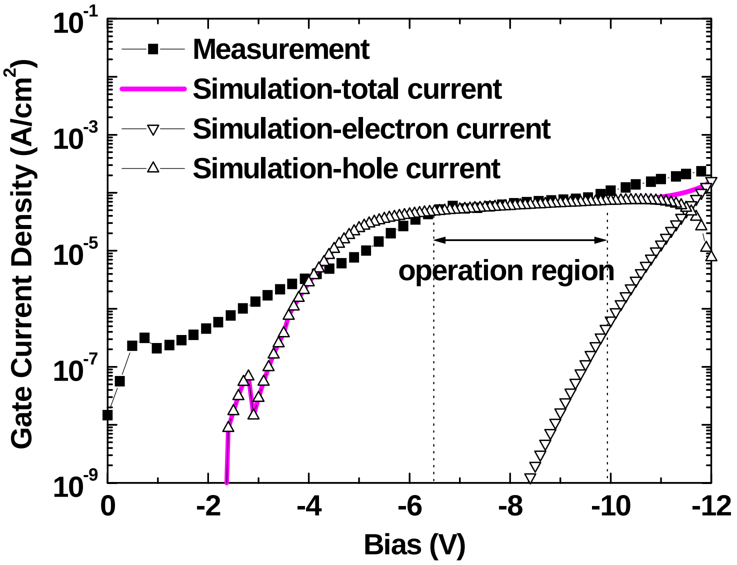
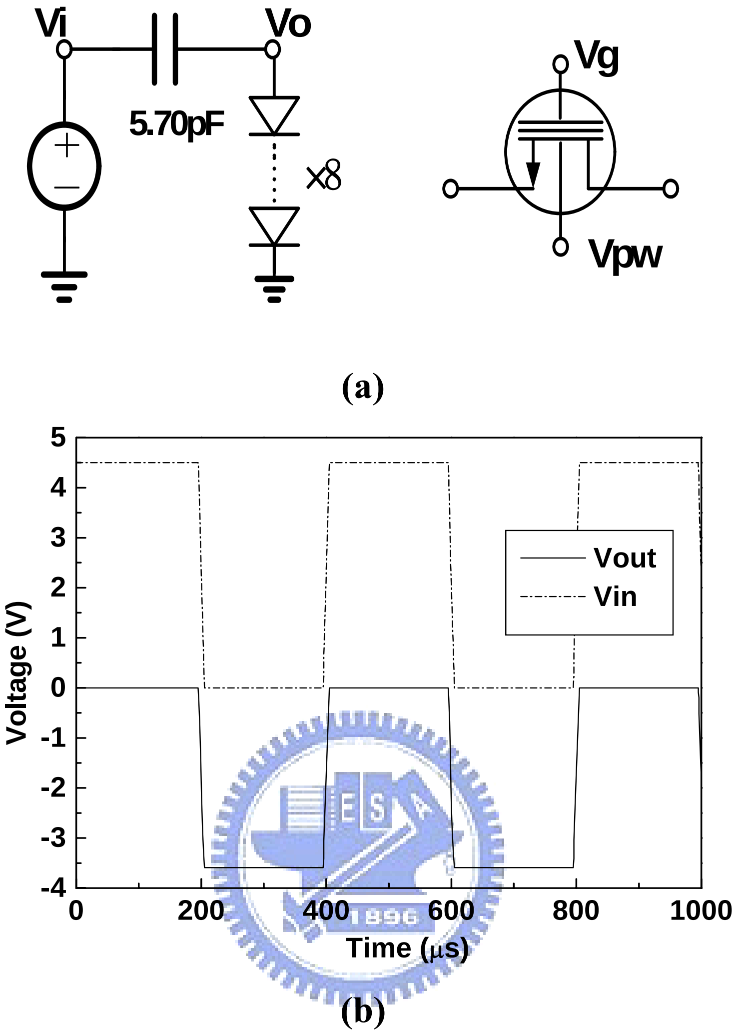


Fig. 5-10 Measured and TMA simulated J-V curves. The erase speed also depends on the hole injection from the Si channel.



(a)

(b)

Fig. 5-11 The diode-clamp circuit to generate negative -3.5 V from supplied 4.5 V voltage source using TSMC 0.18 μm library.

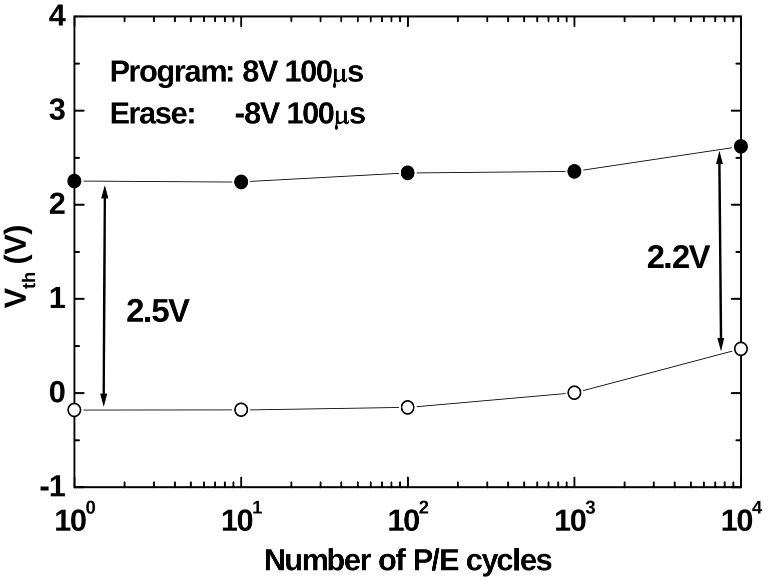
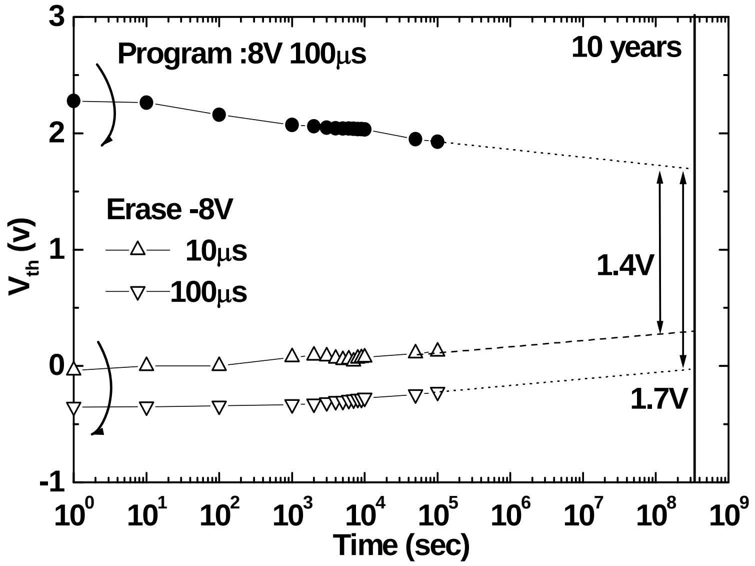
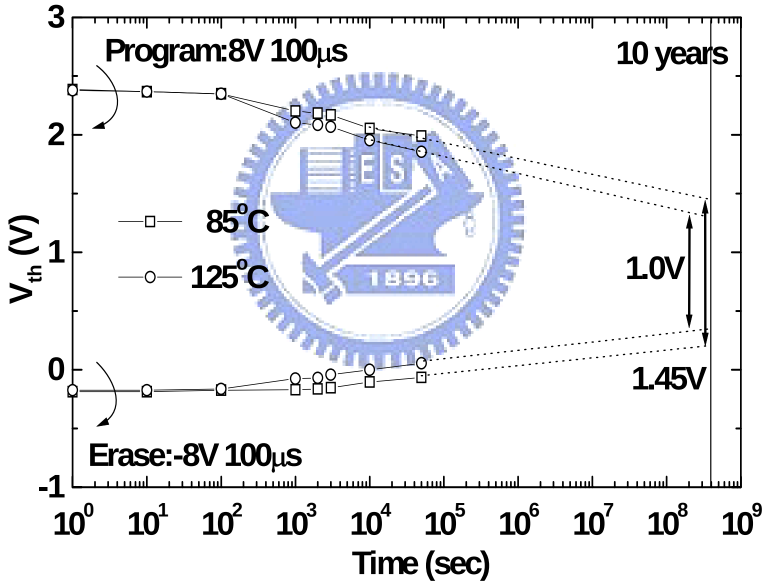


Fig. 5-12 Endurance characteristics of TaN-HfAlO-HfON-SiO_2-Si MONOS devices. The memory window is almost constant until 10 k P/E cycles with only 12% degradation.



(a)



(b)

Fig. 5-13 Retention characteristics of fresh TaN-HfAlO-HfON-SiO_2-Si MONOS devices at (a) room temperature and (b) elevated temperature.

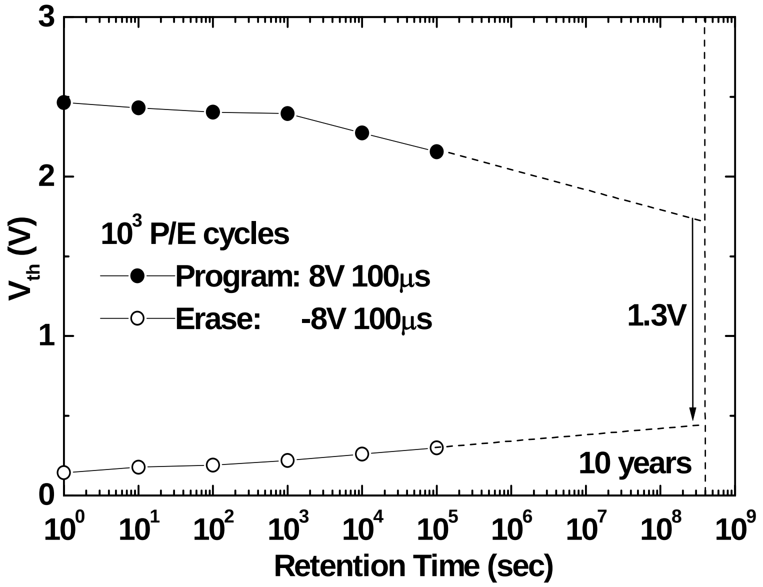


Fig. 5-14 Retention characteristics of 10^3 P/E-cycled MONOS devices.

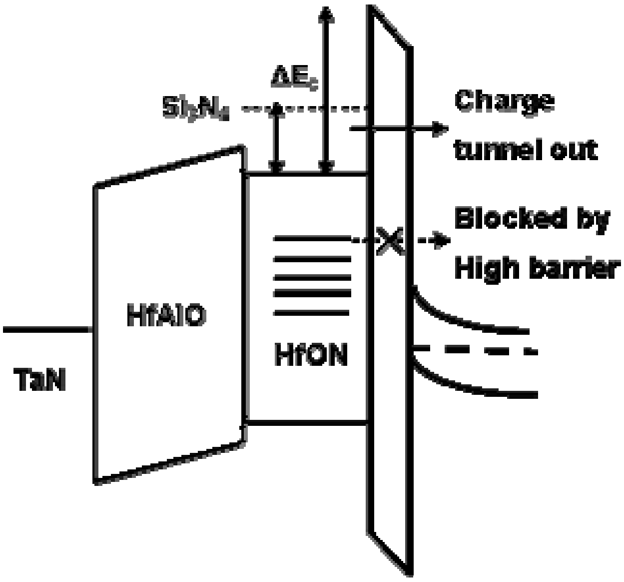


Fig. 5-15 The band diagram of TaN-HfAlO-HfON-SiO$_2$-Si MONOS memory device in retention mode.

Chapter 6
Conclusion

We have demonstrated a new approach using the AlN capacitor for 1T1C memory such as DRAM that has good data retention and program-erase function by charge trapping or de-trapping in the high trap density AlN. The programmed charges can be erased by a small voltage of -4 V for 1 ms. In addition, the AlN has unique merit of higher trap density than Al_2O_3 similar to that of Si_3N_4 than SiO_2, which is confirmed by the larger V_{th} shift at the same electric field. Another merit of this capacitor is the long retention time and evident to the small V_{th} variation of 0.06V after program or erase for 10^4 s and the potential of extended long memory time. This program-erasable high-κ AlN capacitor with good data retention provides an alternative solution to 1T1C memory.

We first compare the trapping capability between normally used Si_3N_4 with novel AlN dielectric. Significant better charge trapping is measured in AlN than Si_3N_4, where good P/E and retention characteristics can be achieved even in single layer AlN. Such excellent performance is further evident from the much better memory integrity in IrO_x-HfAlO-AlN-SiO_2-Si MONOS device with lower operation voltage, faster P/E speed and good retention than the best reported SONOS data using Si_3N_4 trapping layer. At 13 V and 100 μs program and -12 V 100 μs erase, we found a large ΔV_{th} of

3.1 V that extrapolated to 1.4 V for 10-year retention at 85°C. These values increased to 3.7 V for the initial ΔV_{th} and 1.9 V for the 10 year case at ±13 V and 100 μs P/E. This 100 μs speed, low operation voltage of 12-13 V, withstand above 10 k cycles and 1.9 V 10-year memory retention window at 85°C meet all the non-volatile memory requirements simultaneously.

Moreover, we further provide the TaN-HfAlO-HfON-SiO$_2$-Si MONOS device to operate at only 8 V under faster 100 μs. Under thus P/E condition, the device exhibits a large initial memory window of 2.5 V and the 10-years extrapolated retention window of 1.0 V at even 125°C. Using a simple voltage inverter circuit, the P/E voltage can further be reduced to nearly half: by applying 4.5 V and -3.5 V for the same ±8 V gate-channel bias. This is very important for embedded SoC application under a single 5 V voltage source.

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論文題目：

高介電係數介電質與金屬閘極製程技術應用在金屬–氧化層–氮化層–氧化層–矽結構之非揮發性記憶體

Process and Technology for High-k Metal Gate MONOS Structured Non-volatile Memory

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