# 國立交通大學

## 電子工程學系電子研究所

## 博士論文

# 高性能低溫多晶矽薄膜電晶體
# 之製程技術與特性研究

# Study on the Process Technologies and Characteristics of High-Performance Low Temperature Polycrystalline Silicon Thin-Film Transistors

研究生：蔡春乾
指導教授：鄭晃忠 博士

中華民國九十七年一月

# 高性能低溫多晶矽薄膜電晶體之製程技術與特性研究

# Study on the Process Technologies and Characteristics of High-Performance Low Temperature Polycrystalline Silicon Thin-Film Transistors

研究生: 蔡春乾　　Student: Chun-Chien Tsai

指導教授: 鄭晃忠　博士　　Advisor: Dr. Huang-Chung Cheng

國立交通大學

電子工程學系　電子研究所

博士論文

**A Dissertation**

Submitted to Department of Electronics Engineering & Institute of Electronics
College of Electrical Engineering and Computer Science
National Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy
in
Electronics Engineering

January 2008
Hsinchu, Taiwan, Republic of China

中華民國 九十七 年 一 月

# 高性能低溫多晶矽薄膜電晶體
# 之製程技術與特性研究

研究生：蔡春乾　　　　　　　　指導教授：鄭晃忠　博士

國立交通大學電子工程學系暨電子研究所

## 摘要

多晶矽薄膜電晶體因為具有較高的載子移動率，及可將周邊驅動電路與液晶面板積體化至玻璃基板上來降低液晶顯示器之生產成本的優勢，使得它成為液晶顯示技術應用中的關鍵元件，並且在高附加價值與多功能整合的系統面板（System-on-Panel）的應用及三維積體電路(3-D ICs)的實現上具有很大的潛力。在現階段，採用準分子雷射退火法對非晶矽薄膜進行再結晶是最有潛力的量產結晶技術，藉由達到快速熔融與固化再結晶的方法，可得到一高品質的多晶矽薄膜並且可以保持玻璃基板不受到高溫的影響。雖然透過準分子雷射可有效的提升多晶矽層的結晶性，但此方法仍有些許缺點，如隨機的晶粒邊界及晶粒分佈、大晶粒的製程窗口較窄小、主動層和介電層之間造成大的粗糙界面等等。在本篇論文裡，我們將提出多項雷射結晶方法及元件結構來增進低溫多晶矽薄膜電晶體的特性。

首先，為了改善低溫多晶矽薄膜電晶體的電特性，我們先針對元件通道的多晶矽薄膜結晶性進行改善。一種我們具有晶粒邊界位置控制的底閘極低溫多晶矽薄膜電晶體方法將被提出而加以探討。其結晶機制敘述如下，因為底閘極結構邊緣台階區提供了較厚非晶矽層，在準分子雷射退火時，我們只需將雷射能量控制在可以使薄區的非晶矽薄膜

完全熔解的能量密度以上，同時讓厚區的非晶矽薄膜部分熔解而確保留下部分微晶矽作為晶種，就可以得到一致分佈的大型晶粒成長，因此可以提升薄膜的均勻性及元件的效能。由實驗的結果分析可知，我們可以得到最大長度約為0.85μm長的人為控制晶粒。我們也製作出單一晶粒邊界的低溫多晶矽薄膜電晶體，其載子移動率可達到 330cm$^2$／V-s，同時閘極引起的汲極漏電和紐結效應也減少了，而且元件的均勻性也大幅提升。而且在閘極偏壓的可靠度量測之下，我們發現單一晶粒邊界的底閘極低溫多晶矽薄膜電晶體有較小的起始電壓漂移量及較高的崩潰電場，因此更適用於元件的微小化。

雖然單一晶粒邊界的底閘極低溫多晶矽薄膜電晶體表現出良好的電特性，由於偏離的黃光微影製程，造成源極（汲極）相對於閘極的離子佈植不對稱，使的元件的電特性不對稱。因此我們結合背後曝光方法與單一晶粒邊界的底閘極低溫多晶矽薄膜電晶體製作出新穎之自我對準的單一晶粒邊界的底閘極低溫多晶矽薄膜電晶體。我們不僅包留了單一晶粒邊界的底閘極低溫多晶矽薄膜電晶體的良好特性，自我對準的單一晶粒邊界的底閘極低溫多晶矽薄膜電晶體也表現出良好的電對稱性。如此一來我們更能將自我對準的單一晶粒邊界的底閘極低溫多晶矽薄膜電晶體應用於畫素電路中的開關元件。

將元件縮小，雖然可以進一步的提升多晶矽薄膜電晶體的電特性，但是也遭遇到嚴重的短通道效應，尤其是薄膜電晶體因為本身通道較多的缺陷及低溫製程，短通道效應更是較傳統金氧半場效電晶體明顯嚴重，因此雙閘極結構結合通道晶粒成長的技術也在本論文提出，藉由該底閘極的準分子雷射結晶法，通道中的晶粒成長控制來得到較好的結晶性，與上下雙閘極對通道的耦合來改善閘極對通道的控制能力，其 N 型元件以單通道長度換算之等效載子移動率可超過 1000 cm$^2$/V-s，而 P 型元件則超過 400 cm$^2$/V-s。此元件有高驅動電流，高開關電流比，優異的短通道抵抗力，較陡峭之次臨界擺幅，較小的汲極誘導能障下降(DIBL)，同時均勻性也得到改善。

雖然利用底閘極的準分子雷射結晶技術可以有效的改善多晶矽薄膜結晶性，但是不可避免的，在低溫多晶矽薄膜電晶體的通道中存在一高角度的晶粒邊界，進而對於元件電特性造成劣化及耐用度上的問題。因此我們提出了一個新穎的側向雷射結晶方式-間隙壁式結晶法-來消彌通道中的高角度的晶粒邊界，其結晶機制是利用空間上的熱傳機

制來達成晶粒橫向成長的目的，首先利用傳統間隙壁法製作出 50 奈米大小的晶種，並在局部微小區域產生兩種厚度不同的非晶矽薄膜，當準分子雷射照射在此一結構上，使較薄的區域完全熔融時，而間隙壁較厚的區域部分熔解，晶粒便會以這些非晶矽間隙壁為結晶起始點，做橫向成長，再藉由適當的安排間隙壁與元件通道的相關位置，我們將可以消除通道中所有垂直電流方向的晶粒邊界，更進一步的改善元件的載子移動率與均勻性。以通道長度為 2 μm 的元件為例，以此結晶方法做出的低溫多晶矽薄膜電晶體其載子移動率可以到達 288 $cm^2$/V-s，而傳統的元件的載子移動率只有 129 $cm^2$/V-s.。

為了更進一步的提升多晶矽薄膜電晶體的驅動能力，達到一類似絕緣層上覆晶矽（Silicon-On-Insulator-like）金氧半場效電晶體的效能，進而實現 SOP 或 3D ICs 的夢想，無晶粒邊界的單晶矽電晶體（Single-grain TFT）是最終目標的元件，因此我們提出了一個新穎的二維晶粒控制側向成長的雷射結晶方式，結合上述之非晶矽間隙壁及先定義矽薄膜之結晶法來分別達成 X 軸及 Y 軸的熱梯度，進而完成單晶粒之側向晶粒成長。從實驗分析結果發現，我們可以得到一直徑為 1.8 μm 大的圓型週期性單晶粒矽薄膜。以通道長度為 1.5 μm 的元件為例，以此結晶方法做出的低溫多晶矽薄膜電晶體其載子移動率可以到達 308 $cm^2$/V-s，開關電流比則高於 $10^8$，且具高度的均勻性。

上述的結晶法雖然可以達成大晶粒成長及高性能薄膜電晶體的目的，而本論文亦提出一新式的固態連續波雷射（Continuous-wave Laser）退火技術，直接利用控制掃瞄速度及掃瞄功率來達成晶粒橫向成長。一長度達 15 μm 的多晶矽薄膜晶粒可以製作出來而不損傷到玻璃基板，而實驗結果亦顯示矽薄膜具有極佳的結晶性，同時其晶粒邊界位置的表面粗糙度極為平順。利用連續波雷射結晶法製作的低溫多晶矽薄膜電晶體擁有優異的電特性，例如較高的電子移動率（n 通道的其載子移動率可達 500$cm^2$/V-s，而 p 通道的為 200$cm^2$/V-s）及較高的開關電流比。另外，我們也探討了利用連續波雷射在摻雜活化的退火特性，其由四點探針分析可得一片電阻低於 50 Ω/□，同時由二次離子質譜分析儀得到一均勻分佈的摻雜雜質，因此連續波雷射退火法是一個低熱預算和高效率的活化方法。由於連續波雷射結晶法製作大晶粒流程十分簡單，因此使用連續波結晶法製作的低溫多晶矽薄膜電晶體的亦極適合於未來系統面板的應用。

# Study on the Process Technologies and Characteristics of High-Performance Low Temperature Polycrystalline Silicon Thin-Film Transistors

Student: Chun-Chien Tsai Advisor: Dr. Huang-Chung Cheng

Department of Electronics Engineering &
Institute of Electronics
National Chiao Tung University

## ABSTRACT

Low-temperature polycrystalline silicon （LTPS）thin film transistors (TFTs) have been extensively studied for active matrix flat panel displays (AMFPDs), full-function system-on-panel (SOP), and potential for the 3-dimensional integrated circuits (3D-ICs) applications owing to their high field-effect mobility, low power consumption, high reliability, high resolution, and low fabrication cost by the integration of driver and controller ICs. At this moment, excimer laser crystallization (ELC) of amorphous silicon (a-Si) thin films seems to be the most promising method for its great advantages in mass production and high quality silicon grains without damage to the glass/plastic substrates. Although large grains can be attained in the super lateral growth (SLG) regime by ELC, many fine grains still spread between these large grains due to the narrow process window for producing large-grain poly-Si and highly rough interface. Consequently, non-uniform and randomly distributed poly-Si grains will result in the large variation of TFT performance when the laser energy density is controlled in the SLG regime, especially for the small-dimensional TFTs. In this

thesis, many approaches, including techniques of excimer-laser-crystallized poly-Si thin films, advanced device structures, and diode-pumped solid-state (DPSS) continuous-wave (CW) laser annealing, have been proposed to further enhance the performance of LTPS TFTs.

At first, from the perspective of improving channel material quality, LTPS TFTs with bottom gates (BG) have been demonstrated to achieve large silicon grains due to the lateral grain growth. In this method, a-Si thin film with two kinds of thicknesses in a local region was formed by the deposition of a-Si films on the plateau structure. When the excimer laser irradiation is applied on the a-Si thin film, the applied laser energy density is controlled to completely melt the thin region of a-Si film in the channel region but partially melted the thick region of a-Si film near the edges of bottom gate. Therefore, a lateral temperature gradient can be produced between the local thin and thick regions of a-Si film, and the lateral grain growth started from the un-melted silicon solid seed at the base neighbor to the bottom-gate corner, and extended toward the completely melted region until the solid-melt interface from opposite direction impinges. From material analyses, it can be observed that the large longitudinal grains artificially grown of about 0.85 μm in size were observed in the device channel region. Therefore, high-performance BG LTPS-TFTs have been demonstrated with the field-effect mobility exceeding 330cm$^2$/V-s, low GIDL effect, suppressed kink current, and improved device uniformity due to the large silicon grains. Moreover, the BG TFTs reveal higher breakdown voltage and better reliability due to the smooth interface between gate dielectric and poly-Si channel films as thinner gate oxide were employed without additional processes or materials. The improved breakdown and driving characteristics imply that the proposed BG-TFT structure is more suitable for the device-scaled-down applications.

Although BG LTPS-TFTs exhibit superior electrical characteristics, asymmetrical electrical characteristics are also observed due to the misaligned process effect. Therefore, a self–aligned (SA) bottom-gate TFT with appropriate channel length has been fabricated by the simple ELC and backside exposure. As a result, not only all the advantages of BG LTPS-TFTs with lateral silicon grains, but also the symmetrical electrical characteristics can be also observed in SA BG LTPS-TFTs. Consequently, SA-BG TFTs with the channel length of 1 μm exhibited field-effect-mobility reaching 193 cm$^2$/Vs without hydrogenation, while the mobility of the conventional non-SA-BG TFTs and conventional SA top-gate ones were about 17.8 cm$^2$/Vs and 103 cm$^2$/Vs, respectively.

Shrinking the device size is an effective way to improving the device performance, but poor short-channel effects (SCE) is encountered owing to the insufficient gate controllability. Novel high-performance LTPS TFTs with double-gate (DG) structure and controlled lateral grain growth have been demonstrated by excimer laser crystallization. Because of the double gate operation mode and lateral silicon grains formed in the channel region, the devices have a higher driving current, steeper subthreshold slope, superior short-channel effect immunity, and suppression of the floating-body effect. The proposed DG TFTs (W/L = 1/1 μm) have the equivalent field-effect-mobility exceeding 1050 cm$^2$/Vs for the N-channel device, 403 cm$^2$/Vs for the P-channel device, on/off current ratio higher than $10^9$, smaller DIBL, and excellent device uniformity.

Although the crystallinity of poly-Si thin film can be effectively enhanced via ELC with bottom-gate structure, it is inevitable that there is a high angle grain boundary in the middle of channel region, which degrades the TFT performance and reliability. A novel laser crystallization method which can remove the high angle grain boundary and produce the large and uniform grains in the desired local region is proposed to improve the field-effect mobility as well as the device uniformity. Periodically lateral silicon grains with 2 μm in length can be artificially grown in the channel regions via the amorphous silicon spacer structure with excimer laser irradiation. By the way, such periodically large and lateral grains in the TFTs would achieve high field-effect mobility of 298 cm$^2$/Vs, as compared with the conventional ones of 128 cm$^2$/Vs. In addition, the device-to-device uniformity could be improved due to this location-manipulated lateral silicon grains.

In order to further improve the performance of LTPS TFTs, single-grain TFT in which the channel is grain-boundary-free will exhibit SOI-like performance to satisfy the requirements of system on panel. A new crystallization technology for producing two-dimensional lateral grain growth, aiming at single-grain TFT, has been developed by excimer laser irradiation relying on the spatially temperature distribution at the artificially sites. The high quality silicon grains are controlled via manipulating super lateral growth phenomenon by spatially two kinds of silicon films and pre-patterned structure. An array of 1.8-μm-sized disklike silicon grains is formed periodically. Not only high-performance poly-Si TFTs with field-effect-mobility reaching 308 cm$^2$/Vs but also excellent device uniformity are demonstrated owing to the artificially-controlled lateral grain growth. Proposed poly-Si TFTs, therefore, have great potential for the future SOP and 3D-ICs applications.

Although the aforementioned laser crystallization methods can fabricate large homogeneous silicon grains and high-performance LTPS TFTs, another crystallization approach, a new and simple CW laser crystallization, is also proposed to produce lateral grain growth via controlling the laser scanning speed and laser power. According to the experimental results, a directional river-like lateral Si grain growth with tens of micron, flat surface morphology, and excellent crystallinity are achieved without damage to the glass substrates. As a result, ultra-high performance CW laser-annealed LTPS-TFTs have been fabricated on the oxidized silicon wafer for the first time with field-effect mobility exceeding 504 cm$^2$/V-s for n-channel devices and 220 cm$^2$/V-s for p-channel devices. It is also found that CW laser annealing is a low-thermal-budget and high-efficiency dopant activation method attributed to the low sheet resistance and uniformly redistributed dopant profiles after CW laser annealing. Because of the simple process, continuous-wave laser-annealed LTPS TFTs are very promising for the future SOP, 3D-ICs, and solar cell applications.

# 誌　謝

感謝我的論文指導教授 鄭晃忠博士在實驗、研究與論文上的熱心且詳實的指導，老師嚴謹認真的研究態度以及謙恭溫和的待人處事，都讓學生獲益良多，老師耐心的教誨與鼓勵，也使我能順利完成博士學位。

感謝常鼎國學長與林敬偉學長帶領我進入低溫多晶矽薄膜電晶體的研究領域，給予充分熱心的實驗訓練幫助及研究觀念上的指導，也由衷的感謝陳旭信學弟、韋凱方學弟、曾煥均學弟、陳彥佑學弟、張為鈞學弟在實驗及計畫上的幫忙及支援，同時感謝李逸哲同學、李序恆學弟、楊柏宇學弟、李耀仁學長、林家彬學長在行政及生活上的幫忙與協助；使得本論文研究得以順利的完成。

感謝實驗室的學長、同學、學弟妹及助理們，謝謝你們在實驗或是生活上都能夠給予我支持與關心，使得我的研究能夠順利完成，其中包含了王志良學長、阮全平學長、陳國基學長、張芳龍學長、張國瑞學長、曾章和學長、張原熏學長、朱芳村學長、林高照同學、陳柏廷學弟、賴瑞霖學弟、呂健豪學弟、江可玉學妹、郭育如學妹、魏瑛君學妹、廖大傳學弟、許鈞凱學弟、林君翰學弟、王祐圻學弟、陳俠威學弟、高翠敏助理、簡秀芳助理、李瑩姿助理、凌碧蓮助理、張依婷助理、楊宜樺助理以及其他學長、同學、學弟妹們，有了你們在生活上的相伴和打氣，此論文才能順利完成。

感謝國立交通大學奈米中心及國家奈米元件實驗室提供優良的設備與研究環境，尤其要感謝彭兆光先生、吳政三先生、徐秀鑾小姐、陳明麗小姐、黃月美小姐、陳聯珠小姐、陳悅婷小姐、彭馨誼小姐、倪月珍小姐、范秀蘭小姐、林素珠小姐、徐台鳳小姐、劉曉玲小姐及何惟梅小姐等，在製程、設備及分析上的大力協助。也感謝諸位口試委員的指導與建議。

感謝我敬愛的父母 蔡神祐先生與陳蓮枝女士，謝謝你們多年來辛苦的培育我，教育我，有了你們持續的支持與默默的付出，才能讓我得以全心投入學業，完成博士學位，同時也要感謝我的妹妹 蔡月霜以及弟弟 蔡育修，在家中生活上的幫忙扶持。

感謝我的太太 韋郁雯在我研究生生涯中無悔的支持我，不論晴雨，一路相隨；也感謝太太娘家家人的對我的鼓勵與信任，由衷的感謝你們。

最後感謝所有曾經幫助過我的朋友們，謝謝你們一路上給我的支持與關心。

# Contents

# Table Captions

## Chapter 1

## Chapter 2

## Chapter 3

## Chapter 4

## Chapter 5

## Chapter 6

## Chapter 7

# Figure Captions

## Chapter 1

## Chapter 2

## Chapter 3

## Chapter 4

# Chapter 5

## Chapter 6

## Chapter 7

# Chapter 1

# Introduction

## 1.1 The Evolution of Silicon-Based Thin-Film Transistors

Si–based thin film transistors (TFTs) have been successfully utilized in the mature of flat-panel display applications, including liquid crystal displays (LCDs) [1.1], light valves for projectors [1.2], and organic light emitting displays [1.3]. Currently, hydrogenated amorphous Si (a-Si) TFTs are the mainstream technology in AMLCDs as switching devices attributed to the advantages of low processing temperature, simple fabrication process, low leakage current, and compatible with large-area glass substrate. However, the low electron field-effect mobility of a-Si TFTs ($< 1$ cm$^2$ V$^{-1}$ s$^{-1}$) limits their technology to integrate drive circuits on the active matrix glass plate. On the other hand, high temperature poly-Si (HTPS) TFTs processed at temperature of 900°C on quartz substrates for high-definition LCD projection systems compared to a-Si TFTs. High processing temperature, expensive quartz substrate, and limited area backplane, however, limit HTPS TFTs application to niche produce category. Low-temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) fabricated with a maximum temperature below 600 ℃ on glass substrate make large-area high-definition active matrix displays more practical and less expensive. As a result, LTPS TFTs have been great potential of reducing the fabrication cost and improving the system reliability because of their superior mobility performance for integration of both the the peripheral driving circuitry and active matrix pixel switching elements onto the single substrate [1.4] - [1.5]. Such driver integration not only reduces the display module weight and thickness but also improves the panel reliability. In addition, both high-performance n- and p-channel devices can be achieved in poly-Si films to realize complementary metal-oxide-semiconductor (CMOS) circuits [1.6]. The major advantages of CMOS circuits and systems are lower power dissipation, smaller signal voltages, higher fabrication yields, higher circuit gain, and simpler design methods. The higher driving current allows smaller TFTs to be used as the pixel-switching elements, resulting in higher aperture ratio, higher brightness and lower parasitic gate-line capacitance for improved display performance [1.7]. Besides, LTPS TFTs enables the possibility of an entire system-on-panel (SOP), including memory, photodiodes, Sensors, and micro-processor-unit, etc, which could generate variety of innovative new markets such as sheet computer, flexible electronics, and three dimensional integrated circuits (3D-ICs) [1.8] - [1.20].

Although the LTPS TFTs show many benefits comparing with a-Si TFTs and HTPS TFTs, many researchers has been devoted themselves to developing various technologies, improvement of poly-Si film crystallinity, growth of high quality gate oxide at low temperature, suppression of leakage current, and immunity of hot carrier effect, for enhancing the performance and reliability of LTPS TFTs [1.21]-[1.49]. Polycrystalline Si (poly-Si) thin films have been regarded as the most key materials for fabricating high-performance LTPS TFTs. Among various preparation techniques of poly-Si films, excimer laser crystallization has great potential for mass production of flat panel displays at this moment owing to high throughput, low temperature process compatible with glass/plastic substrates, and fabrication of high-quality poly-Si material [1.50]. However, other low-temperature processing technologies, such as high quality gate dielectric formation, high efficiency ion doping/dopant activation, defect passivation, photolithography equipment, and etching system, are also indispensable for producing high-performance and high-reliability LTPS TFTs [1.51].

In the following section, we will discuss more detailed about the fabrication process of poly-Si thin film, TFT architectures, doping and activation technique for LTPS TFTs, and the applications of LTPS TFTs.

## 1.2 TFT Structure

The top-gate structure, the gate electrode located above the semiconductor layer, is the most popular adopted for poly-Si TFTs in AMLCD applications. This is attributed to the fabrication technologies for bulk metal-oxide-semiconductor field effect transistors (MOSFETs), such as ion implantation and thermal oxidation. The self-aligned source/drain capability is the most feature to provide low parasitic capacitances, which are advantageous for achieving high circuit performance. Therefore, the top-gate TFTs is very suitable for device scaling down due to the self-alignment capability.

The bottom-gate structure, the gate electrode located below the semiconductor layer, is the most common configuration for a-Si TFTs due to the clean interface. As a result, if the bottom-gate is used for poly-Si TFTs, it offers some benefits over the top-gate structure for AMLCD applications. First, clean interface control can be easily achieved due to the ability to deposit the gate dielectric and silicon films sequentially in a single system without breaking vacuum. Second, the plasma hydrogenation diffusion rate in the bottom-gate TFT structure is significantly higher than that in top-gate TFT structure, because the channel thin film is not blocked by the gate-electrode thin films during hydrogenation passivation. The main disadvantage of the bottom-gate TFT structure is its lower driving current than top gate TFT. The effective carrier mobility of bottom-gate TFTs is generally much lower than that of top-gate TFTs, because of the smaller poly-Si grain size and poor silicon grain quality produced by laser crystallization.

In order to realize system-on-panel applications, the scaling down of device size is indispensable for better device performance and higher packing density. However, shrinking device size, especially scaling down the channel length, will lead to undesirable short channel effects attributed to the insufficient gate-control ability. It will result in the threshold voltage roll-off, degradation in drain breakdown and severe kink current. Comparing with single crystalline Si MOSFETs, poly-Si TFTs show more seriously short channel effect due to the presence of numerous defects in the grain boundaries, which in turn enhance the impact ionization by increasing the local electric field of drain junction [1.52] - [1.55]. Since the defect traps play an intense influence on electrical characteristics of poly-Si TFTs, one effective approach is to reduce the defect traps by improving the material quality of poly-Si thin films. The other important method is to reduce the undesired effects by modifying the device architecture of poly-Si TFTs. A double gate structure is expected to be the alternative device structure for the ultimate high-performance ideal MOSFETs. The double gate has two gates, one above and the other below the semiconductor layer. The top and bottom gates are symmetrical, in which the gate oxide thickness is the same, and connect together electrically to obtain a perfect coupling between the surface potential in the channel region and the gate. Consequently, the influence of the source and drain depletion regions are kept minimal, which in turn reduce the short channel effects by screening the source and drain electrical field lines away from the channel. The most innovative electrical property of the double gate device is the possibility of forming surface inversion layers at the top and the bottom of the semiconductor channel but also inverting the entire film thickness if the semiconductor film thickness is thin enough. Because the inversion is distributed across the whole silicon film thickness, the effect of bulk carrier mobility, in contrast to surface mobility, can be observed. This phenomenon is called volume inversion which contributes to higher drain current and higher transconductance. Moreover, smaller Drain-Induced-Barrier-Lowering (DIBL), larger on/off current ratio, reduced kink current, and higher channel conductivity are attained in the double-gate poly-Si TFTs. Therefore, double-gate TFTs has emerged as a promising candidate for future applications in SOP and 3D-ICs fields.

## 1.3 Approaches to the Preparation of Polycrystalline Silicon Thin Films

### 1.3.1 Solid Phase Crystallization for Poly-Si Thin Films

Since the direct-deposited poly-Si thin films exhibits small grain size and lots of trap states and need high deposition temperature (~ 620 ℃), the direct deposition method has been excluded in the fabrication of high-performance LTPS TFTs. In polycrystalline silicon material, the grain boundaries play great influence on the electrical characteristics of poly-Si TFTs due to the existing lots of defects such as dangling bonds and strained bonds. These defects trap states lying within the band gap [1.55] deeply degrade the all aspects of device performance, including higher threshold voltage, lower carrier mobility, larger leakage current, and poor long-term stability [1.56]. Therefore, reducing the defect trap densities in poly-Si films becomes an important topic for the fabrication of high performance poly-Si TFTs. Passivation of defect states in the grain boundaries as well as in the grain [1.57] - [1.60] and enlarging poly-Si grain size in the device channel region are two effective methods to reduce the defect state densities in poly-Si thin films [1.61]-[1.64]. Plasma hydrogenation is common used to passivate the defects in poly-Si film for attaining improvement of device performance and uniformity. Poly-Si TFTs after hydrogen passivation suffer from poor hot carrier endurance and a low thermal stability due to the weak Si-H bond [1.65] - [1.66]. Reducing the defect states via enlarging poly-Si grain size is an intrinsic approach to single crystal Si material, which leads to the silicon-on-insulator like (SOI-like) device performance.

Silicon thin films deposited in the amorphous state and then crystallized into poly structure have been shown to have higher carrier mobility due to the large grain size compared to the direct-deposited polycrystalline thin films [1.67]. Solid phase crystallization (SPC) of amorphous Si is a simple method to convert them into poly-Si thin film with large grains via furnace annealing by thermal energy for 24 hours at temperatures of 600 °C [1.68]. SPC involves two distinct processes, the nucleation of seeds and grain growth into final polycrystalline films [1.69]. The transformation proceeds within the amorphous matrix after an apparent incubation period by the nucleation and dendritic-like growth of crystal domain [1.70]. Final grain size could be large if the nucleation rate is low and the grain growth rate is high [1.70]. An alternative to enlarge poly-Si grain size is to modify the structural disorder of the starting a-Si. For example, a significant enlargement of grain size of solid-phase-crystallized poly-Si by self-ion implanted silicon films deposited by LPCVD. The high structure disorder of the Si network increases the active energy required, thus, delays the incubation period of Si nucleate during the thermal annealing [1.71] - [1.72]. Therefore, the grain size is enlarged due to the reduction of nucleation seeds and nucleation rate. Besides, it has been reported that the grain size of the crystallized films formed from disilane ($Si_2H_6$) is larger than that formed from silane ($SiH_4$) because of higher structure disorder of disilane owing to higher deposition rates and lower deposition temperatures as compared with siliane ($SiH_4$) using pyrolytic chemical vapor deposition (CVD) [1.73] - [1.75]. In spite of long crystallization durations of several tens of hours, large defect density still exists in the crystallized poly-Si films due to the low temperature process.

### 1.3.2 Metal Induced Crystallization for Poly-Si Thin Films

It is found that the thermal budget of a-Si can be lowered by the introduction of metal impurities [1.76]-[1.82]. For example, as a certain metal, Al, Pd, or Ni, is deposited on a-Si, the a-Si films crystallizes to poly-Si structure at a lower temperature than its SPC temperature. The reaction between a metal and a-Si occurs at an interlayer by diffusion and it lowers the crystallization temperature. Such enhancement of crystallization is due to an interaction of the free electrons from the metal with covalent Si bonds near the growing interface [1.78]. Considering the temperature of metal-Si eutectic, a-Si thin film can be crystallized below 500°C. Among the above metals, Ni has been the best candidate of inducing metal lateral crystallization technology at low temperature for fabricating high quality poly-Si thin films with better crystallinity.

An equilibrium free-energy diagram is provided for explanation of the mechanism of Ni induced crystallization [1.83]. For $NiSi_2$ in contact with a-Si and c-Si, the driving force for the phase transformation is the reduction in free energy associated with the transformation of metastable a-Si to stable c-Si. The $NiSi_2$ precipitate acts as a good nucleus of Si and the crystallization of a-Si is mediated by the migration of the $NiSi_2$ precipitates [1.83]. The silicide formation proceeds sequentially, starting from the metal-rich silicide ($Ni_2Si$) to end up to the silicon-rich silicide ($NiSi_2$), by the metal/silicon diffusion resulting in the successive formation of the silicides. For a migrating $NiSi_2$ precipitate consuming a-Si at the leading interface and forming a trail of epitaxial single crystal Si, needlelike Si crystal grain grow in the <111> direction due to the surface free energy of the {111} plane in Si is lower than that of any other orientation. [1.83].

Recently, it was found that MILC rate could be enhanced remarkably and the crystallization temperature could be reduced to as below as 380°C due to the presence of an electrical field [1.84] - [1.87]. The phenomenon was explained by the enhanced diffusion of charged nickel through $NiSi_2$ precipitates in the applied electrical field [1.87].

The post high temperature annealing on MILC poly-Si films is a critical step in forming high quality poly-Si films with large grain size. Secondary re-crystallization takes place in MILC poly-Si films via furnace annealing att about 800°C or laser annealing. As a result, most of the intra-grain defects and low-angle grain boundaries between needlelike crystallites disappear, and small grains are merged to become a large grain with extremely large size. The surface anisotropy of the grains is responsible for the further grain enhancement that provides the energy to repair the defects in MILC poly-Si films and to merge the small grains separated by low-angle grain boundaries [1.88]. Finally, super giant silicon grains with the same orientation (110) are achieved for high-performance and good uniformity TFTs.

In spite of low crystallization temperature and high growth rate, metal contamination incorporated into metal induced crystallized poly-Si thin films is a serious problem which resulted in poor TFT performance, such as high leakage current, large kink current, worse subthreshold swing, and poor device stability. In order to alleviate the problem of the metal contamination, using the metal solutions or depositing ultra-thin discrete metal layer on a-Si are proposed to fabricate poly-Si thin films [1.89]-[1.90].

### 1.3.3 Laser Crystallization for Poly-Si Thin Films

Laser crystallization process in fabrication silicon-on-insulator devices for microelectronics and thin-film transistors for displays has been receiving considerable attention [1.91]-[1.97]. Laser crystallization can produce large-grained poly-Si thin film with low intra-grain defects via liquid phase crystallization as compared with solid phase crystallization and metal induced crystallization. Therefore, many researches of laser crystallization of amorphous silicon films for the preparation of poly-Si films for LTPS TFTs have been studied using various kinds of lasers techniques, such as $CO_2$, Ar, Nd:YAG, Nd:$YVO_4$, excimer, femtosecond lasers, and etc [1.96]-[1.104]. Among these laser techniques, excimer laser annealing, to date, is the widely used method to prepare poly-Si thin films because of its high pulsed-laser power for large area glass substrate and the large absorption coefficient for a-Si in the UV light region (optical absorption coefficient > $10^6$ $cm^{-1}$) for no damage to glass substrate. According to the mixture gas used in the laser tube, excimer laser radiation of output wavelengths between 157 - 351 nm (157, 193, 248, 308 and 351 nm for $F_2$, ArF, KrF, XeCl and XeF laser, respectively) by the transient high voltage discharge with a short pulse duration (full width of half maximum ~ tens of nanoseconds). The basic principle of excimer laser crystallization is the phase transformation of silicon thin film from amorphous to single-crystal material via melting the Si thin film within a very short time. Actually, the a-Si thin film is heated to the temperature of about 1200°C during laser irradiation. However, the high temperatures are only persistent for tens of nanoseconds during laser pulse duration. In consequence, the introduction of thermal damage to the glass substrate and the thermal compaction problem are relaxed, which are serious issues in the solid phase crystallization. Another unique advantage of excimer lasers is the strong optical absorption of UV light in silicon. As a result, most of the incident laser energy is absorbed close to the surface of the thin film without causing severe thermal strain on the substrate. The unique advantages of strong optical absorption of the UV light in silicon and short pulse duration of the excimer laser imply that high temperature can be produced in the silicon surface region, causing rapidly melting and solidifying quickly, without significant heating the substrate and impurities contamination from the substrate diffusion into the silicon thin film. This technology yield high quality and large-grained poly-Si thin film for high-performance LTPS TFTs on glass or plastic substrate with high throughput.

Owing to the advantageous features of excimer laser crystallization for large area microelectronics fabrication, many researches have been done to study the dynamics kinetics and transformation mechanisms of the laser crystallization of a-Si thin films. The characteristics of poly-Si thin film have been shown to be related to the process conditions of

ELC, such as laser energy density, laser pulse duration, laser shot number per area, crystallization ambient, and substrate temperature [1.105] - [1.109]. Moreover, the initial status of a-Si precursor film, including a-Si film thickness, hydrogen content, and impurity content, has a profound effect on the properties of the resulting poly-Si film [1.109] - [1.12]. According to the reports of James. S. Im et al., excimer laser crystallization of amorphous silicon thin films on foreign substrate can be divide into three transformation regimes with respect to the applied laser energy densities [1.113] - [1.114]. These are the partial-melting, full-melting, and near-complete-melting regimes, which are schematically illustrated in Fig. 1-1 (a), Fig. 1-2 (a), and Fig. 1-3 (a), respectively.

## Partial-melting regime (Low energy density regime)

In the partial melting regime, the incident laser energy density is larger than the threshold energy of melting of a-Si films. The applied laser energy density can cause only surface melting of a-Si thin films but not the entire silicon films (i.e., melting depth < film thickness). Therefore, a-Si thin film can be partially melted and subsequently be recrystallized from the underlying continuous layer of remained solid Si. In this regime, the poly-Si grain size increases with the increases of the laser energy density. In addition, it is characterized that explosive crystallization of a-Si thin film occurs at the onset of the transformation and follows by vertical grain growth, and competitive occlusion of grains [1.115]. The early trigger of explosive crystallization may be attributed to the presence of microcrystalline clusters or to the presence of impurities in the silicon films. Fig. 1-1 (b) and 1-1 (c) show the plane-view scanning electron micrograph (SEM) and cross-sectional transmission electron micrograph (TEM) of excimer-laser- crystallized poly-Si thin films in the partial-melting regime, respectively. It can be found that the poly-Si grain size crystallized in the partial melting regime are smaller than 0.1 μm and there are two distinct silicon layers of amorphous and polycrystalline material due to the partial melting of a-Si films.

## Complete-melting regime (High energy density regime)

In the complete melting regime, the incident laser energy density is sufficient high to cause the complete melting of the entire a-Si thin films. Since the glass substrate is amorphous structure, epitaxial layer growth from the substrate is not possible. For the complete-melting Si thin film, a deep supercooling of the liquid silicon film leads to homogeneous nucleation before the transformation of poly-Si in solid phase [1.116] - [1.17].. In this regime, the final microstructure is insensitive to the applied laser energy densities. Fine-grained and small-grained poly-Si thin films are attained due to the low substrate temperatures. In addition, a phenomenon of amorphization is observed in thinner silicon films [1.118]. Fig. 1-2 (b) and 1-2 (c) show the plane-view SEM and cross-sectional TEM of excimer-laser- crystallized poly-Si thin films in the complete-melting regime, respectively. It can be observed that the poly-Si grain size of the thin films crystallized in the complete melting regime are smaller than 100 nm and poly-Si films are in the column structure due to the complete melting of the entire silicon layers.

## Near-complete-melting regime (Super-lateral-growth regime)

In the near-complete-melting regime, the incident laser energy density leads to a complete melting a-Si thin film consisting of un-melted discrete silicon islands (i.e. melting depth ≅ film thickness). James. S. Im et al. identified the third transformation regime, the end of the low energy density regime and the beginning of the high energy density regime, in a narrow experimental window [1.113] - [1.114]. In this regime, large-grained poly-Si films with grain sizes many times larger than the film thickness are observed. Since the grain size is much larger than that in the other two transformation regimes, Im named it super lateral growth (SLG) regime due to its unique nature [1.114]. Based on Im's model, it is argued that the un-melted portion of the underlying Si no longer forms a continuous layer but instead consists of discrete solid silicon islands which are separated by small local regions in the completely melting silicon film. The un-melted silicon islands act as nucleation seeds and lateral grain growth can proceed toward the complete melting region. Therefore, a significant lateral growth takes place before the impingement of the grain grown from the other side depending on the separation distance between these seeds. There is a limit for the maximum lateral growth distance; however, since the continuous cooling of the liquid layer via thermal conduction to the underlying substrate eventually would leads to copious nucleation of solids in bulk liquid ahead of the interface. According to the SLG model, the super lateral grain growth distance will increase with thicker film thickness, higher substrate temperature, lower thermal conductivity of the substrate, and longer laser pulse duration. In addition, the applied energy density for super lateral growth regime increases with thicker film thickness, shorter laser pulse duration, higher thermal conductivity of the substrate, and lower substrate temperature. It is concluded that the lateral grain growth is resulted from the thermal gradient between the solid and liquid interface and the lateral grain growth distance is determined by the quenching rate of liquid silicon and the residual solid Si seed distance. As a result, the SLG distance can be prolonged by enlarging the lateral thermal gradient and increasing the solidification duration. Fig. 1-3 (b) and 1-3 (c) show the plane-view SEM and cross-sectional TEM of excimer-laser- crystallized poly-Si thin films in the near-complete-melting regime, respectively. It can be observed that large poly-Si grain size of about 1 μm is observed and the quality of poly-Si grain is excellent in the near-complete melting regime as compared with those in partial-melting and complete-melting regimes. However, a very non-uniform grain size distribution is observed in the SLG regime due to the fluctuation of pulse-to-pulse laser energy density, non-uniform laser beam profile, and non-uniformity of a-Si thin film thickness. The non-uniform grain distribution causes device degradation and poor device-to-device uniformity as the laser energy density is controlled in the SLG regime. It is very undesirable for device and circuits applications.

## 1.4 Ion Doping and Activation

One of the most important properties of semiconductor material is that its conductivity can be adjusted by adding dopants. Ion implantation, adding process by which dopant atoms are forcefully implanted into the semiconductor in terms of energetic ion beam injection, is the most common method in the ultra-large scale integration (ULSI) process technology. The purposes of the impurities doped into semiconductor devices are for channel doping to accurately control threshold voltage, lightly doped drain (LDD) regions to reduce leakage current and enhance reliability, and for forming ohmic contacts in the source and drain regions to reduce the resistance. Threshold voltage control is one of the most important factors for realizing complementary metal-oxide-semiconductor (CMOS) circuits. Precise control of the channel dosage is needed to obtain a low leakage current for low power consumption in CMOS circuits. Hot carriers in poly-Si TFTs degrade the device performance and the long-term stability. The LDD implantation step is performed between the source/drain regions and the channel to reduce the maximum electrical field near the edge of the drain junction regions and suppress the leakage current. The source/drain doping which the primary requirement is the high dose level for desired low source/drain resistance is probably the last doping process in poly-Si TFTs fabrication. Gate electrode or photoresist is used as the mask to cover the area that should not be doped. The masking layer should have the proper power to stop the penetration of the dopant. The photoresist mask requires special attention to stripe because it tends to harden due to the heat build-up during the implantation process. Key parameters for doping technique include precise dose and specie control, substrate temperature cooling, uniformity, and high throughput. Unlike the source/drain doping, the LDD and channel doping implantation are more challenging with more accurate dose control requirements for accurately control of the threshold voltage and the series resistance. It is therefore important to be able to maintain a dosage variation of smaller than 5% for this application in order to maintain good uniformity in device characteristics.

For millions of transistors fully functional working, dopants in the channel, LDD, and source/drain regions must all be well activated. The energetic dopant ions cause significant damage to the silicon crystal structure near the surface regions during ion doping process. Activation is a thermal heating process to repair the lattice damaged regions into single-crystal structure and to activate the dopants. Only when the dopant atoms are at the single-crystal lattice sites can they provide electrons and holes as the majority carriers for device application. It has been reported that device with thinner active layer displays higher driving current, lower off-state leakage current, reduced kink current, and superior short channel characteristics. However, the high parasitic resistance of the thin source/drain regions degrades device performance such as effective field-effect mobility and driving current. In ULSI silicon semiconductor processing, activation is performed by either furnace annealing or rapid thermal processing (RTP) at temperature above 900 ℃. However, the maximum fabrication process temperature of LTPS TFTs is restricted to the softening point of glass substrates ( ~ 600 ℃). Activation poses a considerable challenge to LTPS TFTs producers owing to the temperature limitations. Because of the temperature restriction and the thin active layer, the high series resistance from source/drain regions will degrade device performance. In order to achieve low sheet resistance, the dopants in the source and drain regions must be activated to a high degree. The efficiency of the activation is dependent upon the doped impurities, activation temperatures and activation durations. Basically, activation methods used in LTPS TFT technology include furnace annealing, rapid thermal annealing, and laser annealing.

The most common approach of dopant activation is furnace annealing. This process is typically carried out at 600°C for as long as tens of hours in nitrogen ambient. The long process time at low temperature is necessary in order to effectively activate the dopants while preventing the substrate free from warpage or damage. It is a technique of poor efficiency and low throughput for mass production.

Another concern for furnace annealing is the high thermal budget. The long-time furnace annealing process will cause severe dopant lateral diffusion which is intolerable for small geometrical transistors. Therefore, rapid thermal annealing (RTA) process is preferred for post-implantation annealing in the advanced fab. A RTA system can ramp up the temperature from room temperature to 900 ℃ in a very short time, typically within 10 seconds. The RTA process can precisely control temperature uniformity of the substrate and within substrate. At about 750 ℃, the single-crystal structure can be recovered and the dopant atoms will move to locate substitutional sites in about 1 second, with minimum lateral dopant diffusion. By processing at high temperatures while minimizing substrate damage, short process times, lower cost and high throughput can be achieved via RTA.

Since RTA method will also cause deformation of the glass substrate, laser annealing is the best candidate for dopant activation without substrate damage. Laser annealing process, the silicon is heated, melted and recrystallized without heating the substrate, can achieve the highest activation efficiency compared to the other methods. Despite the high efficiency, some damages to device may occur during laser irradiation, such as the gate metal damage. In addition, throughput may be another potential bottleneck to the mass production.

## 1.5 Motivation

Low-temperature poly-silicon (LTPS) thin film transistors (TFTs) have been succussfully applied to high-definition active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting displays (AMOLEDs) [1.119] - [1.120]. In addition, LTPS TFTs have great potential for flexible electronics, and 3D-ICs application. As compared to a-Si TFTs and organic TFTs (OTFTs), LTPS TFTs have higher mobility, better thermal reliability, and higher immunity to water and oxygen ambient. Therefore, LTPS TFTs have been attracted much attention for integration of both the the peripheral driving circuitry and active matrix pixel switching elements onto the single substrate to reduce the fabrication cost and improve the system reliability. Moreover, such integration contributes to shorten the product lead-time because lengthy development time of ICs can be eliminated. It is expected that the degree of circuit integration will continue to increase as TFT electrical characteristics are approaching to SOI devices, so that system-on-panel (SOP) will be realized. Moreover, SOP technology also has a great potential of integration of input function other than output function of display, which will pave the way for future displays. Although plasma hydrogenation is common method to passivate the defects in poly-Si film for improving further device performance, the essential solution to ultra-high-performance LTPS TFTs is to produce high-quality poly-Si thin film by elaborating the crystallization process. Among various crystallization technologies for preparing poly-Si thin films, excimer laser crystallization (ELC) are the most promising technology to produce high quality poly-Si thin films on foreign substrates at low temperature. Although high-performance LTPS TFTs have been fabricated by ELC, the average grain size is smaller than 1 μm, which results in an upper limitation of the field-effect mobility of LTPS TFTs. Table 1-1 shows the SOP technology roadmap where LTPS TFT performances and related processes are going on in the features [1.10]. In addition, the narrow laser process window and the non-uniform grain size distribution are noteworthy issues for ELC technology. As many previous researches have been reported, the grain size of the ELC poly-Si thin film is significantly dependent on the laser energy density. The fluctuation of pulse-to-pulse laser energy density, non-uniform laser beam profile, and non-uniformity of a-Si thin film thickness will result in a very non-uniform grain distribution as the laser energy density is controlled in the SLG regime. It is very undesirable for devices and circuits applications due to the device degradation and poor device-to-device uniformity. Thus, many laser crystallization methods have been proposed to solve the above problems by producing large grains with uniformly grain size distribution, including sequential lateral solidification (SLS), grain filters method, thin-beam direction crystallization, phase-modulated ELC, dual beam ELA, double–pulsed laser annealing, selectively floating a-Si active layer, and so on. However, some of them are not readily attached to the existing excimer laser annealing systems or are problematic for circuit layout due to the anisotropy of the grain boundary spacing. In this thesis, we propose three novel crystallization techniques, including bottom-gate structure, a-Si spacer structure, and pre-patterned a-Si spacer structure, to control large lateral grain growth in the device channel regions using excimer laser irradiation. These three crystallization methods are capable of fabrication ultra high-performance LTPS TFTs with excellent uniformity.

Besides promoting the material quality of poly-Si thin film, two novel modified device architectures with lateral grain growth are proposed to further improve the performance of LTPS TFTs based on bottom-gate structure. A self–aligned (SA) bottom-gate TFT with appropriate channel length has been fabricated by the simple ELC and backside exposure. As a result, besides the all advantages of BG LTPS-TFTs with lateral silicon grains, symmetrical electrical characteristics are also observed in SA BG LTPS-TFTs. On the other hand, novel high-performance LTPS TFTs with double-gate (DG) structure and controlled lateral grain growth have been demonstrated by excimer laser crystallization. The devices have a higher driving current, steeper subthreshold slope, superior short-channel effect immunity, and suppression of the floating-body effect.

A new and simple diode-pumped solid-state continuous-wave (CW) laser crystallization instead of excimer laser crystallization is proposed to produce lateral grain growth while maintaining high throughput via controlling the laser scanning speed and laser power. Both dopant activation and crystallization of a-Si thin films by CW laser annealing are studied. It is found that CW laser annealing is a low-thermal budget and high-efficiency activation method. Directional river-liked lateral Si grain growth with tens of micron and excellent crystallinity are obtained via CW laser crystallization. By analyzing the microstructure of poly-Si films, CW laser crystallization mechanism of a-Si films are identified.

## 1.6 Thesis Organization

In the first chapter of this thesis, we briefly review the revolution of Si-based TFTs, TFT structure, methods of preparation of poly-Si thin films. For realizing SOP applications, the advantage and necessity of artificially-controlled lateral grain growth by laser crystallization technology are discussed. In addition, we also suggest that self-aligned devices and double-gate structure can further improve the device characteristics.

In chapter 2, excimer laser crystallization (ELC) of a-Si thin films with bottom-gate (BG) structure was studied for the application of high-performance LTPS TFTs in detail. The microstructure of poly-Si thin film with bottom-gate structure was analyzed by several material analyses, including SEM, AFM, TEM, and the factors that affected the final lateral crystallization microstructure were also investigated, including thickness of a-Si thin film, thickness of gate dielectric, thickness of gate electrode, laser shot number, and laser energy density. The lateral grain growth mechanism was identified and the electrical characteristics of ELC LTPS TFTs with bottom-gate structure were then discussed. Moreover, the breakdown voltage and reliability are analyzed.

In chapter 3, a self–aligned (SA) bottom-gate TFT with appropriate channel length was demonstrated by the simple ELC and backside exposure. A self-aligned photolithography using the bottom-gate as an opaque mask is applied by backside exposure through the quartz substrate. From the optical microscope (OM) and SEM micrographs, the photo-resist is perfectly self-aligned to the bottom-gate regions. Electrical characteristics of the resulting devices were reviewed and placed emphasis on the improvement of device performance accompanying the symmetrical electrical characteristics and the all advantages of BG LTPS-TFTs with lateral silicon grains.

In chapter 4, we report the process and characteristics of ultra high-performance double-gate (DG) LTPS TFTs. The same advantage of high quality poly-Si films owing to the lateral grain growth in the channel region as the bottom-gate TFTs is obtained. The microstructure of poly-Si films and the completed device structure were analyzed by an analytical transmission electron microscopy (TEM). Both n-channel and p-channel LTPS TFTs were fabricated to investigate the relation between double gate operation conditions and resulting LTPS TFT performance and uniformity.

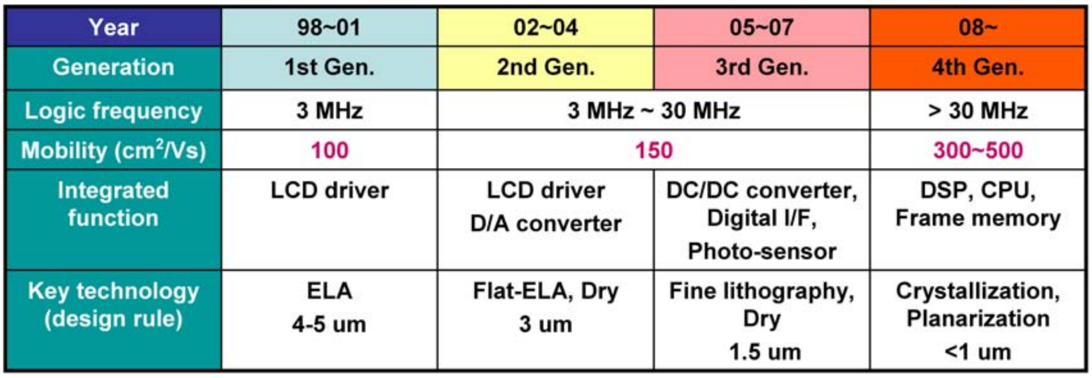
In chapter 5, a new and simple crystallization method to control lateral grain growth in the device channel region using excimer laser irradiation with a-Si spacer structure was proposed. The crystallization mechanism was presented. The results of crystallized poly-Si thin films were also analyzed by SEM and Raman spectrum and. The experimental results display that the resulting LTPS TFTs exhibit higher performance and better uniformity by using the new crystallization method.

In chapter 6, a novel crystallization technology for producing two-dimensional lateral grain growth, aiming at single-grain TFT, was demonstrated by excimer laser irradiation relying on spatially temperature distribution at artificially sites. The microstructure and quality of silicon grains were analyzed by SEM and TEM. The crystallization mechanism and grain boundary trap density were then presented. Not only high-performance poly-Si TFTs but also excellent device uniformity was achieved owing to the artificially-controlled lateral grain growth.

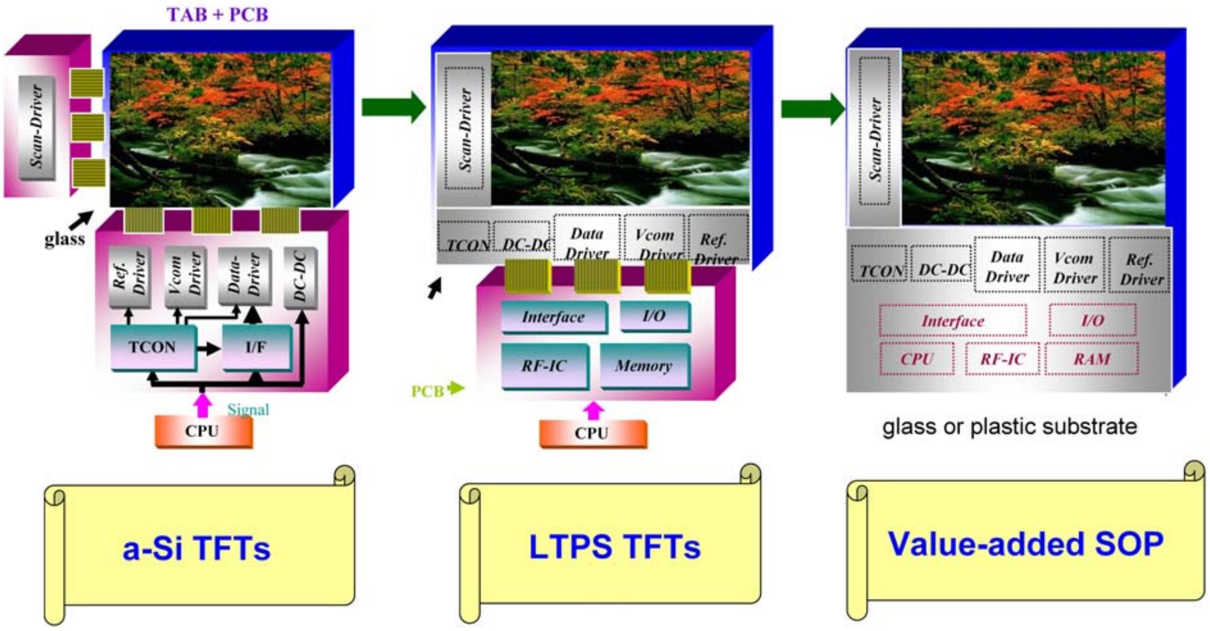
In chapter 7, a novel and simple diode-pumped solid-state continuous-wave (CW) laser crystallization was proposed to produce lateral grain growth for ultra high-performance LTPS TFTs. A comparison of the efficiency of dopant activation among various activation methods is studied. In addition, the CW laser-crystallized poly-Si thin film was analyzed by several material analyses, including SEM, Raman, AFM, TEM, and the factors that affected the final lateral crystallization microstructure were also investigated, including, laser scanning speed, laser power, and the ambient. By analyzing the microstructure of poly-Si films, CW laser crystallization mechanism of a-Si films are presented and the electrical characteristics of resulting LTPS TFTs were then discussed.

Finally, important summary and conclusions are given in chapter 8. Future works worthy of further research are recommended in chapter 9.

Table 1-1. The SOP technology roadmap where LTPS TFT performances and related processes are going on in the features.



| Year | 98~01 | 02~04 | 05~07 | 08~ |
|---|---|---|---|---|
| Generation | 1st Gen. | 2nd Gen. | 3rd Gen. | 4th Gen. |
| Logic frequency | 3 MHz | 3 MHz ~ 30 MHz | | > 30 MHz |
| Mobility ($cm^2/Vs$) | 100 | 150 | | 300~500 |
| Integrated function | LCD driver | LCD driver<br>D/A converter | DC/DC converter,<br>Digital I/F,<br>Photo-sensor | DSP, CPU,<br>Frame memory |
| Key technology (design rule) | ELA<br>4-5 um | Flat-ELA, Dry<br>3 um | Fine lithography, Dry<br>1.5 um | Crystallization, Planarization<br><1 um |



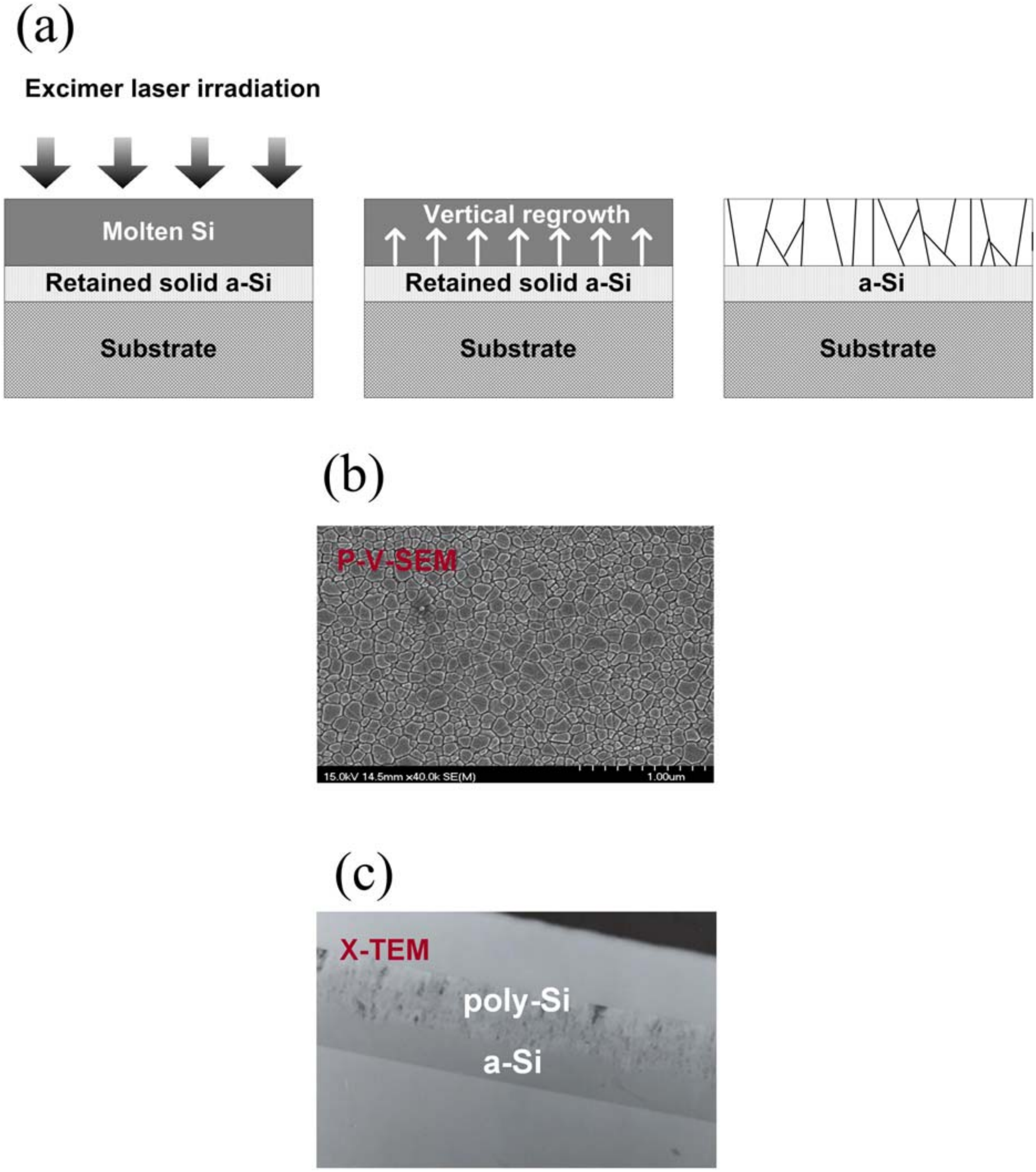


Figure 1-1. (a) The schematic illustration of the excimer laser crystallization mechanism of a-Si thin films in partial-melting regime. (b) The plane-view scanning electron micrograph (SEM) micrograph and (c) the cross-sectional transmission electron micrograph (TEM) of excimer-laser-crystallized poly-Si thin films in the partial-melting regime, respectively.

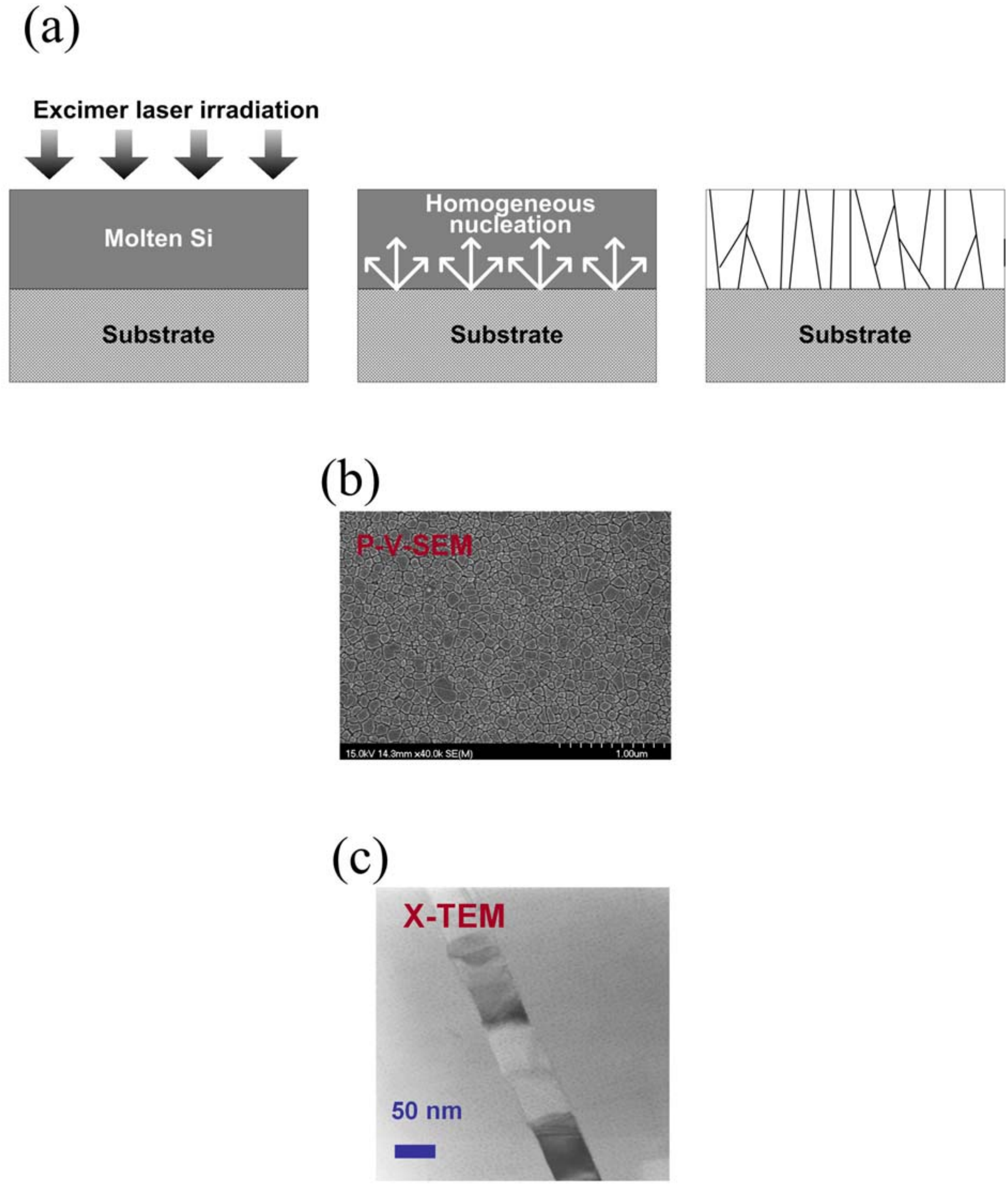


Figure 1-2. (a) The schematic illustration of the excimer laser crystallization mechanism of a-Si thin films in complete-melting regime. (b) The plane-view SEM micrograph and (c) the cross-sectional TEM of excimer-laser-crystallized poly-Si thin films in the complete-melting regime, respectively.

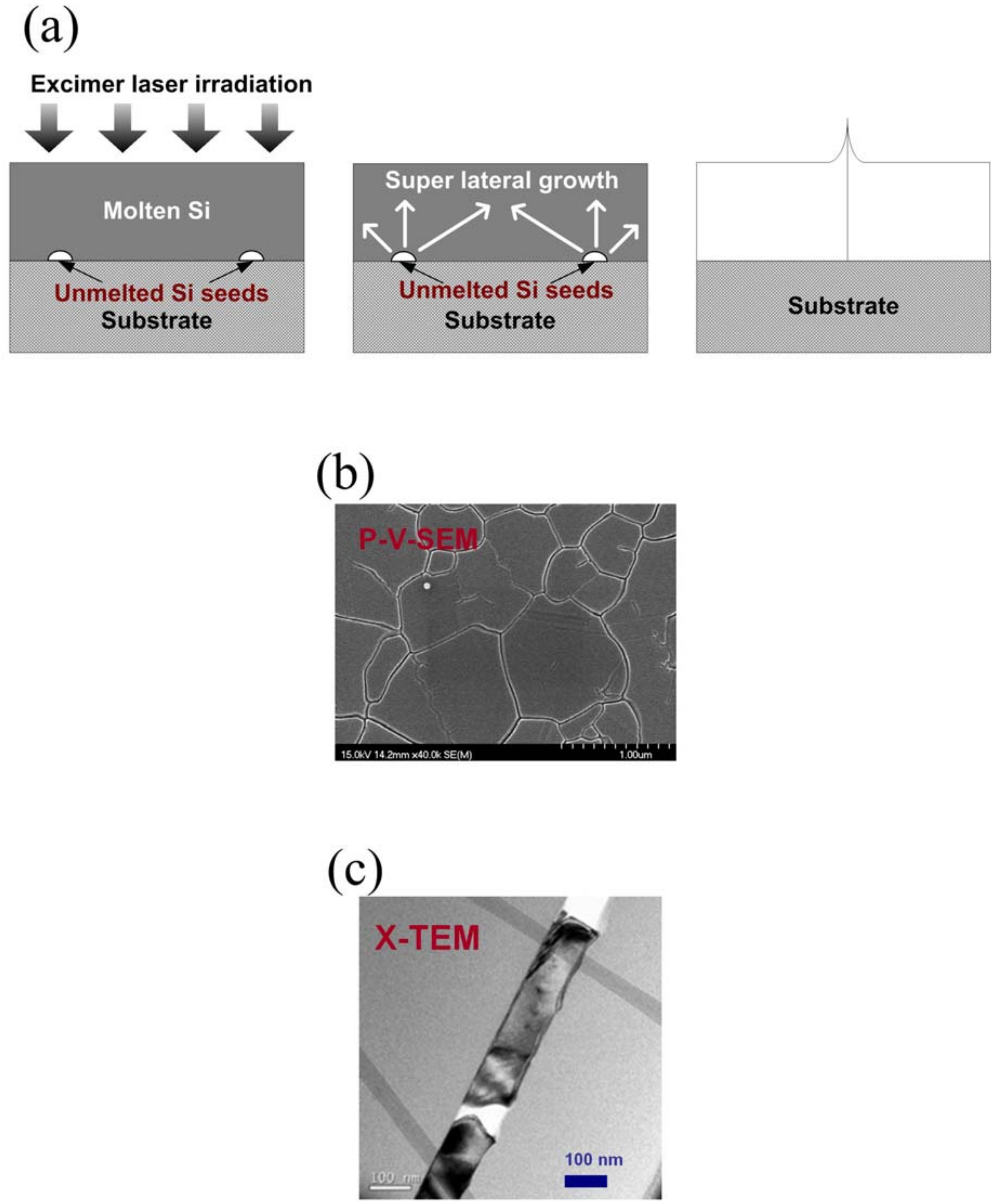


Figure 1-3. (a) The schematic illustration of the excimer laser crystallization mechanism of a-Si thin films in near-complete-melting regime. (b) The plane-view SEM micrograph and (c) the cross-sectional TEM of excimer-laser-crystallized poly-Si thin films in the near-complete-melting regime, respectively.

# Chapter 2

# High-Performance Low Temperature Polycrystalline Silicon Thin-Film Transistor Crystallized by Excimer Laser Irradiation with Bottom-Gate Structure

## 2.1 Introduction

Low-temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have been extensively studied for high-definition active matrix liquid crystal displays (AMLCDs), active matrix organic light emitting displays (AMOLEDs), and great potential for flexible electronics and 3-dimensional integrated circuits (3D-ICs) applications owing to their superior mobility performance [2.1] - [2.22]. As compared to amorphous silicon (a-Si) TFTs and organic TFTs (OTFTs), LTPS TFTs have higher mobility, better thermal reliability, and higher immunity to water and oxygen ambient. Therefore, LTPS TFTs have been attracted much attention for integration of both the the peripheral driving circuitry and active matrix pixel switching elements onto the single substrate to reduce the fabrication cost and improve the system reliability. Although passivation of the defects in poly-Si film is the common method to improve further device performance, the essential solution to ultra-high-performance LTPS TFTs is to produce high-quality poly-Si thin film by elaborating the crystallization process [2.23] - [2.29].

One common and simple approach to crystallize amorphous Si (a-Si) into poly-Si structure is solid phase crystallization (SPC) [2.30]. However, the conventional SPC suffer from long processing times of several tens of hours at temperature of 600°C and large defect density in the crystallized poly-Si thin films, which exclude it from high-performance TFT applications on glass or plastic substrates. Recently, metal-induced-crystallization (MIC) has been proved to produce large and uniform silicon grains with lower thermal budget as compared to SPC [2.31]-[2.36]. In spite of low crystallization temperature and high growth rate, metal contamination incorporated into the crystallized poly-Si thin films is a serious problem which resulted in poor TFT performance, such as high leakage current, large kink current, worse subthreshold swing, and poor device stability. As a result, among various crystallization technologies for preparing poly-Si thin films, laser crystallization (LC) are the most promising technology to produce high quality poly-Si thin films on foreign substrates at low temperature. Therefore, many researches of laser crystallization of amorphous silicon films for the preparation of poly-Si films for LTPS TFTs have been studied using various kinds of lasers techniques, such as $CO_2$, Ar, Nd:YAG, Nd:$YVO_4$, excimer, femosecond lasers, and etc [2.37]-[2.47]. Among these laser techniques, excimer laser crystallization (ELC), to date, is the widely used method to prepare poly-Si thin films because of its high pulsed-laser power for large area glass substrate and the large absorption coefficient for a-Si in the UV light region (optical absorption coefficient > $10^6$ $cm^{-1}$) for no damage to glass substrate. According to the mixture gas used in the laser tube, excimer laser radiation of output wavelengths between 157 - 351 nm (157, 193, 248, 308 and 351 nm for $F_2$, ArF, KrF, XeCl and XeF laser, respectively) by the transient high voltage discharge with a short pulse duration (full width of half maximum ~ tens of nanoseconds). The basic principle of excimer laser crystallization is the phase transformation of silicon thin film from amorphous to single-crystal material via melting the Si thin film within a very short time. Actually, the a-Si thin film is heated to the temperature of about 1200°C during laser irradiation. However, the high temperatures are only persistent for tens of nanoseconds during laser pulse duration. In consequence, the introduction of thermal damage to the glass substrate and the thermal compaction problem are relaxed, which are serious issues in the solid phase crystallization.

Another unique advantage of excimer lasers is the strong optical absorption of UV light in silicon. As a result, most of the incident laser energy is absorbed close to the surface of the thin film without causing severe thermal strain on the substrate. The unique advantages of strong optical absorption of the UV light in silicon and short pulse duration of the excimer laser imply that high temperature can be produced in the silicon surface region, causing rapidly melting and solidifying quickly, without significant heating the substrate and impurities contamination from the substrate diffusion into the silicon thin film. This technology yield high quality and large-grained poly-Si thin film for high-performance LTPS TFTs on glass or plastic substrate with high throughput.

Although high-performance LTPS TFTs have been fabricated by ELC, the average grain size is smaller than 1 μm, which results in an upper limitation of the field-effect mobility of LTPS TFTs [2.48]-[2.49]. In addition, the narrow laser process window and the non-uniform grain size distribution are noteworthy issues for ELC technology [2.50]-[2.51]. As many previous researches have been reported, the grain size of the ELC poly-Si thin film is significantly dependent on the laser energy density [2.52]-[2.53]. The fluctuation of pulse-to-pulse laser energy density, non-uniform laser beam profile, and non-uniformity of a-Si thin film thickness will result in a very non-uniform grain distribution as the laser energy density is controlled in the SLG regime. It is very undesirable for devices and circuits applications due to the device degradation and poor device-to-device uniformity. In addition, to realize system-on-panel (SOP), TFTs with high performance and good uniformity are essential to integrate the memory and controller with driver circuits on a single substrate [2.54]-[2.58]. Thus, many laser crystallization methods have been proposed to solve the above problems by producing large grains with uniformly grain size distribution, including sequential lateral solidification (SLS) [2.59]-[2.72], grain filters (μ-Czochralski) method

[2.73]- [2.80], thin-beam direction crystallization [2.81]-[2.82], phase-modulated ELC [2.83]-[2.91], dual beam ELA [2.92]-[2.93], double–pulsed laser annealing [2.94]-[2.96], capping reflective or anti-reflective layer [2.97]-[2.102], ELC of pre-patterned a-Si thin film [2.103]-[2.107], near-infrared femtosecond laser crystallization [2.43]-[2.45], comb-shaped beam ZMR-ELA [2.108]-[2.109], ELC of selectively floating a-Si active layer [2.110]-[2.115], heat retaining enhanced crystallization [2.116]-[2.117], CLC method using the diode-pumped solid-state continuous wave laser [2.118]-[2.134], and selectively enlarging laser crystallization (SELAX) [2.135]-[2.140], excimer laser crystallization with recessed channel [2.141]-[2.142], and so on [2.143]-[2.144]. Although large-grain poly-Si thin films can be produced by the above mentioned methods, some of them need additional masks or processes, some of them are problematic for circuit layout due to the anisotropy of the grain boundary spacing, and others are not readily to the existing excimer laser annealing systems, which result in the increase of the fabrication cost.

The bottom-gate structure, the gate electrode located below the semiconductor layer, is the most common configuration for a-Si TFTs due to the clean interface. As a result, if the bottom-gate is used for poly-Si TFTs, it offers some benefits over the top-gate structure for AMLCD applications. First, clean interface control can be easily achieved due to the ability to deposit the gate dielectric and silicon films sequentially in a single system without breaking vacuum. Second, the plasma hydrogenation diffusion rate in the bottom-gate TFT structure is significantly higher than that in top-gate TFT structure, because the channel thin film is not blocked by the gate-electrode thin films during hydrogenation passivation. Therefore, in the early stage of the development of LTPS TFTs, bottom-gate (BG) TFT structure was very attractive because the excimer laser annealing was thought as an additional process step to the a-Si TFTs. However, bottom-gate TFTs suffered from worse electrical performance than top-gate (TG) TFTs. The effective carrier mobility of bottom-gate TFTs is generally much lower than that of top-gate TFTs, because of the smaller poly-Si grain size and poor silicon grain quality produced resulting from the bottom-gate metal acting as a heat sink during excimer laser crystallization [2.145]-[2.146]. As a result, only a few studies have been conducted for bottom-gate TFTs with short channel length and top-gate TFTs have been widely adopted in AMLCDs for the last decade.

In this chapter, a novel and simple lateral grain growth method has been proposed using the conventional fabrication process of bottom-gate a-Si TFTs. In this method, the a-Si thin film with two kinds of thicknesses in a local region was formed by the deposition of a-Si on the plateau structure. When the excimer laser irradiation is applied on the a-Si thin film, the applied laser energy density is controlled to completely melt the thin region of a-Si film in the channel region but partially melt the thicker region of a-Si films near the edges of bottom gate. Therefore, a lot of un-melting solid seeds remain near the edges of bottom gate electrode and a lateral temperature gradient can be produced between the local thin and thick regions of a-Si film, and the lateral grain growth started from the un-melted silicon solid seed at the base neighbor to the bottom-gate corner, and extended toward the completely melted region until the solid-melt interface from opposite direction impinges. Consequently, large and uniform longitudinal grains could be formed in the device channel regions which lead to the improved TFT performance and uniformity. Moreover, ideally a single laser pulse is sufficient to induce the lateral grain growth and a wide laser process window is also shown in this method.

In this chapter, the concept of controlled lateral grain growth is first discussed. Then, the experimental details are described in detail. Next, the microstructure of ELC poly-Si thin film with bottom-gate structure is analyzed and the factors that affected the final lateral crystallization microstructure were also investigated, including thickness of a-Si thin film, thickness of gate dielectric, thickness of gate electrode, laser shot number, and laser energy density. The results of ELC BG LTPS TFT performance are presented and analyzed, demonstrating the performance and uniformity enhancement achieved by using the new crystallization method. Moreover, the breakdown voltage and reliability of BG TFTs are analyzed.

## 2.2 The Concept of Controlled Lateral Grain Growth with Bottom-Gate Structure

Large-grained poly-Si thin films always result in high-performance poly-Si TFTs due to the reduction of defect traps in the grain boundaries. Hence, enlarging grain size is the most effective method for improving the device performance. For realizing the SOP applications, it is essential not only to produce large silicon grains but also to control the locations of the grains and the grain boundaries, since it enables the realization of the high-performance LTPS TFTs with excellent device-to-device uniformity by precisely controlling the number and direction of grain boundaries in TFTs. For the formation of silicon grains at the desired position, it can be achieved by controlling the Si nucleation site at the selected region.

In order to induce lateral grain growth, a lateral temperature gradient must be created between the adjacent areas and there must be un-melted solid silicon seeds to act as the nucleation sites for lateral grain growth. If the laser fluence gradient is performed, the a-Si thin film is completely melted at the areas exposed to higher laser fluence and partially melted at the adjacent areas exposed to lower laser fluence. As a result, a large lateral temperature gradient will exist between the complete melting liquid-phase regions and un-melting solid-phase silicon seeds, and grains will grow laterally towards the complete melting regions from the un-melting solid silicon seeds. The lateral grain growth will eventually be arrested by either colliding with lateral grains grown from the other side or by spontaneous nucleation launched in the severely super-cooling molten silicon. Evidently, higher laser fluence gradient makes steeper temperature gradient resulting in a longer lateral grain growth. Because it takes a longer time for the hotter molten silicon region to cool down to the temperature of the spontaneous nucleation, the lateral grain growth can go on for a longer distance [2.147]-[2.148].

In this work, the a-Si thin film with two kinds of thicknesses in a local region was adopted to produce a local temperature gradient during the excimer laser irradiation. A schematic illustration of lateral grain growth mechanism using bottom-gate structure of a-Si thin film is displayed in Fig. 2-1. As the excimer laser irradiation is performed on the a-Si thin film, the applied laser energy density is controlled to completely melt the thin region of a-Si film but partially melt the thicker region of a-Si films near the edges of bottom gate. Therefore, a lot of un-melting solid seeds remain near the edges of bottom gate electrode and a lateral temperature gradient can be produced between the complete melting liquid-phase regions and un-melting solid-phase silicon seeds. The lateral grain growth started from the un-melted silicon solid seeds at the base neighbor to the bottom-gate corner, and extended toward the completely melted region until the solid-melt interface from opposite direction impinges. As the bottom-gate structure of a-Si thin film is formed artificially and the channel are properly designed, the lateral grain growth can be artificially controlled in the desired local region and the grain boundary perpendicular to the current flow in the channel region can be reduced. LTPS TFTs made by such crystallization method will exhibit higher performance and better uniformity.

## 2.3 Experiments

### 2.3.1 The Setup of Excimer Laser Crystallization System

Figure 2-2 shows the schematic illustration of excimer laser crystallization system. The laser light source of this system is KrF excimer laser, which output wavelength is 248 nm (Lambda Physik, LPX 210i series). The maximum laser output peak density is about 670 J/cm$^2$, the maximum frequency is 100 Hz, and the FWHM of the laser pulse is approximately 30 ns. In this work, the pulse laser is operated at a frequency of 10 Hz and the peak energy density at the substrate stage is below 600 mJ/cm$^2$. The long axis optical homogenizer and optical condensers are used to transform the original rectangular laser beam profile into the 22.5 mm × 2.0 mm laser beam spot with a spatial uniform top-hat profile for the long axis and a semi-Gaussian profile for the short axis at the working stage.

The sample is crystallized and scanned via laser beam overlapping on the x-y translation stage in a vacuum chamber. The overlap helps to improve the uniformity of laser-crystallized poly-Si thin films because the crystallinity of poly-Si film in the middle of the laser pulse is better than that in the edges of laser pulse. Crystallization of large area is achieved by moving the sample beneath the laser beam by controlling the movement of the x-y translation stage. The scanning direction is in the short axis direction. The velocity of the x-y translation stage during crystallization process can be adjusted depending on the laser shot number per unit area under determined operating laser frequency. In addition, the crystallization experiments can be performed at either room temperature or 400°C.

## 2.3.2 Sample Preparation for Material Analysis

Figure 2-3 shows the process procedures for the preparation of poly-Si thin films with bottom-gate structure crystallized by ELC. In order to prepare the sample for material analysis, the silicon dioxide ($SiO_2$) of 1 μm-thick was thermally growth on bare silicon wafers by vertical furnace after standard clean process. At first, a 1000 Å-thick in-situ doping poly silicon layer was deposited by decomposition of pure silane ($SiH_4$) and phosphine (PH3) with low pressure chemical vapor deposition (LPCVD) at 550°C on oxidized silicon wafer. After defining the bottom-gate region, the 1000 Å-thick and 500 Å-thick tetraethyl orthosilicate (TEOS) gate oxide layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 385°C. Then, after standard RCA clean process, the 1000 Å-thick and 500 Å-thick amorphous silicon (a-Si) layers were deposited by decomposition of pure silane ($SiH_4$) with LPCVD at 550°C. After standard RCA clean process, the a-Si thin films were then subjected to 248 nm KrF (Lambda Physik Excimer Laser LPX 210i) excimer laser crystallization (ELC). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to $10^{-3}$ Torr and the substrate was maintained at room temperature or 400 ℃. The laser beam was homogenized into a semi-gaussian shape in the short axis and a flat-top shape in the long axis. The number of laser shots per area was 1, 10, 20, and 100 (i.e. 0 %, 90%, 95 %, and 99 % overlapping), respectively. Several laser energy densities were also adopted in this work.

The relations between the resulting laser-crystallized poly-Si thin films with bottom-gate structure and laser process conditions were investigated by utilizing several material analysis techniques. They include scanning electron microscopy (SEM) analysis, atomic force microscopy (AFM) analysis, and transmission electron microscopy (TEM) analysis. SEM was utilized to analyze the grain size and grain structure under different laser process conditions. In order to facilitate the SEM observation, some samples were processed by Secco-etch before analysis [2.149]. Secco-etch etches the grain boundaries more quickly than the interior parts of the grains in poly-Si films. AFM was utilized to analyze the grain size and surface morphology of laser-crystallized poly-Si films. TEM was employed to analyze the microstructure and crystallinity of poly-Si films.

### 2.3.3 Fabrication of Bottom-Gate LTPS TFTs using ELC

Controlling of lateral grain growth at the desired region can be realized by manipulating the Si nucleation sites at the selected positions. As the concept of location-controlled lateral grain growth was applied to the fabrication of BG LTPS TFTs, large and uniform longitudinal grains could be formed in the device channel regions. If the channel length is properly designed, the lateral grain growth can be artificially controlled and only one grain boundary is perpendicular to the current flow in the channel region, which leads to the improvement of device performance and device-to-device uniformity.

The key processes for the fabrication of bottom-gate LTPS TFTs crystallized with ELC are illustrated in Figure 2-4. At first, a 1000 Å-thick in-situ doping poly silicon layer was deposited by decomposition of pure silane ($SiH_4$) and phosphine (PH3) with low pressure chemical vapor deposition (LPCVD) at 550°C on oxidized silicon wafer with thickness of 1 μm. After defining the bottom-gate region, the 1000 Å-thick and 500 Å-thick tetraethyl orthosilicate (TEOS) gate oxide layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 385°C. Then, after standard RCA clean process, the 1000 Å-thick and 500 Å-thick amorphous silicon (a-Si) layers were deposited by decomposition of pure silane ($SiH_4$) with LPCVD at 550°C. After standard RCA clean process, the samples were then subjected to 248 nm KrF excimer laser crystallization (ELC). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to $10^{-3}$ Torr and the substrate was maintained at room temperature. The laser beam was homogenized into a semi-gaussian shape in the short axis and a flat-top shape in the long axis. The excimer laser annealing was performed in the scanning mode with various laser energy densities and laser shot numbers per unit area to investigate the effects of laser annealing conditions on the performance of fabricated BG LTPS TFTs. After excimer laser crystallization, a phosphorous ion implantation with dose of $5\times10^{15}cm^{-2}$ was carried out to form source and drain regions. Then, the device active region was etched by transformer-coupled plasma reactive ion etching

(TCP-RIE). Next, a 3000 Å-thick TEOS passivation oxide layer was deposited by PECVD at 385°C and the implanted dopants were activated by thermal annealing at 600°C for 12 hours in the $N_2$ ambient. After contact hole opening by reactive ion etching, aluminum thin film with a thickness of 5000 Å was deposited by sputtering and Al metal pads were patterned to complete the fabrication of TFTs with bottom gate structure as shown in Fig 2-4 (d). Then, a 30-min sintering process was performed at 400°C in the $N_2$ ambient to reduce the contact series resistance of the source and drain electrodes. Finally, LTPS TFTs were passivated by 2-h $NH_3$ plasma treatment to further improve the device performance [2.23]-[2.24]. For the sake of comparison, the excimer-laser-crystallized LTPS top-gate (TG) TFTs with a channel thickness of 1000Å were also fabricated using the super lateral growth (SLG) laser annealing condition, shown in Figure 2-5.

Current-voltage (I-V) characteristics of the fabricated devices were measured using a semiconductor parameter analyzer of Agilent technologies 4156C. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of $I_{ds} = (W/L) \times 10^{-8}$ A at $V_{ds} = 0.1$ V. The field-effect mobility and subthreshold swing were extracted at $V_{ds} = 0.1$ V, and the $I_{on}/I_{off}$ current ratio was defined at $V_{ds} = 3$ V. A scanning electron microscopy (SEM) (S4700, Hitachi) was used to get the surface micrograph of poly-Si thin films after Secco-etch. An analytical field-emission transmission electron microscopy (TEM) (JEM-2100FX, JEOL Ltd.) was employed to analyze the microstructure and crystallinity of poly-Si film in the channel region and the completed BG TFT device. The cross-sectional TEM samples were prepared by focused-ion-beam (FIB) technique (Nova 200, FEI Company).

## 2.4 Results and Discussion

### 2.4.1 Material Characterization of ELC Poly-Si Thin Films with

## Bottom-Gate Structure

### 2.4.1.1 Scanning Electron Microscopy (SEM) Analysis

The micro-structural properties of the poly-Si thin films are of great interest for device applications. The grain size, quality of the grains, and the grain size distribution will have strong influence on the electrical characteristics of LTPS TFTs. In order to verify the phenomenon of lateral grain growth, the a-Si thin films with bottom-gate structure were subjected to single laser pulse. Figure 2-6 (a) ~ (c) show SEM micrographs of excimer laser crystallized poly-Si thin films with bottom-gate structure after Secco etching, in which the device channel length was 1.2 μm, 1.5 μm, 2.0 μm, respectively. The distances of the channels are indicated by the white lines. In this case, the laser shot number is single pulse and the poly gate thickness was 1000 Å. The laser energy density is 450 mJ/cm$^2$ and the substrate temperature is maintained at room temperature during laser irradiation. According to Fig. 2-6(a) and (b), it is observed that about longitudinal grains of 0.6 μm and 0.75 μm in length were formed in the channel regions, respectively. Besides, ideally single laser pulse was sufficient to induce the lateral grain growth via this new crystallization method. In order to induce lateral grain growth, a lateral temperature gradient must be created between the adjacent areas and there must be un-melting solid Si to act as the seeds for lateral crystallization. By completely melting the a-Si thin film in a certain region and partially melting the one at the adjacent area, a large lateral temperature gradient will exist between the complete melting liquid-phase region and un-melting solid-phase seeds, and grains will grow laterally towards the complete melting region from the un-melting solid seeds [2.53], [2.98], [2.147]. In this experiment, an a-Si thin film with two kinds of thicknesses in a local region was formed by the deposition of a-Si on the plateau structure. When the excimer laser irradiation is applied on the a-Si thin film, the applied laser energy density is controlled to completely melt the thin region of a-Si film in the channel region. Since the laser energy density is almost uniform in a local region, if the thickness of thick region of a-Si film near the edges of bottom gate is thick enough, the thick region of a-Si film is partially melted, and a lot of un-melting solid seeds remain near the edges of bottom gate electrode. Therefore, a lateral temperature gradient can be produced between the local thin and thick regions of a-Si film, and the lateral grain growth started from the un-melted silicon solid seed at the base of the bottom-gate corner, and extended toward the completely melted region until the solid-melt interface from opposite direction impinges. Via a proper excimer laser condition along with the a-Si step height beside the bottom-gate, a super lateral grain growth of Si was formed in the channel length plateau. Consequently, if the bottom-gate plateau were arranged in a proper distance, only single grain boundary perpendicular to the current flow can be artificially controlled in the device channel regions. It leaded to the enhancement of device performance, and the improvement of device uniformity.

It is evident that the laser density determined the extension of lateral grain growth and the lateral grain growth was limited by the spontaneous nucleation in the molten silicon. When a longer channel length was adopted for laser crystallization, the laser density had to increase high enough to make the longitudinal grains collide with those grown from the other side, otherwise, the complete-melting Si thin film is then followed by significant supercooling of the liquid before the occurrence of the transformation to the solid phase. Consequently, fine-grained and small-grained poly-Si thin films caused by spontaneous homogeneous nucleation would form in the area of the channel region, which was indicated in Fig. 2-6 (c). These small grains will degrade the device performance. As a result, by adopting a moderate length of bottom-gate, lateral grain growth formed in the desired channel region will result in high-performance LTPS TFTs, accompanying a wide laser process window.

The dependence of the lateral silicon grain structure on the applied laser energy shot number was investigated. The a-Si thin films with bottom-gate structure were subjected to constant laser energy density of 450 mJ/cm$^2$ and various laser shot numbers. Fig. 2-7 (a) ~ (c) show the SEM micrographs of poly-Si thin films irradiated by excimer laser shot number of 1 shot, 20 shots, and 100 shots, respectively, in which the device channel length was 1.5 μm. The similar lateral silicon grains with 0.75 μm in length formed in the channel region are all observed in these three different cases. In addition, the multiple shots of the laser pulse added to the first single shot hardly changed the size of the location-controlled silicon grains, and appear to hardly move the position of the high angle grain boundary in the middle of the channel region. On the other hand, the density of structural defects inside the silicon grain formed only by the single laser pulse was significantly reduced by the multiple shots ELC. It can be concluded that the lateral grain growth can be induced and the process throughput can be improved by using this new crystallization method with a single laser shot.

The dependence of the lateral silicon grain structure on the applied laser energy density was also investigated. Fig. 2-8 (a) ~ (c) show the SEM micrographs of poly-Si thin films irradiated by excimer laser shot number of 20 shots and the laser energy density of 430, 450, and 490 mJ/cm$^2$, respectively, in which the device channel length was 1.5 μm. As expected, when the laser energy densities are controlled to complete melt of 1000 Å-thick silicon thin film in the channel region but partial melting of the thicker a-Si film near the edge of the bottom-gate corner, there are always two columns of longitudinal grains colliding in the middle of channel region. As a result, if the channel length were adjusted in a moderate distance, lateral grain growth will be manufactured without any spontaneous nucleation as the applied laser density is beyond the fully melting threshold of the thin a-Si region. If spontaneous nucleation can be suppressed or delayed, the lateral grain growth will go on a longer distance, hence producing larger silicon grains. Higher local temperature in the completely melting region resulting from the high laser density implies that the corresponding longer time to reach the deeply supercoolong is required for spontaneous nucleation. From the SEM analysis results, the maximum achievable length of lateral grain growth using this crystallization method is about 0.85 μm.

The dependence of the lateral silicon grain structure on the gate oxide thickness was also investigated. Fig. 2-9(a) ~ (c) show the SEM micrographs of poly-Si thin films irradiated by excimer laser shot number of 20 shots and the gate oxide thickness of 30, 50, and 100 nm, respectively, in which the device channel length was 1.5 μm. The laser energy density is 450 mJ/cm$^2$ and the substrate temperature is maintained at room temperature during laser irradiation. As expected, there are two columns of longitudinal grains colliding in the middle of channel region. However, the density of structural defects inside the silicon grain formed by thinner gate oxide thickness is higher than that formed by thicker gate oxide thickness due to the rapid quenching rate of molten silicon. It is suggested that substrate heating during laser crystallization can produce larger lateral grain growth by prolonging the melting duration of the complete melting silicon.

The dependence of the lateral silicon grain structure on the bottom-gate thickness was also investigated. We used the thicker bottom-gate to increase the thickness of the corner region for the purpose of creating steeper lateral temperature gradient. Fig. 2-10 (a) ~ (c) show the SEM micrographs of poly-Si thin films irradiated by excimer laser shot number of 20 shots and the bottom-gate thickness of 100, 200, and 300 nm, respectively, in which the device channel length was 1.5 μm. The laser energy density is 450 mJ/cm$^2$ and the substrate temperature is maintained at room temperature during laser irradiation. It is found that the polycrystalline silicon films in the corner regions were ablated due to the thinning effect after laser irradiation, as shown in Fig. 2-10 (b) and (c). The higher thickness of bottom-gate caused the more serious thinning effect owing to the larger step height. Therefore, in order to prevent the thinning effect due to the step height, the bottom-gate thickness must be suitable chosen for laser crystallization.

### 2.4.1.2 Atomic Force Microscopy (AFM) Analysis

Figure 2-11 displays the AFM image of 1000 Å-thick poly-Si thin films with bottom-gate structure after laser crystallization, in which the device channel length is 1.5 μm. In this case, the laser shot number is 20 shots and the bottom-gate thickness is 1000 Å. The laser energy density is 450 mJ/cm$^2$ and the substrate temperature is maintained at room temperature during laser irradiation. The surface roughness of the poly-Si thin film becomes obviously and the grains can be apparently distinguished after laser irradiation due to the huge hillock formation at the grain boundaries, as shown in Fig. 2-11. The hillock is attributed to the freezing of capillary waves excited in the melting silicon during laser crystallization [2.150]. According to the report of D. K. Fork et al, the 10% density change between solid and liquid phases of silicon, (2.53 g/cm$^3$ for the liquid and 2.30 g/cm$^3$ for the solid) provides a driving force for the creation of capillary waves in the conventional laser crystallized silicon thin films. Solidifying silicon will expand and exert a positive force on the adjacent melt [2.150]. Grain boundaries and vertices, in which typically are the last to freeze during lateral grain growth, have accumulated silicon due to the action of the expanded solid material on the remaining liquid material. Large and longitudinal grains with 0.75 $\mu$m in length are formed and only one high angle grain boundary is formed in the middle of the device channel region, which can be identified in the AFM image.

### 2.4.1.3 Transmission Electron Microscopy (TEM) Analysis

The micro-structural properties of laser-crystallized poly-Si films with bottom-gate structure such as the grain size, inter-grain defect density, intra-grain defect density, and grain orientation can be identified by using transmission electron microscopy (TEM) and its selected-area electron diffraction patterns. Figure 2-12 displays the cross-sectional TEM image of 1000 Å-thick poly-Si thin films with bottom-gate structure after laser crystallization, in which the device channel length is 1.5 μm. In this case, the laser shot number is 100 shots and the bottom-gate thickness is 1000 Å. The laser energy density is 450 mJ/cm$^2$ and the substrate temperature is maintained at room temperature during laser irradiation. According to the TEM image, there are two large silicon grains formed in the channel region above the bottom-gate electrode and the high angle grain boundary can be artificially controlled in the middle of the channel region. In addition, the cross-sectional TEM image in Figure 2-12 displays the clear interfaces between the bottom-gate oxide and poly-Si active layer. The interface between the bottom-gate electrode and bottom-gate oxide is also clear, implying that both the gate oxide and the bottom-gate electrode are not damaged during excimer laser irradiation. From the correlated selected-area diffraction pattern of poly-Si thin film, the crystallinity of the silicon grain silicon can be investigated. It is found that as the poly-Si grain formed in the channel region is selected, the electron diffraction pattern exhibits a clear dot pattern, which means the crystallinity inside the silicon grain is excellent. While the poly-Si grain near the corner region is selected, the electron diffraction pattern reveals the ring construction, which means the small grains exhibit poor crystallinity. Because the corner regions will act as the source/drain region of TFTs with heavily doped, the poor crystallinity of small grains will not degrade the performance of LTPS-TFTs.

#### 2.4.1.4 Secondary Ion Mass Spectroscopy (SIMS) Analysis

From the TEM analysis, both the gate oxide and the bottom-gate electrode are not damaged during excimer laser irradiation. However, phosphorous atoms in the doped bottom-gate electrode may out-diffuse into the poly-Si channel and gate oxide owing to the local high temperature during excimer laser irradiation. Secondary ion mass spectroscopy

(SIMS) measurement is performed to investigate the phosphorous depth profiles of the excimer laser-crystallized poly-S thin films, the bottom-gate gate oxide, and the bottom-gate electrode as a function of laser energy densities. Figure 2-13 shows the element depth profiles of the excimer laser-crystallized bottom-gate TFTs. The SIMS phosphorous depth profile after excimer laser irradiation at 390 mJ/cm$^2$ is the same to that as-implanted one. Even high excimer laser energy density of 490 mJ/cm$^2$ is performed to crystallize the a-Si thin films; the phosphorous depth profile is not altered as compared to that before laser annealing. It is also found that the secondary counts of phosphorous atoms in the poly-Si channel and gate oxide are two and three order magnitude smaller than those in the bottom-gate electrode. The SIMS results indicate that there are no harmful effects caused by the excimer laser crystallization of a-Si films with bottom-gate structure. Because the out-diffusion phenomenon of phosphorous atoms in the bottom-gate electrode into the poly-Si active channel and bottom-gate oxide during excimer laser irradiation is not observed, the electrical characteristics of BG TFTs will not be degraded.

### 2.4.2 Electrical Characteristics of LTPS TFTs Fabricated Using Excimer Laser Irradiation with Bottom-Gate Structure

For comparison, the conventional ELC TG LTPS TFTs with a thickness of 1000Å are also fabricated. In order to obtain high-performance TG LTPS TFTs, the laser density is controlled in SLG regime to obtain a large-grained poly-Si thin film. Fig. 2-14 (a) depicts the typical transfer characteristics for LTPS BG-TFTs with lateral silicon grains and conventional TG ones with W = L = 1.5 μm at drain voltages ($V_{ds}$) of 0.1 and 3 V. High-performance BG LTPS TFT with field effect mobility of 330 cm$^2$/Vs can be achieved using this crystallization method attributed to the high-quality poly-Si thin film in the device channel region while the mobility of the conventional TG-TFT counterpart is about 130 cm$^2$/Vs. Since the lateral grain growth can be artificially controlled in the channel region of BG TFTs and only one high angle grain boundary perpendicular to the direction of current flow is formed in the middle of the channel region, high on/off current ratio (> $10^8$), and low subthreshold swing are also exhibited in proposed BG devices. The high field-effect mobility is attributed to the high quality poly-Si thin films with reduced grain boundaries in the BG device channel region. It is well known that deep density of trap state and tail density of trap state in the grain boundaries put a negative influence on mostly all aspects of device performance including an increase in threshold voltage, a decrease in mobility, a decrease in subthreshold slope, a raise in leakage current, and worse device stability. The higher threshold voltage and lower mobility indicate that the devices whose channels have more defects require large gate voltage in order to fill the great number of trap states before the device can turn on. On the other hand, after trapping the free carriers in the grain boundaries, the defect states become electrically charged and created a potential energy barrier, which act as potential barriers during carrier transport from drain to source [2.151]. Table 2-1 lists several important electrical characteristics of these two different TFT structures. Fig. 2-14 (b) shows the output characteristics of proposed BG TFT and conventional TG one. In order to avoid the threshold voltage difference, the applied gate driving voltages in Fig. 2-14 (b) are kept at constant values of |Vg-Vth| = 4V, 8V, 12V, and 16V, respectively. It is demonstrated that BG TFTs with location-controlled silicon grains structure exhibit higher driving current than conventional ELC TG TFTs under the same bias condition owing to the high field effect mobility. In addition, according to the SEM image in Fig. 2-6 (a), a single laser shot is sufficient to induce the lateral grain growth of silicon grains for confirming our proposed crystallization method, although the BG TFTs are fabricated with 20 laser shots per area in order to further improve the poly-Si films quality by reducing the density of structure defects inside the lateral silicon grains formed in the channel regions. Consequently, the fabrication process throughput of this new crystallization method is much higher than of the conventional ones.

Figure 2-15 displays the dependence of field effect mobility on the device dimension for proposed BG TFTs and conventional TG ones. Twenty TFTs were measured with optimal laser irradiation condition for maximum field-effect mobility to investigate the device-to-device uniformity. The vertical bars in the figure indicate the minimum and maximum characteristic values attained at the specific laser energy density, and the solid symbols are the average calculated characteristic values. The mobilities of proposed BG TFTs and conventional TG ones increase as the channel length decreases, indicating that the grain boundaries perpendicular to the direction of current flow act as strong trapping centers which degrades the performance of TFTs resulting from grain boundary potential barrier height [2.152]-[2.154]. It is noted that higher field-effect mobility and smaller variation of field effect mobility are achieved at the same time for BG TFTs as compared with the TG TFTs, especially in the small device dimension below W/L = 2μm. The large dispersion of mobility for TG TFT is due to the random grain size distribution controlled in SLG regime, while for the BG TFTs, good uniformity of field effect mobility is attained because the grain boundaries in the channel region are controlled and reduced.

Figure 2-16 displays the dependence of field effect mobility on laser energy densities for proposed BG TFTs and conventional TG ones whose channel length is 1.5 μm. Twenty TFTs were measured for each laser irradiation condition to investigate the device-to-device uniformity. Compared to the conventional ELC TG-TFTs, it was found that ELC BG-TFTs with lateral silicon grains exhibited smaller electrical deviation since the number of spontaneous small grains and grain boundaries were reduced and the uniformity of TFTs performance could be improved with artificially lateral grown grains in the channel regions.

Figure 2-17 (a) displays the transfer characteristics of the n-channel LTPS BG-TFTs with lateral silicon grains and conventional TG ones with W = L = 1.5 μm and gate oxide thickness of 500 Å or 1000 Å at drain voltages ($V_{ds}$) of 0.1 and 3 V. It is as expected that proposed BG

TFTs with 50 nm gate oxide exhibit smaller threshold voltage, higher transconductance, and steeper subthreshold slope as compared to BG TFTs with 100 nm gate oxide owing to the thiner oxide integration for larger gate-to-channel capacitance. Some important electrical characteristics of LTPS TFTs are also listed in Table 2-2. In addition, high field-effect mobility of 323 $cm^2$/V-s and high on/off current ratio of $9.5 \times 10^8$ are demonstrated in the proposed BG TFTs with 50 nm gate oxide owing to the large silicon grains grown in the channel regions as compared to TG ones with 50 nm gate oxide. Figure 2-17 (b) displays the output characteristics of the n-channel LTPS BG-TFTs with lateral silicon grains and conventional TG ones with W = L = 1.5 μm and gate oxide thickness of 500 Å or 1000 Å. In order to avoid the threshold voltage difference, the applied gate driving voltages are kept at constant values of |Vg-Vth| = 4V, and 8V, respectively. It is demonstrated that poly-Si TFTs with location-controlled silicon grains structure and thinner gate oxide provide higher driving current and better saturation current than conventional ELC TG poly-Si TFTs due to the higher transconductance. Take the |Vg-Vth| = 8 V as an example, the current drivability of ELC BG poly-Si TFTs with 50 nm gate oxide is about 1.75 times as large as that of an ELC TG one with 50 nm gate oxide and 2.71 times as large as that of a ELC TG one with 100 nm gate oxide under the same bias condition. Besides the improvement of device performance and uniformity, the BG-TFTs with lateral silicon grains exhibit better reliability than TG-TFTs. Figure 2-18 (a) exhibits the gate-breakdown field strength of two different TFT structures with 500 Å-thick TEOS gate oxide. Figure 2-18 (b) shows the statistical distribution of the gate-breakdown voltage of two different TFT structures with 500 Å-thick TEOS gate oxide. As compared to TG TFTs, proposed BG TFTs show a tighter distribution of gate-breakdown voltage. Bottom-gate TFTs exhibit higher breakdown field strength and tighter parameter distribution than top-gate ones owing to the smooth interface of bottom-gate devices, which is shown in Fig. 2-12. Because the focus-ion-beam prepared (FIB-prepared) TEM sample is thin enough, the lacey support film beneath the BG device are seen through on the finer copper grids. The cross-sectional TEM image reveals that a flat interface morphology between the gate dielectric and poly-Si channel films in the bottom-gate TFTs. The protruded grain boundaries due to the freezing of capillary waves excited in the silicon melt during the crystallization profoundly affect the reliability and gate dielectric integration of TG poly-Si TFTs [2.155]-[2.157]. The improved breakdown and driving characteristics imply that the proposed BG-TFT structure is more suitable for device-size scaled-down application.

## 2.5 Summary

A new crystallization technology for producing lateral silicon gains has been developed by excimer laser irradiation with bottom gate structure. The mechanism of lateral grain growth using plateau structure of a-Si thin film with excimer laser crystallization is based on the spatial thermal gradient. The microstructure of poly-Si thin film with bottom-gate structure was analyzed by several material analyses, including SEM, AFM, TEM, and the factors that affected the final lateral crystallization microstructure were also investigated, including thickness of a-Si thin film, thickness of gate dielectric, thickness of gate electrode, laser shot number, and laser energy density. It can be observed that the large longitudinal grains artificially grown measuring about 0.85 μm were observed in length in the device channel region, while small and fine grains are located near the edges of the bottom-gate electrode. According to the TEM images, not only the interface between the poly-Si channel and bottom-gate oxide but also bottom-gate electrode and bottom-gate oxide is clear, implying that both the gate oxide and the bottom-gate electrode are not damaged during excimer laser irradiation. From the correlated selected-area diffraction pattern of poly-Si thin film, it is found that the crystallinity of the silicon grain silicon in the channel region is excellent. Moreover, the process window could be broadened because the laser energy densities were easier to be controlled for the wider laser energy density range. Therefore, the improved uniformity of TFTs performance is attained due to large silicon grains. In consequence, not only high-performance n-channel LTPS TFTs with field-effect-mobility exceeding 330 $cm^2/Vs$ in 1.5 μm design rule, but also excellent uniformity of device performance are also demonstrated owing to the artificially-controlled lateral grain growth in the device channel regions. The process steps in these technologies are highly compatible with the conventional commercial a-Si TFTs. Moreover, the experimental results revealed higher breakdown voltage and better reliability due to the smooth interface between gate dielectric and poly-Si channel films as thinner gate oxide were employed. LTPS BG-TFTs with lateral silicon grains are therefore promising for future SOP and AMOLED applications.

**Table 2-1**

Measured electrical characteristics of bottom-gate LTPS TFTs and conventional top-gate ones.

| TFT structure | Threshold Voltage (V) | Field-effect Mobility (cm2/V-s) | Subthreshold Swing (V/dec) | On/Off Current Ratio |
|---|---|---|---|---|
| Conventional TG (W=L=1.5 μm) | -1.17 | 130 | 0.345 | 4.32 x$10^7$ |
| **Proposed BG (W=L=1.5 μm)** | **-1.38** | **330** | **0.244** | **4.56× $10^8$** |

**Table 2-2**

Measured electrical characteristics of bottom-gate LTPS TFTs and conventional top-gate ones.

(W = L = 1.5 μm and gate oxide thickness of 500 Å or 1000 Å.)

| TFT Structures (W=L=1.5 um) | Threshold Voltage (V) | Field-effect mobility (cm$^2$/Vs) | Subthreshold Swing (V/dec) | Gm (us) @Vds=0.1V | On/off current ratio |
|---|---|---|---|---|---|
| Proposed BG TFT (50 nm oxide) | -0.88 | 323 | 0.224 | 2.20 | 9.5x $10^8$ |
| Conventional TG TFT (50 nm oxide) | -0.42 | 117 | 0.230 | 0.84 | 6.1x $10^7$ |
| Proposed BG TFT (100 nm oxide) | -1.68 | 362 | 0.251 | 1.25 | 5.8x $10^8$ |
| Conventional TG TFT (100 nm oxide) | -1.13 | 162 | 0.256 | 0.56 | 9.4x $10^7$ |

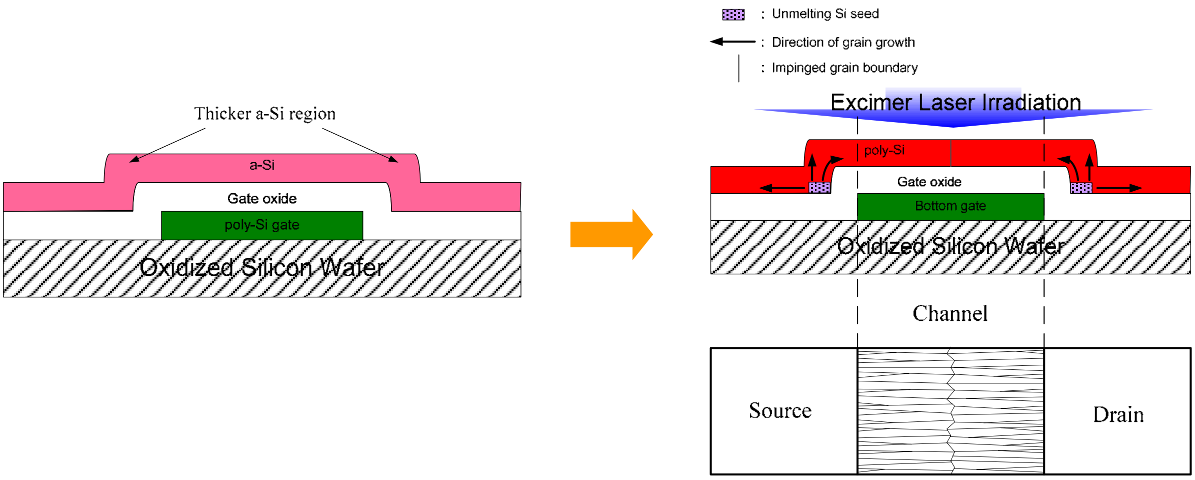


Figure 2-1. The schematic illustration of the mechanism of lateral grain growth using bottom-gate structure of a-Si thin film.

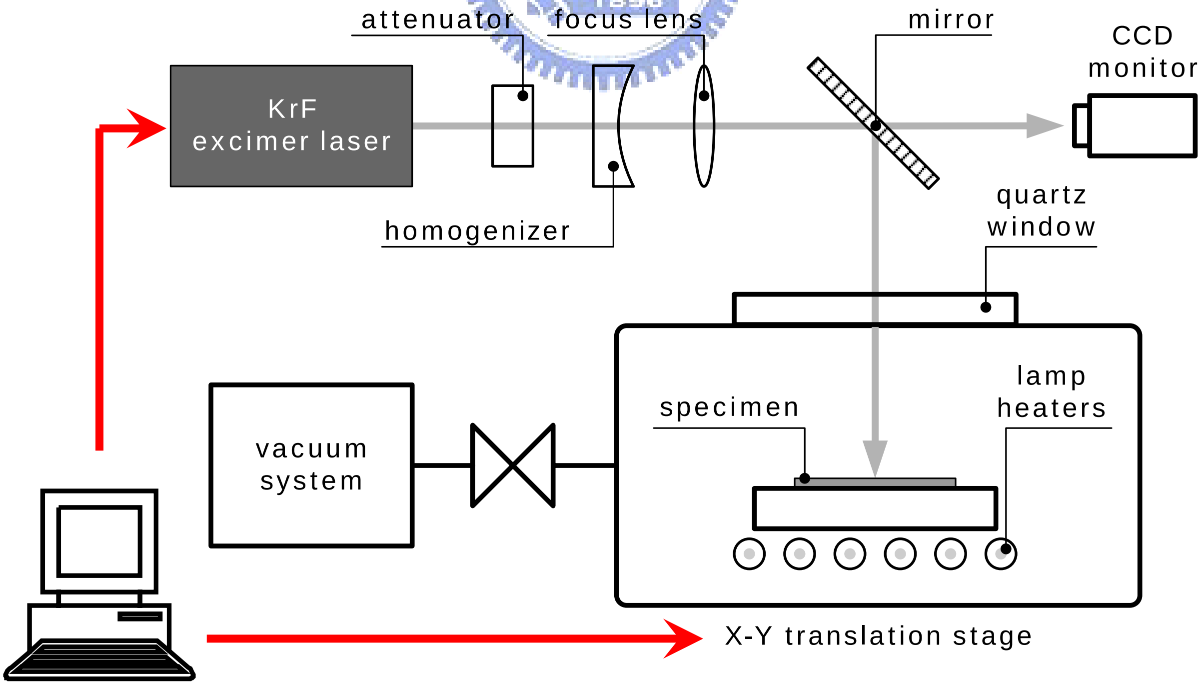


Figure 2-2. The schematic illustration of excimer laser crystallization system.

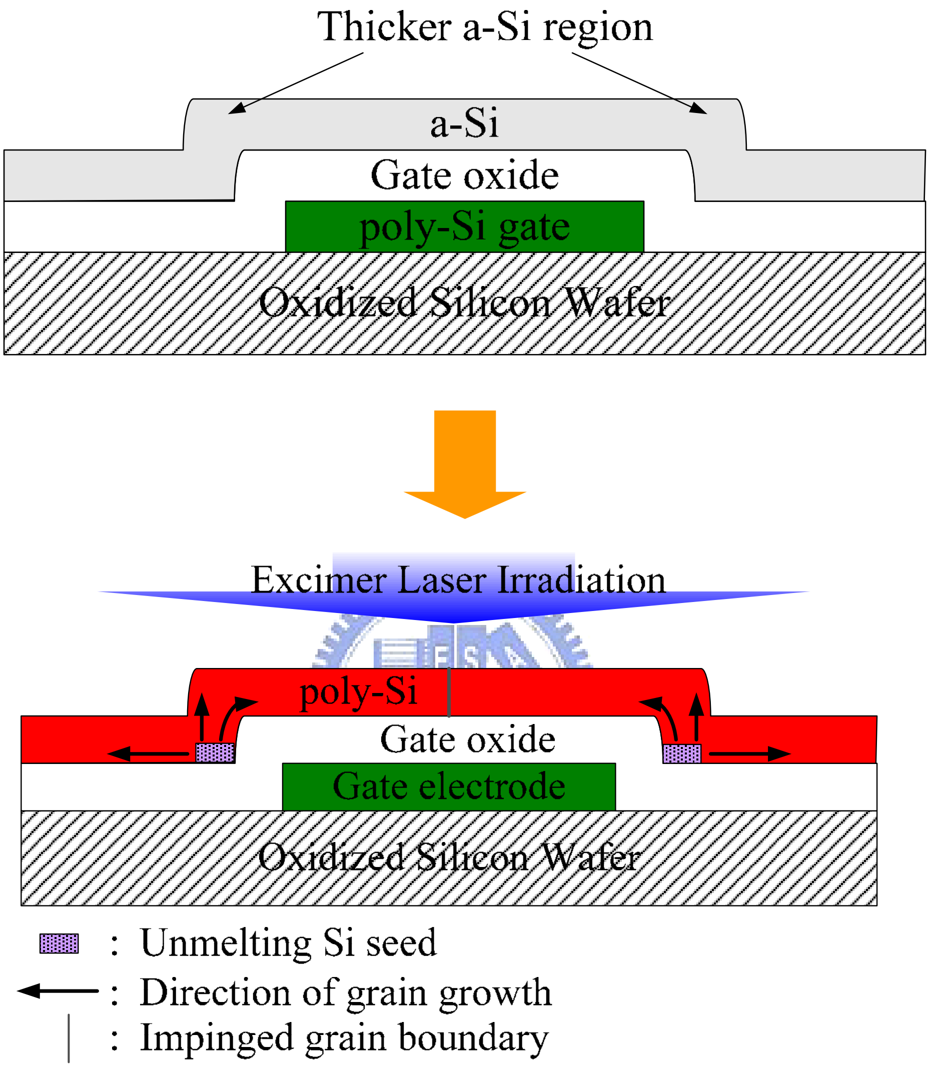


Figure 2-3. The process procedures for the preparation of poly-Si thin films with bottom-gate structure crystallized by ELC.

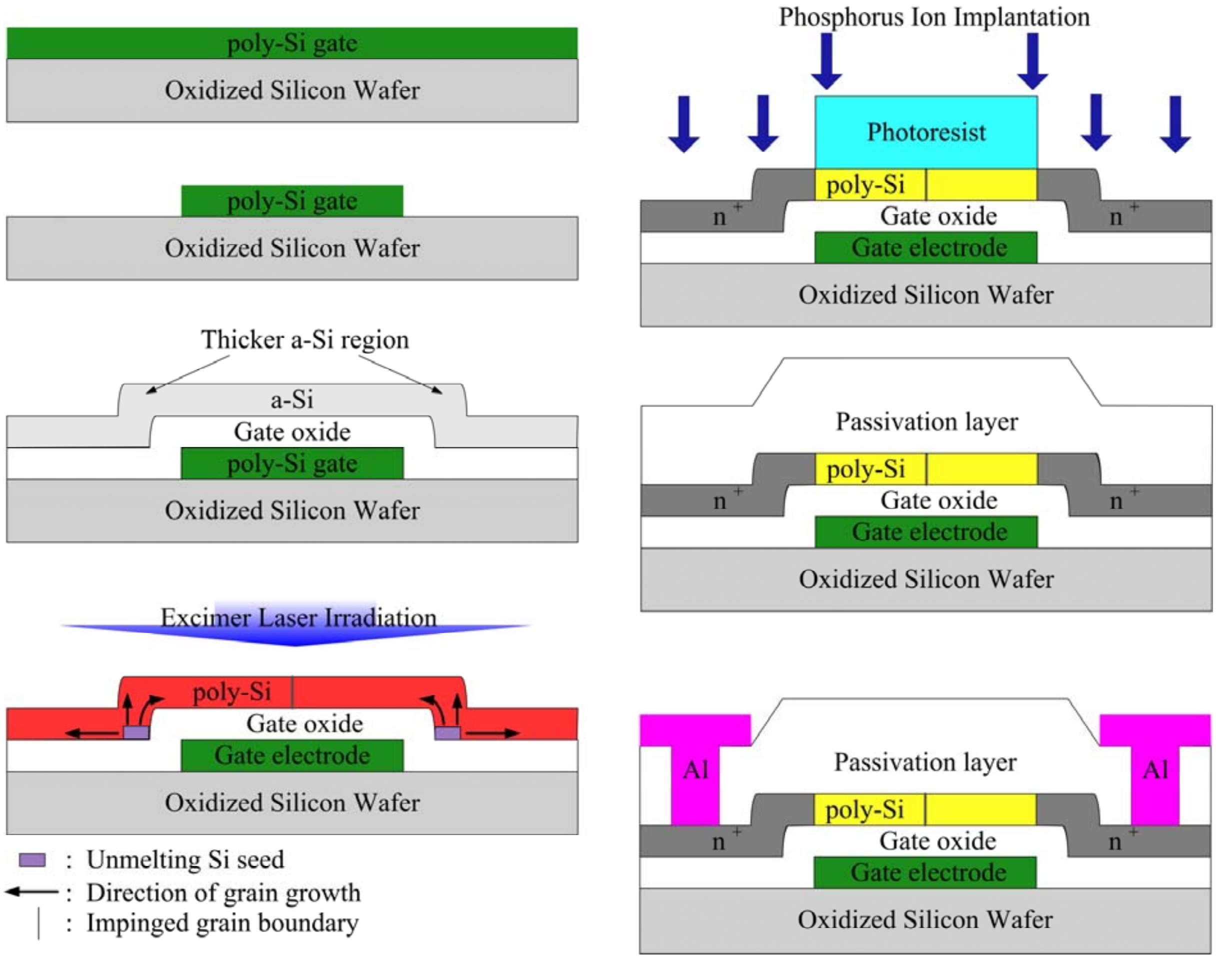


Figure 2-4. The key processes for fabricating short channel bottom-gate LTPS TFTs with excimer laser annealing.

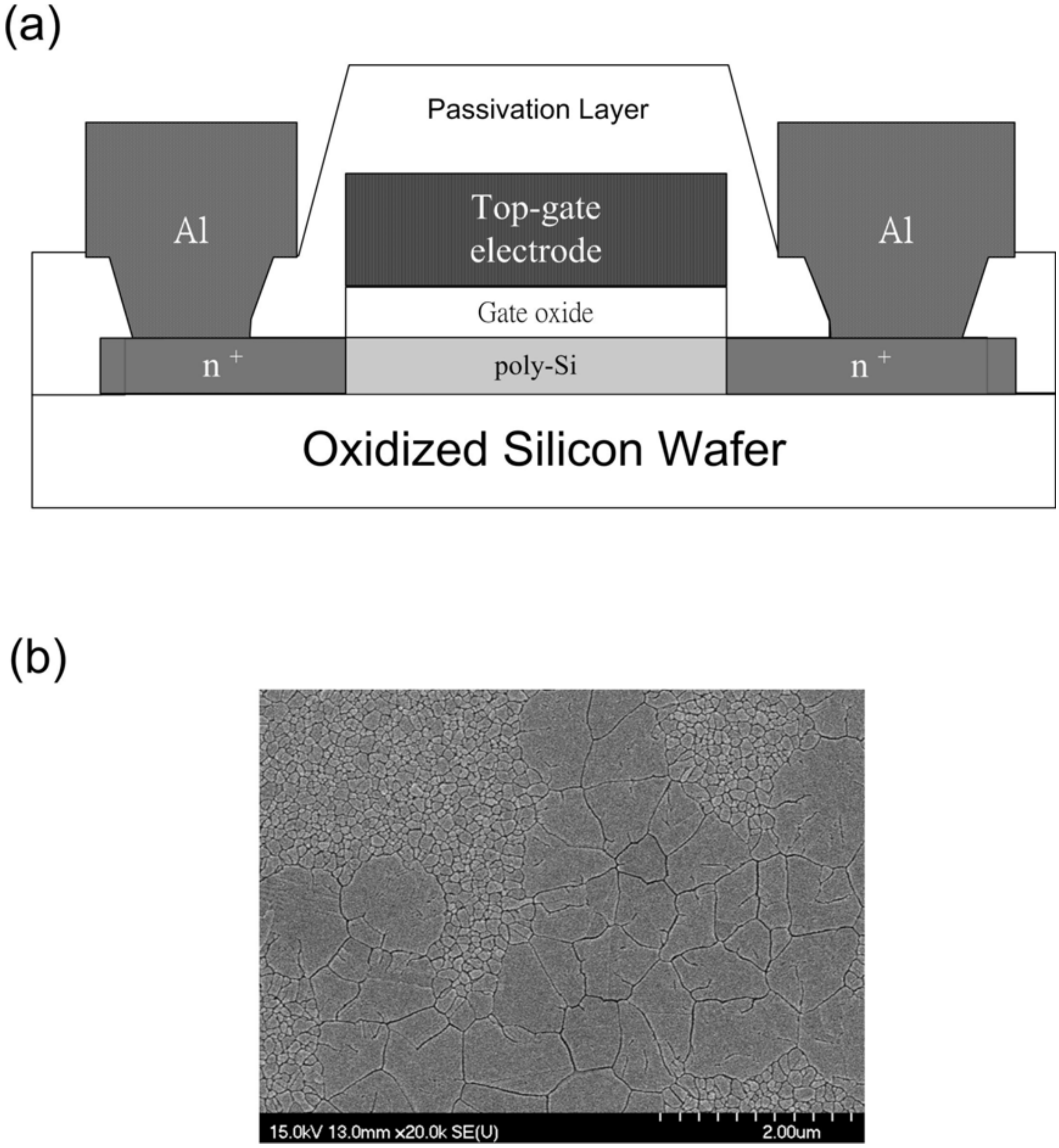


Figure 2-5. (a) The schematic cross-sectional drawing of conventional top- gate LTPS TFTs using the super lateral growth (SLG) excimer laser annealing condition. (b) Plane-view SEM micrograph of excimer laser crystallized poly-Si thin film with SLG laser annealing condition after Secco-etch.

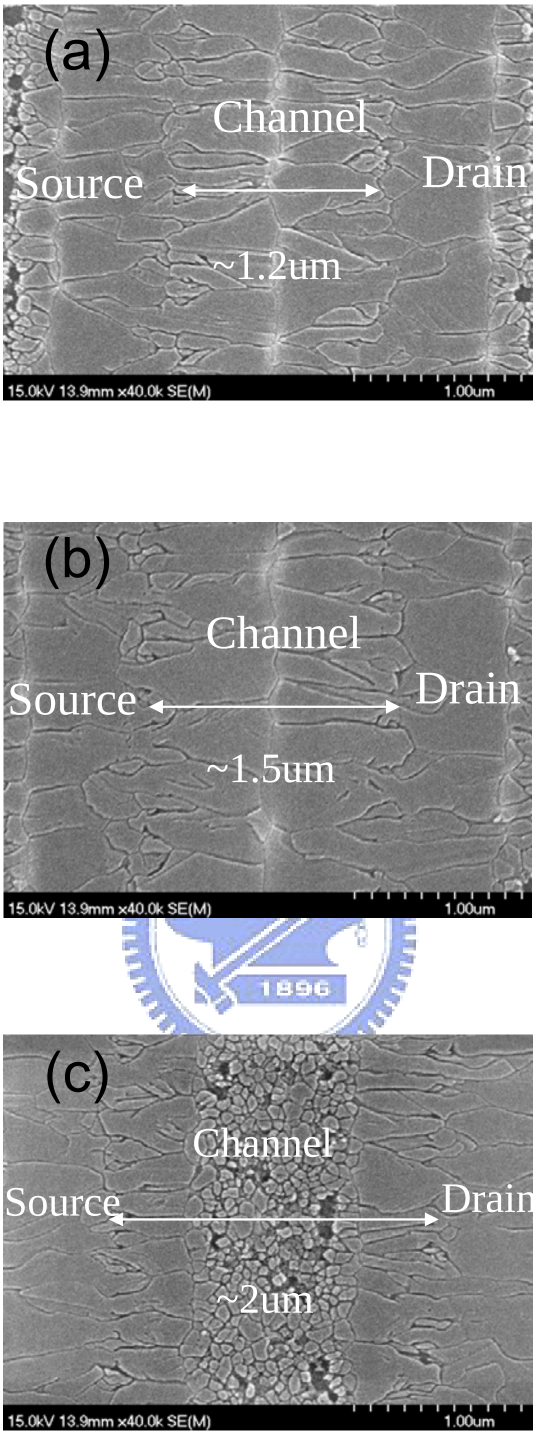


Figure 2-6. The SEM micrographs of excimer laser crystallized poly-Si thin films with bottom-gate structure after Secco etching, in which the device channel length was (a) 1.2 μm, (b) 1.5 μm, and (c) 2.0 μm, respectively. In this case, the laser shot number is single pulse and the poly gate thickness was 1000 Å. The laser energy density is 450 mJ/cm$^2$.

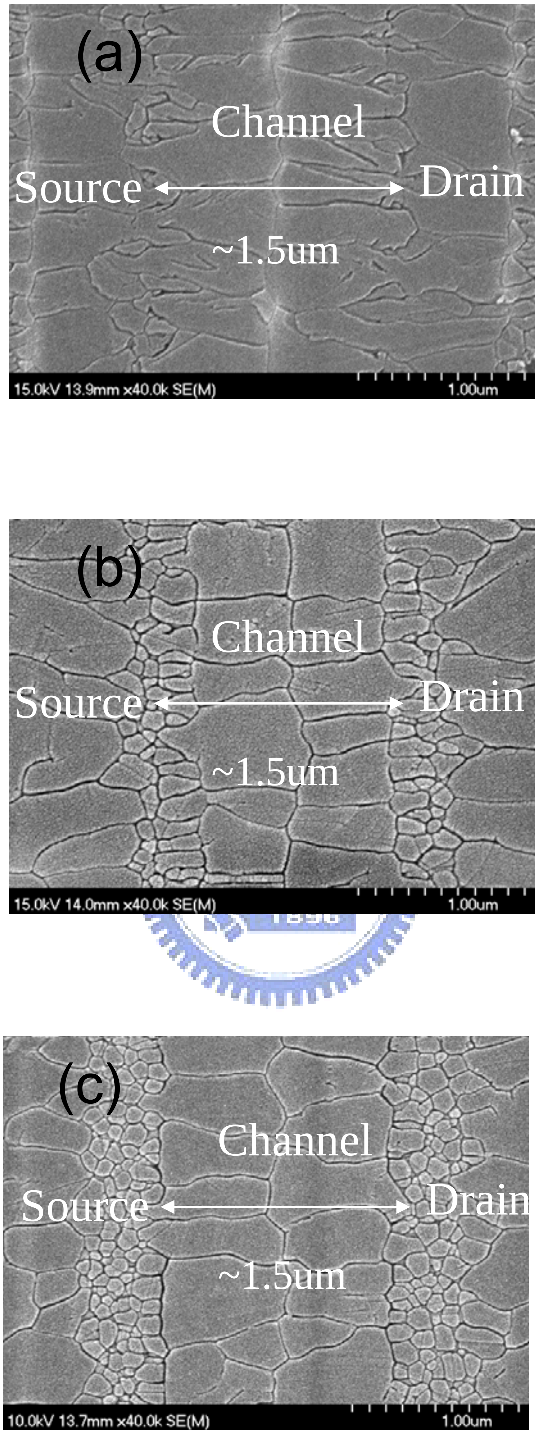


Figure 2-7. Scanning electron microscope micrographs of excimer laser crystallized poly-Si thin film with bottom-gate structure after Secco-etch, in which the device channel length was 1.5μm, and the laser shot number was (a) 1shot, (b) 20 shots, and (c) 100 shots, respectively.

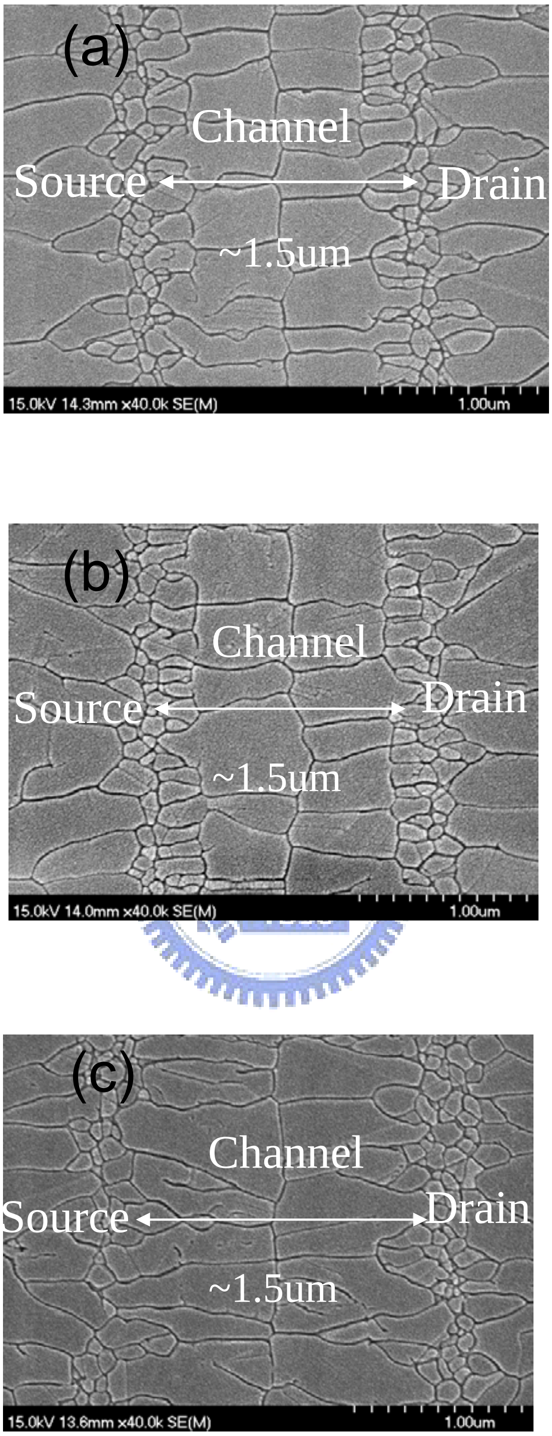


Figure 2-8. Scanning Electron Microscope micrographs of excimer laser crystallized poly-Si thin film with bottom-gate structure after Secco-etch, in which the device channel length was 1.5µm, and the laser energy density was (a) 430, (b) 450, and (c) 490 mJ/cm$^2$, respectively.

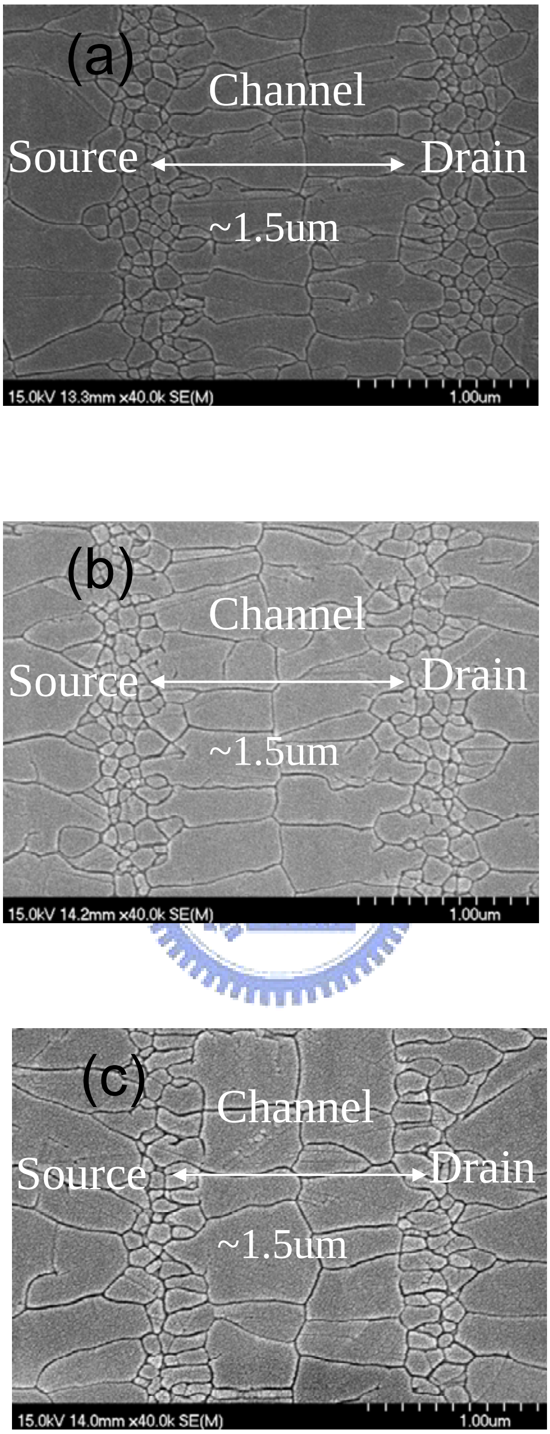


Fig. 2-9. The SEM micrographs of poly-Si thin films irradiated by excimer laser shot number of 20 shots and the gate oxide thickness of (a) 30, (b) 50, and (c) 100 nm, respectively, in which the device channel length was 1.5 μm. The laser energy density is 450 mJ/cm$^2$.

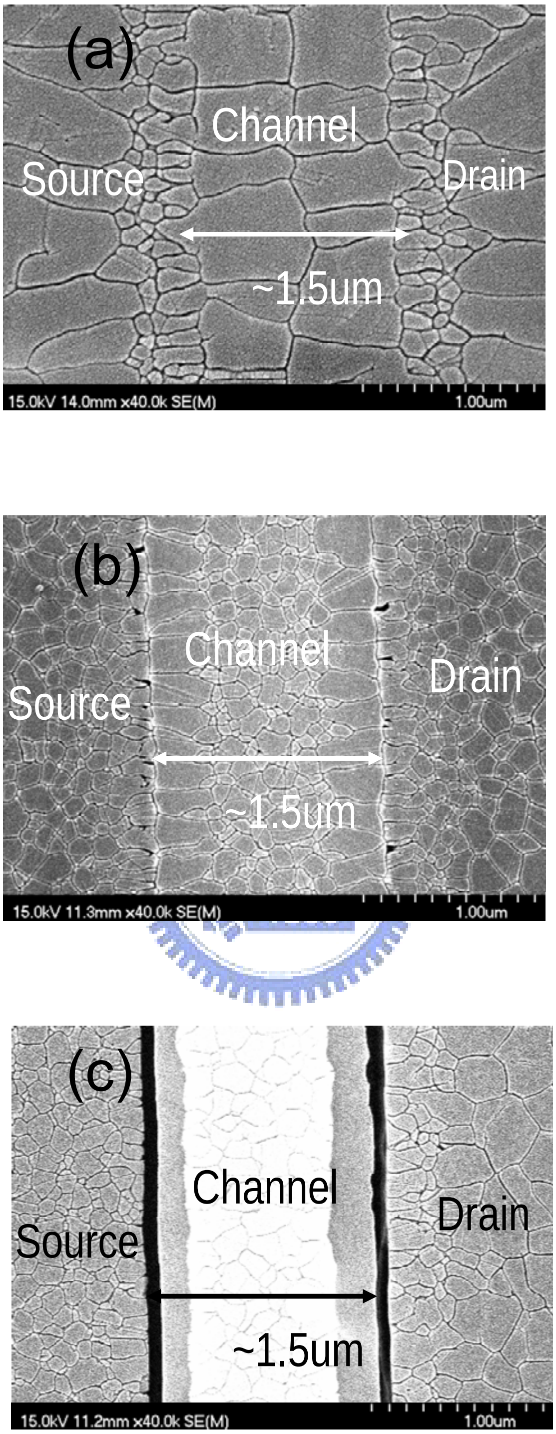
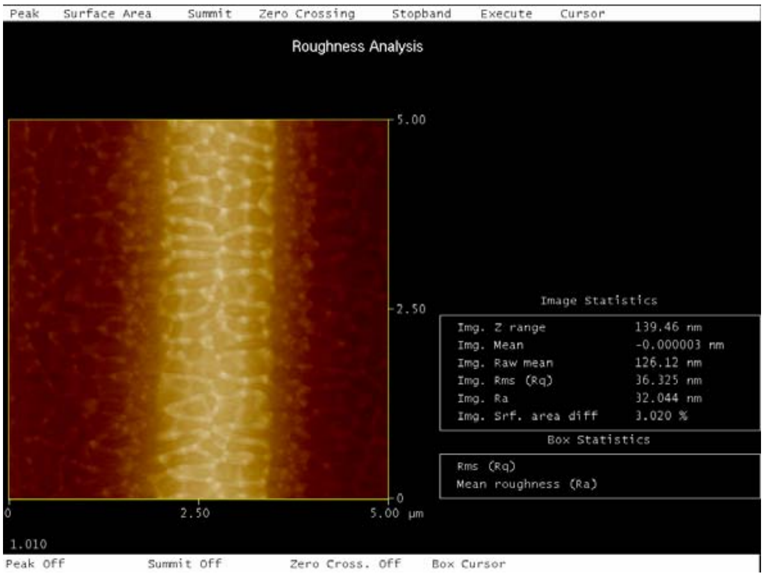


Fig. 2-10. The SEM micrographs of poly-Si thin films irradiated by excimer laser shot number of 20 shots and the bottom-gate thickness of (a) 100, (b) 200, and (c) 300 nm, respectively, in which the device channel length was 1.5 μm.



```
Image Statistics
Img. Z range              139.46 nm
Img. Mean                 -0.000003 nm
Img. Raw mean             126.12 nm
Img. Rms (Rq)             36.325 nm
Img. Ra                   32.044 nm
Img. Srf. area diff       3.020 %
Box Statistics
Rms (Rq)
Mean roughness (Ra)
```

Figure 2-11. The AFM image of 1000 Å-thick poly-Si thin films with bottom-gate structure after laser crystallization, in which the device channel length is 1.5 μm. In this case, the laser shot number is 20 shots and the bottom-gate thickness is 1000 Å.

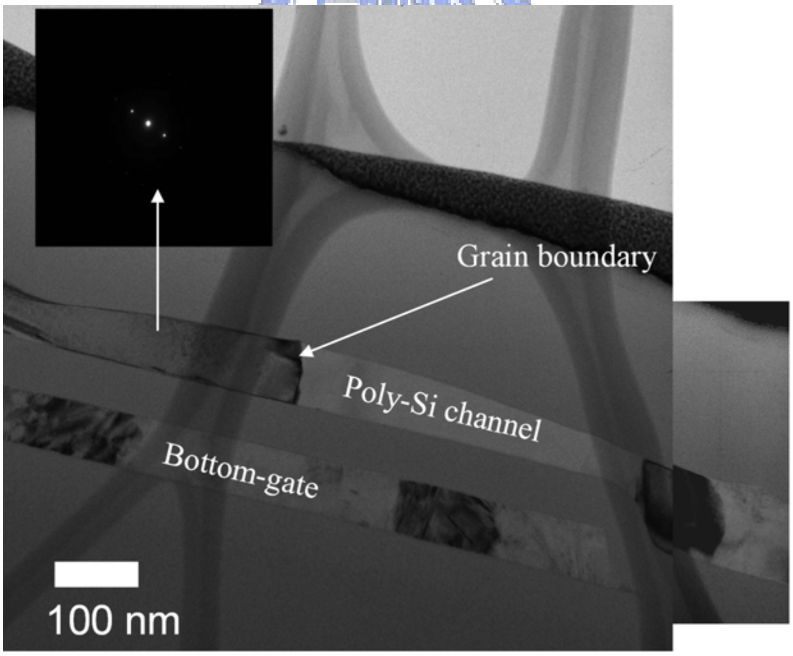


Figure 2-12. The cross-sectional TEM image of 1000 Å-thick poly-Si thin films with bottom-gate structure after laser crystallization, in which the device channel length is 1.5 μm.

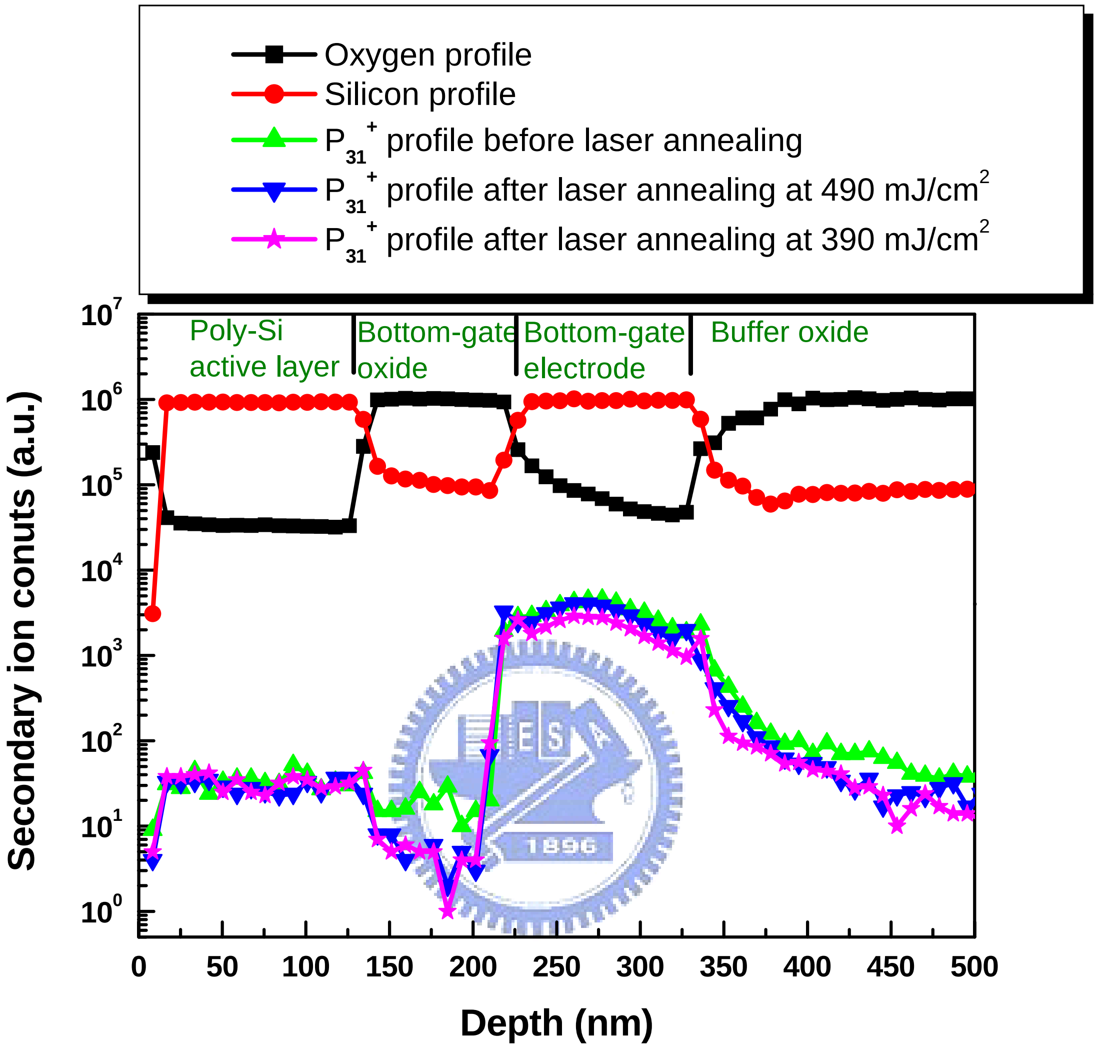


Figure 2-13. The element SIMS depth profiles of the excimer laser-crystallized bottom-gate TFTs

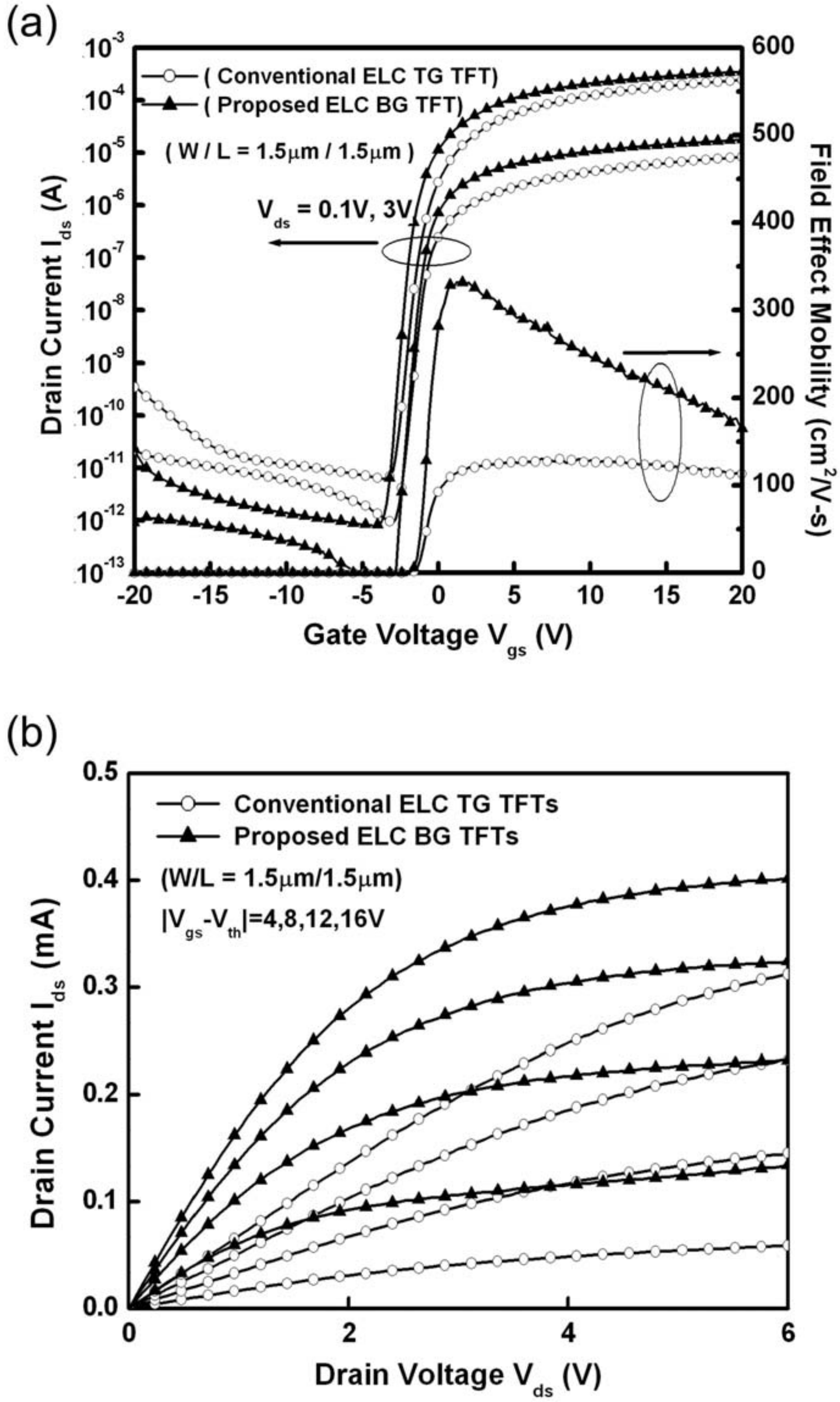


Figure 2-14. Comparisons of (a) Transfer characteristics and (b) Output characteristics for ELC BG LTPS TFT with lateral silicon grains and conventional ELC TG TFT.

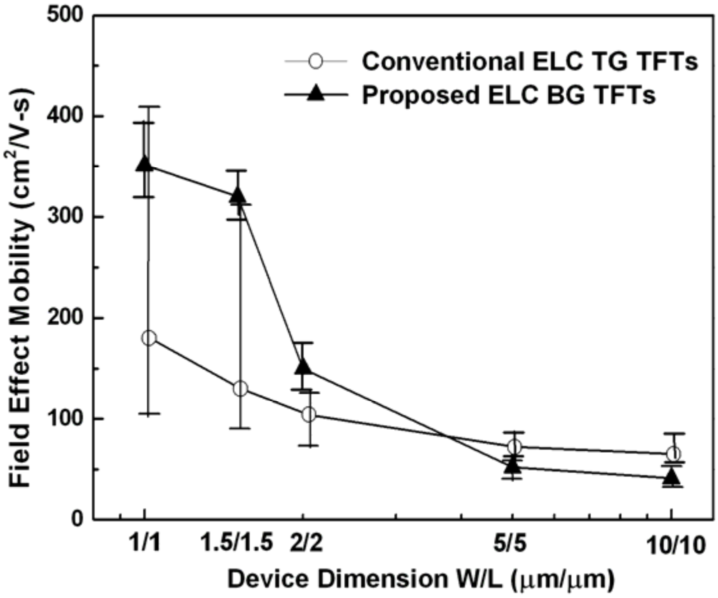


Figure 2-15. Dependence of field-effect-mobility on the device dimension for ELC BG LTPS TFTs with lateral silicon grins and conventional ELC TG ones. The field effect mobility was evaluated at $V_{ds} = 0.1$ V.

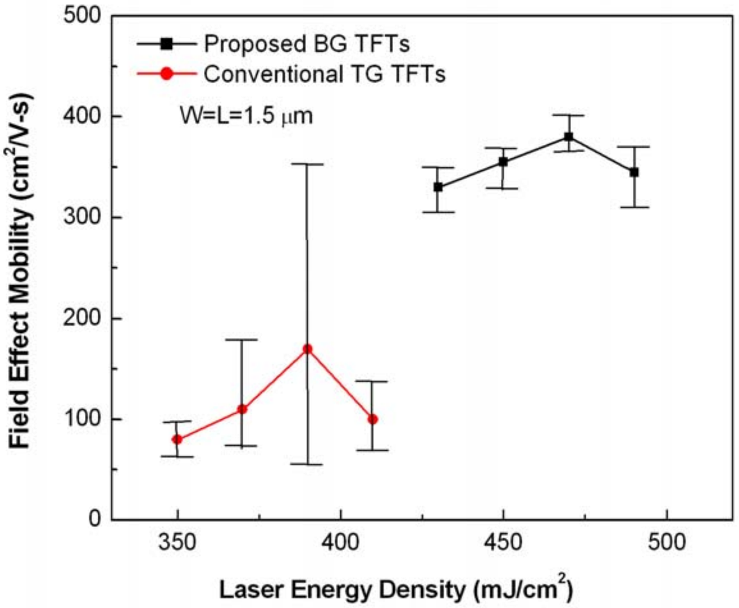


Figure 2-16. Dependence of field-effect-mobility on applied laser energy density for ELC BG TFTs with lateral silicon grins and conventional ELC TG ones with random grain structures.

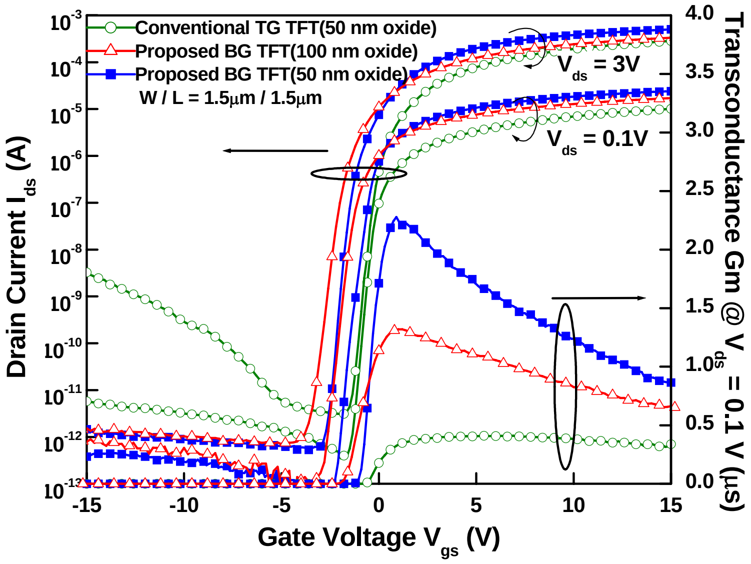


Figure 2-17 (a). Comparison of the transfer characteristics of the n-channel LTPS BG-TFTs with lateral silicon grains and conventional TG ones with W = L = 1.5 μm and gate oxide thickness of 500 Å or 1000 Å.

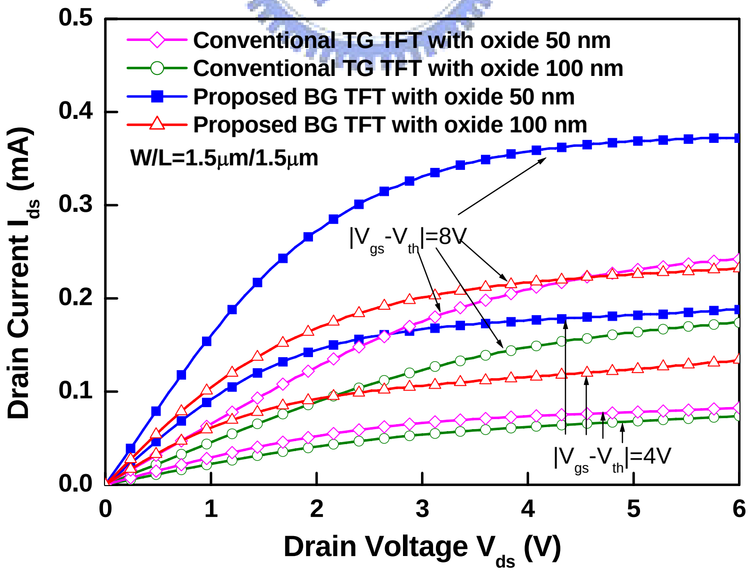


Figure 2-17 (b). Comparison of the output characteristics of the n-channel LTPS BG-TFTs with lateral silicon grains and conventional TG ones with W = L = 1.5 μm and gate oxide thickness of 500 Å or 1000 Å.

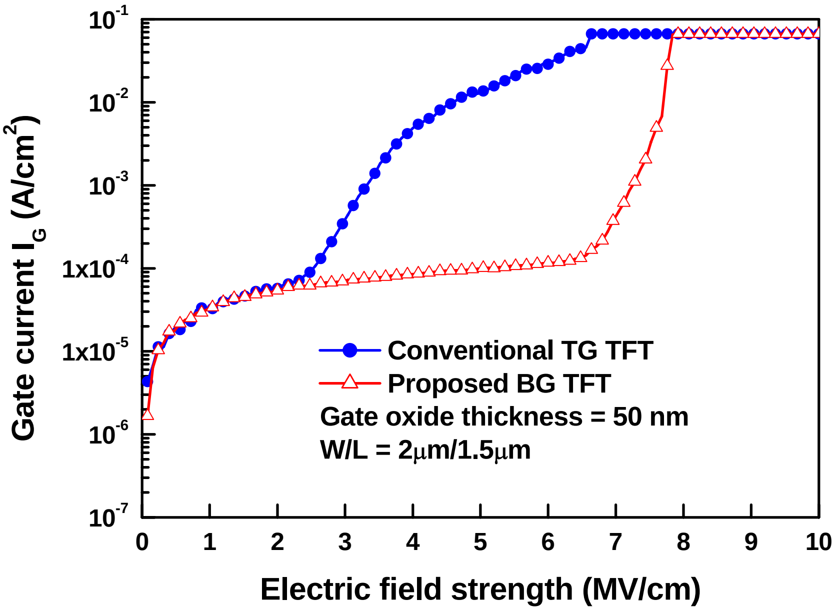


Figure 2-18 (a). The gate-breakdown field strength of two different TFT structures with 500 Å-thick TEOS gate oxide.

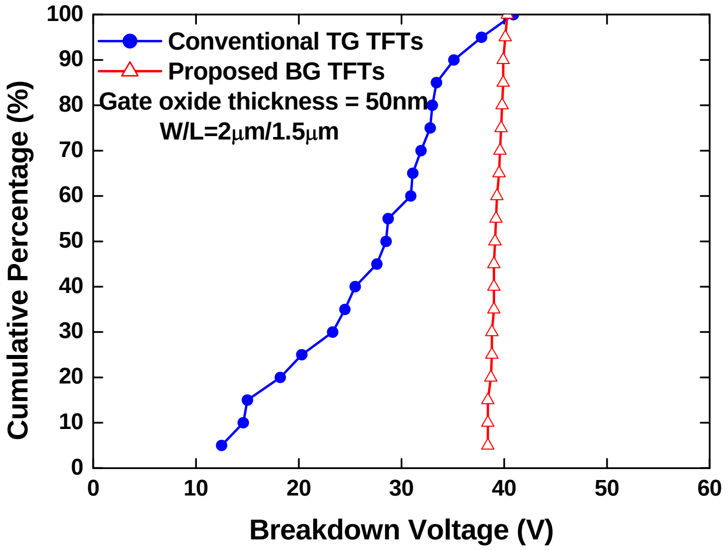


Figure 2-18 (b). Statistical distribution of the gate-breakdown voltage of two different TFT structures with 500 Å-thick TEOS gate oxide.

# Chapter 3

# High-Performance Self-Aligned Bottom-Gate Low Temperature Polycrystalline Silicon Thin-Film Transistors with Excimer Laser Crystallization

## 3.1 Introduction

Low-temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have been extensively investigated for use in active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting displays (AMOLEDs) [3.1]-[3.7]. The mobility of poly-Si TFTs fabricated by excimer laser crystallization is generally two orders higher than amorphous-Si TFTs, therefore the peripheral driving circuits and pixel elements can be integrated on the same glass substrate. In the early stage of the LTPS TFTs development, bottom-gate (BG) TFT structure was attractive because the excimer laser annealing was thought as an additional process step to the a-Si TFTs. However, bottom-gate TFTs suffered from worse electrical performance than top-gate (TG) TFTs because of the smaller grain size and poor grain quality resulting from the bottom-gate metal acting as a heat sink during excimer laser crystallization [3.8]-[3.9]. Moreover, bottom-gate TFTs exhibited significant performance variation as the devices scaled-down resulted from the misalignment effect. Although some self-aligned (SA) BG TFTs have been demonstrated, the device processes were too complicated to be utilized in the large area fabrication [3.10]-[3.11]. As a result, only a few studies have been conducted for bottom-gate TFTs with short channel length and top-gate TFTs have been widely adopted in AMLCD due to the self-alignment capability in the last decade. Although high field-effect-mobility for TG-TFTs has been attained by ELC, it is difficult to make the laser energy density hit the super lateral growth regime everywhere due to the fluctuation of pulse-to-pulse laser energy and amorphous silicon (a-Si) layer thickness [3.12]-[3.14]. Consequently, poor device uniformity and narrow process window were encountered in ELC TG-TFTs. Furthermore, in the applications of system-on-panel (SOP), TFTs must exhibit good uniformity of device-performance and high-reliability. Thus, many methods, such as sequential lateral solidification process [3.15], grain filters method [3.16], capping the reflective or anti-reflective layer [3.17], dual beam ELA [3.18], double–pulsed laser annealing [3.19], selectively floating a-Si active layer [3.20], CLC method using the diode-pumped solid-state continuous wave laser [3.21], and selectively enlarging laser crystallization (SELAX) [3.22], were proposed to solve the above problems. However, most of them need complex fabrication process or are problematic for circuit layout due to the anisotropy of the grain boundary spacing.

In the previous work, ELC BG LTPS-TFTs exhibit superior electrical characteristics, however, asymmetrical electrical characteristics are also observed due to the misaligned process effect. Besides, the mis-alignment effect will degrade the TFT performances more seriously in the short channel devices owing to the more percentage of the mis-alignment variation. Therefore, in this work, a self–aligned (SA) bottom-gate TFT with appropriate channel length has been fabricated by the simple excimer laser crystallization and backside exposure. The process steps in these technologies are not only highly compatible with the conventional commercial a-Si TFT process but also with minimum parasitic capacitance for high circuit performance. The detailed process procedures of self-aligned BG ELC LTPS TFTs will be described and the self-aligned photo-lithography process will be presented and analyzed by optical microscopy (OM) and scanning electron microscopy (SEM) material analyses. The phenomenon of controlled lateral grain growth using bottom-gate structure on quartz wafer is also investigated. Meanwhile, the electrical characteristics of SA BG ELC LTPS TFTs with two kinds of bottom-gate thickness of 1000 Å and 1500 Å were taken in into comparison. The symmetrical electrical characteristics can be observed in the SA BG ELC LTPS TFTs. Owing to the lateral grain growth and self-aligned structure, SA BG LTPS TFTs exhibit higher performance and better uniformity.

## 3.2 Experiments

### 3.2.1 Sample Preparation for Material Analysis

For further improving the bottom-gate LTPS-TFTs performances, we combined lateral grain growth controlled in the device channel region with the backside exposure photo-lithography. Figure 3-1 shows the process procedures for the preparation of self-aligned bottom-gate structure with large silicon grains by the excimer laser crystallization and the backside exposure. Since the self-aligned technique uses g-line light exposure from the back surface, the selection of appropriate substrate is important. Quartz wafer is used as the starting substrate for its high transparency ratio with g-line light wavelength of 436 nm and free from increase in temperature of the substrate. At first, after the RCA clean process, the 1000 Å-thick amorphous silicon layers were deposited by pyrolysis of pure silane ($SiH_4$) with low pressure chemical vapor deposition (LPCVD) at 550 °C on quartz wafers. Next, a phosphorus ion implantation with a dosage of $5\times10^{15}$ $cm^{-2}$ was performed. Then, the phosphorus-doped amorphous silicon layer was defined to form bottom-gate electrode by transformer-coupled plasma reactive ion etching (TCP-RIE). After defining the bottom-gate region, the 1000 Å-thick tetraethyl orthosilicate (TEOS) gate oxide layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 385 °C. Then, after standard RCA clean process, the

1000 Å-thick amorphous silicon (a-Si) layers were deposited by decomposition of pure silane ($SiH_4$) with LPCVD at 550 °C. After standard RCA clean process, the a-Si thin films were then subjected to 248 nm KrF excimer laser crystallization (ELC). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to $10^{-3}$ Torr and the substrate was maintained at room temperature. The laser beam was homogenized into a semi-gaussian shape in the short axis and a flat-top shape in the long axis. The number of laser shots per area was 20 (i.e. 95 % overlapping) and the laser energy density was varied. Then, a self-aligned photolithography by using the bottom-gate as an opaque mask is performed to form self-aligned source/drain to gate by backside exposure through the quartz substrate. Then, a phosphorous ion implantation with dose of $5\times10^{15}cm^{-2}$ was carried out to form source and drain regions.

The relations between the resulting laser-crystallized poly-Si thin films with bottom-gate structure and laser process conditions were investigated by utilizing scanning electron microscopy (SEM) analysis and transmission electron microscopy (TEM) analysis techniques. SEM was utilized to analyze the grain size and grain structure under different laser process conditions. In order to facilitate the SEM observation, some samples were processed by Secco-etch before analysis. TEM was employed to analyze the microstructure and crystallinity of poly-Si films and the completed device. The self-aligned bottom-gate photolithography was investigated by the optical microscopy (OM) and SEM analyses.

### 3.2.2 Fabrication of Self-Aligned (SA) BG LTPS TFTs using ELC

Figure 3-2 illustrates the key processes for the fabrication of SA BG LTPS TFTs by ELC with backside exposure. At first, after the RCA clean process, the 1000 Å-thick and 1500

Å-thick amorphous silicon layers were deposited by pyrolysis of pure silane ($SiH_4$) with low pressure chemical vapor deposition (LPCVD) at 550 °C on quartz wafers. Next, a phosphorus ion implantation with a dosage of $5\times10^{15}$ cm$^{-2}$ was performed. Then, the phosphorus-doped amorphous silicon layer was defined to form bottom-gate electrode by transformer-coupled plasma reactive ion etching (TCP-RIE). After defining the bottom-gate region, the 1000 Å-thick tetraethyl orthosilicate (TEOS) gate oxide layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 385 °C. Then, after standard RCA clean process, the 1000 Å-thick amorphous silicon (a-Si) layers were deposited by decomposition of pure silane ($SiH_4$) with LPCVD at 550 °C. After standard RCA clean process, the a-Si thin films were then subjected to 248 nm KrF excimer laser crystallization (ELC), as shown in Figure 3-2 (b). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to $10^{-3}$ Torr and substrate was maintained at room temperature. The number of laser shots per area was 20 (i.e. 95% overlapping) and laser energy density was varied. Figure 3-2 (c) exhibited a self-aligned photolithography using the bottom-gate as an opaque mask to form self-aligned source/drain to gate by backside exposure through the quartz substrate [3.23]-[3.29], while for the non-self-aligned BG TFT, a front-side UV light exposure is used to defining the source/drain regions which result in the offset region. The offset length in non-self-aligned TFT is about 0.45 μm due to the process of masker aligner and the offset length can be further reduced by using the I-line stepper system. It is worth mentioning that the fabrication processes of new self-aligned TFTs and conventional non-self-aligned ones are almost the same, except the lithography process of defining the source/drain regions. Then, a phosphorous ion implantation with dose of $5\times10^{15}$cm$^{-2}$ was carried out to form source and drain regions. Then, the device active region was etched by reactive ion etching (RIE). Next, a 3000 Å-thick passivation oxide layer was deposited by at PECVD 385 °C and the implanted dopants were activated by thermal annealing at 600°C for 12 h in the $N_2$ ambient. After contact hole opening by reactive ion etching, aluminum thin film with a thickness of 5000 Å was deposited by thermal evaporation and Al metal pads were patterned to complete the fabrication of SA-BG LTPS TFTs as shown in Figure 3-2(d). Finally, a 30-min sintering process was performed at 400°C in the $N_2$ ambient to reduce the contact series resistance of the source and drain electrodes. No hydrogenation plasma treatment was performed during the device fabrication process. For comparison, the conventional non-self-aligned ELC LTPS bottom-gate TFTs with a channel thickness of 1000Å were also fabricated.

Current-voltage (I-V) characteristics of the fabricated devices were measured using a semiconductor parameter analyzer of Agilent technologies 4156C. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of $I_{ds}$ = (W/L) x $10^{-8}$ A at $V_{ds}$ = 0.1 V. The field-effect mobility and subthreshold swing were extracted at $V_{ds}$ = 0.1 V, and the $I_{on}/I_{off}$ current ratio was defined at $V_{ds}$ = 3 V. An analytical transmission electron microscopy (TEM) (JEM-2100FX, JEOL Ltd.) was employed to analyze the microstructure and crystallinity of poly-Si film in the channel region and the completed SA-BG TFT device.

## 3.3 Results and Discussion

### 3.3.1 Material Characterization of SA-BG LTPS Thin Films

#### 3.3.1.1 Optical Microscopy (OM) Analysis

Figure 3-3 (a) and 3-3 (b) shows the optical microscope (OM) images of the samples with bottom gate structure from the transparent light source. The thickness of the amorphous silicon gate electrode was both 1000Å and the channel length was 2 μm and 5 μm, respectively. At first, it was confirmed that the bottom-gate maintained its original structure after excimer laser crystallization. In addition, the bottom amorphous silicon gate is thick

(100 nm) enough to act as a mask for the formation of the self-aligned bottom gate structure by using the back surface exposure. According to those pictures, the regions above the amorphous silicon bottom-gate were dark but the other regions were bright in both cases. It could be found that the g-line light could not pass through the region sheltered by the amorphous silicon (a-Si) bottom-gate but could pass through other regions not covered by bottom-gate electrode. The g-line light was mostly absorbed and reflected by the amorphous silicon bottom-gate electrode. Hence, the thicker a-Si bottom gate, the less g-line light crossed the bottom-gate. Therefore, the a-Si bottom-gates with thickness of 1000 Å and 1500 Å could act as the opaque masks of the photo-lithography process to stop the ultra violate light from the Hg light source. Figure 3-4 (a) and 3-4 (b) shows OM images of the mis-aligned and the self-aligned ion-implanted devices after photo-lithography from the reflected light source, in which the channel length was 2 μm. Due to the process of masker aligner, there were horizontal shifts of photo-resist (P.R.) on the region of a-Si bottom-gate in defining the source/drain regions which result in the offset region after the photo-lithography, as shown in the Figure 3-4 (a). The horizontal shift was about 0.45 μm which would lead to the mis-aligned process of the ion implantation and degrade the device performance. Figure 3-4 (b) show a self-aligned photo-lithography by backside exposure method. It could be observed that a photo-resist pattern designed on the 100 nm-thick a-Si bottom-gate after the backside exposure photo-lithography, as shown in Figure 3-4 (b). The bottom gate pattern was copied for the photo-resist coating on the bottom-gate. Owing to the perfect self-aligned back surface exposure, the P.R. on the bottom-gate would not absorb UV light. Therefore, the P.R. would be remained and perfectly aligned to the bottom-gate after the develop process. Consequently, the self-aligned ion implantation of source and drain regions to gate would be precisely carried out without any shifts.

### 3.3.1.2 Scanning Electron Microscopy (SEM) Analysis

Figure 3-5 shows the SEM micrograph of the self-aligned ion-implanted devices after the photo-lithography. According to the SEM micrograph, the P.R. with thickness of 1.2 μm was observed and the P.R. was perfectly aligned to the a-Si bottom-gate electrode which was consistent with the results obtained by OM graphs. To sum up, the a-Si bottom-gate could act as the opaque mask of the photo-lithography process to stop the ultra violate light from the Hg light source and this method leaded to the easy formation of a self-aligned bottom-gate TFTs. As a result, the P.R. aligned to the amorphous silicon gate would benefit the ion implantation of source and drain regions for the minimal series resistance.

Figure 3-6 (a) and 3-6 (b) display the SEM photographs of excimer laser crystallized poly-Si with bottom-gate structure after Secco etching, in which the thickness of bottom-gate electrode was 100 nm, and 150 nm, respectively. In these cases, the length of bottom-gate is 1.5 μm, the laser energy density is 450 mJ/cm$^2$ and the substrate temperature is maintained at room temperature during laser irradiation. According to the SEM graphs in the Fig. 3-6(a) and 3-6(b), it can be observed that the large silicon grains with 0.75 μm in lateral dimension could be formed in the channel regions, while small and fine grains were located near the edges of the bottom-gate for the 100 nm-thick and 150 nm-thick bottom-gate electrodes, respectively.

### 3.3.1.3 Transmission Electron Microscopy (TEM) Analysis

The micro-structural properties of laser-crystallized poly-Si films with bottom-gate structure such as the grain size, inter-grain defect density, intra-grain defect density, and grain orientation can be identified by using transmission electron microscopy (TEM) and its selected-area electron diffraction patterns. Figure 3-7(a) displays the cross-sectional TEM image and the selected-area electron diffraction patterns of 1000 Å-thick poly-Si thin films with bottom-gate structure after laser crystallization, in which the device channel length is 1.5

μm. In this case, the laser shot number is 100 shots and the bottom-gate thickness is 1000 Å. The laser energy density is 450 mJ/cm$^2$ and the substrate temperature is maintained at room temperature during laser irradiation. It is observed that four large silicon grains with good crystallinity are formed based on the ELC with bottom-gate structures. It is further confirmed that the lateral grain growth using ELC with bottom-gate structure can also be fabricated on the quartz wafer. For the short channel length with the proper thicknesses of gate electrode, gate oxide, and channel layers using this crystallization, only single grain boundary perpendicular to the channel direction is also observed by TEM image, as shown in Figure 3-7(b). According to the TEM image in the Figure 3-7 (b), there are two large silicon grains formed in the channel region above the bottom-gate electrode and the high angle grain boundary can be artificially controlled in the middle of the channel region. The crystallinity of the silicon grain in the channel region is pretty good and the normal orientation of the grain is in <110> direction due to the simple spots based on the selected-area electron diffraction patterns. In addition, the cross-sectional TEM image in Figure 3-7 display the clear interfaces between the bottom-gate oxide and poly-Si active layer. The interface between the bottom-gate electrode and bottom-gate oxide is also clear, implying that both the gate oxide and the bottom-gate electrode are not damaged during excimer laser irradiation. Moreover, the cross-sectional TEM image reveals that a flat interface morphology between the gate dielectric and poly-Si channel films in the bottom-gate TFTs. The smoother interface of bottom-gate TFT implies that the proposed TFT will exhibit improved breakdown characteristics and better reliability [3.30]-[3.31]. The performance and uniformity of TFT devices can be improved with such artificially large laterally grains. In addition, the circuit layout design is easier because proposed crystallization method is insensitive to laser scanning direction or device location.

### 3.3.2 Electrical Characteristics of SA-BG LTPS TFTs using ELC

It is anticipated that the thicker the a-Si bottom-gate the less UV light passes through the bottom-gate electrode. In the chapter 2, it has been investigated that if the thickness of bottom-gate electrode was larger than 2000 Å, there will be serious thinning effect of silicon thin films during laser crystallization. Therefore, SA BG LTPS TFTs with gate thickness of 1000 Å and 1500 Å are chosen and fabricated for comparison. Figure 3-8 (a) shows the typical transfer characteristics of SA BG LTPS TFTs with bottom-gate thickness of 1000 Å and 1500 Å, respectively. The laser process conditions were both optimized for two devices. According to the Id-Vg, the SA-BG LTPS TFTs with a-Si gate thickness of 1000 Å exhibit better electrical characteristics than that of poly-Si TFTs with 1500 Å-thick gate. Take the device of W = L = 1 μm for example, SA-BG TFT with field effect mobility of about 192 $cm^2/V$-s could be achieved by using a-Si gate thickness of 1000 Å while the mobility of the SA-BG TFT with 1500 Å-thick gate was about 129 $cm^2/V$-s. The lower mobility of SA BG TFTs with bottom-gate thickness of 1500 Å could be attributed to the faster cooling rate in the channel region. The thicker the a-Si gate, the faster heat flow was conducted to the substrate by crossing the gate, which resulted in poorer quality of silicon grains and shorter lateral grain growth in the device channel region. Figure 3-8 (b) shows the output characteristics of SA BG LTPS TFTs with bottom-gate thickness of 1000 Å and 1500 Å, respectively. It was demonstrated that SA BG LTPS TFTs with gate thickness of 1000 Å provided higher output driving current than that of SA BG LTPS TFTs with gate thickness of 1500 Å under the same bias condition. The improved driving current could be attributed to the higher field-effect mobility due to the better crystallinity of large silicon grains in the device channel region. Therefore, the 1000 Å-thick a-Si bottom-gate was the optimized condition for the fabrication of SA-BG LTPS TFTs and would be discussed in the following report.

Typical transfer characteristics of SA-BG LTPS TFTs and conventional non-SA-BG ones for W = L = 1 μm are shown in Figure 3-9 (a). Owing to the uniformly large transverse grains grown in the device channel region and self-aligned source/drain to the bottom-gate, this proposed SA-BG TFTs with lateral grains exhibited better electrical characteristics, the field-effect-mobility of 193 $cm^2/Vs$, than the conventional ones, the field-effect-mobility of 17.8 $cm^2/Vs$. Although the poly-Si grain structure in the channel region is similar in the SA-BG and non-SA-BG TFTs after excimer laser crystallization. However, after the lithography process of defining the source/drain regions, the lateral grain structure is still symmetric above the gate electrode in the SA TFTs, while the grain structure becomes asymmetric in the channel region and there is an offset region in the conventional non-SA TFTs due to the mis-aligment process effect. The mis-alignment effect will degrade the TFT performances more seriously in the short channel devices owing to the more percentage of the mis-alignment variation. In consequence, for the non-self-aligned TFTs, because small and fine grains are near the edges of bottom gate and the series resistance of the offset region is large, the non-SA-BG TFTs display lower field-effect-mobility, large subthreshold swing and lower on-current. The high field effect mobility is attributed to the reduced grain boundary in the channel regions [3.32]. Table 3-1 lists several important electrical characteristics of the two different TFT structures. Figures 3-9 (b) shows the output characteristics of of SA-BG LTPS TFTs and conventional non-SA-BG ones for W = L = 1 μm, respectively. SA BG TFTs provide higher driving current than that of non-SA BG ones under the same bias condition because of the large silicon grains in the channel regions and less series resistance near the source and drain regions.

Figures 3-10 and show the transfer characteristics of SA-BG TFTs and non-SA-BG ones under both the forward and reverse measurement modes. The roles of source and drain electrode are changed for the forward and reverse measurement modes. Figures 3-11(a) and 3-11(b) show the output characteristics of SA-BG TFTs and non-SA-BG ones under both the forward and reverse measurement modes, respectively. The symmetric and better electrical characteristics confirm that the proposed BG TFT is a SA gate structure, while asymmetrical electrical characteristics are observed in non-SA BG TFTs. The non-SA BG LTPS TFTs exhibit not only the shift of the threshold voltage but also the serious kink current. These problems were all suppressed in SA-BG LTPS TFTs.

Moreover, to study the uniformity of these three different TFTs performance, twenty TFTs for the optimal laser irradiation condition are measured. SA-TG TFTs display the worst uniformity which the mobilities range from 45 to 285 cm$^2$/Vs owing to the non-uniform grain distribution in the SLG regime. As for the bottom-gate deivces, the mobilities of the SA-BG TFTs range from 170 to 210 cm$^2$/Vs, but for the non-SA BG-TFTs, the mobilities range from 8.5 to 60 cm$^2$/Vs. It is found that the variation range of mobility is similar about 50 cm$^2$/Vs. But for the calculation of non-uniformity, our definition of non-uniformity is $\frac{\text{maximum mobility - minimum mobility}}{\text{average mobility}}$. As a result, the non-uniformity of non-SA-BG device is worse from the lower average mobility. The improved electrical characteristics and high device uniformity of SA-BG TFTs are more suitable for device-size scaled-down application attributed to the location-controlled lateral silicon grains and self-aligned S/D structure.

## 3.4 Summary

High-performance SA-BG LTPS TFTs have been fabricated by excimer laser crystallization with backside exposure. The process flows are simple and fully compatible with conventional a-Si TFTs fabrication processes. The bottom amorphous silicon gate is thick (100 nm) enough to act as an opaque mask for the formation of the self-aligned bottom gate structure by using the back surface exposure. From the OM and SEM micrographs, the photo-resist is perfectly self-aligned to the bottom-gate regions. Consequently, besides the high field-effect-mobility reaching 193 $cm^2/Vs$ in 1 μm design rule, SA BG TFTs exhibit excellent device uniformity owing to the artificially-controlled lateral grain growth and the self-aligned structure. The SA-BG LTPS TFTs with a-Si gate thickness of 1000 Å exhibit better electrical characteristics than that of poly-Si TFTs with 1500 Å-thick gate owing to the better quality of large silicon grains in the device channel region. Furthermore, the experimental results also reveal symmetric electrical characteristics. The SA-BG TFTs with lateral silicon grains are therefore promising for future system-on-panel applications.

Table 3-1

Measured electrical characteristics of SA-BG LTPS TFTs with lateral grain growth and conventional non-SA BG ones.

| **TFT Structures (W = L = 1 μm)** | **Threshold Voltage (V)** | **Field-effect-Mobility ($cm^2$/Vs)** | **Subthreshold Swing (V/dec)** | **On/off Current Ratio** |
|---|---|---|---|---|
| **Proposed SA Bottom-Gate** | **-0.77** | **193** | **1.19** | **1.14 x$10^7$** |
| **Conventional non-SA Bottom-Gate** | **1.70** | **17.8** | **1.25** | **1.07 x$10^7$** |

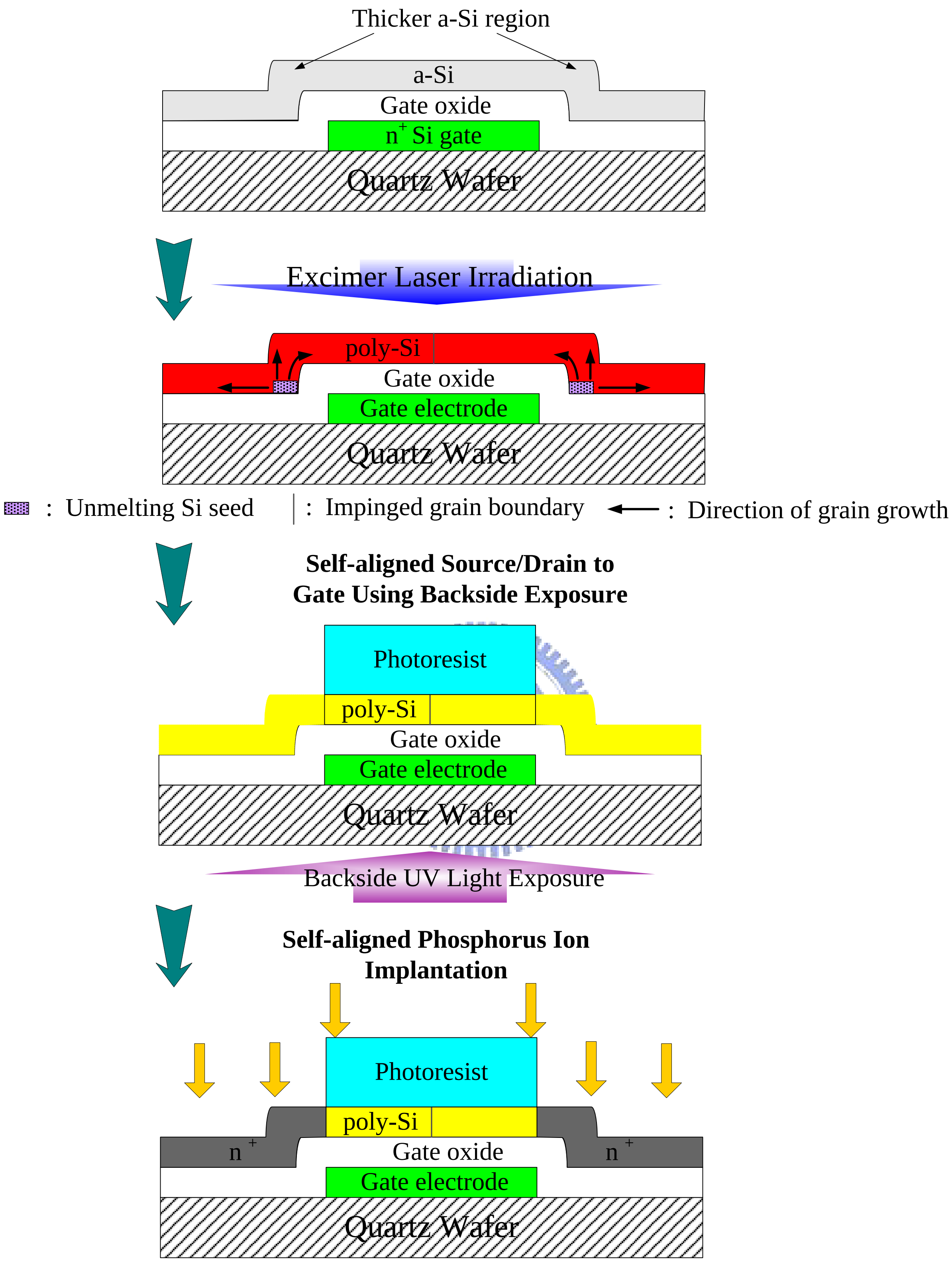


Figure 3-1. The process procedures for the preparation of self-aligned bottom-gate structure with large silicon grains by the excimer laser crystallization and the backside exposure.

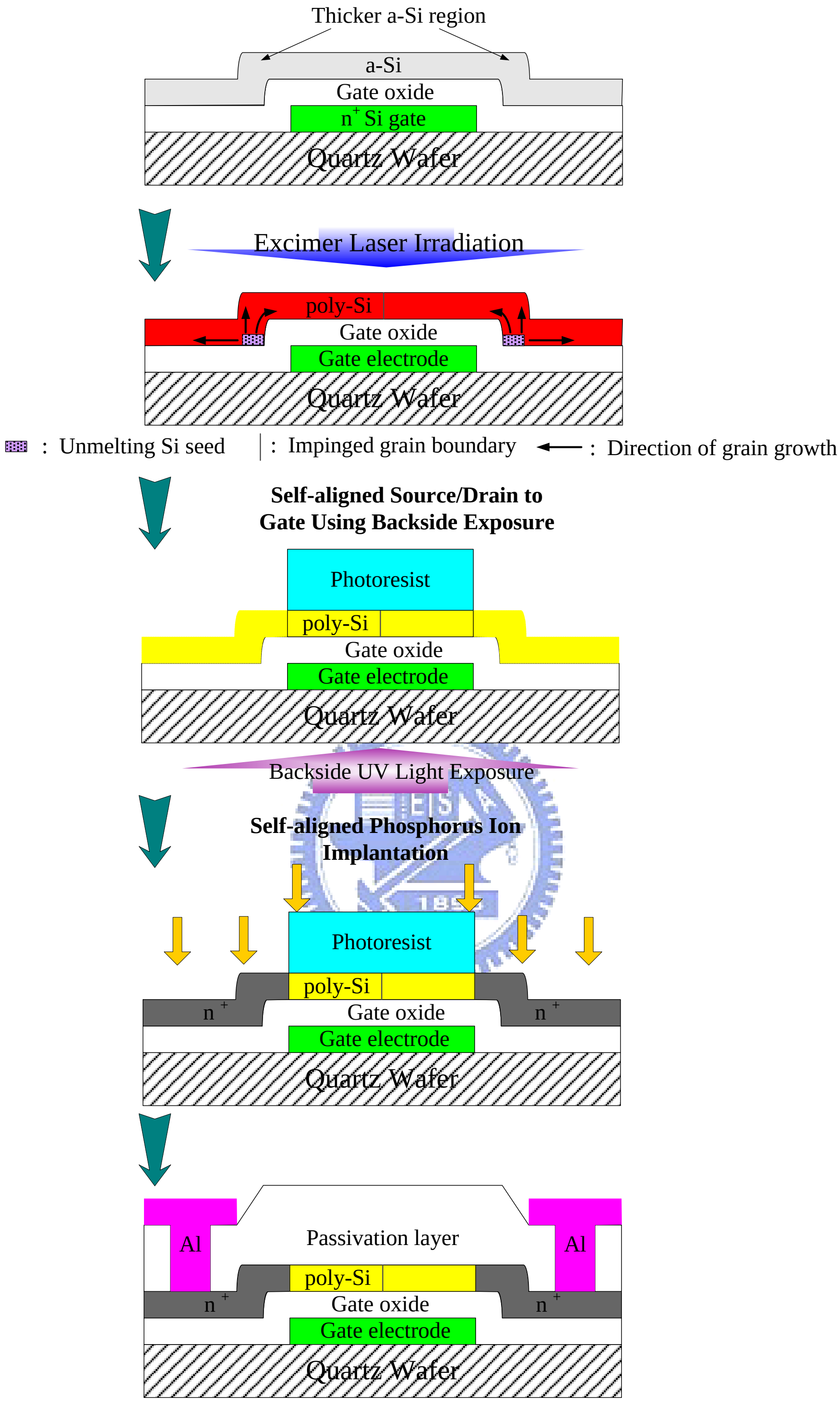


Figure 3-2. The key process procedures for fabricating small-dimension self-aligned bottom-gate LTPS TFTs with lateral grain growth.

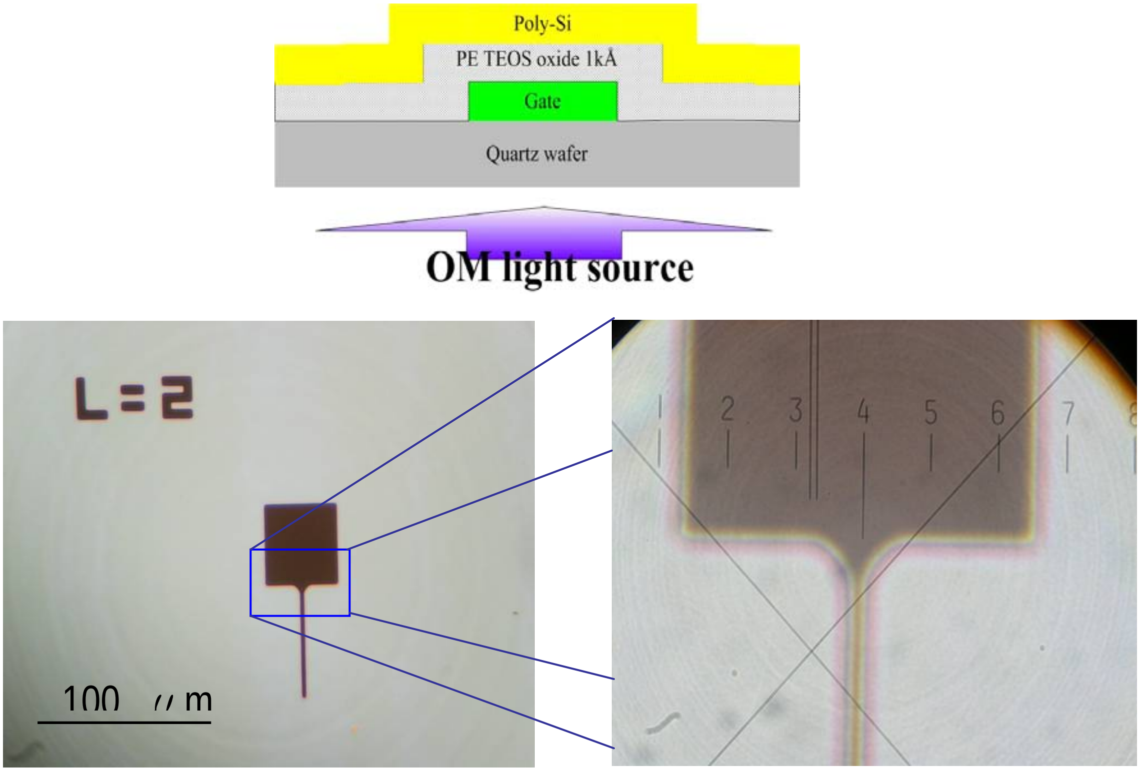


Figure 3-3(a). The optical microscope (OM) images of the samples with bottom gate structure from the transparent light source. The thickness of the amorphous silicon gate electrode was both 1000Å and the channel length was 2 μm.

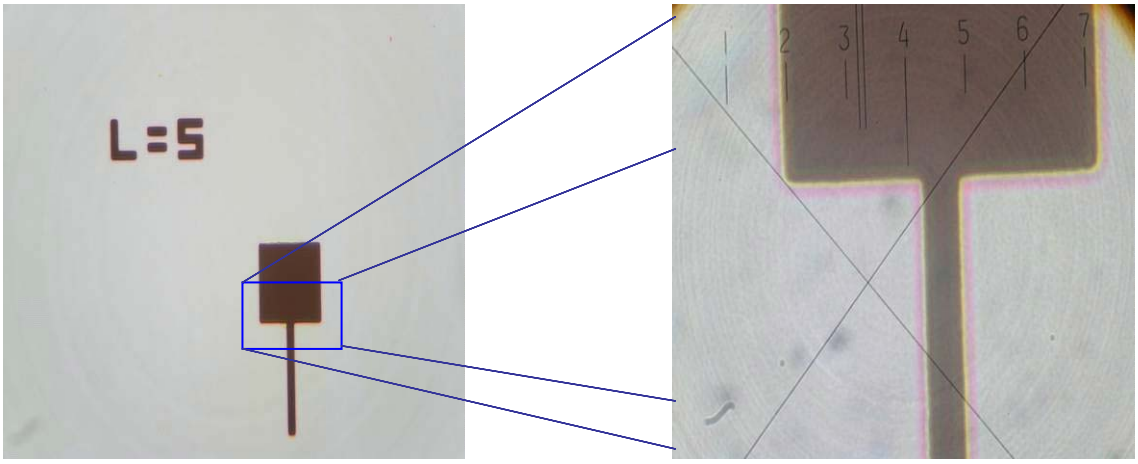


Figure 3-3(b). The optical microscope (OM) images of the samples with bottom gate structure from the transparent light source. The thickness of the amorphous silicon gate electrode was both 1000Å and the channel length was 5 μm.

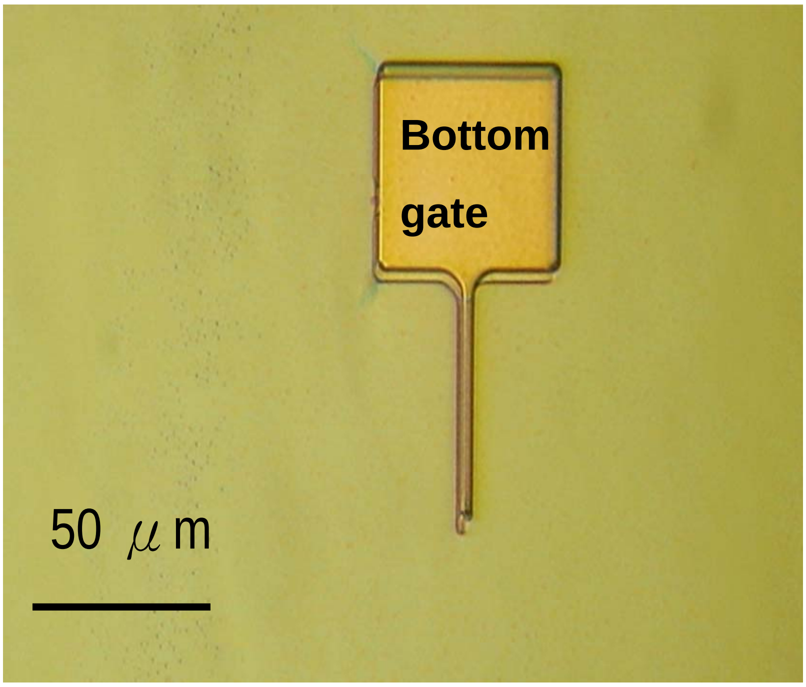


Figure 3-4(a). OM images of the non-self-aligned ion-implanted devices after photo-lithography from the reflected light source, in which the channel length was 2 μm.

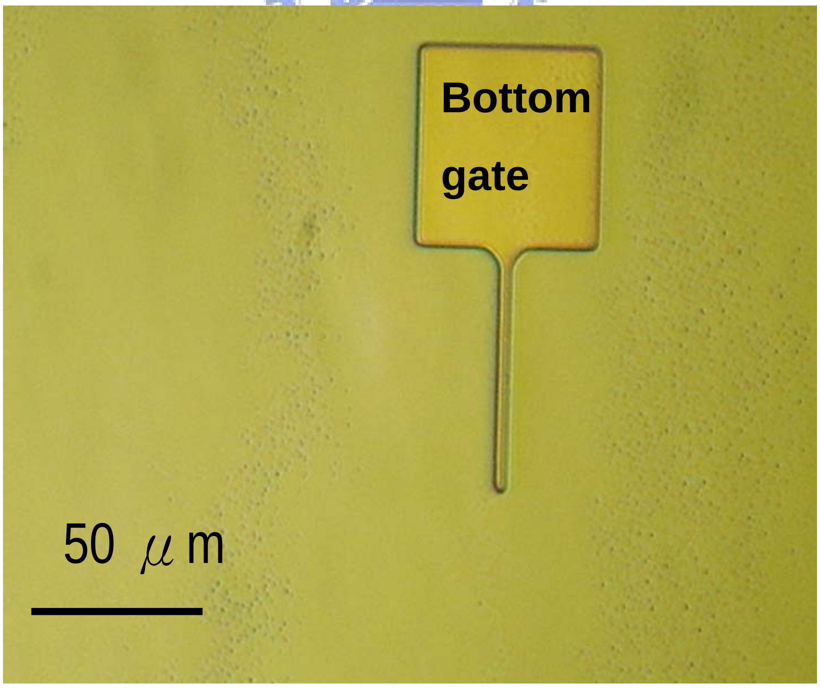


Figure 3-4(b). OM images of the self-aligned ion-implanted devices after photo-lithography from the reflected light source, in which the channel length was 2 μm.

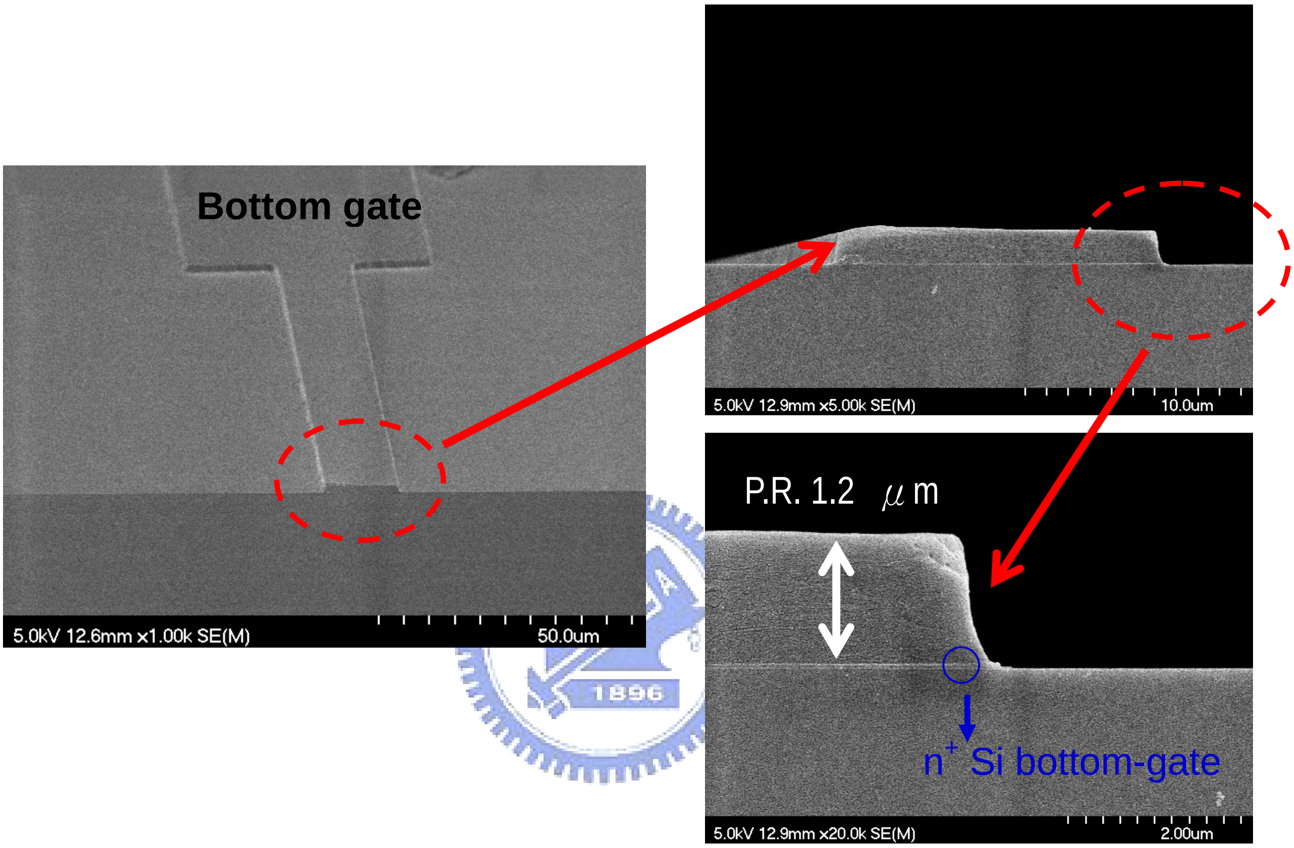


Figure 3-5. The SEM micrographs of the self-aligned ion-implanted devices after the photo-lithography.

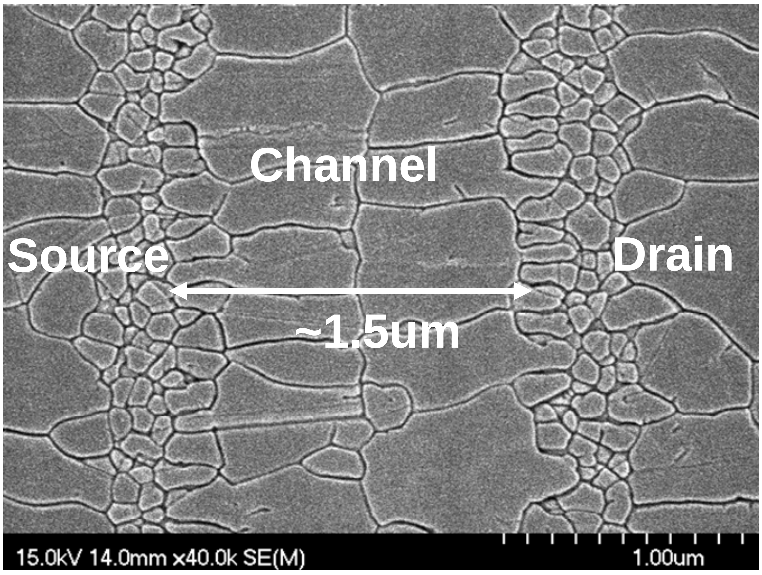


Figure 3-6 (a). Scanning electron microscope micrograph of excimer laser crystallized poly-Si film with bottom-gate structure on quartz wafer after Secco etching, in which the thickness of bottom-gate electrode was 100 nm.

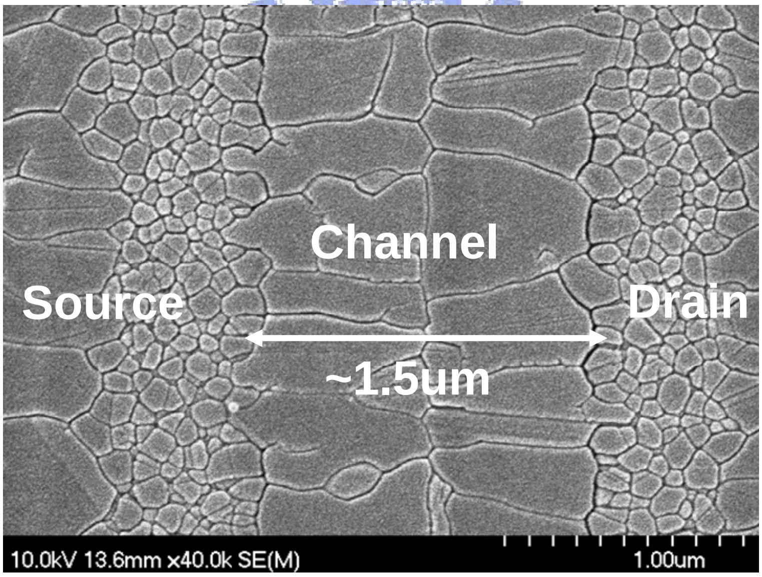


Figure 3-6 (b). Scanning electron microscope micrograph of excimer laser crystallized poly-Si film with bottom-gate structure on quartz wafer after Secco etching, in which the thickness of bottom-gate electrode was 150 nm.

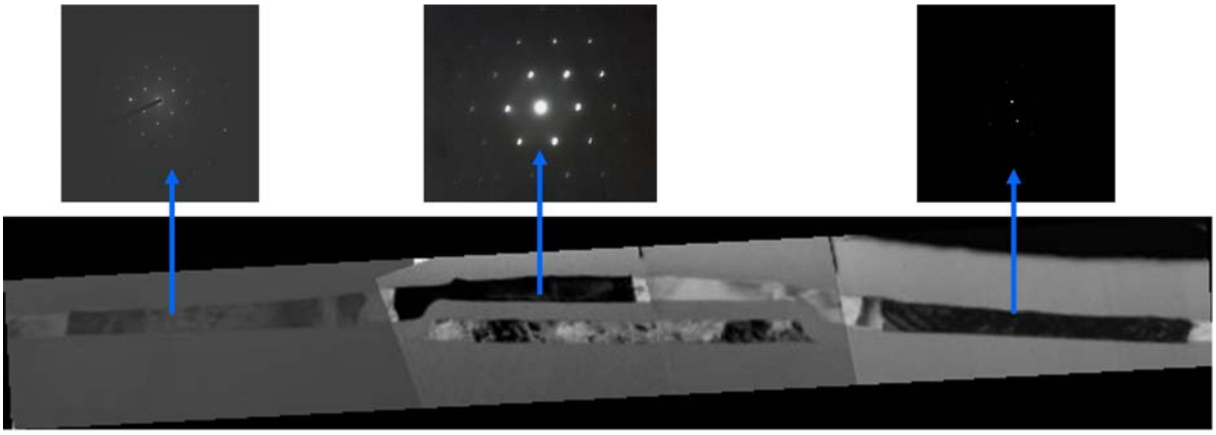


Figure 3-7 (a). FIB-prepared cross-sectional TEM images and the diffraction patterns of laser-crystallized poly-Si thin films of the self-aligned bottom-gate devices.

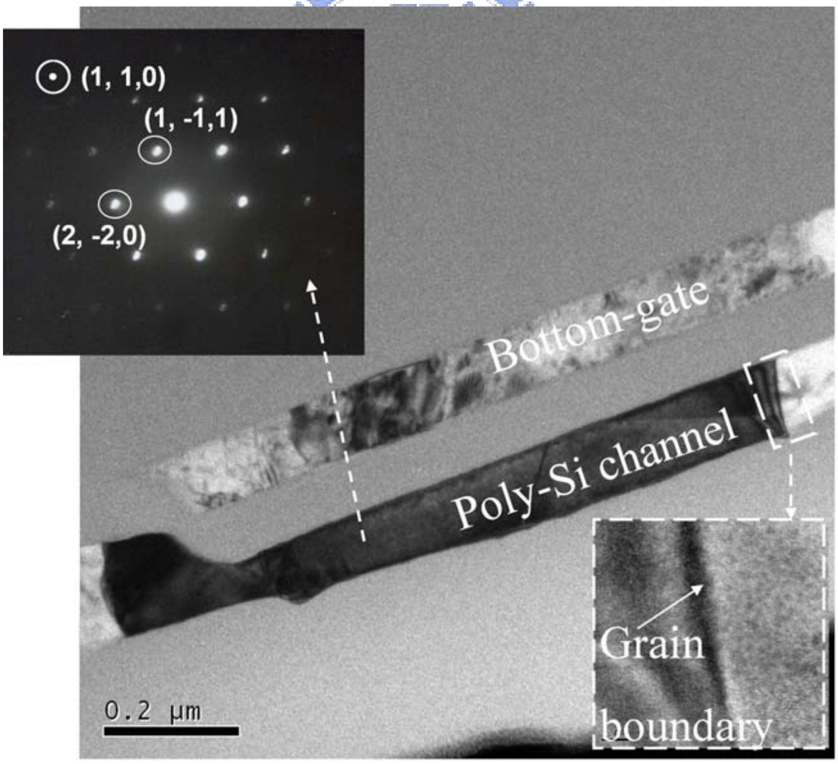


Figure 3-7 (b). High-magnification cross-sectional bright-field TEM image and the selected-area electron diffraction pattern of laser-crystallized poly-Si thin films of the self-aligned bottom-gate devices.

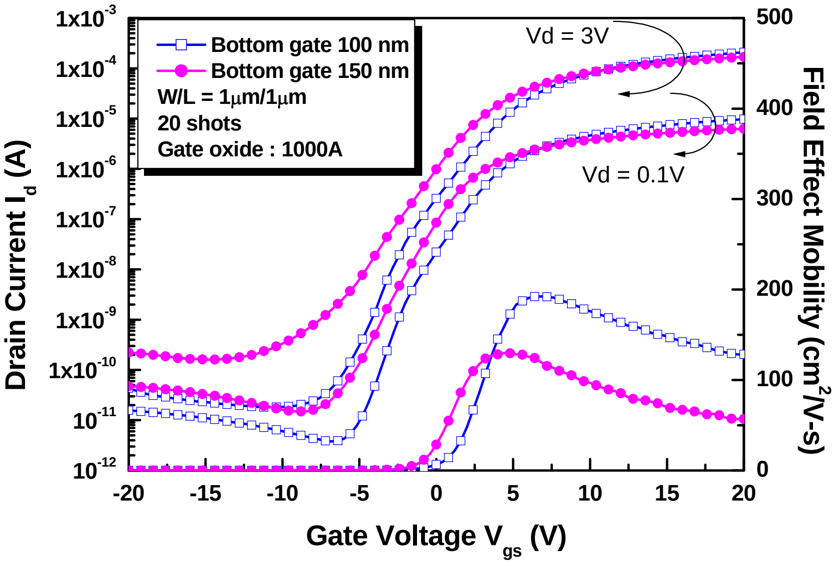


Figure 3-8 (a). The typical transfer characteristics of SA BG LTPS TFTs with bottom-gate thickness of 1000 Å and 1500 Å, respectively.

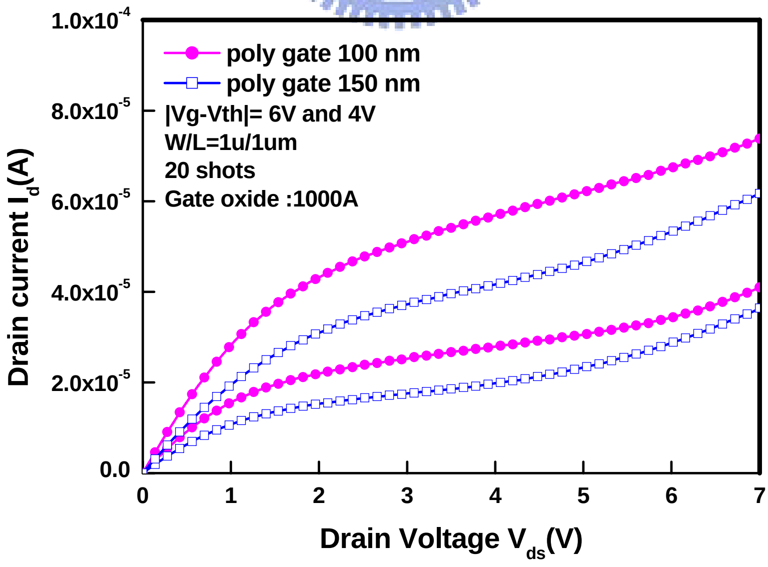


Figure 3-8 (b). The output characteristics of SA BG LTPS TFTs with bottom-gate thickness of 1000 Å and 1500 Å, respectively.

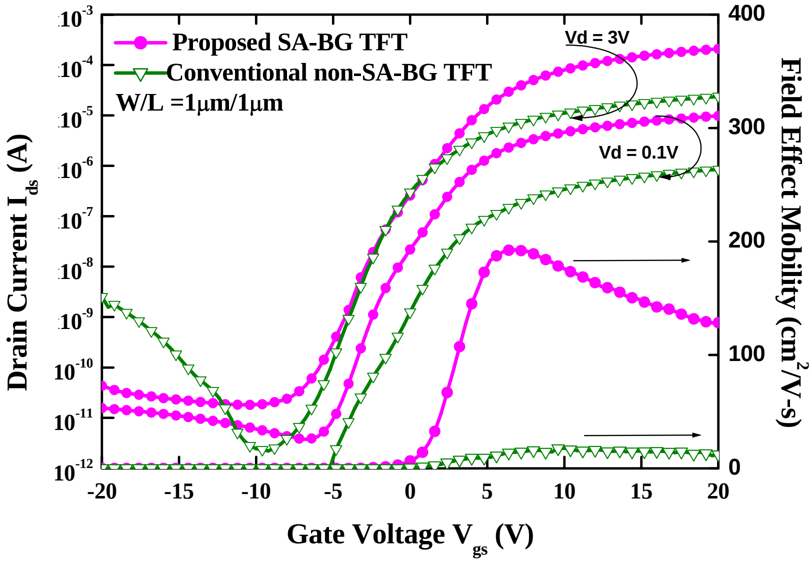


Figure 3-9 (a). Comparison of the transfer characteristics between the SA-BG LTPS TFTs and conventional non-SA-BG ones with W = L = 1 μm.

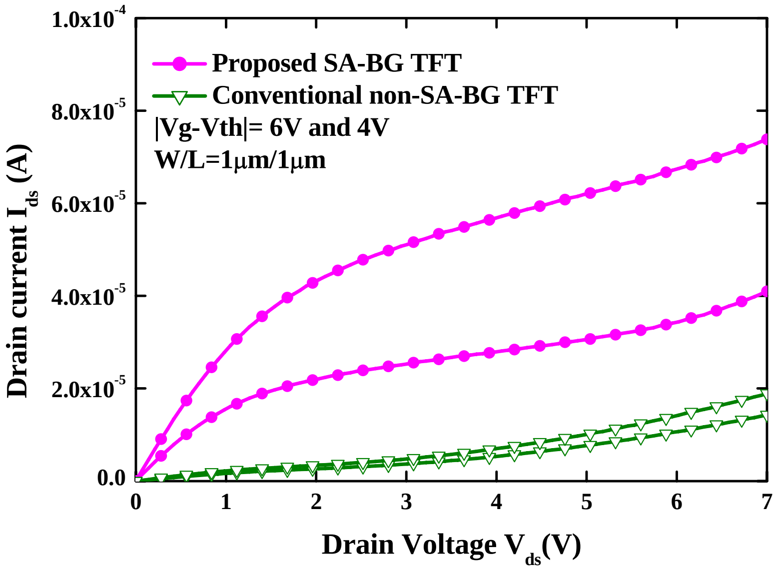


Figure 3-9 (b). Comparison of the output characteristics between the SA-BG LTPS TFTs and conventional non-SA-BG ones with W = L = 1 μm.

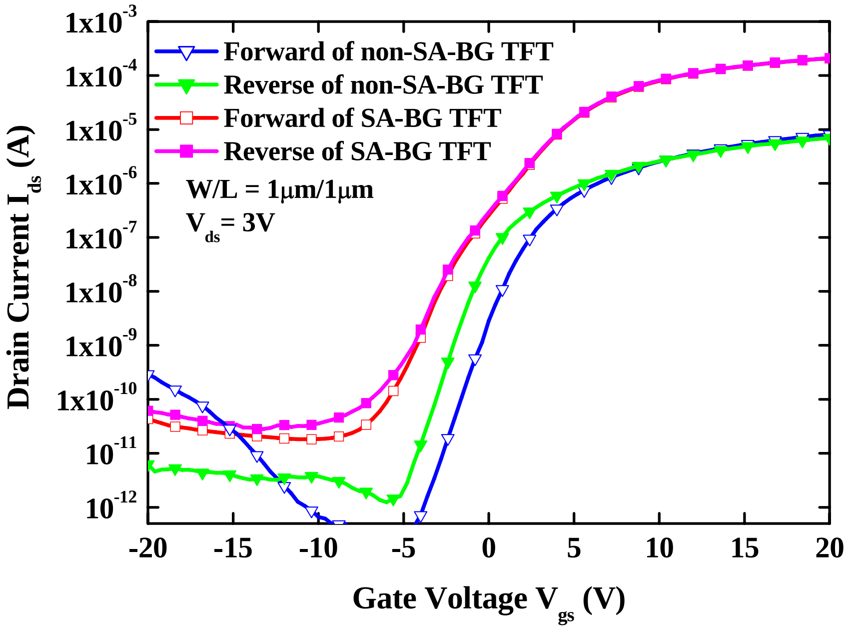


Figure 3-10. Experimental measured bi-directional transfer characteristics of SA-BG TFT and conventional one under the polarities of the source and drain are interchanged.

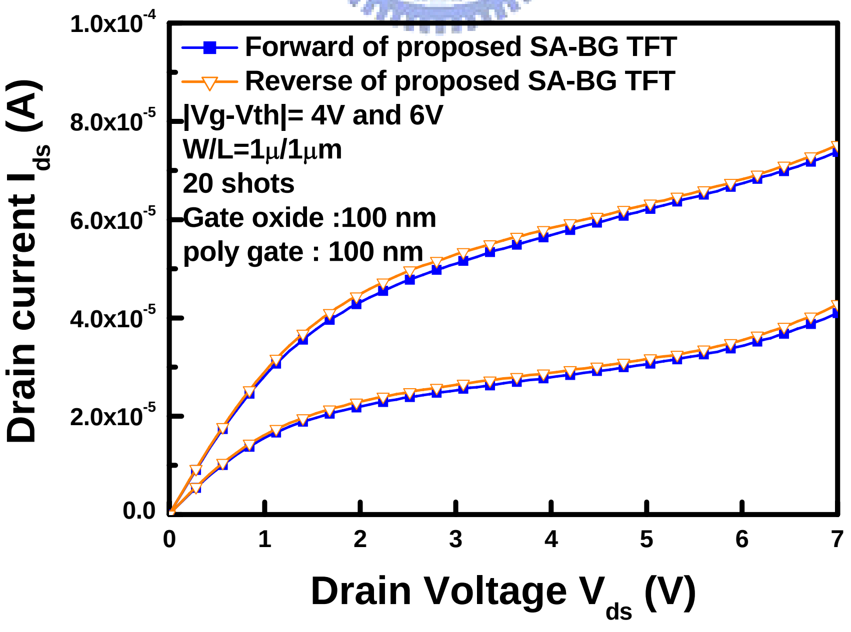


Figure 3-11 (a). Experimental measured bi-directional output characteristics of SA-BG TFT under the polarities of the source and drain are interchanged.

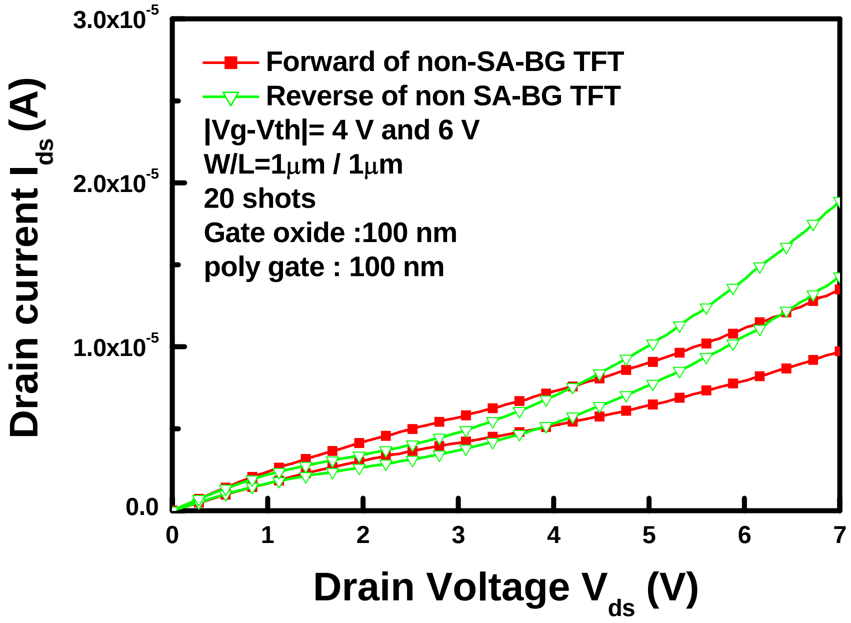


Figure 3-11 (b). Experimental measured bi-directional output characteristics of non-SA-BG TFT under the polarities of the source and drain are interchanged.

# Chapter 4

# High-Performance Short-Channel Double-Gate Low-Temperature Polycrystalline Silicon Thin Film Transistors Using Excimer Laser Crystallization

## 4.1 Introduction

Low-temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) fabricated by excimer laser crystallization (ELC) have been extensively studied for active matrix liquid crystal displays (AMLCDs), active matrix organic light emitting displays (AMOLEDs), and potential for 3-dimension integrated circuits applications owing to their superior mobility performance [4.1]-[4.3]. In recent years, many efforts has been devoted to producing LTPS TFTs with silicon-on-insulator-like (SOI-like) performance by improving the channel material quality and advanced device structures of poly-Si TFTs for system-on-panel applications [4.4]-[4.7]. Double gate structure is expected to be the alternative device structure for the ultimate high-performance ideal metal oxide semiconductor field effect transistors (MOSFETs). These devices possess the potential advantages of excellent control of short-channel effects (SCE), drain-induced-barrier-lowering (DIBL), larger on/off current ratio, and higher channel conductivity [4.8]-[4.17]. If this advanced structure is applied to polycrystalline-Si, the performance of TFTs will be also improved. From the perspective of improving channel quality, excimer laser crystallization (ELC) seems to be the most promising method at this moment for its great potential in mass production and high quality silicon grains without damage to glass substrates. Although large grains can be attained in the super lateral growth (SLG) regime by ELC, many fine grains still spread between these large grains due to the narrow process window for producing large-grain poly-Si [4.18]-[4.19]. Consequently, non-uniform and randomly distributed poly-Si grains will result in large variation of TFT performance when the laser energy density is controlled in the SLG regime, especially for small-dimension TFTs [4.20]-[4.21]. Thus, many laser crystallization methods have been proposed to produce large grains with uniformly grain size distribution, including SLS [4.22]-[4.23], grain filters method [4.24], capping the reflective or anti-reflective layer [4.25], phase-modulated ELC [4.26], dual beam ELA [4.27], double–pulsed laser annealing [4.28]-[4.29], selectively floating a-Si active layer [4.30], continuous-wave laser lateral crystallization [4.31]-[4.32], selectively enlarging laser crystallization [4.33]-[4.34], and so on. However, some of them need complex fabrication process or not readily be attached to the existing excimer laser annealing systems.

Shrinking the device size is an effective way to improving the device performance, but serious short-channel effects is encountered owing to the insufficient gate controllability and the numerous intra-grain and inter-grain defects in the poly silicon films. In this work, high-performance double-gate LTPS TFTs with lateral grain growth via a simple excimer laser crystallization method have been demonstrated. Because of the double gate operation mode and lateral silicon grains formed in the channel region, the devices have a high driving current, steeper subthreshold slope, superior short-channel effect immunity, and suppression of the floating-body effect. Moreover, not only the fabrication process steps are highly compatible with the conventional commercial a-Si TFTs but also the uniformity of device performance can be further improved. At first, the experimental process flows are described in detail. Next, the microstructure of ELC poly-Si thin film with double-gate structure and the completed devices are analyzed by TEM. The results of ELC DG LTPS TFT performance are presented and analyzed, demonstrating the performance and uniformity enhancement achieved by combing the new crystallization method with advanced structure. Moreover, we will also compare the electrical characteristics of top gate, bottom gate, and double gate devices crystallized with plateau structure.

## 4.2 Experiments

For the sake of simple analysis and comparison, a schematic cross-sectional view of the n-channel double-gate poly-Si TFT is shown in Figure 4-1(b) along with the conventional ELC top-gate TFT, as shown in Figure 4-1(a). The maximum process temperature of n-channel LTPS TFTs fabrication is 600°C for the dopant activation by furnace annealing. Figure 4-2 displays the key fabrication steps for the proposed double-gate short-channel LTPS TFTs structure crystallized with excimer laser annealing. At first, a 1000 Å-thick phosphorus-doped poly silicon layer was deposited by low-pressure chemical vapor deposition (LPCVD) by decomposition of pure silane ($SiH_4$) at 550°C on silicon wafer with oxide thickness of 1μm. After defining the bottom-gate region, a 1000 Å-thick tetraethyl orthosilicate (TEOS) bottom-gate oxide layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350°C following a 1000 Å-thick a-Si layer deposited by pyrolysis of pure silane ($SiH_4$) using LPCVD at 550°C. After standard RCA clean process, the samples were then subjected to 248nm KrF (Lambda Physik Excimer Laser LPX 210i) excimer laser crystallization (ELC). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to $10^{-3}$ Torr and substrate was maintained at room temperature. The laser beam was homogenized into a semi-gaussian shape in the short axis and a flat-top shape in the long axis. The number of laser shots per area was 20 (i.e. 95% overlapping) and laser energy density was varied. A scanning electron microscopy (SEM) (S4700, Hitachi) is used to get the surface micrograph of poly-Si thin films after

Secco-etching. After laser crystallization, the poly-Si active layers were etched to define the active channel region, and a 1000 Å-thick TEOS top-gate oxide was subsequently deposited by PECVD at 350°C. Phosphorus-doped poly-Si layer were deposited by LPCVD for formation of the top-gate electrode at 550°C. Then, the poly-Si thin films and were etched by transformer-coupled plasma reactive ion etching (TCP-RIE) to form top-gate electrodes and a phosphorous ion implantation with dose of $5\times10^{15}$cm$^{-2}$ was carried out to form source and drain regions. Next, a TEOS passivation oxide layer was deposited by PECVD at 350°C and the implanted dopants were activated by thermal annealing at 600°C for 12 h in the $N_2$ ambient. Contact hole opening and metallization were carried out to complete the fabrication of DG TFTs. Then, a 30-min sintering process was performed in the $N_2$ ambient at 400°C to reduce the contact series resistance of the source and drain electrodes. Finally, LTPS TFTs were passivated by 2-h $NH_3$ plasma treatment to further improve the device performance. For comparison, the conventional SPC DG TFTs and conventional ELC TG ones with using the super lateral growth (SLG) laser annealing condition were also fabricated in the same run. In addition, we have also fabricated the high-temperature processed TFT by the deposition of gate oxide by LPCVD at 700°C. All devices were characterized comparatively.

After TFTs formation, an automatic measurement system that combines IBM PC/AT, semiconductor parameter analyzer (4156C, Agilent Technologies) and a probe station were used to measure the I-V characteristics. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of Ids = (W/L) x $10^{-8}$ A at Vds = 0.1 V. The transconductance, field effect mobility and subthreshold swing were extracted at Vds = 0.1 V, and the Ion/Ioff current ratio was defined at Vds = 3 V. An analytical field-emission transmission electron microscopy (TEM) (JEM-2100FX, JEOL Ltd.) was employed to analyze the microstructure of poly-Si films and the device structure of DG TFTs. Cross-sectional TEM samples were prepared by focused-ion-beam (FIB) technique (Nova 200, FEI Company).

## 4.3 Results and Discussion

### 4.3.1 Material Characterization of Excimer Laser-Crystallized Double-Gate Low-temperature Poly-Si Thin Films Transistors

The schematic illustration of lateral grain growth mechanism using plateau structure of a-Si thin film with excimer laser crystallization is shown in the Figure 4-2. When the excimer laser irradiation is applied on the a-Si thin film, the applied laser energy density is controlled to completely melt the thin region of a-Si film in the channel region. Since the laser energy density is almost uniform in a local region, if the thickness of thick region of a-Si film near the edges of bottom gate is thick enough, the thick region of a-Si film is partially melted, and a lot of un-melting solid seeds remain near the edges of bottom gate electrode. As a result, a lateral temperature gradient can be produced between the local thin and thick regions of a-Si film, and grains will grow laterally towards the complete melting region from the un-melting solid seeds. Therefore, the lateral grain growth can be artificially controlled in the channel region of DG TFTs and only one grain boundary perpendicular to the direction of current flow is formed in the middle of the channel region.

Figure 4-3 (a) and 4-3 (b) display the low magnification, plane-view optical micrograph and high magnification, bird's-eye view SEM image of the completed excimer laser-crystallized double-gate LTPS TFTs. Figure 4-3 (c) exhibits the cross-sectional SEM graph of the completed excimer laser-crystallized double-gate LTPS TFTs. From the SEM graphs, the passivation layer, top-gate electrode, top-gate oxide, poly-Si channel, bottom-gate oxide, bottom-gate electrode, and the buffer oxide can be distinguished and indicated by the arrows.

Figure 4-4 is the cross-sectional TEM photograph of the completed DG device and energy dispersive X-ray (EDX) spectrometer investigated at the gate regions. According to the cross-sectional TEM image, the connection of the top-gate electrode and the bottom-gate electrode is fairly good. The energy dispersive X-ray (EDX) analysis is used to verify the atomic composition existing across the DG TFTs. The EDX results indicate that the top-gate poly-Si electrode and the bottom-gate poly-Si electrode are connected together by the Al metal.

Atomic force microscopy (AFM) analysis is used to investigate the surface morphology of silicon thin film after laser crystallization. Figure 4-5 exhibits that the ridge and hillock occur at the grain boundaries located at the center of channel where two grains collide due to the freezing of capillary waves excited in the melting silicon during laser crystallization [4.35]. The protruded grain boundaries may cause severe gate leakage and thicker gate dielectric must be integrated into poly-Si TFTs for better reliability.

In order to investigate the relationship between laser energy density and length of lateral grain growth, the channel length was adjusted to laser energy density of 450 mJ/cm$^2$ and laser shot number of 1 shot. Figure 4-6 (a) ~ 4-6 (c) show the SEM graphs of poly-Si thin films irradiated by excimer laser in which the device channel length was 1.2, 1.5, 2 μm, respectively. As the device channel length was less than 1.5 μm, there were always two columns of longitudinal grains colliding in the middle of channel region.

Figure 4-7 displays the cross-sectional transmission electron microscopy (TEM) photograph to analyze the microstructure of excimer laser crystallized poly-Si films, the gate-stacked structure of double-gate TFT with gate length of 1.2 μm, and the selected-area electron diffraction patterns of the fabricated ELC double-gate poly-Si TFTs. The thickness of top-gate electrode, top-gate oxide, poly-Si channel layer, bottom-gate oxide, and the bottom-gate electrode all are 100 nm. In this case, the laser shot number is 20 shots and the substrate temperature is maintained at room temperature during laser irradiation. It is observed that a spatially-controlled silicon grain with 0.60 μm in length formed in the channel region via the super lateral growth phenomenon using excimer laser irradiation with the plateau structure, shown in the inseted top-view scanning electron microscopy (SEM) image of excimer laser crystallized poly-Si films shown in the Fig. 4-7. According to the TEM image in the Figure 4-7, there are two large silicon grains formed in the channel region above the bottom-gate electrode and only single grain boundary perpendicular to the channel direction can be artificially controlled in the middle of the channel region. The inset also shows the high-resolution cross-sectional TEM image of the grain boundary region in the middle of the channel region. The inset of Fig. 4-7 also depicts the selected-area electron diffraction patterns of the one of lateral silicon grains in the channel regions above the bottom-gate electrode, the top-gate poly-Si electrode, and the bottom-gate poly-Si electrode, respectively. The diffraction pattern reveals that the lateral silicon grain in the channel region exhibits <123> orientation with respect to the normal direction of the paper and the crystallinity within this lateral silicon grain is excellent attributed to the clear dot pattern as compared with the top-gate poly-Si electrode and bottom-gate poly-Si electrode crystallized by solid phase crystallization. Moreover, the originally thicker a-Si films around the edges of step height caused by bottom gate become thinner and smoother. This phenomenon is attributed to two mechanisms which are the reflow of molten silicon into the sunken regions during excimer laser annealing and the capillary waves excited by the volume change at the silicon melt transition.

### 4.3.2 Electrical Characterization of Excimer Laser-Crystallized Double-Gate Low-temperature Poly-Si Thin Films

### Transistors

Figure 4-8 (a) and 4-8(b) show the typical transfer and output characteristics of proposed ELC DG LTPS TFT (Fig. 4-1 (b)) and conventional SPC DG TFT and conventional ELC TG TFT (Fig. 4-1(a)) for W = L = 1 μm. The nominal mobility of the DG TFT was calculated from transconductance ($g_m$), which we defined as a TG TFT of the same gate length and gate width with a 100 nm gate-$SiO_2$ layer. Owing to both of the uniformly large transverse grains grown in the device channel region and double-gate operation mode, this proposed ELC DG TFT exhibits better electrical characteristics than conventional SPC DG TFT and conventional ELC TG TFT. Table 4-1 lists several important electrical characteristics of these there different TFTs. Via the top and bottom gates connected together, the higher electron density in the channel region at on state and the channel is more efficiently modulated by both gate electrodes [4.36]. Obvious improvement in devices characteristics is obtained for ELC DG TFTs instead of ELC TG TFTs, the threshold voltage decreases from -1.60 to -1.55 V, SS decreases from 0.258 to 0.172 V/dec, field-effect-mobility increases from 186 to 550 $cm^2/Vs$, $I_{on}/I_{off}$ increases from $4.37\times 10^{7}$ to $4.35\times 10^{8}$ , and DIBL decreases from 0.241 to 0.075. Because the top and bottom gates are symmetrical, in which the gate oxide thickness is the same, and connect together electrically to obtain a perfect coupling between the surface potential in the channel region and the gate. Consequently, the influence of the source and drain depletion regions are kept minimal, which in turn reduce the short channel effects by screening the source and drain electrical field lines away from the channel. In addition, lateral silicon grains formed in the channel region as the bottom-gate TFTs is obtained, the DG devices have a higher driving current, steeper subthreshold slope, smaller drain-induced-barrier-lowering, superior short-channel effect immunity, and suppression of the floating-body effect. But the proposed ELC DG TFT has a high off-current under a large negative gate bias at the Vds = 3 V from the Id-Vg transfer characteristics. The large leakage current indicates that ELC DG TFTs suffer a higher lateral peak electric field than the ELC TG TFT [4.37]. If offset, lightly-doped-drain (LDD) and gate-overlapped lightly-doped-drain (GOLDD) structures were applied to the ELC DG TFTs, the severe anomalous off-current could be relieved by reducing the lateral peak electric field in the drain region [4.38]-[4.45]. In order to avoid the threshold voltage difference, the applied gate driving voltages in Figure 4-8 (b) are kept at constant values of |Vg-Vth| = 4, 8, 12 and 16 V, respectively. It is demonstrated that the ELC DG poly-Si TFTs exhibit higher driving capability due to both of the location-controlled silicon grains in the channel and double-gate operation mode. Take the |Vg-Vth| = 8 V as an example, the current drivability of ELC DG poly-Si TFTs is about 2.1 times as large as that of an ELC TG poly-Si TFT and 18.1 times as large as that of a SPC DG poly-Si TFT under the same bias condition. At higher gate voltages, however, the current ratio between these three devices decreases. The plausible reason is the self-heating effect due to the large driving current on the poor thermal conducting $SiO_2$ substrate. It also clearly shows that ELC DG poly-Si TFTs provide better current saturation characteristics than the other two TFTs. The superior short channel characteristics and driving capability imply that the proposed ELC DG-TFT structure is more suitable for high-resolution active matrix liquid crystal displays, active matrix organic light emitting displays, and device scaled-down applications.

The grain boundary trap state densities (Nt) of the conventional TG and proposed DG poly-Si TFTs were estimated according to the modified Levinsons analysis [4.46]-[4.47]. The Nt was extracted from the slopes of $\ln(I_D/V_{GS})$ versus $1/(V_{GS})$ at $V_{DS}=0.1$ V and high $V_{GS}$. Figure 4-9 displays that ELC DG poly-Si TFT exhibits the Nt of $9.72\times 10^{10}$ $cm^{-2}$ four times smaller that of conventional ELC TG TFT. This result implies that DG TFTs with lateral silicon grains possess better crystallinity and fewer microstructure defects which are also confirmed by cross-sectional TEM image of excimer laser crystallized poly-Si thin films with double-gate structure shown in the Figure 4-10.

The dependence of field effect mobility on temperature for ELC DG TFTs with lateral silicon grains, ELC TG TFTs with random silicon grains and SPC DG TFTs was investigated to study the electron-transport-scattering mechanism of poly-Si thin films, as shown in the Figure 4-11. For ELC TG TFTs with random silicon grains, the electron field-effect-mobility increases as the temperature increases. Such positive temperature dependency of field-effect-mobility is attributed to the reduced grain boundary scattering where the probability of carrier transport over the grain boundary potential barrier height by thermionic emission increases [4.48]-[4.49]. On the other hand, negative dependency of field-effect-mobility for ELC DG TFTs with lateral silicon grains indicates lattice-phonon scattering is the dominate scattering mechanism because only one grain boundary perpendicular to the direction of current flow in the channel region [4.50]. The field-effect-mobility of SPC DG TFTs increase as first and then starts to decrease as the temperature increases, indicating grain-boundary scattering and lattice-phonon scattering compete with each other and dominate under different temperature.

Figure 4-12 displays the dependence of field effect mobility on laser energy densities for DG TFTs and conventional TG ones whose channel length is 1 μm. Twenty TFTs were measured for each laser irradiation condition to investigate the device-to-device uniformity. Compared to the conventional ELC TG-TFTs, it was found that ELC DG-TFTs with lateral silicon grains exhibited smaller electrical deviation since the number of spontaneous small grains and grain boundaries were reduced and the uniformity of TFTs performance could be improved with artificially laterally-grown grains.

The device transfer and output characteristics of high-temperature and low-temperature DG TFTs are shown in Figure 4-13 (a) and 4-13 (b), respectively. Some important electrical characteristics of LTPS TFTs are also listed in Table 4-2. Opened curves are for the low-temperature processed DG TFTs with PECVD gate oxide at 350 ℃. The field-effect mobility was 550 cm$^2$/Vs at Vds = 0.1 V. The off current was 1 pA/µm at Vds = 3 V. The on–off current ratio was 4.30x 10$^8$. Threshold voltage was -1.55 V, and a subthreshold swing 0.180 V/decade, respectively. The output characteristic shows the kink current was mostly suppressed. Characteristics are also shown in Fig. 4-13 (a) by solid curves for the high-temperature processed TFT. The field-effect mobility was 1050 cm /Vs, the off current 0.2 pA/µm, the threshold voltage -2.58 V, the subthreshold voltage swing 0.166 V/decade, and DIBL 0.059 V/V, respectively.

The high field-effect mobility means that the single high angle grain boundary in the middle of the channel region does not disturb seriously the carrier drift transportion. And the low off current implies that the crystallinity and defect density of the grain at the drain region is pretty good and low. For the kink effect, there is also a room for perfect killing, since deep traps at the grain-boundary can act more effectively as carrier recombination centers, if the Si film thickness is reduced from 100 nm. In addition, we speculated that the further improved performance for the high temperature processed TFT with LPCVD gate oxide came predominantly from the better quality gate insulator and the thermally annealing of the insulator-semiconductor interface. Thus, we expect that the low-temperature TFT performance can be improved by better cleaning process and deposition process of high-quality $SiO_2$. Figure 4-14 displays the basic electrical characteristics of the n-channel and p-channel ELC DG LTPS TFTs with LPCVD gate oxide. Some important electrical characteristics of high-temperature processed ELC DG LTPS TFTs are also listed in Table 4-3. Ultra high-performance ELC DG LTPS TFTs with field effect mobility of 1050 cm$^2$/V-s for n-channel and 484 cm$^2$/V-s for p-channel, substhreshold swing of 166 mV/dec for n-channel and 96 mV/dec for p-channel, on/off current ratio more than 10$^9$ for n-channel can be achieved. These values are superior to those of single-crystal silicon MOSFET.

Proposed double-gate TFTs are less prone to the self-heating effect than the conventional single-gate TFTs, shown in Figure 4-13 (b). Indeed, single-gate TFTs are thermally isolated from the substrate owing to the thick buried oxide, which exhibits a low thermal conductivity. In the case of double-gate TFTs, the device channel regions are isolated from the substrate by the top-gate electrode, bottom-gate electrode, and two thin gate-oxide layers, which exhibit a much better thermal conductivity path to the substrate than a thick buried oxide. Thus, in spite of the high driving current in the double-gate TFTs, slightly self-heating effect is observed in DG TFTs.

Figure 4-15 (a) shows the comparison of the transfer characteristics of top gate, bottom gate and double gate devices crystallized by ELC with plateau structure in which the channel length is 1μm and P-type carrier. It is found that the on current is enhanced with the double-gate TFTs. For the comparison of bottom gate and top gate devices, the current drive in the single gate operation is not the same between the top-gate and bottom-gate devices. This is considered to be attributed to the asymmetrical channel structure resulting from the process steps of device fabrication. The top gate TFTs exhibit higher field-effect mobility than bottom gate ones. This might arise from the fact that the TG device is a self-aligned structure during ion implantation of source/drain regions, while the BG device is a non-self-aligned structure. Therefore, the parasitic resistance in TG device is smaller than that of BG device and the TG exhibit higher performance than BG one. For the comparison of double gate devices and top/bottom gate devices, we could refer to the extracted electrical characteristics listed in Table 4-4. The steeper subthreshold swing and smaller DIBL reveal the enhanced gate controlling ability of double gate structure. The equivalent field-effect mobility of p-channel double gate TFTs was 484cm$^2$/V-s, while that of p-channel top gate TFTs and p-ahannel bottom gate TFTs was 221cm$^2$/V-s and 130cm$^2$/V-s, respectively. The driving current of double gate devices is higher than the sum of top gate and bottom gate devices, as shown in Figure 4-15(b). This phenomenon indicates that the top-gate electrode and bottom-gate electrode are well-coupled and give both influences on the channel carrier density in the double-gate TFTs.

## 4.4 Summary

A novel high-performance DG LTPS TFTs have been fabricated by excimer laser crystallization. The microstructure of poly-Si films and the completed device structure were analyzed by an analytical transmission electron microscopy. Because the top and bottom gates are symmetrical, in which the gate oxide thickness is the same, and connect together electrically to obtain a perfect coupling between the surface potential in the channel region and the gate. Consequently, n-channel DG LTPS TFTs exhibit high field-effect-mobility of 550 $cm^2/Vs$, SS of 0.172 V/dec, $I_{on}/I_{off}$ of $4.35\times 10^8$, and DIBL of 0.075 and excellent short channel characteristics because of the large transverse grains artificially grown in the channel region and double-gate structure for better gate controllability. In addition, the experimental results reveal a steeper subthreshold value, smaller drain-induced-barrier-lowering, higher driving current, suppression of the floating-body effect, and excellent device uniformity in proposed DG TFTs. Moreover, ELC DG LTPS TFTs (W/L = 1/1 μm) with high-temperature processed LPCVD gate oxide have the equivalent field-effect-mobility exceeding 1050 $cm^2/Vs$ for the n-channel device, 484 $cm^2/Vs$ for the P-channel device, substhreshold swing of 166 mV/dec for n-channel and 96 mV/dec for p-channel, on/off current ratio higher than $10^8$ for both structures, smaller DIBL (59 mV/V) for n-channel ones, DIBL (33 mV/V) for p-channel ones. We also compare the electrical characteristics of top gate, bottom gate and double gate devices crystallized by ELC with plateau structure in which the channel length is 1μm and P-type carrier. From the experimental results, the performances are greatly improved in the double-gate TFTs as compared with the top-gate TFTs and bottom-gate TFTs. The larger on current, higher field-effect mobility, steeper subthreshold swing and smaller DIBL reveal the enhanced gate controlling ability of double gate structure. The ELC DG TFTs are, therefore, ideally suitable for future system-on-panel and 3 dimensional integrated circuit applications.

**Table 4-1**

Measured electrical characteristics of ELC DG TFTs with lateral grain growth, SPC DG TFTs, and conventional ELC TG TFTs.

| TFT Structures (W=L=1um) N-channel | Threshold Voltage (V) | Field-effect mobility (cm$^2$/Vs) | Subthreshold Swing (V/dec) | DIBL (V/V) | On/off current ratio |
|---|---|---|---|---|---|
| **Proposed ELC DG TFT** | -1.55 | 550 | 0.180 | 0.075 | 4.30x $10^8$ |
| **Conventional ELC TG TFT** | -1.60 | 186 | 0.258 | 0.241 | 4.37x $10^7$ |
| **Proposed SPC DG TFT** | 1.91 | 40.0 | 0.850 | 0.414 | 7.50x $10^6$ |

**Table 4-2**

Measured electrical characteristics of ELC DG TFTs with high-temperature LPCVD gate oxide and ELC DG TFTs with low-temperature PECVD gate oxide.

| TFT Structures (W=L=1um) | Threshold Voltage (V) | Field-effect-mobility (cm$^2$/Vs) | Subthreshold Swing (V/dec) | DIBL (V/V) | On/off current ratio |
|---|---|---|---|---|---|
| **PECVD TFT** | -1.55 | 550 | 0.180 | 0.075 | 4.30x $10^8$ |
| **LPCVD TFT** | -2.58 | 1050 | 0.166 | 0.059 | 3.78x $10^9$ |

**Table 4-3**

Measured electrical characteristics of high-temperature processed n-channel and p-channel ELC DG TFTs with lateral grain growth.

| TFT Structures (W=L=1um) | Threshold Voltage (V) | Field-effect-mobility (cm$^2$/Vs) | Subthreshold Swing (mV/dec) | DIBL (V/V) | On/off current ratio |
|---|---|---|---|---|---|
| LPCVD p-channel TFT | -1.83 | 484 | 96 | 0.034 | 1.10x $10^8$ |
| LPCVD n-channel TFT | -2.58 | 1050 | 166 | 0.059 | 3.78x $10^9$ |

**Table 4-4**

Measured electrical characteristics of ELC DG TFTs with lateral grain growth, ELC TG TFTs with lateral grain growth, and ELC BG TFTs with lateral grain growth.

| TFT Structures (W=L=1um) P-channel | Threshold Voltage (V) | Field-effect mobility (cm$^2$/Vs) | Subthreshold Swing (V/dec) | DIBL (V/V) | On/off current ratio |
|---|---|---|---|---|---|
| Proposed ELC DG TFT | -1.83 | 484 | 0.096 | 0.034 | 1.10x $10^8$ |
| Proposed ELC TG TFT | -2.17 | 221 | 0.159 | 0.052 | 1.23x $10^8$ |
| Proposed ELC BG TFT | -4.45 | 130 | 0.238 | 0.210 | 5.47x $10^7$ |

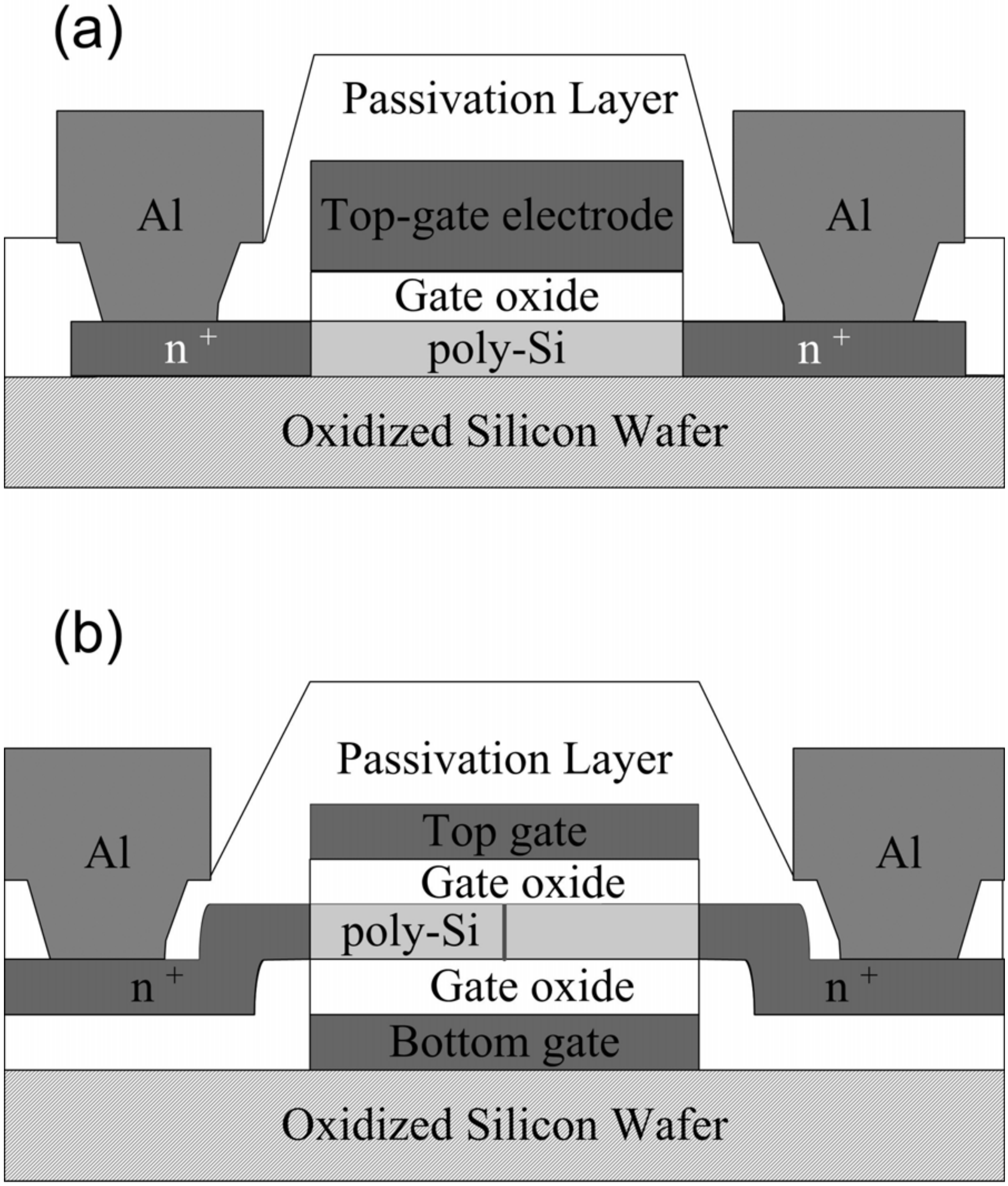


Figure 4-1. The schematic cross-sectional view of the different poly-Si TFT devices. (a) Conventional n-channel top-gate TFT and (b) n-channel DG TFT.

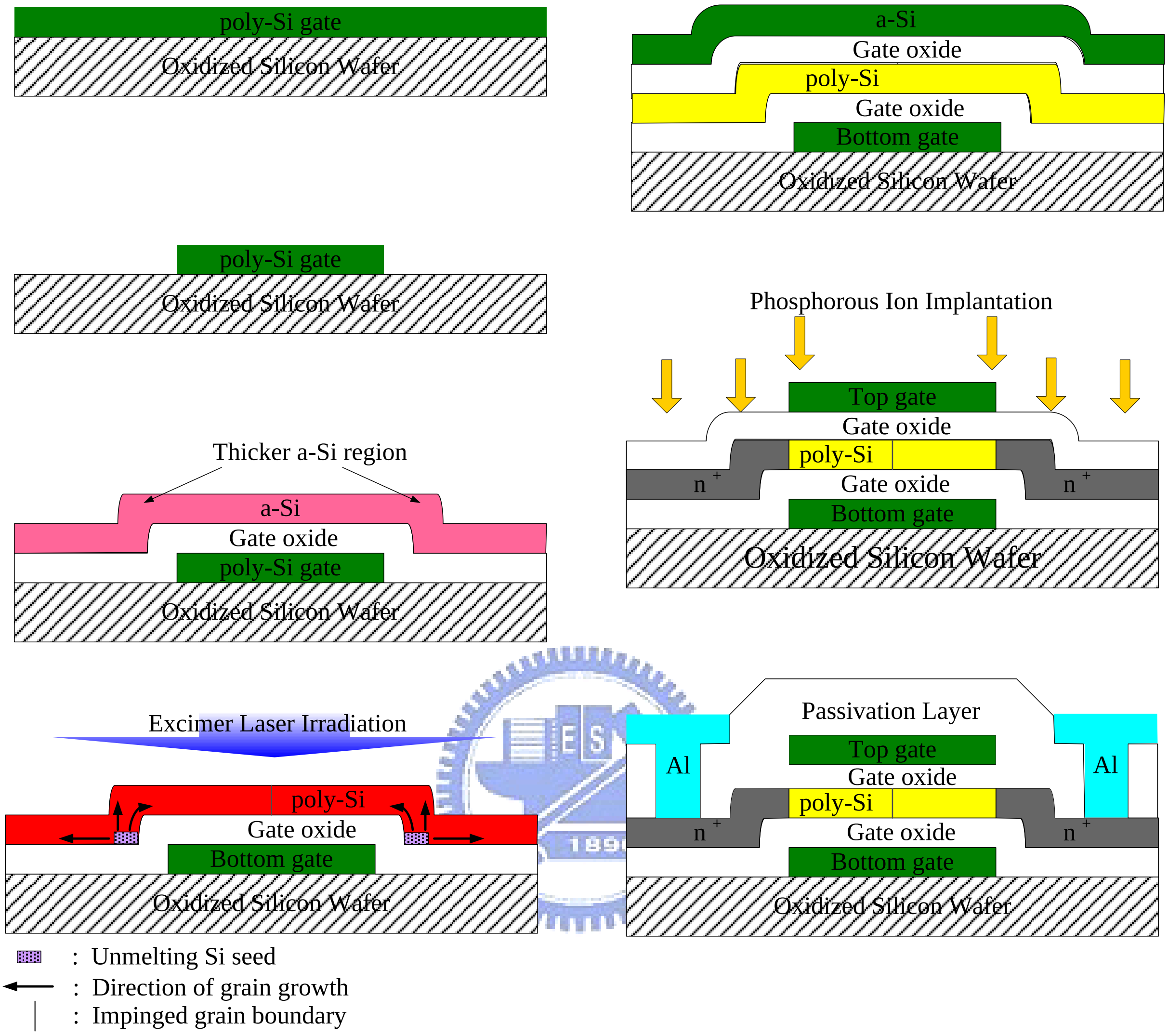


Figure 4-2. The key fabrication process steps for the proposed short-channel double-gate LTPS TFTs structure crystallized with excimer laser annealing.

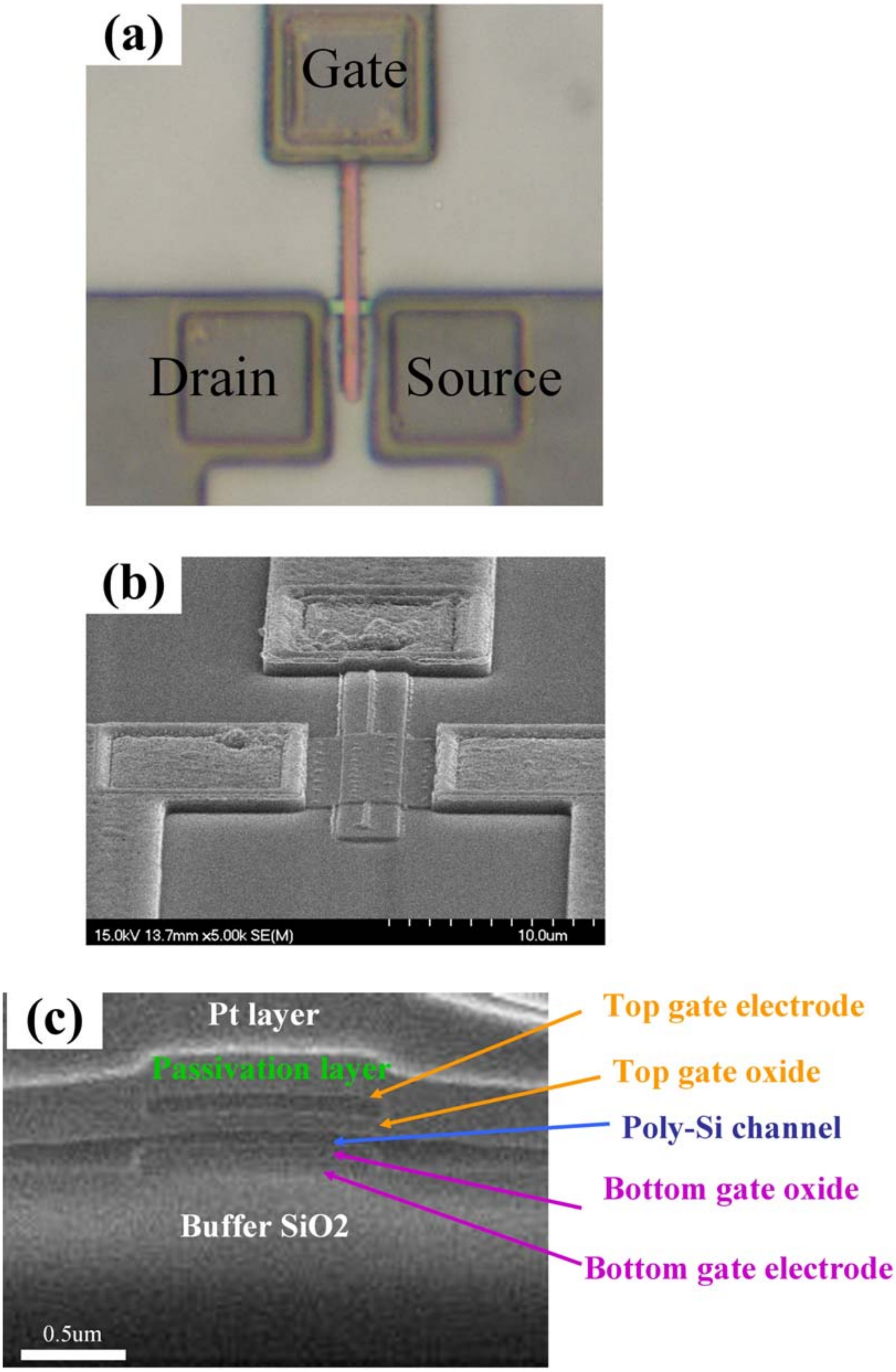


Figure 4-3. (a) The optical micrograph, (b) the bird-eye SEM graph, and (c) the cross-sectional SEM graph of proposed excimer-laser-crystallized double-gate LTPS TFTs.

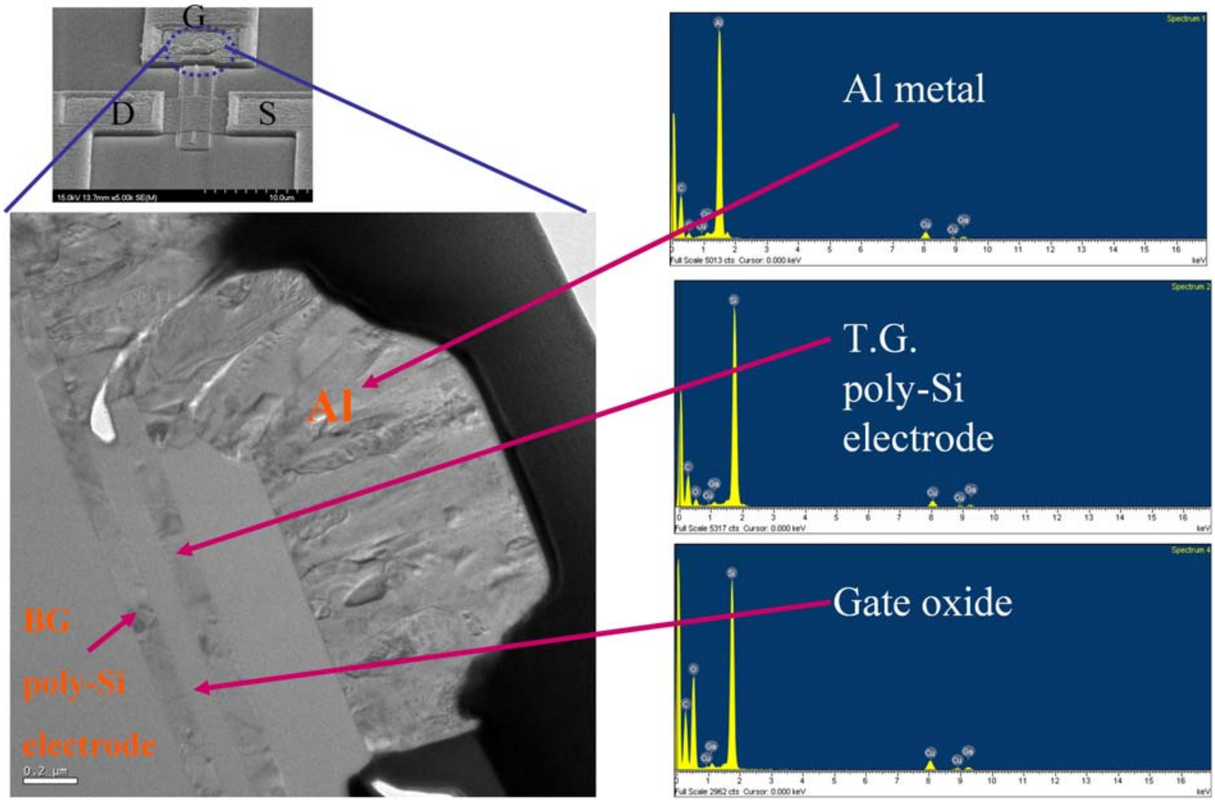
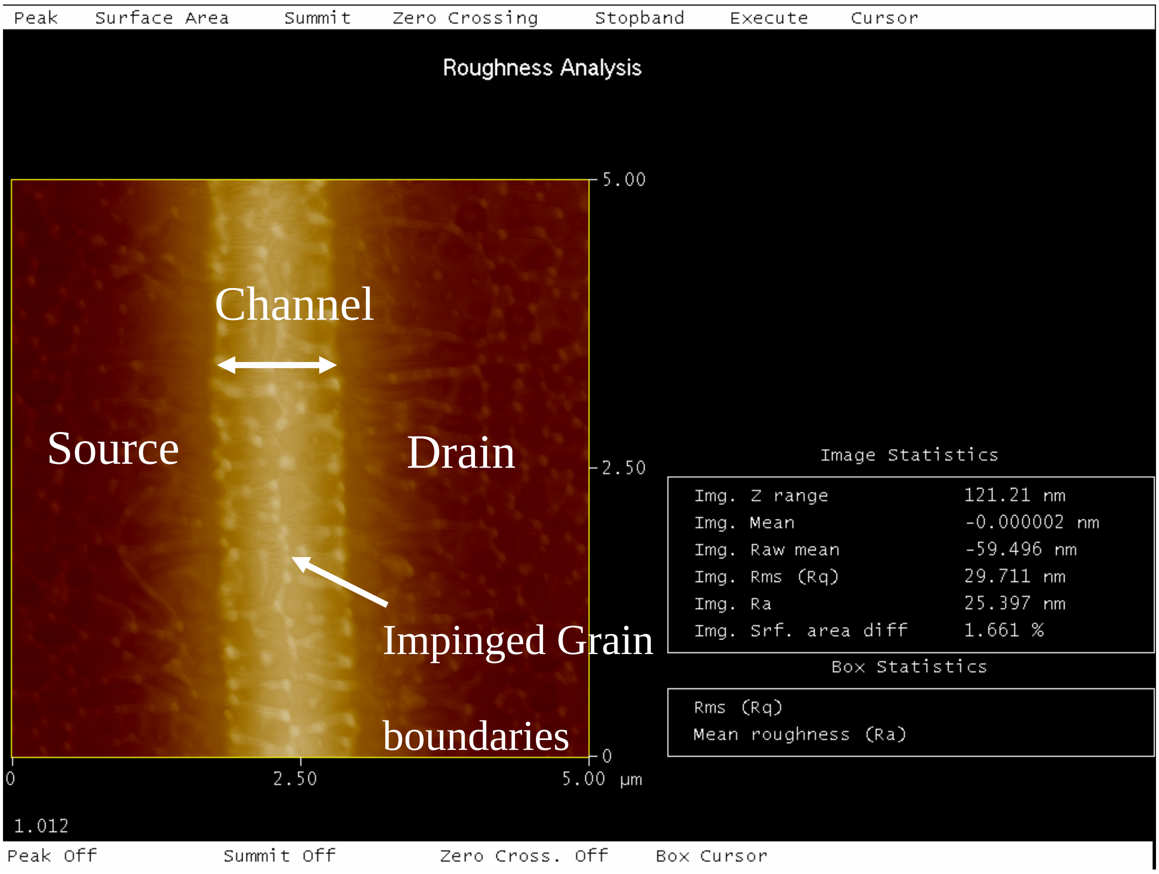


Figure 4-4. The Cross-sectional TEM photograph of connection of the top-gate electrode and the bottom-gate electrode and energy dispersive X-ray (EDX) Spectrometer analyses.



```
Image Statistics
Img. Z range              121.21 nm
Img. Mean                 -0.000002 nm
Img. Raw mean             -59.496 nm
Img. Rms (Rq)             29.711 nm
Img. Ra                   25.397 nm
Img. Srf. area diff       1.661 %
Box Statistics
Rms (Rq)
Mean roughness (Ra)
```

Figure 4-5. Atomic force microscopy (AFM) images of poly-Si thin film with bottom-gate structure after laser irradiation.

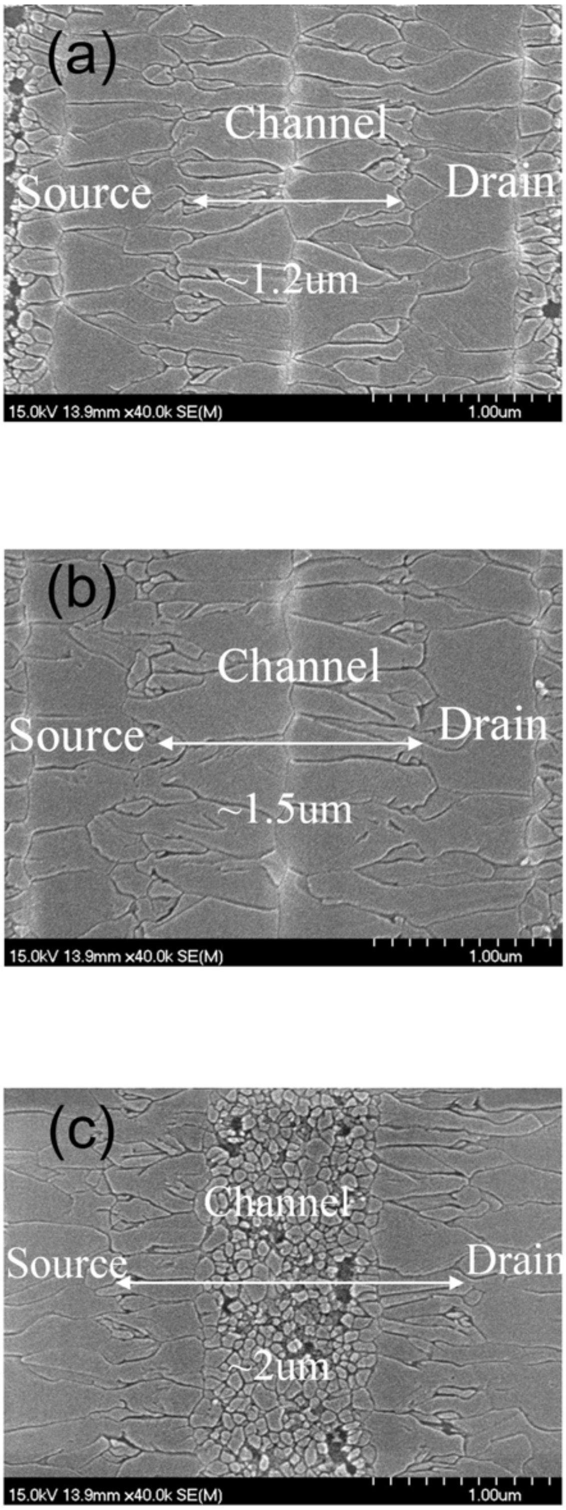


Figure 4-6. Scanning electron microscope (SEM) micrographs of excimer laser crystallized poly-Si film with bottom-gate structure after Secco etching, in which the device channel length was (a) 1.2, (b) 1.5, and (c) 2 μm, respectively.

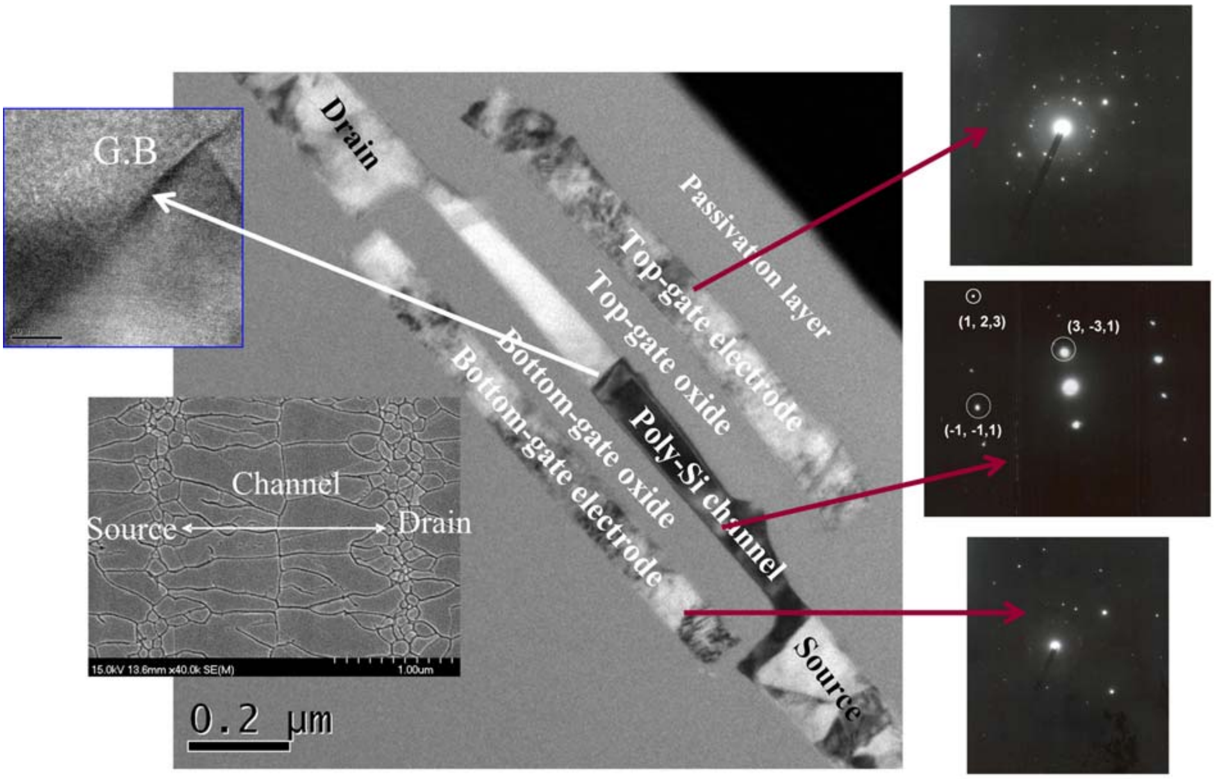


Figure 4-7. The cross-sectional TEM image and the selected-area electron diffraction patterns of the fabricated ELC double-gate poly-Si TFTs. The channel length of DG TFTs is 1.2 μm. The thickness of top-gate electrode, top-gate oxide, poly-Si channel layer, bottom-gate oxide, and the bottom-gate electrode all are 100 nm. The insets show the top-view SEM graph of excimer laser-crystallized poly-Si thin films with bottom-gate structure and the high-resolution cross-sectional TEM image of the grain boundary region.

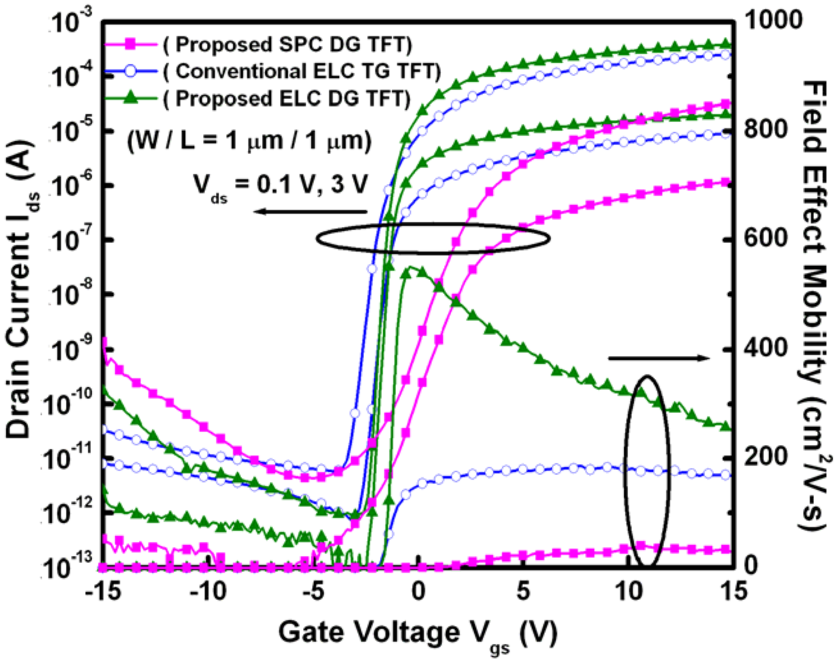


Figure 4-8 (a). Transfer characteristics of proposed ELC DG TFT, conventional SPC DG TFT, and conventional ELC TG TFT.

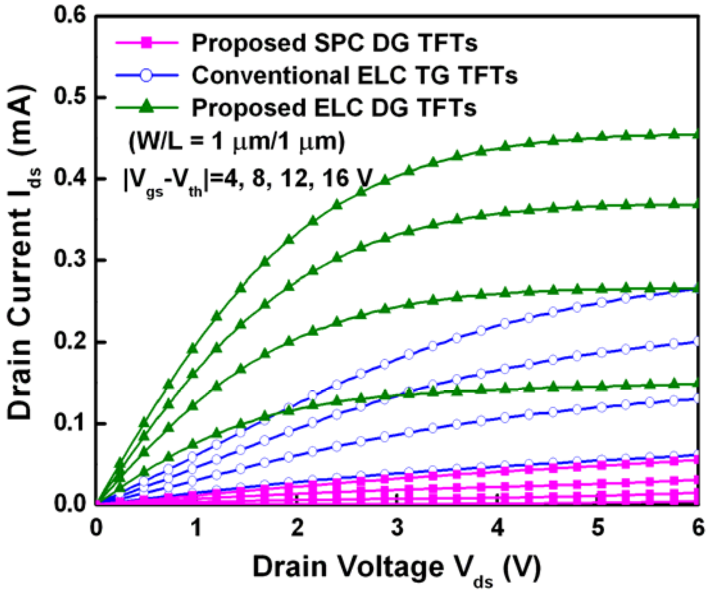


Figure 4-8 (b). Output characteristics of proposed ELC DG TFT, conventional SPC DG TFT, and conventional ELC TG TFT.

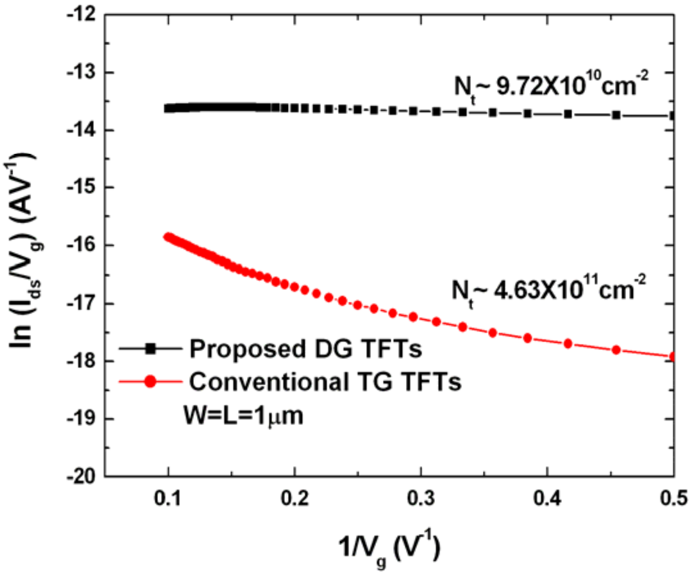


Figure 4-9. Plot of ln($I_D$/$V_{GS}$) versus 1/($V_{GS}$) curves at $V_{DS}$ = 0.1 V and high $V_{GS}$ for DG poly-Si TFTs and conventional TG ones.

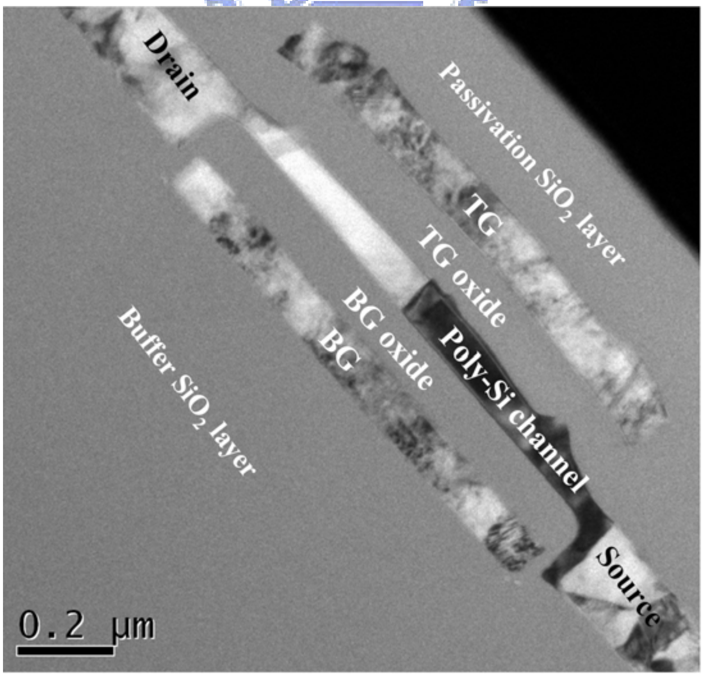


Figure 4-10. FIB-prepared cross-sectional TEM image of excimer laser crystallized DG poly-Si TFTs.

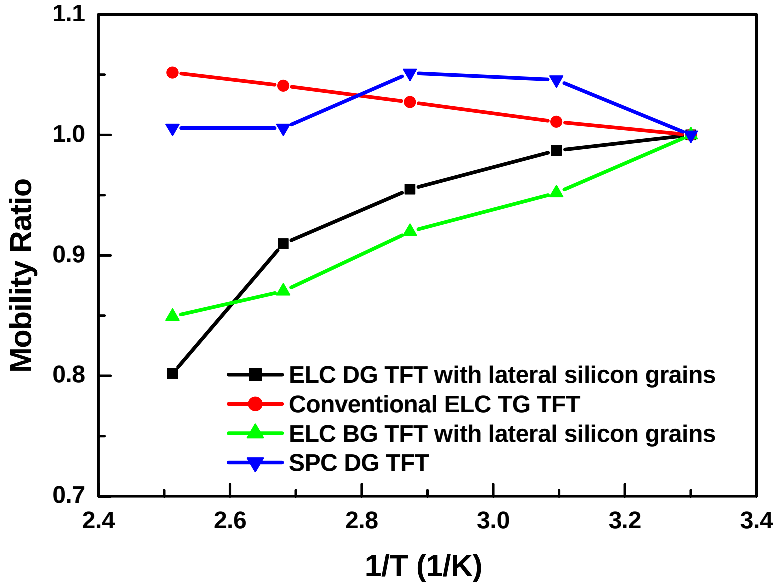


Figure 4-11. The dependence of field effect mobility on temperature for ELC DG TFTs with lateral silicon grains, ELC TG TFTs with random silicon grains and SPC DG TFTs.

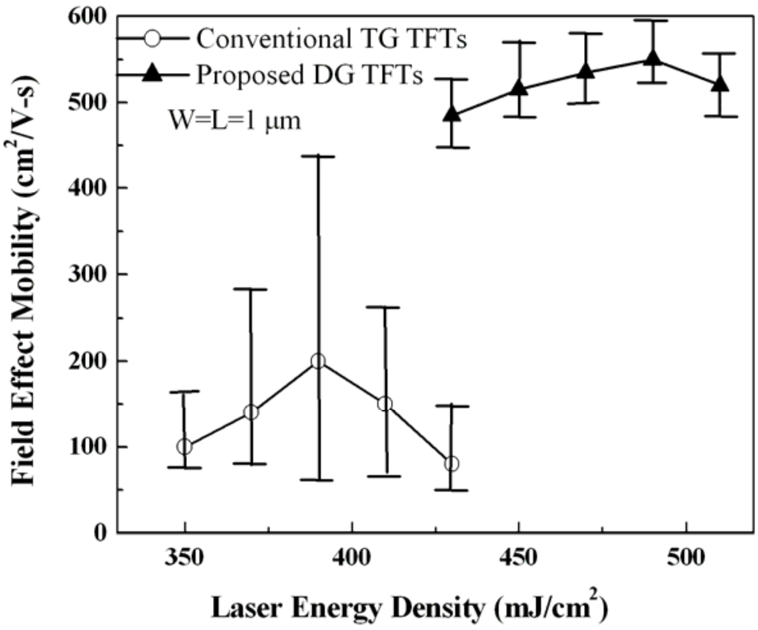


Figure 4-12. Dependence of field-effect mobility on applied laser energy density for ELC DG TFTs with lateral silicon grins and conventional ELC TG ones.

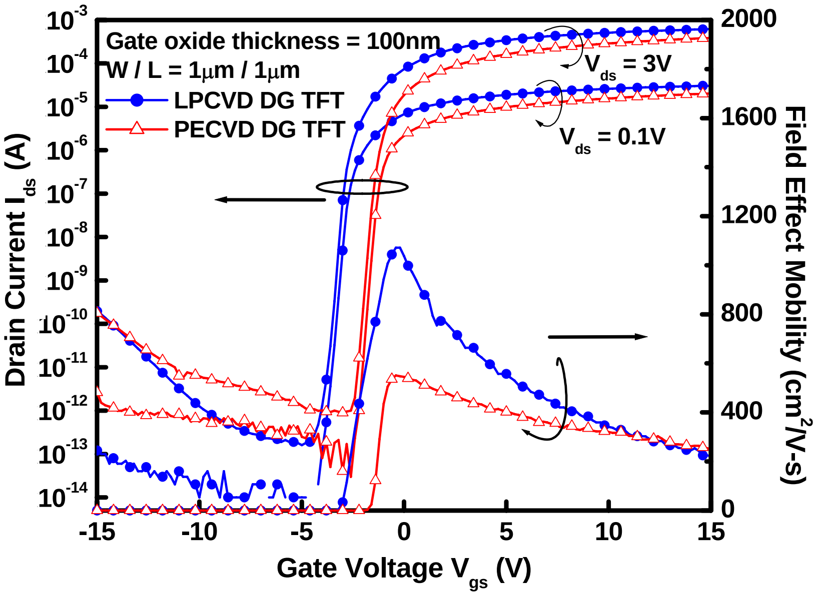


Figure 4-13 (a). Transfer characteristics of proposed high-temperature ELC DG TFT with LPCVD gate oxide and proposed low-temperature ELC DG TFT with PECVD gate oxide.

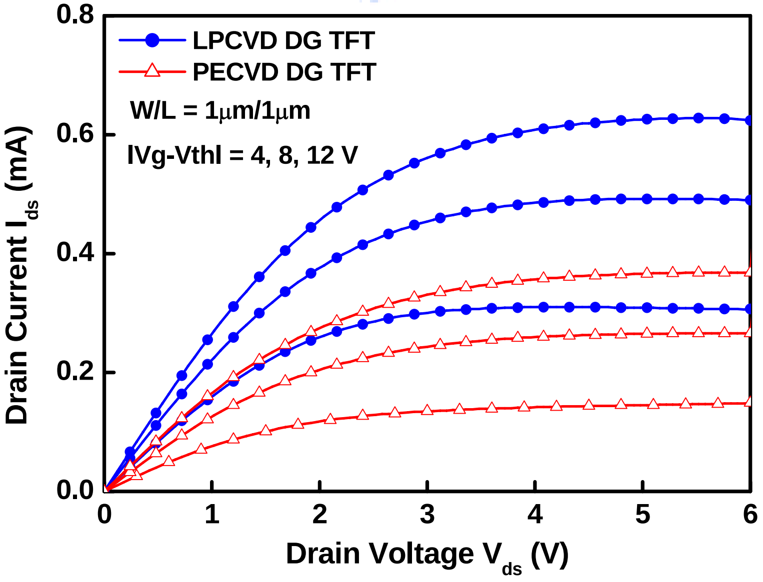


Figure 4-13 (b). Output characteristics of proposed high-temperature ELC DG TFT with LPCVD gate oxide and proposed low-temperature ELC DG TFT with PECVD gate oxide.

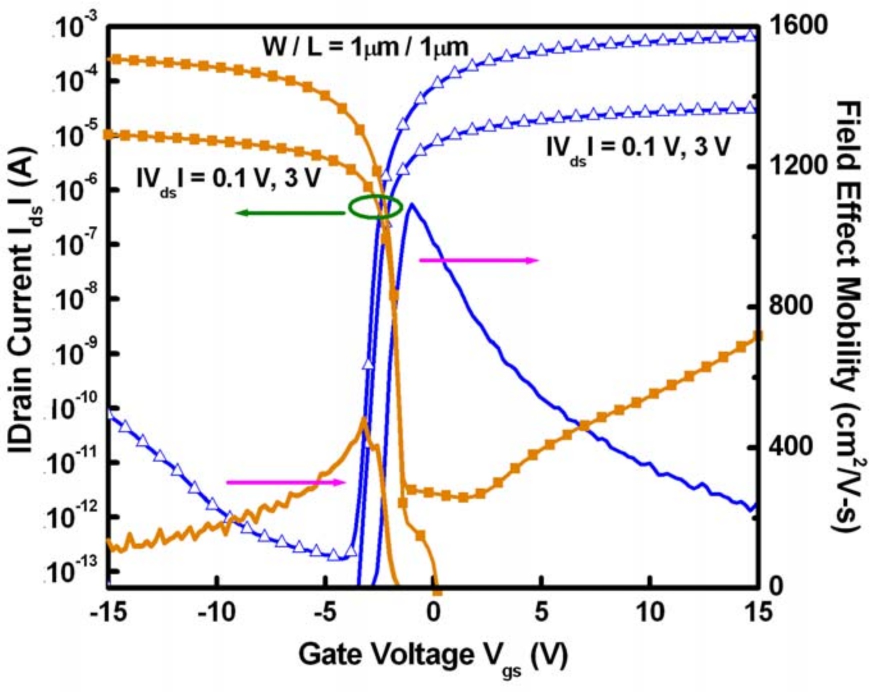


Figure 4-14(a). Transfer characteristics of high-temperature processed n-channel and p-channel ELC DG LTPS TFT with LPCVD gate oxide.

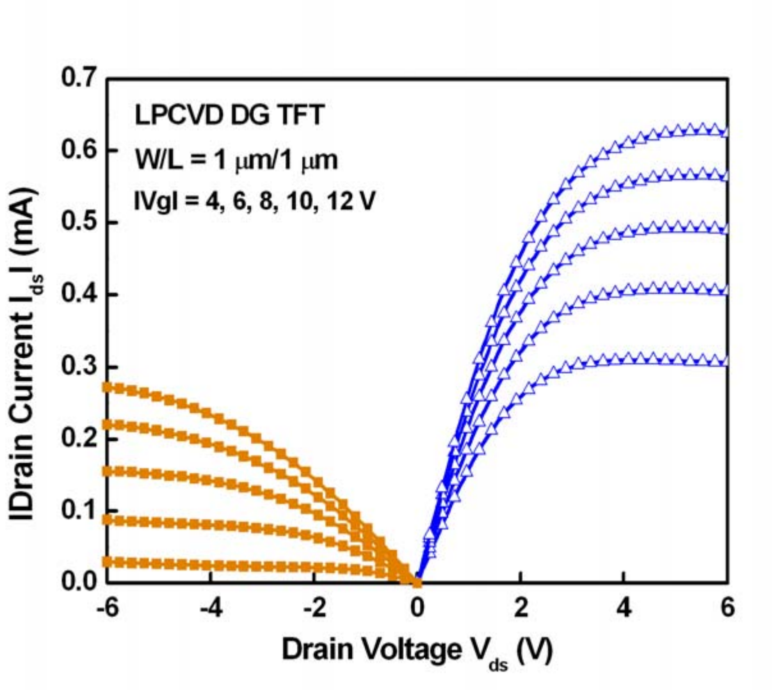


Figure 4-14(b). Output characteristics of high-temperature processed n-channel and p-channel ELC DG LTPS TFT with LPCVD gate oxide.

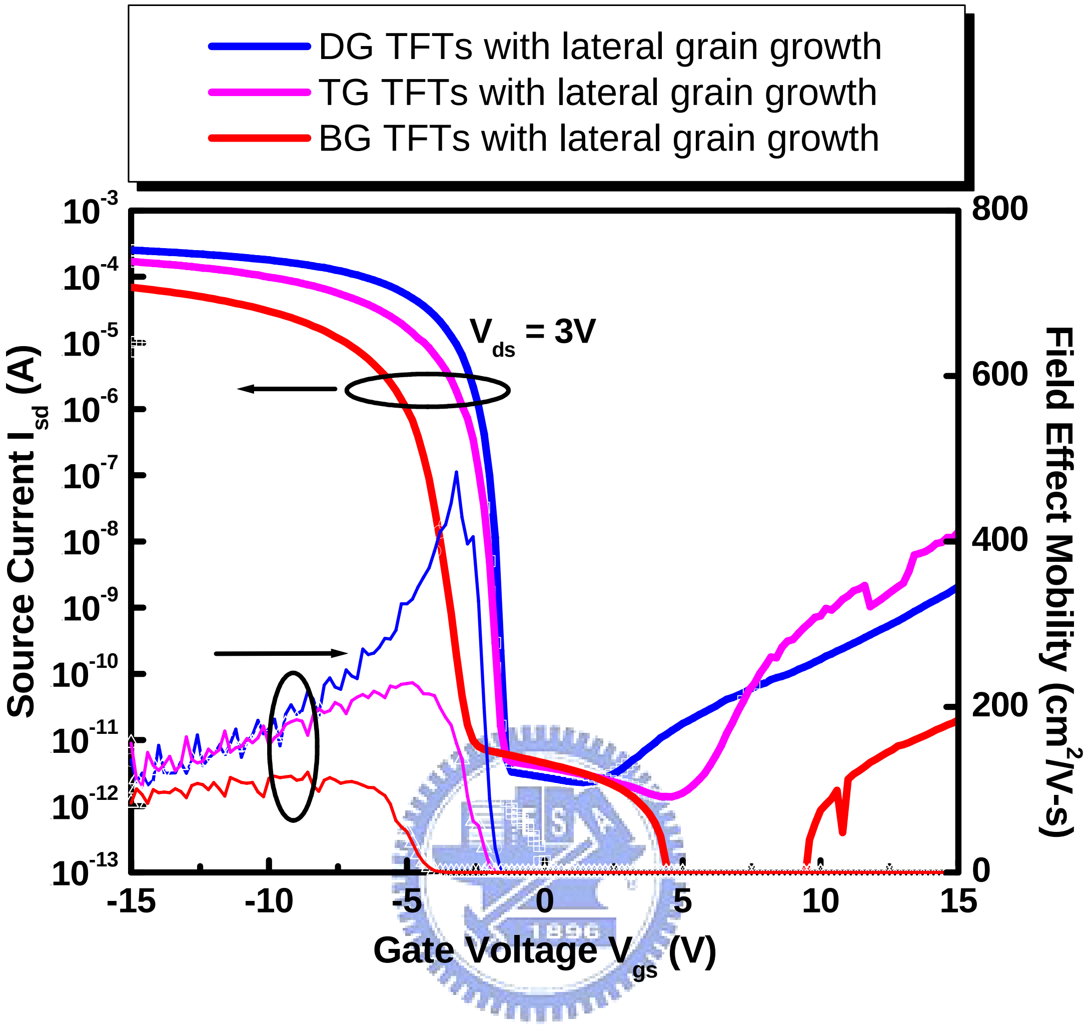


Figure 4-15 (a). Transfer characteristics of proposed p-channel ELC DG TFT, proposed p-channel ELC TG TFT, and proposed p-channel ELC BG TFT which are crystallized with plateau structure.

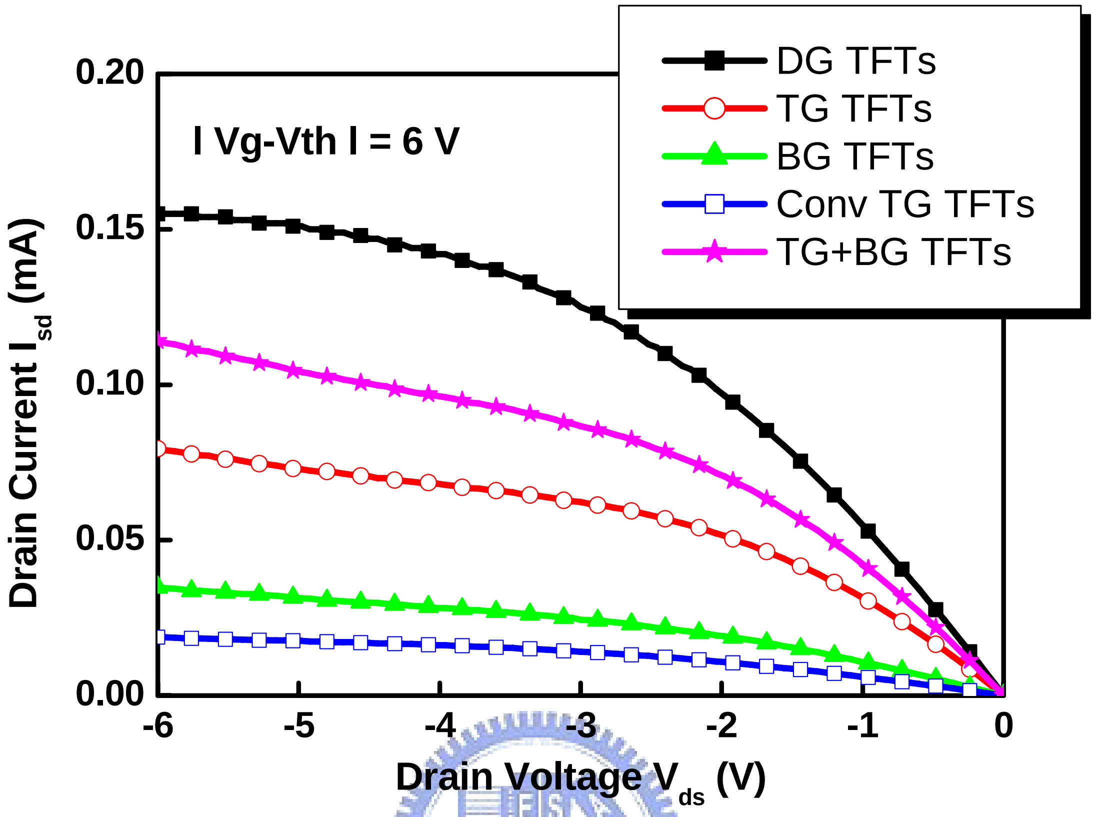


Figure 4-15 (b). Output characteristics of proposed p-channel ELC DG TFT, proposed p-channel ELC TG TFT, and proposed p-channel ELC BG TFT which are crystallized with plateau structure, and conventional p-channel TG TFT.

# Chapter 5

# Periodically Lateral Silicon Grains Fabricated by Excimer Laser Irradiation with Amorphous Silicon Spacers and Its Application to High-Performance Low Temperature Polycrystalline Silicon Thin Film Transistors

## 5.1 Introduction

Low-temperature polycrystalline silicon (LTPS) thin film transistors fabricated by excimer laser crystallization (ELC) have been extensively studied for active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting displays (AMOLEDs) owing to their high driving-current capability [5.1] - [5.2]. Although field-effect-mobility of 200 $cm^2$/Vs for TFTs has been attained by ELC, it is difficult to make the laser energy density hit the super lateral growth regime everywhere due to the fluctuation of pulse-to-pulse energy and amorphous silicon (a-Si) layer thickness [5.1] - [5.5]. Furthermore, in the applications of system-on-panel (SOP), high-performance LTPS TFTs are still needed to integrate memory and controller with driver circuits on a single substrate. Thus, there is a great interest in improving the performance of LTPS TFTs by laser crystallization approaches, including sequential lateral solidification by laser beam scanning within several micrometers step by step [5.6]-[5.9], phase-modulated ELC using an optical phase-shift mask [5.10]-[5.12], μ-Czochralski (grain filters) method [5.13]-[5.15], ELC of selectively floating a-Si layer [5.16]-[5.17], CLC method using the diode-pumped solid state continuous wave laser [5.18]-[5.19], and selectively enlarging laser crystallization (SELAX) [5.20]. However, most of them are complicated or not easy to be controlled from the viewpoints of LTPS TFTs fabrication.

In the previous works, the crystallinity of poly-Si thin film can be effectively enhanced via ELC with bottom-gate structure, however it is inevitable that there is a high angle grain boundary in the middle of channel region, which degrades the TFT performance and reliability. In this chapter, a novel and simple laser crystallization method which can remove the high angle grain boundary and produce the large and uniform grains in the desired local region is proposed to improve the field-effect mobility as well as the device uniformity. Consequently, high-mobility poly-Si TFTs has been demonstrated owing to the periodically lateral silicon grains with 2 μm in length artificially grown in the channel regions via the amorphous silicon spacer structure with excimer laser irradiation. The concept of controlled lateral grain growth is first discussed. Then, the experimental details are described in detail. Next, the microstructure of ELC poly-Si thin film with a-Si spacer structure is analyzed by SEM, Raman spectrum, and AFM. The electrical characteristics of the resulting ELC LTPS TFT performance are presented and analyzed. It leads to the enhancement of device performance and the improvement of device uniformity. The effect of the number of grain boundary on large dimension TFTs is also investigated.

## 5.2 The Basic Concept of Periodically Lateral Silicon Grains Employing Excimer Laser Crystallization with a-Si Spcaer Structures

It is well-known that the electrical characteristics of poly-Si TFTs are deeply influenced on the microstructure of poly-Si thin films, including grain crystallinity, grain size, grain structure, grain boundary, and grain orientation. Reducing the grain boundaries within the active channel region is an effective way to improving TFT performance and uniformity. As expected, the lateral large grains with excellent quality in the channel region are desirable for the device fabrication and circuit application. The TFTs without any grain boundary perpendicular to the current flow will exhibit superior performance, including large on current, high field-effect mobility, steeper subthreshold swing, and low leakage current. For the formation of large silicon grains at the desired position, controlling the Si nucleation site at the selected region are fabricated by a-Si spacer structure. The proposed process steps of excimer laser annealing on a-Si thin films with spacer structures is illustrated in Figure 5-1. A lateral temperature gradient in the melted silicon will induce the lateral grain growth. Besides, there must be un-melted solid silicon seeds to act as the nucleation sites for lateral grain growth between the adjacent areas. In our proposed ELA method employing a-Si spacer structure, one dimensional temperature gradient in induced. In this work, the a-Si thin film with two kinds of thicknesses in a local region was adopted to produce a local temperature gradient during the excimer laser irradiation. The a-Si thin films with spacer structure are fabricated by using the dry-etching of the a-Si/TEOS-$SiO_2$ step structure following the TEOS stripping-off before excimer laser irradiation. A schematic illustration of lateral grain growth in the channel region using spacer structure of a-Si thin film with ELA is displayed in Fig. 5-2. As the excimer laser irradiation is performed on the a-Si thin film, the applied laser energy density is controlled to completely melt the thin region of a-Si film but partially melt the thicker region of a-Si spacer-structured films. Therefore, un-melting solid seeds remain at the spacer position and a lateral temperature gradient can be produced between the complete melting liquid-phase regions and un-melting solid-phase silicon seeds. The lateral grain growth started from the partial-melted spacer silicon solid seeds and extended toward the completely melted region until the solid-melt interface from opposite direction impinges. Owing to the tiny width of the a-Si spacer (< 500Å), the a-Si spacers can be arranged periodically inside the channel region. Hencc, as the channel region and the location of a-Si spacers are properly designed, the lateral grain growth can be artificially controlled in the desired local region and the grain boundary perpendicular to the current flow in the channel region can be reduced. LTPS TFTs made by this new crystallization method will exhibit higher performance and better uniformity.

## 5.3 Experiments

The maximum process temperature of n-channel LTPS TFTs fabrication is 600°C for the dopant activation by thermal annealing in the $N_2$ ambient. Figure 5-3 illustrates the key processes for the fabrication of LTPS TFTs crystallized by ELC with a-Si spacer structure. At first, a 1000 Å-thick amorphous silicon (a-Si) layer was deposited by pyrolysis of pure silane ($SiH_4$) by low pressure chemical vapor deposition (LPCVD) at 550°C on oxidized silicon wafer with oxide thickness of 1μm. Then, a 500 Å-thick tetraethyl orthosilicate (TEOS) oxide layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 385°C. Next, the TEOS oxide layer in some regions was removed using reactive ion etching (RIE) to form individual islands following by another 1000 Å-thick a-Si layer deposition by LPCVD at 550°C. Subsequently, the upper a-Si layer was etched by transformer-coupled plasma reactive ion etching (TCP-RIE) to leave the a-Si spacer on the initial a-Si thin film. The a-Si spacers with 500 Å height were formed at the sidewalls of the TEOS islands. After stripping-off the remains of TEOS oxide by buffer oxide etchant (BOE) and standard RCA cleaning, excimer laser crystallization (ELC) was performed by KrF excimer laser ($\lambda$=248 nm). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to

$10^{-3}$ Torr and substrate was maintained at 400°C. The number of laser shots per area was 20 (i.e. 95% overlapping) and laser energy density was varied. A scanning electron microscopy (SEM) was used to get the surface micrograph and the microstructure of poly-Si thin films after Secco-etch. A Raman spectroscopy was employed to analyze the crystallinity of poly-Si film in the channel region. The surface morphology of laser-crystallized poly silicon thin film was investigated by atomic force microscopy (AFM) analysis. After defining the device active region, a 1000 Å-thick TEOS gate oxide was deposited by PECVD at 385°C. Then, a 2000 Å-thick a-Si thin film was then deposited by LPCVD at 550°C for gate electrode. The a-Si thin film and gate oxide were etched by TCP-RIE to form the gate electrode. A self-aligned phosphorous ion implantation with dose of $5\times10^{15}$cm$^{-2}$ was carried out to form source and drain regions. Next, a 3000 Å-thick TEOS passivation oxide was deposited by PECVD at 350°C and the implanted dopants were activated by thermal annealing at 600°C for 12 hours. Finally, after contact hole opening by reactive ion etching, aluminum thin film with a thickness of 5000 Å was deposited by sputtering and Al metal pads were patterned to complete the fabrication of TFTs with spacer structure. No hydrogenation plasma treatment was performed during the device fabrication process. For the sake of comparison, the conventional excimer-laser-crystallized LTPS TFTs with a channel thickness of 1000Å were also fabricated in the same run.

## 5.4 Results and Discussion

### 5.4.1 Material Characterization of ELC Poly-Si Thin Films with a-Si Spacer Structure

Figure 5-4 (a) and Figure 5-4 (b) display the SEM images of a-Si spacer structure formation. Two apparent silicon spacer lines with 1500 Å-thick are indicated by white dash lines fabricated by using the dry-etching of the a-Si/TEOS-$SiO_2$ step structure following the TEOS stripping-off in the Figure 5-4 (a). According to the magnified SEM image of Figure 5-4 (b), the 50 nm-wide a-Si spacer is successfully formed without using advanced photolithography process or expensive electron beam lithography equipment.

Atomic force microscopy analysis is used to investigate the surface morphology of silicon thin film before and after laser crystallization. Figure 5-5 (a) and Figure 5-5 (b) display the AFM images of silicon thin film with 1500 Å-thick spacer height before and after excimer laser irradiation, respectively. Three apparent silicon spacer lines are indicated by white dash lines formed using dry-etching of the a-Si/TEOS-$SiO_2$ step structure following the TEOS stripping-off before laser irradiation in the Figure 5-5 (a). After laser crystallization, the spacers disappear and the silicon thin film becomes smooth due to the effect of surface tension during excimer laser irradiation. The location of a-Si spacers has been verified by protecting some spacers from excimer laser crystallization. The ridge and hillock occur at the grain boundaries due to the freezing of capillary waves excited in the melting silicon during laser crystallization [5.21]. Figure 5-6 shows the Raman spectra from poly-Si film with periodic lateral grains, from the conventional excimer-laser-crystallized poly-Si film, and from a silicon wafer for reference. The insets describe that full width at half maximum (FWHM) and normalized peak intensity of the poly-Si film with periodic lateral silicon grains (PLSG) are close to those of silicon wafer, reflecting that the crystallinity of PLSG poly-Si film is better than that of conventional ELC poly-Si film.

Figure 5-7 (a) and 5-7(b) exhibit the SEM photographs of excimer laser crystallized poly-Si with a-Si spacer structure after Secco etching and the distances between adjacent a-Si spacers are 2 μm and 3 μm, respectively. The inset of Figure 5-7(a) shows the microstructure of conventional ELC poly-Si with the same scale. The location of a-Si spacer is indicated by white dash lines. It can be observed that Figure 5-7 (a) shows the transverse grains with 2 μm in length formed periodically in the laser crystallized poly-Si thin film, while small and fine grains which are formed in the middle region of the channel caused by spontaneous homogeneous nucleation, presented in Figure 5-7 (b). It has been reported that lateral thermal gradient could arise as a result of the heat generated at moving solid-melting interfaces [5.5]-[5.22]. As a proper laser energy density is performed on the amorphous silicon thin film containing different thickness, the thin silicon region is completely melted while the thick region is partially melted, and the lateral grain growth starts from the un-melted solid Si toward the completely melted thin region. In this experiment, as excimer laser irradiation is performed on the amorphous silicon thin film with a-Si spacers, the laser energy densities can cause complete melting 1000 Å-thick silicon thin film but partial melting 1500 Å-thick a-Si film. Therefore, the 1000 Å-thick poly-Si film with the 500 Å-thick spacer will proceed the lateral grain growth starting from the un-melted silicon solid seed under the spacer, and extend toward the completely melted region until the solid-melt interface from opposite direction impinges. If the a-Si seeds were arranged in a proper distance, periodic grain growth will be manufactured without any spontaneous nucleation. Thus, the grain boundaries in the channel region can be controlled and reduced. From the SEM analyses, the maximum achievable length of lateral grain growth in this crystallization method is about 2.5 μm. Since the number of spontaneous small grain and grain boundary is reduced, the uniformity of TFTs performance can be improved with artificially periodic lateral grains.

### 5.4.2 Electrical Characteristics of LTPS TFTs Fabricated Using Excimer Laser Irradiation with a-Si Spacer Structure

Typical transfer characteristics and output characteristics of LTPS TFTs with periodic lateral silicon grains and conventional ones for W = L = 2 μm are shown in Figure 5-8(a) and Figure 5-8(b), respectively. Several important electrical characteristics of the TFTs are listed in Table 5-1. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of $I_{ds} = (W/L) \times 10^{-8}$ A at $V_{ds} = 0.1$ V. The field-effect mobility and subthreshold swing were extracted at $V_{ds} = 0.1$ V, and the $I_{on}/I_{off}$ current ratio was defined at $V_{ds} = 5$ V. Because of the uniformly large transverse grains grown in the device channel region, TFTs with periodic lateral grains exhibit better electrical characteristics than the conventional ones. Poly-Si TFT with field effect mobility of 298 $cm^2$/Vs can be achieved using this a-Si spacer crystallization method while the mobility of the conventional counterpart is about 128 $cm^2$/Vs. It is generally believed that the grain boundary acts as a strong trapping center which degrades the performance of TFTs resulting from grain boundary potential barrier height. The high field effect mobility is attributed to that the carrier transport is not interrupted by the grain boundary parallel to the channel direction for the periodic lateral grain silicon structure. Although small and fine grains are located in the channel region as the distance between neighboring a-Si spacers exceeds 2.5 μm, the characteristics of TFTs crystallized with a-Si spacer structure are still better than those of conventional TFTs.

In addition to the improvement of LTPS TFTs performance, TFTs with periodic lateral grains demonstrate better uniformity due to the wide laser process window. Figure 5-9(a) and 5-9(b) show the dependences of field effect mobility and threshold voltage on laser energy densities for LTPS TFTs crystallized with two different structures whose channel length is 2 μm. In the Figure 5-9(a) and 5-9(b), twenty TFTs for each laser irradiation condition are measured to study the device-to-device variation. The vertical bars in the figures indicate the maximum and minimum characteristic values and the solid symbols are the average calculated characteristic values at the specific laser energy density. Unlike the conventional devices, it is found that the threshold voltage and field effect mobility of LTPS TFTs with periodic lateral grains are much less sensitive for different laser energy densities.

Since periodic lateral silicon grains can be arranged periodically inside the channel region (Figure 5-7(a)), this proposed crystallization method is also suitable for large-dimension TFTs. Figure 5-10isplays the schematic illustration of the positions of a-Si spacer in the channel region for large-sized device. Periodic lateral grains are constructed inside the channel and the number of longitudinal grain boundary can be varied by adjusting the distance of adjacent a-Si spacers. Figure 5-11a) and Figure 5-11b) show the typical transfer characteristics and output characteristics of LTPS TFT crystallized with periodic lateral silicon grains, in which the distance between neighboring a-Si spacers is 2.5 μm, and conventional one for W = L = 10 μm, respectively. Table 5-2 summarizes several important electrical characteristics of the TFTs crystallized with conventional and a-Si spacer structures, in which the distances between adjacent spacers are 1 μm, 2 μm, 2.5 μm, 3 μm, and 4 μm, respectively. The device channel width and length are equal 10 μm. Periodic lateral grains in the channel region make the performance of poly-Si TFTs better than that of conventional TFTs. Besides the enhancement of field effect mobility, high on/off current ratio and low threshold voltage are also demonstrated in these devices. These electrical characteristics are gradually improved due to the decrease of the number of longitudinal grain boundary in the channel region as the distance between adjacent a-Si spacer increases. The optimal electrical characteristics are obtained when the distance between neighboring a-Si spacers is 2.5 μm. This result consists with the SEM analyses, which reveal the largest lateral grain crystallized made by this technique is about 2.5 μm.

## 5.5 Summary

A new crystallization technology for producing periodic lateral silicon gains has been developed by excimer laser irradiation with a-Si spacers. The 50 nm-wide a-Si spacers are successfully formed without using advanced photolithography process or expensive electron beam lithography equipment. The transverse grains with 2 μm in length formed periodically in the excimer laser crystallized poly-Si thin film with better crystallinity as compared with the conventional ELC poly-Si films. Consequently, in addition to the high-performance n-channel LTPS TFTs with field-effect-mobility reaching 298 cm$^2$/Vs in 2 μm design rule, excellent uniformity of device performance is also demonstrated owing to the artificially-controlled periodic lateral grain growth. Large-dimension TFTs crystallized with the distance between adjacent a-Si spacers of 2.5 μm also exhibit the better characteristics resulting from the minimum number of longitudinal grain boundary in the channel region. LTPS TFTs with periodic lateral silicon grains are therefore promising for future system-on-panel applications.

**Table 5-1**

Measured electrical characteristics of LTPS TFTs crystallized with a-Si spacer and conventional structures.

| **Structure** | **Threshold Voltage (V)** | **Field-effect Mobility ($cm^2$/Vs)** | **Subthreshold Swing (mV/dec)** | **On/off Current Ratio ($10^7$)** |
|---|---|---|---|---|
| **Conventional (W = L = 1.5 μm)** | -0.652 | 155 | 1072 | 0.17 |
| **A-Si spacer (W = L = 1.5 μm)** | 0.46 | 312 | 310 | 8.2 |
| **Conventional (W = L = 2 μm)** | 1.94 | 128 | 738 | 3.3 |
| **A-Si spacer (W = L = 2 μm)** | 0.86 | 298 | 477 | 6.3 |

## Table 5-2

Measured optimal electrical characteristics of LTPS TFTs crystallized with conventional and a-Si spacer structures, respectively.

| **Structure (W/L = 10/10 μm)** | **Threshold Voltage (V)** | **Field-effect-Mobility ($cm^2$/Vs)** | **Subthreshold Swing (V/dec)** | **On/off current ratio ($10^7$)** |
|---|---|---|---|---|
| **Conventional** | 6.16 | 114 | 1.61 | 0.93 |
| **Spacer distance = 1 μm** | 5.88 | 141 | 1.68 | 2.5 |
| **Spacer distance = 2 μm** | 4.88 | 170 | 1.27 | 7.7 |
| **Spacer distance = 2.5 μm** | 5.35 | 176 | 1.13 | 8.9 |
| **Spacer distance = 3 μm** | 6.40 | 176 | 1.81 | 6.8 |
| **Spacer distance = 4 μm** | 5.99 | 168 | 1.73 | 14 |

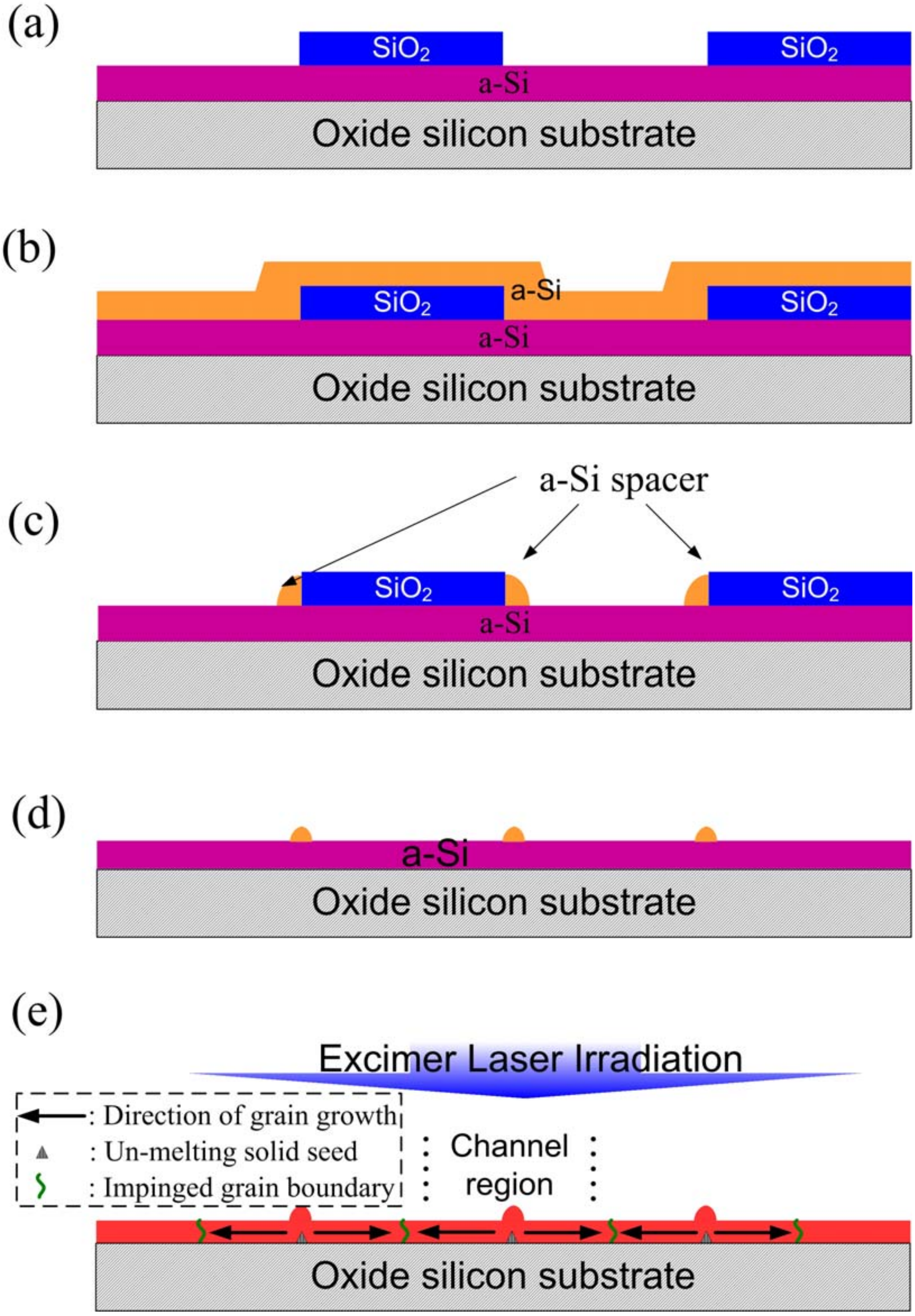


Figure 5-1. The proposed processes of excimer laser annealing on a-Si thin films with a-Si spacer structures.

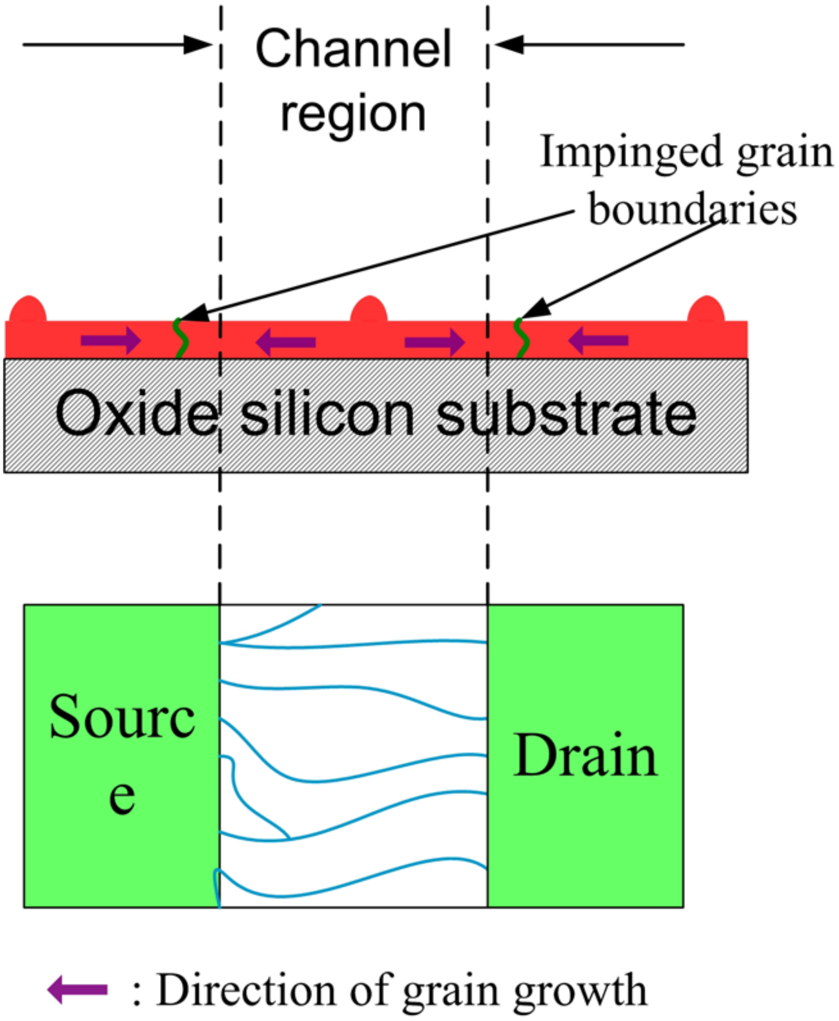


Figure 5-2. The schematic illustration of lateral grain growth in the channel region using spacer structure of a-Si thin film with ELA.

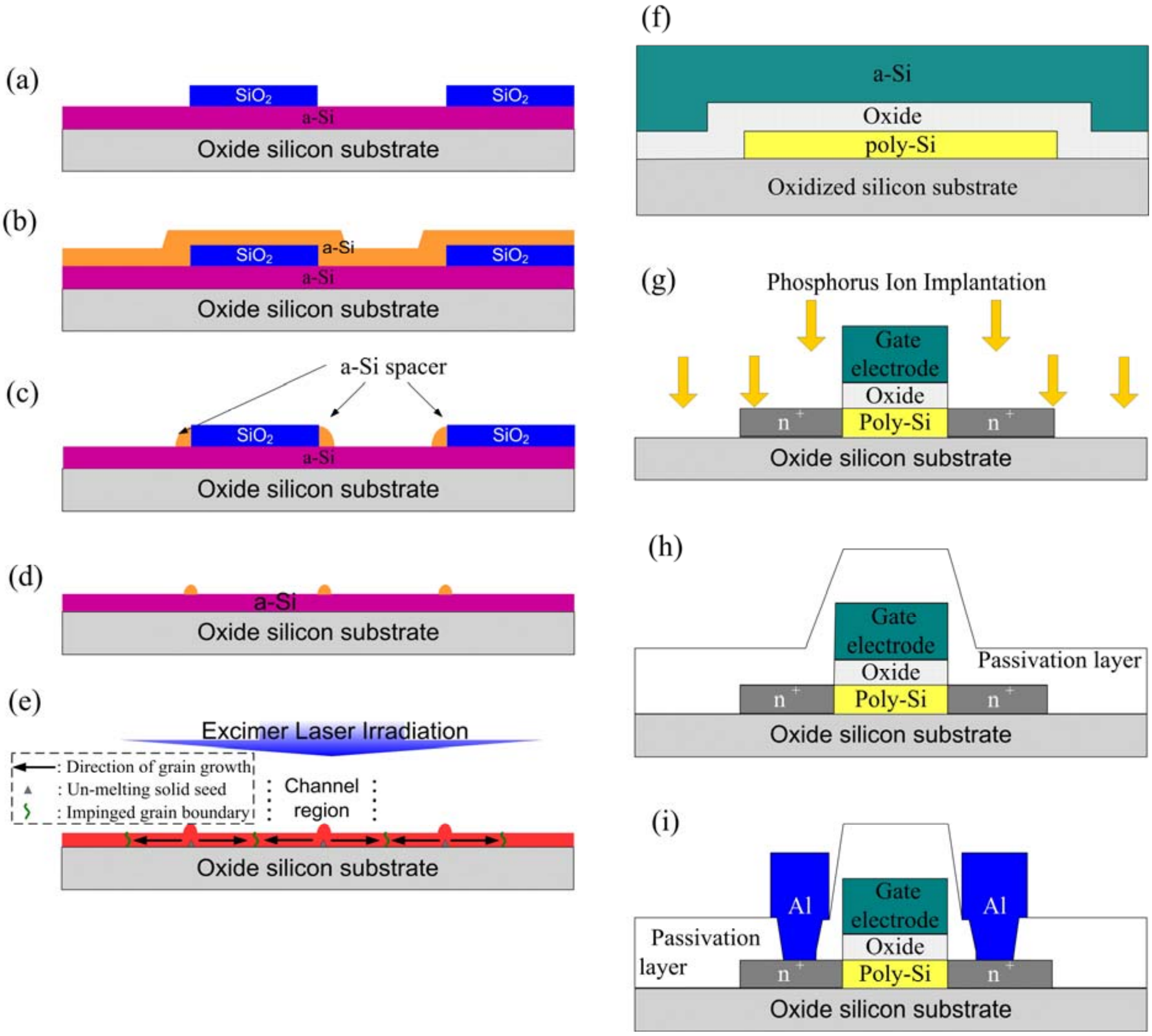


Figure 5-3. The key processes for fabricating small-dimension LTPS TFTs with a-Si spacer structure.

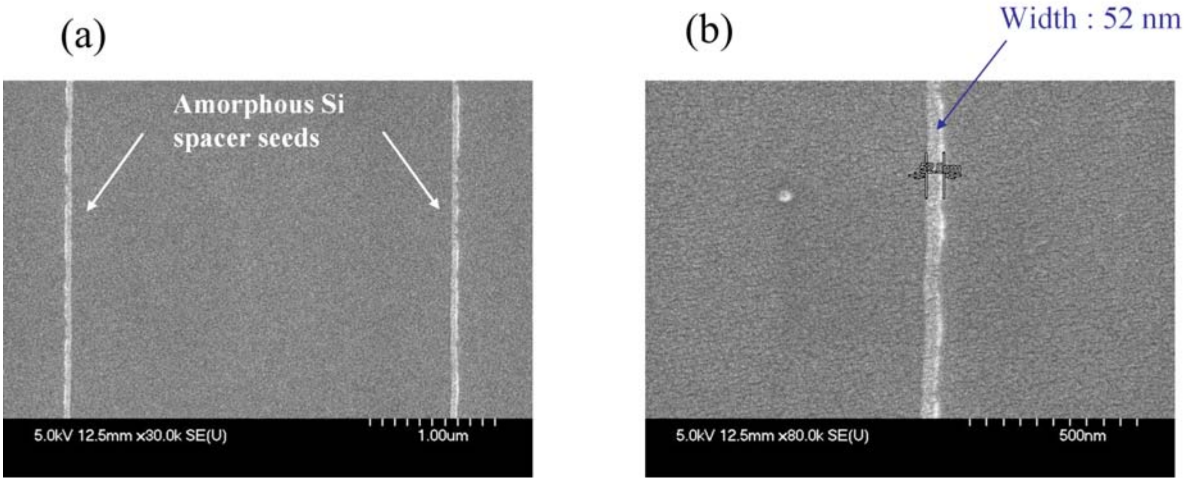


Figure 5-4. (a) The SEM images of a-Si spacer structure formation. (b) The enlarged SEM image.

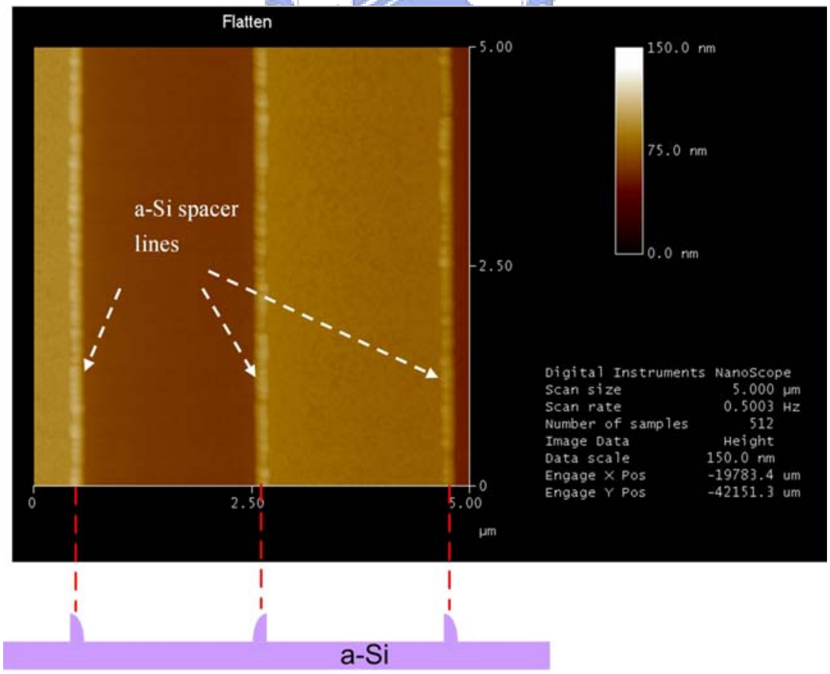


Figure 5-5(a). AFM images of poly-Si thin film with spacers of 1500 Å-height before excimer laser irradiation.

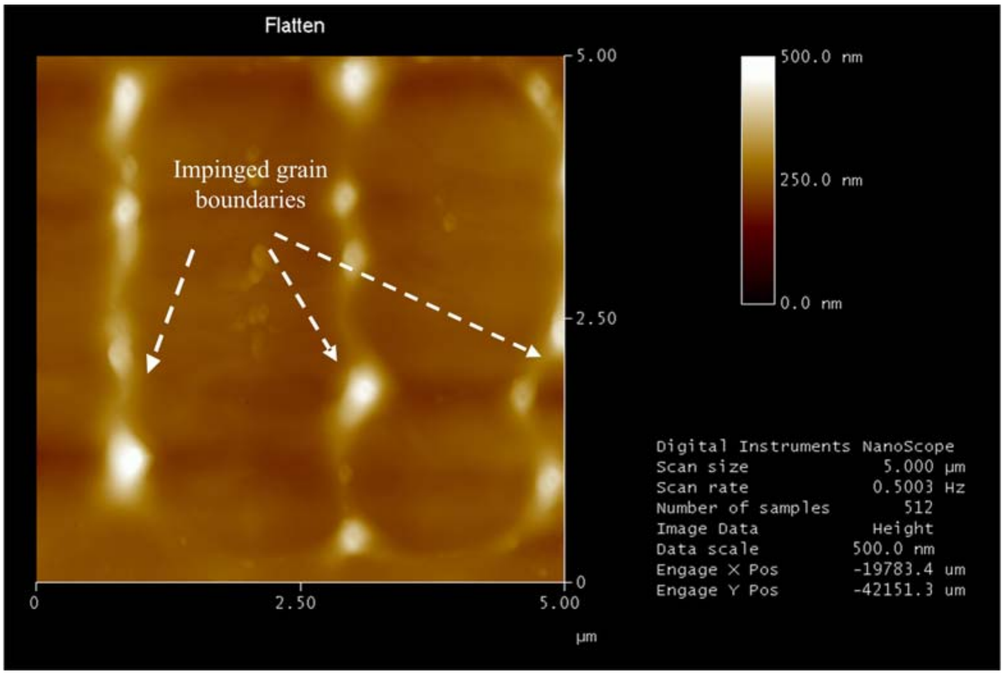


Figure 5-5(b). AFM images of poly-Si thin film with spacers of 1500 Å-height after excimer laser irradiation.

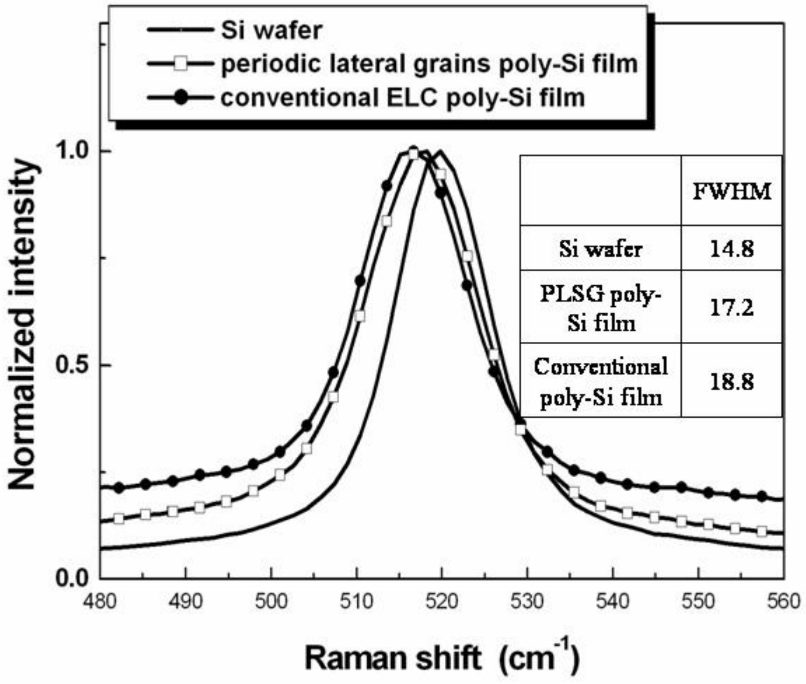


Figure 5-6. Raman spectra for poly-Si film with periodic lateral grains and those for conventional ELC poly-Si film.

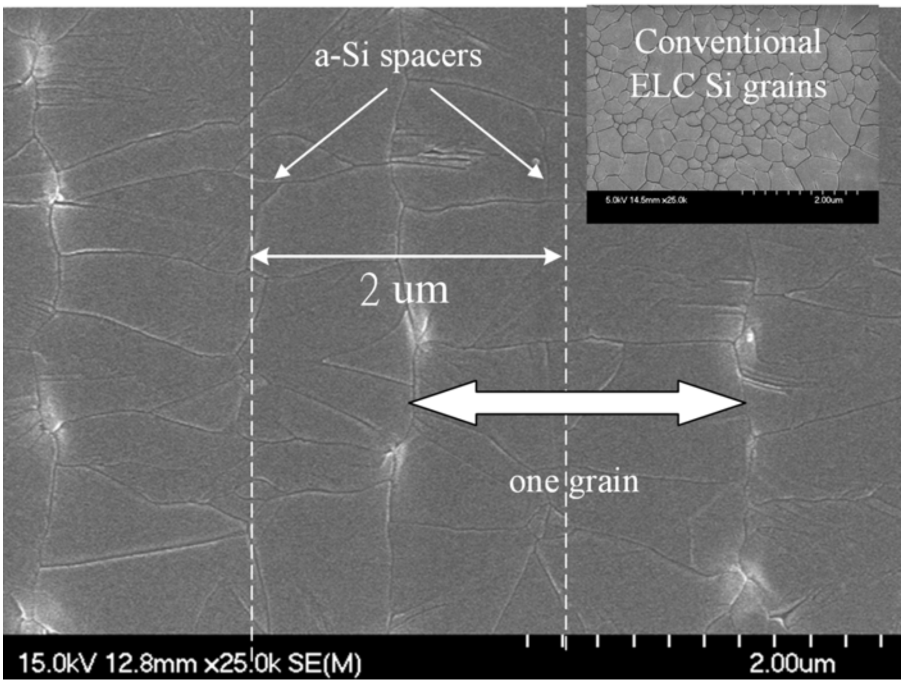


Figure 5-7(a). SEM micrographs of excimer laser crystallized poly-Si film with amorphous Si spacer structure after Secco etching and the distances between adjacent a-Si spacers are 2 μm. Inset of Figure 5-7 (a) is the conventional ELC poly-Si film.

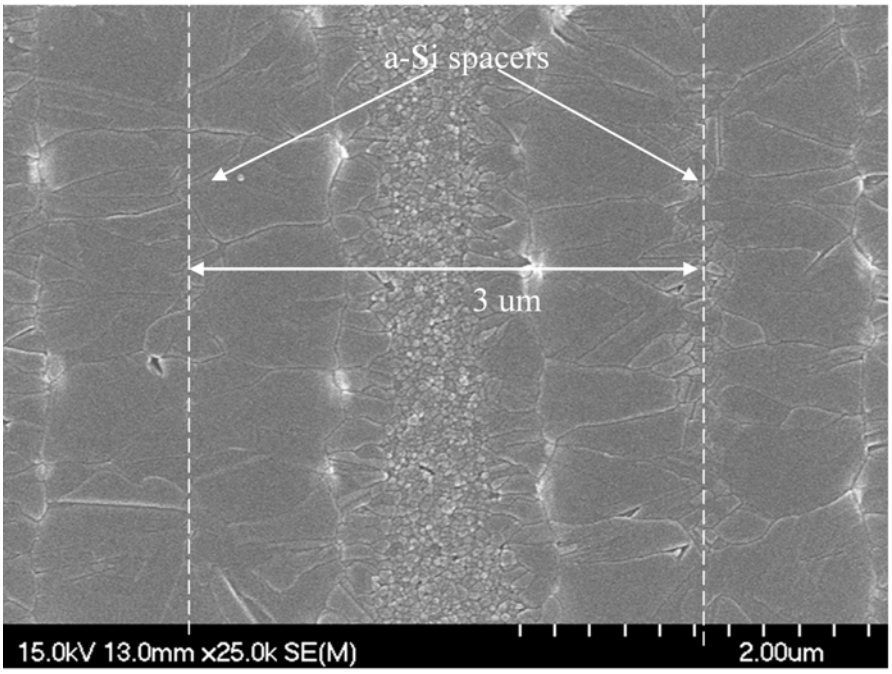


Figure 5-7(b). SEM image of excimer laser crystallized poly-Si film with a-i spacer structure after Secco etching and the distances between adjacent a-Si spacers are 3 μm.

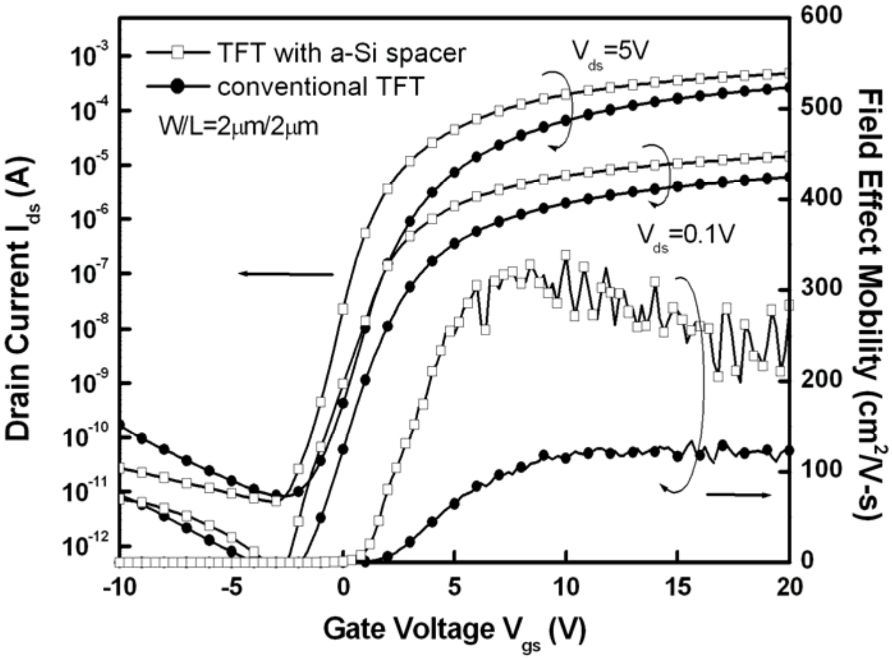


Figure 5-8(a). Transfer characteristics of LTPS TFT with a-Si spacer structure and conventional TFT.

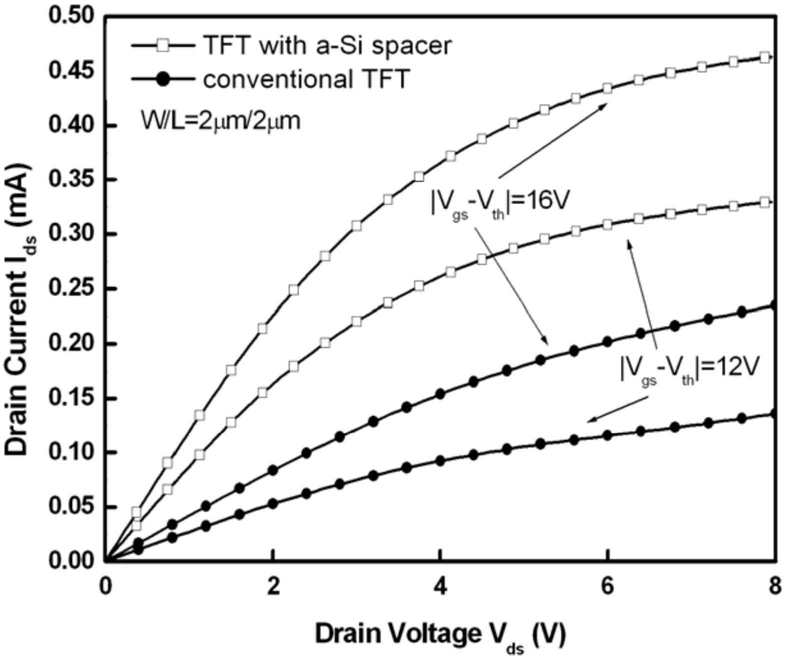


Figure 5-8(b). Output characteristics of LTPS TFT with a-Si spacer structure and conventional TFT.

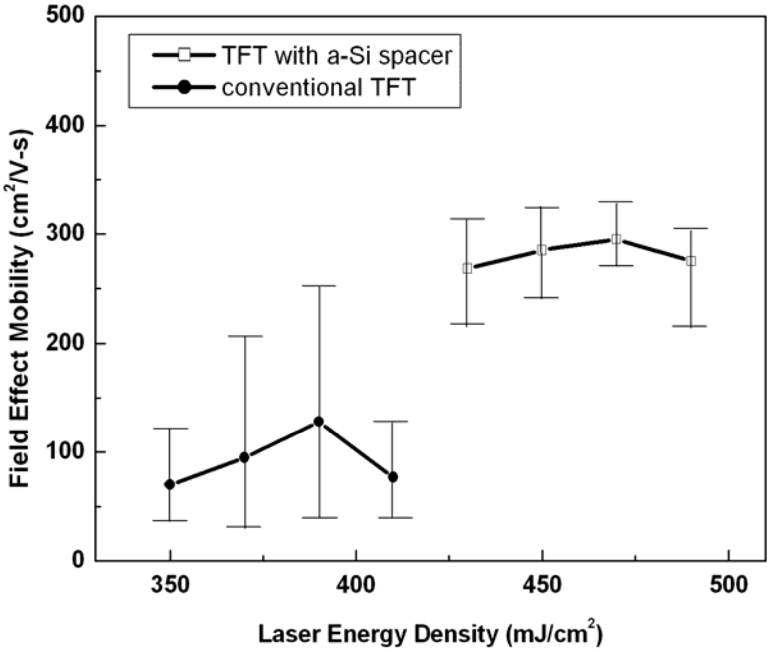


Figure 5-9(a). Dependences of field-effect mobility on applied excimer laser energy density for TFTs with a-Si spacer and conventional TFTs.

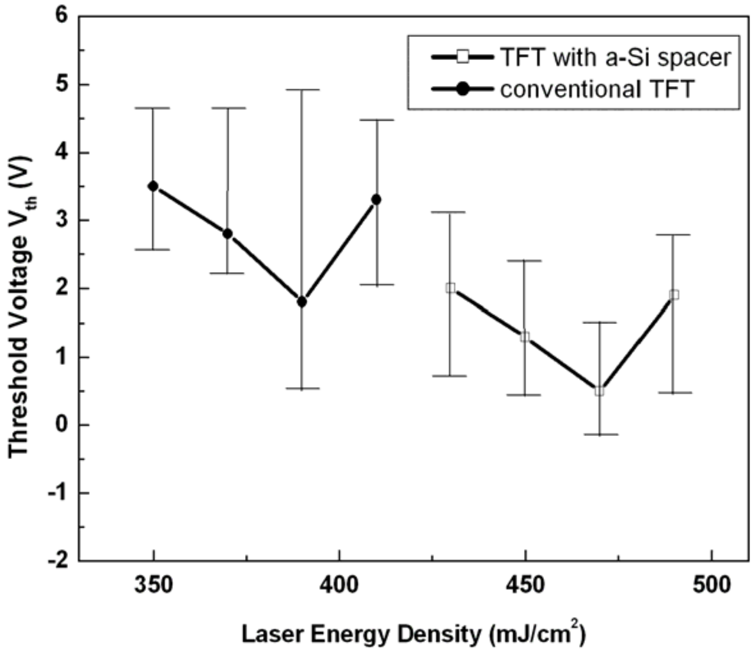


Figure 5-9(b). Dependences of threshold voltage on applied excimer laser energy density for TFTs with a-Si spacer and conventional TFTs.

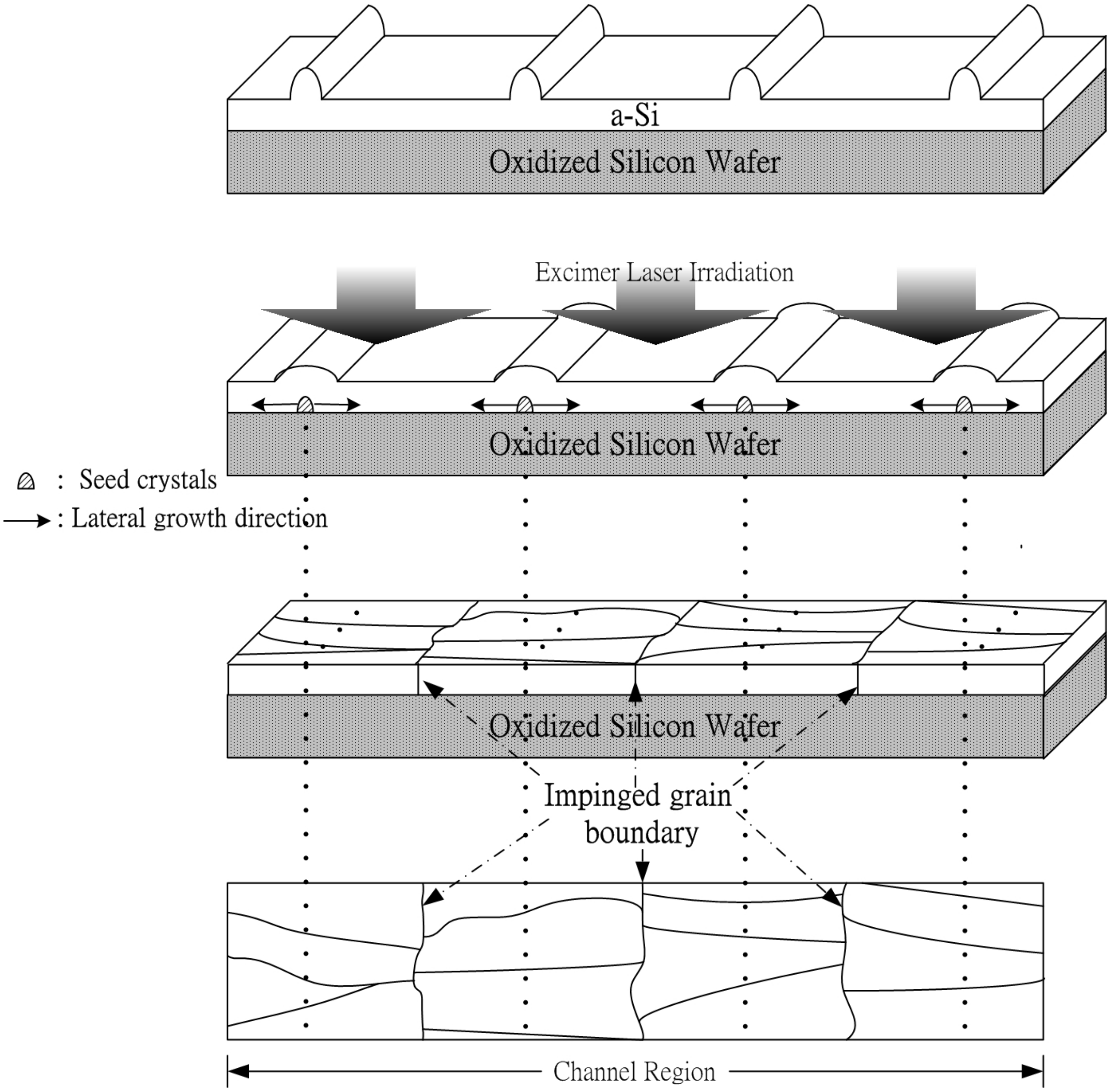


Figure 5-10. The schematic illustration of poly-Si film with periodic lateral grains applied to large-dimension TFTs.

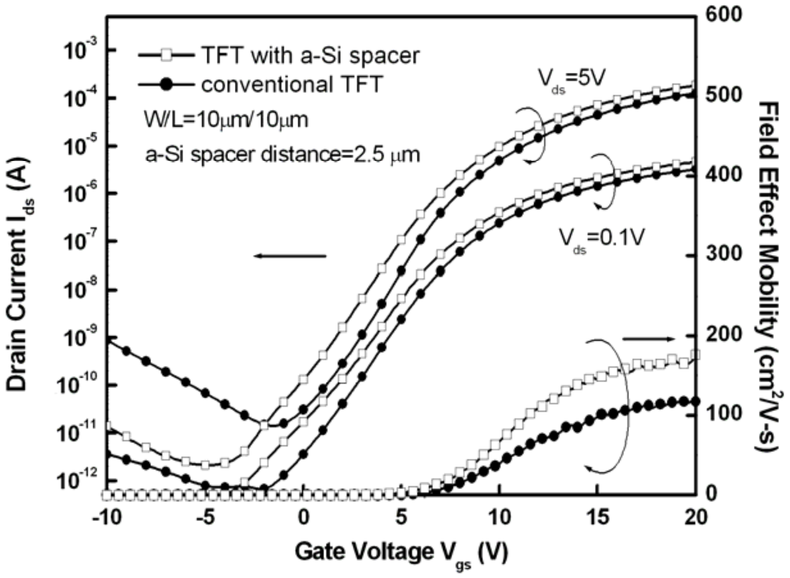


Figure 5-11(a). Typical transfer characteristics of LTPS TFT crystallized with periodic lateral silicon grains, in which the distance between neighboring a-Si spacers is 2.5 μm, and conventional TFT for W = L = 10 μm.

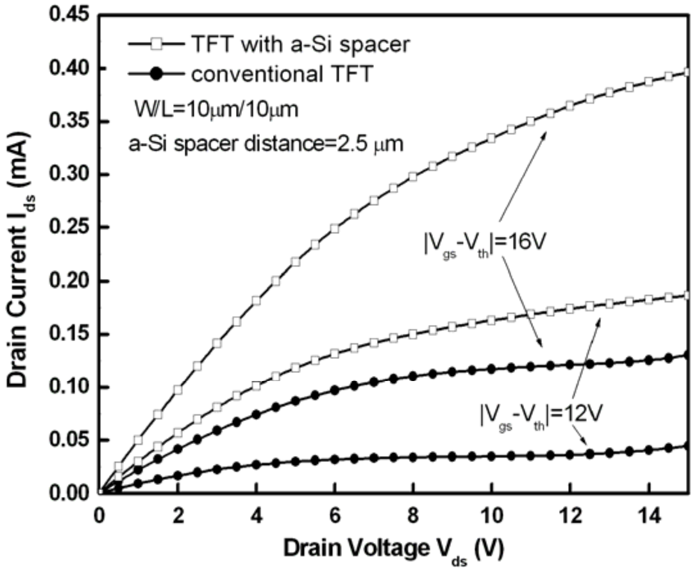


Figure 5-11(b). Typical output characteristics of LTPS TFT crystallized with periodic lateral silicon grains, in which the distance between neighboring a-Si spacers is 2.5 μm, and conventional TFT for W = L = 10 μm.

# Chapter 6

# Low Temperature Polycrystalline Silicon Thin-Film Transistors on Location-Controlled Silicon Crystal Grains Fabricated by Pre-Patterned Silicon Films with A-Si Spacers using Excimer Laser Irradiation

## 6.1 Introduction

Low-temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have been extensively studied for active matrix liquid crystal displays (AMLCDs), active matrix organic light emitting displays (AMOLEDs), and great potential for flexible electronics and 3-dimensional integrated circuits (3D-ICs) applications owing to their high driving-current capability and better thermal reliability [6.1] - [6.4]. Metal-induced lateral crystallization (MILC) of amorphous silicon (a-Si) thin film has been proved to produce good-performance LTPS TFTs [6.5]. However, metal contamination and high intra-grain defect densities in MILC poly-Si thin films degrade TFT performance, such as large leakage current, high subthreshold swing, and so on [6.6]. At this moment, excimer laser crystallization (ELC) seems to be the most promising method for its great potential in mass production and high quality silicon grains without damage to glass/plastic substrates. However, the average grain size of poly-Si thin films recrystallized by conventional ELC is less than 0.8 μm, which results in inferior TFTs performance as compared with silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect-transistor (MOSFET) [6.7]. Since the randomness of grain-boundary location and the electrical potential barrier localized at the grain boundaries are the major factors in causing the device non-uniformity and degrading the TFT performance by hindering the carrier transport [6.8] - [6.9], enlarging silicon grain size and controlling the grain boundary location are effective approaches to high-performance TFT and good device uniformity [6.10] - [6.19]. For realizing system-on-panel (SOP) technology, integrating memory, micro-processor-unit, driver circuits, sensors, etc. on a single substrate, both of the device performance and the device-to-device uniformity need further enhancement [6.20] - [6.28]. Single-grain TFT in which the channel is grain-boundary-free will exhibit silicon-on-insulator-like (SOI-like) performance to satisfy the requirements of SOP. More researches, therefore, have been devoted to the two-dimensional (2D) grain control, aiming at single-grain TFT [6.11], [6.13], [6.14], [6.28]-[6.38].

In our previous work, the laser crystallization method with a-Si spacer structure has been proposed and demonstrated to produce one-dimensional periodically lateral silicon grains. The purpose of this work is to present a new crystallization process for producing high quality two-dimensional lateral grains based on spatial temperature distribution and artificial sites. 1.8-μm-sized disk-like grains can be artificially grown in the channel regions via the amorphous silicon spacer structure and pre-patterned silicon thin film with excimer laser irradiation. The detailed fabrication processes and characteristics of TFTs on location-controlled silicon crystal grains are presented and discussed using the conventional ELC TFTs as a comparison. Excimer laser crystallization mechanism of pre-patterned silicon film with a-Si spacer structures are presented and analyzed. The experimental results exhibit that both the device performance and the device-to-device uniformity are improved in proposed TFTs.

## 6.2 Experiments

Figure 6-1 illustrates the key processes for the fabrication of excimer-laser-crystallized poly-Si TFTs with a-Si spacer structure and pre-patterned silicon thin films. At first, $Si_3N_4$ thin film with a 500Å thickness was deposited on an oxidized silicon wafer with oxide thickness of 1μm and was defined to form individual islands (Figure 6-1 (a)). Then, a 1000Å a-Si layer was deposited by pyrolysis of pure silane ($SiH_4$) gas source with low pressure chemical vapor deposition (LPCVD) at 550°C (Figure 6-1 (b)). The a-Si layer was subjected to reactive ion etching (RIE), so that the a-Si spacer with a 500 Å height was formed at the sidewall of the $Si_3N_4$ islands, as shown in Fig.6-1 (c). After removing the $Si_3N_4$ layer by phosphoric acid at 175°C, another 1000 Å-thick a-Si layer was deposited by LPCVD at 550°C with $SiH_4$ as gas source. Therefore, a-Si thin film with two kinds of thicknesses (1000 and 1500 Å) in a local region was formed by this spacer technique (Figure 6-1 (d)). A-Si layer was subjected to another reactive ion etching (RIE) to define silicon stripes which were perpendicular to the previous $Si_3N_4$ islands, as shown in Fig. 6-1 (e). After standard RCA cleaning process, the samples were then subjected to 248 nm KrF excimer laser crystallization (ELC). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to $10^{-3}$ Torr and the substrate was maintained at 400°C (Figure 6-1 (f)). The laser beam was homogenized into a semi-gaussian shape in the short axis and a flat-top shape in the long axis. The excimer laser annealing was performed in the scanning mode. The number of laser shots per area was single pulse and laser energy density was controlled in the near-complete-melting regime for 1500-Å-thick a-Si spacers and completely-melting condition for 1000-Å-thick a-Si thin films [6.9]. The surface morphology and microstructure of excimer-laser-crystallized poly-Si thin films were analyzed by transmission electron microscopy (TEM) and scanning electron microscopy (SEM), respectively. The TEM samples were prepared via the focused-ion-beam (FIB) technique and the SEM samples were prepared using the Secco-etch process. After excimer laser crystallization, poly-Si thin films were etched by drying etching to define the device active region. Then, a 1000-Å-thick tetraethyl orthosilicate (TEOS) gate oxide was deposited by LPCVD. A 2000-Å-thick a-Si thin film was deposited by LPCVD for formation of the gate electrode at 550°C. Then, a-Si thin film and gate oxide were etched by TCP-RIE to form the gate electrode. A self-aligned phosphorous ion implantation with dose of $5\times10^{15}cm^{-2}$ was carried out to form source and drain regions (Figure 6-1 (g)). Next, a 3000 Å-thick TEOS passivation layer was deposited by LPCVD and the implanted dopants were activated by thermal annealing at 600°C for 12 hours in the $N_2$ ambient. Contact hole opening and metallization were carried out to complete the fabrication of TFTs with pre-patterned spacer structure (Figure 6-1 (h)). Finally, a 30-min sintering process was performed in $N_2$ ambient at 400°C to reduce the contact series resistance of the source and drain electrodes. No hydrogenation plasma treatment was performed during the device fabrication process. For the sake of comparison, the conventional excimer-laser-crystallized poly-Si TFTs with an average grain size of about 5000 Å and a channel thickness of 1000 Å were also fabricated in the same run.

Current-voltage characteristics of the fabricated devices were measured using a semiconductor parameter analyzer of Agilent technologies 4156C. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of $I_{ds} = (W/L) \times 10^{-8}$ A at $V_{ds} = 0.1$ V. The field effect mobility and subthreshold swing were extracted at $V_{ds} = 0.1$ V, and the $I_{on}/I_{off}$ current ratio was defined at $V_{ds} = 5$ V. A scanning electron microscopy (SEM) (S4700, Hitachi) was used to get the surface micrograph of poly-Si thin films after Secco-etch. An analytical field-emission transmission electron microscopy (TEM) (JEM-2100FX, JEOL Ltd.) was employed to analyze the microstructure and crystallinity of the disklike poly-Si grains.

## 6.3 Results and Discussion

Figure 6-2 (a) displays the SEM photograph of excimer-laser-crystallized poly-Si thin films with pre-patterned a-Si spacer structure after Secco etching. In this case, the thick region of a-Si spacer is 1500 Å and a-Si in the other thin region is 1000 Å. The distance between adjacent a-Si spacers is 2 μm and the width of the pre-pattern silicon stripes is 5 μm. The locations of a-Si spacer seeds and the pre-pattern silicon stripes are indicated by the white dash lines and the solid black arrowhead lines, respectively. The laser energy fluence is controlled at 475 mJ/cm$^2$ and the substrate temperature is isothermally heated at 400°C during laser irradiation in order to reduce the cooling rate of the complete melting Si for the purpose of enlarging silicon grain size [6.39]. It can be observed that transverse grains with 2 μm in length formed periodically in the laser crystallized poly-Si thin film which is consistent with the result of one dimensional lateral grain growth owing to the large width of striped silicon films. Figure 6-2 (b) displays the SEM photograph of excimer-laser-crystallized poly-Si thin films with pre-patterned a-Si spacer structure after Secco etching. In this case, the thick region of a-Si spacer is 1500 Å and a-Si in the other thin region is 1000 Å. The distance between adjacent a-Si spacers is 2 μm and the width of the pre-pattern silicon stripes is 4 μm. The laser energy fluence is controlled at 475 mJ/cm$^2$ and the substrate temperature is isothermally heated at 400°C. Similar one dimensional lateral grain growth is also observed. Figure 6-2 (c) displays the SEM photograph of excimer-laser-crystallized poly-Si thin films with pre-patterned a-Si spacer structure after Secco etching. In this case, the distance between adjacent a-Si spacers is 2 μm and the width of the pre-pattern silicon stripes is 3 μm. Periodical disklike grain growth is formed in the laser-crystallized poly-Si films owing to the temperature gradient in two directions. Figure 6-2 (d) displays the SEM photograph of excimer-laser-crystallized poly-Si thin films with pre-patterned a-Si spacer structure after

Secco etching. In this case, the distance between adjacent a-Si spacers is 2 μm and the width of the pre-pattern silicon stripes is 2 μm. Periodical lateral grain growth is formed in the laser-crystallized poly-Si films. The deformation of the striped silicon films after excimer laser irradiation occurs due to the surface tension effect. As the width of the pre-pattern silicon stripes is 1 μm, the striped silicon films are damaged and discrete islands are formed due to the serious surface tension effect as shown in the Figure 6-2 (e) and 6-2 (f), respectively. Figure 6-3 displays the plane-view TEM images of location-controlled poly-Silicon thin films and the width of the pre-pattern silicon stripes is 1 μm. According to the high-magnification bright-field and dark-field TEM images and the selected-area electron diffraction pattern, it can be found that the periodical silicon grains are formed due to the shrinkage of the silicon films during laser irradiation and the poly-Si grain is composed of many small grains. As a result, the width of the pre-pattern silicon stripes must be optimized in order to induce temperature gradient without serious deformation of silicon films.

Figure 6-4 (a) displays the SEM photograph of excimer-laser-crystallized poly-Si thin films with pre-patterned a-Si spacer structure after Secco etching. In this case, the thick region of a-Si spacer is 1500 Å and a-Si in the other thin region is 1000 Å. The distance between adjacent a-Si spacers is 7 μm and the width of the pre-pattern silicon stripes is 3 μm. The locations of a-Si spacer seeds and the pre-pattern silicon stripes are indicated by the white dash lines and the solid black arrowhead lines, respectively. The laser energy fluence is controlled at 475 mJ/cm$^2$ (near-complete-melting condition for 1500 Å-thick a-Si spacers) and the substrate temperature is isothermally heated at 400°C during laser irradiation in order to reduce the cooling rate of the complete melting Si for the purpose of enlarging silicon grain size. It can be observed that disk-like grains are formed periodically in the laser crystallized poly-Si thin film as shown in Figure 6-4 (a). Figure 6-4 (b) shows the enlarged SEM graph to focus on a single grain with grain size of 1.8 μm in diameter and there are three different kinds of poly-Si regions, which are the large disked-liked grain formed in the center of the striped poly-Si film (region I), the radial grains (~ 150-nm-sized) surrounded the large disked-liked grain in the form of thin ring (region II), and the small and fine grains (~ 40-nm-sized) in the outer zone (region III). The scenario for this new crystallization mechanism of a-Si thin films is described as follows. It has been reported that lateral thermal gradient could arise as a result of the heat generated at moving solid-melting interfaces [6.9], [6.40]. In our proposed ELC method employing a-Si spacer structure and pre-patterned silicon thin film, as excimer laser irradiation is performed on the striped amorphous silicon thin film with a-Si spacers, the laser energy densities can cause the complete melting of 1000-Å-thick silicon thin film but near-complete-melting of 1500-Å-thick a-Si spacer. In addition, along the y axis, since the edges of the striped silicon films adjacent to the air during laser irradiation and the surface regions of the bulk silicon wafer outside the pre-patterned stripes can absorb intense KrF excimer laser UV light, they are melted to the high temperature. Therefore, for the striped silicon films, the cooling rate of the edges is slower than that of the center, because of the poor thermal conductivity of air and the heated surface regions of the bulk silicon wafer by laser irradiation. Figure 6-5 shows the simulated temperature distribution during excimer laser annealing on the pre-patterned silicon films. Therefore, the temperature near the edges of the striped Si films is higher than that in the center of the striped films. As a result, the temperature gradient also occurs along the y axis due to surface tension effect and additional heat reservation at the edges of striped films so that the numbers of silicon solid seeds are gradually reduced resulting from pre-patterned effect [6.41]-[6.42]. As a result, only a part of the spacers survive to serve as the seeds and a large lateral thermal gradient will exist between the un-melting solid silicon seeds and the complete-melting liquid silicon regions. Therefore, the un-melted silicon solid seed will proceed to start the lateral grain growth in the silicon films and extend toward the completely melted region until the solid-melting interface from opposite direction impinges after excimer laser irradiation, forming region I with the disked-liked grain of 1.8 μm in diameter. For the complete-melting outer zone, fine-grained poly-Si form region III due to the random spontaneous nucleation in the severely deep supercooling of melting liquid silicon films. Finally the spontaneously nucleated grains grow inward and then impinge on the oncoming lateral disk-like grain, therefore, radial grains form region II. It is also found that the locations of the grain boundaries where grains collide with each other shows brightly shining parts indicated by an arrow in Figure 6-4 (b), implying that the ridge and hillock are formed at the grain boundaries due to the mass transport of the molten Si at the liquid/solid interface [6.43]. Figure 6-6 shows the plane-view TEM image of the silicon film after ELC, which exhibits a 1.8 μm-sized silicon grain formed at the artificially site. This disk-like silicon grain is analyzed by its electron diffraction pattern and it reveals that the silicon grain has an excellent crystallinity due to the clear dot pattern. The crystallization mechanism we proposed is further verified by the cross-sectional TEM micrograph of excimer laser crystallized poly-Si thin films with pre-pattern a-Si spacer structure, as shown in the Figure 6-7. The blue dash line indicates the cutting direction of FIB-prepared sample shown in the inset optical micrograph of Figure 6-7. The bright-field TEM image and the selected-area electron diffraction pattern show that the edges of the stripe silicon films become thinner attributed to the surface tension effect after laser irradiation and the lateral silicon grain possess a good crystallinity, respectively. Moreover, the inset high-magnification cross-sectional TEM image of Figure 6-7 displays that these three different kinds of poly-Si regions and the impinged grain boundary are apparently recognized, which are consistent with our proposed mechanism. Since the number of spontaneous small grain and grain boundary is reduced by using this new crystallization technique, the uniformity of TFT performance can be improved with homogeneous silicon grains.

Typical transfer characteristics and output characteristics of poly-Si TFTs on location-controlled silicon grains and conventional TFTs with random grain structure for W = L= 1.5 μm are shown in Figures 6-8 (a) and 6-8 (b), respectively. In order to avoid the threshold voltage difference, the applied gate driving voltages in Fig. 6-8 (b) are kept at constant values of |Vg-Vth| = 12 V, and 16 V, respectively. Owing to the uniformly disk-like silicon grains grown in the device channel region, TFTs with location-controlled silicon grains exhibit superior electrical characteristics to the conventional ones. Poly-Si TFT with field effect mobility of 308 $cm^2/Vs$ can be achieved using this new crystallization method while the mobility of the conventional counterpart is about 150 $cm^2/Vs$. It is also demonstrated that poly-Si TFTs with location-controlled silicon grains structure provide higher driving current than conventional ELC poly-Si TFTs under the same bias condition. The improved driving current can be attributed to the high field effect mobility implying that location-controlled TFTs have the lower density of defect states, which are regards as localized states mainly at the grain boundaries of the poly-Si films. Table 6-1 lists the average values of several important electrical characteristics of the two different TFT structures with the standard deviations in parentheses. Ten TFTs were measured in each case to investigate the device-to-device variation, and the laser energy density was controlled at nearly optimal value for these two different TFT structures. As compared with the conventional TFTs, the small standard deviations of proposed TFTs indicate improved uniformity attributed to the location-controlled lateral silicon grains.

The grain boundary trap state densities (Nt) of the proposed LC poly-Si TFTs and conventional ones were estimated according to the modified Levinsons analysis. The Nt was extracted from the slopes of $\ln(I_D/V_{GS})$ versus $1/(V_{GS})$ at $V_{DS}$=0.1 V and high $V_{GS}$. Figure 6-9 displays that LC poly-Si TFT exhibits the Nt of $2.35\times 10^{11}$ $cm^{-2}$ two times smaller that of conventional ones. This result implies that proposed poly-Si TFTs with lateral silicon grains in the channel regions possess better crystallinity and fewer microstructure defects which are also confirmed by plane-view and cross-sectional TEM image of excimer laser crystallized poly-Si thin films with pre-patterned a-Si spacer structures shown in the Figure 6-7.

## 6.4 Summary

A new crystallization technology for producing location-controlled silicon gains has been developed by excimer laser irradiation relying on spatially temperature distribution at artificially sites. The high quality lateral silicon grains are controlled via manipulating super lateral growth phenomenon by spatially two kinds of silicon films and pre-patterned structure. The tiny amorphous-silicon spacers (< 50 nm) formed served as seed crystals and formed spatially different silicon thicknesses. An array of 1.8-μm-sized disk-like silicon grains are formed periodically in the silicon film by isothermal substrate heating at 400 °C during laser irradiation. Not only high-performance n-channel poly-Si TFTs with field-effect mobility reaching 308 $cm^2/Vs$ in 1.5 μm design rule but also excellent uniformity of device performance are also demonstrated owing to the artificially controlled lateral grain growth. Poly-Si TFTs with position-manipulated silicon grains, therefore, have great potential for the future system-on-panel and 3D-ICs applications.

**Table 6-1**

Measured electrical characteristics of poly-Si TFTs with location-controlled (LC) silicon grains and conventional TFTs with random grain structure.

| TFT Structure (W = L = 1.5 μm) | Threshold Voltage (V) | Field-effect-Mobility ($cm^2/Vs$) | Subthreshold Swing (mV/dec) | On/Off Current Ratio |
|---|---|---|---|---|
| Conventional TFT | 2.4 (0.85) | 150 (41) | 875 (80) | $3.3 \times 10^6$ |
| LC grains TFT | -0.8 (0.18) | 308 (18) | 390 (42) | $9.7 \times 10^7$ |

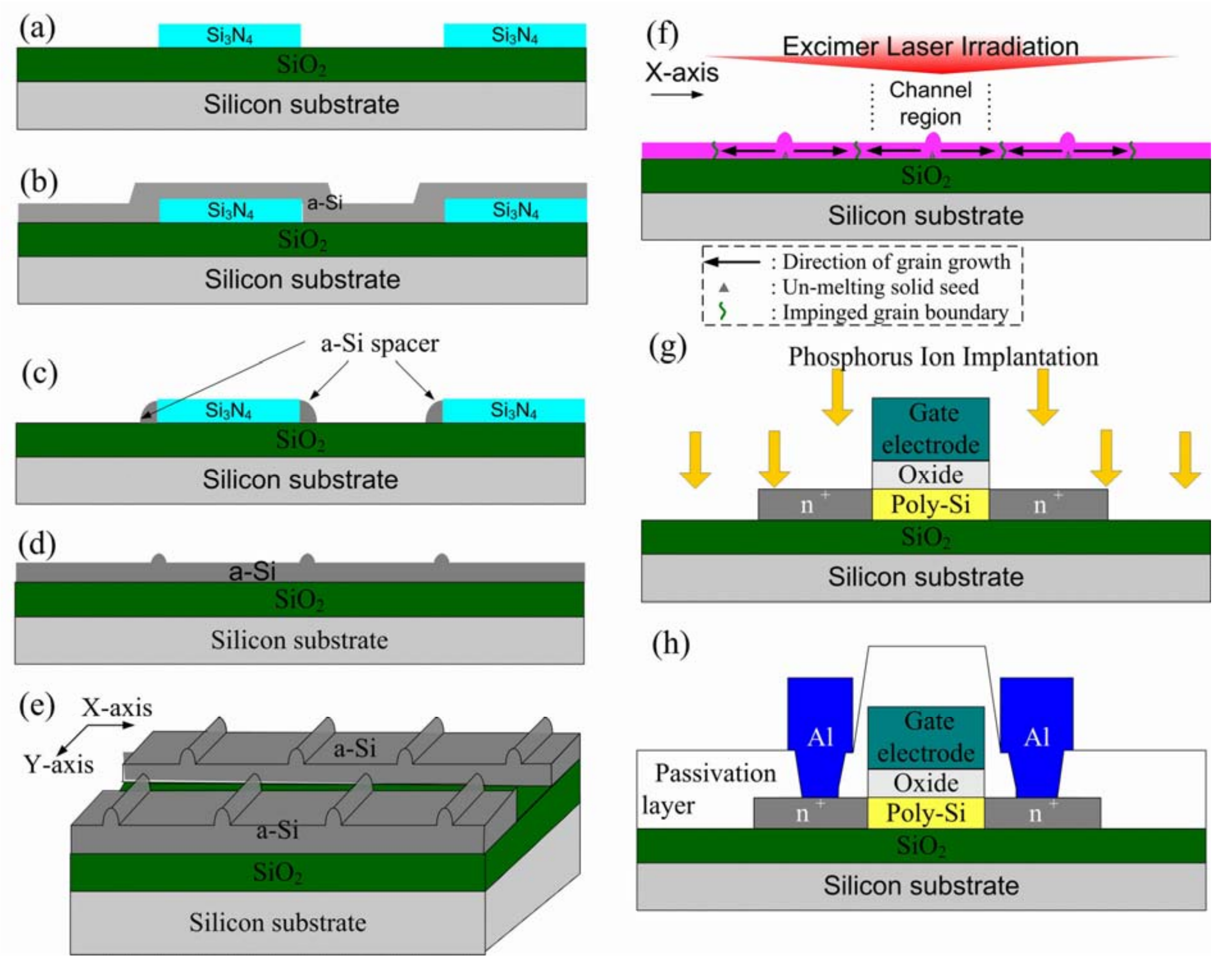


Figure 6-1. The key processes for the fabrication of poly-Si TFTs with a-Si spacer structure and pre-patterned silicon thin films.

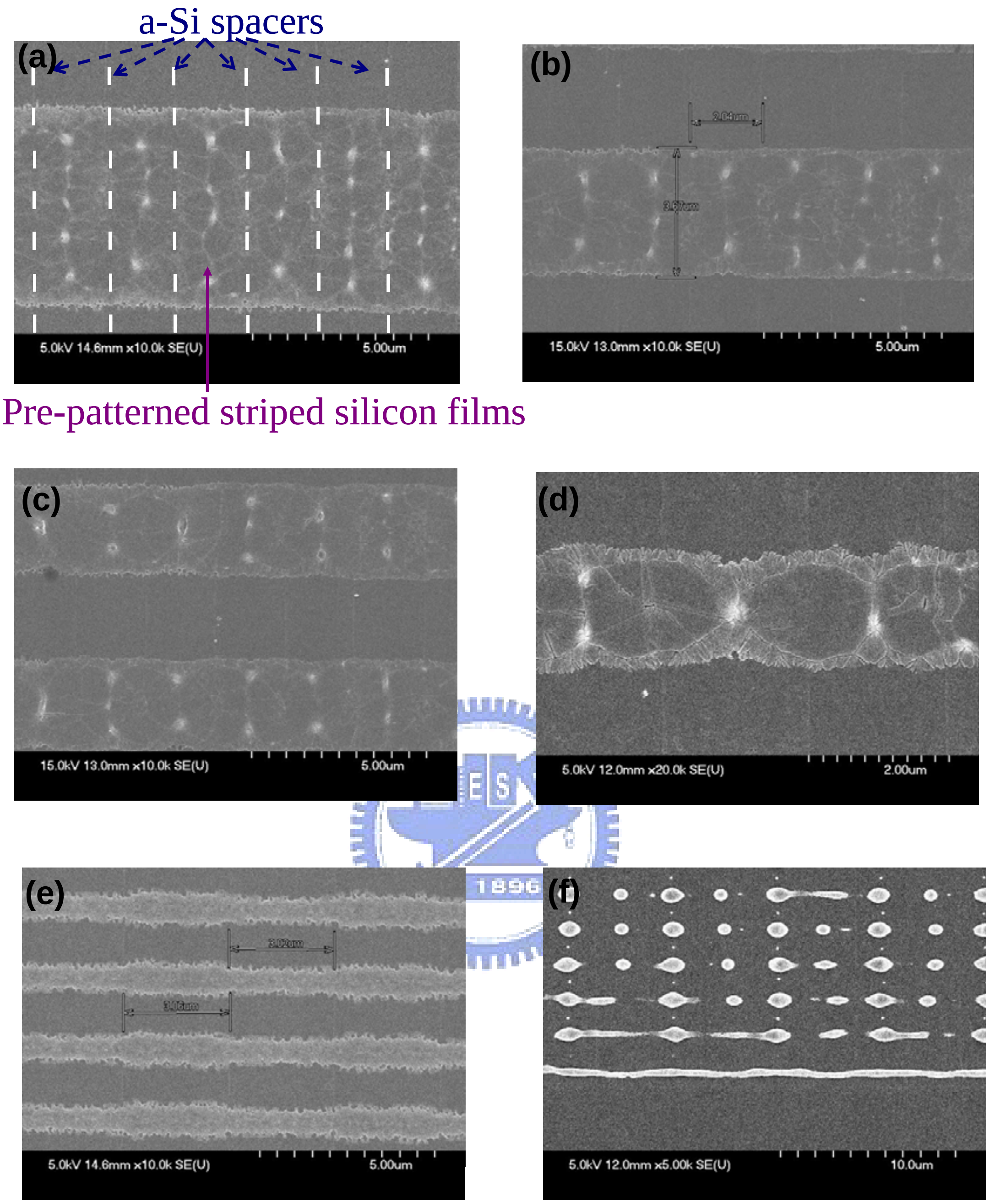


Figure 6-2. Scanning electron microscope photograph of excimer laser crystallized striped poly-Si films with amorphous Si spacer structure after Secco etching. (a) The distance between adjacent a-Si spacers is 2 μm and the width of the pre-pattern silicon stripes is 5 μm. (b) The width of the pre-pattern silicon stripes is 4 μm. (c) the width of the pre-pattern silicon stripes is 3 μm. (d) The width of the pre-pattern silicon stripes is 2 μm. (e) and (f) The width of the pre-pattern silicon stripes is 1 μm.

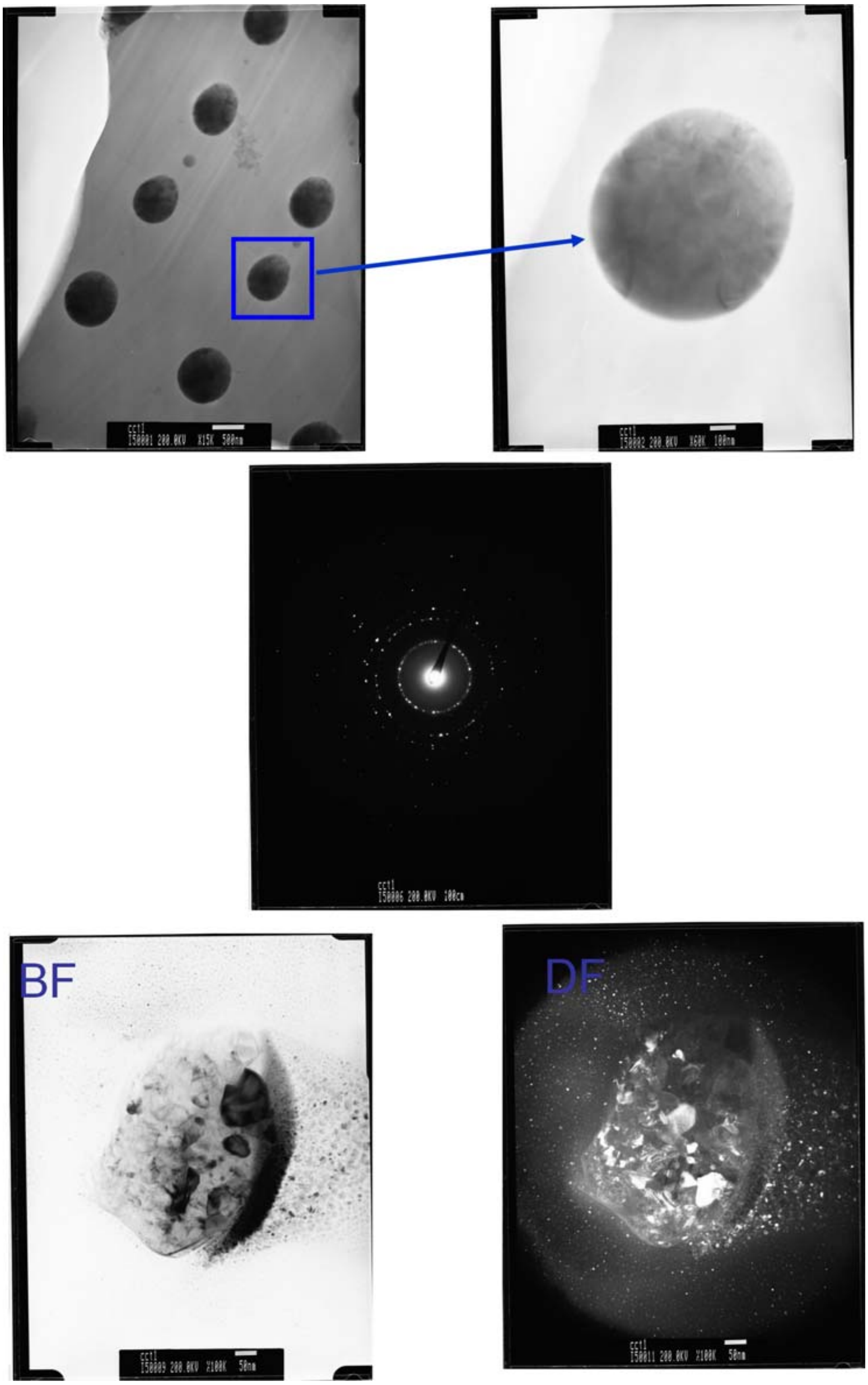


Figure 6-3. The plane-view TEM images of location-controlled poly-Silicon thin films and the width of the pre-pattern silicon stripes is 1 μm. The high-magnification bright-field and dark-field TEM images and the selected-area electron diffraction pattern of the poly-Si grains.

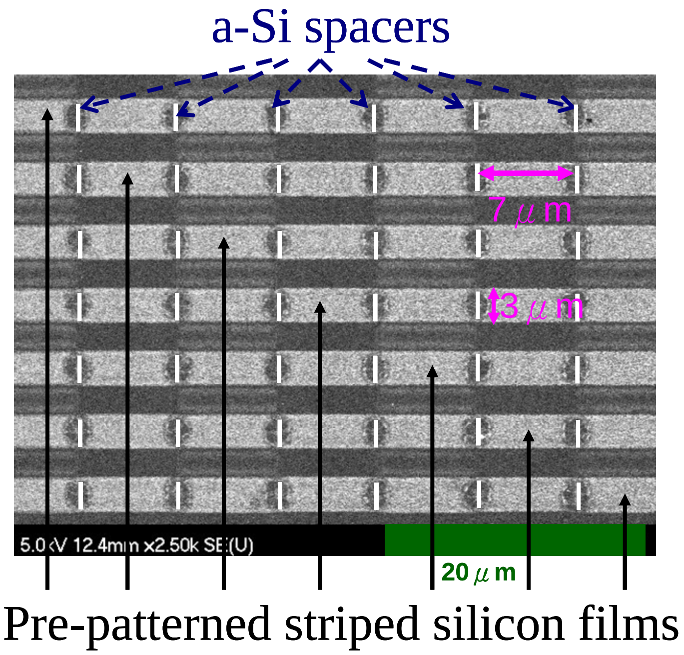


Figure 6-4 (a). Scanning electron microscope photograph of excimer laser crystallized striped poly-Si films with amorphous Si spacer structure after Secco etch and the disk-like grains with 1.8 μm in length formed periodically in the laser crystallized poly-Si thin film.

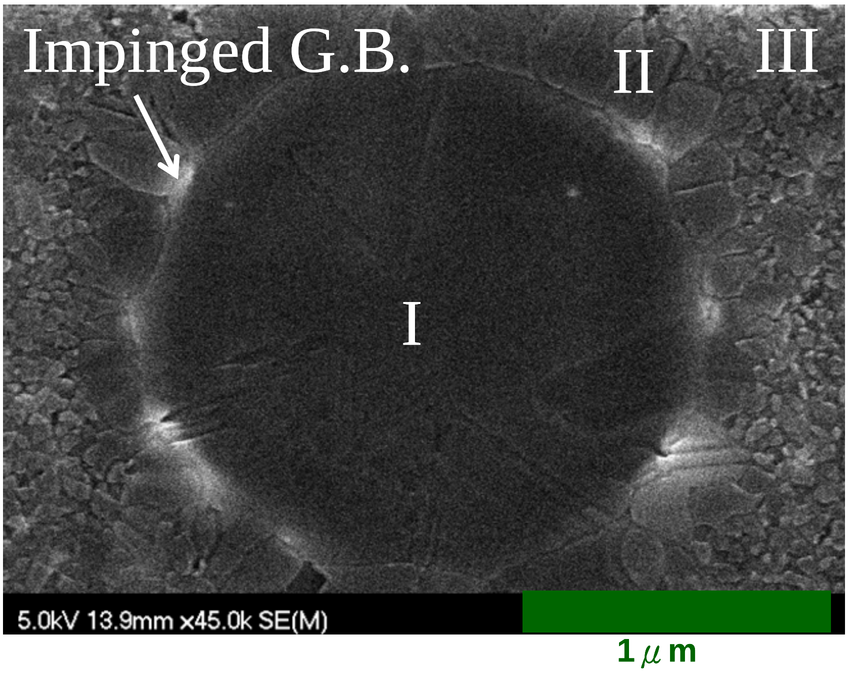


Figure 6-4 (b). The enlarged SEM photograph focuses on single silicon grain.

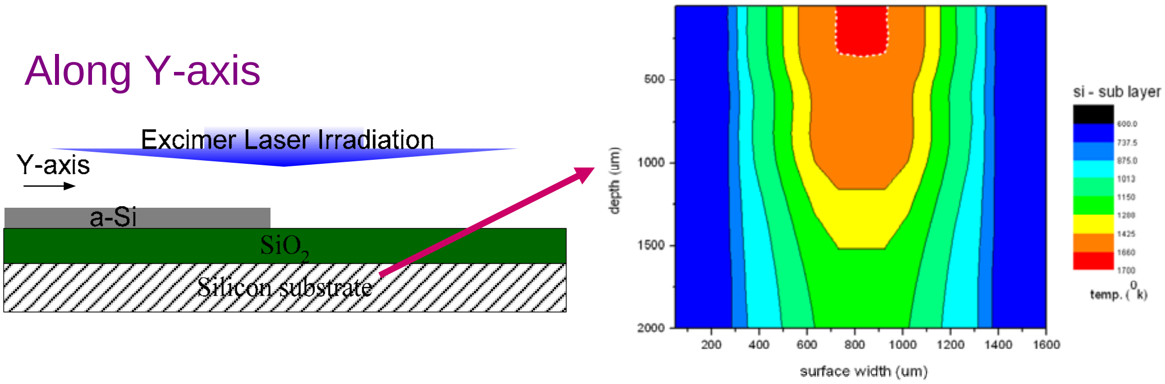


Figure 6-5. Schematic of simulation for excimer laser annealing on the pre-patterned silicon films and the simulated temperature distribution

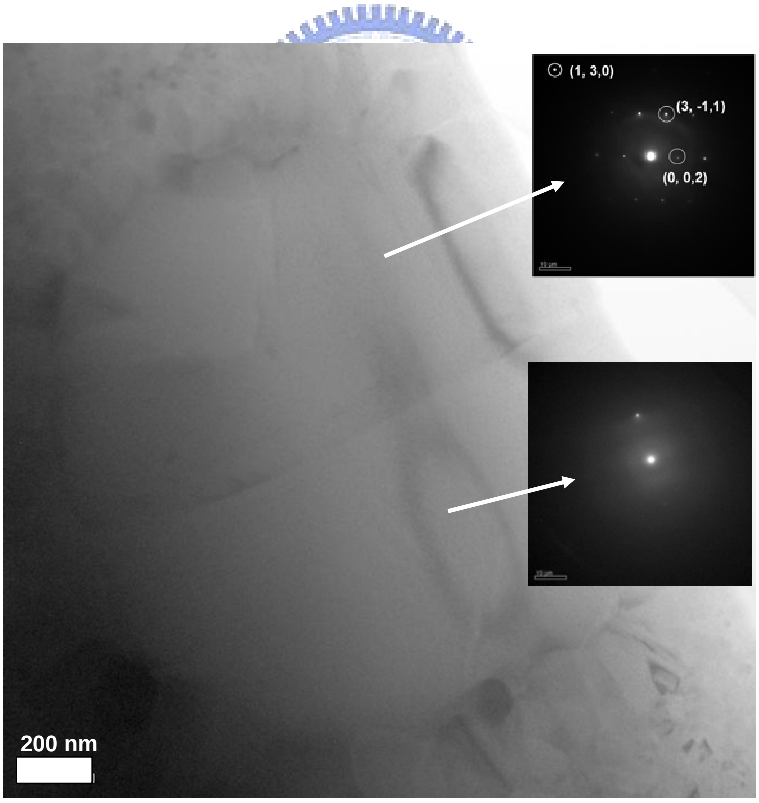


Figure 6-6. High-magnification bright-field plane-view TEM image and the selected-area electron diffraction pattern of the disk-like silicon grain. The width of the pre-pattern silicon stripes is 3 μm.

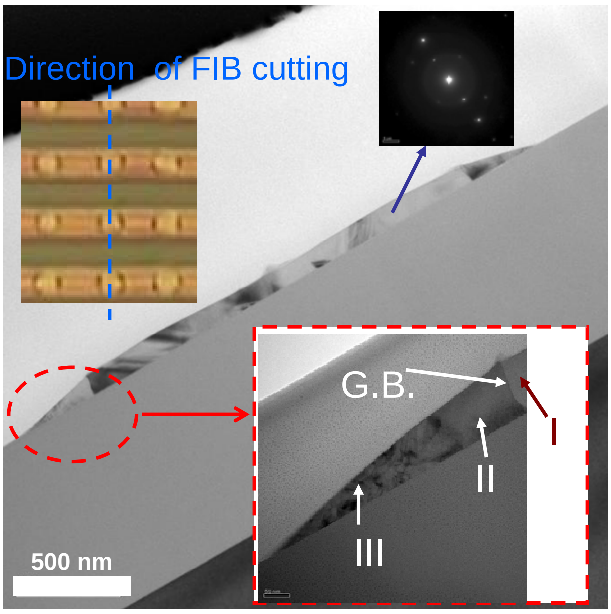


Figure 6-7. Cross-sectional TEM image of striped silicon film display the disk-like grain. The insets of Figure 6-7 are optical micrograph, selected-area electron diffraction pattern, and the enlarged cross-sectional TEM image to display the direction of FIB cutting, crystallinity of the disk-like grain, and the three different kinds of poly-Si grains near the edges of the striped films, respectively.

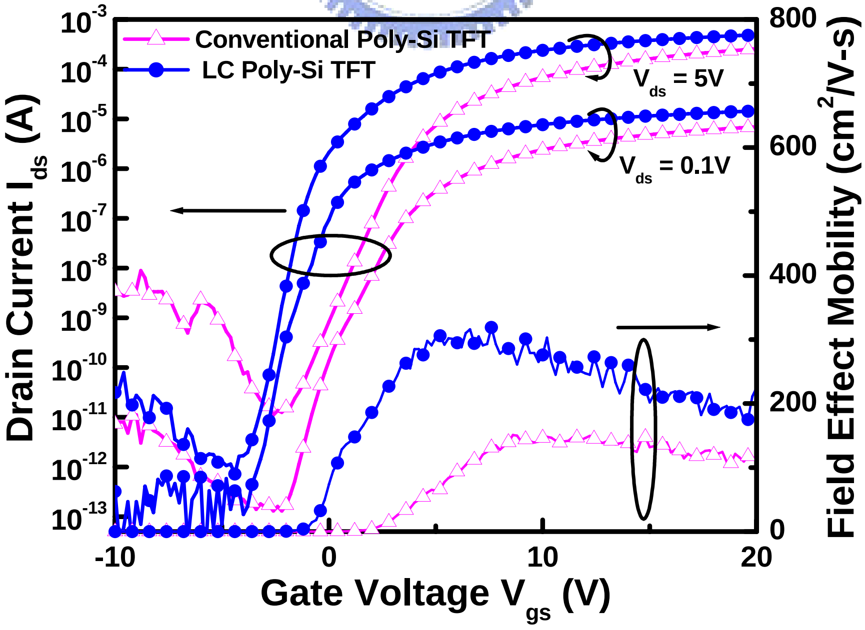


Figure 6-8 (a). Transfer characteristics of poly-Si TFT with location-controlled grains and conventional TFT with random grain structure.

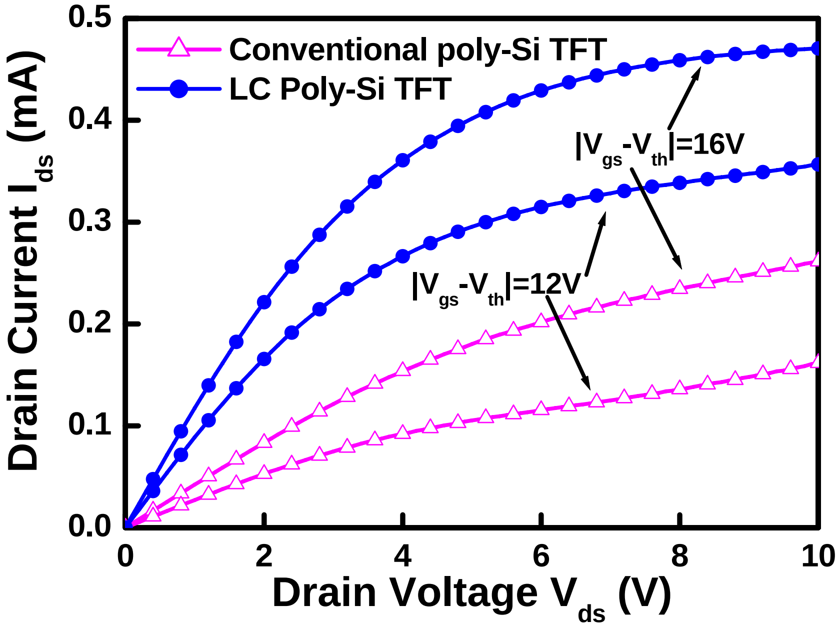


Figure 6-8 (b). Output characteristics of poly-Si TFT with location-controlled grains and conventional TFT with random grain structure.

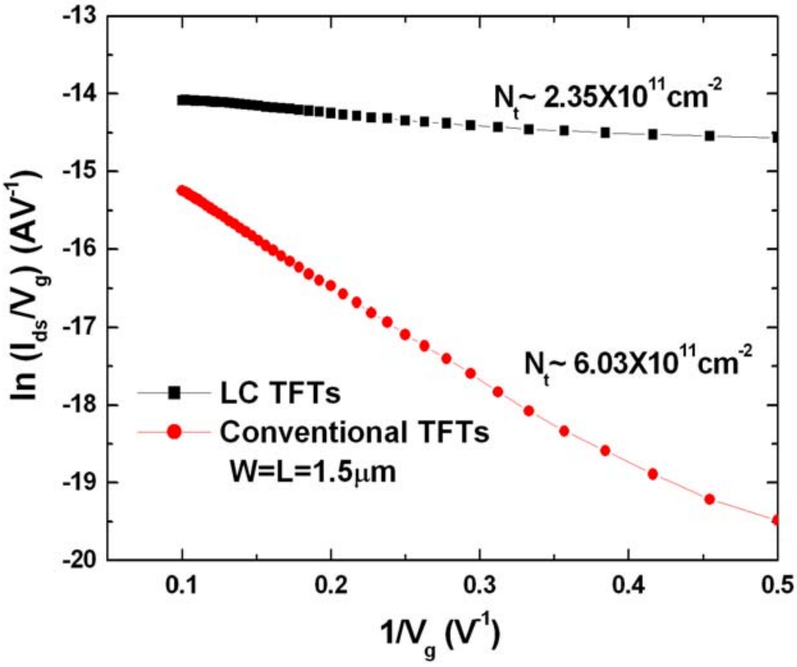


Figure 6-9. Plot of ln($I_D$/$V_{GS}$) versus 1/($V_{GS}$) curves at $V_{DS}$ = 0.1 V and high $V_{GS}$ for LC poly-Si TFTs and conventional ones.

# Chapter 7

# Ultra High-Performance Low Temperature Polycrystalline Silicon Thin-Film Transistors Fabricated via Diode-Pumped Solid-State Green Continuous Wave Laser Annealing

## 7.1 Introduction

Low-temperature polycrystalline silicon (LTPS) technology has been the most promising method to manufacture high performance thin film transistors (TFTs) for the past decades [7.1] – [7.3]. As compared to conventional a-Si TFTs, LTPS TFTs using excimer laser crystallization (ELC) technology have been promise to integrate display driver circuits on glass substrates such as integrated ambient light sensing, memory in pixel, integrated touch, ultra-low power display driving, advanced active matrix liquid crystal displays (AMLCDs) driving, and advanced active matrix organic light emitting displays (AMOLEDs) driving. The demands for thin, light-weight, compact, and high resolution displays are getting stronger in the mobile applications. Integrating large scale circuits in small area and reducing power consumption both are requisite features for mobile applications with high resolution or more functional LCDs [7.4]. In addition, as the mobility of poly-Si TFT is approaching that of single crystalline silicon, it is possible to realize system-on-panel (SOP) application which build an integrated drive circuit, sensors, controller IC, CPU as well as display on glass [7.5]. In order to achieve such features, short channel length of TFTs and precise control of analog circuits are required. However, the current conventional ELC LTPS technology can not meet the requirements owing to the large variation in electrical characteristics caused by grain boundaries in the channel regions. Although high-performance ELC LTPS TFTs with mobility exceeding 200 cm$^2$/Vs can be fabricated by optimizing the applied laser energy density and increasing the shot density per area, ELC LTPS TFTs suffer from poor uniformity of device performance due to the narrow laser process window for producing large-grain poly-Si. The fluctuation of pulse-to-pulse laser energy density, non-uniform laser beam profile, and non-uniformity of a-Si thin film thickness make laser energy density hard to hit the super lateral growth (SLG) regime everywhere [7.6] – [7.7]. Non-uniform and randomly distributed poly-Si grains will result in large variation of TFT performance when the laser energy density is controlled in the SLG regime, especially for small geometry TFTs [7.8]-[7.10]. Increasing laser shot density per area may improve the crystallization uniformity and promote the secondary grain growth [7.11], however, the mass production throughput will decrease. Besides, excimer laser annealing has some essential drawbacks such as complex optical system, high facility cost, troublesome maintenance, and poor output energy stability. As a result, novel crystallization methods are strong demanded to enhance both the device performance and uniformity for next generation LTPS TFTs.

Large-grained poly-Si thin films always result in high-performance LTPS TFTs by reducing the defect traps in the grain boundaries and the interior grains. Hence, recently, solid-state laser crystallizations of amorphous silicon, including pulsed YAG2ω green laser, selectively enlarging laser crystallization (SELAX), green laser annealing double layer x’tallization (GLADLAX), visible laser induced lateral crystallization (VILC), double–pulsed laser annealing, and the diode-pumped solid-state (DPSS) continuous wave laser lateral crystallization (CLC), have been widely studied by effectively enlarging the poly silicon grain size for high-performance TFTs as compared with conventional excimer laser crystallization

[7.12] – [7.43]. Among these crystallization methods, diode-pumped solid-state continuous wave laser lateral crystallization proposed by Hara et al. has been demonstrated to fabricate high-performance poly-Silicon TFTs on non-alkali glass substrate because of the large directional silicon grains. In addition, CW laser lateral crystallization has the advantages of simple process, superior power stability, wide laser process window for large grains, high throughput, and easy maintenance. The comparisons of excimer laser and DPSS continuous wave laser are listed in Table 7-1. In the previous work, although single-grain TFT has been demonstrated to exhibit high device performance and good uniformity, the grain size is limited to 2 μm. In order to produce ultra-large silicon grains in large area substrates for SOP, 3D-ICs, and solar cell applications, the CW laser crystallization of a-Si thin films is investigated.

Moreover, to further improve transistor performance, the source and drain contacts must require low sheet resistance and low defect density in drain junction. As a result, the implanted dopants in source and drain regions must be activated to a high degree. The energetic dopant ions cause significant damage to the silicon crystal structure near the surface regions during ion doping process. Activation is a thermal heating process to repair the lattice damaged regions into single-crystal structure and to activate the dopants. In ULSI silicon semiconductor processing, activation was performed by either a furnace anneal or rapid thermal processing (RTP). However, both these steps require temperatures well beyond the strain point of glass. In laser activation, the silicon was heated, melted and reformed without heating the glass, resulting in very high efficiency activation with low thermal budget. But the activation technology using CW laser was rarely studied. We will also investigate the dopant activation by CW laser annealing in this chapter. A comparison of the efficiency of dopant activation among various activation methods is studied in detail. The material properties of boron-doped poly-Si thin films by CW laser activation are analyzed by four point probe measurement system and secondary ion mass spectrometer (SIMS).

In this chapter, a novel and simple crystallization method to control lateral grain growth using frequency-doubled DPSS Nd:$YVO_4$ continuous-wave laser irradiation is proposed. At first, the experimental procedures and CW laser system setup are described in detail. Then, the CW laser-crystallized poly-Si thin film was analyzed by several material analyses, including SEM, Raman, AFM, TEM, XRD, EBSD, and the factors that affected the final lateral crystallization microstructure were also investigated, including, laser scanning speed, laser power, and the ambient. The experimental details of dopant activation are also discussed. Finally, CW laser crystallization mechanism of a-Si films and the results of crystallized poly-Si thin films and LTPS TFT performance are presented and analyzed; demonstrating the performance and uniformity enhancement achieved using the new crystallization method.

## 7.2 Experiments

Figure 7-1 shows the key processes for the fabrication of LTPS TFTs crystallized by using frequency-doubled diode-pumped solid-state Nd:$YVO_4$ continuous-wave laser irradiation. At first, a 500 Å-thick a-Si layer was deposited by pyrolysis of pure silane ($SiH_4$) with low pressure chemical vapor deposition (LPCVD) at 550°C on oxidized silicon wafer. Then, after standard RCA clean process, the samples were then subjected to green laser crystallization by diode-pumped solid-state continuous-wave laser ($\lambda$=532nm). During the laser irradiation, the samples were located on a substrate in air and substrate was maintained at room temperature. The power of laser energy density, the laser process ambient, and the laser scan speed were varied. The CW laser annealing was performed in the scanning mode with 88% overlapping with various laser energy powers and laser scan speed to investigate the effects of laser annealing conditions on the performance of fabricated continuous-wave-crystallized (CWC) LTPS TFTs. Several material analysis techniques were used to investigate the relation between the morphology of crystallized poly-Si thin films and laser process conditions. They include optical microscopy (OM), Raman spectroscopy analysis, scanning electron microscopy (SEM) analysis, X-ray diffraction (XRD) analysis, electron backscattering diffraction pattern (EBSD) analysis, transmission electron microscopy (TEM) analysis, and atomic force microscopy (AFM) analysis. In order to facilitate the SEM observation, some samples were processed by Secco-etch before analysis. After defining the device active region and standard RCA clean process, a 1000 Å-thick tetraethyl orthosilicate (TEOS) gate oxide layer was deposited by plasma-enhanced chemical vapor deposition (PECVD0 at 385°C. Then, a 2000 Å-thick a-Si thin film was then deposited by LPCVD at 550 °C for gate electrode. The a-Si thin film and gate oxide were etched by reactive ion etching (RIE) and buffer oxide etchant (BOE) to form the gate electrode. A self-aligned boron or phosphorous ion implantation with dose of $5\times10^{15}cm^{-2}$ was carried out to form source and drain regions. Next, a 3000 Å-thick TEOS passivation oxide was deposited by PECVD at 350°C and the implanted dopants were activated by laser annealing at room temperature in the air ambient . After contact hole opening by reactive ion etching, aluminum thin film with a thickness of 5000 Å was deposited by sputtering and Al metal pads were patterned to complete the fabrication of CW laser annealed LTPS TFTs. Then, a 30-min sintering process was performed at 400°C in the $N_2$ ambient to reduce the contact series resistance of the source and drain electrodes. Finally, LTPS TFTs were passivated by 2-h $NH_3$ plasma treatment to further improve the device performance. For the sake of comparison, the conventional excimer-laser-crystallized LTPS TFTs with a channel thickness of 500Å were also fabricated. In addition, the doped polycrystalline silicon thin films via various activation methods were analyzed by using four point probe measurement system and secondary ion mass spectrometer (SIMS).

Current-voltage (I-V) characteristics of the fabricated devices were measured using a semiconductor parameter analyzer of Agilent technologies 4156C. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of $I_{ds}$ = (W/L) x $10^{-8}$ A at $V_{ds}$ = 0.1 V. The transconductance, field-effect mobility and subthreshold swing were extracted at $V_{ds}$ = 0.1 V, and the $I_{on}/I_{off}$ current ratio was defined at $V_{ds}$ = 3 V. A scanning electron microscopy (SEM) (S4700, Hitachi) was used to get the surface micrograph of poly-Si thin films after Secco-etch. An analytical field-emission transmission electron microscopy (TEM) (JEM-2100FX, JEOL Ltd.) was employed to analyze the microstructure and crystallinity of poly-Si film in the channel region. Atomic force microscopy (AFM) was utilized to analyze the grain size and surface morphology of laser-crystallized poly-Si films. X-ray diffraction (XRD) analysis and Electron backscattered diffraction pattern (EBSD) analyses are performed to investigated the crystallinity and the preferential orientation of the CW laser-crystallized poly-Si thin films.

## 7.3 Results and Discussion

### 7.3.1 Material Characterization of Poly-Si Thin Films Crystallized by Diode-Pumped Solid-State Continuous Wave Laser

The principle setup of Diode-Pumped Solid-State (DPSS) continuous-wave (CW) laser crystallization apparatus is shown in Figure 7-2. The heart of the experiment is the frequency-doubled diode-pumped solid-state Nd:$YVO_4$ continuous-wave laser, operating at the wavelength of 532 nm. The laser can achieve a maximum peak output power ~ 18 watt and the sample can move with a maximum speed of 100 cm/s. The sample is crystallized and scanned via laser beam scanning and overlapping on the x-y translation stage in a vacuum chamber. The overlap helps to improve the uniformity of CW laser-crystallized poly-Si thin films because the crystallinity of poly-Si film in the middle regions of the laser pulse is better than that in the edges of laser pulse. Crystallization of large area is achieved by moving the sample beneath the laser beam via controlling the movement of the x-y translation stage. The scanning direction is along the short axis direction. The velocity of the x-y translation stage during crystallization process can be adjusted depending on the laser power and the ambient. In addition, the crystallization experiments can be performed at either room temperature or 500°C.

Figure 7-3 shows the sheet resistance of samples after excimer laser activation by four-point probe measurement system. The energy fluence of excimer laser was varied from 190mJ/cm$^2$ to 390mJ/cm$^2$. As expected, the higher energy density, the lower sheet resistance was achieved. It was attributed that there were more heat and longer activation time in the doped a-Si thin films at higher energy density. Since more implanted atoms were aligned into the correct lattice sites and the damaged lattice regions were recovered into single-crystal structure, the sheet resistance of laser-crystallized poly-Si films could be lower.

Figure 7-4 and Figure 7-5 show the sheet resistance of samples after DPSS CW laser activation with laser power of 10 W and 15W by four-point probe system, respectively. According to the Figure 7-4, the slower CW laser scanning speed, the lower sheet resistance was attained attributed to the longer annealing time, especially in the low ion implantation dosage. Figure 7-5 displays similar results and the CW laser-annealed polycrystalline silicon films with a low sheet resistance of 50 Ω/□, which is suitable to form ohmic contacts between source/drain silicon regions and contact metal. The sheet resistances of samples after furnace annealing, rapid thermal annealing, CW laser activation, and excimer laser activation were summarized in Table 7-2. Figure 7-6 shows the SIMS redistribution profiles of boron atoms after CW laser annealing. Dopant profiles in the polycrystalline silicon thin films after CW laser were redistributed as uniformly as that of excimer laser ones. Therefore, CW laser activation was a low thermal-budget and high efficiency method.

Figure 7-7 (a) shows a SEM graph of continuous-wave laser crystallized poly-Si film with laser power of 8W and laser scanning speed of 1cm/s after Secco etching. In this case, the laser energy fluence is sufficient to induce surface melting of amorphous or crystalline silicon thin films but laser energy density is still low. The laser fluence is larger than the threshold energy of crystallization but is low enough that a continuous layer of solid Si remains (i.e., melt-depth < film thickness). Therefore, the grain size is limited by high quenching rate. As a result, laser power increases, larger poly-Si grains are produced. Figure 7-7 (b) displays a SEM graph of continuous-wave laser crystallized poly-Si film with laser power of 10W and laser scanning speed of 1cm/s after Secco etching. The grain size is about 0.3 μm and is larger than that of 8W. As laser power increases to 12W, the a-Si thin film is completely melting due to high laser energy. In this situation, a lateral grain growth can be stimulated by continuous-wave laser crystallization. Figure 7-7 (c) displays a SEM graph of continuous-wave laser crystallized poly-Si with laser power of 12W and laser scanning speed of 5cm/s after Secco etching. A directional grain growth with size of 15 μm in length can be stimulated and the grain boundaries are generally parallel to each other and to the laser scan direction by the continuous-wave laser crystallization. According to SLG model, the lateral grain growth is resulted from a thermal gradient in solid/liquid interface. The SLG distance is determined by the quenching rate of liquid silicon and the lateral growth velocity which is a function of lateral thermal gradient. Therefore, the SLG distance can be increased by enlarging the lateral thermal gradient. In the experiments of continuous wave laser crystallization of a-Si thin films, CW laser crystallization method makes it easy to form directional large grains (15 μm in length) owing to the continuous energy supply and slow cooling rate of the molten Si without damage to the substrates via controlling the laser scanning speed and laser power suitably. Figure 7-7 (d) shows the damaged poly-Si thin films after CW laser irradiation due to the too high laser energy power.

Figure 7-8 displays the SEM graphs of continuous-wave laser crystallized poly-Si film with laser power of 12W and laser scanning speed of 5 cm/s after Secco etching. From the magnified SEM images, it can be obviously distinguished that there are four different kinds of silicon grain structure in the CW-laser crystallized poly-Si thin films with single scanning mode. The laser scan direction is from the bottom to the top of the image. According to the magnified image of region I, it is composed of discrete silicon islands after Secco-etching which means that a-Si at region I did not melt during the CW laser scanning. The crystallized region is distinguished by the grain size from region II to IV. It is clearly observed that the river-like region IV (center region) in the center of crystallized region is composed of directionally solidified large grains as shown in Fig.7-8. It indicates that the region IV was completely melting and then sequentially crystallized along the CW laser scanning direction. In the magnified SEM images of regions II (edge region) and III (transition region), it is obvious that the grains in regions II through III are getting larger. The poly-Si grain structures in the region II composed of small and fine grains with the average size of several tens of nanometers are identical with that of solid phase crystallized (SPC) poly-Si films. The poly-Si grain structures in the region III composed of large grains with the average size of several micrometers are identical with that of mixed solid-liquid phase crystallized poly-Si films. It is noted that the microstructure of region III is similar that of conventional ELA poly-Si grain. It is well-known that the electrical characteristics of poly-Si TFTs are deeply influenced on the microstructure of poly-Si thin films and the grain boundaries within the active channel region strongly degrade the TFT performance. As expected, the directional large grains with excellent quality in the region IV are the optimal condition for the device fabrication and circuit application. The TFTs fabricated in the region IV will exhibit the best performance, including high field-effect mobility, steeper subthreshold swing, and low leakage current. Consequently, in order to crystallize large area with directional large grains, the CW laser scanning with an overlapping 88% between the traces is performed. An overlapping 88% leads to melting the region in the middle of the previously crystallized trace, resulting in an epitaxial growth from its central region. As aresult, the size of the grains is expected to exceed the width of a single trace.

Raman spectroscopy is a standard non-destructive characterization method in the field of silicon thin film. It has been proven to be sensitive to the composition, crystallinity, thermal stress and phonon correlation length. By measuring the Raman spectra in the range of 100 ~ 900 $cm^{-1}$, information on the crystallinity can be obtained. Figure 7-9 displays the Raman peak intensity of the CW laser crystallized poly-Si thin films as a function of crystallization region, for which the crystallization was carried out at room temperature. In the center region of CW laser crystallized poly-Si thin film, it exhibits the best crystallinity due to highest Raman peak intensity and the narrowest FWHM, which is consistent with SEM images [7.37], [7.44]. Figure 7-10 displays the dependence of Raman peak intensity of the crystallized poly-Si thin films on different crystallization methods. As shown in these figures, the broad band of the as-deposited a-Si thin film represents no crystalline phase existing inside the film. After laser irradiation, a sharper Raman peak (at 520$cm^{-1}$) with great intensity of the poly-Si thin films implies an improvement in the crystallinity. Poly-Si grains fabricated by continuous-wave laser crystallization exhibit better crystallinity than those of excimer laser crystallization. Because the duration of continuous-wave crystallization is longer than that of excimer laser crystallization and a large thermal gradient is induced by CW laser irradiation, the directional larger grains form due to longer time for grain growth by CW laser. And the thermal stress of poly-Si thin films crystallized by CW laser is larger than that by ELA due to its long melting duration.

The crystallinity and the preferential orientation of the CW laser-crystallized poly-Si thin films are also analyzed by X-ray diffraction (XRD) analysis. It is reported that CW laser crystallized poly-Si thin films will have a strong preferential (100) normal orientation [7.39]. Figure 7-11 displays the XRD result of continuous wave laser crystallized poly-Si thin film. In this case, the a-Si thin film of 50 nm was crystallized by laser power of 12 W, laser scanning speed of 5 cm/sec, and substrate temperature of room temperature. The diffraction peaks appearing at around $2\Theta = 28.5^{\circ}$, $47.5^{\circ}$, $58.1^{\circ}$and $76.5^{\circ}$ represent the diffraction peaks from the (111), (220), (311) and (400) planes, respectively. This is confirmed the silicon thin film deposited in an amorphous state can be effectively converted to polycrystalline state after CW laser irradiation. In addition, the result shows that the CW laser crystallized poly-Si thin film, which was crystallized in large grain size regime, exhibits the random orientation in this experiment.

Electron backscattered diffraction pattern (EBSD) is a method of analyzing the microstructure and orientation simultaneously. The advantage of EBSD over TEM is that the orientation acquiring procedure is completely automated and data can be acquired from the entire surface of the sample. Because quantitatively reliable orientation data acquisition from EBSD is much easier than those from TEM, using high resolution EBSD system on a field emission scanning electron microscopy (FESEM) recently have been attracted much attention for analyzing the crystalline properties of poly Si thin film. The crystallographic properties of the CW laser crystallized poly Si thin films are examined by the EBSD technique. A JEOL 6500F Schottky type FESEM equipped with Oxford INCA Crystal EBSD system is used for EBSD analysis. EBSD experiments are carried out at 15 kV accelerating voltage and 4 nA probe current. Pseudo-Kikuchi patterns were integrated for 180 ms in each analysis point and the step size for the orientation mapping was 0.5 μm. The typical surface normal orientation maps of CW laser crystallized poly Si films acquired from EBSD technique are shown in Figure 7-12. Each color indicates the specific crystallographic direction, and it is also shown as a color triangle. Inverse pole figure of orientation of normal direction is also shown in Figure 7-12. A single grain is regards as a region with the same crystallographic orientations and same phases. Therefore, it is quite reasonable to identify the grains from EBSD data that consist of orientation data. CW laser poly Si grain is larger than that of conventional ELA poly Si. The river-like poly-Si grains with the average size of about 15 μm in length and 2 μm in width are crystallized by CW laser, while the random polygonal poly Si grain structures with the average size of about 0.5 μm in diameter are crystallized by conventional ELA. Besides the large poly-Si grains, the orientations inside the grains are almost identical and the normal direction to the surface shows random oriented <110>, <100>, <111> directions from EBSD analysis. The crystallinity of the grain is excellent due to the same specific color. Grain boundaries between adjacent grains are distinguished by high-angle misorientation. The neighboring poly-Si grains do not have the same color, indicating multiple orientations appearing in the CW laser-crystallized poly-Si thin films. The electron EBSD results are similar to those attained by XRD, as shown in Figure 7-11.

Figure 7-13 (a) and 7-13 (b) are the AFM images of the poly-Si films crystallized by CW laser with a power of 12 watt. The image was taken from the as-crystallized sample with single scan and the width of directionally solidified large grains is about 80 μm, as shown in Figure 7-13(a). The mountain-like grains can be clearly distinguished and the grains extend in tens of micron. The reason for this is the 10% density change between solid and liquid phases of silicon, (2.53 g/cm$^3$ for the liquid and 2.30 g/cm$^3$ for the solid) provides a driving force for the mass transport induced by surface tension in the molten silicon during the laser crystallization. The root-mean-square (rms) roughness and maximum height of the crystallized poly-Si thin film shown in Figure 7-13 (b) is 6.912 nm and 55.41 nm, respectively. Figure 7-14 shows the comparisons of AFM images of poly-Si grain structure and surface roughness crystallized by the DPSS CW laser crystallization and excimer laser crystallization methods, respectively. Indeed, CW laser crystallized poly-Si grains exhibit large silicon grain size than the conventional ELC poly silicon grains. However, the surface roughness of CW laser-crystallized and excimer laser-crystallized poly-Si thin films are both quite large due to the mass transport during laser crystallization. From a device standpoint, such a high surface roughness occurring in CW laser crystallization regime may be problematic because the reliability, uniformity, and gate dielectric integration of poly-Si TFTs are degraded.

Figure 7-15 shows the plane-view bright-field TEM images of continuous-wave laser crystallized poly-Si thin films. The plane-view TEM image displays a directional river-like lateral Si grain growth with tens of micron. The magnified plane-view TEM image and the selected-area electron diffraction pattern reveal that the crystallite exhibits <111> orientation with excellent quality. The diffraction pattern from the CW laser crystallite is made up of simple spots, and this means a single-crystal silicon region is formed by this novel CW laser crystallization. Figure 7-16 displays the cross-sectional TEM images of CW laser crystallized poly-Si thin film and excimer laser crystallized poly-Si thin film, respectively. The cross-sectional TEM picture shows that the surface morphology of continuous-wave laser crystallized poly-Si films is fairly flat at the grain boundary, while a rigid at the grain boundary is formed in the excimer laser crystallized poly-Si films. In order to further confirm the surface roughness at the grain boundary and the crystallinity of silicon grains, more cross-sectional images of CW laser crystallized poly-Si thin films are investigated by TEM technique. According to the Figure 7-17 of the cross-sectional TEM images and the selected area electron diffraction patterns, a clear interface between poly-Si and buffer oxide is confirmed and the crystallinity of poly-Si grain is excellent. Moreover, CW laser-crystallized poly-Si films are quietly smooth and do not form a rigid at the grain boundary. Figure 7-18 demonstrate the high-resolution cross-sectional TEM image and the selected-area electron diffraction pattern of the CW laser-crystallized crystallite. The diffraction pattern reveals that the crystallite exhibits single-crystal silicon with <110> orientation along the direction of film grain growth.

### 7.3.2 Crystallization Mechanism of Diode-Pumped Solid-State Continuous Wave Laser-Crystallized Poly-Si Thin Films

Figure 7-19(a) exhibits the mechanism of continuous-wave laser lateral grain growth to explain the directional-controlled poly-Si thin films via controlling the laser power and laser scan speed. In the SLG regime of ELC, the maximum point of melting the un-melted portion of the underlying Si no longer forms a continuous layer but instead consists of islands of solid that are separated by small local regions of completely molten silicon. The un-melted islands act as solidification seeds, from which a lateral grain growth commences. However, in the CW laser crystallization, a lateral temperature gradient can be created between the adjacent areas and there must be un-melting solid Si to act as the seeds for lateral crystallization. By completely melting the a-Si thin film in a certain region using CW laser and the solidified poly-Si films at the adjacent area, a large lateral temperature gradient will exist between the complete melting high-temperature liquid-phase region and un-melting low-temperature solid-phase seeds, and grains will grow laterally towards the complete melting region from the un-melting solid seeds. As a result, if the temperature gradient is stable in the liquid-solid interface by suitable laser power and laser scan speed, directional lateral grain growth of several hundred micrometers can be achieved easily. The lateral grain growth will eventually be arrested by lateral grains grown from the other side.

### 7.3.3 Electrical Characteristics of LTPS TFTs Fabricated Using Diode-Pumped Solid-State Continuous Wave Laser Annealing

Producing large poly-Si grains and controlling lateral grain growth at the desired region can be realized by DPSS CW laser crystallization. Large and uniform longitudinal grains could be formed in the device channel regions via controlling the laser scanning speed and laser power. From the above results, as the directional grain growth with size of 15 μm in length can be stimulated and the grain boundaries are generally parallel to the laser scan direction by the continuous-wave laser crystallization, TFT performance and device-to-device uniformity can be improved.

Figure 7-20 (a) compares the transfer characteristics of the n-channel LTPS TFTs using CW laser crystallization (CWC) with those by ELC with W = L = 2 μm at drain voltages ($V_{ds}$) of 0.1 and 3 V. The CWC LTPS TFTs are fabricated with optimal laser condition of laser power of 12 W and laser scan speed of 5 cm/s. For the conventional ELC LTPS TFTs, the laser condition is controlled in the SLG regime with laser shot density per area of 100 to fabricate high-performance LTPS TFTs. The n-channel CWC TFTs exhibit superior performance with the field-effect mobility of 505 $cm^2$/V-s, subthreshold swing of 105 mV/dec, on/off current ratio of $3.94 \times 10^{10}$, drain-induced-barrier-lowering of 15.2 mV/V, and threshold voltage of -0.312 V to the n-channel ELC TFTs with the field-effect mobility of 130 $cm^2$/V-s, subthreshold swing of 277 mV/dec, on/off current ratio of $1.4 \times 10^{10}$, drain-induced-barrier-lowering of 124 mV/V, and threshold voltage of -0.375 V. CWC TFTs display higher on-current, higher field-effect mobility, steeper subthreshold slope, lower leakage current, and lower threshold voltage due to the single-crystal-like silicon grains in the device channel regions as compared to the ELC TFTs. Figure 7-20 (b) compares the ourput characteristics of the n-channel CWC LTPS TFTs with those of ELC ones with W = L = 2 μm. In order to avoid the threshold voltage difference, the applied gate driving voltages in Fig. 7-20 (b) are kept at constant values of $|Vg-Vth|$ = 4 V, 8 V, 12 V, and 16 V, respectively. It is demonstrated that CWC TFTs with large directional grains demonstrate higher driving current than conventional ELC TFTs under the same bias condition owing to the higher field-effect mobility. The high field-effect mobility is attributed to the high quality poly-Si thin films with reduced grain boundaries in the device channel region. Figure 7-21 displays the basic electrical characteristics of the n-channel and p-channel LTPS TFTs using CW laser crystallization. Some important electrical characteristics of LTPS TFTs are also listed in Table

7-3. The p-channel CWC TFTs exhibit excellent performance with the field-effect mobility of 212 cm$^2$/V-s, subthreshold swing of 127 mV/dec, on/off current ratio of 1.02 × $10^9$, drain-induced-barrier-lowering of 30.8 mV/V, and threshold voltage of -0.712 V. Owing to large longitudinal grains growth in the channel regions, LTPS TFTs crystallized using CW laser exhibited better electrical characteristics than the ELC ones. Ultra high-performance CWC LTPS TFTs with field effect mobility of 505 cm$^2$/V-s for n-channel and 212 cm$^2$/V-s for p-channel, substhreshold swing of 105 mV/dec for n-channel and 127 mV/dec for p-channel, on/off current ratio more than $10^9$ for n- and p-channel, and good ohmic contacts for n- and p-channel can be achieved. These values are comparable to those of single-crystal silicon MOSFET. In addition to the enhancement of LTPS TFT performance, LTPS TFT crystallized by CW laser also exhibited better uniformity due to the wide laser process window as compared with excimer laser crystallization of a-Si thin films. For large directional grain growth, there are similar grain structures in the channel region. As a result, a wide laser process window for producing high-performance LTPS TFTs was shown in both short and long device structures.

Two different grain structures in the channel regions are fabricated to investigate the effect of grain boundaries on TFT performance. One device is the channel length parallel to the direction of the lateral grain growth induced by CW laser crystallization; the other one is the channel length perpendicular to the direction of the lateral grain growth induced by CW laser crystallization. Figure 7-22(a) and 7-22(b) are the comparisons of Id-Vg and Id-Vd curves for CWC TFTs which the directions of source to drain are structurally parallel and perpendicular to the direction of laser scanning, respectively. Some important electrical characteristics of LTPS TFTs are also listed in Table 7-4. The driving current and the field-effect mobility are higher in the parallel CWC TFTs due to the carriers hardly interrupted by grain boundaries parallel to the current direction.

## 7.4 Summary

A new and simple diode-pumped solid-state (DPSS) continuous-wave (CW) laser crystallization is also proposed to produce lateral grain growth via controlling the laser scanning speed and laser power. As compared with excimer laser, DPSS CW laser ($\lambda = 532$ nm) exhibit superior power stability. The CW laser-crystallized poly-Si thin film was analyzed by several material analyses, including SEM, Raman, AFM, TEM, and the factors that affected the final lateral crystallization microstructure were also investigated, including, laser scanning speed, laser power, and the ambient. From the magnified SEM images, it can be obviously distinguished that there are four different kinds of silicon grain structure in the CW-laser crystallized poly-Si thin films with single scanning mode. In order to crystallize large area with directional large grains for high TFT performance with good uniformity, the CW laser scanning with an overlapping 88% between the traces is performed. From the SEM and AFM analyses, CW laser lateral crystallization makes it easy to form directional large grains (15 μm in length) owing to the continuous energy supply and slow cooling rate of the molten Si without damage to the glass substrates. In addition, the plane-view TEM pictures and selected-area electron diffraction pattern display a directional river-like lateral Si grain growth with tens of micron and excellent crystallinity due to the clear dots, respectively. From the cross-sectional TEM picture, a flat surface morphology is formed at the grain boundary which is suitable for gate oxide scale down. According to the experimental results, ultra high-performance CW laser-crystallized LTPS TFTs have been demonstrated on the oxidized silicon wafer for the first time with field-effect mobility of 505 $cm^2$/V-s for n-channel devices and 212 $cm^2$/V-s for p-channel devices, subthreshold swing of 105 mV/dec for n-channel and 127 mV/dec for p-channel, drain-induced-barrier-lowering of 15.2 mV/V for n-channel and 30.8 mV/V for p-channel, and on/off current ratio more than $10^9$ for n-channel and p-channel devices. Besides, dopant activation by CW laser annealing is also studied. A comparison of the efficiency of dopant activation among various activation methods is studied in detail. It can be found that CW laser annealing is a low-thermal budget and high-efficiency activation method attributed to the low sheet resistance of 50 Ω/□ and uniformly redistributed dopant profiles after CW laser annealing. CW laser-annealed LTPS TFTs are, therefore, very promising for the future system-on-panel (SOP), solar cell, and 3D-ICs applications because of the simple process.

Table 7-1

The comparisons of excimer laser and DPSS continuous wave laser.

| Laser type | Pulse laser (Excimer laser) | CW laser (DPSS) |
|---|---|---|
| Irradiation time | Few tens ns | ∞ |
| wavelength | UV range (XeCl, ArF etc) | Visible range (532 nm, Green) |
| A-Si absorption coefficient (cm-1) | $10^{6}$ | $10^{5}$ |
| Power stability | ± 10% | ± 1% |
| Optical elements | Quartz | Glass |
| Process ambient | Vacuum/Air | Air |
| Growth mechanism | Random nucleation and growth | Continuous lateral crystallization |
| Cost (facility + maintenance) | High | Low |

Table 7-2

Measured sheet resistance of samples after various activation methods.

| Sheet resistance Ω/□ | B11 (5E15) |
|---|---|
| CW laser 15 W | 50 |
| CW laser 10 W | 141 |
| Excimer laser 390 mJ/cm2 | 55 |
| RTA 650℃ 60s | 108 |
| FA 600℃ 24hrs | 93 |

**Table 7-3**

Measured electrical characteristics of LTPS TFTs crystallized by DPSS CW laser and excimer laser.

| TFT Structures | Threshold Voltage (V) | Field-effect mobility (cm2/Vs) | Subthreshold Swing (V/dec) | DIBL (mV/V) | On/off current ratio |
|---|---|---|---|---|---|
| **N-channel CWC (W=L=2um)** | **-0.312** | **505** | **0.105** | **15.2** | **3.94x $10^{10}$** |
| **N-channel ELC (W=L=2um)** | **-0.375** | **130** | **0.277** | **124** | **1.41x $10^{10}$** |
| **P-channel CWC (W=L=2um)** | **-0.712** | **212** | **0.127** | **30.8** | **1.02x $10^{9}$** |

**Table 7-4**

Comparisons of CWC TFTs channel length structurally parallel and perpendicular to the direction of laser scanning.

| TFT Structures | Threshold Voltage (V) | Field-effect Mobility (cm$^2$/Vs) | Subthreshold Swing (V/dec) | On/off current ratio |
|---|---|---|---|---|
| **Parallel CWC TFTs (W=L=10um)** | 0.90 | 195 | 0.107 | 4.4x $10^{10}$ |
| **Perpendicular CWC TFTs (W=L=10um)** | 2.41 | 68 | 0.179 | 6.7x $10^{8}$ |
| **Parallel CWC TFTs (W=L=5um)** | 0.98 | 226 | 0.148 | 8x $10^{9}$ |
| **Perpendicular CWC TFTs (W=L=5um)** | 0.828 | 99 | 0.133 | 1.1x $10^{9}$ |

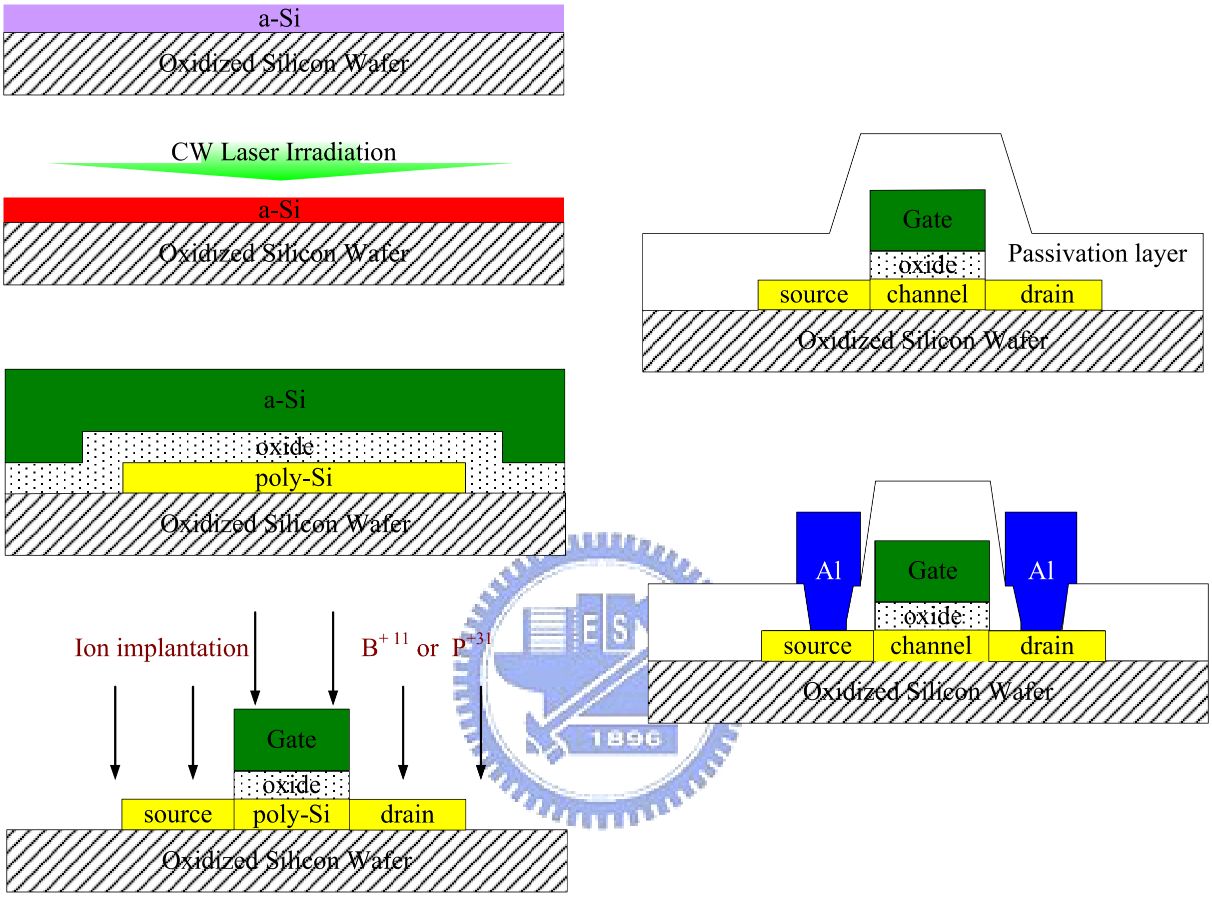
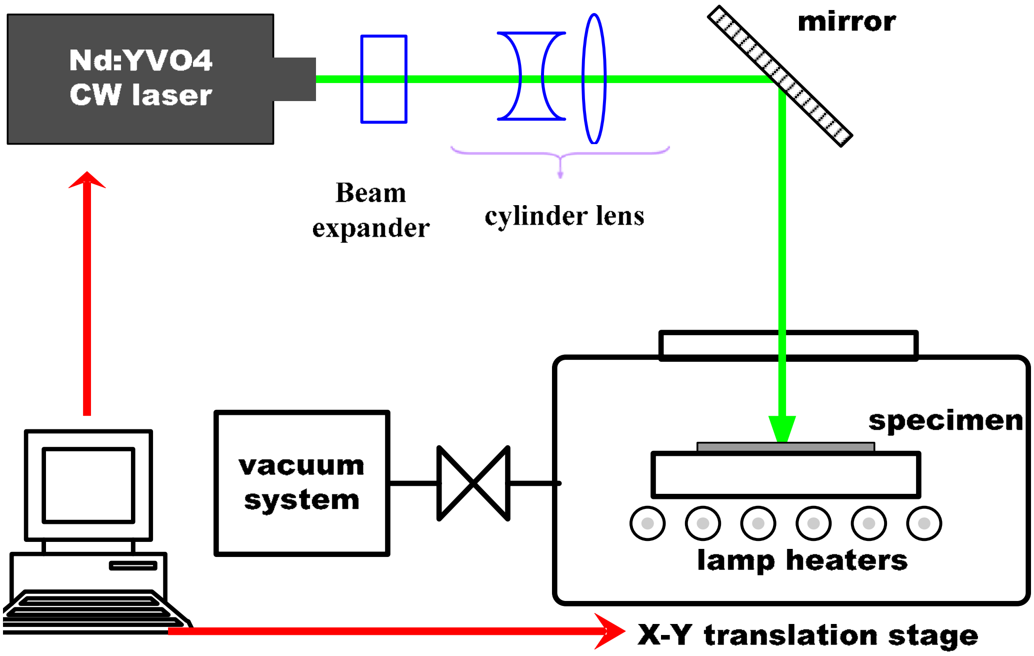


Figure 7-1. The process procedures of fabricating CWC LTPS TFTs.



■ **Coherent, Verdi-V18, Diode-Pumped Solid- State (DPSS) Laser Nd:$YVO_4$**

- CW mode
- Output power : 18W Max
- λ = 532nm, single frequency
- 400 um × 100 um laser spot
- Gaussian uniform profile

■ **X-Y translation Stage**

- Substrate size : 310X470mm$^2$
- Moving speed :    50cm/s Max
- Moving resolution : 1um
- Substrate heating : 500$^0$C Max

Figure 7-2. The setup of DPSS continuous-wave laser crystallization.

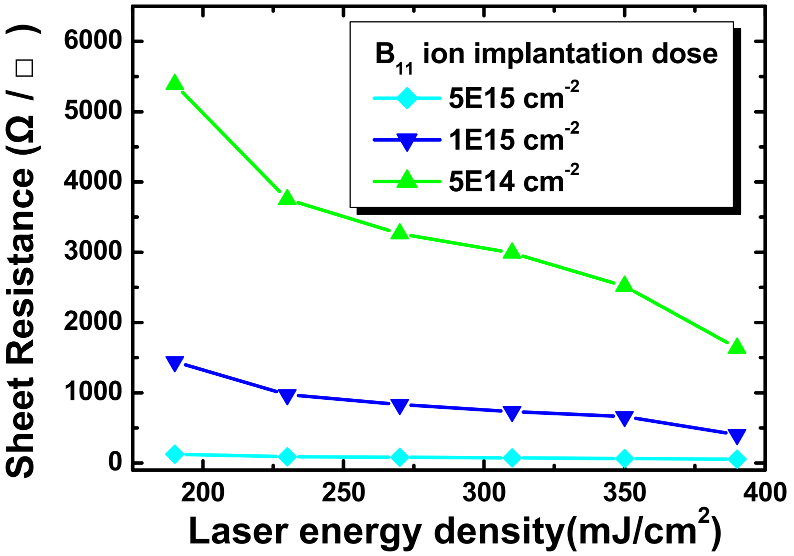


Figure 7-3. The sheet resistance of boron-doped silicon films after excimer laser activation.

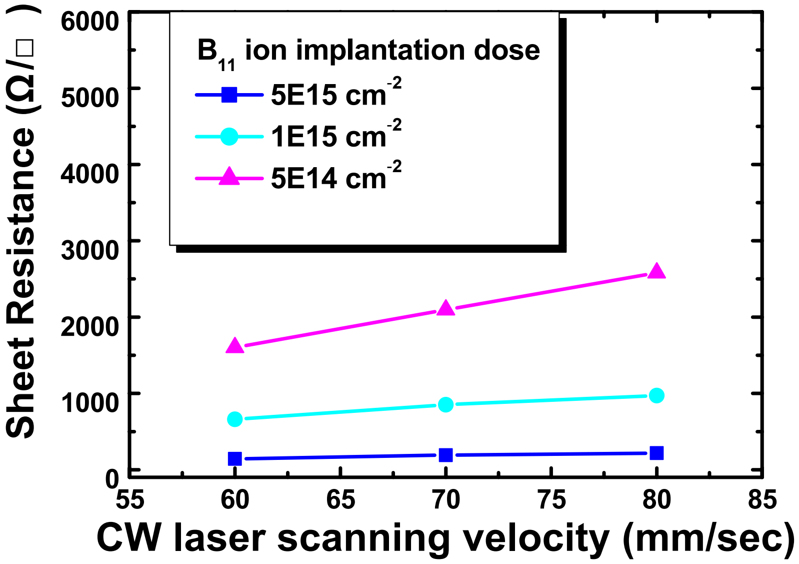


Figure 7-4. The sheet resistance of boron-doped silicon films after CW laser activation with laser power of 10 W.

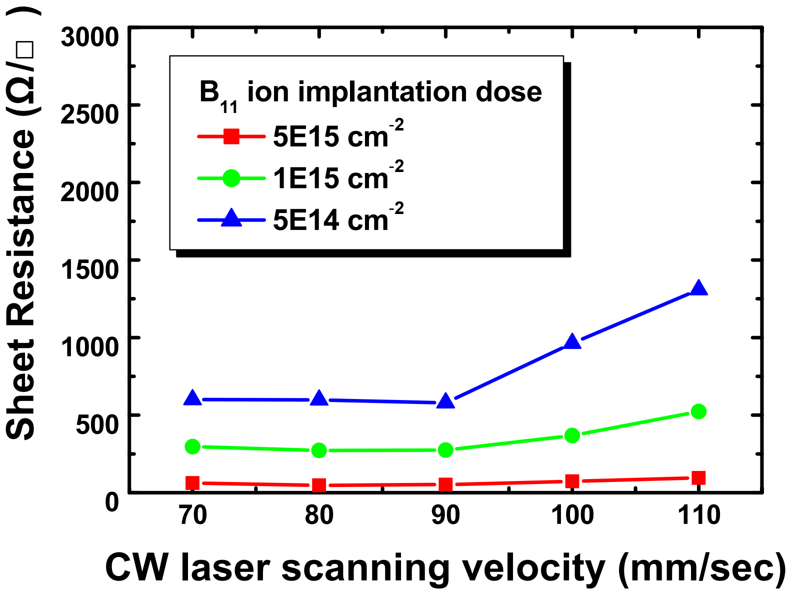


Figure 7-5. The sheet resistance of boron-doped silicon films after CW laser activation with laser power of 15 W.

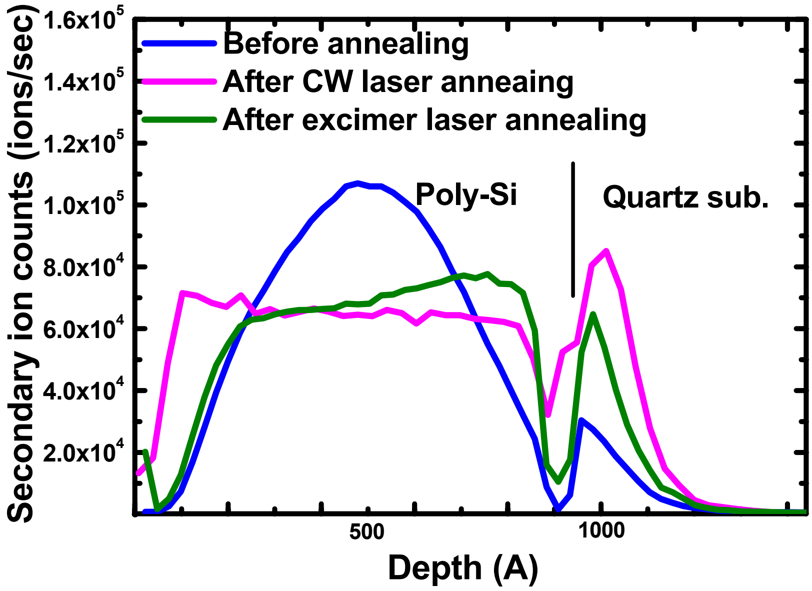


Figure 7-6. The SIMS redistribution profiles of boron atoms after laser annealing.

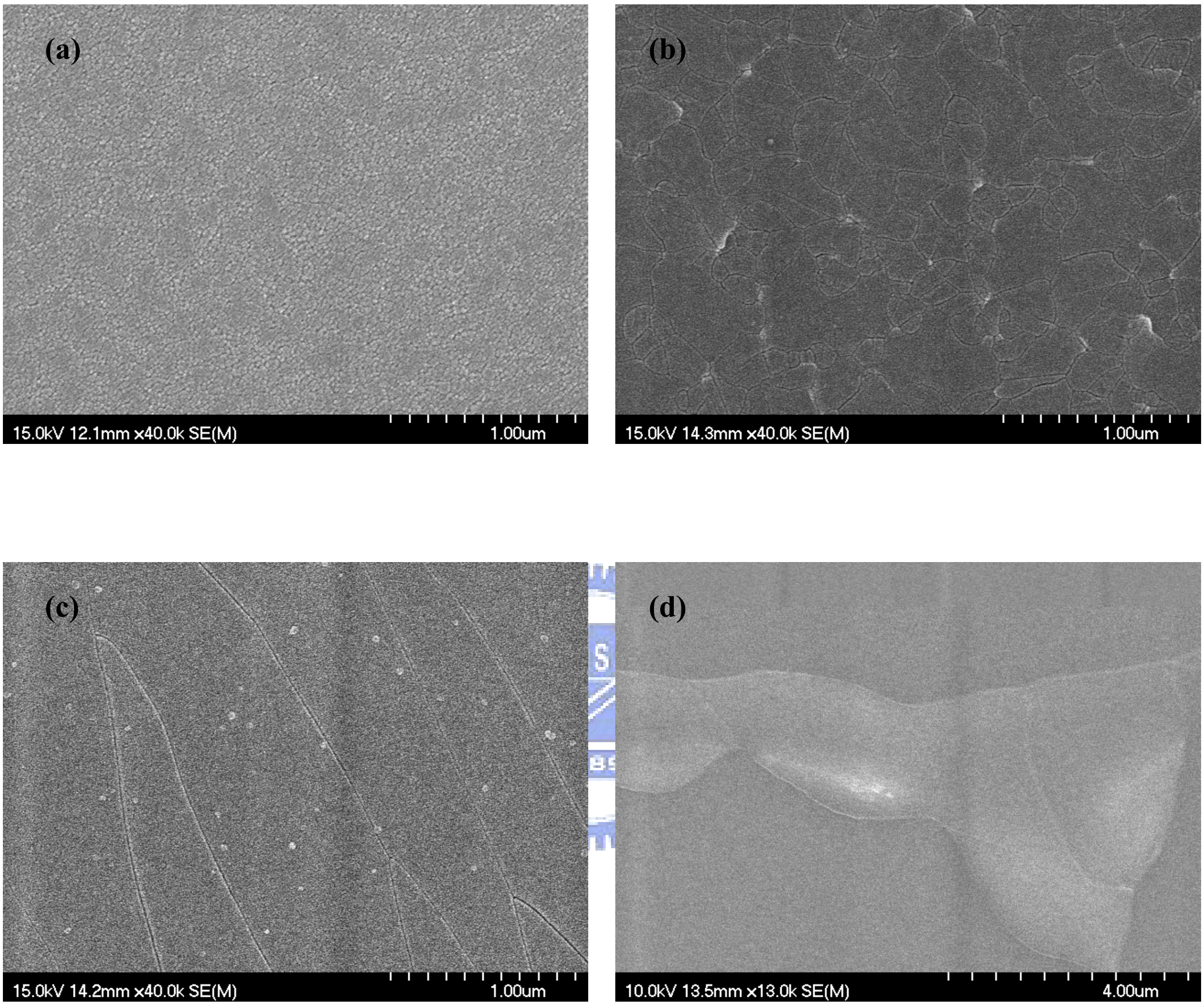


Figure 7-7. SEM graphs of poly-Si films crystallized by CW laser with different power of (a) 8 watt, (b) 10watt, (c) 12watt, and (d) 14watt.

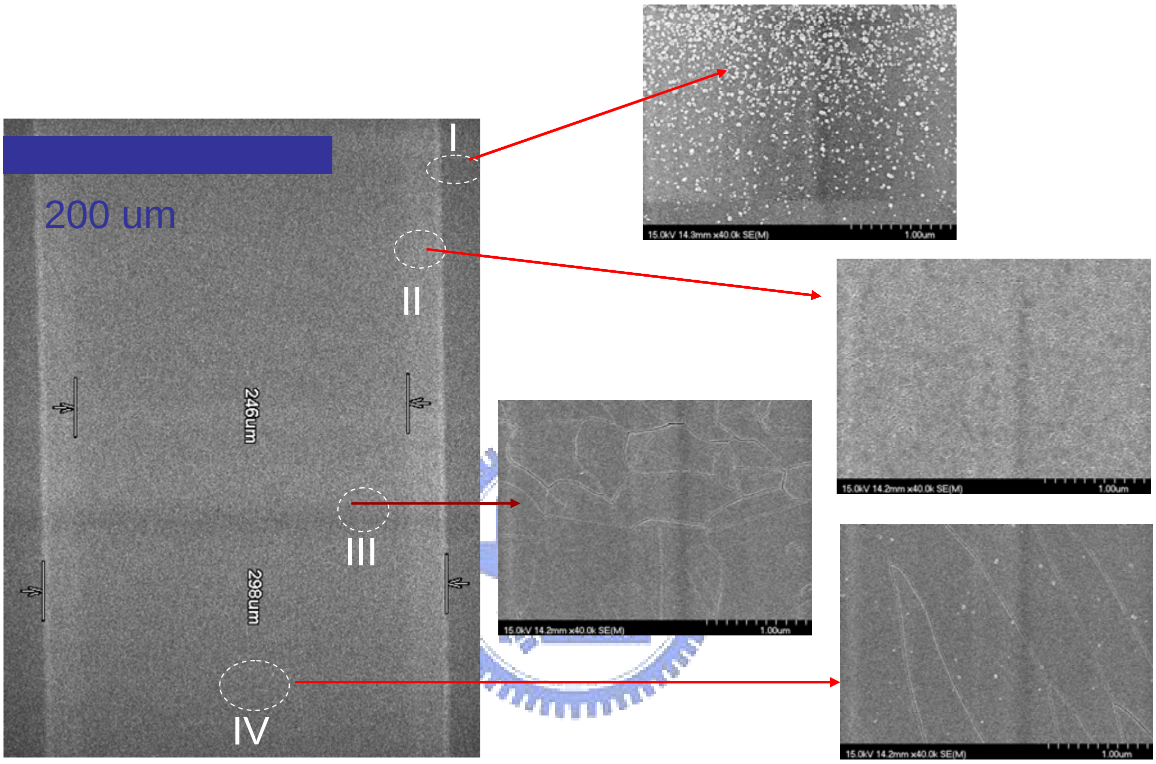


Figure 7-8. SEM graphs of a sample crystallized by CW laser with laser power of 12 W and laser scanning speed of 5 cm/s after Secco etching.

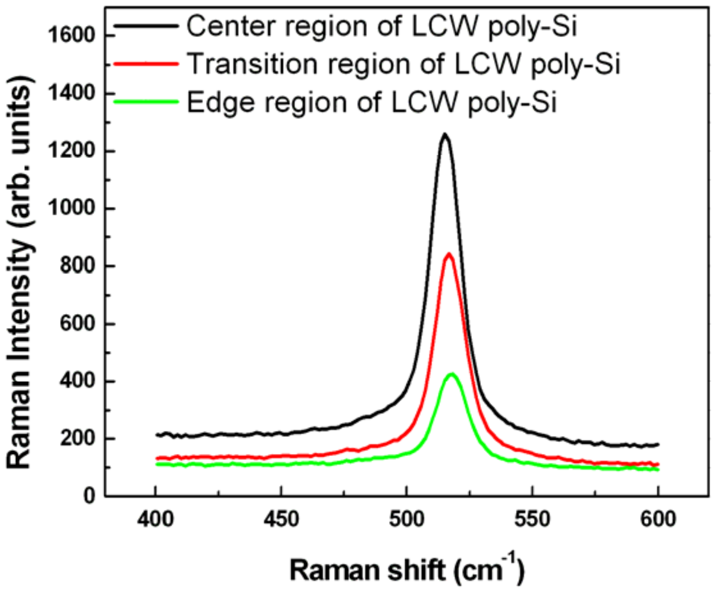


Figure 7-9. Raman peak intensity of the CW laser-crystallized poly-Si thin films with laser power of 12W as a function of crystallization region, for which the crystallization was carried out at room temperature.

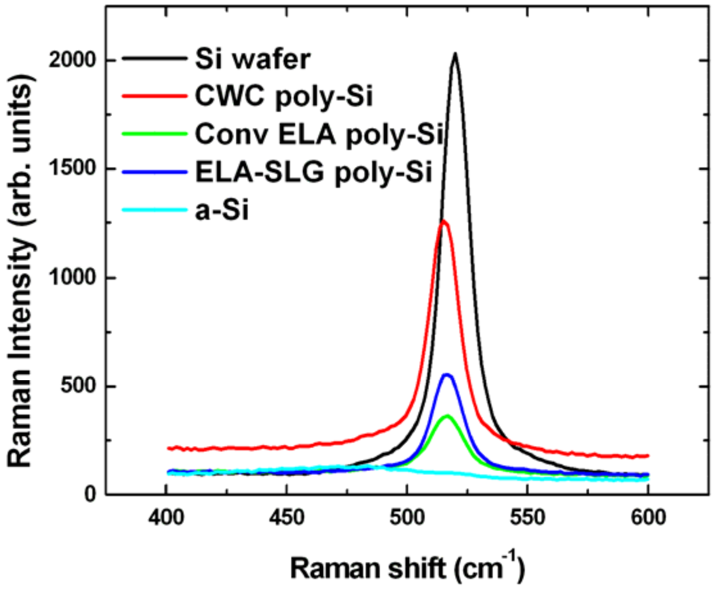


Figure 7-10. The dependence of Raman peak intensity of the crystallized poly-Si thin films on different crystallization methods.

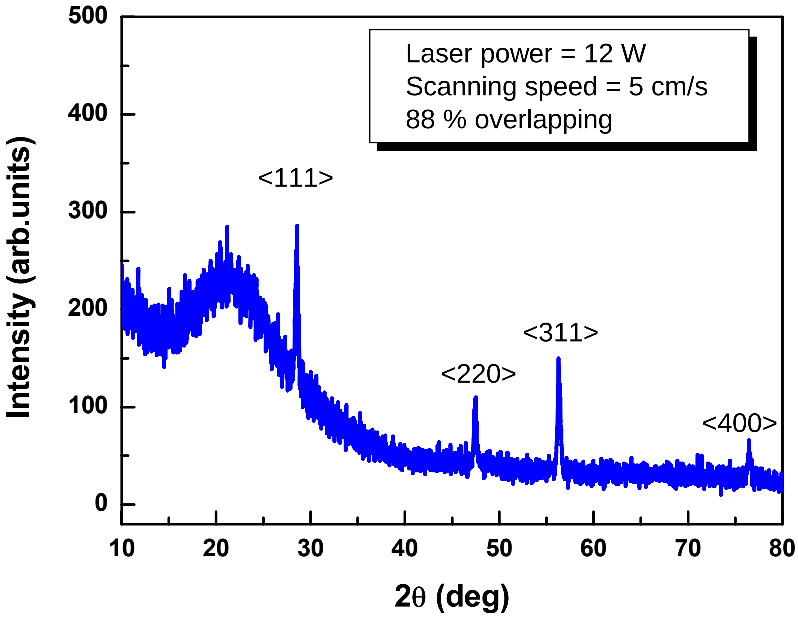


Figure 7-11. XRD spectrum of the poly-Si thin films crystallized by CW laser annealing.

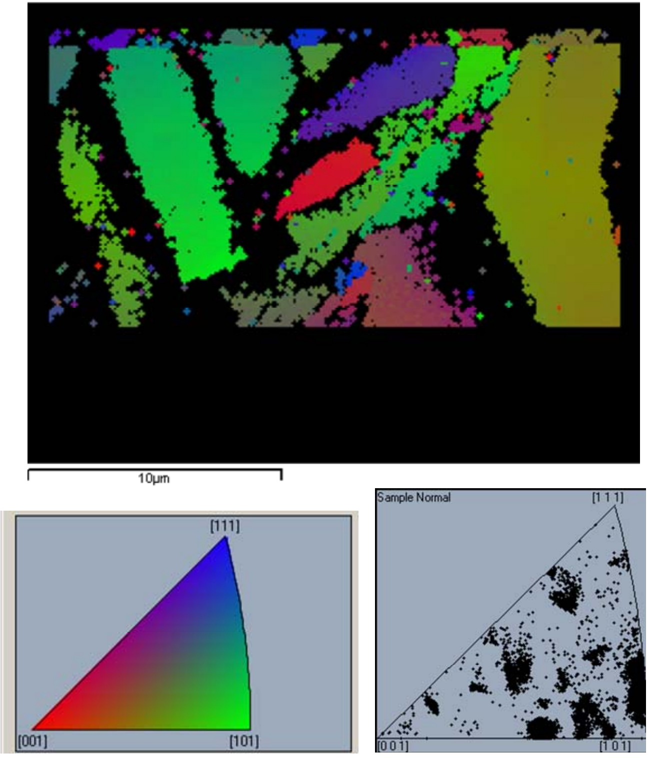
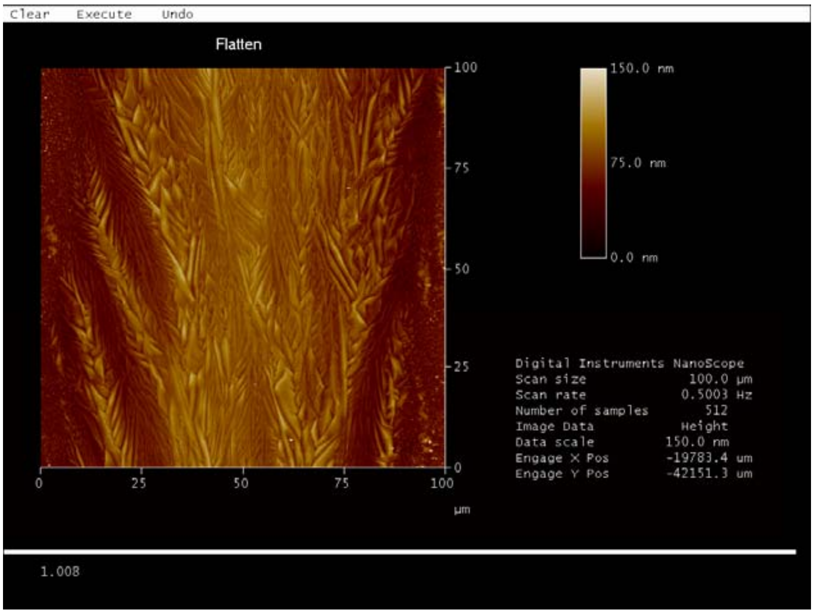
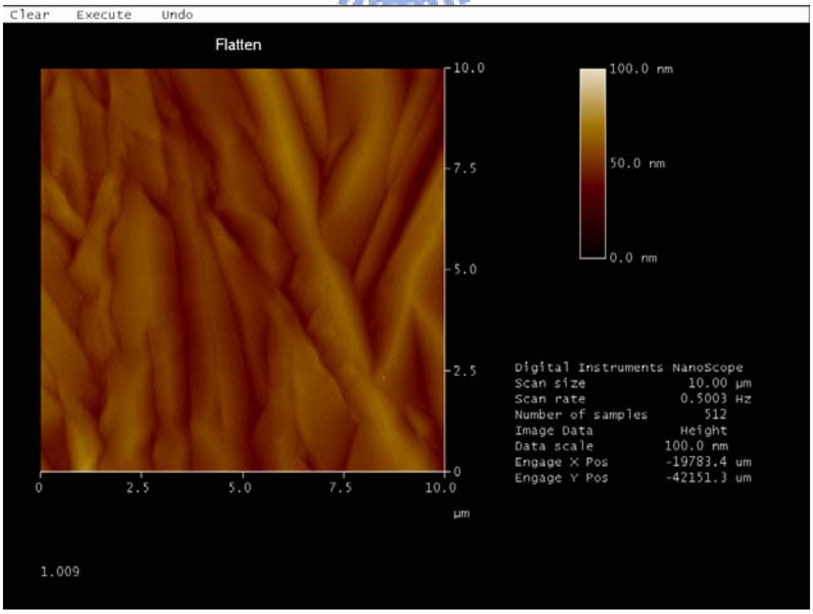


Figure 7-12. EBSD of the poly-Si sample crystallized by CW laser annealing.



```
Digital Instruments NanoScope
Scan size            100.0 µm
Scan rate           0.5003 Hz
Number of samples        512
Image Data            Height
Data scale          150.0 nm
Engage X Pos      -19783.4 um
Engage Y Pos      -42151.3 um
```

Figure 7-13(a). Atomic force microscope image of the CW laser crystallized poly-Si thin films with directional large grains.



```
Digital Instruments NanoScope
Scan size            10.00 µm
Scan rate           0.5003 Hz
Number of samples        512
Image Data            Height
Data scale          100.0 nm
Engage X Pos      -19783.4 um
Engage Y Pos      -42151.3 um
```

Figure 7-13(b). Enlarged AFM image of the CW laser crystallized poly-Si thin films with directional large grains.

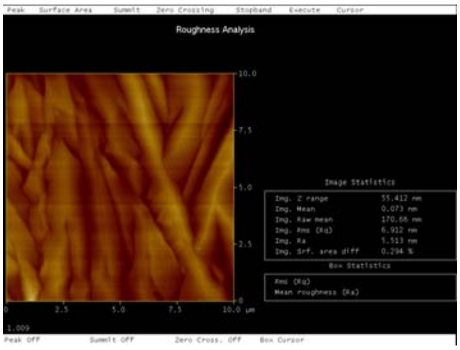
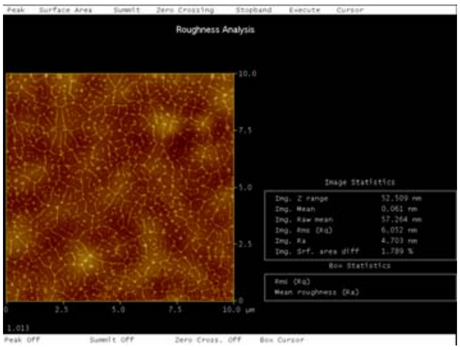
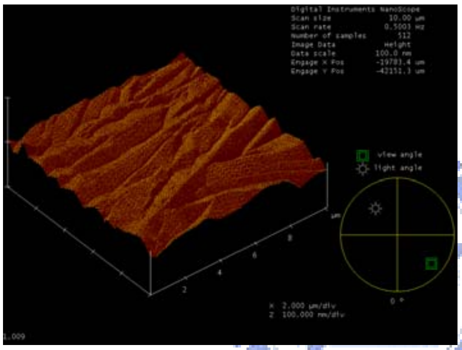
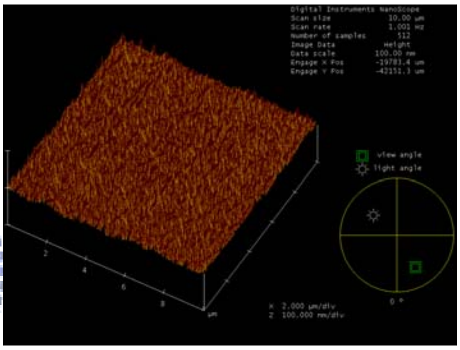
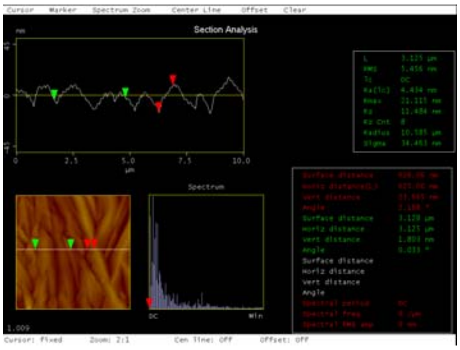
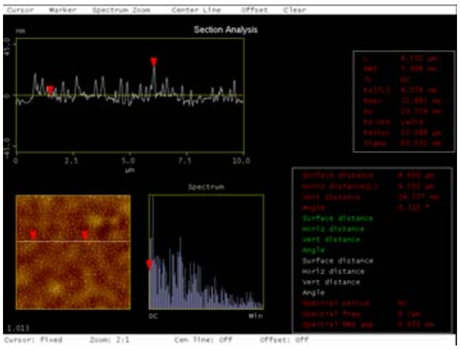
|  | **Continuous wave laser-crystallized poly-Si thin films** | **Excimer laser-crystallized poly-Si thin films** |
|---|---|---|
| **Flat image** | <br>Roughness Analysis<br>Image Statistics<br>Img. Z range 55.412 nm<br>Img. Mean 0.073 nm<br>Img. Raw mean 170.66 nm<br>Img. Rms (Rq) 6.912 nm<br>Img. Ra 5.513 nm<br>Img. Srf. area diff 0.294 %<br>Box Statistics<br>Rms (Rq)<br>Mean roughness (Ra) | <br>Roughness Analysis<br>Image Statistics<br>Img. Z range 52.509 nm<br>Img. Mean 0.061 nm<br>Img. Raw mean 57.264 nm<br>Img. Rms (Rq) 6.052 nm<br>Img. Ra 4.703 nm<br>Img. Srf. area diff 1.789 %<br>Box Statistics<br>Rms (Rq)<br>Mean roughness (Ra) |
| **3-D image** |  |  |
| **Cross-sectional image** | <br>Section Analysis | <br>Section Analysis |

Figure 7-14. Comparisons of AFM images of poly-Si grain structure and surface roughness crystallized by the DPSS CW laser crystallization and excimer laser crystallization methods, respectively.

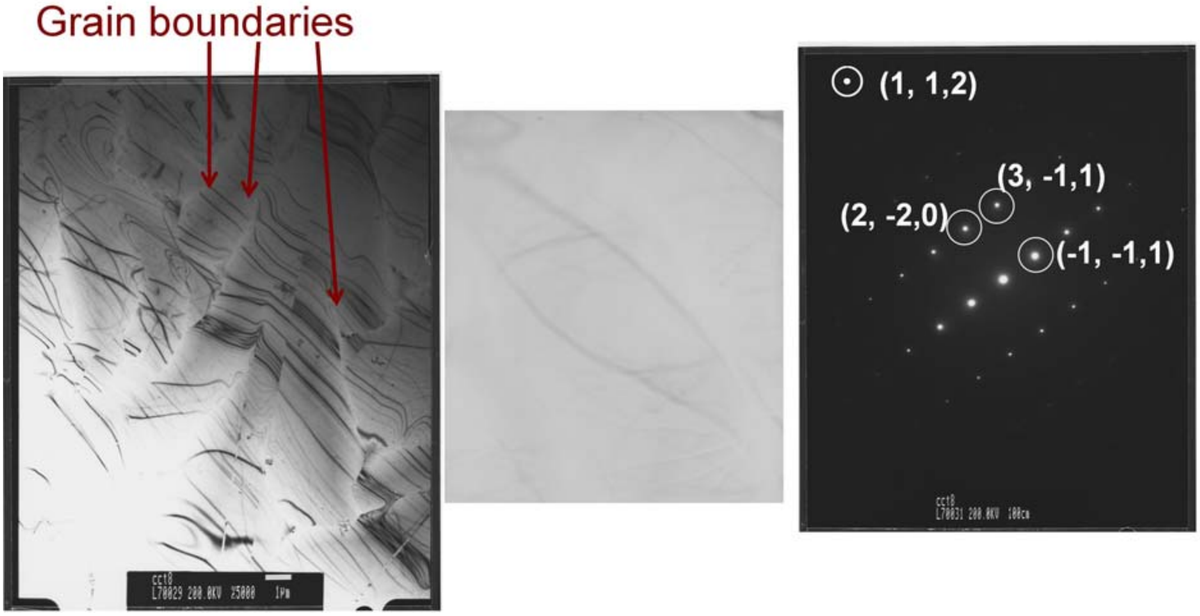


Figure 7-15. Plane-view bright-field TEM image of CW laser crystallized poly-Si thin film and its selected-area electron diffraction pattern.

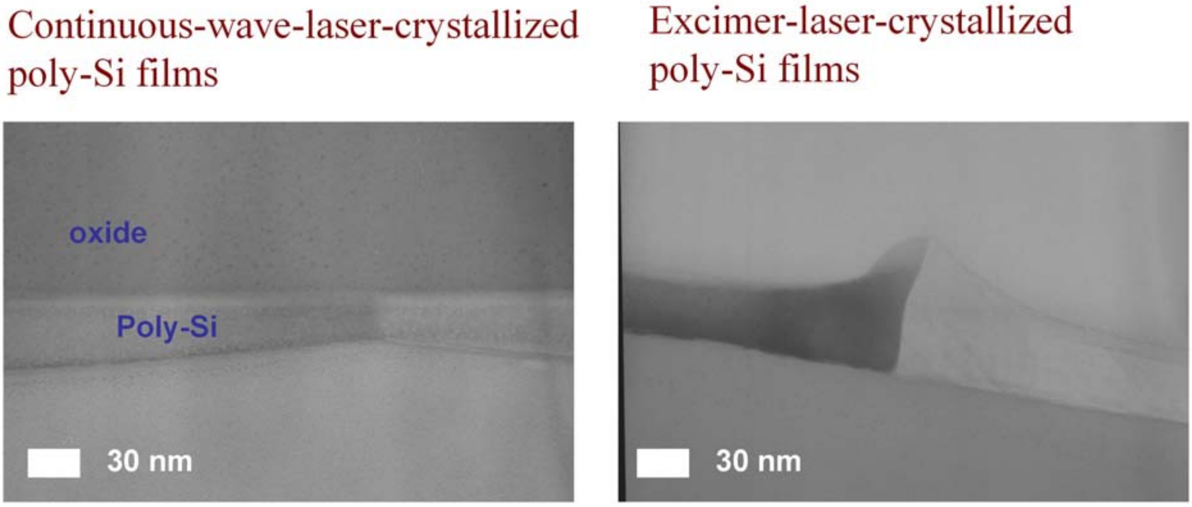


Figure 7-16. Cross-sectional TEM images of CW laser crystallized poly-Si thin film and excimer laser crystallized poly-Si thin film, respectively.

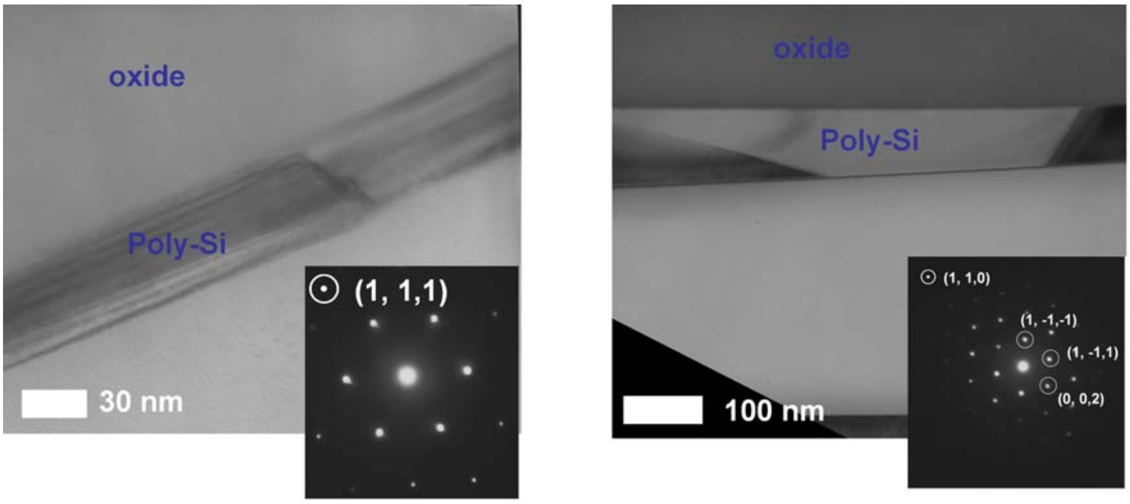


Figure 7-17. Cross-sectional TEM images of CW laser crystallized poly-Si thin films and their selected-area electron diffraction patterns.

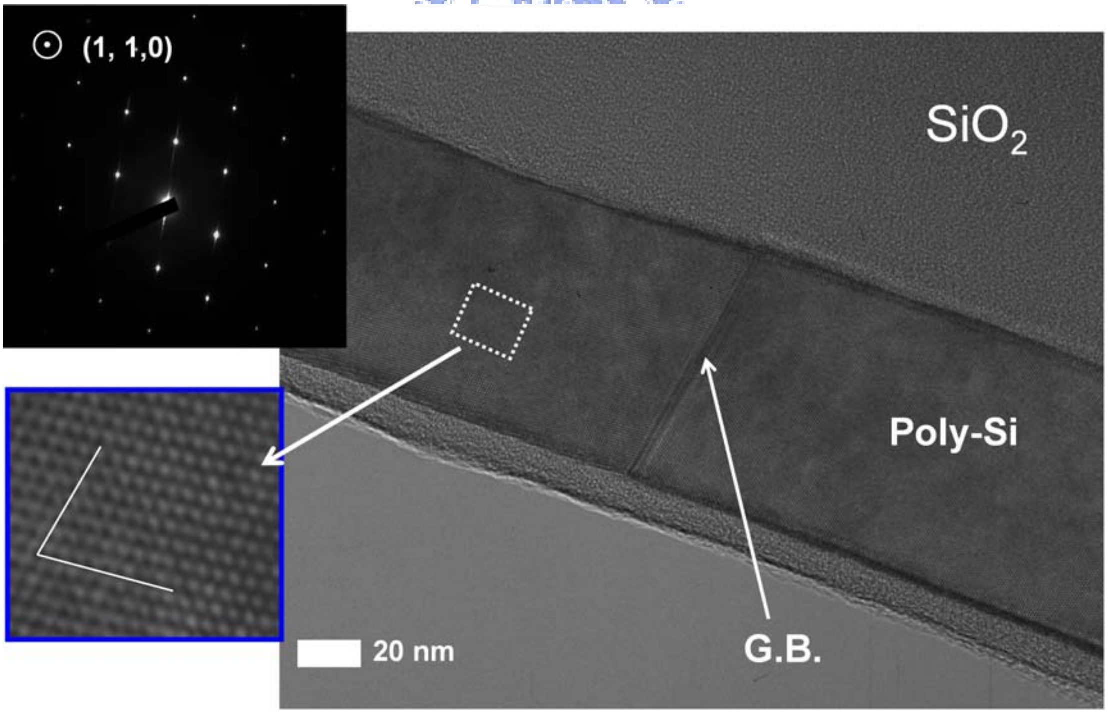


Figure 7-18. High-resolution cross-sectional TEM image and the selected-area electron diffraction pattern of the CW laser-crystallized crystallite. The diffraction pattern reveals that the crystallite exhibits <110> orientation along the direction of film grain growth.

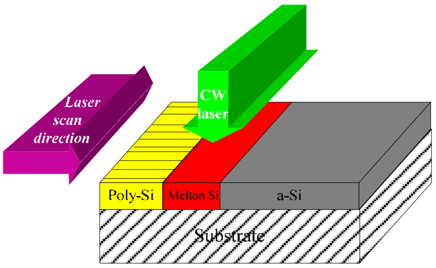
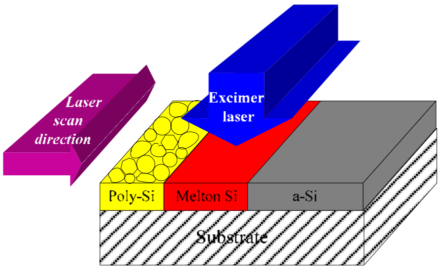
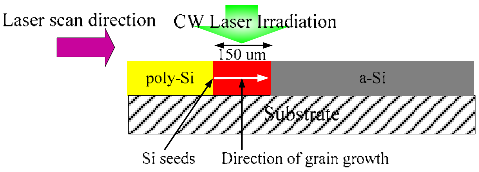
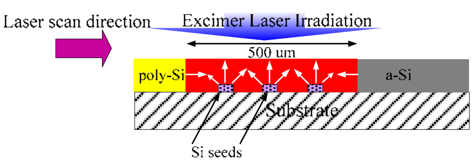
| Crystallization methods | (a) DPSS Continuous wave laser | (b) KrF Excimer laser |
|---|---|---|
| Schematically 3-D image | <br> | <br> |
| Schematically Cross-sectional image | <br> | <br> |

Figure 7-19. The crystallization mechanism of (a) continuous-wave laser lateral grain growth, and of (b) SLG regime on ELC.

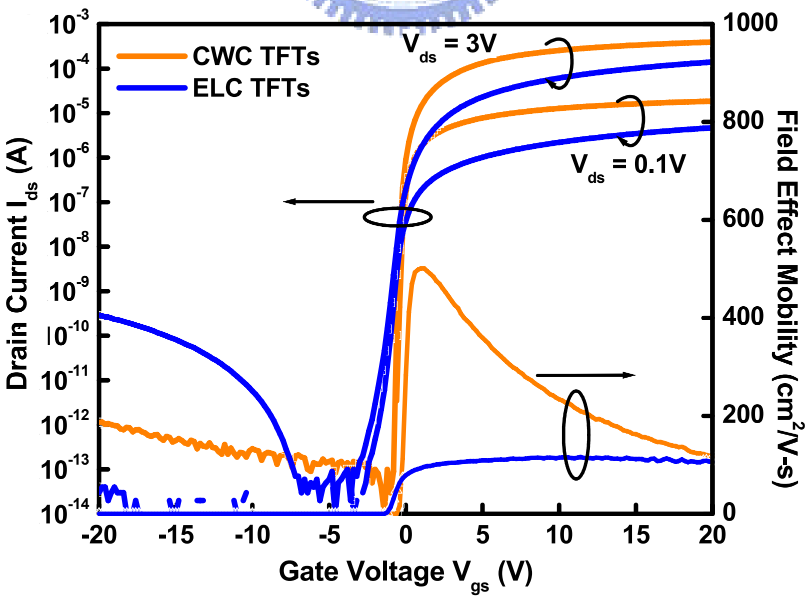


Figure 7-20(a). Comparison of transfer characteristics between the n-channel LTPS TFT crystallized by DPSS CW laser and the n-channel conventional ELC TFTs.

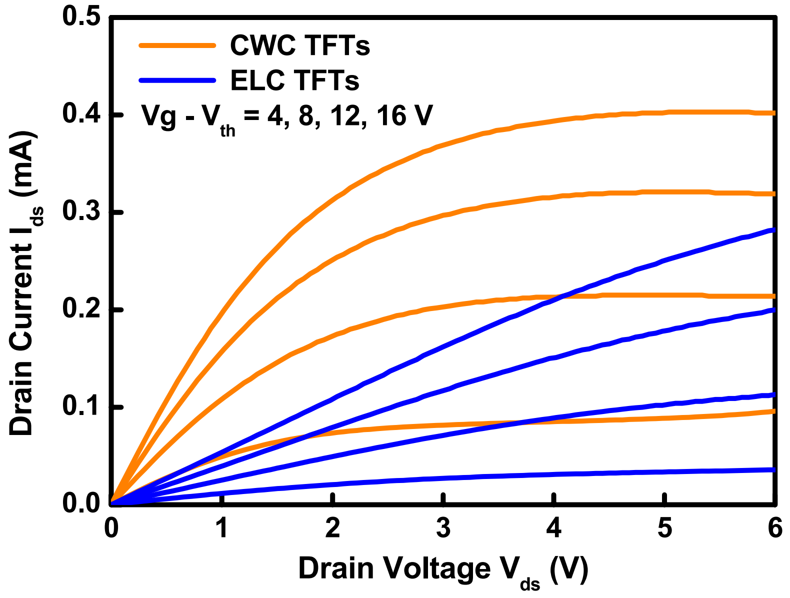


Figure 7-20(b). Comparison of output characteristics between the n-channel LTPS TFT crystallized by DPSS CW laser and the n-channel conventional ELC TFTs.

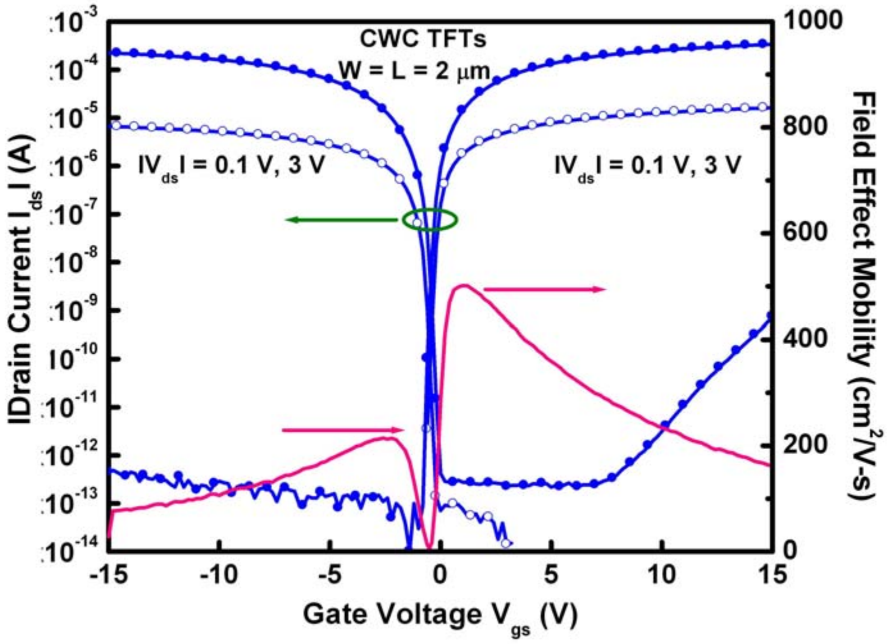


Figure 7-21(a). Transfer characteristics of n- and p-channel LTPS TFT crystallized by CW laser annealing.

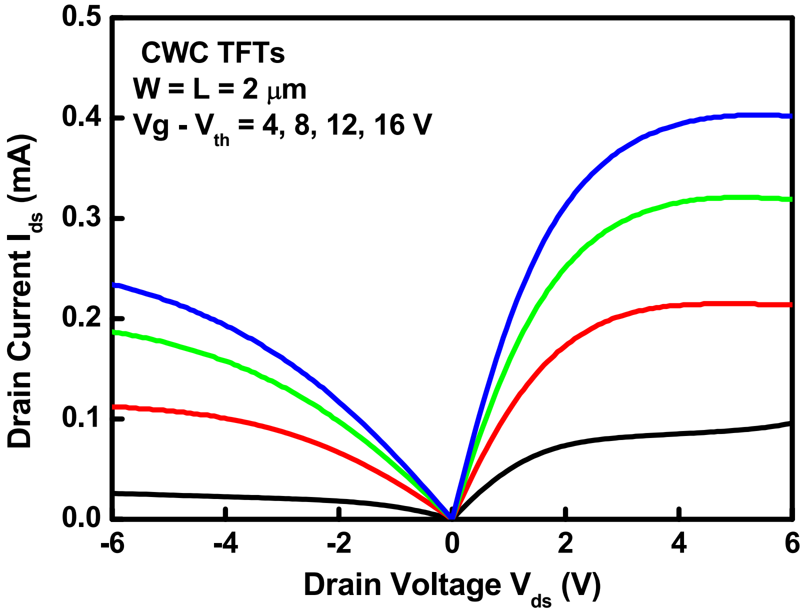


Figure 7-21(b). Output characteristics of n- and p-channel LTPS TFT crystallized by CW laser annealing.

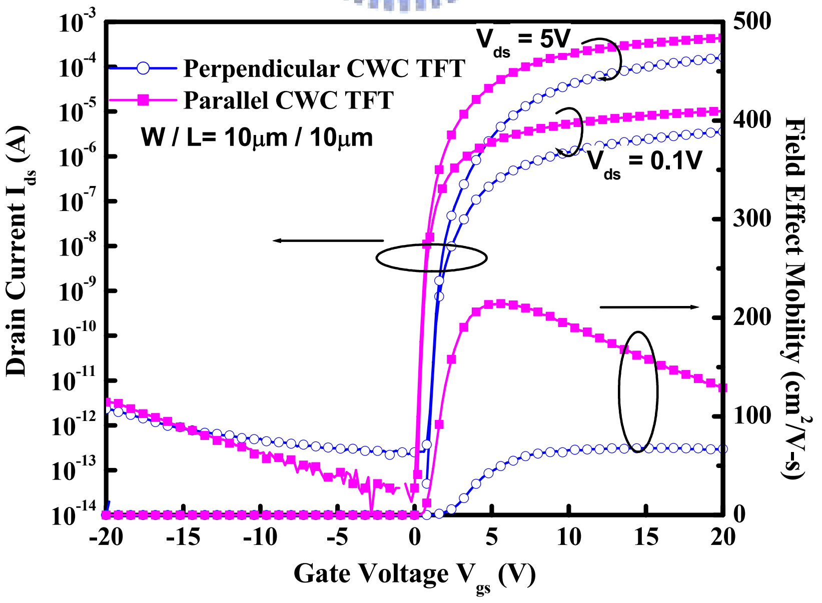


Figure 7-22(a). Transfer characteristics of n-channel LTPS TFT crystallized by CW laser with different scanning direction.

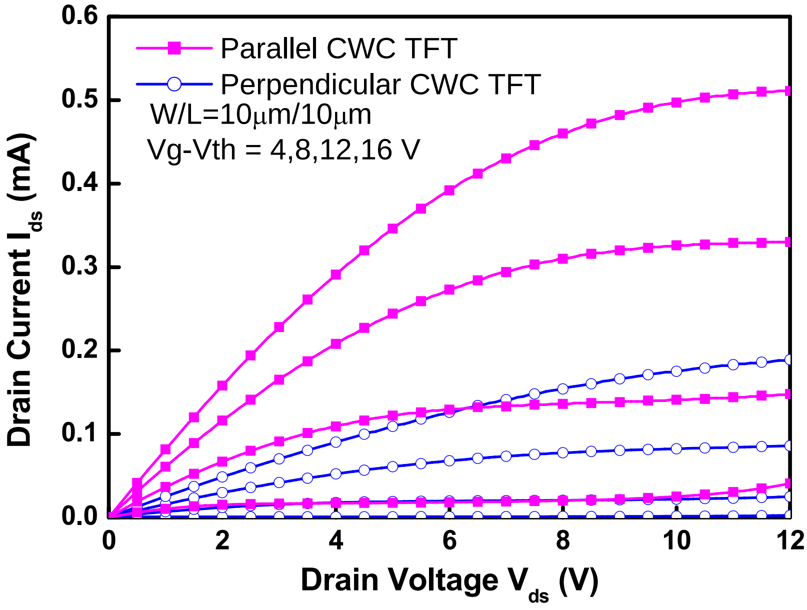


Figure 7-22(b). Output characteristics of n-channel LTPS TFT crystallized by CW laser with different scanning direction.

# Chapter 8

# Summary and Conclusions

In this thesis, various techniques, including novel excimer-laser-crystallized poly-Si thin films, advanced device structures, and diode-pumped solid-state (DPSS) continuous-wave (CW) laser annealing, are studied for the fabrication of ultra high-performance low-temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) based on the improvement of the channel material quality.

In the chapter 2, LTPS TFTs with bottom-gate (BG) structure have been demonstrated to achieve lateral grain growth using excimer laser irradiation. The mechanism of lateral grain growth using plateau structure of a-Si thin film with excimer laser crystallization is based on the spatial thermal gradient. Consequently, if the bottom-gate plateau were arranged in a proper distance, only single grain boundary perpendicular to the current flow can be artificially controlled in the channel regions, which would lead to improved device performance. The microstructure of poly-Si thin film with bottom-gate structure was analyzed by several material analyses, including SEM, AFM, TEM, and the factors that affected the final lateral crystallization microstructure were also investigated, including thickness of a-Si thin film, thickness of gate dielectric, thickness of gate electrode, laser shot number, and laser energy density. It can be observed that the large longitudinal grains artificially grown measuring about 0.85 μm were observed in length in the device channel region, while small and fine grains are located near the edges of the bottom-gate electrode. According to the TEM images, not only the interface between the poly-Si channel and bottom-gate oxide but also bottom-gate electrode and bottom-gate oxide is clear, implying that both the gate oxide and the bottom-gate electrode are not damaged during excimer laser irradiation. From the correlated selected-area diffraction pattern of poly-Si thin film, it is found that the crystallinity of the silicon grain silicon in the channel region is excellent. Moreover, the process window could be broaden because the laser energy densities, between completely melting silicon thin film in the channel but partially melting the thicker one at the corner, were easier to be controlled for the wider laser energy density range. Therefore, a wide process window and improved uniformity of TFTs performance are attained due to large silicon grains. High-performance BG LTPS-TFTs have been demonstrated with field-effect mobility exceeding 330cm$^2$/V-s, low GIDL effect, suppressed kink current and improved device uniformity due to the artificial lateral silicon grains. The process steps in these technologies are highly compatible with the conventional commercial a-Si TFTs. Moreover, the BG TFTs reveal higher breakdown voltage and better reliability due to the smooth interface between gate dielectric and poly-Si channel films as thinner gate oxide were employed without additional processes or materials. The improved breakdown and driving characteristics imply that the proposed BG-TFT structure is more suitable for device-scaled-down applications.

Although BG LTPS-TFTs exhibit superior electrical characteristics, asymmetrical electrical characteristics are also observed due to the misaligned process effect. Therefore, a self–aligned (SA) bottom-gate TFT with appropriate channel length by using the simple ELC and backside exposure has been demonstrated in the chapter 3. A self-aligned photolithography using the bottom-gate as an opaque mask is applied by backside exposure through the quartz substrate. The bottom amorphous silicon gate is thick (100 nm) enough to act as an opaque mask for the formation of the self-aligned bottom gate structure by using the back surface exposure. From the optical microscope (OM) and SEM micrographs, the photo-resist is perfectly self-aligned to the bottom-gate regions. As a result, besides all the advantages of BG LTPS-TFTs with lateral silicon grains, symmetrical electrical characteristics are also observed in SA BG LTPS-TFTs. Consequently, SA-BG TFTs with the channel length of 1 μm exhibited field-effect-mobility reaching 193 $cm^2/Vs$ without hydrogenation, while the mobility of the conventional non-SA-BG TFTs and conventional SA top-gate ones were about 17.8 $cm^2/Vs$ and 103 $cm^2/Vs$, respectively. Moreover, the SA-BG LTPS TFTs with a-Si gate thickness of 1000 Å exhibit better electrical characteristics than that of poly-Si TFTs with 1500 Å-thick gate owing to the better quality of large silicon grains in the device channel region.

In the chapter 4, novel ultra high-performance LTPS TFTs with double-gate (DG) structure and controlled lateral grain growth have been demonstrated by excimer laser crystallization. Although shrinking the device size is an effective way to improving the device performance, poor short-channel effects (SCE) is encountered owing to the insufficient gate controllability. Poly-Si TFTs suffer from worse electrical characteristics than bulk Si MOSFETs owing to the presence of numerous intra-grain and inter-grain defects in the poly silicon films. The microstructure of poly-Si films and the completed device structure were analyzed by an analytical transmission electron microscopy (TEM). Because the top and bottom gates are symmetrical, in which the gate oxide thickness is the same, and connect together electrically to obtain a perfect coupling between the surface potential in the channel region and the gate. Consequently, the influence of the source and drain depletion regions are kept minimal, which in turn reduce the short channel effects by screening the source and drain electrical field lines away from the channel. In addition, lateral silicon grains formed in the channel region as the bottom-gate TFTs is obtained, the DG devices have a higher driving current, steeper subthreshold slope, smaller drain-induced-barrier-lowering (DIBL), superior short-channel effect immunity, and suppression of the floating-body effect. The proposed DG TFTs (W/L = 1/1 μm) have the equivalent field-effect-mobility exceeding 1050 $cm^2/Vs$ for the N-channel device, 403 $cm^2/Vs$ for the P-channel device, on/off current ratio higher than $10^9$ for both structures, smaller DIBL (75mV/V) for N-channel ones, DIBL (33mV/V) for P-channel ones, and excellent device uniformity. We also compare the electrical characteristics of top gate, bottom gate and double gate devices crystallized by ELC with plateau structure in which the channel length is 1μm and P-type carrier. From the experimental results, the performances are greatly improved in the double-gate TFTs as compared with the top-gate TFTs and bottom-gate TFTs. The larger on current, higher field-effect mobility, steeper subthreshold swing and smaller DIBL reveal the enhanced gate controlling ability of double gate structure.

Although the crystallinity of poly-Si thin film can be effectively enhanced via ELC with bottom-gate structure, it is inevitable that there is a high angle grain boundary in the middle of channel region, which degrades the TFT performance and reliability. In the chapter 5, a novel and simple laser crystallization method which can remove the high angle grain boundary and produce the large and uniform grains in the desired local region is proposed to improve the field-effect mobility as well as the device uniformity. Amorphous silicon spacers played the role to let the bottom of the under-layered amorphous silicon film serve as seed crystals. Periodically lateral silicon grains with 2 μm in length can be artificially grown in the channel regions via the amorphous silicon spacer structure with excimer laser irradiation. As a result, such periodically large and lateral grains in the TFTs would achieve high field-effect mobility of 298 cm$^2$/Vs, as compared with the conventional ones of 128 cm$^2$/Vs. In addition, the uniformity of device-to-device could be improved due to this location-manipulated lateral silicon grains. Owing to the tiny width of the a-Si spacer (< 50 nm), such crystallization is also suitable for large- dimension TFTs (W = L = 10 μm). Large-dimension TFTs crystallized with the distance between adjacent a-Si spacers of 2.5 μm also exhibited the better characteristics resulting from the minimum number of longitudinal grain boundary in the channel region.

In the chapter 6, a novel crystallization technology for producing two-dimensional lateral grain growth, aiming at single-grain TFT, was demonstrated by excimer laser irradiation relying on the spatially temperature distribution at the artificially sites. The high quality silicon grains are controlled via manipulating super lateral growth phenomenon by spatially two kinds of silicon films and pre-patterned structure. The tiny a-Si spacers (< 50 nm) are served as seed crystals and form spatially different silicon thicknesses. An array of 1.8-μm-sized disklike silicon grains is formed periodically by isothermal substrate heating at 400°C during laser irradiation. Not only high-performance poly-Si TFTs with field-effect-mobility reaching 308 cm2/Vs but also excellent device uniformity are demonstrated owing to the artificially-controlled lateral grain growth. Proposed poly-Si TFTs therefore have great potential for the future SOP and 3D-ICs applications.

A new and simple diode-pumped solid-state (DPSS) continuous-wave (CW) laser crystallization is also proposed to produce lateral grain growth via controlling the laser scanning speed and laser power. As compared with excimer laser, DPSS CW laser ($\lambda = 532$ nm) exhibit superior power stability. The CW laser-crystallized poly-Si thin film was analyzed by several material analyses, including SEM, Raman, AFM, TEM, and the factors that affected the final lateral crystallization microstructure were also investigated, including, laser scanning speed, laser power, and the ambient. From the SEM and AFM analyses, CW laser lateral crystallization makes it easy to form large grains (15 μm in length) owing to the continuous energy supply and slow cooling rate of the molten Si without damage to the glass substrates. In addition, the plane-view TEM pictures and selected-area electron diffraction pattern display a directional river-like lateral Si grain growth with tens of micron and excellent crystallinity due to the clear dots, respectively. From the cross-sectional TEM picture, a flat surface morphology is formed in the grain boundary which is suitable for gate oxide scale down. According to the experimental results, ultra high-performance CW laser-crystallized LTPS TFTs have been demonstrated on the oxidized silicon wafer for the first time with field-effect mobility of 505 cm$^2$/V-s for n-channel devices and 220 cm$^2$/V-s for p-channel devices, and on/off current ratio more than $10^9$ for n-channel and p-channel devices. Besides, dopant activation by CW laser annealing is also studied. A comparison of the efficiency of dopant activation among various activation methods is studied in detail. It can be found that CW laser annealing is a low-thermal budget and high-efficiency activation method attributed to the low sheet resistance of 50 Ω/□ and uniformly redistributed dopant profiles after CW laser annealing. CW laser-annealed LTPS TFTs are, therefore, very promising for the future SOP, solar cell, and 3D-ICs applications because of the simple process.

# Chapter 9

# Future Prospects

There are some interesting and important topics that are valuable for the further research about the low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs):

The highly surface roughness of the crystallized poly-Si thin films resulting from the mass transport during laser irradiation causes the difficulty on the thinner thickness gate dielectric integration of LTPS TFTs as well as the long-term reliability of LTPS TFTs. In addition, the non-uniform thickness of silicon layer will cause the variation of TFT electrical characteristics. It has been proven that bottom-gate (BG) TFTs reveal higher breakdown voltage and better reliability than top-gate (TG) ones owing to the flat interface between gate dielectric and poly-Si channel films. Although BG structure has better immunity of gate bias stress, developing process technologies to reduce the surface roughness for TG TFTs is indispensable for further improving TFT performances when using thin gate dielectric integration and scaling down the device size of TFT. Developing surface planarization techniques and modifying the laser crystallization approach are plausible methods for the flat silicon surface.

Shrinking the device size is an effective way to improving the device performance, but poor short-channel effects (SCE) is encountered owing to the insufficient gate controllability. Ultra high-performance double-gate (DG) LTPS TFT with controlled lateral grain growth has been demonstrated by excimer laser crystallization. Because of the top gate and bottom-gate connected together as well as large silicon grains formed in the channel region, the DG devices display a higher driving current, steeper subthreshold slope, superior short-channel effect immunity, and suppression of the floating-body effect. As a result, it is as expected that if fully-depleted multi-gate and/or gate-all-around (GAA) structures were further applied to the fabrication of LTPS TFTs, ideally device with higher channel conductivity and excellent of subthreshold slope can be obtained.

Thin gate dielectric integration is another effective method to improve the device performance as well as the immunity of short-channel effects. But, the quality of deposited oxide can hardly meet the requirements for gate dielectric as thinner gate oxide is applied to LTPS TFTs. Hence, high-K gate dielectric and high-density plasma deposition and oxidation thin gate oxide dielectric may be the solutions to form high-quality gate dielectric at low temperature. And the reliability and stability of these gate dielectrics are also interesting issues and needed further study.

Although excimer laser crystallization have been shown to be the most promising candidate for LTPS TFTs in the mass production, however, the instability and short pulse duration of excimer laser put difficulty on the formation of uniform and large-grained poly-Si thin films. Solid-state CW laser may be the other alternative for LTPS TFTs due to its advantages of better laser energy stability, lower facility cost, easier maintenance, and longer melting duration. Ultra high-performance CW laser-crystallized LTPS TFTs have been fabricated. But, controlling the grain boundary location is essential to further improve the TFT performance and device-to-device uniformity.

Self–aligned (SA) bottom-gate TFT with appropriate channel length by using the simple ELC and backside exposure has been demonstrated. Such BG TFTs exhibit higher performance and better uniformity. It is as expected that this simple self-aligned process can be also applied to the fabrication of the double-gate LTPS TFTs with lateral silicon grains.

As the device dimension is comparable with the poly-Si grain size, the electrical characteristics of LTPS TFTs will be deeply influenced by the location and the number of grain boundary. Hence, if single large grain is formed in the device channel region, the resulting LTPS TFTs will exhibit uniform and excellent electrical characteristics. In this thesis, two-dimensional location-controlled grain growth has been demonstrated by excimer laser irradiation relying on spatially temperature distribution at artificially sites. However, simpler process as wall as orientation-controlled approaches are needed in the single-grain TFTs for the fabrication of mass production.

It is found that as the LTPS TFTs performance approaching to that of silicon-on-insulator (SOI) device, self-heating effect becomes serious owing to the poor thermal conductivity of the insulating glass substrates. As a result, some novel device structures and approaches are required to dissipate the heat generating during the device operation in the future LTPS TFTs.

As the LTPS TFTs are used for active-matrix organic light-emitting displays (AMOLEDs), it is always required to adopt new driving pixie circuits of AMOLEDs to compensate the variation of the LTPS TFT performance. Since our proposed LTPS TFTs exhibit both high-performance and good uniformity, it is worthy of further study in the device application in the AMOLEDs.

# References

## Chapter 1

[1.1] C. T. Liu, **“**Revolution of the TFT LCD Technology,” *IEEE/OSA J. Display Technology.*, vol. 3, pp. 342-350, 2007.

[1.2] Li Yulin, Yun Zhisheng, He Zhengquan, Liu Jifmg, and Zheng Genxiang, ” Liquid Crystal Light Valve Color Projection System,” in *ASID Tech. Dig.*, 1997, pp. 133-135.

[1.3] A. Nathan, A. Kumar, K. Sakariya, P. Servati, S. Sambandan, and D. Striakhilev, ” Amorphous silicon thin film transistor circuit integration for organic LED displays on glass and plastic,” *IEEE J. Solid-State Circuits.*, vol. 39, pp.1477 – 1486, 2004.

[1.4] A. Kohno, T. Sameshima, N. Sano, M. Sekiya, and M. Hara, “High performance poly-Si TFTs fabricated using pulsed laser annealing and remote plasma CVD with low temperature processing,” *IEEE Trans. Electron Devices*, vol. 42, pp. 251- 257, 1995.

[1.5] Z. Meng; M. Wang; and M. Wong,” High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film transistors for system-on-panel applications**,”** *IEEE Trans. Electron Devices*, vol. 47, pp. 404-409, 2000.

[1.6] M. Takabatake, J. Ohwada, Y. A. Ono, K. Ono, A. Mimura, N. Konishi, “CMOS circuits for peripheral circuit integrated poly-Si TFT LCD fabricated at low temperature below 600 degrees C,” *IEEE Trans. Electron Devices*, vol. 38, pp. 1303-1309, 1991.

[1.7] I-W. Wu, “Cell design considerations for high-aperture-ratio direct-view and projection polysilicon TFT-LCDs,” in *SID Tech. Dig.*, 1995, pp. 19-22.

[1.8] J. W Lee, N. I. Lee, H. J. Chung, and C. H. Han,” Improved stability of polysilicon thin-film transistors under self-heating and high endurance EEPROM cells for systems-on-panel,” in *IEDM Tech. Dig.*, 1998, pp. 265-268.

[1.9] Y. Matsueda, S. Inoue, and T. Shimoda, "Concept of system on panel," in *AMLCD Tech. Dig.*, 2001, pp. 77-80.

[1.10] T. Nishibe and H. Nakamura, "Value-Added Circuit and Function Integration for SOG (System-on Glass) Based on LTPS Technology," in *SID Tech. Dig.*, 2006, pp. 1091-1094.

[1.11] Y. Yamamoto, T. Matsuo, and H. Komiya, "CG Silicon Technology and System Integration for Mobile Applications," in *SID Tech. Dig.*, 2006, pp. 1173-1176.

[1.12] Y. Nakajima, Y. Teranishi, Y. Kida, and Y Maki, "Ultra-Low-Power LTPS TFT-LCD Technology Using a Multi-Bit Pixel Memory Circuit," in *SID Tech. Dig.*, 2006, pp. 1185-1188.

[1.13] M. Miyasaka, "Suftla Flexible Microelectronics on Their Way to Business," in *SID Tech. Dig.*, 2007, pp. 1673-1676.

[1.14] C. D Kim, I. B Kang, and I. J Chung "TFT Technology for Flexible Displays," in *SID Tech. Dig.*, 2007, pp. 1669-1672.

[1.15] Y. Kuo, **"**TFT and ULSIC - Competition or Collaboration," in *AMFPD Tech. Dig.*, 2007, pp. 1-4.

[1.16] V. W. C. Chan, Philip C. H. Chan, M. Chan," Three dimensional CMOS integrated circuits on large grain polysilicon films," in *IEDM Tech. Dig.,* 2000, pp. 161-164.

[1.17] Nobuo Karaki, Takashi Nanmoto, Hiroaki Ebihara, Satoshi Inoue, Tatsuya Shimoda, "A Flexible 8-bit Asynchronous Microprocessor Based on Low-Temperature Poly-Silicon (LTPS) TFT Technology," in *SID Tech. Dig.*, 2005, pp. 1430-1433.

[1.18] H. Wang, M. Chan, S. Jagar, Y. Wang, and P. K. Ko, "Submicron super TFTs for 3-D VLSI applications," *IEEE Electron Device Lett.*, vol. 21, pp. 439-441, 2000.

[1.19] Victor W. C. Chan, Philip C. H. Chan, and Mansun Chan, "Three-dimensional CMOS SOI integrated circuit using high-temperature metal-induced lateral crystallization," *IEEE Trans. Electron Devices*, vol. 48, pp. 1394-1399, 2001.

[1.20] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, “3-D ICs: a novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration,” *Proceedings of the IEEE*, vol. 89, pp. 602-633, 2001.

[1.21] Robert S. Sposili and James S. Im, “Sequential lateral solidification of thin silicon films on $SiO_2$,” *Appl. Phys. Lett.*, vol. 69, pp. 2864-2866, 1996.

[1.22] Paul Ch. Van der Wilt, Ryoichi Ishihara, and Jurgen Bertens, “Location-controlled large-grains in near-ablation excimer-laser crystallized silicon films,” *Mat. Res. Soc. Symp. Proc.*, vol. 621, Q7.4.1-Q7.4.6, 2000.

[1.23] Chang-Ho Oh, Motohiro Ozawa, and Masakiyo Matsumura, “A novel phase-modulated excimer-laser crystallization method of silicon thin films,” *Jpn. J. Appl. Phys. Part 2*, vol. 37, pp. L492-L495, 1998.

[1.24] H. J. Kim and James S. Im, “New excimer-laser-crystallization method for producing large-grained and grain boundary-location-controlled Si films for thin film transistors,” *Appl. Phys. Lett.*, vol. 68, pp. 1513-1515, 1996.

[1.25] P. M. Smith, P. G. Carey, and T. W. Sigmon, “Excimer laser crystallization and doping of silicon films on plastic substrates,” *Appl. Phys. Lett.*, vol. 70, pp. 342-344, 1997.

[1.26] S. D. Brotherton, D. J. McCulloch, J. P. Gowers, J. R. Ayres, C. A. Fisher, and F. W. Rohlfing, “Excimer laser crystallization of poly-Si TFTs for AMLCDs,” *Mat. Res. Soc. Symp. Proc.*, vol. 621, pp. Q7.1.1 - Q7.1.12, 2000.

[1.27] S. W. Lee, Y. C. Jeon, and S. K. Joo, “Pd induced lateral crystallization of amorphous Si thin films,” *Appl. Phys. Lett.*, vol. 66, pp.1671-1673, 1995.

[1.28] Zhonghe Jin, Gururaj A. Bhat, Milton Yeung, Hoi S. Kwok, and Man Wong, “Nickel induced crystallization of amorphous silicon thin films,” *J. Appl. Phys.*, vol. 84, pp. 194-200, 1998.

[1.29] Z. Jin, K. Moulding, H. S. Kwok, and M. Wong, “The effects of extended heat treatment on Ni induced lateral crystallization of amorphous silicon thin films,” *IEEE*

*Trans. Electron Devices*, vol. 46, pp. 78-82, 1999.

[1.30] Atsushi Kohno, Toshiyuki Sameshima, Naoki Sano, Mitsunobu Sekiya, and Masaki Hara, “High performance poly-Si TFTs fabricated using pulsed laser annealing and remote plasma CVD with low temperature processing,” *IEEE Trans. Electron Devices*, vol. 42, pp. 251- 257, 1995.

[1.31] J. Y. Lee, C. H. Han, and C. K. Kim,” ECR plasma oxidation effects on performance and stability of polysilicon thin film transistors,” in *IEDM Tech. Dig.,* 1994, pp. 523-526.

[1.32] J. W. Lee, N. I. Lee, and C. H. Han,” Stability of short-channel p-channel polysilicon thin-film transistors with ECR N2O-plasma gate oxide,” *IEEE Electron Device Lett.*, vol. 20, pp. 12-14, 1999.

[1.33] J. W. Lee, N. I. Lee, and C. H. Han,” Characteristics of polysilicon thin-film transistor with thin-gate dielectric grown by electron cyclone resonance nitrous oxide plasma,” *IEEE Electron Device Lett.*, vol. 18, pp.172-174, 1997.

[1.34] K. Sekine, Y. Saito, M. Hirayama, and T. Ohmi,” Highly reliable untrathin silicon oxide film formation at low temperature by oxygen radical generated in high-density krypton plasma,” *IEEE Trans. Electron Device*, vol. 48, pp.1550-1555, 2001.

[1.35] K. Tanaka, H. Arai, and S. Kohda, “Characteristics of offset-structure polycrystalline-silicon thin-film transistors,” *IEEE Electron Device Lett.*, vol. 9, pp. 23-25, 1988.

[1.36] B. H. Min, C. M. Park, and M. K. Han, “A novel offset gated polysilicon thin film transistor without an additional offset mask,” *IEEE Electron Device Lett.*, vol. 16, pp. 161-163, 1995.

[1.37] Byung-Hyuk Min and Jerzy Kanicki, “Electrical characteristics of new LDD poly-Si TFT structure tolerant to process misalignment,” *IEEE Electron Device Lett.*, vol. 20, pp. 335-337, 1999.

[1.38] Shengdong Zhang, Ruqi Han, and Mansun J. Chan, “A novel self-aligned bottom gate poly-Si TFT with in-situ LDD," *IEEE Electron Device Lett.*, vol. 22, pp. 393-395, 2001.

[1.39] Y. Uemoto, E. Fujii, F. Emoto, A. Nakamura, K. Senda, "A high-voltage polysilicon TFT with multigate structures," *IEEE Trans. Electron Devices*, vol. 38, pp. 95-100, 1991.

[1.40] Yasuyoshi Mishima and Yoshiki Ebiko, "Improved lifetime of poly-Si TFTs with a self-aligned gate-overlapped LDD structure," *IEEE Trans. Electron Devices*, vol. 49, pp. 981-985, 2002.

[1.41] M. Hatano, H. Akimoto, and T. Sakai, "A novel self-aligned gate-overlapped LDD poly-Si TFT with high reliability and performance," in *IEDM Tech. Dig.*, 1997, pp. 523-526.

[1.42] Kwon-Young Choi, Jong-Wook Lee, and Min-Koo Han, "Gate-overlapped lightly doped drain poly-Si thin-film transistors for large area-AMLCD," *IEEE Trans. Electron Devices*, vol. 45, pp. 1272-1279, 1998.

[1.43] T. Y. Huang, I. W. Wu, A. G. Lewis, A. Chiang, and R. H. Bruce, "A simpler 100-V polysilicon TFT with improved turn-on characteristics," *IEEE Electron Device Lett.*, vol. 11, pp. 244-246, 1990.

[1.44] K. Tanaka, N. Nakazawa, S. Suyama, and K. Kato, "Field-induction-drain (FID) poly-Si TFT with high on/off current ratio," in *Extend Abstract of SSDM*, 1990, pp.1011.

[1.45] N. Lifshitz, S. Luryi, M. R. Pinto, and C. S. Rafferty, "Active gate thin-film transistor," *IEEE Electron Device Lett.*, vol. 14, pp. 394-395, 1993.

[1.46] B. H. Min, C. M. Park, and M. K. Han, "A novel polysilicon thin-film transistor with a p-n-p structured gate electrode," *IEEE Electron Device Lett.*, vol. 17, pp. 560-562, 1996.

[1.47] Shengdong Zhang, Chunxiang Zhu, Johnny K. O. Sin, J. N. Li, and Philip K. T. Mok, "Ultra-thin elevated channel poly-Si TFT technology for fully-integrated AMLCD system on glass," *IEEE Trans. Electron Devices*, vol. 47, pp. 569-575, 2000.

[1.48] Shengdong Zhang, Chunxiang Zhu, Johnny K. O. Sin, and Philip K. T. Mok, "A novel ultrathin elevated channel low-temperature poly-Si TFT," *IEEE Electron Device Lett.*, vol. 20, pp. 569-571, 1999.

[1.49] J. S. Yoo, C. H. Kim, M. C. Lee, M. K. Han, H. J. Kim, "Reliability of low temperature poly-Si TFT employing counter-doped lateral body terminal," in *IEDM Tech. Dig.*, 2000, pp. 217-220.

[1.50] S. Uchikoga and N. Ibaraki, "Low temperature poly-Si TFT-LCD by excimer laser anneal," *Thin Solid Films*, vol. 383, pp. 19-24, 2001.

[1.51] T. Sameshima, "Status of Si thin film transistors," *J. Non-Cryst. Solids*, vol. 227-230, pp. 1196-1201, 1998.

[1.52] Alan G. Lewis, I-Wei Wu, Tiao Y. Huang, Mitsu Koyanagi, Anne Chiang and Richard H. Bruce, "Small geometry effects in n- and p-channel polysilicon thin film transistors," in *IEDM Tech. Dig.*, 1988, pp. 260-263.

[1.53] Alan G. Lewis, Tiao Y. Huang, I-Wei Wu, Richard H. Bruce and Anne Chiang, "Physical mechanisms for short channel effects in polysilicon thin film transistors," in *IEDM Tech. Dig.*, 1989, pp. 349-352.

[1.54] M. Valdinoci, L. Colalongo, G. Baccarani, G. Fortunato, A. Pecora, and I. Policicchio, "Floating body effects in polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 44, pp. 2234-2241, 1997.

[1.55] M. Hack, and A. G. Lewis, "Avalanche-induced effects in polysilicon thin-film transistors," *IEEE Electron Device Lett.*, vol. 12, pp. 203-205, 1991.

[1.56] G. Fortunato and P. Migliorato, "Determination of gap state density in polycrystalline silicon by field-effect conductance," *Appl. Phys. Lett.*, vol. 49, p. 1025, 1986.

[1.57] I. W. Wu, T. Y. Huang, W. B. Jackson, A. G. Lewis, and A. Chiang, "Passivation kinetics of two types of defects in polysilicon TFT by plasma hydrogenation," *IEEE Electron Device Lett.*, vol. 12, p. 181, 1991.

[1.58] M. Cao, T. Zhao, K. C. Saraswat, and J. D. Plummer, "Study on hydrogenation of polysilicon thin film transistors by ion implantation," *IEEE Trans. Electron Devices*, vol. 42, p. 1134, 1995.

[1.59] H. C. Cheng, F. S. Wang, and C. Y. Huang, "Effects of NH3 plasma passivation on n-channel polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 44, p. 64, 1997.

[1.60] J. D. Bernstein, S. Qin, C. Chan, and T. J. King, "High dose-rate hydrogen passivation of polycrystalline silicon CMOS TFT's by plasma ion implantation," *IEEE Trans. Electron Devices*, vol. 43, p. 1876, 1996.

[1.61] M. K. Hatalis and D. W. Greve, "High-performance thin film transistors in low temperature crystallized LPCVD amorphous silicon films," *IEEE Electron Device Lett.*, vol. 8, p. 361, 1987.

[1.62] E. Scheid, B. De Maauduit, P. Taurines and D. Bielle-Daspet, "Super large grain polycrystalline silicon obtained from pyrolysis of Si2H6 and annealing," *Jpn. J. Appl. Phys.* Part2, vol. 29, p. L2105, 1990.

[1.63] K. Nakazawa, "Recrystallization of amorphous silicon films deposited by low-pressure chemical vapor deposition from Si2H6 gas," *J. Appl. Phys.*, vol. 69, p. 1703, 1991.

[1.64] C. W. Lin, L. J. Cheng, Y. L. Lu, Y. S. Lee, and H. C. Cheng, "High-performance low-temperature poly-Si TFTs crystallized by excimer laser irradiation with recessed-channel structure," *IEEE Electron Device Lett.*, vol. 22, p. 269, 2001.

[1.65] I-Wei Wu, Warren. B. Jackson , Tiao-Yuan Huang, Alan G. Lewis, and Anne Chiang, "Mechanism of device degradation in n- and p-channel polysilicon TFT's by electrical stressing," *IEEE Electron Device Lett.*, vol. 11, p. 167, 1990.

[1.66] Michael Hack, Alan G. Lewis, and I-Wei Wu, "Physical models for degradation effects in polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 40, p. 890, 1993.

[1.67] A. Mimura, N. Konishi, K. Ono, J. Ohwada, Y. Hosokawa, Y. Ono, T. Suzuki, K.

Miyata, and H. Kawakami, “High performance low-temperature poly-Si n-channel TFTs for LCD,” *IEEE Trans. Electron Devices*, vol. 36, pp. 351-359, 1989.

[1.68] Miltiadis K. Hatalis and David W. Greve, “Large grain polycrystalline silicon by low-temperature annealing of low-pressure chemical vapor deposited amorphous silicon films,” *J. Appl. Phys.*, vol. 63, pp. 2260-2266, 1988.

[1.69] K. Pangal, J. C. Sturm, S. Wagner, and T. H. Buyuklimanli, “Hydrogen plasma enhanced crystallization of hydrogenated amorphous silicon films,” *J. Appl. Phys.*, vol. 85, pp. 1900-1906, 1999.

[1.70] R. B. Iverson and R. Reif,” Recrystallization of amorphized polycrystalline silicon films on $SiO_2$: Temperature dependence of the crystallization parameters,” *J. Appl. Phys.*, vol. 62, pp. 1675-1681, 1987.

[1.71] I. W. Wu, A. Chiang, M. Fuse, L. Ovecoglu, and T. Y. Huang,” Retardation of nucleation rate for grain size enhancement by deep silicon ion implantation of low-pressure chemical vapor deposited amorphous silicon films,” *J. Appl. Phys.*, vol. 65, pp. 4036-4039, 1987.

[1.72] C. Spinella, S. Lombardo, and S. U. Campisano,” Early stages of grain growth in ion-irradiated amorphous silicon,” *Phys. Rev. Lett.*, Vol. 66, pp. 1102-1105, 1991.

[1.73] E. Scheid, B. De Maauduit, P. Taurines and D. Bielle-Daspet, “Super large grain polycrystalline silicon obtained from pyrolysis of $Si_2H_6$ and annealing,” *Jpn. J. Appl. Phys. Part2*, vol. 29, pp. L2105-2107, 1990.

[1.74] K. Nakazawa, “Recrystallization of amorphous silicon films deposited by low-pressure chemical vapor deposition from $Si_2H_6$ gas,” *J. Appl. Phys.*, vol. 69, pp. 1703-1706, 1991.

[1.75] S. Hasegawa, S. Sakamoto, T. Inokuma and Y. Kurata, “Structure of recrystallized silicon films prepared from amorphous silicon deposited using disilane,” *Appl. Phys. Lett.*, vol. 62, pp. 871-877, 1993.

[1.76] G. Radnoczi, A. Robertsson, H. T. G. Hentzell, S. F. Gong, and M. A. Hasan, "Al induced crystallization of a-Si," *J. Appl. Phys.*, vol. 69, pp. 6394-6399, 1991.

[1.77] L. Hultman, A. Robertsson, H. T. G. Hentzell, I. Engström, and P. A. Psaras, "Crystallization of amorphous silicon during thin-film gold reaction," *J. Appl. Phys.*, vol. 62, pp. 3647-3655, 1987.

[1.78] Soo Young Yoon, Ki Hyung, Chae Ok Kim, Jae Young Oh, and Jin Jang, "Low temperature metal induced crystallization of amorphous silicon using a Ni solution," *J. Appl. Phys.*, vol. 82, pp. 5865-5867, 1997.

[1.79] Seok-Woon Lee, Yoo-Chan Jeon, and Seung-Ki Joo, "Pd induced lateral crystallization of amorphous Si thin films," *Appl. Phys. Lett.*, vol. 66, pp.1671-1673, 1995.

[1.80] Zhonghe Jin, Gururaj A. Bhat, Milton Yeung, Hoi S. Kwok, and Man Wong, "Nickel I nduced crystallization of amorphous silicon thin films," *J. Appl. Phys.*, vol. 84, pp. 194-200, 1998.

[1.81] Zhonghe Jin, Keith Moulding, Hoi S. Kwok, and Man Wong, "The effects of extended heat treatment on Ni induced lateral crystallization of amorphous silicon thin films," *IEEE Trans. Electron Devices*, vol. 46, pp. 78-82, 1999.

[1.82] Seok-Woon Lee and Seung-Ki Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization," *IEEE Electron Device Lett.*, vol. 17, pp. 160-162, 1996.

[1.83] C. Hayzelden and J. L. Batstone, "Silicide formation and silicide-mediated crystallization of nickel-implanted amorphous silicon thin films," *J. Appl. Phys.*, vol. 73, pp. 8279-8289, 1993.

[1.84] Jin Jang, Jae Young Oh, Sung Ki Kim, Young Jin Choi, Soo Young Yoon, and Chae Ok Kim, " Electric-field-enhanced crystallization of amorphous silicon," *Nature*, vol. 395, pp. 481-483, 1998.

[1.85] Sang-Hyun Park, Peung-Ik Jun, Kyung-Sub Song, Chang-Kyung Kim, and Duck-Kyun

Choi, “Field aided lateral crystallization of amorphous silicon thin film,” *Jpn. J. Appl. Phys. Part2*, vol. 38, pp. L108-L109, 1999.

[1.86] Won Kyu Kwak, Bong Rae Cho, Soo Young Yoon, Seong Jin Park, and Jin Jang, “A high performance thin-film transistor using a low temperature poly-Si by silicide mediated crystallization,” *IEEE Electron Device Lett.*, vol. 21, pp. 107-109, 2000.

[1.87] Soo Young Yoon, Jae Young Oh, Chae Ok Kim, and Jin Jang, “Low temperature solid phase crystallization of amorphous silicon at 380°C,” *J. Appl. Phys.*, vol. 84, pp. 6463-6465, 1998.

[1.88] J. E. Palmer, C. V. Thompson, and H. I. Smith,” Grain growth and grain size distribution in thin germanium films,” *J. Appl. Phys*, vol. 62, pp. 2492-2497, 1987.

[1.89] Soo Young Yoon, Ki Hyung, Chae Ok Kim, Jae Young Oh, and Jin Jang, “Low temperature metal induced crystallization of amorphous silicon using a Ni solution,” *J. Appl. Phys.*, vol. 82, pp. 5865-5867, 1997.

[1.90] Soo Young Yoon, Seong Jin Park, Kyung Ho Kim, and Jin Jang, “Structural and electrical properties of polycrystalline silicon produced by low-temperature Ni silicide mediated crystallization of the amorphous phase,” *J. Appl. Phys.*, vol. 87, pp. 609-611, 2000.

[1.91] G. K. Celler, H. J. Leamy, L. E. Trimble, and T. T. Sheng, “Annular grain structures in pulsed laser recrystallized Si on amorphous insulators,” *Appl. Phys. Lett.*, vol. 39, pp. 425-427, 1981.

[1.92] N. M. Johnson, D. K. Biegelsen, H. C. Tuan, M. D. Moyer, and L. E. Fennell, “Single-crystal silicon transistors in laser-crystallized thin films on bulk glass,” *IEEE Electron Device Lett.*, vol. 3, pp. 369-372, 1982.

[1.93] G. J. Willems, J. J. Poortmans, and H. E. Maes “A semiempirical model for the laser-induced molten zone in the laser recrystallization process,” *J. Appl. Phys.*, vol. 62, pp. 3408-3415, 1987.

[1.94] H. W. Lam, R. F. Pinizzotto, and A. F. Tasch, Jr, “Single Crystal Silicon-on-Oxide by a Scanning CW Laser Induced Lateral Seeding Process,” *J. Electrochem. Soc.* vol. 128, pp. 1981-1986, 1981.

[1.95] J. P. Colinge, E. Demoulin, D. Bensahel, and G. Auvert, “Use of selective annealing for growing very large grain silicon on insulator films,” *Appl. Phys. Lett.*, vol. 41, pp. 346-347, 1982.

[1.96] K. Sera, F. Okumura, H. Uchida, S. Itoh, S. Kaneko, and K. Hotta, “High-performance TFTs fabricated by XeCl excimer laser annealing of hydrogenated amorphous-silicon film,” *IEEE Trans. Electron Devices*, vol. 36, pp. 2868-2872, 1989.

[1.97] T. Sameshima, S. Usui, and M. Sekiya, “XeCl Excimer laser annealing used in the fabrication of poly-Si TFT's,” *IEEE Electron Device Lett.*, vol. 7, pp. 276-278, 1986.

[1.98] Y. F. Tang, S. R. P. Silva, and M. J. Rose, “Super sequential lateral growth of Nd:YAG laser crystallized hydrogenated amorphous silicon,” *Appl. Phys. Lett.*, vol. 78, pp. 186-188, 2001.

[1.99] Akito Hara, Fumiyo Takeuchi, Michiko Takei, Katsuyuki Suga, Kenichi Yoshino, Mitsuru Chida, Yasuyuki Sano, and Nobuo Sasaki, “High-performance polycrystalline silicon thin film transistors on non-alkali glass produced using continuous wave laser lateral crystallization,” *Jpn. J. Appl. Phys., Part 2*, vol. 41, pp. L311-L313, 2002.

[1.100] Bohuslav Rezek, Christoph E. Nebel, and Martin Stutzmann, “Polycrystalline silicon thin films produced by interference laser crystallization of amorphous silicon,” *Jpn. J. Appl. Phys., Part 2*, vol. 38, pp. L1083-L1084, 1999.

[1.101] Y. Helen, R. Dassow, M. Nerding, K. Mourgues, F. Raoult, J.R. Kohler, T. Mohammed-Brahim, R. Rogel, O. Bonnaud, J.H. Werner, and H.P. Strunk, “High mobility thin film transistors by Nd:YVO4-laser crystallization,” *Thin Solid Films*, vol. 383, pp. 143-146, 2001.

[1.102] Jia-Min Shieh, Zun-Hao Chen, Bau-Tong Dai, Yi-Chao Wang, Alexei Zaitsev, and

Ci-Ling Pan, “Near-infrared femtosecond laser-induced crystallization of amorphous silicon,” *Appl. Phys. Lett.*, vol. 85, pp. 1232-1234, 2004.

[1.103] W. G. Hawkins, J. G. Black, and C. H. Griffiths, “Growth of single-crystal silicon islands on bulk fused silica by CO2 laser annealing,” *Appl. Phys. Lett.*, vol. 40, pp. 319-321, 1982.

[1.104] K. Masumo, N. Kato, and M. Kunigita, “Anisotropically High Mobility Polycrystalline Silicon by High-speed Scanning Beam Annealing,” in *AMLCD Tech. Dig.*, 1997, pp. 183-186.

[1.105] H. Kuriyama, S. Kiyama, S. Noguchi, T. Kuwahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, S. Tsuda, and S. Nakano,” High Mobility Poly-Si TFT by a New Excimer Laser Annealing Method for Large Area Electronics,” in *IEDM Tech. Dig.*, 1991, pp. 563-566.

[1.106] S. D. Brotherton, D. J. McCulloch, J. P. Gowers, J. R. Ayres, and M. J. Trainor, “Influence of melt depth in laser crystallized poly-Si thin film transistors,” *J. Appl. Phys.*, vol. 82, pp. 4086-4094, 1997.

[1.107] H. Kuriyama, T. Nohda, S. Ishida, T. Kuwahara, S. Noguchi, S. Kiyama, S. Tsuda, and S. Nakano, “Lateral grain growth of poly-Si films with a specific orientation by an excimer laser annealing method,” *Jpn. J. Appl. Phys.*, *Part 1*, vol. 32, pp. 6190-6195, 1993.

[1.108] H. Kuriyama, S. Kiyama, S. Noguchi, T. Kuwahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, H. Kawata, M. Osumi, S. Tsuda, S. Nakano, and Y. Kuwano, “Enlargement of poly-Si film grain size by excimer laser annealing and its application to high-performance poly-Si thin film transistor,” *Jpn. J. Appl. Phys.*, vol. 30, pp. 3700-3703, 1991.

[1.109] A. T. Voutsas, A. M. Marmorstein, and R. Solanki, “The impact of annealing ambient on the performance of excimer-laser-annealed polysilicon thin-film transistors,” *J.*

*Electrochem. Soc.*, vol. 146, pp. 3500-3505, 1999.

[1.110] D. Toet, P. M. Smith, T. W. Sigmon, T. Takehara, C. C. Tsai, W. R. Harshbarger, and M. O. Thompson, "Laser crystallization and structural characterization of hydrogenated amorphous silicon thin films," *J. Appl. Phys.*, vol. 85, pp. 7914-7918, 1999.

[1.111] Jae-Hong Jeon, Juhn-Suk Yoo, Cheol-Min Park, Hong-Seok Choi, and Min-Koo Han, "A novel method for a smooth interface at poly-$SiO_x/SiO_2$ by employing selective etching," *IEEE Electron Device Lett.*, vol. 21, pp. 152-154, 2000.

[1.112] Aaron Marmorstein, Apostolos T. Viutsas, and Rai Solanki, "A systematic study and optimization of parameters affecting grain size and surface roughness in excimer laser annealed polysilicon thin films," *J. Appl. Phys.*, vol. 82, pp. 4303-4309, 1997.

[1.113] James S. Im, H. J. Kim, and Michael O. Thompson, "Phase transformation mechanisms involved on excimer laser crystallization of amorphous silicon films," *Appl. Phys. Lett.*, vol. 63, pp. 1969-1971, 1993.

[1.114] James S. Im and H. J. Kim, "On the super lateral growth phenomenon observed in excimer laser-induced crystallization of thin Si films," *Appl. Phys. Lett.*, vol. 64, pp. 2303-2305, 1994.

[1.115] M. O. Thompson, G. J. Galvin, J. W. Mayer, P. S. Peercy, J. M. Poate, D. C. Jacobson, A. G. Cullis, and N. G. Chew, "Melting temperature and explosive crystallization of amorphous silicon during pulsed laser irradiation," *Phys. Rev. Lett.*, vol. 52, pp. 2360-2363, 1984.

[1.116] S. R. Stiffler, Michael O. Thompson, and P. S. Peercy, "Supercooling and nucleation of silicon after laser melting," *Phys. Rev. Lett.*, vol. 60, pp. 2519-2522, 1988.

[1.117] S. R. Stiffler, M. O. Thompson, and P. S. Peercy, "Transient nucleation following pulsed-laser melting of thin silicon films," *Phys. Rev. B,* vol. 43, pp. 9851-9855, 1991.

[1.118] T. Eiumchotchawalit and James S. Im, "The mechanism of excimer laser-induced amorphization of ultra-thin Si films," *Mat. Res. Soc. Symp. Proc.*, vol. 321, pp. 725-730, 1994.

[1.119] H. J. Kim, D. Kim, J. H. Lee, I. G. Kim, G. S. Moon, J. H. Huh, J. W. Hwang, S. Y. Joo, K. W. Kim, and J. H. Souk, "A 7-in. full-color low-temperature poly-Si TFT-LCD," in *SID Tech. Dig.*, 1999, pp. 184-187.

[1.120] Z. Meng and M. Wong, "Active-matrix organic light-emitting diode displays realized using metal-induced unilaterally crystallized polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 49, pp. 991-996, 2002.

# Chapter 2

[2.1] H. J. Kim, D. Kim, J. H. Lee, I. G. Kim, G. S. Moon, J. H. Huh, J. W. Hwang, S. Y. Joo, K. W. Kim, and J. H. Souk, "A 7-in. full-color low-temperature poly-Si TFT-LCD," in *SID Tech. Dig.*, 1999, pp. 184-187.

[2.2] Jun Hanari, "Development of a 10.4-in. UXGA display using low-temperature poly-Si technology," *Journal of the SID*, vol. 10, pp. 53-56, 2002.

[2.3] Yasuhisa Oana, "Current and future technology of low-temperature poly-Si TFT-LCDs," *Journal of the SID*, vol. 9, pp. 169-172, 2001.

[2.4] S. Uchikoga and N. Ibaraki, "Low temperature poly-Si TFT-LCD by excimer laser anneal," *Thin Solid Films*, vol. 383, pp. 19-24, 2001.

[2.5] K. Yoneda, H. Ogata, S. Yuda, K. Suzuki, T. Yamaji, S. Nakanishi, T. Yamada, and Y. Morimoto, "Optimization of low-temperature poly-Si TFT-LCDs and a large-scale production line for large glass substrates," *Journal of the SID*, vol. 9, pp. 173-179, 2001.

[2.6] J. G. Blake, J. D. III Stevens, and R. Young, "Impact of low temperature polysilicon on the AMLCD market," *Solid State Tech.*, vol. 41, pp. 56-62, 1998.

[2.7] Y. Aoki, T. Lizuka, S. Sagi, M. Karube, T. Tsunashima, S. Ishizawa, K. Ando, H. Sakurai, T. Ejiri, T. Nakazono, M. Kobayashi, H. Sato, N. Ibaraki, M. Sasaki, and N. Harada, "A 10.4-in. XGA low-temperature poly-Si TFT-LCD for mobile PC applications," in *SID Tech. Dig.*, 1999, pp. 176-179.

[2.8] Y. Matsueda, T. Ozawa, M. Kimura, T. Itoh, K. Kitwada, T. Nakazawa, H. Ohsima, "A 6-bit-color VGA low-temperature poly-Si TFT-LCD with integrated digital data drivers," in *SID Tech. Dig.*, 1998, pp. 879-882.

[2.9] G. Rajeswaran, M. Itoh, M. Boroson, S. Barry, T. K. Hatwar, K. B. Kahen, K. Yoneda, R. Yokoyama, T. Yamada, N. Komiya, H. Kanno, and H. Takahashi, "Active matrix low temperature poly-Si TFT / OLED full color displays: development status," in *SID Tech. Dig.*, 2000, pp. 974-977.

[2.10] M. Kimura, I. Yudasaka, S. Kanbe, H. Kobayashi, H. Kiguchi, S. I. Seki, S. Miyashita, T. Shimoda, T. Ozawa, K. Kitawada, T. Nakazawa, W. Miyazawa, and H. Ohshima, "Low-temperature polysilicon thin-film transistor driving with integrated driver for high-resolution light emitting polymer display," *IEEE Trans. Electron Devices*, vol. 46, pp. 2282-2288, 1999.

[2.11] Mark Stewart, Robert S. Howell, Leo Pires, Miltiadis K. Hatalis, Webster Howard, and Olivier Prache, "Polysilicon VGA active matrix OLED displays – technology and performance," in *IEDM Tech. Dig.*, 1998, pp. 871-874.

[2.12] Mark Stewart, Robert S. Howell, Leo Pires, and Miltiadis K. Hatalis, "Polysilicon TFT technology for active matrix OLED displays," *IEEE Trans. Electron Devices*, vol. 48, pp. 845-851, 2001.

[2.13] T. Sasaoka, M.Sekiya, A. Yumoto, J. Yamada, T. Hirano, Y. Iwase, T. Yamada, T. Ishibashi, T. Mori, M. Asano, S. Tamura, and T. Urabe, "A 13.0-inch AM-OLED display with top emitting structure and adaptive current mode programmed pixel circuit (TAC)," in *SID Tech. Dig.*, 2001, pp. 384-387.

[2.14] Z. Meng, H. Chen, C. F. Qiu, H. S. Kwok, and M. Wong, "Active-matrix organic light-emitting diode display implemented using metal-induced unilateral crystallized polycrystalline silicon thin-film transistors," in *SID Tech. Dig.*, 2001, pp. 380-383.

[2.15] Z. Meng and M. Wong, "Active-matrix organic light-emitting diode displays realized using metal-induced unilaterally crystallized polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 49, pp. 991-996, 2002.

[2.16] M. Miyasaka, "Suftla Flexible Microelectronics on Their Way to Business," in *SID Tech. Dig.*, 2007, pp. 1673-1676.

[2.17] C. D Kim, I. B Kang, and I. J Chung "TFT Technology for Flexible Displays," in *SID Tech. Dig.*, 2007, pp. 1669-1672.

[2.18] Y. Kuo, **"**TFT and ULSIC - Competition or Collaboration," in *AMFPD Tech. Dig.*, 2007, pp. 1-4.

[2.19] V. W. C. Chan, Philip C. H. Chan, M. Chan," Three dimensional CMOS integrated circuits on large grain polysilicon films," in *IEDM Tech. Dig.*, 2000, pp. 161-164.

[2.20] H. Wang, M. Chan, S. Jagar, Y. Wang, and P. K. Ko, "Submicron super TFTs for 3-D VLSI applications," *IEEE Electron Device Lett.*, vol. 21, pp. 439-441, 2000.

[2.21] Victor W. C. Chan, Philip C. H. Chan, and Mansun Chan, "Three-dimensional CMOS SOI integrated circuit using high-temperature metal-induced lateral crystallization," *IEEE Trans. Electron Devices*, vol. 48, pp. 1394-1399, 2001.

[2.22] K. Banerjee, S. J. Souri, P Kapur, and K. C. Saraswat, "3-D ICs: a novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proceedings of the IEEE*, vol. 89, pp. 602-633, 2001

[2.23] F. S. Wang, M. J. Tsai, and H. C. Cheng, "The effects of $NH_3$ plasma passivation on polysilicon thin film transistors, "*IEEE Electron Device Lett.*, vol. 16, pp. 503-505, 1995.

[2.24] H. C. Cheng, F. S. Wang, and C. Y. Huang, “Effects of $NH_3$ plasma passivation on n-channel polycrystalline silicon thin-film transistors,” *IEEE Trans. Electron Devices*, vol. 44, pp. 64-68, 1997.

[2.25] J. Lai, and T. J. King Liu, “Defect Passivation by Selenium-Ion Implantation for Poly-Si Thin Film Transistors, “*IEEE Electron Device Lett.*, vol. 28, pp. 725-727, 2007.

[2.26] S. D. Wang, W. H. Lo, T. Y. Chang, and T. F. Lei, “A novel process-compatible fluorination technique with electrical characteristic improvements of poly-Si TFTs, “*IEEE Electron Device Lett.*, vol. 26, pp. 372-274, 2005.

[2.27] C. H. Tu, T. C. Chang, P. T. Liu, C. Y. Yang, H. C. Liu, W. R. Chen, Y. C. Wu, and C. Y. Chang,, “Improvement of electrical characteristics for fluorine-ion-implanted poly-Si TFTs using ELC, “*IEEE Electron Device Lett.*, vol. 27, pp. 262-264, 2006.

[2.28] S. D. Wang, W. H. Lo, and T. F. Lei, “CF4 Plasma Treatment for Fabricating High-Performance and Reliable Solid-Phase-Crystallized Poly-Si TFTs,” *J. Electrochem. Soc.*, vol. 152, pp. G703-G706, 2005.

[2.29] M. A. Crowder, P. G. Carey, P. M. Smith, Robert S. Sposili, Hans S. Cho, and James S. Im, “Low-temperature single-crystal Si TFT’s fabricated on Si films processed via sequential lateral solidification,” *IEEE Electron Device Lett.*, vol. 19, pp. 306-308, 1998.

[2.30] N. Yamauchi and R. Reif, “Polycrystalline silicon thin films processed with silicon ion implantation and subsequent solid-phase crystallization: Theory, experiments, and thin-film transistor applications,” *J. Appl. Phys.*, vol. 75, pp. 3235-3257, 1994.

[2.31] V. W. C. Chan, Philip C. H. Chan, M. Chan,” Three dimensional CMOS integrated circuits on large grain polysilicon films,” in *IEDM Tech. Dig.*, 2000, pp. 161-164.

[2.32] H. Wang, M. Chan, S. Jagar, Y. Wang, and P. K. Ko, “Submicron super TFTs for 3-D VLSI applications,” *IEEE Electron Device Lett.*, vol. 21, pp. 439-441, 2000.

[2.33] Victor W. C. Chan, Philip C. H. Chan, and Mansun Chan, "Three-dimensional CMOS SOI integrated circuit using high-temperature metal-induced lateral crystallization," *IEEE Trans. Electron Devices*, vol. 48, pp. 1394-1399, 2001.

[2.34] Soo Young Yoon, Seong Jin Park, Kyung Ho Kim, and Jin Jang, "Structural and electrical properties of polycrystalline silicon produced by low-temperature Ni silicide mediated crystallization of the amorphous phase," *J. Appl. Phys.*, vol. 87, pp. 609-611, 2000.

[2.35] Soo Young Yoon, Ki Hyung, Chae Ok Kim, Jae Young Oh, and Jin Jang, "Low temperature metal induced crystallization of amorphous silicon using a Ni solution," *J. Appl. Phys.*, vol. 82, pp. 5865-5867, 1997.

[2.36] Zhonghe Jin, Keith Moulding, Hoi S. Kwok, and Man Wong, "The effects of extended heat treatment on Ni induced lateral crystallization of amorphous silicon thin films," *IEEE Trans. Electron Devices.*, vol. 46, pp. 78-82, 1999.

[2.37] K. Sera, F. Okumura, H. Uchida, S. Itoh, S. Kaneko, and K. Hotta, "High-performance TFTs fabricated by XeCl excimer laser annealing of hydrogenated amorphous-silicon film," *IEEE Trans. Electron Devices*, vol. 36, pp. 2868-2872, 1989.

[2.38] T. Sameshima, S. Usui, and M. Sekiya, "XeCl Excimer laser annealing used in the fabrication of poly-Si TFT's," *IEEE Electron Device Lett.*, vol. 7, pp. 276-278, 1986.

[2.39] Y. F. Tang, S. R. P. Silva, and M. J. Rose, "Super sequential lateral growth of Nd:YAG laser crystallized hydrogenated amorphous silicon," *Appl. Phys. Lett.*, vol. 78, pp. 186-188, 2001.

[2.40] Akito Hara, Fumiyo Takeuchi, Michiko Takei, Katsuyuki Suga, Kenichi Yoshino, Mitsuru Chida, Yasuyuki Sano, and Nobuo Sasaki, "High-performance polycrystalline silicon thin film transistors on non-alkali glass produced using continuous wave laser lateral crystallization," *Jpn. J. Appl. Phys., Part 2*, vol. 41, pp.

L311-L313, 2002.

[2.41] Bohuslav Rezek, Christoph E. Nebel, and Martin Stutzmann, "Polycrystalline silicon thin films produced by interference laser crystallization of amorphous silicon," *Jpn. J. Appl. Phys., Part 2*, vol. 38, pp. L1083-L1084, 1999.

[2.42] Y. Helen, R. Dassow, M. Nerding, K. Mourgues, F. Raoult, J.R. Kohler, T. Mohammed-Brahim, R. Rogel, O. Bonnaud, J.H. Werner, and H.P. Strunk, "High mobility thin film transistors by Nd:YVO4-laser crystallization," *Thin Solid Films*, vol. 383, pp. 143-146, 2001.

[2.43] Jia-Min Shieh, Zun-Hao Chen, Bau-Tong Dai, Yi-Chao Wang, Alexei Zaitsev, and Ci-Ling Pan, "Near-infrared femtosecond laser-induced crystallization of amorphous silicon," *Appl. Phys. Lett.*, vol. 85, pp. 1232-1234, 2004.

[2.44] Y. C. Wang, J. M. Shieh, H. W. Zan, and C. L. Pan, "Near-infrared femtosecond laser crystallized poly-Si thin film transistors," *Optics Express.*, vol. 15, pp. 6982-6986, 2007.

[2.45] Y. C. Wang, C. L. Pan, J. M. Shieh, and B. T. Dai, "Dopant profile engineering by near-infrared femtosecond laser activation," *Appl. Phys. Lett.* Vol. 88, pp. 131104-131106, 2006.

[2.46] W. G. Hawkins, J. G. Black, and C. H. Griffiths, "Growth of single-crystal silicon islands on bulk fused silica by CO2 laser annealing," *Appl. Phys. Lett.*, vol. 40, pp. 319-321, 1982.

[2.47] K. Masumo, N. Kato, and M. Kunigita, "Anisotropically High Mobility Polycrystalline Silicon by High-speed Scanning Beam Annealing," in *AMLCD Tech. Dig.*, 1997, pp. 183-186.

[2.48] A. Hara, F. Takeuchi, and N. Sasaki, "Mobility enhancement limit of excimer-laser-crystallized polycrystalline silicon thin film transistors," *J. Appl. Phys.*, vol. 91, pp. 708-714, 2002.

[2.49] G. K.Giust, T. W. Sigmon, J. B. Boyce, and J. Ho, “High-performance laser-processed polysilicon thin-film transistors,” *IEEE Electron Device Lett.*, vol. 20, pp. 77-79, 1999.

[2.50] K. Yamaguchi, “Modeling and characterization of polycrystalline-silicon thin-film transistors with a channel-length comparable to a grain size,” *J. Appl. Phys.*, vol. 89, pp. 590-595, 2001.

[2.51] M. Kimura, S. Inoue, T. Shimoda, and T. Eguchi, “Dependence of polycrystalline silicon thin-film transistor characteristics on the grain-boundary location,” *J. Appl. Phys.*, vol. 89, pp. 596-600, 2001.

[2.52] James S. Im, H. J. Kim, and Michael O. Thompson, “Phase transformation mechanisms involved on excimer laser crystallization of amorphous silicon films,” *Appl. Phys. Lett.*, vol. 63, pp. 1969-1971, 1993.

[2.53] James S. Im and H. J. Kim, “On the super lateral growth phenomenon observed in excimer laser-induced crystallization of thin Si films,” *Appl. Phys. Lett.*, vol. 64, pp. 2303-2305, 1994.

[2.54] J. W Lee, N. I. Lee, H. J. Chung, and C. H. Han,” Improved stability of polysilicon thin-film transistors under self-heating and high endurance EEPROM cells for systems-on-panel,” in *IEDM Tech. Dig.,* 1998, pp. 265-268.

[2.55] Y. Matsueda, S. Inoue, and T. Shimoda, “Concept of system on panel,” in *AMLCD Tech. Dig.*, 2001, pp. 77-80.

[2.56] T. Nishibe and H. Nakamura, “Value-Added Circuit and Function Integration for SOG (System-on Glass) Based on LTPS Technology,” in *SID Tech. Dig.*, 2006, pp. 1091-1094.

[2.57] Y. Yamamoto, T. Matsuo, and H. Komiya, “CG Silicon Technology and System Integration for Mobile Applications,” in *SID Tech. Dig.*, 2006, pp. 1173-1176.

[2.58] Y. Nakajima, Y. Teranishi, Y. Kida, and Y Maki, “Ultra-Low-Power LTPS TFT-LCD

Technology Using a Multi-Bit Pixel Memory Circuit," in *SID Tech. Dig.*, 2006, pp. 1185-1188.

[2.59] Robert S. Sposili and James S. Im, "Sequential lateral solidification of thin silicon films on $SiO_2$," *Appl. Phys. Lett.*, vol. 69, pp. 2864-2866, 1996.

[2.60] M. A. Crowder, P. G. Carey, P. M. Smith, Robert S. Sposili, Hans S. Cho, and James S. Im, "Low-temperature single-crystal Si TFT's fabricated on Si films processed via sequential lateral solidification," *IEEE Electron Device Lett.*, vol. 19, pp. 306-308, 1998.

[2.61] J. S. Im, R. S. Sposili, and M. A. Crowder, "Single-crystal Si films for thin-film transistor devices," *Appl. Phys. Lett.*, vol. 70, pp. 3434-3436, 1997.

[2.62] H. S. Cho, D. B. Kim, A. B. Limanov, M. A. Crowder, and J. S. Im, "Sequential lateral solidification of ultra-thin a-Si films," *Mat. Res. Soc. Symp. Proc.*, vol. 621, Q9.9.1-Q9.9.6, 2000.

[2.63] Y. H. Jung, J. M. Yoon, M. S. Yang, W. K. Park, H. S. Soh, H. S. Cho, A. B. Limanov, and J. S. Im, "The dependence of poly-Si TFT characteristics on the relative misorientation between grain boundaries and the active channel," *Mat. Res. Soc. Symp. Proc.*, vol. 621, Q9.14.1-Q9.14.6, 2000.

[2.64] Y. H. Jung, J. M. Yoon, M. S. Yang, W. K. Park, H. S. Soh, H. S. Cho, A. B. Limanov, and J. S. Im, "Low temperature polycrystalline Si TFTs fabricated with directionally crystallized Si film," *Mat. Res. Soc. Symp. Proc.*, vol. 621, Q8.3.1-Q8.3.6, 2000.

[2.65] M. A. Crowder, Robert S. Sposili, A. B. Limanov, and James. S. Im, "Sequential lateral solidification of PECVD and sputter deposited a-Si films," *Mat. Res. Soc. Symp. Proc.*, vol. 621, Q9.7.1-Q9.7.6, 2000.

[2.66] M. A. Crowder, A. B. Limanov, and James. S. Im, "Sub-grain boundary spacing in directionally crystallized Si films obtained via sequential lateral solidification," *Mat. Res. Soc. Symp. Proc.*, vol. 621, Q9.6.1-Q9.6.6, 2000.

[2.67] R.S. Sposili, and J.S. Im, "Line-scan sequential lateral solidification of Si thin films," *Appl. Phys. A.*, vol. 67, pp. 273–276, 1998.

[2.68] Ji-Yong Park, Hye-Hyang Park, Ki-Yong Lee and Ho-Kyoon Chung, "Design of Sequential Lateral Solidification Crystallization Method for Low Temperature Poly-Si Thin Film Transistors," *Jpn. J. Appl. Phys.*, vol. 43, pp. 1280-1286, 2004.

[2.69] Mark A. Crowder, A. Tolis Voutsas, Steven R. Droes, Masao Moriguchi, and Yasuhiro Mitani, "Sequential Lateral Solidification Processing for Polycrystalline Si TFTs," *IEEE Trans. Electron Devices*, vol. 51, pp.560-568, 2004.

[2.70] A. T. Voutsas, A. Limanov and J. S. Im, "Effect of process parameters on the structural characteristics of laterally grown, laser-annealed polycrystalline silicon films," *J. Appl. Phys.*, vol. 94, pp. 7445-7452, 2003.

[2.71] A. T. Voutsas, "Assessment of the performance of laser-based lateral-crystallization technology via analysis and modeling of polysilicon thin-film-transistor mobility," *IEEE Trans. Electron Devices*, vol. 50, pp.1494-1500, 2003.

[2.72] P.C. van der Wilt, M.G. Kane, A.B. Limanov, A.H. Firester, L. Goodman, J. Lee, J.R. Abelson, A.M. Chitu, and James S. Im, "Low-Temperature Polycrystalline Silicon Thin-Film Transistors and Circuits on Flexible Substrates," *MRS BULLETIN*, vol. 31, pp. 461-465, June 2006.

[2.73] Paul Ch. van der Wilt, B. D. van Dijk, G. J. Bertens, R. Ishihara, and C. I. M. Beenakker, "Formation of location-controlled crystalline islands using substrate-embedded seeds in excimer-laser crystallization of silicon films," *Appl. Phys. Lett.*, vol. 79, pp. 1819-1821, 2001.

[2.74] Ryoichi Ishihara, Paul C. van der Wilt, Barry D. van Dijk, J. W. Metselaar, and C. I. M. Beenakker, "Property of single-crystalline Si TFTs fabricated with μ-Czochralski (grain filter) process," *Proceedings of SPIE.*, vol. 5004, pp. 10-19, 2003.

[2.75] R. Ishihara, Y. Hiroshima, D. Abe, B. D. van Dijk, P. C. van der Wilt, S. Higashi, S.

Inoue, T. Shimoda, J.W. Metselaar, and C. I. M. Beenakker, “Single-grain Si TFTs with ECR-PECVD gate $SiO_2$,” *IEEE Trans. Electron Devices*, vol. 51, pp.500-502, 2004.

[2.76] Paul Ch. Van der Wilt, R. Ishihara, and J. Bertens, “Location-controlled large-grains in near-ablation excimer-laser crystallized silicon films,” *Mat. Res. Soc. Symp. Proc.*, vol. 621, pp. Q7.4.1-Q7.4.6, 2000.

[2.77] B. D. van Dijk, Paul Ch. Van der Wilt, G. J. Bertens, Lis.K. Nanver, and R. Ishihara, “Single-crystal thin film transistor by grain-filter location-controlled excimer-laser crystallization,” *Mat. Res. Soc. Symp. Proc.*, vol. 685, pp. D12.3.1-D12.3.6, 2001.

[2.78] Hiroyuki Shimada, Yasushi Hiroshima and Tatsuya Shimoda, “Low temperature single grain thin film transistor (LTSG-TFT) with SOI performance using cmp-flattened μ-czochralski process,” in *IEDM Tech Dig.*, 2005, pp.923-926.

[2.79] Ming He, Ryoichi Ishihara, Yasushi Hiroshima, Satoshi Inoue, Tatsuya Shimoda, Wim Metselaar and Kees Beenakker, “Effects of Capping Layer on Grain Growth with μ-Czochralski Process during Excimer Laser Crystallization,” *Jpn. J. Appl. Phys.*, vol. 45, pp. 1-6, 2995.

[2.80] Vikas Rana, Ryoichi Ishihara, Yasushi Hiroshima, Daisuke Abe, Satoshi Inoue, Tatsuya Shimoda, Wim Metselaar, and Kees Beenakker, “Dependence of single-crystalline Si TFT characteristics on the channel position inside a location-controlled grain,” *IEEE Trans. Electron Devices*, vol. 52, pp.2622-2628, 2005.

[2.81] David S. Knowles, Ji-yong Park, Chaiin Im, Palash Das, Thomas Hoffman, “Thin-beam Crystallization Method for Fabrication of LTPS,” *in SID Tech. Dig.*, 2005, pp. 503-505.

[2.82] Chihwei Chao, Jiatien Peng, CW Cheng, Chunghung Chen, Brandon A. Turk, Bernd Burfeindt, “The Investigation of High Performance TFT by Thin Beam Directional

X-stallization Method," *Mat. Res. Soc. Symp. Proc.*, vol. 910, pp. A15-4 – A15-9 , 2006.

[2.83] Masayuki Jyumonji, Yoshinobu Kimura, Yukio Taniguchi, Masato Hiramatsu, Hiroyuki Ogawa and Masakiyo Matsumura , "Optimum Light Intensity Distribution for Growing Large Si Grains by Phase-Modulated Excimer-Laser Annealing," *Jpn. J. Appl. Phys.*, vol. 43, pp. 739-744, 2004.

[2.84] Y. Taniguchi, M. Matsumura, M. Jyumonji, H. Ogawa, and M. Hiramatsu, "Novel Phase Modulator for ELA-Based Lateral Growth of Si," *J. Electrochem. Soc.*, vol. 153, pp. G67-G71, 2006.

[2.85] Genshiro Kawachi, Shinzo Tsuboi, Takashi Okada, Masahiro Mitani, and Masakiyo Matsumura, "Analysis of threshold voltage of short channel polycrystalline silicon thin-film transistors fabricated on large grains," *J. Appl. Phys.*, vol. 100, pp. 114507-1 - 114507-6, 2007.

[2.86] C. H. Oh, M. Ozawa, and M. Matsumura, "A novel phase-modulated excimer-laser crystallization method of silicon thin films," *Jpn. J. Appl. Phys. Part 2*, vol. 37, pp. L492-L495, 1998.

[2.87] C. H. Oh and M. Matsumura, "A proposed single grain-boundary thin-film transistor," *IEEE Electron Device Lett.*, vol. 22, pp. 20-22, 2001.

[2.88] C. H. Oh and M. Matsumura, "Preparation of position-controlled crystal- silicon island arrays by means of excimer-laser annealing," *Jpn. J. Appl. Phys. Part 1*, vol. 37, pp. 5474-5479, 1998.

[2.89] M. Ozawa, C. H. Oh, and M. Matsumura, "Two-dimensionally position-controlled excimer-laser-crystallization of silicon thin films on glassy substrate," *Jpn. J. Appl. Phys. Part 1*, vol. 38, pp. 5700-5705, 1999.

[2.90] M. Matsumura and C. H. Oh, "Advanced excimer-laser annealing process for quasi single-crystal silicon thin-film devices," *Thin Solid Films*, vol. 337, pp. 123-128, 1999.

[2.91] T. Endo, Y. Taniguchi, T. Katou, S. Shimoto, T. Ohno, K. Azuma, and M. Matsumura, "Pseudo-Single-Nucleus Lateral Crystallization of Si Thin Films" in *AMFPD Tech. Dig.*, 2007, pp. 61-63.

[2.92] R. Ishihara, and A. Burtsev, "Location Control of Large Grain Following Excimer-Laser Melting of Si Thin-Films," *Jpn. J. Appl. Phys. Part 1*, vol. 37, pp. 1071-1075, 1998.

[2.93] R. Ishihara, A. Burtsev, and P. F. A. Alkemade, "Location-control of large Si grains by dual-beam excimer-laser and thick oxide portion," *Jpn. J. Appl. Phys. Part* 1, vol. 39, pp. 3873-3878, 2000.

[2.94] K.Yamazaki, T. Kudo, K. Seike, D. Ichishima and C. G. Jin, "Double-pulsed laser annealing system and polycrystallization with Green DPSS lasers " in *AMLCD Tech. Dig.*, 2002, pp. 149-152.

[2.95] S. Sakuragi, T. Kudo, K.Yamazaki and T. Asano, "High field effect mobility poly-Si TFTs fabricated by advanced lateral crystal growth process using double-pulsed laser annealing system," *in the proceeding of the 12th International Display Workshops*, 2005, pp. 965-968.

[2.96] T. Kudo, K. Seike, K.Yamazaki, H. Komori, S. Yawaka, S. Hamada, and C. G. Jin, "Advanced lateral crystal growth of a-Si thin films by Double-pulsed irradiation od all solid-state lasers " in *Mat. Res. Soc. Symp. Proc.*, vol. 762, pp. A16.5.1-A16.5.6 , 2003.

[2.97] J. H. Jeon, M. C. Lee, S. H. Jung, and M. K. Han, "Excimer laser recrystallization of a-Si employing aluminum masking window," *Mat. Res. Soc. Symp. Proc.*, vol. 609, pp. A25.3.1-A25.3.5 , 2000.

[2.98] H. J. Kim and James S. Im, "New excimer-laser-crystallization method for producing large-grained and grain boundary-location-controlled Si films for thin film transistors," *Appl. Phys. Lett.*, vol. 68, pp. 1513-1515, 1996.

[2.99] H. J. Kim and James S. Im, "Optimization and transformation analysis of grain-boundary-location-controlled Si films," *Mat. Res. Soc. Symp. Proc.*, vol. 397, pp. 401-406, 1996.

[2.100] L. Mariucci, R. Carluccio, A. Pecora, V. Foglietti, G. Fortunato, P. Legagneux, D. Pribat, D. Della Sala, and J. Stoemenos, "Lateral growth control in excimer laser crystallized polysilicon," *Thin Solid Films*, vol. 337, pp. 137-142, 1999.

[2.101] J. H. Jeon, M. C. Lee, K. C. Park, and M. K. Han, "A new polycrystalline silicon TFT with a single grain boundary in the channel," *IEEE Electron Device Lett.*, vol. 22, pp. 429-431, 2001.

[2.102] J. H. Jeon, M. C. Lee, K. C. park, and M. K. Han, "New excimer laser recrystallization of poly-Si for effective grain growth and grain boundary arrangement," *Jpn. J. Appl. Phys. Part 1*, vol. 39, pp. 2012-2014, 2000.

[2.103] T. Sameshima, "Self organized grain growth larger than 1 μm through pulsed-laser-induced melting of silicon films," *Jpn. J. Appl. Phys.*, vol. 32, pp. L1485-L1488, 1993.

[2.104] M. Cao, S. Talwar, K. Josef Kramer, T. W. Sigmon, and K. C. Saraswat, "A high-performance polysilicon thin-film transistor using XeCl excimer laser crystallization of pre-patterned amorphous Si films," *IEEE Trans. Electron Devices*, vol. 43, pp. 561-567, 1996.

[2.105] G. K. Giust and T. W. Sigmon, "Comparison of excimer laser recrystallized prepatterned and unpatterned silicon films on $SiO_2$," *J. Appl. Phys.*, vol. 81, pp. 1204-1211, 1997.

[2.106] G. K. Giust and T. W. Sigmon, "Performance improvement obtained for thin-film transistors fabricated in prepatterned laser-recrystallized polysilicon," *IEEE Electron Device Lett.*, vol. 18, pp. 296-298, 1997.

[2.107] A. Hara and N. Sasaki, “Use of necked-down areas to control nucleation site and direction of solidification of polycrystalline silicon using excimer laser crystallization,” *J. Appl. Phys.*, vol. 88, pp. 3349-3353, 2000.

[2.108] M. Nakata, H. Okumura, H. Kanoh, H. Hayama, and S. Kaneko, “Single-crystal silicon TFT fabricated with comb-shaped beam ZMR-ELA,” *in the proceeding of the 12th International Display Workshops*, 2005, pp. 957-960.

[2.109] F. Okumura, “SOG technologies in NEC,” *in the proceeding of the International Display Manufacture Conference*, 2005, pp. 311-314.

[2.110] C. H. Kim, I. H. Song, W. J. Nam, and M. K. Han, “A poly-Si TFT fabricated by excimer laser recrystallization on floating active structure,” *IEEE Electron Device Lett.*, vol. 23, pp. 325-327, 2002.

[2.111] I. H. Song, S. H. Kang, W. J. Nam, and M. K. Han, “A high-performance multichannel dual-gate poly-Si TFT fabricated by excimer laser irradiation on a floating a-Si thin film,” *IEEE Electron Device Lett.*, vol. 24, pp. 580-582, 2003.

[2.112] C. H. Kim, J. S. Yoo, I. H. Song and M. K. Han, “Excimer laser recrystallization of selectively floating a-Si active layer for large-grained poly-Si film,” *Mat. Res. Soc. Symp. Proc.*, vol. 664, pp. A6.11.1-A6.11.6, 2001.

[2.113] C. H. Kim, I. H. Song, W. J. Nam, and M. K. Han, “Excimer laser recrystallization of selectively floating a-Si thin film,” *J. Non-Cryst. Solids*, vol. 299-302, pp. 721-725, 2002.

[2.114] D. H. Choi, K. Shimizu, O. Sugiura, and M. Matsumura, “Drastic enlargement of grain size of excimer-laser-crystallized polysilicon films,” *Jpn. J. Appl. Phys. Part 1*, vol. 31, pp. 4545-4549, 1992.

[2.115] D. H. Choi, E. Sadayuki, O. Sugiura, and M. Matsumura, “Lateral growth of poly-Si film by excimer laser and its thin film transistor application,” *Jpn. J. Appl. Phys. Part 1*, vol. 33, pp. 70-74, 1994.

[2.116] W. C. Yeh and Y. C. Liu, "Excimer laser crystallization of silicon islands with a peninsular structure as a nucleation," in *AMLCD Tech. Dig.*, 2003, pp. 159-160.

[2.117] J. X. Lin, C. C. Chen, Y. C. Chen, W. C. Yeh and Y. C. Liu, "Fabrication of large-grained poly-silicon thin film by heat-retaining enhanced crystallization," in *AMLCD Tech. Dig.*, 2004, pp. 157-160.

[2.118] Y. Helen, , R. Dassow, M. Nerding, K. Mourgues, F. Raoult, J.R. K¨ohler,T. Mohammed-Brahim, R. Rogel, O. Bonnaud, J.H. Werner, H.P. Strunk, "High mobility thin film transistors by Nd:YVO4-laser crystallization," *Thin Solid Films*, vol. 383, pp. 143-146, 2001.

[2.119] M. Nerding, S. Christiansen, J. Krinke, R. Dassow, J. R. Köhler, J. -H. Werner and H. -P. Strunk, "Grain populations in laser-crystallised silicon thin films on glass substrates," *Thin Solid Films*, vol. 383, pp. 110-112, 2001.

[2.120] J. H. Werner, R. Dassow, T. J. Rinke, J. R. Köhler and R. B. Bergmann, "From polycrystalline to single crystalline silicon on glass," *Thin Solid Films*, vol. 383, pp. 95-100, 2001.

[2.121] F. Falk, and G. Andrä, "Laser crystallization — a way to produce crystalline silicon films on glass or on polymer substrates," *Journal of Crystal Growth*, vol. 287, pp. 397-401, 2006.

[2.122] G. Andrä, J. Bergmann and F. Falk, "Laser crystallized multicrystalline silicon thin films on glass," *Thin Solid Films*, vol. 487, pp. 77-80, 2005.

[2.123] A. Saboundji, T. Mohammed-Brahim, G. Andrä, J. Bergmann and F. Falk, "Thin film transistors on large single crystalline regions of silicon induced by cw laser crystallization," *Journal of Crystal Growth*, vol. 338-340, pp. 758-761, 2004.

[2.124] A. Hara, F. Takeuchi, and N. Sasaki, "Selective single-crystalline-silicon growth at the pre-defined active regions of TFTs on a glass by a scanning CW laser irradiation," in *IEDM Tech Dig.*, 2000, pp.209-212.

[2.125] A. Hara, M. Takei, F. Takeuchi, K. Suga, K. Yoshino, M. Chida, T. Kakehi, Y. Ebiko, Y. Sano and N. Sasaki, "High Performance Low Temperature Polycrystalline Silicon Thin Film Transistors on Non-alkaline Glass Produced Using Diode Pumped Solid State Continuous Wave Laser Lateral Crystallization," *Jpn. J. Appl. Phys. Part 1*, vol. 43, pp. 1269-1276, 2004.

[2.126] A. Hara, M. Takei, K. Yoshino, F. Takeuchi and N. Sasaki, "Self-Aligned Metal Double-Gate Low-Temperature Polycrystalline Silicon Thin-Film Transistors on Non-Alkali Glass Substrate Using Diode-Pumped Solid-State Continuous Wave Laser Lateral Crystallization," *Jpn. J. Appl. Phys.*, vol. 43, pp. L790-L793, 2004.

[2.127] A. Hara, F. Takeuchi, M. Takei, K. Suga, K. Yoshino, M. Chida, Y. Sano and N. Sasaki, "High-Performance Polycrystalline Silicon Thin Film Transistors on Non-Alkali Glass Produced Using Continuous Wave Laser Lateral Crystallization," *Jpn. J. Appl. Phys.*, vol. 41, pp. L311-L313, 2002.

[2.128] A. Hara, K. Yoshino, F. Takeuchi, and N. Sasaki, "Selective Single-Crystalline-Silicon Growth at the Pre-defined Active Region of a Thin Film Transistor on Glass by Using Continuous Wave Laser Irradiation," *Jpn. J. Appl. Phys.*, vol. 42, pp. 23-27, 2003.

[2.129] K. Kitahara, Y. Ohashi, Y. Katoh, A. Hara and N. Sasaki, "Submicron-scale characterization of poly-Si thin films crystallized by excimer laser and continuous-wave laser," *J. Appl. Phys.*, vol. 95, pp. 7850-7855, 2004.

[2.130] Y. Sano, M. Takei, A. Hara, and N. Sasaki, "High-Performance Single-Crystalline-Silicon TFTs on a Non-Alkali Glass Substrate," in *IEDM Tech Dig.*, 2002, pp.565-568.

[2.131] A. Hara, Y. Mishima, T. Kakehi, F. Takeuchi, M. Takei, K. Yoshino, K. Suga, M. Chida, and N. Sasaki, "High Performance Poly-Si TFTs on a Glass by a Stable Scanning CW Laser Lateral Crystallization," in *IEDM Tech Dig.*, 2001, pp.747-750.

[2.132] A. Hara, M. Takei, K. Yoshino, F. Takeuchi, M. Chida, and N. Sasaki, “Self-Aligned Top and Bottom Metal Double Gate Low Temperature Poly-Si TFT Fabricated at 550 ℃ on Non-Alkali Glass Substrate by Using DPSS CW Laser Lateral Crystallization Method,” in *IEDM Tech Dig.*, 2003, pp.211-214.

[2.133] N. Sasaki, A. Hara, F. Takeuchi, Y. Mishima, T. Kakehi, K. Yoshino, and M. Takei, “High Throughput CW-Laser Lateral Crystallization for Low-Temperature Poly-Si TFTs and Fabrication of 16 bit SRAMs and 270MHz Shift Registers,” in *SID Tech. Dig.*, 2002, pp. 154-157.

[2.134] T. Yoshida, K. Yoshino, M. Takei, A. Hara, N. Sasaki, and T. Tsuchiya, “Experimental evidence of grain-boundary related hot-carrier degradation mechanism in low-temperature poly-Si thin-film-transistors,” in *IEDM Tech Dig.*, 2003, pp.219-222.

[2.135] M. Hatano, and T. Shiba “Selectively enlarging laser crystallization technology for high and uniform performance poly-Si TFTs,” *in SID Symposium Digest*, 2002, pp. 158-161.

[2.136] M. Matsumura, M. Hatano, T. Kaitoh, and M. Ohkura, “Subthreshold properties of TFTs with laser-crystallized laterally grown polysilicon layers,” *IEEE Electron Device Lett.*, vol. 27, pp. 278-280, 2006.

[2.137] M. Tai, M. Hatano, S. Yamaguchi, T. Noda, S. K. Park, T. Shiba, and M. Ohkura, “Performance of poly-Si TFTs fabricated by SELA,” *IEEE Trans. Electron Devices*, vol. 51, pp. 934-939, 2004.

[2.138] M. Hatano, T. Sato, M. Matsumura, Y. Toyota, M. Tai, M. Ohkura, and T. Miyazawa, “System on glass display with LTPS TFTs formed using SELAX technology” *in the proceeding of the 12th International Display Workshops*, 2005, pp. 953-956.

[2.139] M. Tai, T. Sato, M. Matsumura, M. Hatano, and M. Ohkura, “Relationship between Mobility and Configuration of Thin-Film Transistor Fabricated with Laterally-Grown Polycrystalline Silicon Layer” in *AMLCD Tech. Dig.*, 2007, pp. 205-206.

[2.140] Y. Toyota, M. Matsumura, M. Hatano, and T. Shiba, “Integration of Reliability with High Current Drivability by using SELAX Technology for High-Resolution (>300 ppi) System-in-Displays,” in *SID Tech. Dig.*, 2005, pp. 1439-1441.

[2.141] C. W. Lin, L. J. Cheng, Y. L. Lu, Y. S. Lee, and H. C. Cheng, “High performance low-temperature poly-Si TFTs crystallized by excimer laser irradiation with recessed-channel structure,” *IEEE Electron Device Lett.*, vol. 22, pp. 269-271, 2001.

[2.142] L. Mariucci, A. Pecora, R. Carluccio, G. Fortunato, “Advanced excimer laser crystallization techniques,” *Thin Solid Films*, vol. 383, pp. 39-44, 2001.

[2.143] T. K. Chang, C. W. Lin, C. C. Tsai, J. H. Lu, B. T. Chen and H. C. Cheng, “High-performance poly-Si thin film transistors crystallized by excimer laser irradiation with a-Si spacer structure,”*IEEE/ECS Electrochemical and solid-state Lett.* Vol. 8, pp.G14-G16, 2005.

[2.144] H. C. Cheng, C. C. Tsai, J. H. Lu, H. H. Chen, B. T. Chen, T. K. Chang, and C. W. Lin, “Periodically Lateral Silicon Grains Fabricated by Excimer Laser Irradiation with a-Si Spacers for LTPS TFTs,” *J. Electrochem. Soc.*, vol. 154, pp. J5-J10, 2007.

[2.145] Y. Mishima, K. Yoshino, M. Takei, and N. Sasaki, “Characteristics of low-temperature poly-Si TFTs on Al/glass substrates,” *IEEE Trans. Electron Devices*, vol. 48, pp. 1087-1091, 2001.

[2.146] I. Wei Wu, I. Wei Wu, “Polycrystalline silicon thin film transistors for liquid crystal displays,” *Solid State Phenomena*, vol. 37~38, pp. 553-564, 1994.

[2.147] M .H .Lee, S. J. Moon, M. Hatano, K. Suzuki, and C. P. Grigoropoulos, “Relationship between fluence gradient and lateral grain growth in spatially controlled excimer laser crystallization of amorphous silicon films,” *J. Appl. Phys.*, vol. 88, pp. 4994-4999, 2000.

[2.148] S. R. Stiffler and M. O. Thompson, “Transient nucleation following pulsed-laser melting of thin silicon films,” *Phys. Rev. B*, vol. 43, pp. 9851-9855, 1991.

[2.149] E. Cortesi, M. K. El-Ghor, H. H. Hosack, L. P. Allen, P. Roitman, and S. J. Krause, "Evaluation of Secco etch technique for determination of dislocationdensities in SIMOX wafers," *in the proceeding of the International IEEE SOI Conference*, 1991, pp. 118-119.

[2.150] D. K. Fork, G. B. Anderson, J. B. Boyce, R. I. Johnson, and P. Mei, "Capillary waves in pulsed excimer laser crystallized amorphous silicon," *Appl. Phys. Lett.*, vol. 68, pp. 2138-2140, 1996.

[2.151] G. Y. Yang, S. H. Hur, and C. H. Han, "A physical-based analytical turn-on model of polysilicon thin-film transistors for circuit simulation," *IEEE Trans. Electron Devices*, vol. 46, pp. 165-172, 1999.

[2.152] J. Y. Seto, "The electrical properties of polycrystalline silicon films," *J. Appl. Phys.*, vol. 46, pp. 5247-5254, 1975.

[2.153] R. Ishihara, "Effects of grain-boundaries on excimer-laser crystallized poly-Si thin-film transistors," in *AMLCD Tech. Dig.*, 2001, pp. 259-260.

[2.154] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys.*, vol. 53, pp. 1193-1202, 1982.

[2.155] Yu-Cheng Chen, Hung-Tse Chen, Chih-Ming Lai, Chi-Lin Chen, Jia-Xing Lin, Jung-Fang Chang, Yu-Rung Liu, "Investigation of Low Roughness Polycrystalline-Silicon and Thin Gate Insulator Thin Film Transistor," in *AMLCD Tech. Dig.*, 2004, pp. 143-146.

[2.156] T. Fujimura, A. Takami, A. Ishida, S. Kawamura, and T. Nishibe, "Reliability improvement of TFTs with thin gate insulator films by smoothing polycrystalline silicon surface roughness," in *AMLCD Tech. Dig.*, 2001, pp. 175-178.

[2.157] Yu-Cheng Chen, Yu-Rung Liu, Jia-Xing Lin, Chi-Lin Chen, Jung-Fang Chang, Yung-Fu Wu, Yung-Hui Yeh, Chai-Yuan Sheu, and Shang-Wen Chang, "Fabrication of Extremely Low Roughness Polycrystalline Silicon and Its Correlation to Device Performance," in *SID Tech. Dig.*, 2003, pp. 216-219.

# Chapter 3

[3.1] S. D. Brotherton, "Polycrystalline silicon thin film transistors," *Semi. Sci. Tech.*, vol. 10, pp 721-738, 1995

[3.2] K. Chung, M. P. Hong, C. W. Kim, and I. Kang, "Needs and solutions of future flat panel display for information technology industry," in *IEDM Tech. Dig.*, 2002, pp. 385-388.

[3.3] Shuichi Uchikoga, "Low-Temperature Polycrystalline Silicon Thin-Film Transistor Technologies for System-on-Glass Displays," in *MRS BULLETIN*, 2002, pp. 881-886.

[3.4] Yasuhisa Oana, "Current and future technology of low-temperature polycrystalline silicon TFT-LCDs," *Journal of the SID*, vol. 9, pp. 169-172, 2001.

[3.5] H. Ohshima, and S. Morozumi, "Future trends for TFT integrated circuits on glass substrates," in *IEDM Tech. Dig.*, 1989, pp. 157-160.

[3.6] H. J. Kim, D. Kim, J. H. Lee, I. G. Kim, G. S. Moon, J. H. Huh, J. W. Hwang, S. Y. Joo, K. W. Kim, and J. H. Souk, "A 7-in. full-color low-temperature poly-Si TFT-LCD," in *SID Tech. Dig.*, 1999, pp. 184-187.

[3.7] Y. I. Park, T. J. Ahn, S. K. Kim, J. Y. Park, J. S. Yoo, C. Y. Kim, and C. D. Kim, "Active matrix OLED displays using simple Poly-Si TFT process," in *SID Tech. Dig.*, 2003, pp. 487-489.

[3.8] Y. Mishima, K. Yoshino, M. Takei, and N. Sasaki, "Characteristics of low-temperature poly-Si TFTs on Al/Glass substrates," *IEEE Trans. Electron Devices*, vol. 48, pp. 1087-1091, June. 2001.

[3.9] I. W. Wu, "Polycrystalline silicon thin film transistors for liquid crystal displays," Solid State Phenomena, 1994, vol. 37~38, pp. 553-564.

[3.10] S. Zhang, R. Han, Z. Zhang, R. Huang, P. K. Ko, and M. Chan, "Implementation of fully self-aligned bottom-gate MOS transistor," *IEEE Electron Device Lett.*, vol. 23, pp. 618-620, 2002.

[3.11] R.S. Shenoy and K.C. Saraswat, "Novel process for fully self-aligned planar ultrathin body Double-Gate FET," in *Proc. of IEEE Internnational SOI conf.*, 2004, pp. 190-191.

[3.12] A. Hara, F. Takeuchi, and N. Sasaki, "Mobility enhancement limit of excimer-laser-crystallized polycrystalline silicon thin film transistors," *J. Appl. Phys.*, vol. 91, pp. 708-714, 2002.

[3.13] J. S. Im, H. J. Kim, and M. O. Thompson, "Phase transformation mechanisms involved on excimer laser crystallization of amorphous silicon films," *Appl. Phys. Lett.*, vol. 63, pp. 1969-1971, 1993.

[3.14] J. S. Im and H. J. Kim, "On the super lateral growth phenomenon observed in excimer laser-induced crystallization of thin Si films," *Appl. Phys. Lett.*, vol. 64, pp. 2303-2305, 1994.

[3.15] M. A. Crowder, P. G. Carey, P. M. Smith, R. S. Sposili, H. S. Cho, and J. S. Im, "Low-temperature single-crystal Si TFT's fabricated on Si films processed via sequential lateral solidification," *IEEE Electron Device Lett.*, vol. 19, pp. 306-308, 1998.

[3.16] Paul Ch. van der Wilt, B. D. van Dijk, G. J. Bertens, R. Ishihara, and C. I. M. Beenakker, "Formation of location-controlled crystalline islands using substrate-embedded seeds in excimer-laser crystallization of silicon films," *Appl. Phys. Lett.*, vol. 79, pp. 1819-1821, 2001.

[3.17] L. Mariucci, R. Carluccio, A. Pecora, V. Foglietti, G. Fortunato, P. Legagneux, D.

Pribat, D. Della Sala, and J. Stoemenos, “Lateral growth control in excimer laser crystallized polysilicon,” *Thin Solid Films*, vol. 337, pp. 137-142, 1999.

[3.18] R. Ishihara, A. Burtsev, and Paul F. A. Alkemade, “Location-control of large Si grains by dual-beam excimer-laser and thick oxide portion,” *Jpn. J. Appl. Phys. Part 1*, vol. 39, pp. 3873-3878, 2000.

[3.19] S. Sakuragi, T. Kudo, K.Yamazaki and T. Asano, “High field effect mobility poly-Si TFTs fabricated by advanced lateral crystal growth process using double-pulsed laser annealing system,” *in the proceeding of the 12th International Display Workshops*, 2005, pp. 965-968.

[3.20] C. H. Kim, I. H. Song, W. J. Nam, and M. K. Han, “A poly-Si TFT fabricated by excimer laser recrystallization on floating active structure,” *IEEE Electron Device Lett.*, vol. 23, pp. 325-327, 2002.

[3.21] A. Hara, M. Takei, F. Takeuchi, K. Suga, K. Yoshino, M. Chida, T. Kakehi, Y. Ebiko, Y. Sano and N. Sasaki, “High performance low temperature polycrystalline silicon thin film transistors on non-alkaline glass produced using diode pumped solid state continuous wave laser lateral crystallization,” *Jpn. J. Appl. Phys. Part 1*, vol. 43, pp. 1269-1276, 2004.

[3.22] M. Tai, M. Hatano, S. Yamaguchi, T. Noda, S. K. Park, T. Shiba, and M. Ohkura, “Performance of poly-Si TFTs fabricated by SELAX,” *IEEE Trans. Electron Devices*, vol. 51, pp. 934-939, June. 2004.

[3.23] Y. Kuo, “A self-aligned, tri-layer, a-Si:H thin film transistor prepared from two photo masks,” *J. Electrochem. Soc.*, vol. 139, pp. 1199–1204, 1992.

[3.24] R. T. Fulks, J. Ho, and J. B. Boyce “A new laser-processed polysilicion TFTs architecture,” *IEEE Electron Device Lett.*, vol. 22, pp. 86-88 , 2001.

[3.25] Z. Xiong, H. Liu, C. Zhu, and J. K. O. Sin, “A new polysilicon CMOS self-aligned double-gate TFT technology,” *IEEE Trans. Electron Devices*, vol. 52, pp. 2629-2633, Dec. 2005.

[3.26] I-Chun Cheng, Alex Z. Kattamis, Ke Long, James C. Sturm, and Sigurd Wagner, “Self-Aligned Amorphous-Silicon TFTs on Clear Plastic Substrates,” *IEEE Electron Device Lett.*, vol. 27, pp. 166-168 , 2006.

[3.27] H. Hayashi, M. Kunii, N. Suzuki, Y. Kanaya, M. Kuki, M. Minegishi, T. Urazono, M. Fujino, T. Noguchi and M. Yamazaki, “Fabrication of Low-Temperature Bottom-Gate Poly-Si TFTs on Large-Area Substrate by Linear-Beam Excimer Laser Crystallization and Ion Doping Method,” in *IEDM Tech. Dig.*, 1995, pp. 829-832.

[3.28] D. B. Thomasson and T. N. Jackson, “Fully self-aligned tri-layer a-Si:H thin-film transistors with deposited doped contact layer,” *IEEE Electron Device Lett.*, vol. 19, pp. 124–126, 1998.

[3.29] C. S. Yang, W. W. Read, C. Arthur, E. Srinivasan, and G. N. Parsons, “Self-aligned gate and source drain contacts in inverted-staggered a-Si:H thin-film transistors fabricated using selective area silicon PECVD,” *IEEE Electron Device Lett.*, vol. 19, pp. 180–182, 1998.

[3.30] D. K. Fork, G. B. Anderson, J. B. Boyce, R. I. Johnson, and P. Mei, “Capillary waves in pulsed excimer laser crystallized amorphous silicon,” *Appl. Phys. Lett.*, vol. 68, pp. 2138-2140, 1996.

[3.31] T. Fujimura, A. Takami, A. Ishida, S. Kawamura, and T. Nishibe, “Reliability improvement of TFTs with thin gate insulator films by smoothing polycrystalline silicon surface roughness,” in *AMLCD Tech. Dig.*, 2001, pp. 175-178.

[3.32] R. Ishihara, “Effects of grain-boundaries on excimer-laser crystallized poly-Si thin-film transistors,” in *AMLCD Tech. Dig.*, 2001, pp. 259-260.

# Chapter 4

[4.1] H. J. Kim, D. Kim, J. H. Lee, I. G. Kim, G. S. Moon, J. H. Huh, J. W. Hwang, S. Y. Joo, K. W. Kim, and J. H. Souk, "A 7-in. full-color low-temperature poly-Si TFT-LCD," in *SID Tech. Dig.*, 1999, pp. 184-187.

[4.2] G. Rajeswaran, M. Itoh, M. Boroson, S. Barry, T. K. Hatwar, K. B. Kahen, K. Yoneda, R. Yokoyama, T. Yamada, N. Komiya, H. Kanno, and H. Takahashi, "Active matrix low temperature poly-Si TFT / OLED full color displays: development status," in *SID Tech. Dig.*, 2000, pp. 974-977.

[4.3] K. Banerjee, S. J. Souri, P Kapur, and K. C. Saraswat, "3-D ICs: a novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proceedings of the IEEE*, vol. 89, pp. 602-633, 2001

[4.4] Y. Helen, R. Dassow, M. Nerding, K. Mourgues, F. Raoult, and J.R. Kohler et al., "High mobility thin film transistors by Nd:YVO4-laser crystallization," *Thin Solid Films*, vol. 383, pp. 143-146, 2001.

[4.5] Z. Meng, M. Wang, and M. Wong, "High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film transistors for system-on-panel applications," *IEEE Trans. Electron Devices*, vol. 47, pp. 404-409, 2000.

[4.6] C. W. Lin, L. J. Cheng, Y. L. Lu, Y. S. Lee, and H. C. Cheng, "High performance low-temperature poly-Si TFTs crystallized by excimer laser irradiation with recessed-channel structure," *IEEE Electron Device Lett.*, vol. 22, pp. 269-271, 2001.

[4.7] S. Zhang, R. Han, J. K. O. Sin, and M. Chan, "Implementation and characterization of self-aligned double-gate TFT with thin channel and thick source/drain," *IEEE Trans. Electron Devices*, vol. 49, no. 5, pp. 718–724, May 2002.

[4.8] H. R. Farrah, R. F. Steinberg, "Analysis of Double-Gate Thin-Film Transistor," *IEEE*

*Trans. Electron Devices*, vol. 14, pp. 69-74, 1967.

[4.9] J.M. Hergenrother, D. Monroe, F. P. Klemens, A. Kornblit, G. R. Weber, W. M. and Mansfield et al., “The vertical replacement-gate (VRG) MOSFET: a 50-nm vertical MOSFET with lithography-independent gate length,” in *IEDM Tech. Dig.*, 1999, pp. 71-74.

[4.10] S. Venkatesan, Gerold W. Neudeck, and Robert F. Pierret, “Dual-Gate Operation and Volume Inversion in n-Channel SO1 MOSFET’s,” *IEEE Electron Device Lett.*, vol. 13, pp. 44-46, 1992.

[4.11] K. W. Guarini, P. M. Solomon, Y. Zhang, K. K. Chan, E. C. Jones, and G. M. Cohen et al., “Triple-self-aligned, planar double-gate MOSFETs: devices and circuits,” in *IEDM Tech. Dig.*, 2001, pp. 415-418.

[4.12] H. S. Philip Wong, Kevin. K. Chan, and Yuan Taur, “Self-aligned (Top and Bottom) double-gate MOSFET with a 25 nm thick silicon channel,” in *IEDM Tech. Dig.*, 1997, pp. 427-430.

[4.13] J. P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys, “Silicon-on-insulator "Gate-all-around device",” in *IEDM Tech. Dig.*, 1990, pp. 595-598.

[4.14] T. Tanaka, H. Horie, S. Ando, and S. Hijiya, “Analysis of $P^+$ poly Si double-gate thin-film SOI MOSFETs,” in *IEDM Tech. Dig.*, 1991, pp. 683-686.

[4.15] D. Hisamoto, W. C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, and K. Asano et al., “A Folded-channel MOSFET for deep-sub-tenth micron era,” in *IEDM Tech. Dig.*, 1998, pp. 1032-1034.

[4.16] C. H. Wann, R. Tu,B. Yu, and C. Hu, “A comparative study of advanced MOSFET structures,” in *VLSI Symp. Tech. Dig.*, 1996, pp. 32-33.

[4.17] Yuan Taur, “An Analytical Solution to a Double-Gate MOSFET with Undoped Body,” *IEEE Electron Device Lett.*, vol. 21, pp. 245-247, 2000.

[4.18] J. S. Im, H. J. Kim, and M. O. Thompson, "Phase transformation mechanisms involved on excimer laser crystallization of amorphous silicon films," *Appl. Phys. Lett.*, vol. 63, pp. 1969-1971, 1993.

[4.19] J. S. Im and H. J. Kim, "On the super lateral growth phenomenon observed in excimer laser-induced crystallization of thin Si films," *Appl. Phys. Lett.*, vol. 64, pp. 2303-2305, 1994.

[4.20] K. Yamaguchi, "Modeling and characterization of polycrystalline-silicon thin-film transistors with a channel-length comparable to a grain size," *J. Appl. Phys.*, vol. 89, pp. 590-595, 2001.

[4.21] M. Kimura, S. Inoue, T. Shimoda, and T. Eguchi, "Dependence of polycrystalline silicon thin-film transistor characteristics on the grain-boundary location," *J. Appl. Phys.*, vol. 89, pp. 596-600, 2001.

[4.22] Robert S. Sposili and James S. Im, "Sequential lateral solidification of thin silicon films on $SiO_2$," *Appl. Phys. Lett.*, vol. 69, pp. 2864-2866, 1996.

[4.23] M. A. Crowder, P. G. Carey, P. M. Smith, R. S. Sposili, H. S. Cho, and J. S. Im, "Low-temperature single-crystal Si TFT's fabricated on Si films processed via sequential lateral solidification," *IEEE Electron Device Lett.*, vol. 19, pp. 306-308, 1998.

[4.24] P. C. van der Wilt, B. D. van Dijk, G. J. Bertens, R. Ishihara, and C. I. M. Beenakker, "Formation of location-controlled crystalline islands using substrate- embedded seeds in excimer-laser crystallization of silicon films," *Appl. Phys. Lett.*, vol. 79, pp. 1819-1821, 2001.

[4.25] L. Mariucci, R. Carluccio, A. Pecora, V. Foglietti, G. Fortunato, and P. Legagneux, D. Pribat et al., "Lateral growth control in excimer laser crystallized polysilicon," *Thin Solid Films*, vol. 337, pp. 137-142, 1999.

[4.26] C. H. Oh, M. Ozawa, and M. Matsumura, "A novel phase-modulated excimer-laser crystallization method of silicon thin films," *Jpn. J. Appl. Phys. Part 2*, vol. 37, pp. L492-L495, 1998.

[4.27] R. Ishihara, and A. Burtsev, "Location Control of Large Grain Following Excimer-Laser Melting of Si Thin-Films," *Jpn. J. Appl. Phys. Part 1*, vol. 37, pp. 1071-1075, 1998.

[4.28] K.Yamazaki, T. Kudo, K. Seike, D. Ichishima and C. G. Jin, "Double-pulsed laser annealing system and polycrystallization with green DPSS laser," in *AMLCD Tech. Dig.*, 2002, pp. 149-152.

[4.29] S. Sakuragi, T. Kudo, K.Yamazaki and T. Asano, "High field effect mobility poly-Si TFTs fabricated by advanced lateral crystal growth process using double-pulsed laser annealing system," *in the proceeding of the 12th International Display Workshops*, 2005, pp. 965-968.

[4.30] C. H. Kim, I. H. Song, W. J. Nam, and M. K. Han, "A poly-Si TFT fabricated by excimer laser recrystallization on floating active structure," *IEEE Electron Device Lett.*, vol. 23, pp. 325-327, 2002.

[4.31] A. Hara, F. Takeuchi, and N. Sasaki, "Selective single-crystalline-silicon growth at the pre-defined active regions of TFTs on a glass by a scanning CW laser irradiation," in *IEDM Tech Dig, 2000*, pp.209-212.

[4.32] A. Hara, M. Takei, F. Takeuchi, K. Suga, K. Yoshino, and M. Chida et al., "High performance low temperature polycrystalline silicon thin film transistors on non-alkaline glass produced using diode pumped solid state continuous wave laser lateral crystallization," *Jpn. J. Appl. Phys. Part 1*, vol. 43, pp. 1269-1276, 2004.

[4.33] M. Hatano, and T. Shiba, "Selectively enlarging laser crystallization technology for high and uniform performance poly-Si TFTs," in *SID Tech Dig, 2002*, pp.158-161.

[4.34] M. Tai, M. Hatano, S. Yamaguchi, T. Noda, S. K. Park, and T. Shiba et al., "Performance of poly-Si TFTs fabricated by SELAX," *IEEE Trans. Electron Devices*, vol. 51, pp. 934-939, June. 2004.

[4.35] D. K. Fork, G. B. Anderson, J. B. Boyce, R. I. Johnson, and P. Mei, "Capillary waves in pulsed excimer laser crystallized amorphous silicon," *Appl. Phys. Lett.*, vol. 68, pp. 2138-2140, 1996.

[4.36] David Esseni, Marco Mastrapasqua, George K. Celler, Claudio Fiegna, Luca Selmi, and Enrico Sangiorgi, "An experimental study of mobility enhancement in ultrathin SOI transistors operatedin double-gate mode," *IEEE Trans. Electron Devices*, vol. 50, pp. 802-808, March. 2003.

[4.37] S. Zhang, R. Han, J. K. O. Sin, and M. Chan, "Reduction of Off-Current in Self-Aligned Double-Gate TFT With Mask-Free Symmetric LDD", *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 1490-1492, August. 2002.

[4.38] K. Tanaka, H. Arai, and S. Kohda, "Characteristics of offset-structure polycrystalline-silicon thin-film transistors," *IEEE Electron Device Lett.*, vol. 9, pp. 23-25, 1988.

[4.39] S. D. Zhang, R. Han, and M. J. Chan, "A novel self-aligned bottom gate poly-Si TFT with in-situ LDD," *IEEE Electron Device Lett.*, vol. 22, pp. 393-395, 2001.

[4.40] J. I. Han and C. H. Han, "A self-aligned offset polysilicon thin-film transistor using photoresist reflow," *IEEE Electron Device Lett.*, vol. 20, pp. 476-478, 1999.

[4.41] K. Y. Choi, J. W. Lee, and M. K. Han, "Gate-overlapped lightly doped drain poly-Si thin-film transistors for large area-AMLCD," *IEEE Trans. Electron Devices*, vol. 45, pp. 1272-1279, 1998.

[4.42] M. Hatano, H. Akimoto, and T. Sakai, "A novel self-aligned gate-overlapped LDD poly-Si TFT with high reliability and performance," in *IEDM Tech. Dig.*, 1997, pp. 523-526.

[4.43] K. Ohgata, Y. Mishima, and N.Sasaki, "A new dopant activation technique for poly-Si TFTs with a self-aligned gate-overlapped LDD structure," in *IEDM Tech. Dig.*, 2000, pp. 205-208.

[4.44] A. Valletta, Luigi Mariucci, Guglielmo Fortunato, S. D. Brotherton, and J. R. Ayres, "Hot carrier-induced degradation of gate overlapped lightly doped drain (GOLDD) polysilicon TFTs," *IEEE Trans. Electron Devices*, vol. 49, pp. 636-642, 2002.

[4.45] S. Zhang, C. Zhu, Johnny K. O. Sin, and Philip K. T. Mok, "A novel ultrathin elevated channel low-temperature poly-Si TFT," *IEEE Electron Device Lett.*, vol. 20, pp. 569-571, 1999.

[4.46] L. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys.*, vol. 53, pp. 1193-1202, 1982.

[4.47] R. E. Proano, R. S. Misage, and D. G. Ast, "Development and electrical properties of undoped polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 36, pp. 1915-1922, Sept. 1989.

[4.48] J. Y. Seto, "The electrical properties of polycrystalline silicon films," *J. Appl. Phys.*, vol. 46, pp.5247-5254, 1975.

[4.49] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys.*, vol. 53, pp. 1193-1202, 1982.

[4.50] S. M. Sze, *Physics of semiconductor devices* $2^{nd}$ *ed.*, John Wiley & Sons, New York, 1981.

# Chapter 5

[5.1] H. J. Kim, D. Kim, J. H. Lee, I. G. Kim, G. S. Moon, J. H. Huh, J. W. Hwang, S. Y. Joo, K. W. Kim, and J. H. Souk, "A 7-in. full-color low-temperature poly-Si

TFT-LCD," in *SID Tech. Dig.*, 1999, pp. 184-187.

[5.2] Tatsuya Sasaoka, Mitsunobu Sekiya, Akira Yumoto, Jiro Yamada, Takashi Hirano, Yuichi Iwase, Takao Yamada, Tadashi Ishibashi, Takao Mori, Mitsuru Asano, Shinichiro Tamura, and Tetsuo Urabe, "A 13.0-inch AM-OLED display with top emitting structure and adaptive current mode programmed pixel circuit (TAC)," in *SID Tech. Dig.*, 2001, pp. 384-387.

[5.3] A. Hara, F. Takeuchi, and N. Sasaki, "Mobility enhancement limit of excimer-laser-crystallized polycrystalline silicon thin film transistors," *J. Appl. Phys.*, vol. 91, pp. 708-714, 2002.

[5.4] James S. Im, H. J. Kim, and Michael O. Thompson, "Phase transformation mechanisms involved on excimer laser crystallization of amorphous silicon films," *Appl. Phys. Lett.*, vol. 63, pp. 1969-1971, 1993.

[5.5] James S. Im and H. J. Kim, "On the super lateral growth phenomenon observed in excimer laser-induced crystallization of thin Si films," *Appl. Phys. Lett.*, vol. 64, pp. 2303-2305, 1994.

[5.6] Robert S. Sposili and James S. Im, "Sequential lateral solidification of thin silicon films on $SiO_2$," *Appl. Phys. Lett.*, vol. 69, pp. 2864-2866, 1996.

[5.7] M. A. Crowder, P. G. Carey, P. M. Smith, Robert S. Sposili, Hans S. Cho, and James S. Im, "Low-temperature single-crystal Si TFT's fabricated on Si films processed via sequential lateral solidification," *IEEE Electron Device Lett.*, vol. 19, pp. 306-308, 1998.

[5.8] R. Dassow, J. R. Köhler, Y. Helen, K. Mourgues, O. Bonnaud, T. Mohammed-Brahim and J. H. Werner, "Laser crystallization of silicon for high-performance thin-film transistors," *Semicond. Sci. Technol*, vol. 15, pp. L31-L34, 2000.

[5.9] J. Y. Park, H. H. Park, K. Y. Lee and H. K. Chung, "Design of Sequential Lateral Solidification Crystallization Method for Low Temperature Poly-Si Thin Film

Transistors," *Jpn. J. Appl. Phys. Part 2*, vol. 43, pp.1280-1286, 2004.

[5.10] C. H. Oh, M. Ozawa, and M. Matsumura, "A novel phase-modulated excimer-laser crystallization method of silicon thin films," *Jpn. J. Appl. Phys. Part 2*, vol. 37, pp. L492-L495, 1998.

[5.11] C. H. Oh and M. Matsumura, "A proposed single grain-boundary thin-film transistor," *IEEE Electron Device Lett.*, vol. 22, pp. 20-22, 2001.

[5.12] M. Jyumonji, Y. Kimura, Y. Taniguchi, M. Hiramatsu, H. Ogawa and M. Matsumura, "Optimum Light Intensity Distribution for Growing Large Si Grains by Phase-Modulated Excimer-Laser Annealing," *Jpn. J. Appl. Phys. Part 1*, vol. 43, pp. 739-744, 2004.

[5.13] Paul Ch. van der Wilt, B. D. van Dijk, G. J. Bertens, R. Ishihara, and C. I. M. Beenakker, "Formation of location-controlled crystalline islands using substrate-embedded seeds in excimer-laser crystallization of silicon films," *Appl. Phys. Lett.*, vol. 79, pp. 1819-1821, 2001.

[5.14] R. Ishihara, Y. Hiroshima, D. Abe, B. D. van Dijk, P. C. van der Wilt, S. Higashi, S. Inoue, T. Shimoda, J.W. Metselaar, and C. I. M. Beenakker, "Single-grain Si TFTs with ECR-PECVD gate $SiO_2$," *IEEE Trans. Electron Devices*, vol. 51, pp.500-502, 2004.

[5.15] R. Ishihara, Paul Ch. van der Wilt, B. D. van Dijk, J. W. Metselaar and C. I. M. Beenakker, in *Poly-Silicon Thin Film Transistor Technology and Applications in Displays and Other Novel Technology Areas,* Apostolos T. Voutsas, Editor, Vol. 5004, p. 10, SPIE Proceeding Series (2003).

[5.16] C. H. Kim, I. H. Song, W. J. Nam, and M. K. Han, "A poly-Si TFT fabricated by excimer laser recrystallization on floating active structure," *IEEE Electron Device Lett.*, vol. 23, pp. 325-327, 2002.

[5.17] I. H. Song, S. H. Kang, W. J. Nam, and M. K. Han, "A high-performance multichannel dual-gate poly-Si TFT fabricated by excimer laser irradiation on a floating a-Si thin film," *IEEE Electron Device Lett.*, vol. 24, pp. 580-582, 2003.

[5.18] A. Hara, K. Yoshino, F. Takeuchi and N. Sasaki, "Selective Single-Crystalline-Silicon Growth at the Pre-defined Active Region of a Thin Film Transistor on Glass by Using Continuous Wave Laser Irradiation," *J. Appl. Phys. Part 1*, vol. 42, pp. 23-27, 2003.

[5.19] A. Hara, M. Takei, F. Takeuchi, K. Suga, K. Yoshino, M. Chida, T. Kakehi, Y. Ebiko, Y. Sano and N. Sasaki, "High Performance Low Temperature Polycrystalline Silicon Thin Film Transistors on Non-alkaline Glass Produced Using Diode Pumped Solid State Continuous Wave Laser Lateral Crystallization," *Jpn. J. Appl. Phys. Part 1*, vol. 43, pp. 1269-1276, 2004.

[5.20] M. Tai, M. Hatano, S. Yamaguchi, T. Noda, S. K. Park, T. Shiba, and M. Ohkura, "Performance of poly-Si TFTs fabricated by SELA," *IEEE Trans. Electron Devices*, vol. 51, pp. 934-939, 2004.

[5.21] D. K. Fork, G. B. Anderson, J. B. Boyce, R. I. Johnson, and P. Mei, "Capillary waves in pulsed excimer laser crystallized amorphous silicon," *Appl. Phys. Lett.,* vol. 68, pp. 2138-2140, 1996.

[5.22] M .H .Lee, S. J. Moon, M. Hatano, K. Suzuki, and C. P. Grigoropoulos, "Relationship between fluence gradient and lateral grain growth in spatially controlled excimer laser crystallization of amorphous silicon films," *J. Appl. Phys.*, vol. 88, pp. 4994-4999, 2000.

# Chapter 6

[6.1] H. J. Kim, D. Kim, J. H. Lee, I. G. Kim, G. S. Moon, J. H. Huh, J. W. Hwang, S. Y. Joo, K. W. Kim, and J. H. Souk, "A 7-in. full-color low-temperature poly-Si

TFT-LCD," in *SID Tech. Dig.*, 1999, pp. 184-187.

[6.2] G. Rajeswaran, M. Itoh, M. Boroson, S. Barry, T. K. Hatwar, K. B. Kahen, K. Yoneda, R. Yokoyama, T. Yamada, N. Komiya, H. Kanno, and H. Takahashi, "Active matrix low temperature poly-Si TFT / OLED full color displays: development status," in *SID Tech. Dig.*, 2000, pp. 974-977.

[6.3] M. Miyasaka, "Suftla Flexible Microelectronics on Their Way to Business," in *SID Tech. Dig.*, 2007, pp. 1673-1676.

[6.4] K. Banerjee, S. J. Souri, P Kapur, and K. C. Saraswat, "3-D ICs: a novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proceedings of the IEEE*, vol. 89, pp. 602-633, 2001

[6.5] S. Jagar, M. Chan, M.C. Poon, H. Wang, M. Qin, P. K. KO, Y. Wang, "Single Grain Thin-Film-Transistor (TFT) with SOI CMOS Performance Formed by Metal-Induced-Lateral-Crystallization," in *IEDM Tech. Dig.*, 1999, pp. 293-296.

[6.6] M. Wong, Z. Jin, G. A. Bhat, P. C. Wong, H. S. Kwok, "Characterization of the MIC/MILC Interface and Its Effects on the Performance of MILC Thin-Film Transistors," *IEEE Trans. Electron Devices*, vol. 47, pp.1061-1067, 2000.

[6.7] A. Hara, F. Takeuchi, and N. Sasaki, "Mobility enhancement limit of excimer-laser-crystallized polycrystalline silicon thin film transistors," *J. Appl. Phys.*, vol. 91, pp. 708-714, 2002.

[6.8] J. Y. Seto, "The electrical properties of polycrystalline silicon films," *J. Appl. Phys.*, vol. 46, pp. 5247-5254, 1975.

[6.9] James S. Im and H. J. Kim, "On the super lateral growth phenomenon observed in excimer laser-induced crystallization of thin Si films," *Appl. Phys. Lett.*, vol. 64, pp. 2303-2305, 1994.

[6.10] Robert S. Sposili and James S. Im, "Sequential lateral solidification of thin silicon films on $SiO_2$," *Appl. Phys. Lett.*, vol. 69, pp. 2864-2866, 1996.

[6.11] M. A. Crowder, P. G. Carey, P. M. Smith, Robert S. Sposili, Hans S. Cho, and James S. Im, “Low-temperature single-crystal Si TFT’s fabricated on Si films processed via sequential lateral solidification,” *IEEE Electron Device Lett.*, vol. 19, pp. 306-308, 1998.

[6.12] Chang-Ho Oh, Motohiro Ozawa, and Masakiyo Matsumura, “A novel phase-modulated excimer-laser crystallization method of silicon thin films,” *Jpn. J. Appl. Phys. Part 2*, vol. 37, pp. L492-L495, 1998.

[6.13] Y. Taniguchi, M. Matsumura, M. Jyumonji, H. Ogawa, and M. Hiramatsu,” Novel Phase Modulator for ELA-Based Lateral Growth of Si,’ *J. Electrochem. Soc.*, vol. 153, pp. G67-G71, 2006.

[6.14] Paul Ch. van der Wilt, B. D. van Dijk, G. J. Bertens, R. Ishihara, and C. I. M. Beenakker, “Formation of location-controlled crystalline islands using substrate-embedded seeds in excimer-laser crystallization of silicon films,” *Appl. Phys. Lett.*, vol. 79, pp. 1819-1821, 2001.

[6.15] R. Ishihara, P. C. van der Wilt, B. D. van Dijk, J. W. Metselaar and C. I. M. Beenakker, in *Poly-Silicon Thin Film Transistor Technology and Applications in Displays and Other Novel Technology Areas,* Apostolos T. Voutsas, Editor, Vol. 5004, p. 10, SPIE Proceeding Series (2003).

[6.16] C. H. Kim, I. H. Song, W. J. Nam, and M. K. Han, “A poly-Si TFT fabricated by excimer laser recrystallization on floating active structure,” *IEEE Electron Device Lett.*, vol. 23, pp. 325-327, 2002.

[6.17] J. H. Jeon, M. C. Lee, K. C. Park, S. H. Jung and M. K. Han, “A new poly-Si TFT with selectively doped channel fabricated bynovel excimer laser annealing,” in *IEDM Tech. Dig.,* 2000 , pp.. 213-216.

[6.18] C. W. Lin, L. J. Cheng, Y. L. Lu, Y. S. Lee, and H. C. Cheng, “High performance low-temperature poly-Si TFTs crystallized by excimer laser irradiation with recessed-channel structure," *IEEE Electron Device Lett.*, vol. 22, pp.269-271, 2001.

[6.19] J. X. Lin, C. C. Chen, Y. C. Chen, W. C. Yeh and Y. C. Liu, "Fabrication of large-grained poly-silicon thin film by heat-retaining enhanced crystallization," in *AMLCD Tech. Dig.*, 2004, pp. 157-160.

[6.20] Hideki Asada, "Low-Power System-on-Glass LCD Technologies," in *SID Tech. Dig.*, 2005, pp. 1434-1437.

[6.21] Nobuo Karaki, Takashi Nanmoto, Hiroaki Ebihara, Satoshi Inoue, and Tatsuya Shimoda, "A Flexible 8-bit Asynchronous Microprocessor Based on Low-Temperature Poly-Silicon (LTPS) TFT Technology," in *SID Tech. Dig.*, 2005, pp. 1430-1433.

[6.22] Y. Toyota, M. Matsumura, M. Hatano, T. Shiba, T. Itoga, and M. Ohkura, "Integration of Reliability with High Current Drivability by using SELAX Technology for High-Resolution (>300 ppi) System-in-Displays," in *SID Tech. Dig.*, 2005, pp. 1439-1441.

[6.23] Yoshiharu Nakajima, Yoshitoshi Kida, Masaki Murase, Yoshihiko Toyoshima, and Yasuhito Maki, "Latest Development of "System-on-Glass" Display with Low Temperature Poly-Si TFT," in *SID Tech. Dig.*, 2004, pp. 864-867.

[6.24] C.-W. Kim, K.-C. Moon, H.-J. Kim, K.-C. Park, C.-H. Kim, I.-G. Kim, C.-M. Kim, S.-Y. Joo, J.-K. Kang, and U.-J. Chung, "Development of SLS-Based System on Glass Display," in *SID Tech. Dig.*, 2004, pp. 868-871.

[6.25] Y. Matsueda, S. Inoue, and T. Shimoda, "Concept of system on panel," in *AMLCD Tech. Dig.*, 2001, pp. 77-80.

[6.26] T. Nishibe and H. Nakamura, "Value-Added Circuit and Function Integration for SOG (System-on Glass) Based on LTPS Technology," in *SID Tech. Dig.*, 2006, pp. 1091-1094.

[6.27] Y. Yamamoto, T. Matsuo, and H. Komiya, "CG Silicon Technology and System

Integration for Mobile Applications," in *SID Tech. Dig.*, 2006, pp. 1173-1176.

[6.28] Y. Nakajima, Y. Teranishi, Y. Kida, and Y Maki, "Ultra-Low-Power LTPS TFT-LCD Technology Using a Multi-Bit Pixel Memory Circuit," *in SID Tech. Dig.*, 2006, pp. 1185-1188.

[6.29] W. C. Yeh, D. Y. Ke, and C. J. Zhuang, "Enlargement of Grain Size and Location Control of Grain in Excimer-laser Crystallization of Si Film," *in Mater. Res. Soc. Symp. Proc.*, vol. 910, Symposium A, pp. 0910-A14-01, 2006.

[6.30] H. Kumomi, "Location control of crystal grains in excimer laser crystallization of silicon thin films," *Appl. Phys. Lett.*, vol. 83, pp. 434-436, 2003.

[6.31] Hideya Kumomi, Chihiro Shin, Gou Nakagawa, and Tanemasa Asano, "Single-grain TFTs on location-controlled crystal grains formed by excimer laser crystallization of Si thin films," in *IEDM Tech Dig.*, 2004, pp.773-776.

[6.32] P. C. van der Wilt, B. A. Turk, A. B. Limanov, A. M. Chitu, and J. S. Im, in *IDMC* Symposium Digest, p. 150-152 (2005).

[6.33] I. H. Song, S. H. Kang, W. J. Nam, and M. K. Han, "A high-performance multichannel dual-gate poly-Si TFT fabricated by excimer laser irradiation on a floating a-Si thin film," *IEEE Electron Device Lett.*, vol. 24, pp. 580-582, 2003.

[6.34] S. Sakuragi, T. Kudo, K.Yamazaki and T. Asano, "High field effect mobility poly-Si TFTs fabricated by advanced lateral crystal growth process using double-pulsed laser annealing system," *in the proceeding of the 12th International Display Workshops*, 2005, pp. 965-968.

[6.35] F. Okumura, "SOG technologies in NEC," *in the proceeding of the International Display Manufacture Conference*, 2005, pp. 311-314.

[6.36] A. Hara, F. Takeuchi, and N. Sasaki, "Selective single-crystalline-silicon growth at the pre-defined active regions of TFTs on a glass by a scanning CW laser irradiation," in *IEDM Tech Dig.*, 2000, pp.209-212.

[6.37] M. Hatano, and T. Shiba "Selectively enlarging laser crystallization technology for high and uniform performance poly-Si TFTs," in *SID Symposium Digest*, 2002, pp. 158-161.

[6.38] Kenji Makihira, Masahito Yoshii and Tanemasa Asano, "CMOS Application of Single-Grain Thin Film Transistor Produced Using Metal Imprint Technology," *Jpn. J. Appl. Phys.*, vol. **42**, pp. 1983-1987, 2003.

[6.39] H. Kuriyama, S. Kiyama, S. Noguchi, T. Kuwahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, H. Kawata, M. Osumi, S. Tsuda, S. Nakano, and Y. Kuwano, "Enlargement of poly-Si film grain size by excimer laser annealing and its application to high-performance poly-Si thin film transistor," *Jpn. J. Appl. Phys.*, vol. **30**, pp. 3700-3703, 1991.

[6.40] M .H .Lee, S. J. Moon, M. Hatano, K. Suzuki, and C. P. Grigoropoulos, "Relationship between fluence gradient and lateral grain growth in spatially controlled excimer laser crystallization of amorphous silicon films," *J. Appl. Phys.*, vol. 88, pp. 4994-4999, 2000.

[6.41] G. K. Giust and T. W. Sigmon, "Comparison of excimer laser recrystallized prepatterned and unpatterned silicon films on $SiO_2$," *J. Appl. Phys.*, vol. 81, pp. 1204-1211, 1997.

[6.42] R. Ishihara, A. Burtsev, and Paul F. A. Alkemade, "Location-Control of Large Si Grains by Dual-Beam Excimer-Laser and Thick Oxide Portion," *Jpn. J. Appl. Phys. Part 1*, **39**, 3872 (2000).

[6.43] D. K. Fork, G. B. Anderson, J. B. Boyce, R. I. Johnson, and P. Mei, "Capillary waves in pulsed excimer laser crystallized amorphous silicon," *Appl. Phys. Lett.*, vol. 68, pp. 2138-2140, 1996.

# Chapter 7

[7.1] H. Kuriyama, S. Kiyama, S. Noguchi, T. Kuwahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, S. Tsuda, and S. Nakano, ”High mobility poly-Si TFT by a new excimer laser annealing method for large area electronics,” in *IEDM Tech. Dig.*, 1991, pp. 563-566.

[7.2] J. R. Ayres, “Low temperature poly-Si active matrix LCDs,” *IEE Colloquium on Novel Display Technologies*, 1995, pp. 3/1.

[7.3] A. Kohno, T. Sameshima, N. Sano, M. Sekiya, and M. Hara, “High performance poly-Si TFTs fabricated using pulsed laser annealing and remote plasma CVD with low temperature processing,” *IEEE Trans. Electron Devices*, vol. 42, pp. 251-257, 1995.

[7.4] Hiroyuki Ohshima and Marcel Führen, “High-Performance LTPS Technologies for Advanced Mobile Display Applications,” in *SID Tech. Dig.*, 2007, pp. 1482-1485.

[7.5] Y. Yamamoto, T. Matsuo, and H. Komiya, “CG Silicon Technology and System Integration for Mobile Applications,” in *SID Tech. Dig.*, 2006, pp. 1173-1176.

[7.6] James S. Im, H. J. Kim, and Michael O. Thompson, “Phase transformation mechanisms involved on excimer laser crystallization of amorphous silicon films,” *Appl. Phys. Lett.*, vol. 63, pp. 1969-1971, 1993.

[7.7] James S. Im and H. J. Kim, “On the super lateral growth phenomenon observed in excimer laser-induced crystallization of thin Si films,” *Appl. Phys. Lett.*, vol. 64, pp. 2303-2305, 1994.

[7.8] C. F. Cheng, M. C. Poon, C. W. Kok, and Mansun. Chan, “Impact of transistor-to-grain size statistics on large-grained polysilicon TFT characteristics,” in *IEDM Tech Dig.*, 2004, pp.789-792.

[7.9] Mutsumi Kimura, Satoshi Inoue, Tatsuya Shimoda, and Tsukasa Eguchi, "Dependence of polycrystalline silicon thin-film transistor characteristics on the grain-boundary location," *J. Appl. Phys.*, vol. 89, pp. 596-600, 2001.

[7.10] H. J. Kim and James S. Im, "Multiple pulse irradiation effects in excimer laser-induced crystallization of amorphous Si films," *Mat. Res. Soc. Symp. Proc.*, vol. 321, pp. 665-670, 1994.

[7.11] Ken Yamaguchi, "Modeling and characterization of polycrystalline-silicon thin-film transistors with a channel-length comparable to a grain size," *J. Appl. Phys.*, vol. 89, pp. 590-595, 2001.

[7.12] S. Yura, A. Sono, T. Okamoto, Y. Sato, T. Kojima, J. Nishimae, M. Inoue, and K. Motonami, "Crystallization of amorphous Si films by a pulsed YAG2ω green laser for polycrystalline Si TFT fabrication ," *in the proceeding of the International Display Manufacture Conference*, 2005, pp. 142-145.

[7.13] M. Hatano, and T. Shiba "Selectively enlarging laser crystallization technology for high and uniform performance poly-Si TFTs," *in SID Symposium Digest*, 2002, pp. 158-161.

[7.14] M. Matsumura, M. Hatano, T. Kaitoh, and M. Ohkura, "Subthreshold properties of TFTs with laser-crystallized laterally grown polysilicon layers," *IEEE Electron Device Lett.*, vol. 27, pp. 278-280, 2006.

[7.15] M. Tai, M. Hatano, S. Yamaguchi, T. Noda, S. K. Park, T. Shiba, and M. Ohkura, "Performance of poly-Si TFTs fabricated by SELA," *IEEE Trans. Electron Devices*, vol. 51, pp. 934-939, 2004.

[7.16] M. Hatano, T. Sato, M. Matsumura, Y. Toyota, M. Tai, M. Ohkura, and T. Miyazawa, "System on glass display with LTPS TFTs formed using SELAX technology" *in the proceeding of the 12th International Display Workshops*, 2005, pp. 953-956.

[7.17] M. Tai, T. Sato, M. Matsumura, M. Hatano, and M. Ohkura, "Relationship between Mobility and Configuration of Thin-Film Transistor Fabricated with Laterally-Grown

Polycrystalline Silicon Layer” in *AMLCD Tech. Dig.*, 2007, pp. 205-206.

[7.18] Y. Toyota, M. Matsumura, M. Hatano, and T. Shiba, “Integration of Reliability with High Current Drivability by using SELAX Technology for High-Resolution (>300 ppi) System-in-Displays,” in *SID Tech. Dig.*, 2005, pp. 1439-1441.

[7.19] Y. Sugawara, Y. Uraoka, H. Yano, T. Hatayama, T. Fuyuki, and A. Mimura, **“**Crystallization of double-layered silicon thin films by solid green laser annealing for high performance thin film transistors,” in *AMFPD Tech. Dig.*, 2007, pp. 25-28.

[7.20] Kuniaki Matsuki, Ryusuke Saito, Shuji Tsukamoto, Mutsumi Kimura, Yuta Sugawara and Yukiharu Uraoka, **“**Analysis of Laser Crystallization of Double-Layered poly-Si Thin Films using Process Simulation of Laser Crystallization,” in *AMFPD Tech. Dig.*, 2007, pp. 199-200.

[7.21] N. Kawamoto, T. Miyoshi, N. Matsuo, T. Fujiwara, H. Ishikawa, K. Ueno, and A. Heya, **“**A concept of visible laser induced lateral crystallization,” in *AMFPD Tech. Dig.*, 2007, pp. 255-258.

[7.22] N. Kawamoto, T. Miyoshi, N. Matsuo, H. Ishikawa, T. Fujiwara, K. Ueno, and A. Heya, **“**Influence of wavelength on laser crystallization of amorphous Si film,” in *AMFPD Tech. Dig.*, 2007, pp. 163-167.

[7.23] K.Yamazaki, T. Kudo, K. Seike, D. Ichishima and C. G. Jin, “Double-pulsed laser annealing system and polycrystallization with Green DPSS lasers ” in *AMLCD Tech. Dig.*, 2002, pp. 149-152.

[7.24] S. Sakuragi, T. Kudo, K.Yamazaki and T. Asano, “High field effect mobility poly-Si TFTs fabricated by advanced lateral crystal growth process using double-pulsed laser annealing system,” *in the proceeding of the 12th International Display Workshops*, 2005, pp. 965-968.

[7.25] T. Kudo, K. Seike, K.Yamazaki, H. Komori, S. Yawaka, S. Hamada, and C. G. Jin, “Advanced lateral crystal growth of a-Si thin films by Double-pulsed irradiation od all solid-state lasers ” in *Mat. Res. Soc. Symp. Proc.*, vol. 762, pp. A16.5.1-A16.5.6 , 2003.

[7.26] Y. Helen, , R. Dassow, M. Nerding, K. Mourgues, F. Raoult, J.R. K¨ohler,T. Mohammed-Brahim, R. Rogel, O. Bonnaud, J.H. Werner, H.P. Strunk, “High mobility thin film transistors by Nd:YVO4-laser crystallization,” *Thin Solid Films*, vol. 383, pp. 143-146, 2001.

[7.27] M. Nerding, S. Christiansen, J. Krinke, R. Dassow, J. R. Köhler, J. -H. Werner and H. -P. Strunk, “Grain populations in laser-crystallised silicon thin films on glass substrates,” *Thin Solid Films*, vol. 383, pp. 110-112, 2001.

[7.28] J. H. Werner, R. Dassow, T. J. Rinke, J. R. Köhler and R. B. Bergmann, “From polycrystalline to single crystalline silicon on glass,” *Thin Solid Films*, vol. 383, pp. 95-100, 2001.

[7.29] F. Falk, and G. Andrä, “Laser crystallization — a way to produce crystalline silicon films on glass or on polymer substrates,” *Journal of Crystal Growth*, vol. 287, pp. 397-401, 2006.

[7.30] G. Andrä, J. Bergmann and F. Falk, “Laser crystallized multicrystalline silicon thin films on glass,” *Thin Solid Films*, vol. 487, pp. 77-80, 2005.

[7.31] A. Saboundji, T. Mohammed-Brahim, G. Andrä, J. Bergmann and F. Falk, “Thin film transistors on large single crystalline regions of silicon induced by cw laser crystallization,” *Journal of Crystal Growth*, vol. 338-340, pp. 758-761, 2004.

[7.32] A. Hara, F. Takeuchi, and N. Sasaki, “Selective single-crystalline-silicon growth at the pre-defined active regions of TFTs on a glass by a scanning CW laser irradiation,” in *IEDM Tech Dig.*, 2000, pp.209-212.

[7.33] A. Hara, M. Takei, F. Takeuchi, K. Suga, K. Yoshino, M. Chida, T. Kakehi, Y. Ebiko, Y. Sano and N. Sasaki, “High Performance Low Temperature Polycrystalline Silicon Thin Film Transistors on Non-alkaline Glass Produced Using Diode Pumped Solid

State Continuous Wave Laser Lateral Crystallization," *Jpn. J. Appl. Phys. Part 1*, vol. 43, pp. 1269-1276, 2004.

[7.34] A. Hara, M. Takei, K. Yoshino, F. Takeuchi and N. Sasaki, "Self-Aligned Metal Double-Gate Low-Temperature Polycrystalline Silicon Thin-Film Transistors on Non-Alkali Glass Substrate Using Diode-Pumped Solid-State Continuous Wave Laser Lateral Crystallization," *Jpn. J. Appl. Phys.*, vol. 43, pp. L790-L793, 2004.

[7.35] A. Hara, F. Takeuchi, M. Takei, K. Suga, K. Yoshino, M. Chida, Y. Sano and N. Sasaki, "High-Performance Polycrystalline Silicon Thin Film Transistors on Non-Alkali Glass Produced Using Continuous Wave Laser Lateral Crystallization," *Jpn. J. Appl. Phys.*, vol. 41, pp. L311-L313, 2002.

[7.36] A. Hara, K. Yoshino, F. Takeuchi, and N. Sasaki, "Selective Single-Crystalline-Silicon Growth at the Pre-defined Active Region of a Thin Film Transistor on Glass by Using Continuous Wave Laser Irradiation," *Jpn. J. Appl. Phys.*, vol. 42, pp. 23-27, 2003.

[7.37] K. Kitahara, Y. Ohashi, Y. Katoh, A. Hara and N. Sasaki, "Submicron-scale characterization of poly-Si thin films crystallized by excimer laser and continuous-wave laser," *J. Appl. Phys.*, vol. 95, pp. 7850-7855, 2004.

[7.38] Y. Sano, M. Takei, A. Hara, and N. Sasaki, "High-Performance Single-Crystalline-Silicon TFTs on a Non-Alkali Glass Substrate," in *IEDM Tech Dig.*, 2002, pp.565-568.

[7.39] A. Hara, Y. Mishima, T. Kakehi, F. Takeuchi, M. Takei, K. Yoshino, K. Suga, M. Chida, and N. Sasaki, "High Performance Poly-Si TFTs on a Glass by a Stable Scanning CW Laser Lateral Crystallization," in *IEDM Tech Dig.*, 2001, pp.747-750.

[7.40] A. Hara, M. Takei, K. Yoshino, F. Takeuchi, M. Chida, and N. Sasaki, "Self-Aligned Top and Bottom Metal Double Gate Low Temperature Poly-Si TFT Fabricated at 550 ℃ on Non-Alkali Glass Substrate by Using DPSS CW Laser Lateral Crystallization

Method," in *IEDM Tech Dig.*, 2003, pp.211-214.

[7.41] N. Sasaki, A. Hara, F. Takeuchi, Y. Mishima, T. Kakehi, K. Yoshino, and M. Takei, "High Throughput CW-Laser Lateral Crystallization for Low-Temperature Poly-Si TFTs and Fabrication of 16 bit SRAMs and 270MHz Shift Registers," in *SID Tech. Dig.*, 2002, pp. 154-157.

[7.42] T. Yoshida, K. Yoshino, M. Takei, A. Hara, N. Sasaki, and T. Tsuchiya, "Experimental evidence of grain-boundary related hot-carrier degradation mechanism in low-temperature poly-Si thin-film-transistors," in *IEDM Tech Dig.*, 2003, pp.219-222.

[7.43] F. Takeuchi, A. Hara and N. Sasaki, "Performance of poly-Si TFT using the CW laser lateral crystallization (CLC) ," *in the proceeding of the International Display Manufacture Conference*, 2002, session 7.3.

[7.44] K. Kitahara, R. Yamazaki, T. Kurosawa1, K. Nakajima, and A. Moritani, "Analysis of Stress in Laser-Crystallized Polysilicon Thin Films by Raman Scattering Spectroscopy," *Jpn. J. Appl. Phys.*, vol. 41, pp. 5055-5059, 2002.

# Publication Lists

## International Journal:

[1] （新--3 點，A 類長文） Huang-Chung Cheng, **Chun-Chien Tsai**, Jian-Hao Lu, Hsu-Hsin Chen, Bo-Ting Chen, Ting-Kuo Chang, and Ching-Wei Lin, “Periodically Lateral Silicon Grains Fabricated by Excimer Laser Irradiation with a-Si Spacers for LTPS TFTs,” *J. Electrochem. Soc.*, vol. 154, pp. J5-J10, 2007.

[2] （新--2 點，B 類長文）**Chun-Chien Tsai**, Yao-Jen Lee, Jyh-Liang Wang, Kai-Fang Wei, I-Che Lee, Chih-Chung Chen, and Huang-Chung Cheng, “High-Performance Top and Bottom Double-Gate Low-Temperature Poly-Silicon Thin Film Transistors Fabricated by Excimer Laser Crystallization,” *Solid-State Electronics.* (accepted for future publication)

[3] （新--0 點，B 類長文）**Chun-Chien Tsai**, Ko-Yu Chiang, Jyh-Liang Wang, Yao-Jen Lee, Kai-Fang Wei, I-Che Lee, and Huang-Chung Cheng, “Instability of Low-Temperature Poly-Si N-channel Thin-Film Transistors under AC Gate Bias Stress,” *Jpn. J. Appl. Phys.* (under revision)

[4] （新--0 點） **Chun-Chien Tsai**, Hsu-Hsin Chen, Bo-Ting Chen, Yao-Jen Lee, and Huang-Chung Cheng, “High-Performance Low Temperature Poly-Silicon Thin Film Transistors Fabricated by Excimer Laser Irradiation with Bottom-Gate Scheme,” in *ECS Trans.*, vol. 3, pp.143-146, 2006.

[5] （新--0 點）Chuan-Ping Juan, **Chun-Chien Tsai,** Kuei-Hsien Chen, Li-Chyong. Chen and Huang-Chung Cheng, “Fabrication and Characterization of lateral Field Emission Device Based on Carbon Nanotubes” *Jpn. J. Appl. Phys. Part 1*, vol. 44, pp. 2612-2617, 2005.

[6] （新--0 點 )Chuan-Ping Juan, **Chun-Chien Tsai**, Kuei-Hsien Chen, Li-Chyong Chen

and Huang-Chung Cheng, “Effects of High-Density Oxygen Plasma Posttreatment on Field Emission Properties of Carbon Nanotube Field-Emission Displays” *Jpn. J. Appl. Phys. Part 1*, vol. 44, pp. 8231-8236, 2005.

[7] （新--0 點）Huang-Chung Cheng, Fang-Long Chang, Ming-Jang Lin, **C. C. Tsai,** C. W. Liaw, “Novel low-temperature polycrystalline-siliconpower devices with very-low on-resistance using excimer laser-rystallization” *J. Electrochem. Soc.*, vol 151, pp. G900-G903, 2004.

[8] （新--0 點）Ya-Hsiang Tai, Bo-Ting Chen, Yu-Ju Kuo, **Chun-Chien Tsa**i, Ko-Yu Chiang, Ying-Jyun Wei, and Huang-Chung Cheng, “A New Pixel Circuit for Driving Organic Light Emitting Diode with Low Temperature Polycrystalline Silicon Thin Film Transistors”, *IEEE/OSA Journal of Display Technology*, vol. 1, pp. 100-104, 2005.

[9] （新--0 點） Bo-Ting Chen, Ya-Hsiang Tai, Ying-Jyun Wei, **Chun-Chien Tsai**, Chun-Yao Huang, Yu-Ju Kuo, and Huang-Chung Cheng, “Threshold Voltage Compensation Methods for AMOLED Pixel and Analog Buffer Circuits”, *Journal of the Society for Information Display*, vol. 14, pp.793-800, 2006.

## International Letter:

[1] （新--3 點，A 類短文）**Chun-Chien Tsai**, Hsu-Hsin Chen, Bo-Ting Chen, and Huang-Chung Cheng, “High-Performance Self-Aligned Bottom-Gate Low-Temperature Poly-Silicon Thin-Film-Transistors with Excimer Laser Crystallization,” *IEEE Electron Device Lett.*, vol. 28, pp. 599-602, 2007.

[2] （新--3 點，A 類短文） **Chun-Chien Tsai**, Kai-Fang Wei, Yao-Jen Lee, Hsu-Hsin

Chen, Jyh-Liang Wang, I-Che Lee, and Huang-Chung Cheng, “High-Performance Short-Channel Double-Gate Low-Temperature Polysilicon Thin-Film Transistors Using Excimer Laser Crystallization,” *IEEE Electron Device Lett.*, vol. 28, pp. 1010-1013, 2007.

[3] （新--3 點，A 類短文）**Chun-Chien Tsai**, Yao-Jen Lee, Ko-Yu Chiang, Jyh-Liang Wang, I-Che Lee, Hsu-Hsin Chen, Kai-Fang Wei, Ting-Kuo Chang, Bo-Ting Chen, and Huang-Chung Cheng ” Polycrystalline silicon thin-film transistors with location-controlled crystal grains fabricated by excimer laser crystallization,” *Applied Physics Lett.*, vol. 91, pp. 201903-1 - 201903-3, 2007.

[4] **Chun-Chien Tsai**, Yao-Jen Lee, I-Che Lee, Hsu-Hsin Chen, Syu-Heng Lee, Jyh-Liang Wang, and Huang-Chung Cheng, “Green Continuous Wave laser annealed Low Temperature Polycrystalline Silicon Thin Film Transistors,” submitted to *IEEE Electron Device Lett.*.

[5] **Chun-Chien Tsai**, I-Che Lee, Yao-Jen Lee, Hsu-Hsin Chen, Jyh-Liang Wang, Syu-Heng Lee, and Huang-Chung Cheng, “High reliable Bottom-Gate Low Temperature Polycrystalline Silicon Thin Film Transistors,” submitted to *IEEE Electron Device Lett.*.

[6] （新--0 點）**Chun-Chien Tsai**, Ting-Kuo Chang, Hsiu-Hsin Chen, Bo-Ting Chen, Huang-Chung Cheng, “Fabrication of Location-Controlled Silicon Crystal Grains by Combining Excimer Laser Irradiation with Nanometer-sized A-Si,” in *Mat. Res. Soc. Symp. Proc.*, vol 910, Symposium A, 0910-A21-08, 2006.

## International Conferences:

[1] （新--0 點，國際會議） Huang-Chung Cheng, **Chun-Chien Tsai**, Jian-Hao Lu, Ting-Kuo Chang, and Bo-Ting Chen, “Low Temperature Polycrystalline Silicon Thin

Film Transistors Fabricated by Amorphous Silicon Spacer Structure with Pre-patterned TEOS Oxide Layer”, *in International Display Manufacturing Conference (IDMC)* ,pp. 52-54, 2005. (oral)

[2] （新--1 點，國際會議）**Chun-Chien Tsai**, Hsu-Hsin Chen, Yao-Jen Lee, Kai-Fang Wei, Jyh-Liang Wang, Bo-Ting Chen, and Huang-Chung Cheng, “High-Performance Double-Gate LTPS Thin Film Transistors Fabricated by Excimer Laser Irradiation,” *2007 International Thin Film Transistors Conference (ITC'07 in conjunction with SID-Mid Europe Chapter Spring Meeting),* Rome Italy, pp. 44-47, January 25-26, 2007. (oral)

[3] （新--0 點，國際會議）**Chun-Chien Tsai**, Hsu-Hsin Chen, Yao-Jen Lee, Kai-Fang Wei, Jyh-Liang Wang, Bo-Ting Chen, and Huang-Chung Cheng, “High-Performance Self-Aligned Bottom-Gate LTPS TFTs Fabricated by Excimer Laser Irradiation with Backside Exposure Photolithography,” *2007 International Thin Film Transistors Conference (ITC'07 in conjunction with SID-Mid Europe Chapter Spring Meeting),* Rome Italy, pp. 134-137, January 25-26, 2007. (poster)

[4] （新--0 點，國際會議）**Chun-Chien Tsai**, Yao-Jen Lee, I-Che Lee, Hsu-Hsin Chen, Kai-Fang Wei, Jyh-Liang Wang, and Huang-Chung Cheng, “Fabrication of Excimer Laser Crystallized Double-Gate Low-Temperature Poly-Silicon Thin Film Transistors,” in *AMFPD Tech. Dig.*, 2007vol. 14, pp. 37-40. (oral)

[5] （新--0 點，國際會議） **Chun-Chien Tsai**, Kai-Fang Wei, I-Che Lee, Yao-Jen Lee, Jyh-Liang Wang, and Huang-Chung Cheng, “High-Performance LTPS-TFTs Fabricated by Continuous Wave Laser Annealing,” in *Solid State Devices and Materials (SSDM ) Tech. Dig.*, 2007, pp. 568-569. (poster)

[6] （新--0 點，國際會議） **Chun-Chien Tsai**, Kai-Fang Wei, Yao-Jen Lee, I-Che Lee, Hsu-Hsin Chen, Jyh-Liang Wang, Hsai-Wei Chen, and Huang-Chung Cheng, “Fabrication and Characterization of Excimer Laser Crystallized Double-Gate

Low-Temperature Poly-Silicon Thin Film Transistors,” in *International Display Manufacturing Conference (IDMC)* , pp. 529-532, 2007. (poster)

## Domestic Journal:

[1] 鄭晃忠、常鼎國、**蔡春乾**、陳柏廷、呂健豪“低溫複晶矽薄膜電晶體技術及其在平面顯示器上之應用”，科儀新知第二十五卷第二期，92.10.

[2] **蔡春乾**、李逸哲、韋凱方、鄭晃忠 “低溫複晶矽薄膜電晶體中之先進雷射結晶技術發展”，電子月刊第145期，2007.8月號.

## Domestic Conferences:

[1] Huang-Chung Cheng, Ching-Wei Lin, Ting-Kuo Chang, Bo-Ting Chen, **Chun-Chien Tsai**, and Jian-Hao Lu “Low Temperature Poly-Si Thin Film Transistor”, *2003 International Electronic Devices and Material Symposia* (*2003IEDMS*), I29-I36, 2003.

[2] Bo-Ting Chen, Ya-Hsiang Tai, Ying-Jyun Wei, Kai-Fang Wei, **Chun-Chien Tsai**, and Huang-Chung Cheng, “New Source-Follower Type Analog Buffer Using Low Temperature Poly-Si TFTs for Integrated Driving Circuits of Active Matrix Displays”, in *Taiwan Display Conference*, pp. 261-264, 2006.

[3] Hsu-Hsin Chen, **Chun-Chien Tsai**, Ta-Chuan Liao, Bo-Ting Chen, Kuo-Jui Chang and Huang-Chung Cheng, “Location-Control Single Grain-Boundary Silicon Thin Films Fabricated by Excimer Laser Irradiation with Bottom-Gate Structure and It’s Application to High-Performance Low Temperature Polycrystalline Silicon Thin Film Transistors”, in *Taiwan Display Conference*, 03-018, 2006.

[4] Huang-Chung Cheng, Ting-Kuo Chang, **Chun-Chien Tsai**, Jian-Hao Lu, and Bo-Ting Chen, “Fabrication of high-performance poly-Si thin film transistors by excimer laser irradiation with a-Si spacer structure,”in *Taiwan Display Conference*, pp. 134-138, 2004.

[5] **Chun-Chien Tsai**, Hsu-Hsin Chen, Yao-Jen Lee, Kai-Fang Wei, Jyh-Liang Wang, Bo-Ting Chen, and Huang-Chung Cheng, “Location-Controlled Poly-Si TFTs Fabricated by Excimer-Laser-Crystallization with A-Si Spacer Structure and Pre-patterned Silicon Films,” *Optics and Photonics, Taiwan 2006 (OPT 2006)*, Hsinchu ROC, Abs. # GP-51, December 15-16, 2006.

[6] **Chun-Chien Tsai**, I-Che Lee, Yao-Jen Lee, Jyh-Liang Wang, Hsu-Hsin Chen, Kai-Fang Wei, Syu-Heng Lee, Bo-Ting Chen, and Huang-Chung Cheng, “High-Performance Low-Temperature Polycrystalline Silicon Thin-Film Transistors Fabricated by Continuous Wave Laser Annealing” *Optics and Photonics, Taiwan 2007 (OPT 2007)*, Abs. # AP-009, November 30 - December 1, 2007.

## Patents:

[1] 鄭晃忠, 蔡春乾, 陳旭信, “一種具有底閘極之高性能低溫複晶矽薄膜電晶體元件之製造,” *中華民國專利申請中*.

[2] 鄭晃忠, 蔡春乾, 陳旭信, “High-Performance Low-Temperature Polycrystalline Silicon Thin-Film Transistors with Bottom-Gate Structure,” *美國專利申請中*.

[3] 鄭晃忠, 蔡春乾, 陳旭信, “上下雙閘極之高性能低溫複晶矽薄膜電晶體元件之製造,” *中華民國專利申請中*.

# 簡歷

姓名: 蔡春乾

性別: 男

出生年月日: 民國 六十六 年 十 月 三十 日

地址: 台南縣永康市復國一路 68 巷 26 號

學歷: 國立台灣師範大學物理學系

(85 年 9 月 ～ 89 年 6 月)

國立交通大學電子工程研究所碩士班

(90 年 9 月 ～ 92 年 6 月)

國立交通大學電子工程研究所博士班

(92 年 9 月 ～ 97 年 1 月)

論文題目：高性能低溫多晶矽薄膜電晶體之製程技術與特性研究

Study on the Process Technologies and Characteristics of
High-Performance Low Temperature Polycrystalline
Silicon Thin-Film Transistors