國立交通大學

電子工程學系 電子研究所

博士論文

高介電係數閘極介電層在金氧半電晶體中之電特性及其可靠度研究

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摘要

隨著互補式金氧半電晶體(CMOSFETs)元件尺寸跟隨著摩爾定律(Moore's Law)持續微縮，傳統的二氧化矽(SiO_2)閘極介電層(Gate Dielectrics)將遭遇極大的直接穿遂漏電流(Direct Tunneling Leakage Current)導致元件特性失效及可靠度衰退。而高介電係數介電質(High-κ Dielectrics)具有較高的介電係數值，在保有較小的等效氧化層厚度(Effective Oxide Thickness, EOT)情況下，可有效地降低因氧化層微縮至過薄所帶來的巨大直接穿遂漏電流，並且同時保有良好的元件特性。因此高介電係數介電層成為了取代二氧化矽作為下一新世代閘極介電層最有潛力的候選。然而使用高介電係數介電層也將導致伴隨而來的幾個嚴重問題，包括了材料上的熱穩定性(Thermal Stability)、費米能階鎖定效應(Fermi-Level Pinning Effect)、通道內載子移動率的衰減(Mobility Degradation)、以及電荷被高介電係數介電層內之缺陷捕捉/散逸之現象(Charge Trapping/De-trapping)……等等。由於介電質的熱穩定性、費米能階鎖定效應、以及通道內載子移動率的衰減已分別可以藉由使用其它元素的摻雜、金屬閘極的應用、以及利用應力效應來改善其影響，而電荷在高介電係數介電層內被其缺陷捕捉/散逸之現象至今仍為尚在解決之急迫困難。

本論文主要是探討高介電係數介電質的電特性及其可靠度研究，針對高介電係數介電質所遭遇的問題，我們不僅在製程上尋求可以改善的適當方法，也有系統地透過許多量測上的分析來瞭解電荷捕捉/散逸效應的相關物理機制。本論文一開始的首章，我們將說明半導體製程上為何需要應用高介電係數介電層，以及在長年相關研究之中所發現的幾個主要關鍵問題，並講解整個論文的組織架構。

在第二章中，我們利用製程技術針對高介電係數介電層的幾個關鍵問題來加以改善元件特性。包括：(a)在與矽基板之界面特性研究中—我們成功地利用臭氧水成長超薄氧化層(Ozone Oxide)來作為高介電係數介電質以及矽基板之間的中間介電層(Interfacial Layer, IL)，以有效地改善界面特性、抵抗大量的直接穿遂漏電流、減少電荷捕捉/散逸效應，並且提升元件可靠度。(b) 在針對高介電係數介電層內眾多的本體缺陷(Bulk Traps)—我們利用氟離子植入法(Fluorine Incorporation)有效地修補高介電係數介電質的界面缺陷和本體內缺陷，降低電荷捕捉/散逸效應，並提升元件之電特性及其可靠度。(c)在應用高介電係數介電質之後所造成的載子移動率衰減—我們利用舒張性應力(Tensile Strain)在搭配高介電係數閘極介電層的 n 型金氧半電晶體(nMOSFETs)上進行元件特性的改善。我們有效地提升了 n 型金氧半電晶體通道內的電子遷移率，並分析出應力效應的使用對元件電特性及其可靠度之影響。此外，我們也從實驗中的結果發現電荷的捕捉效應無論是在 n 型通道或 P 型通道的高介電係數閘極介電層元件，都大大地主導其元件的可靠度特性。

在第三章中，我們仔細地研究高介電係數閘極介電層元件中之電荷捕捉效應(Charge Trapping Effect)的物理機制及其對元件可靠度所帶來之影響。我們對 n 型金氧半電晶體(nMOSFETs)，在正電壓及嚴苛溫度條件下，研究元件可靠度之不穩定性變化 (Positive Bias Temperature Instability, PBTI)。我們分析出在高介電係數介電層中，電子被其本體缺陷的捕捉效應有著速度上及數量上的差別。在我們的量測上，我們定義反應比較快的第一群組(0 ~ 1.78 sec)中所發生的捕捉效應為「快速捕捉」(Fast Trapping)，而相對後來的第二群組(1.78 ~ 100 sec)中所看到的捕捉效應

我們稱做「慢速捕捉」(Slow Trapping)。我們發現在 100 秒以內的 DC 量測中，快速捕捉在數量上具有非常顯著的捕捉電荷量，並且對元件可靠度有著主導性的影響。此外，我們也發現在 Fowler Nordheim 穿遂現象的發生前後，電子由直接穿遂過基底氧化層，進入高介電係數介電層而被其內的淺缺陷捕捉，轉變成電子先穿遂到高介電係數介電層的導電帶，再被高介電係數介電層內的缺陷所捕捉。並且整個電荷捕捉現象將完全由快速捕捉效應所主導。而經由實驗結果的分析以及相關文獻的比對，我們也發現在高介電係數介電層 HfO_2 中所反映出的這些快速捕捉效應，主要是由 HfO_2 中的 Vo^{2+}, Vo^{-}, Vo^{2-}等等的氧空乏缺陷(Oxygen Vacancies) 以及晶體邊界缺陷 (grain boundary defects)所主導。

在第四章中，我們利用與第三章相同的元件及分析方式，有系統地分析研究回復電壓(Recovery Voltage)對高介電係數介電層內的電荷的散逸效應(Charge De-trapping Effect)所造成的影響。而電荷的散逸效應和捕捉效應同樣有著速度上及數量上的差別，反應比較快的散逸效應我們定義為「快速散逸」，而相對較慢的我們稱做「慢速散逸」。如同於電荷捕捉中的快速捕捉現象，快速散逸效應也在整個電荷回復行為中具有著相當大的主導性。此外，我們發現整個電荷散逸效應的物理機制，主要是由高介電係數介電層中被捕捉住的載子所可允許穿遂回矽基板的能階所決定。

在第五章中，針對一般 DC 量測無法精準萃取到的快速暫態電荷捕捉/散逸效應，我們也導入具有極短量測時間並可解析數奈秒(ns)下電荷行為之優勢的脈衝式量測(Pulse IV Measurement)，來正確完整的分析在高介電係數介電層中的電荷捕捉/散逸效應。對幾個重要的物理參數，諸如：逼迫電壓，逼迫時間，回復電壓，以及較嚴峻的操作溫度。我們分別有系統的進行完整的相關研究，並探討其背後的物理意義。電荷的捕捉/散逸效應也經由溫度的相關性確定為電荷的穿遂效應所主導。此外，我們也利用脈衝式量測模擬了高介電係數介電層元件在 AC 電壓形式操作下的情況。我們證實了電荷的捕捉/散逸效應在 AC 電壓形式的操作下，對元件

的電特性及可靠度仍有顯著的影響。

在第六章中，我們仔細地分析高介電係數閘極介電層元件在動態的連續操作電壓下，電荷捕捉/散逸效應對其電特性及可靠度之影響。我們發現在回復電壓不足的情況下，被捕捉在高介電係數介電層本體內部的電荷將會持續留存，並會累積在下一次電荷捕捉效應之中。而透過一個足夠回復電壓的條件來分析，我們可以知道整個電荷捕捉/散逸效應是具有回復性。進一步也證實在小電壓逼迫的條件下，並無造成高介電係數介電層中任何額外的缺陷產生，只是重複電荷捕捉/散逸的行為。因此，我們在動態電性逼迫之不穩定性測試中所看到元件的劣化，是由於在高介電係數介電層本體中未能散逸而出的電荷，在重複的電荷捕捉/散逸效應下造成了留存電荷的累積，而非在小電壓電性逼迫中產生新的缺陷。如此，我們也映證了電荷的捕捉/散逸現象將對元件的連續操作造成顯著的影響。

在第七章中，我們對具有高介電係數閘極介電層的 p 型金氧半電晶體(pMOSFETs)，在負電壓及嚴苛溫度條件下，研究元件可靠度之不穩定性變化(Negative Bias Temperature Instability, NBTI)。在 NBTI 的研究中，我們除了分析電洞在高介電係數介電層中的被捕捉特性，也藉由一個奇異的 NBTI 現象(Anomalous NBTI Behavior)，額外發現電子在 NBTI 的可靠度衰退中也扮演一個不可忽視的角色。因此，當我們在利用 NBTI 可靠度考量元件的生命週期之時，我們必須慎重地同時考量電子和電洞在 p 型高介電係數閘極電晶體中的捕捉現象，並以此修正整個元件生命週期的預測。

在第八章中，我們總結了所有的研究成果，於高介電係數介電層的可靠度研究中，我們在考量了電荷的快速暫態行為所帶來的影響，建立了一個具有合理解釋的物理模型，並可有效地說明在高介電係數介電層中之電荷捕捉/散逸效應的物理機制。最後，我們也根據這些年來研究高介電係數介電層的經驗，針對高介電係數介電層在未來的研究方向提出一些看法。

A Study of Electrical Characteristics and Reliability in CMOSFETs with High-κ Gate Dielectrics

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Abstract

As the CMOS technology continues to scale down following the Moore's Law, the shrinkage of gate dielectric thickness will suffer the intolerable direct-tunneling gate leakage-current which leads to degrade the device performance and reliability. High permittivity dielectrics (High-κ Dielectrics) have been proposed to be the potential candidates to solve the critical issues since their thicker films can be utilized to effectively reduce the great direct tunneling leakage current while it maintains EOT (Effective Oxide Thickness) value and the device performances. However, several critical problems such as thermal stability, Fermi-level pinning effect, channel mobility degradation, and charge trapping/de-trapping effects have been accompanied with the applications of high-κ gate dielectrics. The thermal stability, Fermi-level pinning effect, channel mobility degradation have been improved through the multi-element incorporations, metal gate process, and strain effect technology, respectively. However,

the charge trapping/de-trapping effects are still the major difficulties which are waiting for the effective solutions in the progress of the high-κ gate dielectrics.

In the dissertation, we would mainly discuss the electrical characteristics and device reliability of high-κ gate dielectrics. For the derivative issues of high-κ gate dielectrics applications, we not only effectively enhance the device performance through appropriate fabrication technologies, but also systematically investigate the physical mechanisms of charge trapping/de-trapping effects through a variety of electrical characterizations. At the beginning, in the chapter 1, we will explain the necessary of high-κ gate dielectrics applied on semiconductor progress, and further point out several critical issues discovered during related investigations in recent years. Besides, we finally describe the organization of this dissertation.

In the early stages of this dissertation, we study the enhancements of device performance through the fabrication technologies. In the chapter 2, the ozone oxidation has been successful as an interfacial layer (IL) to apparently improve the interface between high-κ gate dielectrics and Si-substrate with fine interface properties, low direct tunneling leakage current, and less charge trapping effect. The fluorine incorporation has been confirmed to effectively reduce the interface states, high-κ bulk traps, and further suppress the charge trapping/de-trapping effects. Moreover, the device performance and related reliability are also successfully enhanced by fluorine incorporation. The tensile strain effect has been demonstrated to successfully enhance the device performance for nMOSFETs with high-κ gate stack. We have effectively enhanced the n-channel electron mobility and further investigated the influences of strain effect on device characterizations and related reliability. Besides, the charge trapping effect has been verified to dominate the reliability degradation in both nMOSFETs and pMOSFETs with the high-κ gate stack.

In the chapter 3, we have carefully studied the physical mechanism of charge trapping effect in high-κ gate dielectrics and its impacts on device reliability. In the reliability investigations of positive bias temperature instability (PBTI) on the nMOSFETs, we observed that the charge trapping phenomenon at high-κ bulk traps has the different characteristics with respect to responding time constant and quantity. In our measurements, we have defined the charge trapping occurred on the first stage (0 ~ 1.78 sec) as the “First Trapping”, and the second stage (1.78 ~ 100 sec) as the “Slow Trapping”. We have discovered that the fast trapping has the apparently significant impacts on device reliability with a great quantity of trapped charges during a 100 sec electrical stress in DC measurements. Moreover, we also found the distinct charge trapping behaviors before and after the occurrence of Fowler Nordheim tunneling (FN-tunneling). Before FN-tunneling, the injected charges form Si-substrate will tunnel through the IL and further be trapped at those shallow traps in the high-κ bulk. After FN-tunneling, the injected charges form Si-substrate still tunnel through the IL but drop on the conduction band of high-κ gate dielectrics. Afterward, these charges are captured from the conduction band of high-κ gate dielectrics by those shallow traps in high-κ bulk. From the experimental analysis and related literatures, we also have discovered that the oxygen vacancies (Vo^{2+}, Vo^{-}, Vo^{2-}) and grain boundary defects are the main shallow traps which are responsible for the fast trapping in HfO_2.

In the chapter 4, we have systematically investigated the influences of recovery voltage on charge de-trapping effect in high-κ gate dielectrics with the same devices and similar analytic methodologies in chapter 3. The charge de-trapping effect also shows the different responding time constant and quantity as well as charge trapping effect. The charge de-trapping with short time respondence is defined as “fast de-trapping” (Recovery Time = 0 ~ 1.78 sec). On the contrary, the slower respondence

(Recovery Time = 1.78 ~ 100 sec) is defined as “slow de-trapping” As the finding of the fast trapping in charge trapping phenomenon, the fast de-trapping is also significantly predominant in whole recovery behavior. Furthermore, we discover the physical mechanism of charge de-trapping effect is mainly determined by the trapped charges in high-κ bulk which can tunnel through the available energy levels back to Si-substrate.

In the chapter 5, a pulse IV measurement which can capture the real electrical characteristics within only several nano seconds (ns) is introduced to accurately realize the charge trapping/de-trapping effects in high-κ gate dielectrics since the fast transient charge trapping/de-trapping behaviors can not be actually presented in conventional DC measurements. We have systematically investigated the impacts of some significantly physical parameters such as stress voltage, stress time, recovery voltage, and crucial operation temperature on the complete phenomena and detailed mechanisms of charge trapping/de-trapping effects. Lower activation energy extracted form the temperature dependence demonstrates that the charge tunneling is the predominance for both charge trapping/de-trapping dynamics. Besides, the electrical characteristics of high-κ gate stack also have been analyzed under the AC stress conditions. We demonstrate that the charge trapping/de-trapping effects have apparent influences on device performance and related reliability under the AC operation.

In the chapter 6, we have carefully discussed the dynamic-PBTI degradation in nMOSFETs with high-κ gate stack in order to understand the impacts of charge trapping/de-trapping effects on the continuing device operation. We observe that the trapped charges which are not recoverable under the insufficient recovery voltage will be residual in high-κ bulk and further contribute to the significant PBTI degradation in next charge trapping sequence. The charge trapping/de-trapping phenomena are verified to be reproducible, and it implies that there is no additional trap generation under a smaller stress condition because the full recovery can be achieved with an appropriate recovery voltage. Therefore, we have realize the connection of residual charges with dynamic PBTI degradation, and further confirmed the apparent influences of charge trapping/de-trapping phenomena on the continuing device operation.

In the chapter 7, we discover a anomalous negative bias temperature instability (Anomalous NBTI) behavior in pMOSFETs with high-κ gate stack. This specific phenomenon is verified to be the contribution of electron trapping in high-κ bulk through a variety of electrical measurements including the threshold voltage shift, NBTI degradation, and charge pumping results. For the most important implication of anomalous NBTI discovery, the linear lifetime extraction is not able to accurately predict the lifetime at normal operation with high-κ gate stack once we consider both electron trapping and hole trapping in high-κ bulk traps.

In the chapter 8, we summarize all of the experimental results in the series of high-κ investigations. We build a reasonable physical model with the considerations of fast transient behaviors to appropriately explain the charge trapping/de-trapping effects in high-κ gate dielectrics. Finally, we also give some suggestions which are considered to be helpful to the realization and promotion of high-κ gate dielectrics applied on the CMOS technology.

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當博士畢業發表順利通過之際，內心所蘊含的百感交集已非點滴筆墨能足以形容。是以，完成了一個當初為自己立下的里程碑，得到了不是結束一切的感覺，反倒是有種替自己的人生打開了另一扇嶄新大門一般。帶著自己辛勤耕耘的收穫，有著充滿了堅定的自信，很高興自己在完成博士學位的時候，能夠驕傲並榮耀地懷帶著這樣的心情。

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Chapter 1

Introduction

1.1 Motivation of Using High-κ Gate Dielectrics

As the CMOS technology continues to scale down following the Moore's Law, the shrinkage of gate dielectric thickness is approaching a physical limitation of conventional SiO_2-based ultrathin oxide [1]. The aggressive scaling of CMOS technology leads the ultrathin gate oxide to suffer the intolerable direct tunneling gate leakage current which results in the devices to face the serious concerns such as gate integrity, stand-by power consumption, and associated reliability issues [2-5]. As the rapid reduction of equivalent oxide thickness (EOT), the appropriate EOT requirements with the considerations of the tough challenges are outlined by the International Technology Roadmap for Semiconductors (ITRS) in Table 1-1 [6].

In recent years, numbers of alternative gate dielectric materials have been extensively investigated on the aggressive attempts to replace the conventional ultrathin gate oxide. High dielectric permittivity gate dielectrics (high-κ gate dielectrics) have been proposed to be the potential candidates to solve the critical issues since their thicker films can be utilized to reduce the large direct tunneling leakage current while maintaining EOT value and the device performances [7-9]. Presently, many associated researches about high-κ gate dielectrics have been widely investigated to explore their detailed properties. The experimental results have demonstrated the compatibility of high-κ gate dielectrics in CMOS technology, and some findings have successfully exhibited the excellent device performances to confirm the feasibility of high-κ gate applications [10-12]. The selections of high-κ gate dielectrics are usually consistent with the requirements of sufficient κ-value, wide bandgap, thermal stability, and process compatibility [13-15]. At the beginning of high-κ researches, many high-κ gate dielectrics including Ta_2O_5, TiO_2, Si_3N_4, Al_2O_3, and HfO_2 are considerations in the related researches [16-23]. However, Ta_2O_5, TiO_2, Al_2O_3, are gradual far away the major current in high-κ investigations with the comprehensive considerations of poor thermal stability (Ta_2O_5, TiO_2) and insufficient κ-value (Si_3N_4, Al_2O_3). Nowadays, Hf-based family such as HfO_2, HfON (nitride), HfSiO (silicate), HfAlON (multi-elements incorporation) become the most promising solutions due to the moderate dielectric constant (20~25), large energy bandgap (5.7~6.2 eV), sufficient barrier height to Si for both electrons and holes (1.5~1.9eV), and excellent thermal stability of amorphous phase and interface properties (~1000℃) [19-22, 24-26].

1.2 Critical Issues of High-κ Gate Dielectrics

Nowadays, high-κ gate dielectrics become the promising solutions to replace the conventional ultrathin oxide in order to keep the steps of developing advanced CMOS technology. However, the high-κ gate dielectrics have several critical problems needed to overcome in progress. In the early researches, the thermal stability of high-κ materials is a quite urgent issue in the device integration. The high-κ gate dielectrics easily react with the Si-substrate to result in the formation of based oxide (or silicate) on the Si surface. These extra interfacial layers between high-κ and Si-substrate usually have the poor film quality and the increasing EOT requirements to restrain the CMOS technology development. Moreover, the amorphous crystallization is the preferable phase to prevent from the significant direct-tunneling gate-leakage-current. However, many high-κ gate dielectrics have poor thermal stability might crystallize as easy due to low crystallization temperature. For HfO_2, slight crystallization is already observed when temperature is around 400 ~ 500 ℃ [27]. Nevertheless, the high-κ gate dielectrics are inevitable to suffer the crucial temperature which might be up to 950 ℃ in a complete CMOS process (such as the post rapid thermal annealing to enhance the quality of gate dielectrics ; high temperature activation to drive the implanted dopants.) [28-29]. Fig. 1-1(a)-(d) showed the HRTEM pictures of the HfO_2 with various high temperature annealing (a) as-deposited state, 400 °C, (b) 800 °C annealing, (c) 900 °C annealing, (d) 1000 °C annealing, respectively [27]. Although HfO_2 is more close to amorphous phase in the as-deposited state, there is still partially crystallization observed in HfO_2 itself. Moreover, higher temperature drives up the crystallization of HfO_2 itself and increase the interfacial layer (eq. based oxide); those imply the poor thermal stability of high-κ gate dielectrics. In order to overcome the significant issues of thermal stability, numbers of related process have been modified with less thermal budget (^{ex} a rapid thermal process is preferred replacing the conventional furnace process.) to avoid the interaction between high-κ and Si-substrate. In addition, the formation of multi-element high-κ compounds is also adopted to solve this critical problem because of elevated crystallization temperature. The Hf-based high-κ gate dielectrics have been demonstrated to depict better capability of crystallization temperature even above 1000 ℃ [30-33].

Except the concerns of thermal stability, plenty of the pre-existing bulk traps have been verified to exist in Hf-based high-κ gate dielectrics, thus led to significant impacts on device performance and reliability. The Fermi-level pinning effect is one of the critical issues. The origin of Fermi-level pinning effect is resulted from the existence of electrical dipole with respect to the inter reaction and electron exchange between the poly-Si gate electrode and high-κ gate dielectrics [34-39]. According to the recent reports [36, 39], a formation of an oxygen vacancy would result in the generation of two electrons. If the oxygen vacancy is near the interface, the generated electrons can transfer across the interface to the poly-Si gate electrode and an interface dipole produced in the oxide. The dipole would lead to the large threshold shift and causes some difficulties in logic designs. This existence of Fermi-level pinning effect has persecuted the developments of the advanced gate stack to achieve the appropriately low threshold voltage, which can meet the future progress of CMOS technology. Fig. 1-2(a)-(c) showed the Fermi-level pinning effect in high-κ gate dielectrics revealed in C-V characteristics (a) SiON (b) $HfAlO_x$ (c) $HfSiO_x$ [39]. Today, a method of replacing the poly-Si electrode by metal gate is considered as the practical solution for this problem [40]. The related investigations have been verified to effectively reduce the Fermi-level pinning effect and accomplish the proper requirements of low threshold voltage. Furthermore, the other researches also have found that insertion of an ultra-thin cap layers in between the poly-Si and the high-κ gate dielectrics can also improve the Fermi-level pinning effect by means of eliminating the inter electron exchange and oxygen vacancies in between gate electrodes and high-κ gate dielectrics [41].

The channel mobility degradation becomes another significant problem when the high-κ gate dielectrics have been applied on the CMOS technology [42-43]. Fig. 1-3 represented the apparent mobility degradation with the high-κ gate stack. This phenomenon is governed by various scattering mechanisms at the bulk silicon and at the gate dielectric/Si interface with respect to the variety of Coulomb, phonon, and surface roughness (at high electric field) scattering as well known [44-45]. In high-κ gate dielectrics, the most critical concern is the most significant phonon scattering referred to the great quantity of high-κ bulk traps. Plenty of high-κ investigations demonstrated the remote phonon scattering in high-κ bulk is the primary origin of channel mobility degradation [46-47]. These phonons will interact with the channel electrons and produce the apparent mobility degradation. Especially, the soft optical phonons would become actively at the elevated temperature because of the plenty of ionic bonds in high-k gate dielectrics themselves [48-49]. Besides, the interface dipole existed between high-κ gate dielectrics and based oxide (or called as interfacial layer, IL) is also demonstrated as the major reason which is responsible for the channel mobility degradation shown in Fig. 1-4 [50]. Therefore, eliminating the high-κ bulk traps is essential for solving this perplexing problem. However, this specific and urgent problem is hard to remove due to the intrinsic properties of quantities of natural bulk traps in high-κ gate dielectrics. For the consideration, strain effect is thought as one of the most potential solutions to enhance the degraded mobility under the seriously unfavorable bulk traps. The physical mechanism can be explained as the related band splitting induced by the strain force. It leads the carriers with lower effective mass and higher mobility, and further enhances the channel mobility [51]. Many related researches have exhibited the brilliant results to verify the feasibility of strain effects including the globe strain and the local strain [45, 52]. The associated achievements of mobility enhancements conducted by strain effect are also revealed in Fig. 1-5(a) and Fig. 1-5(b) [53].

Overall, the most troublesome issue is considered as the significant charge trapping/de-trapping effects in the high-k gate dielectrics [54-55]. In the conventional SiO_2 gate dielectrics, the NBTI degradation is a serious concern while the PBTI degradation is as less consideration [56]. However, both of hole trapping and electron trapping in high-κ are equally significant, and their impacts on device characteristics can not be neglected anymore according to plenty of intrinsic bulk defects. On one hand, the charge trapping usually occurs when devices are under the electrical stress due to the capture of injection charges by the pre-existing high-κ bulk traps [57-58]. On the other hand, the charge de-trapping normally happens when devices are under the recovery force according to the relaxation of the trapped charges from the traps centers in high-κ gate dielectrics [59-60]. Both the charge trapping/de-trapping effects would result in the serious threshold voltage shift to degrade the device performance and associated reliability. Fig. 1-6(a) and Fig. 1-6(b) exhibited the charge trapping/de-trapping phenomena in the both nMOSFETs and pMOSFETs through the dynamic-PBTI and dynamic-NBTI degradations, respectively [61]. In our studies, the investigations of charge trapping/de-trapping in high-κ dielectrics are our major aims to understand the related physical mechanisms and further expect to develop the high-κ gate dielectrics on CMOS technology.

1.3 Dissertation Organization

As the passage above indicated, the aims of this dissertation will contain two parts of related high-κ researches including: (a) The investigations of device enhancements on the critical high-κ issues through the fabrication technologies are coordinated in the chapter 2, and (b) The studies of charge trapping/de-trapping behaviors in the aspects of device reliabilities through electrical characterizations. They are discussed in the chapter 3, 4, 5, 6, 7, respectively. The organization of this dissertation is briefly described as below. The chapter 2 studies the enhancements of device performance for the critical issues accompanied with the application of high-k gate dielectrics through the fabrication technologies. The ozone oxidation, fluorine incorporation, and tensile strain effect were utilized to improve the interfacial properties between high-κ gate dielectrics and Si-substrate, high-k bulk properties, and n-channel electron mobility, respectively. The chapter 3 studies the charge trapping behavior in the high-κ gate dielectrics under the PBTI degradation. A mathematical modeling demonstrates that the charge trapping behavior leads the PBTI degradation in nMOSFETs with high-κ gate dielectrics. A universal physics model for the charge trapping in high-κ gate dielectrics is established through the investigations on stress voltage, stress time, and analysis of fast/slow charge trapping behaviors. Moreover, the new findings of charge trapping at the critical voltage which the FN-tunneling starts are also carefully discussed. The chapter 4 studies the charge de-trapping behavior in the high-κ gate dielectrics under various recovery conditions. As similar to the chapter 3, a mathematical modeling demonstrates the charge relaxation from the bulk trap centers to primarily dominate the charge de-trapping behavior in high-κ gate dielectrics. A universal physics model is also established through the investigations on stress voltage, recovery voltage, and analysis of fast/slow charge de-trapping behaviors. The chapter 5 discusses the necessary and the applications of pulse measurements with the further considerations of fast transient charge trapping/de-trapping behaviors. The transient charge trapping/de-trapping effects are systematically investigated through the stages of stress voltage, stress time, and recovery voltage. Lower activation energy extracted form the temperature dependence demonstrated the charge tunneling is the predominance for both charge trapping/de-trapping dynamics. Besides, the AC stress is also verified to have the apparent impacts on the charge trapping/de-trapping. The chapter 6 further explores the influences of charge trapping/de-trapping on the continuing device operation. The residual charges are demonstrated to significantly affect the dynamic-PBTI degradation in both DC and pulse measurements. The chapter 7 searches for the origin of anomalous NBTI behavior. A NBTI lifetime prediction is clarified to be necessary in the considerations of both hole trapping and electron trapping in pMOSFETs. The chapter 8 summarizes the related findings and recommends the further suggestions to the future works through the related experiences of high-κ gate dielectrics researches.

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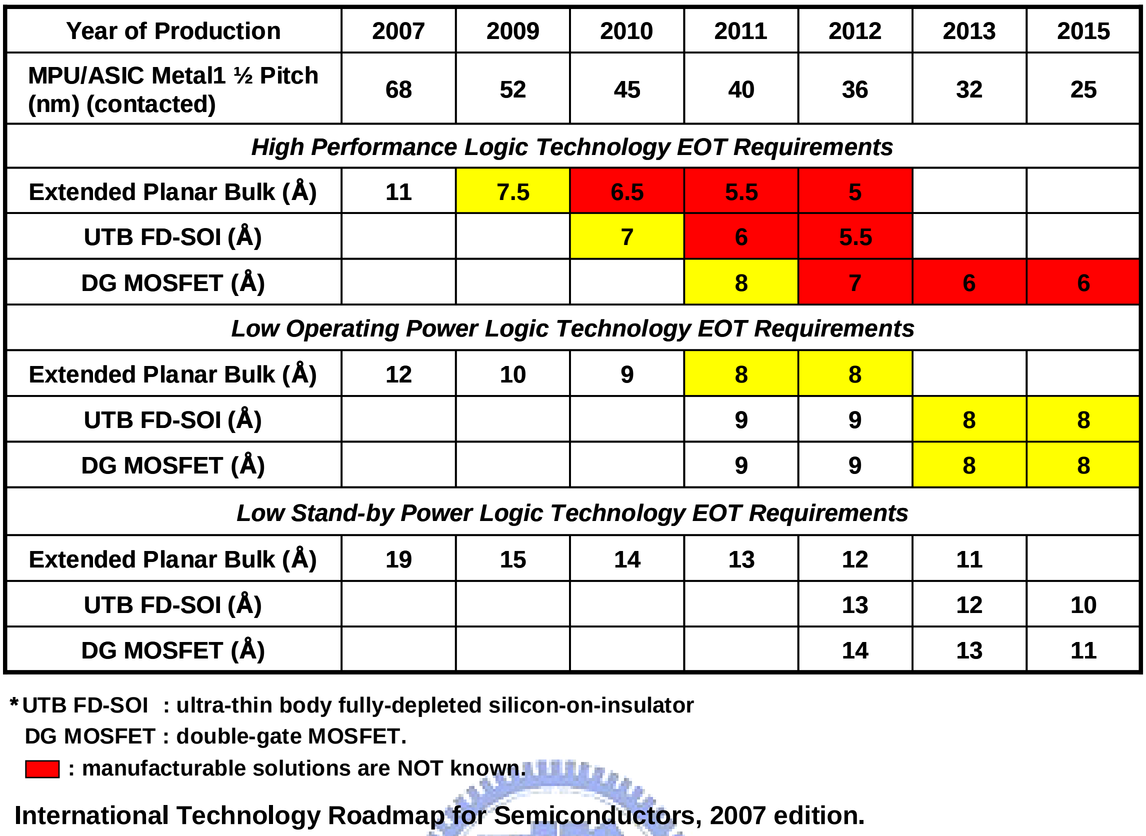


Year of Production	2007	2009	2010	2011	2012	2013	2015
MPU/ASIC Metal1 ½ Pitch (nm) (contacted)	68	52	45	40	36	32	25
High Performance Logic Technology EOT Requirements							
Extended Planar Bulk (Å)	11	7.5	6.5	5.5	5		
UTB FD-SOI (Å)			7	6	5.5		
DG MOSFET (Å)				8	7	6	6
Low Operating Power Logic Technology EOT Requirements							
Extended Planar Bulk (Å)	12	10	9	8	8		
UTB FD-SOI (Å)				9	9	8	8
DG MOSFET (Å)				9	9	8	8
Low Stand-by Power Logic Technology EOT Requirements							
Extended Planar Bulk (Å)	19	15	14	13	12	11	
UTB FD-SOI (Å)					13	12	10
DG MOSFET (Å)					14	13	11

***UTB FD-SOI : ultra-thin body fully-depleted silicon-on-insulator**
DG MOSFET : double-gate MOSFET.
🟥 : manufacturable solutions are NOT known.

International Technology Roadmap for Semiconductors, 2007 edition.

Table 1-1 EOT scaling in the International Technology Roadmap for Semiconductor, 2007 edition [7].

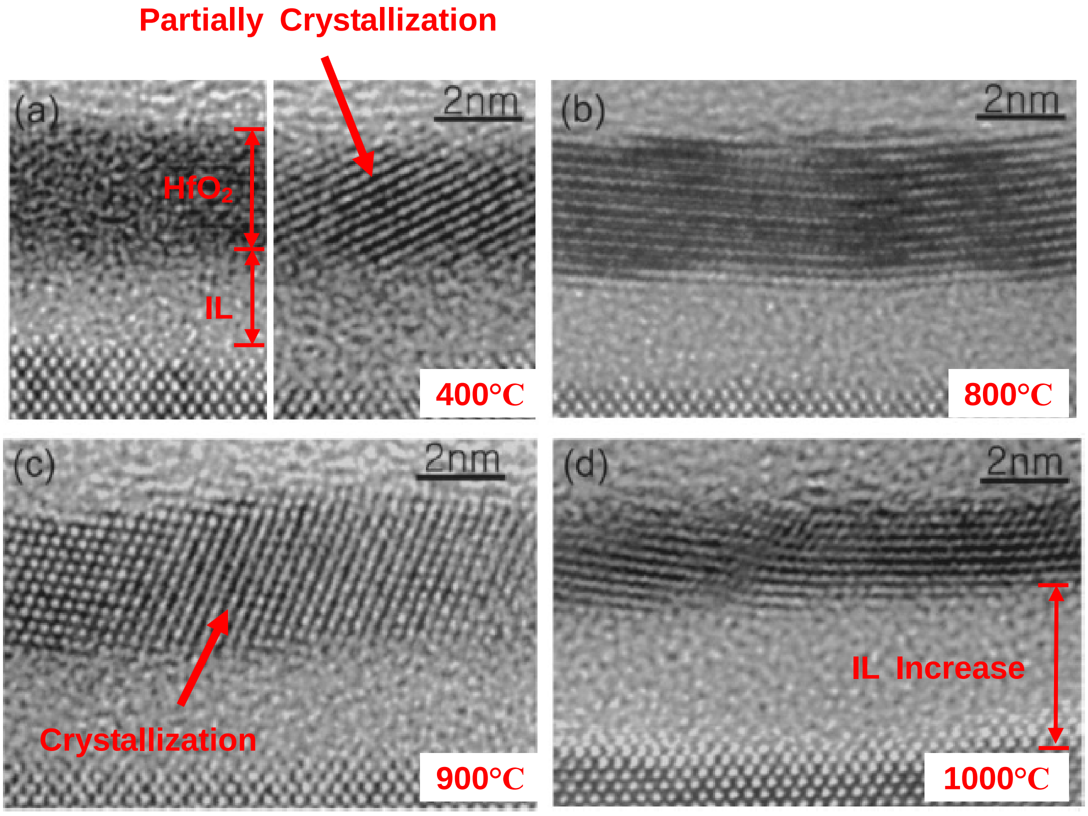
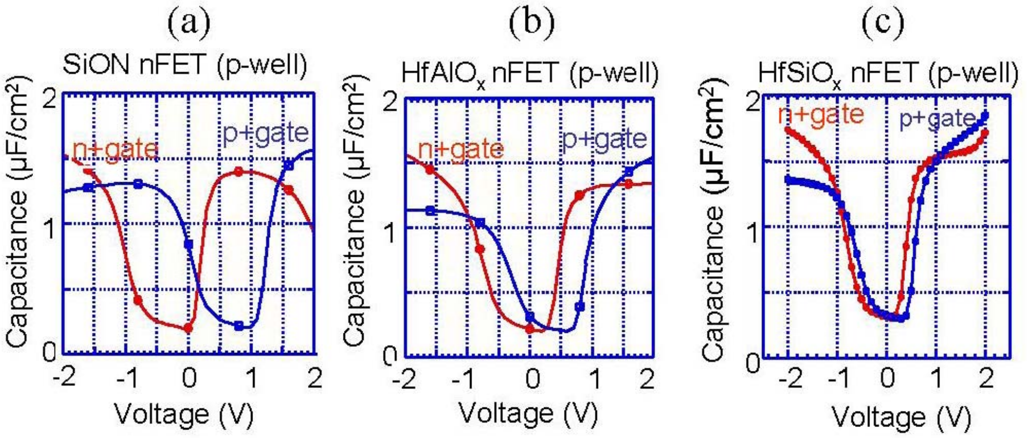

Partially Crystallization
(a)
HfO2
IL
2nm
400°C
(b)
2nm
800°C
(c)
2nm
Crystallization
900°C
(d)
2nm
IL Increase
1000°C

Fig. 1-1 HRTEM pictures of the HfO_2 with various high temperature annealing (a) as-deposited state, 400 °C, (b) 800 °C annealing, (c) 900 °C annealing, (d) 1000 °C annealing, respectively [27].



ΔV_{fb}=1.0 eV ΔV_{fb}=0.5 eV ΔV_{fb}=0.15 eV

Fig. 1-2 The Fermi-level pinning effect in high-κ gate dielectrics revealed in C-V characteristics (a) SiON (b) $HfAlO_x$ (c) $HfSiO_x$ [39].

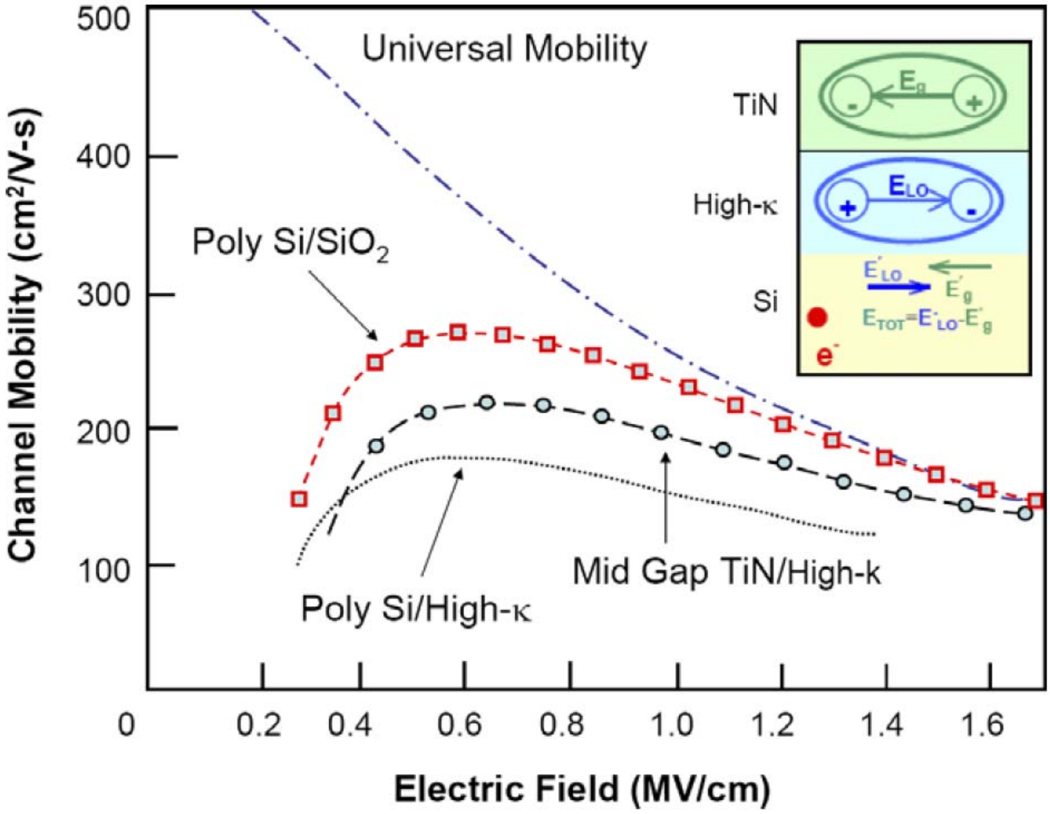


Fig. 1-3 Significant mobility degradation in the devices with poly-Si/high-κ gate dielectrics. The mobility can be improved with mid-gap metal gate electrode by screening the remote phonons scattering. Redraw based on [45].

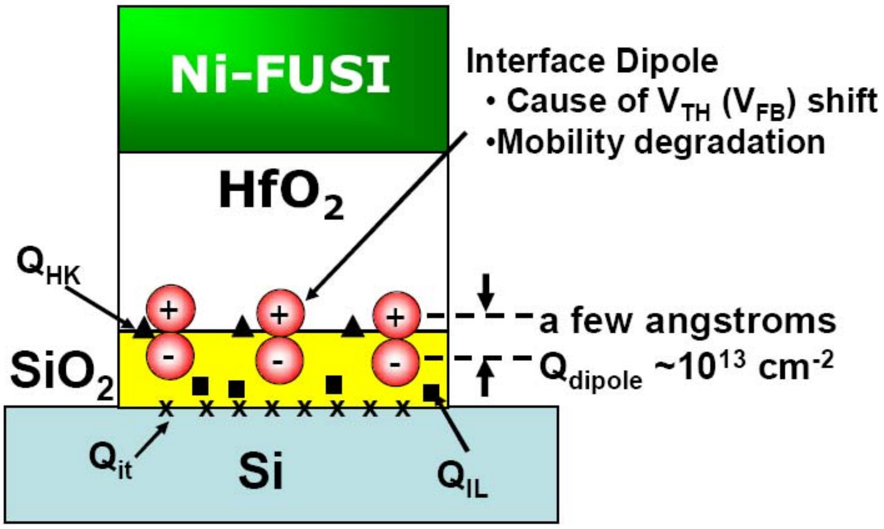

Ni-FUSI
HfO$_2$
Interface Dipole
• Cause of V_{TH} (V_{FB}) shift
•Mobility degradation
Q_{HK}
+
-
a few angstroms
SiO$_2$
Q_{dipole} ~10^{13} cm^{-2}
Q_{it}
Si
Q_{IL}

Fig. 1-4 Interface dipole is considered as the primary origin of significant mobility degradation [50].

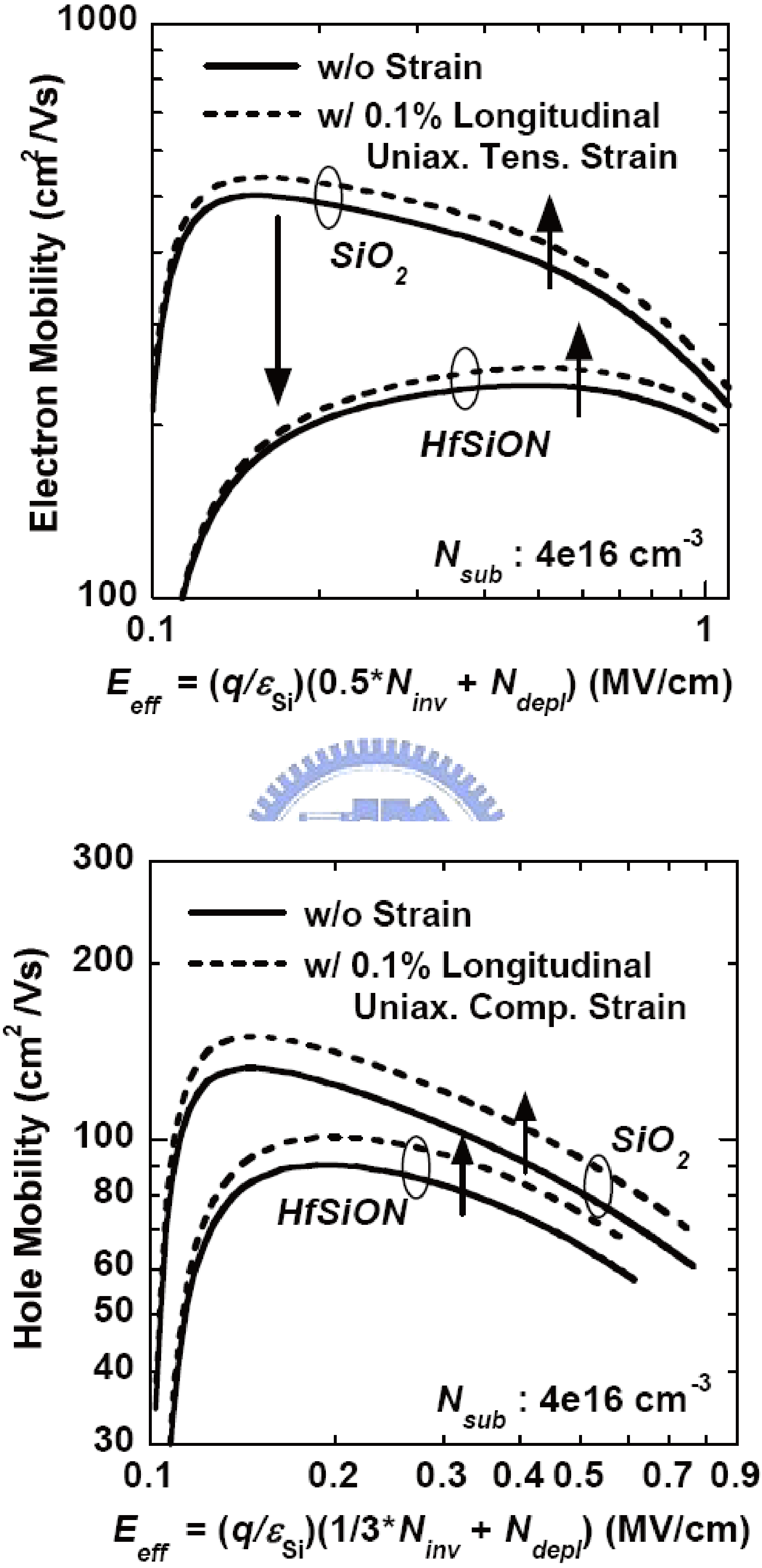


Fig. 1-5 The strain engineering for High-k FETs (a) nMOSFETs (b) pMOSFETs [53].

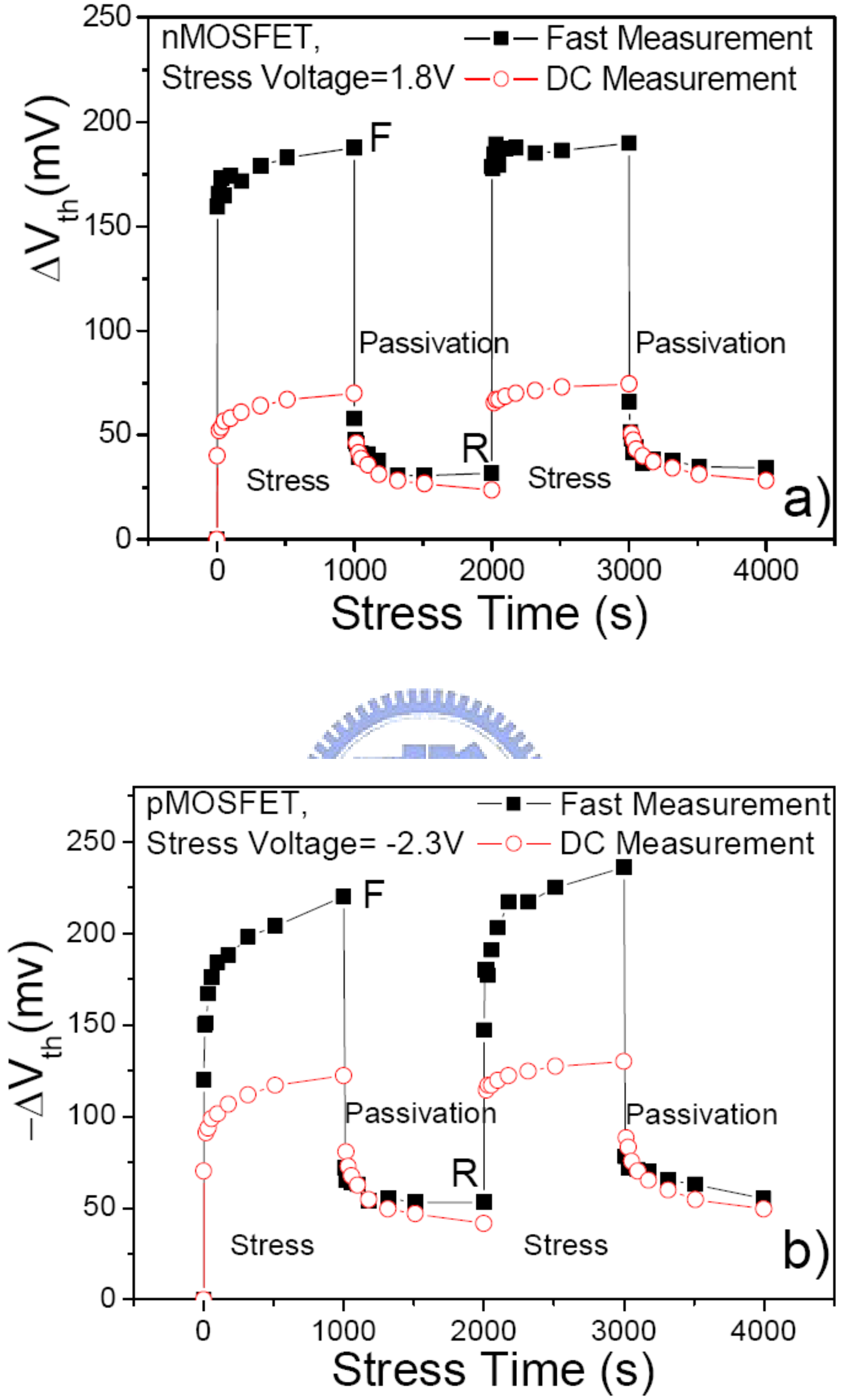


Fig. 1-6 The charge trapping/de-trapping phenomena in (a) Dynamic-PBTI, nMOSFETs (b) Dynamic-NBTI, pMOSFETs [61].

Chapter 2

The Enhancements of Device Performance for High-κ Gate Dielectrics with Fabrication Technologies

2.1 General Background

It is imperative to introduce high-κ gate dielectrics into the continuous shrinkage of CMOS technology since thicker films can be utilized to reduce the large direct tunneling leakage current while maintaining the device performance. Many researches about high-κ gate dielectrics have been investigated in recent years. The related experimental results have demonstrated that high-κ gate dielectrics were compatible with standard CMOS process. However, several key issues of high-κ gate dielectrics are necessary to solve, including (1) interface properties between high-κ materials and silicon substrate, (2) plenty of high-κ bulk traps, and (3) channel carrier mobility degradation shown in Fig.2-1. In this chapter, we will study these critical problems and improve them through the feasible fabrication technologies.

2.2 Improvements of Ozone Surface Treatment on the Electrical Characteristics and Reliability in HfO$_2$ Gate Stacks

2.2.1 Motivation

From the recent studies, it has been demonstrated that high-κ materials would easily react with the silicon substrate to form an unwanted interfacial layer at the interface such as metal-oxide (MO_x) or silicide (MSi_x) after a high temperature process [1-3]. The interface controlling between the high-κ gate dielectrics and the silicon substrate is really important because device performance and reliability characteristics are strongly affected by the quality of the interface [3-5]. Therefore, surface treatments prior to high-κ deposition are considered to be necessary in order to enhance the capabilities of high-κ gate stack [5]. In general, surface oxidation and nitridation are both considered to improve the interface properties. Surface nitridation on the silicon substrate prior to high-κ deposition has been shown to be effective in achieving the low EOT (equivalent oxide thickness) [5], preventing boron penetration [6], and lowering gate leakage current [5-6]. However this technique would result in large interface states, which leads to significant charge trapping and degradation of channel mobility [7]. Therefore, superior film quality of surface oxidation with lower EOT became the potential candidate for surface treatment prior to high-κ deposition.

In our study, surface treatment with ozonated water has been utilized to deposit ultrathin oxide layers (<10 Å) at low temperatures (nearly room temperature) [8]. The growth of the ozonic oxide occurs in a layer-by-layer manner, with a thinner transition layer. [9]. The ozonic oxide is homogeneous from the surface to the interface, unlike corresponding thermal oxide layers [10]. Moreover, the density of an ozonic oxide is, however, comparable to that of a thick thermal oxide [9]. Our aim for this experiment was to use ozonic water treatment to improve the quality of high-κ/Si interface.

2.2.2 Experimental Procedures

LOCOS-isolated MOS capacitors were fabricated on p-type (100) silicon wafers and then cleaned using standard RCA processes (with HF-last). The samples were treated using ozone oxidation (Ozone), rapid thermal oxidation (RTO), and ammonia nitridation (NH_3). Diluted ozonated water was used to grow an ultrathin ozonic oxide at room temperature (~ 7-8 Å, measured by ellipsometer). RTO was also employed to deposit a thin SiO_2 layer (~ 10 Å) at 800 °C using a rapid thermal process system. NH_3 nitridation was performed in a high-temperature furnace at 800 °C for 1 hr to generate an ultrathin oxynitride layer (~ 10 Å). After each of these surface treatments, a 55Å-thick HfO_2 layer was deposited at 500 °C using an MOCVD system, followed by high-temperature post-deposition annealing (PDA) at 600 °C in a nitrogen ambient for 30 sec. Aluminum metal, which served as the gate electrode, was created using a thermal evaporation system. After the gate electrodes had been patterned and the contact holes etched, metallization and backside contact were performed, followed by sintering at 450 °C. The process flow and experimental conditions were shown in Fig.2-2.

2.2.3 Results and Discussions

2.2.3.1 Ozone Thin Oxide

The properties of ozone-mediated oxidation were investigated in advance. Fig. 2-3 displays the growth rates of the ozone-mediated oxide as a function of the ozone concentration in the water. The ozone-mediated oxidation revealed a specific property of self-limited growth, which provided an ultrathin surface oxide (<10 Å) that was a necessary requirement prior to high-κ dielectric deposition; not only was this oxide ultrathin, it was also of high quality. In Fig. 2-4, from the comparisons of the etching rate we observed a high film density of the ozone-mediated oxide because of the extremely low etching rate near the SiO_2/Si interface. This superior film density originated from the layer-by-layer growth of the ozone-mediated oxidation process. From the above experimental results, ozone-mediated oxidation was considered to achieve the requirements of suitable surface treatment prior to high-κ deposition. Hence, this method was introduced into MOS device fabrication with high-κ gate dielectric, HfO_2 deposited by MOCVD. Fig. 2-5 presents a high-resolution TEM image in which we observed a thin Ozone-SiO_2 layer (<10 Å) and smooth Ozone-SiO_2/Si-substrate and HfO_2/Ozone-SiO_2 interfaces. We can observe that the Ozone-SiO_2 layer remained amorphous after PDA at 600 °C. A PDA process is necessary for high-κ dielectrics because a lot of nature defects in high-κ bulk can be reduced to enhance film quality of high-κ gate stack through a high temperature process.

2.2.3.2 Electrical Characteristics on HfO_2/Ozone-SiO_2 Gate Stack

In Fig. 2-6(a)-(b), the ozone-treated HfO_2 with an appropriate PDA exhibited the improved interface properties, and the less hysteresis even after a severe electrical stress. For understanding the influences of different surface treatments, the comparisons of electrical characteristics in several surface treatments were investigated. Fig. 2-7 demonstrates the effects of surface treatments on the leakage current density of 600°C-PDA HfO_2. Both NH_3 and Ozone treatment suppressed the leakage current of the stacked gate dielectric relative to that of a sample that was not subjected to surface treatment. The lower leakage current of ozone treatment is considered to be partial due to the formation of smoother interfaces [11]. Although surface nitridation also reduced the gate leakage current, poor interfacial properties were inevitable; for example, C-V deterioration is apparent for the NH_3-treated sample in Fig. 2-8. The significant negative C-V shift indicates that positive charges arising from the interfacial Si-N layer after surface nitridation [12]. Besides, both the RTO- and Ozone-treated samples exhibited negligible interfacial reactions and V_{FB} shifts, demonstrating that surface oxidation provided interfaces that were superior to those formed after surface nitridation. Fig. 2-9 displays the hysteresis curves of the various samples. The sample that had not been subjected to surface treatment and that which had been subjected to NH_3-mediated nitridation both exhibited large degrees of hysteresis, which were enhanced slightly further after high-temperature PDA. Fortunately, surface oxidation resulted in excellent hysteresis behaviors. Especially, the Ozone-treated sample exhibited almost hysteresis-free feature. Charge trapping phenomena in high-κ dielectrics will have great influences on the electrical characteristics and reliabilities of MOSFETs devices [13-14]. Fig. 2-10 and Fig. 2-11 demonstrated the influences of surface treatments on charge trapping effect. We observe that each of the surface treatment processes improved the value of ΔV_{FB}. In particular, ozone treatment provided excellent experimental results ascribed to the superior interfacial quality of the layer-by-layer and homogeneous growth from the surface to the interface. The Ozone-treated sample exhibited the lowest trapping effects, consistent with the its improved interfacial properties and lower value of ΔV_{FB}. The results demonstrated that a superior interfacial quality of ozone-mediated oxide can efficiently improve the charge trapping effect in such high-κ gate stack. In addition, the reliability was investigated through the behaviors of time dependent dielectric breakdown (TDDB) in Fig. 2-12. After surface treatments, the Ozone-treated sample exhibiting superior performance in TDDB investigation relative to other surface-treated samples. These reasonable experimental results were not only consistent with the previous electrical characteristics but also explain that less charge trapping in the ozone surface treatment can effectively improve the reliability characteristics.

2.2.4 Summary

In this study, we systematically investigated the basic properties of ozone-mediated oxide growth. The low temperature (RT) employed, the slow growth rate, and the self-limiting growth process all provided an ultrathin oxide (<10 Å) of high density and excellent quality, which can be utilized to improve the properties of the HfO_2/Si-substrate interface. The ozone-treated samples exhibited better interfacial properties, a smaller leakage current, negligible hysteresis, lower charge trapping effects and excellent dielectric reliability than did the NH_3 and RTO surface-treated systems. Consequently, this technique is considered as an effective method to improve the interfacial properties between high-κ dielectrics and silicon surfaces.

2.3 The Effect of Fluorine Incorporation on pMOSFETs with HfO_2/SiON Gate Stack

2.3.1 Motivation

HfO_2 has been considered as the potential high-κ candidate in next generation due to its relative high dielectric constants (~25), wide band gap, suitable tunneling barrier heights for both electrons and holes (>1 eV). Moreover, it has been demonstrated the compatibility in CMOS technology and effectively enhanced device performance. However, the quantity of nature traps in high-κ bulk brought a number of pending issues, such as charge trapping/de-trapping leading into threshold voltage instability, and remote phonon scattering induced channel mobility degradation. For the intrinsic properties of a lot of high-κ bulk traps, numerous of investigations have conducted regarding methods to incorporate other elements including nitrogen [15-16], silicon [17-18], and other metallic atoms [19-20] into Hf-based gate dielectrics to improve the film's characteristics. In our work, the method of fluorine implantation into the silicon substrate and consequently thermal driving into HfO_2 bulk was adopted to evaluate the impacts of fluorine incorporation on the device performance and reliability characteristics in pMOSFETs. From our experimental results, fluorine incorporation indeed successfully improved the device performances and enhanced the reliability characteristics. It was verified to reduce the interface states and high-κ bulk traps due to the protection of F-Si bonding and Hf-F bonding formation, respectively [21-23]. In addition, we also demonstrated that the HfO_2 bulk traps were the main cause to dominate whole NBTI degradation.

2.3.2 Experimental Procedures

LOCOS-isolated pMOSFETs device were fabricated on n-type (100) silicon wafers and then implanted fluorine (D: 5E13 cm^{-2}, E: 10keV) with native oxide. Then wafers were cleaned using standard RCA processes with final HF-last. A 1.0 nm thin interfacial oxyntride layer (SiON) using rapid thermal processing in an N_2O ambient at 700 °C. Subsequently, a 3.0 nm HfO_2 layer was deposited by atomic layer deposition (ALD) at 500 °C followed by high temperature post-deposition annealing (PDA) at 700 °C in a N_2 ambient for 30 sec. A 200nm polycrystalline silicon (poly-Si) layer was next deposited by low pressure chemical vapor deposition (LPCVD). After the gate patterning, and source/drain formation, the dopant activation was conducted at 950 °C by rapid thermal annealing (RTA) for 20 sec in an N_2 atmosphere. Subsequent passivation and contact holes formation were done, aluminum metallization subject to the forming gas annealing at 400 °C for 30 minutes was finally performed to complete the device fabrication.

Current-Voltage (I-V) and capacitance-voltage (C-V) characteristics were evaluated using an HP4156C precision semiconductor parameter analyzer and an HP4284 LCR meter, respectively. The equivalent oxide thickness (EOT) of the gate dielectrics was extracted from high-frequency (100 kHz) capacitance-voltage (C-V) curves at strong inversion ($EOT = SiO_2/C_{inv}$) without considering the quantum effect.

The interface trap density (N_{it}) was extracted by charge pumping method (f = 1MHz, fixed amplitude = 1.5V) as following equation.

$$N_{it} = I_{cp}/qA_G f \qquad (2\text{-}1)$$

The increase of total trap density was calculated as

$$\Delta N_{tot} = C\Delta V_t/qA_G \qquad (2\text{-}2)$$

Where A_G is the gate area and C is gate capacitance.

2.3.3 Results and Discussions

2.3.3.1 Electrical Characteristics

Fig. 2-13 illustrated main process flow and experimental conditions. In our work, a substrate implantation with fluorine dose 5E13 cm^{-2} was conducted to accomplish the fluorine incorporation. As literatures reported, the implanted fluorine atom could diffuse from silicon substrate into high-κ gate stack through the high temperature process such as PDA, and dopant activation. Fig. 2-14 showed SIMS profile of fluorine incorporation into Hf-based high-κ gate dielectrics investigated by Y. Ohno et al. [21]. The results demonstrated the method can be feasible to our aim. Fig.2-15 represented the effect of fluorine incorporation on C-V characteristics. The EOT values measured at strong inversion were almost the same regardless of fluorine incorporation. Only a positive C-V shift was observed according to the diffusion of fluorine atom into HfO_2 [21]. The influences of fluorine incorporation on I_d-V_g characteristics were shown in Fig.2-16. The origin of positive V_t shift was similar to the C-V behavior due to fluorine diffusion into HfO_2. An enhanced transconductance (G_m) revealed the improvement at interface of gate dielectric/Si-substrate because of F-Si bonding formation by fluorine incorporation. In Fig.2-17, the elevated device driving current on I_d-V_d characteristics also demonstrated the enhancements of fluorine incorporation. In Fig.2-18(a)-(c), the channel length dependence were investigated on threshold voltage (V_t), maximum transconductance (G_m), and subthreshold swing (S.S), respectively. As we mentioned above, the positive V_t shift observed in fluorine-incorporated samples indicated the diffusion of fluorine atom from silicon substrate into HfO_2. The influences were almost independent of channel length since the diffusion path (silicon substrate → SiON → HfO_2) for fluorine atoms were the same in all channel length conditions. The elevation of maximum G_m was considered as fine efficiency of trap passivation for both interface states and HfO_2 bulk traps (by F-Si bonding and Hf-F bonding, respectively) at shorter channel length. The slight improvement of S.S on fluorine-incorporated samples may imply that a main effect of fluorine incorporation was active in the passivation of HfO_2 bulk traps. As shown in Fig. 2-19, the interface properties were investigated through charge pumping technique. Lower charge pumping current was extracted from fluorine-incorporated samples verified the improvements of fluorine incorporation at gate dielectric/Si-substrate. In Fig. 2-20, the interface degradation in various fluorine dose conditions was investigated after electrical stress. Although fluorine incorporation indeed has suppressed the interface degradation according to the protection of trap passivation, the bond breaking of F-Si bonding (bonding energy: 5.73eV) may still occur after a severe electrical stress. In Fig.2-21, two-frequency charge pumping method was used to investigate the characteristics of interface state and high-κ bulk traps. The experimental results revealed the effective reduction of HfO_2 bulk traps by fluorine incorporation. Moreover, they also implied that the NBTI degradation was mainly dominated by the HfO_2 bulk traps rather than interface degradation.

2.3.3.2 NBTI Investigations

In Fig.2-22, the temperature effect on interface degradation was studied through NBTI process (V_g-V_t = -2.5V, T = 25°C, 75°C, 125°C) in fluorine-incorporated samples. The interface degradation was functional of stress time and dependent on elevated temperatures, like the bond breaking at interface in conventional NBTI results of SiO_2. In Fig.2-23, the NBTI degradation (V_g-V_t = -2.5V, T = 25°C, 125°C) was investigated with respect to fluorine dose conditions. The fluorine-incorporated samples showed a robust ability to resist reliability degradation even at 125°C. Besides, the ΔN_{tot} extracted form experimental results also exhibited the similar behavior to ΔV_t shown in Fig.2-24. Furthermore, in Fig.2-25, the comparisons of N_{it} and N_{bulk} firmly demonstrated that the whole NBTI degradation was strongly dominated by HfO_2 bulk traps. These powerful evidences in NBTI were well consistent with the experimental results shown of two-frequency charge pumping method in Fig.2-21. They all pointed out the significant influences of HfO_2 bulk traps on device reliabilities, and the importance of the trap passivation. In Fig.2-26, the enhanced carrier mobility extracted by Split-CV method was apparently observed in fluorine-incorporated samples. The improvement was considered to be according to that fluorine incorporation could successfully passivate the high-k bulk traps, and further reduce the influence of coulomb scattering on those channel carriers. From these experimental results above, the fluorine incorporation was verified not only to enhance device performances but also to reinforce reliability characteristics attributing to the effective passivation of interface states and HfO_2 bulk traps.

2.3.4 Summary

In order to improve the high-κ bulk properties, the fluorine incorporation was conducted in pMOSFETs with HfO_2/SiON gate stack. This method has successfully reinforced the electrical characteristics and reliability abilities without degrading the C-V characteristics and increasing the equivalent oxide thickness. Besides, the charge trapping effect in high-κ bulk traps is verified to be the dominant of whole NBTI results instead of interface degradation. The enhanced channel carrier mobility is also attained through fluorine incorporation because fluorine successfully reduced the HfO_2 bulk traps and further decreased the coulomb scattering. Overall, fluorine incorporation indeed can effectively ameliorate the bulk properties of high-κ gate dielectrics.

2.4 The Enhancements of Device Performance Using SiN Capping Layer on nMOSFETs with HfO_2/SiON Gate Stack

2.4.1 Motivation

High-κ dielectrics were considered as the most potential candidates to replace the conventional SiO_2 thin film because of a thicker thickness can effectively suppress the large direct tunneling leakage current while maintaining the same gate capacitance. However, the application of high-κ gate dielectrics brings significant mobility degradation. For the enhancement of channel carrier mobility, many investigations were studied through the strain effect including globe strain and locally strain [24-25]. The globe strain is usually conducted by changing the silicon substrate with other alternative materials, such as Ge, SiGe, and strained Si substrates (hence it also called: substrate strain), but expensive cost is the major issue [26]. On the other hand, the locally strain can be performed through changing partial fabrication conditions with a compatible standard CMOS process including shallow trench isolation (STI), sidewall spacer, strained S/D (ex:SiGe-S/D) [27-28], contact etch-stop-layers (CESLs) [29-31], strained gate (Strained Poly-Si Gate and Silicide Gate), and impurity implantation into films (Ge, As implant into capping layers) [32] (hence it also called : process-induced strain). This method is convenient and less cost to carry out the enhancements of channel carrier mobility. In our study, a tensile strain was performed by the CESLs method using SiN capping as a passivation layer on nMOSFETs. The mechanism of tensile strain revealed the prominent enhancement on nMOSFETs is according to the electrons in the two-fold valley accompanied with lower effective mass and higher mobility (μ). The detailed mechanism of the band split induced by strain effect and its impacts on the enhancements of channel mobility are illustrated in Fig.2-27. From our experimental results, the enhanced device performances were apparently observed to verify the improvement of CESLs strain. Moreover, the strained samples have been demonstrated to have more significant high-κ bulk traps leading into a severe PBTI degradation. The influences of strain effect on both device performances and reliabilities were discussed in this section.

2.4.2 Experimental Procedures

LOCOS-isolated nMOSFETs device were fabricated on p-type (100) silicon wafers. Then wafers were cleaned using standard RCA processes with final HF-last. A 0.8 nm thin interfacial oxyntride layer (SiON) using rapid thermal processing in an N_2O ambient at 700 °C. Subsequently, a 3.0 nm HfO_2 layer was deposited by atomic layer deposition (ALD) at 500 °C followed by high temperature post-deposition annealing (PDA) at 700 °C in a N_2 ambient for 30 sec. A 200nm polycrystalline silicon (poly-Si) layer was next deposited by low pressure chemical vapor deposition (LPCVD). After the gate patterning, and source/drain formation, the dopant activation was conducted at 950 °C by rapid thermal annealing (RTA) for 20 sec in an N_2 atmosphere. Subsequent passivation layers were split as w/o SiN, 200 nm SiN, and 300 nm SiN. After contact holes formation was done, aluminum metallization subject to the forming gas annealing at 400 °C for 30 minutes was finally performed to complete the device fabrication. The related process flow was exhibited explicitly in Fig.2-28.

Current-Voltage (I-V) and capacitance-voltage (C-V) characteristics were evaluated using an HP4156C precision semiconductor parameter analyzer and an HP4284 LCR meter, respectively. The equivalent oxide thickness (EOT) of the gate dielectrics was extracted from high-frequency (100 kHz) capacitance-voltage (C-V) curves at strong inversion (EOT = SiO_2/C_{inv}) without considering the quantum effect. The interface trap density (N_{it}) was extracted by charge pumping method (f = 1MHz, fixed amplitude = 1.5V) as following equation.

$$N_{it} = I_{cp}/qA_G f \qquad (2\text{-}1)$$

The increase of total trap density was calculated as

$$\Delta N_{tot} = C\Delta V_t/qA_G \qquad (2\text{-}2)$$

Where A_G is the gate area and C is gate capacitance.

2.4.3 Results and Discussions

2.4.3.1 Electrical Characteristics

C-V curves and EOT values were shown in Fig. 2-29(a) and Fig. 2-29(b), respectively. The C-V characteristics were almost identical with various CESLs strain conditions, and the film thickness was fairly close in all samples with the EOT deviation less than 2 Å. The results indicated that the CESLs strain effect do not change these basic device properties. In Fig. 2-30(a)-(b), the device performances apparently got the benefit of strain force shown on the driving current (I_d) and transconductance (G_m) with the elevated SiN thickness. Beside, in Fig. 2-31, the CESLs strain was clearly revealed to effectively promote the device ability through I_d-V_d characteristics. These achievements demonstrated the successful enhancements of tensile CESLs strain on nMOSFETs with the high-κ gate dielectrics what were denounced as the critical issue of mobility degradation. In Fig. 2-32, the channel length dependences on $G_{m.MAX}$ exhibited the enhancements of strain effect were apparently effective in small geometry. Therefore, the experimental results tell us that strain technology is a practical method to enrich device performance, especially when CMOS technology in the aggressive scaling is necessary to adopt the high-k gate dielectrics to restrain the large direct tunneling gate leakage current, even through high-κ itself accompanied with the drawback of mobility degradation. In Fig. 2-33, interface properties at SiON/Si-substrate were investigated through charge pumping method. A reduces of donor-like traps and interface states were found because a hydrogen passivation was conducted during SiN deposition by PECVD [33-34].

2.4.3.2 PBTI Degradation and Traps Properties

The PBTI degradation was investigated with respect to CESLs strain conditions in Fig. 2-34. Significant reliability degradation was found in samples with elevated CESLs strain. The PBTI degradation was fine fitting as the charge trapping model reported by Sufi Zafar et al. [35].

$$\Delta V_T = \Delta V_{\max}\left[1-\exp\left(-\left(\frac{t}{\tau_{c0}}\right)^{\gamma}\right)\right] \tag{2-3}$$

The evidences point out that the electron trapping effect remains to be the dominant of whole PBTI degradation with the employment of high-κ gate dielectrics although the utilization of CESLs strain may have some unknown influences on device reliability. The dependence of applied stress voltage on PBTI degradation was illustrated in Fig. 2-35. The strained samples showed severer degradation than samples w/o SiN. In many related studies, the PBTI degradation in high-κ gate dielectrics is mainly contributed by the electron trapping at high-κ bulk traps, and electron trapping phenomenon in high-κ bulk commonly has strong dependence on applied stress voltage. As the results, an enlargement of ΔV_t difference observed at stricter stress condition (V_g-V_t = 2.0V) between samples with SiN and w/o SiN was considered to be associated with the imparity of high-κ bulk traps resulted form various CESLs strain conditions. Moreover, the improved interface as we discussed above has the contrary contribution compared with the tendency of whole PBTI degradation (ΔV_t). Therefore, these experimental results are evident to demonstrate that the CESLs strain indeed affects the high-κ bulk traps and further sways the reliability characteristics. In order to verify the influences of tensile CESLs strain on HfO_2 bulk traps, the high-κ trap properties were further investigated through related carrier transport mechanisms in high-κ gate dielectrics. In Fig. 2-36(a)-(b) Frenkel-Poole fitting was modeled for both samples w/o SiN capping and with 300nm SiN capping since Frenkel-Poole emission is the well known trap-assisted conduction mechanism which is suitable for intrinsic defect-rich high-κ dielectrics. The Frenkel-Poole emission is as below [36]:

$$J = B \times a \times E_{eff} \times \exp\left(\frac{-q(\phi_B - \sqrt{aqE_{eff} / \pi\varepsilon_{HfO2}\varepsilon_0})}{kT}\right) \qquad (2\text{-}4)$$

$$B = q\mu N_T \,,\ \mathrm{a} = \frac{\varepsilon_{SiO2}}{\varepsilon_{HfO2}}$$

The extracted trap energy levels with respect to conduction band of HfO_2 were extracted as Φ_B = 0.92 eV in samples w/o SiN capping and Φ_B = 0.93 eV in samples with 300 nm SiN capping, respectively. The experimental results evidently indicated that CESLs strain does not change the intrinsic properties of HfO_2 bulk traps themselves even though this methodology was demonstrated to have some influences on trap generation during PBTI degradation discussed above.

In another aspect of carrier transport through tunneling mechanism, Fowler-Nordheim tunneling fitting was modeled for samples w/o SiN capping and with SiN capping (200 nm & 300 nm) in Fig. 2-37. The Fowler-Nordheim tunneling is as below [36]:

$$J = AE_{eff}^{\ 2}\exp\left[-\frac{B}{E_{eff}}\right];\ \mathrm{A}=\frac{\mathrm{q}^{3}}{16\pi\hbar\Phi_{\mathrm{B}}},\ \mathrm{B}=\frac{4}{3}\frac{(2m_{ox})^{1/2}}{q\hbar}\Phi_{\mathrm{B}}^{\ 3/2} \qquad (2\text{-}5)$$

The nearly identical slopes of FN-tunneling fitting are the powerful evidences once again to demonstrate that CESLs strain does not change the trap energy levels and intrinsic charge trapping behaviors in HfO_2. Furthermore, the characteristics of HfO_2 bulk traps before and after PBTI stress were also investigated by means of flicker noise measurement in samples w/o SiN capping and with 300 nm SiN capping in Fig. 2-38. The elevated γ value extracted from flicker noise signal indicated the increase of trap density after PBTI degradation [37]. In Fig. 2-39, for the analysis of the variation of HfO_2 bulk traps, the effective trap density was transformed from flicker noise signal using the unified model as below [38-40]:

$$\begin{aligned} S_{VG}(f) &= \frac{kTq^{2}}{\gamma fWLC^{2}}\left(1\pm\frac{\mu_{eff}N(x)}{\mu_{C0}\sqrt{N_{inv}}}\right)^{2}N_{t}(E_{fn}) \\ &\approx \frac{kTq^{2}}{\gamma fWLC^{2}}N_{t}(E_{fn}) \Rightarrow N_{t}(E_{fn}) = \frac{kTq^{2}}{\gamma fWLC^{2}}S_{VG}(f) \qquad (2\text{-}6) \end{aligned}$$

where κT = 0.0259 eV, q = 1.6×10^{-19} C, $\gamma = 4.6\times10^{7}$ cm^{-1} for HfO_2, W = 10 μm, and L = 1μm. The calculated results indicated that samples with SiN capping had a large number of initial bulk traps. Sequentially, a severer bulk trap generation of HfO_2 was observed in samples with CESLs strain, and it led to more significant PBTI degradation. From the results, it is assumed that CESLs strain may have some impacts on the atomic boding in HfO_2 bulk to make film properties become the inferior quality. Thus a numbers of trap density and the following poor reliability degradation are visible to observed in strained-samples. From the overall impacts of tensile CESLs strain acted on nMOSFETs with HfO_2/SiON gate stack, the locally strain using a SiN capping is verified to increase the quantity of HfO_2 bulk traps during PBTI degradation, but the intrinsic properties of HfO_2 bulk traps are independent of CESLs strain.

2.4.4 Summary

In this study, we have successfully enhanced the device performance through a tensile strain force produced by a SiN capping method. The experimental results ensure that the CESLs strain is an effective method to solve the mobility degradation after using the high-k dielectrics as the gate stack in CMOS technology. In addition, we also discovered that the CESLs strain has apparent impacts to increase the magnitude of initial bulk traps in HfO_2 and lead a severer bulk trap generation to be the dominant of whole PBTI degradation. However, the utilization of CESLs strain does not change the intrinsic properties of HfO_2 bulk traps, even though it results in a negative side of large trap density. Finally, we conclude that CESLs strain technology indeed has the benefits to better device performance but a reliability issue has to be the serious concern.

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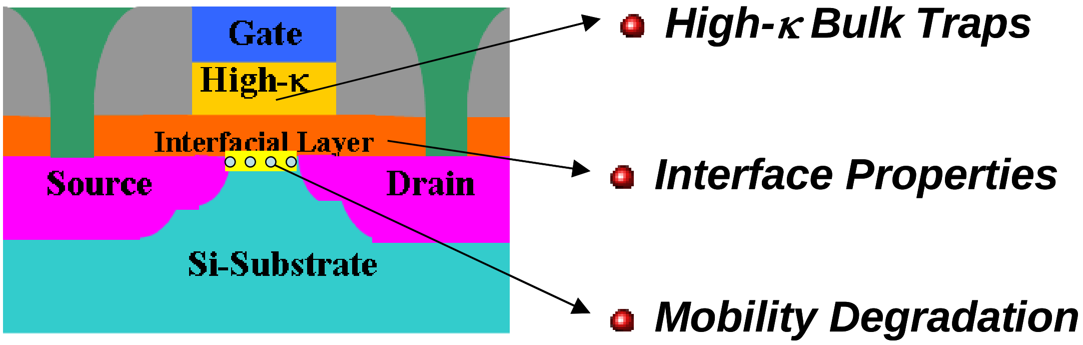

Gate
High-κ
Interfacial Layer
Source
Drain
Si-Substrate
High-κ Bulk Traps
Interface Properties
Mobility Degradation

Fig. 2-1 Key issues of high-κ gate dielectrics applied on CMOS technology.

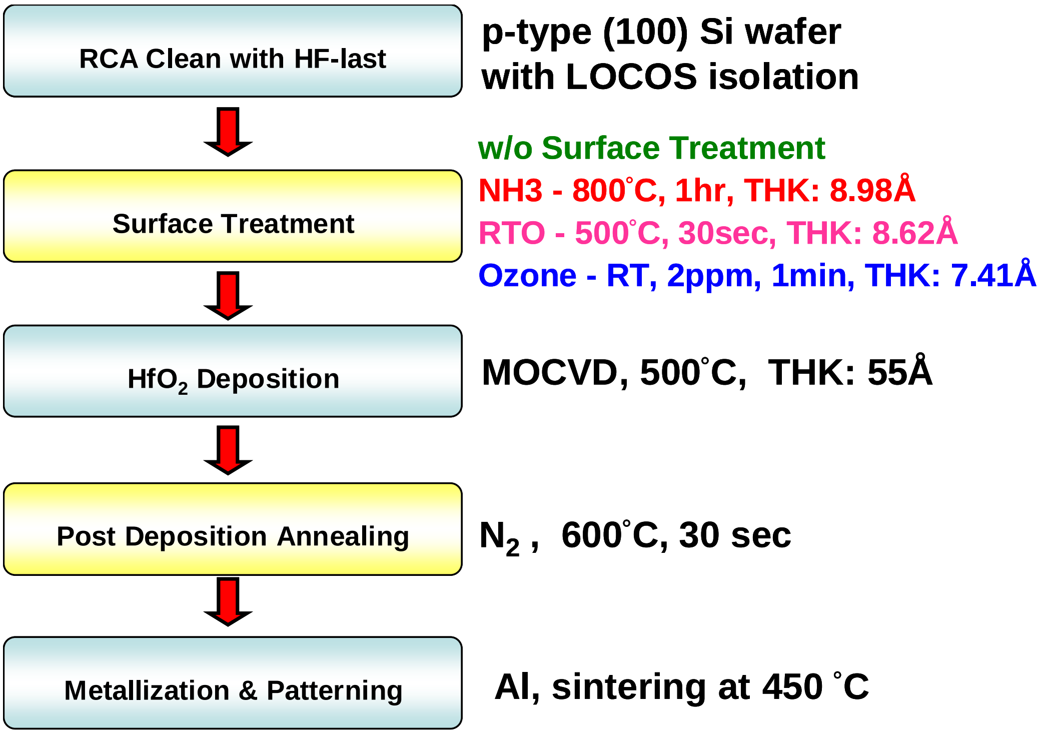

RCA Clean with HF-last
p-type (100) Si wafer
with LOCOS isolation
w/o Surface Treatment
NH3 - 800˚C, 1hr, THK: 8.98Å
Surface Treatment
RTO - 500˚C, 30sec, THK: 8.62Å
Ozone - RT, 2ppm, 1min, THK: 7.41Å
HfO_2 Deposition
MOCVD, 500˚C, THK: 55Å
Post Deposition Annealing
N_2 , 600˚C, 30 sec
Metallization & Patterning
Al, sintering at 450 ˚C

Fig. 2-2 Process flows and experimental conditions with the ozone surface treatment.

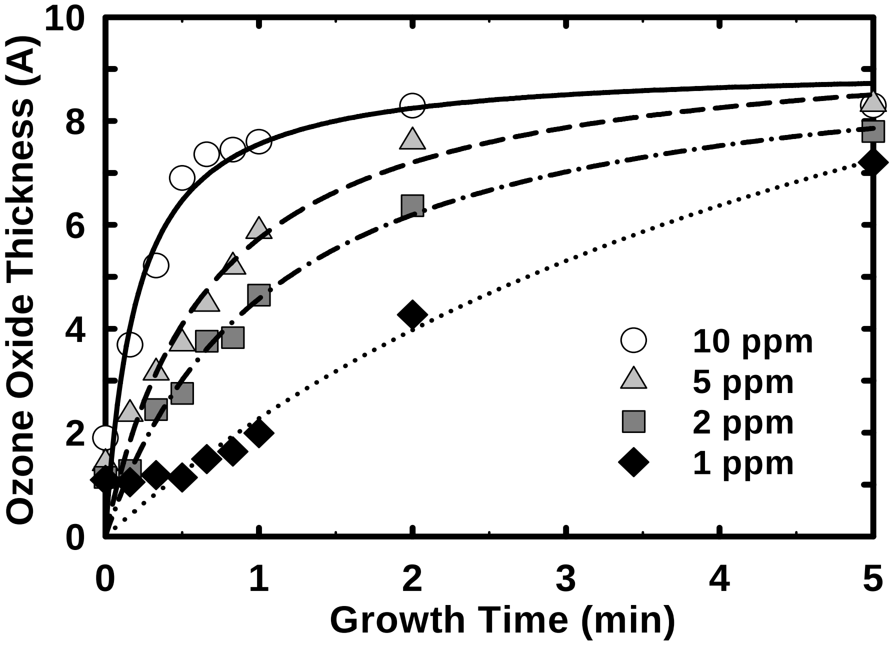


Fig. 2-3 Growth curves of ozone-mediated oxides plotted as a function of the concentration of ozone in water.

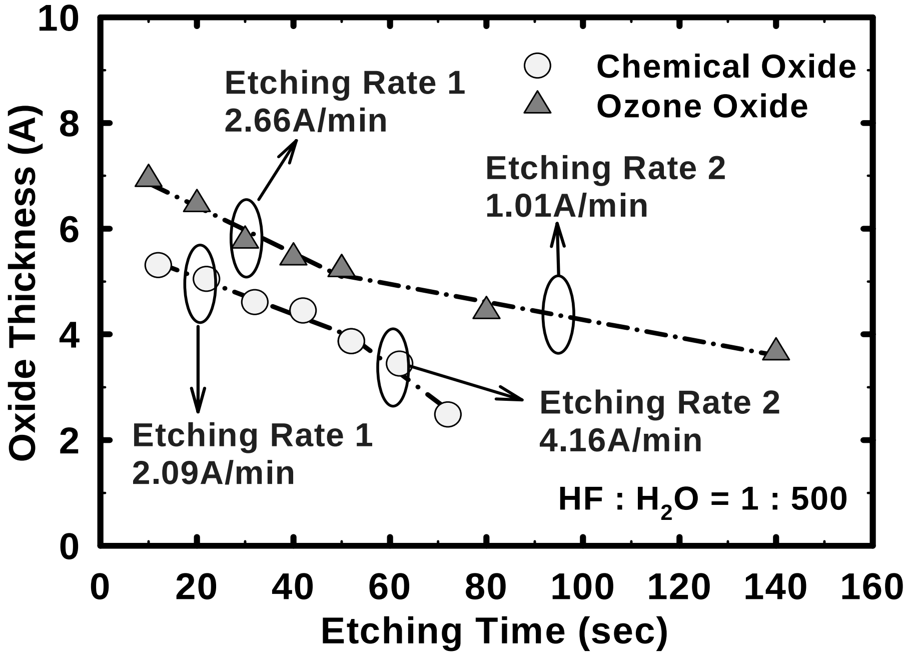


Fig. 2-4 Comparison of the etching rates at $HF:H_2O = 1:500$ of the ozone-mediated oxide to that of the chemical oxide formed by RCA cleaning without HF-last.

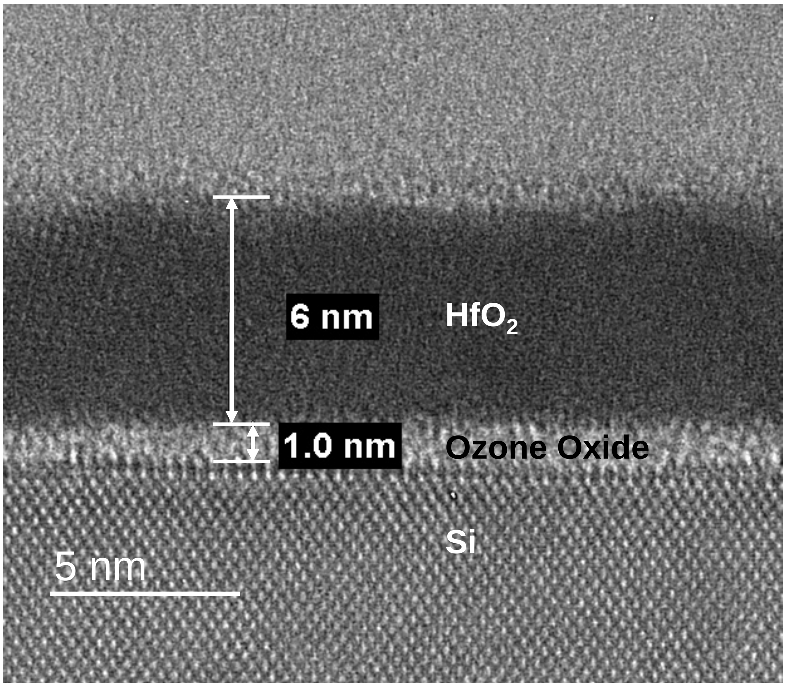
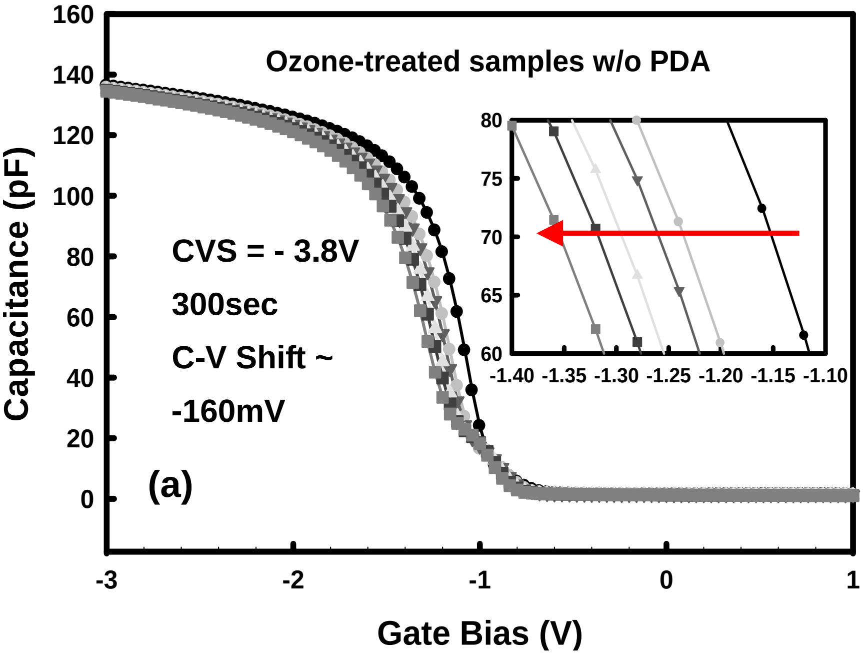

6 nm
HfO2
1.0 nm
Ozone Oxide
Si
5 nm

Fig. 2-5 HRTEM image of the ozone-treated HfO_2 after PDA at 600 °C.



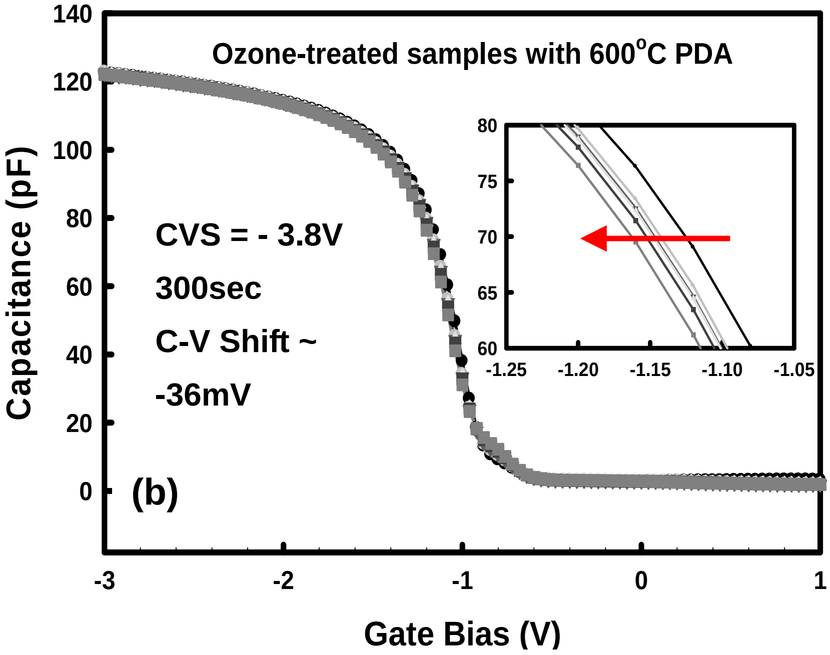


Fig. 2-6 (a) Ozone-treated HfO_2 w/o PDA (b) Ozone-treated HfO_2 with PDA. Ozone-treated HfO_2 with an appropriate PDA exhibit the improved interface, and the less hysteresis even after a severe electrical stress.

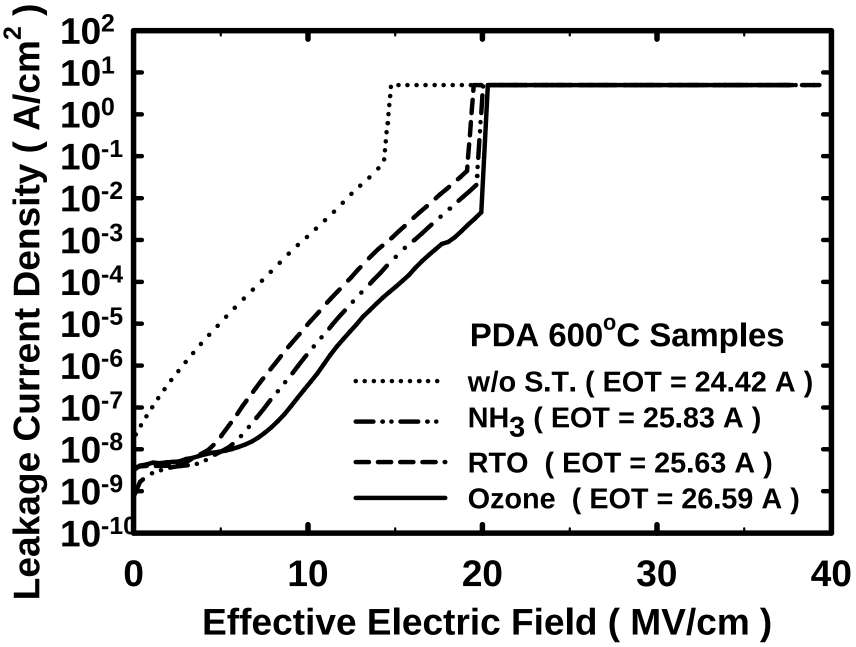


Fig. 2-7 Leakage current density of HfO_2 gate stacks with respect to the various surface treatment processes.

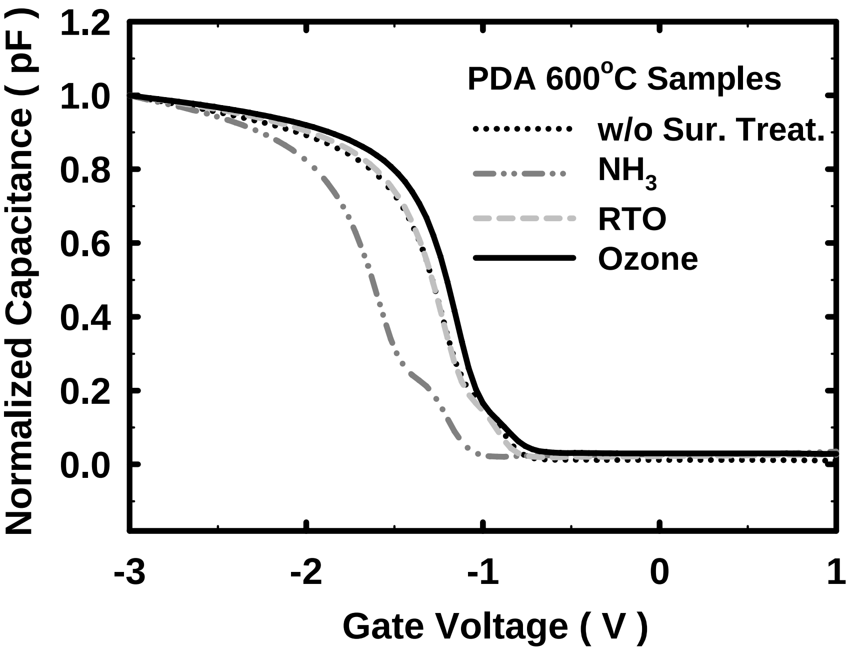


Fig. 2-8 C-V characteristics of HfO_2 stacked gate dielectrics with respect to various surface treatment processes

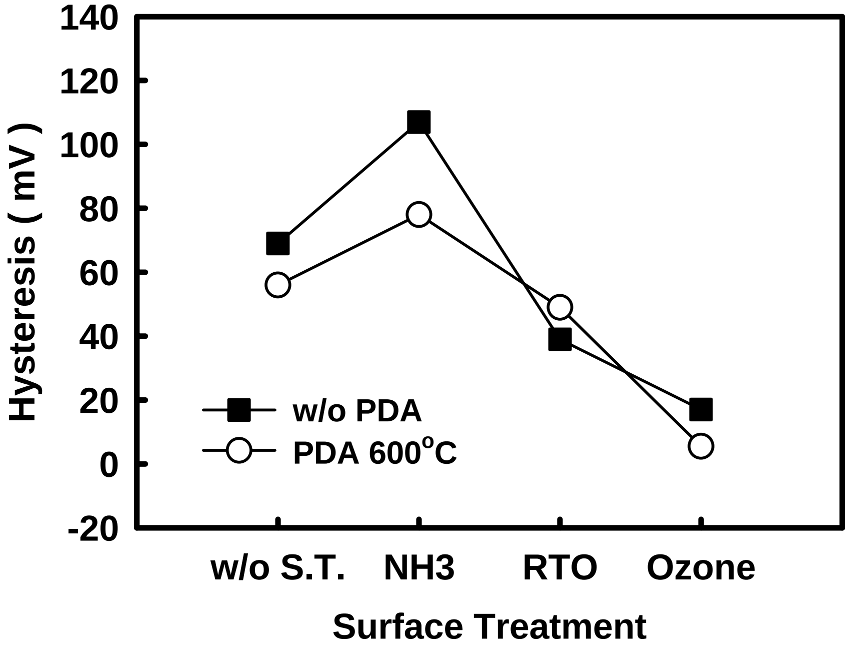


Fig. 2-9 Hysteresis curves obtained with respect to the various surface treatment processes.

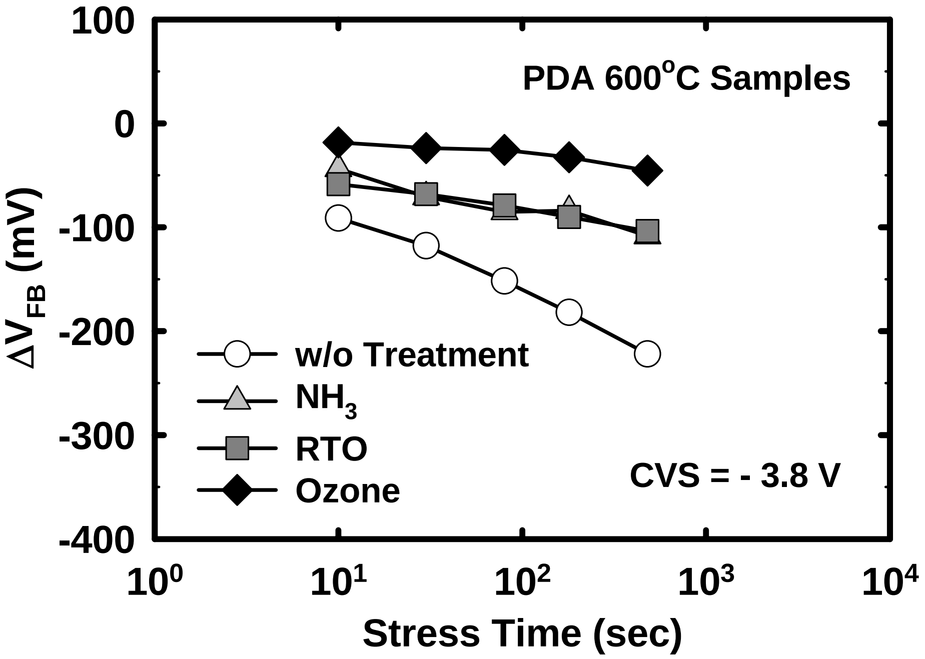


Fig. 2-10 Plots of ΔV_{FB} under a CVS of -3.8 V with respect to the various surface treatment processes.

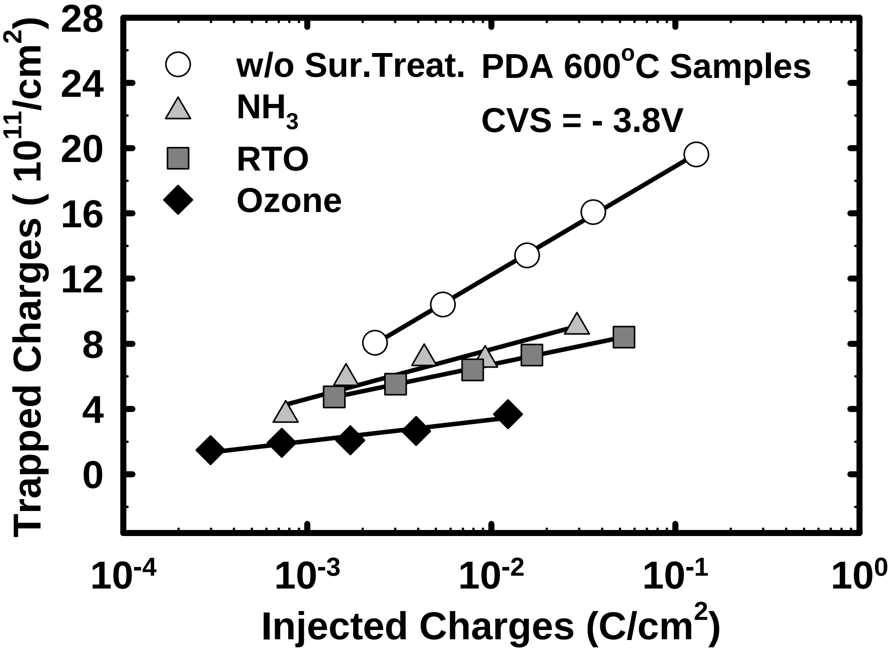


Fig. 2-11 Charge trapping effects plotted with respect to the various surface treatment processes.

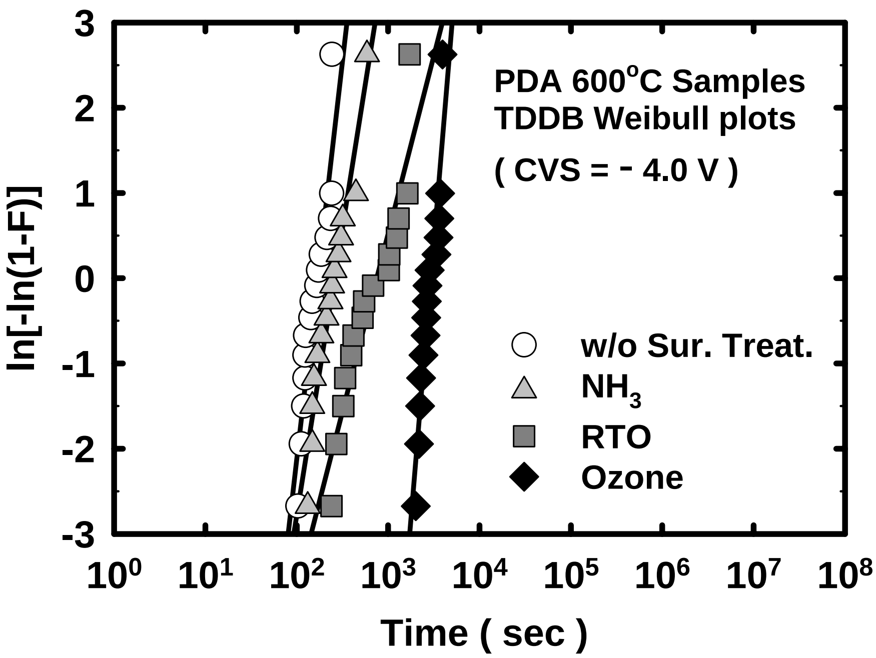


Fig. 2-12 Investigations of reliability obtained in TDDB measurements with respect to the various surface treatment processes.

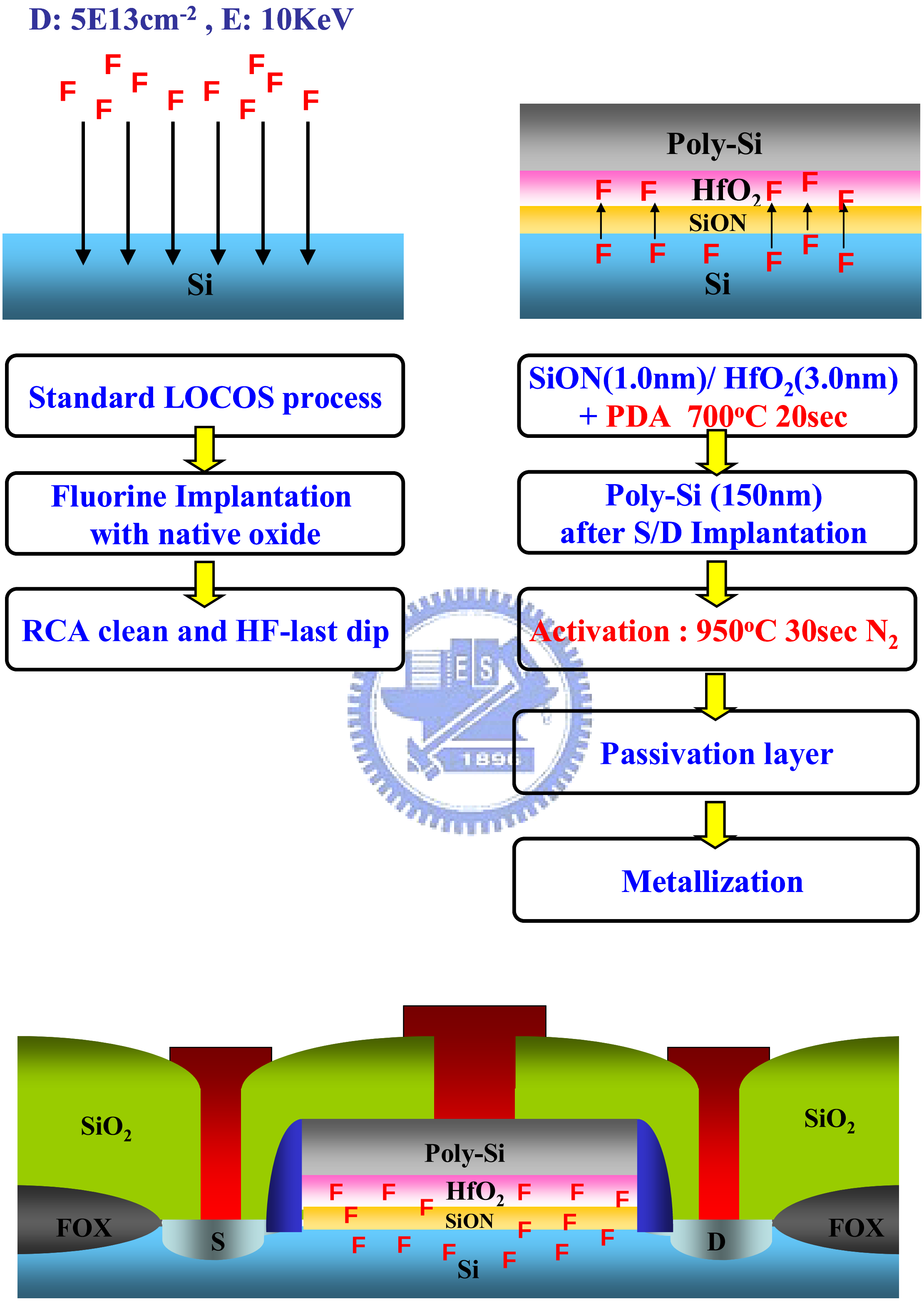

D: 5E13cm-2 , E: 10KeV
F
Si
Standard LOCOS process
Fluorine Implantation with native oxide
RCA clean and HF-last dip
Poly-Si
HfO2
SiON
Si
SiON(1.0nm)/ HfO2(3.0nm) + PDA 700oC 20sec
Poly-Si (150nm) after S/D Implantation
Activation : 950oC 30sec N2
Passivation layer
Metallization
SiO2
FOX
S
D
Poly-Si
HfO2
SiON
Si
SiO2
FOX

Fig. 2-13 Process flow of fluorine incorporation.

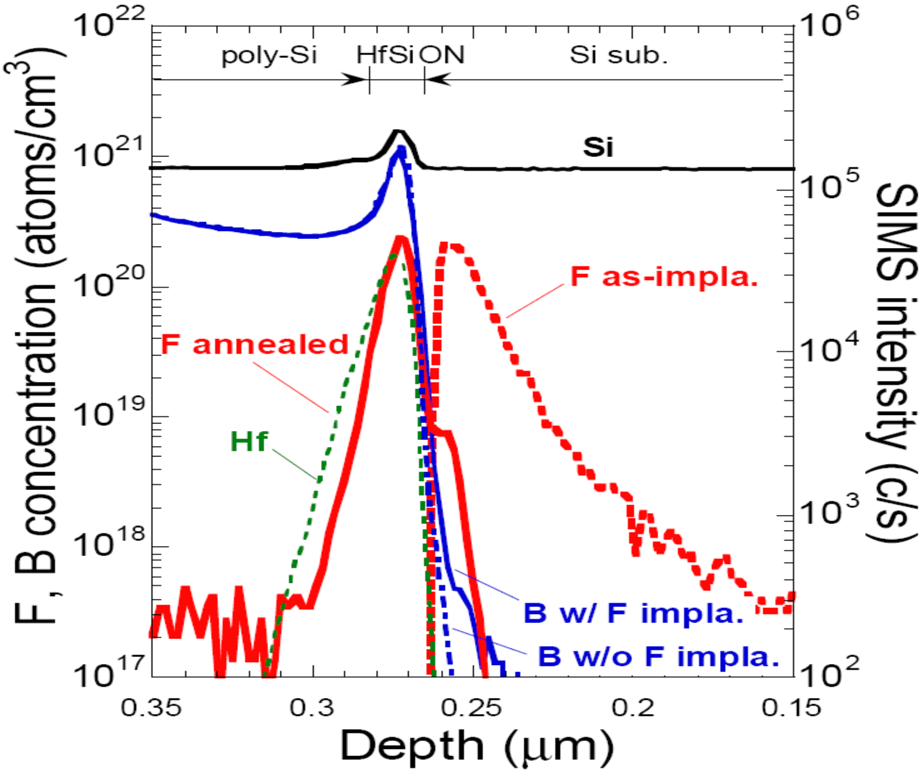


Fig. 2-14 SIMS profile of fluorine incorporation into Hf-based high-κ gate dielectrics [21].

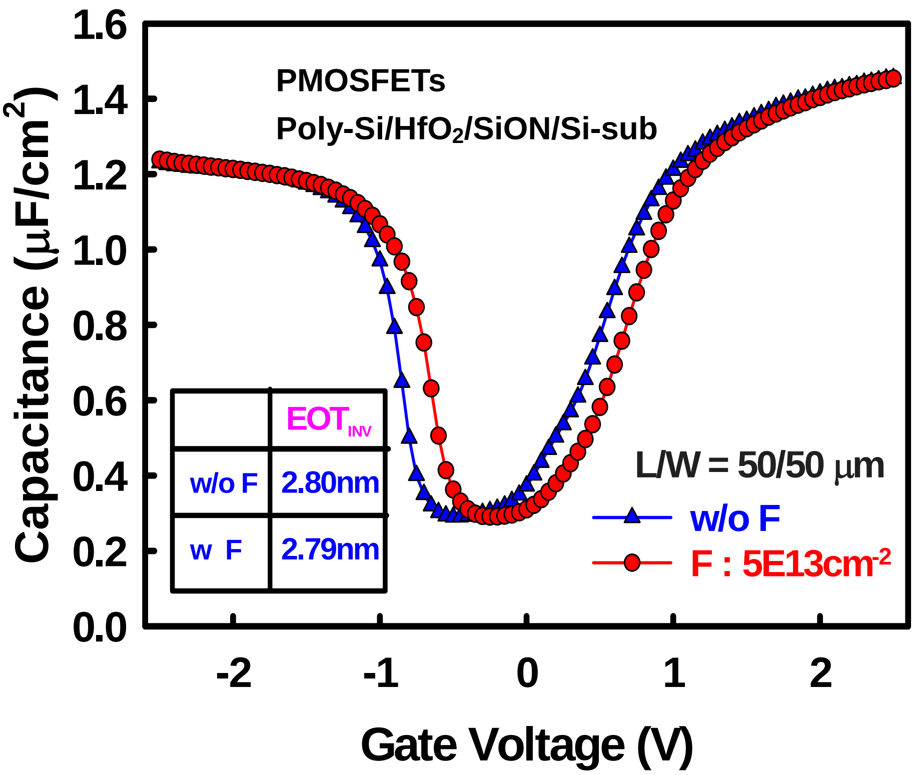


Fig. 2-15 Effect of fluorine incorporation was shown on C-V characteristics. A positive C-V shift was according to the diffusion of fluorine atom into HfO_2 [21].

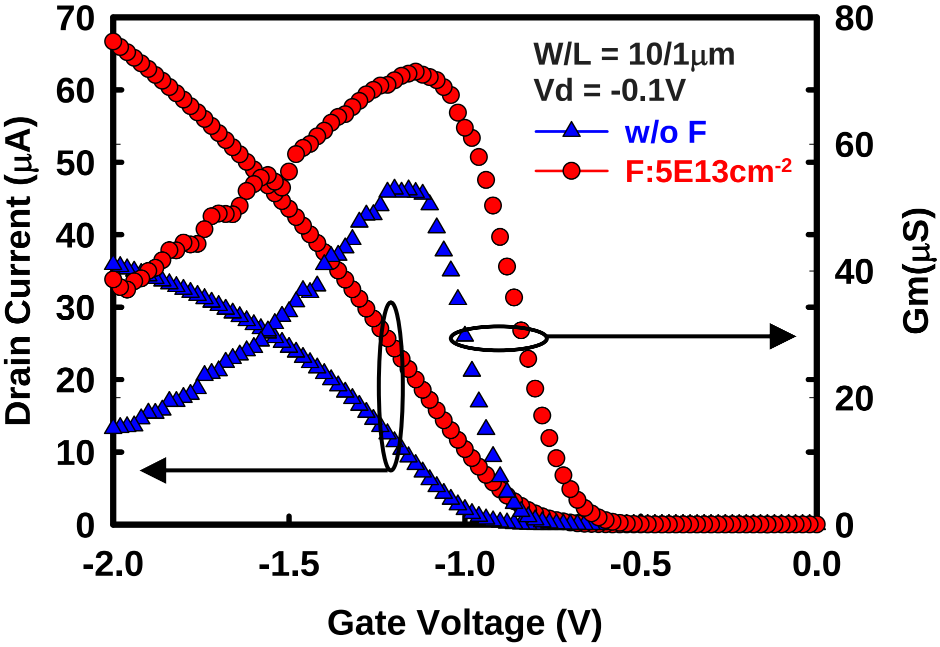


Fig. 2-16 The I_d-V_g characteristics showed the influences of fluorine incorporation. The mechanism of positive V_t shift was similar to the C-V behavior due to fluorine diffusion into HfO_2. The enhanced G_m revealed the improvement at interface of gate dielectric/Si-substrate because of F-Si bonding by fluorine incorporation [22].

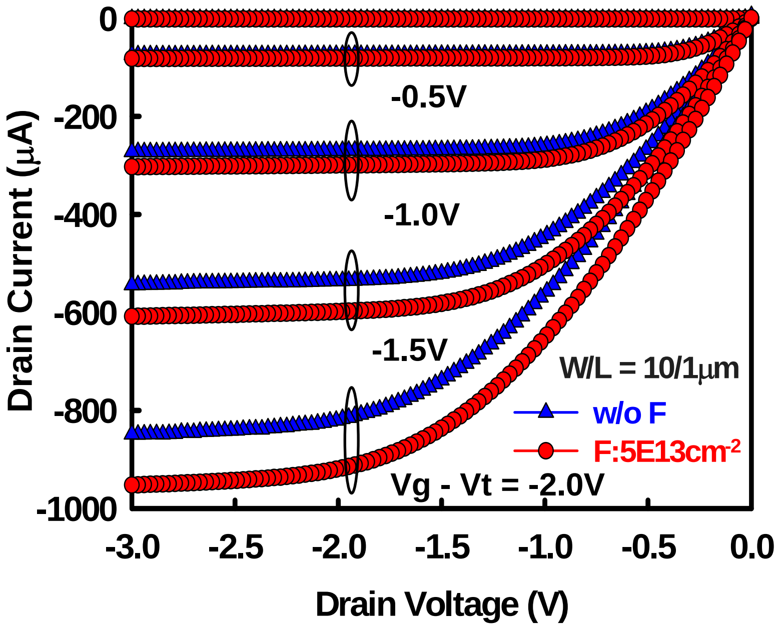


Fig. 2-17 The I_d-V_d characteristics showed the enhancement of fluorine incorporation on device driving current.

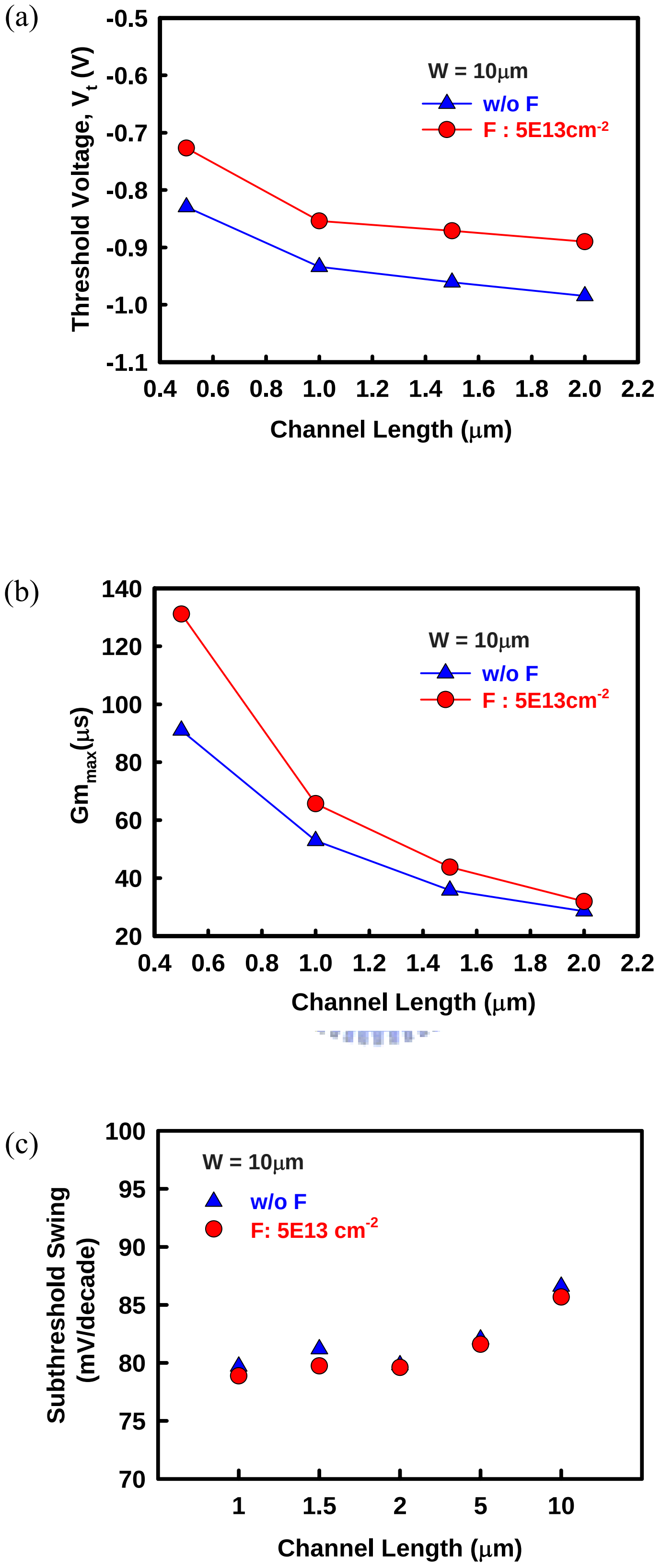


Fig. 2-18 The dependence of channel length on (a) threshold voltage, V_t (b) maximum transconductance, Gm (c) subthreshold swing, S.S

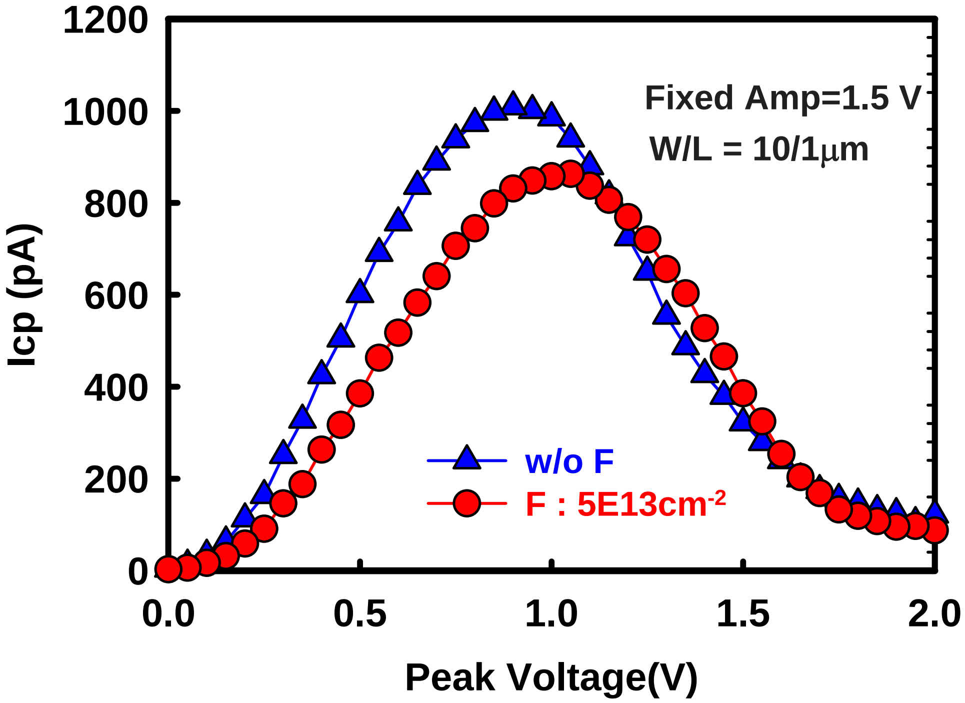


Fig. 2-19 Improvement of fluorine incorporation at gate dielectric/Si-substrate was demonstrated by charge pumping current.

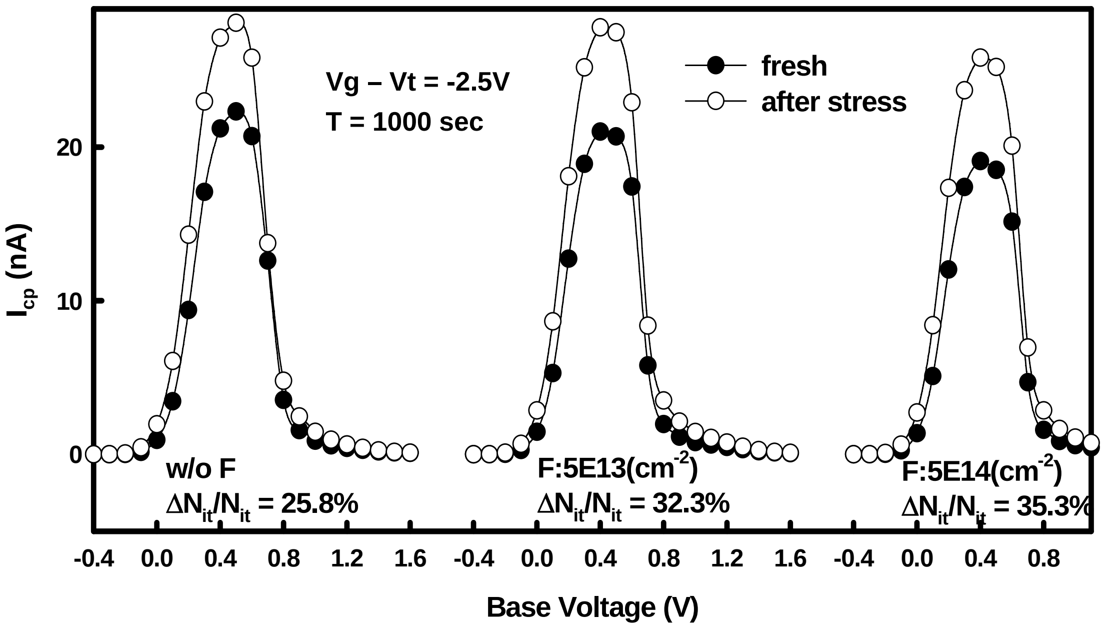


Fig. 2-20 The interface degradation in various fluorine dose conditions was investigated after electrical stress.

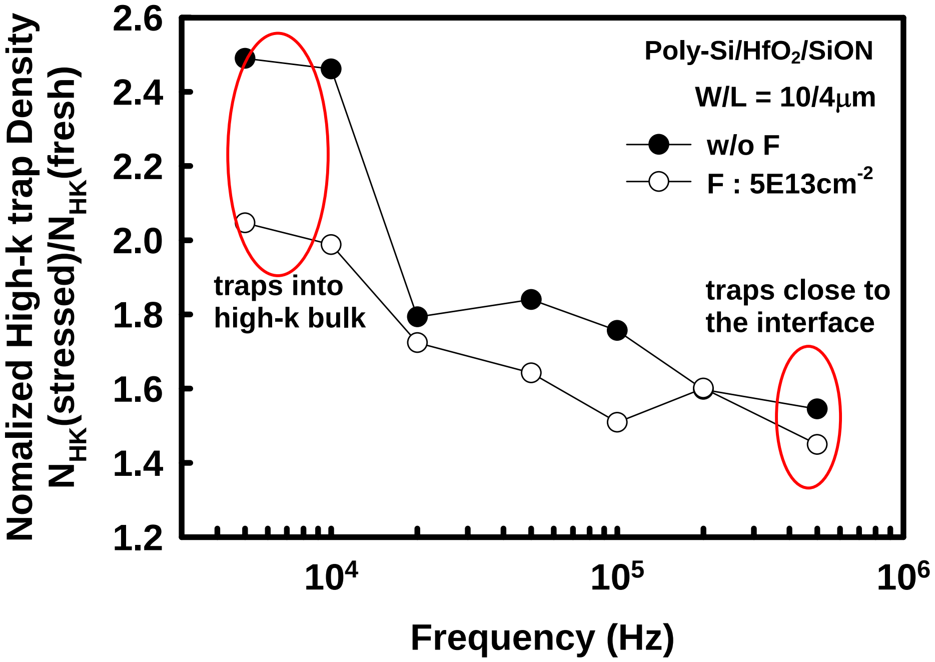


Fig. 2-21 Two-frequency charge pumping method revealed the characteristics of interface state and high-κ bulk traps.

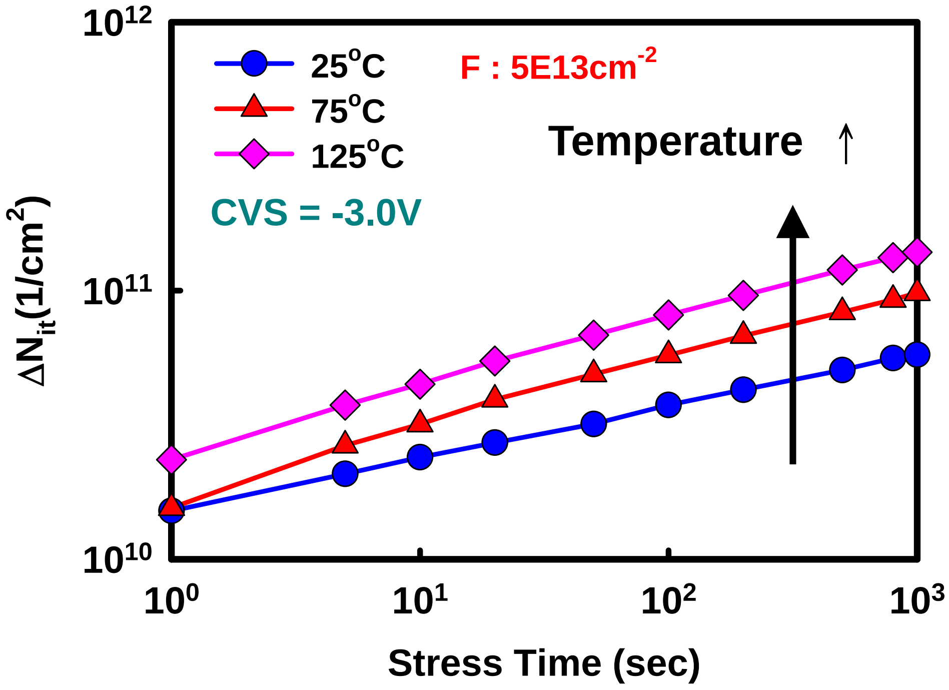


Fig. 2-22 The influence of temperature effect on interface degradation was studied through the NBTI process.

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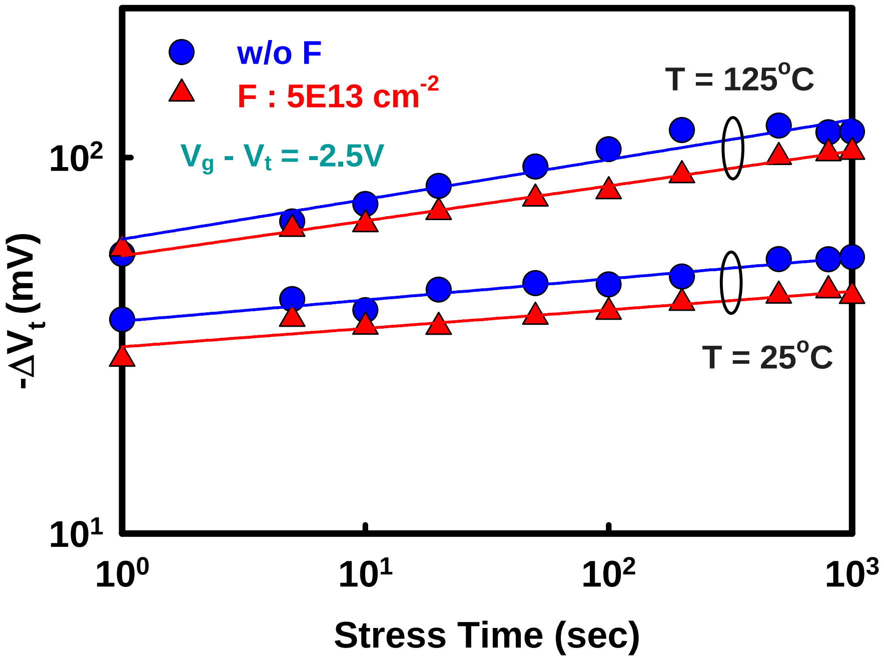


Fig. 2-23 The NBTI degradation was investigated with respect to fluorine dose conditions. The fluorine-incorporated samples showed a robust ability for reliability characteristics even at 125 °C.

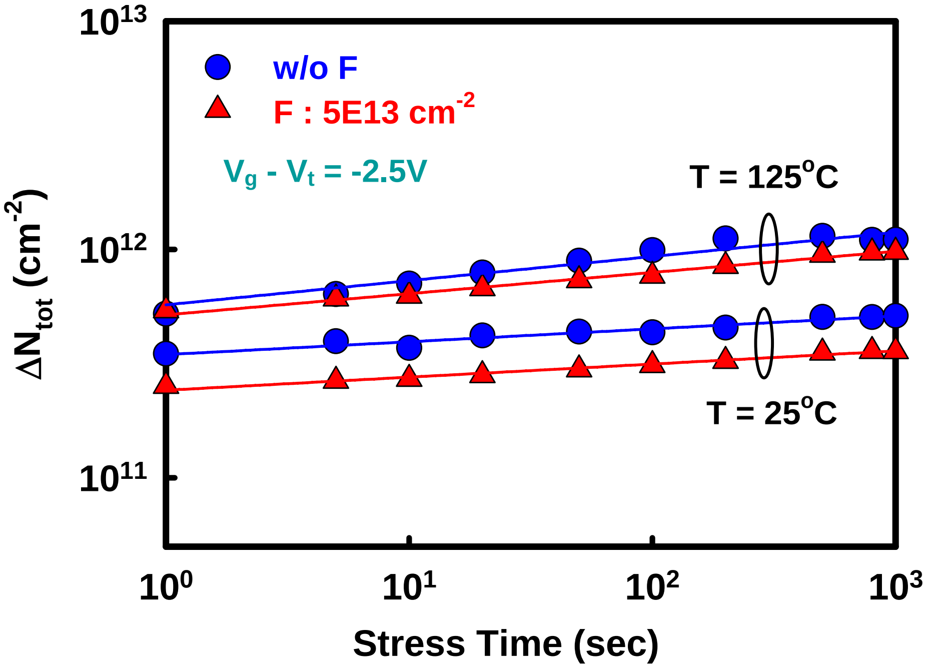


Fig. 2-24 The behavior of total trap generation during NBTI degradation.

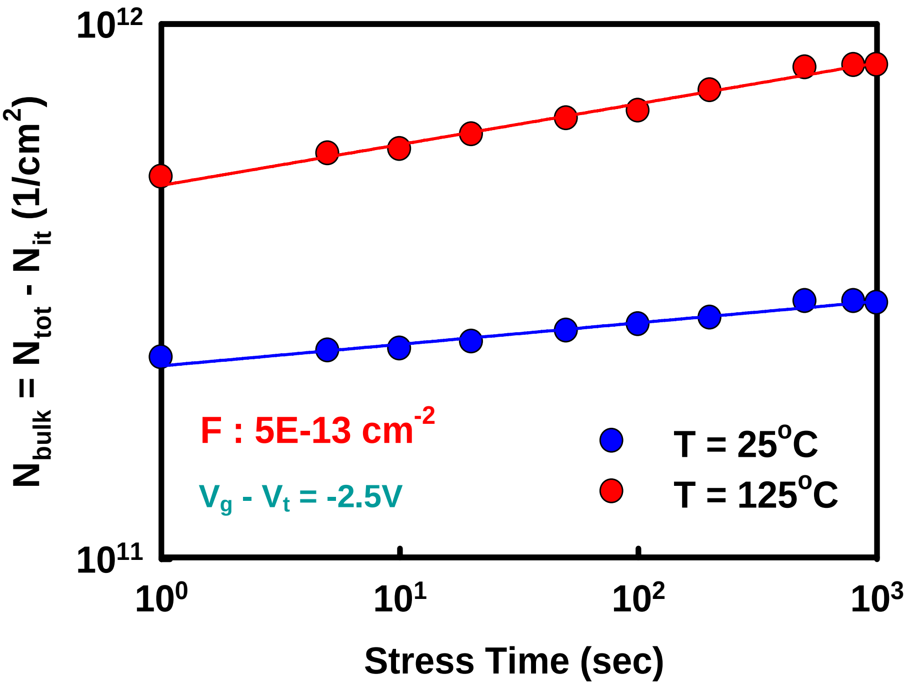


Fig. 2-25 The whole NBTI degradation was dominated by high-κ bulk degradation rather than the interface degradation.

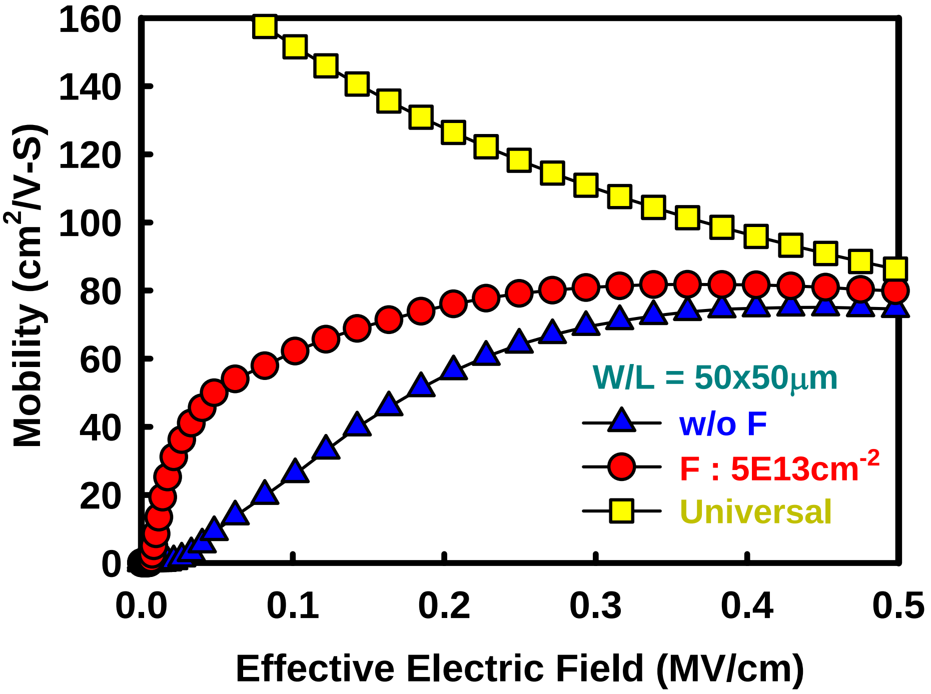


Fig. 2-26 Channel carrier mobility was extracted by Split-CV method. The enhancement of fluorine-incorporated samples was considered to be according to the reduction of high-κ bulk traps.

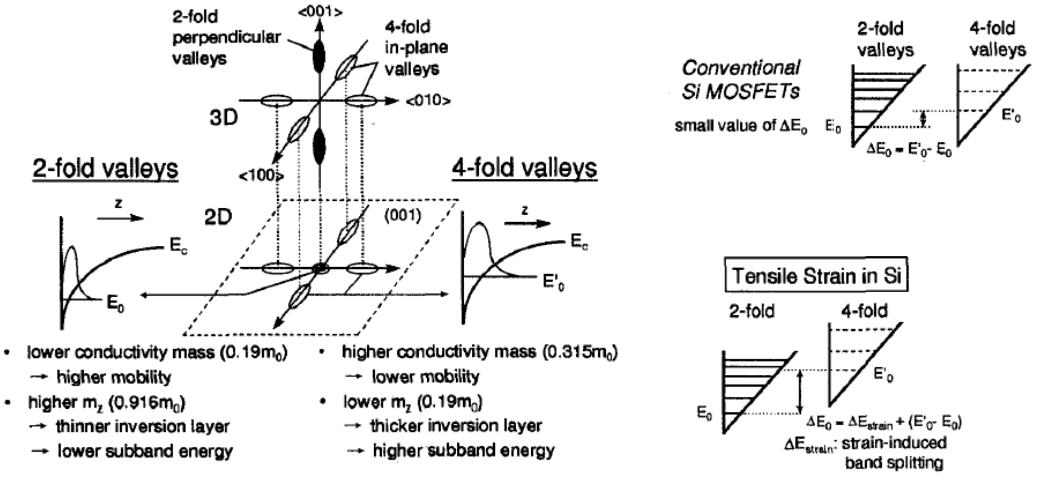
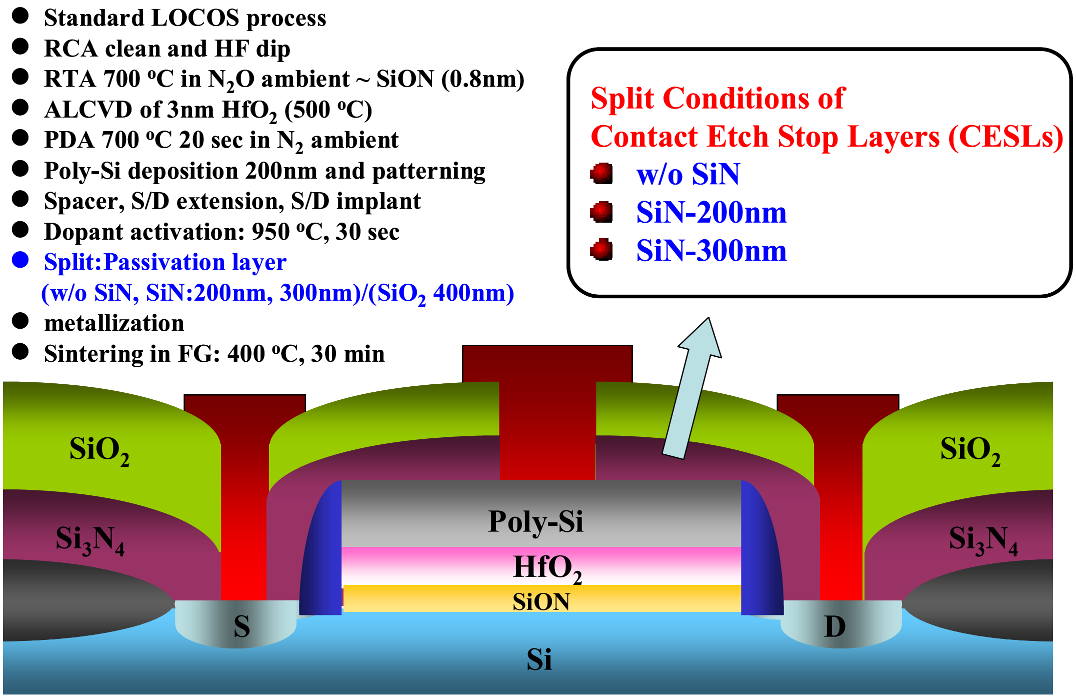

2-fold perpendicular valleys
<001>
4-fold in-plane valleys
<010>
3D
<100>
2-fold valleys
4-fold valleys
2D
(001)
z
E_c
E_0
z
E_c
E'_0
• lower conductivity mass (0.19m_0)
→ higher mobility
• higher m_z (0.916m_0)
→ thinner inversion layer
→ lower subband energy
• higher conductivity mass (0.315m_0)
→ lower mobility
• lower m_z (0.19m_0)
→ thicker inversion layer
→ higher subband energy
Conventional Si MOSFETs
small value of ΔE_0
2-fold valleys
4-fold valleys
E_0
E'_0
ΔE_0 = E'_0 - E_0
Tensile Strain in Si
2-fold
4-fold
E_0
E'_0
ΔE_0 = ΔE_strain + (E'_0 - E_0)
ΔE_strain: strain-induced band splitting

Fig. 2-27 Mechanism of strain effect influences on the enhancements of channel mobility.



- Standard LOCOS process
- RCA clean and HF dip
- RTA 700 °C in N_2O ambient ~ SiON (0.8nm)
- ALCVD of 3nm HfO_2 (500 °C)
- PDA 700 °C 20 sec in N_2 ambient
- Poly-Si deposition 200nm and patterning
- Spacer, S/D extension, S/D implant
- Dopant activation: 950 °C, 30 sec
- Split:Passivation layer (w/o SiN, SiN:200nm, 300nm)/(SiO_2 400nm)
- metallization
- Sintering in FG: 400 °C, 30 min

Split Conditions of Contact Etch Stop Layers (CESLs)

- w/o SiN
- SiN-200nm
- SiN-300nm

Fig. 2-28 Device structure and split conditions of contact etch stop layers (CESLs).

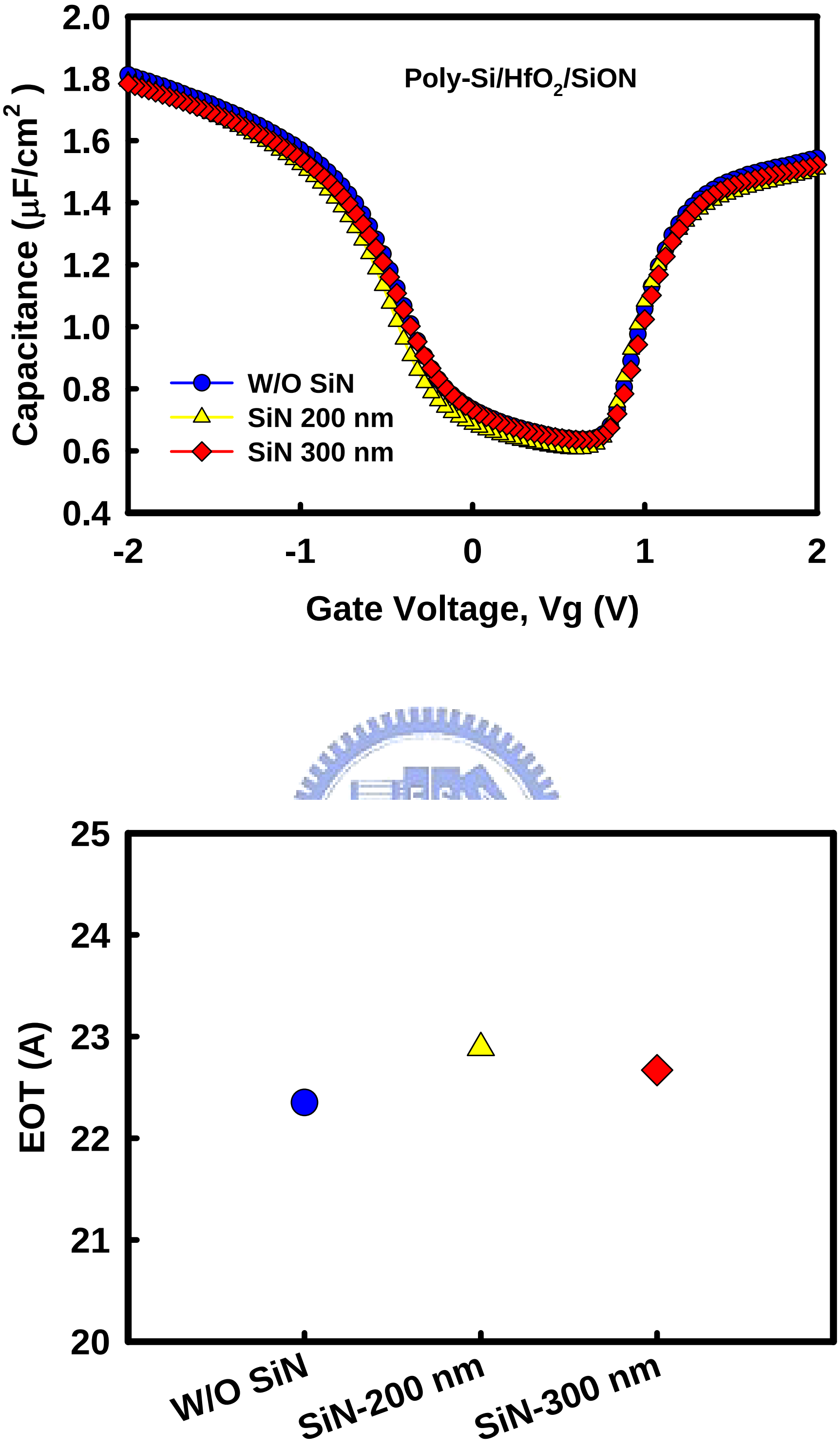


Fig. 2-29 (a) C-V characteristics were identical with various CESLs strain conditions.
(b) Extracted EOT form C-V characteristics were between 2.2~2.4 nm.

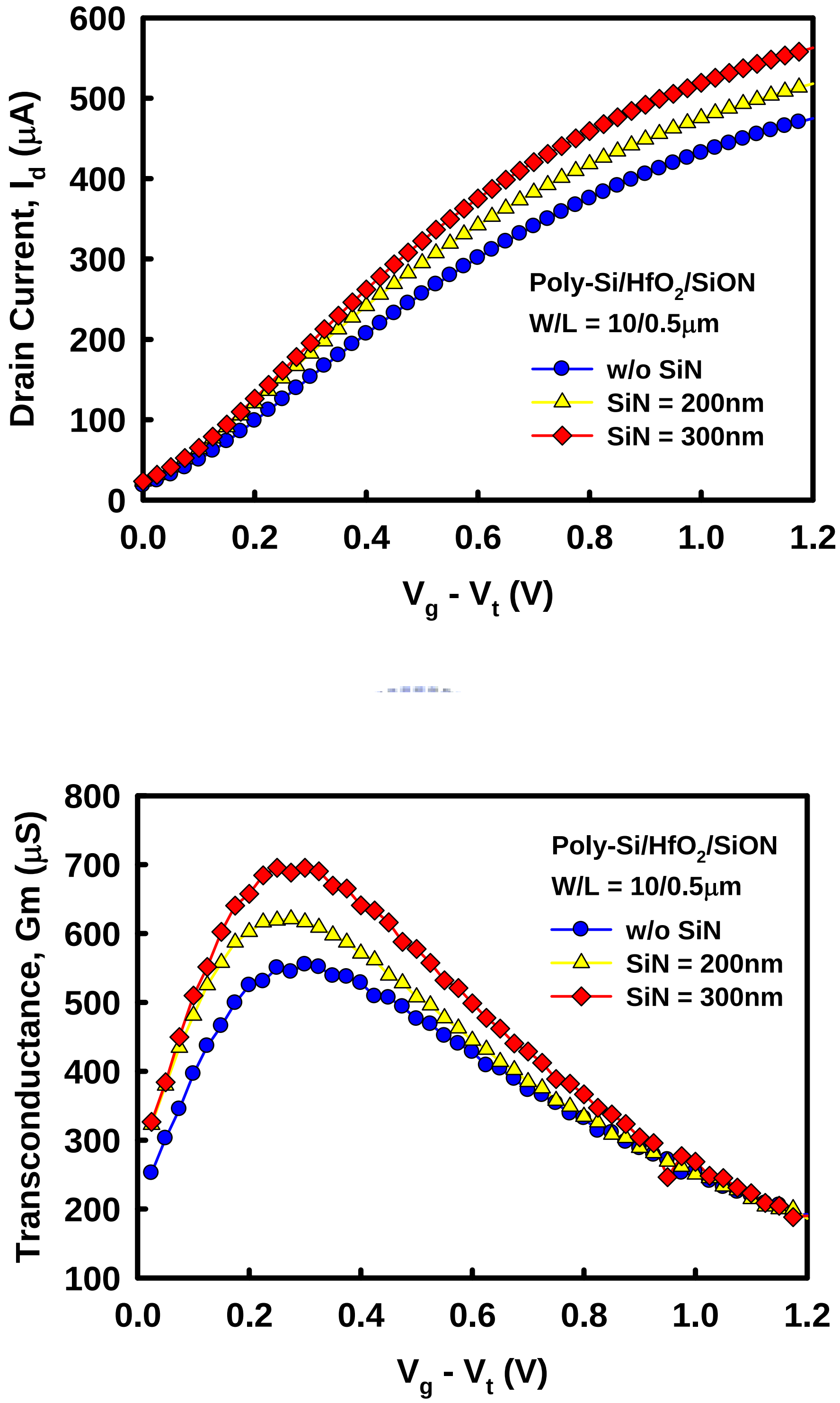


Fig. 2-30 The enhancements of CESLs strain effects exhibited in (a) I_d-V_g characteristics (b) G_m-V_g characteristics.

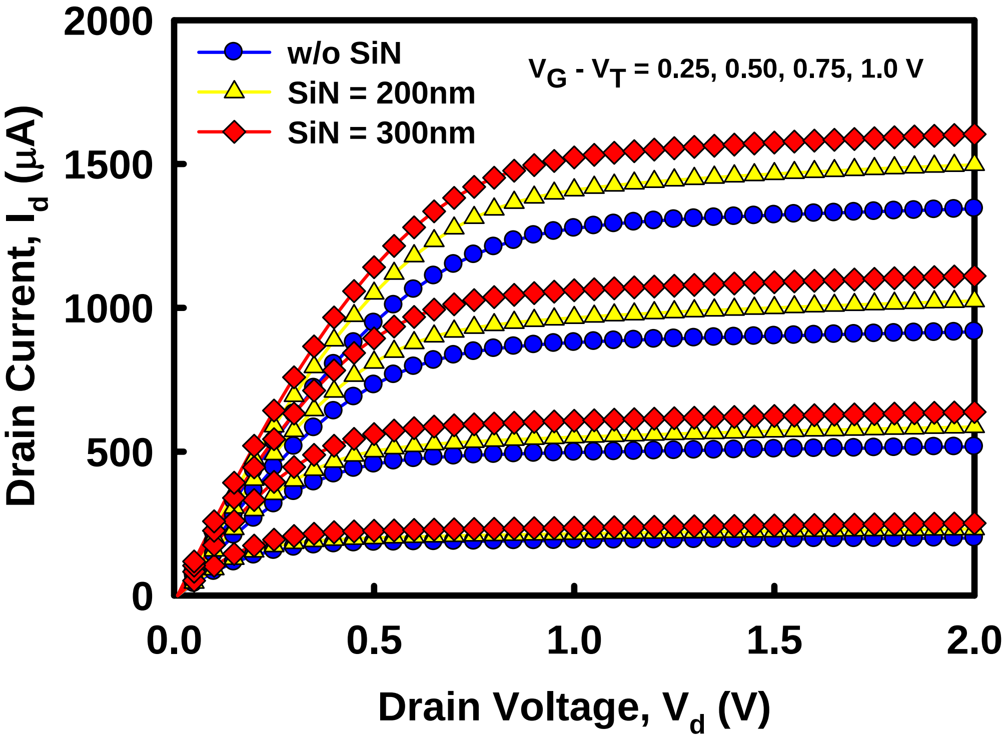


Fig. 2-31 The CESLs strain effect were demonstrated in the enhanced driving current.

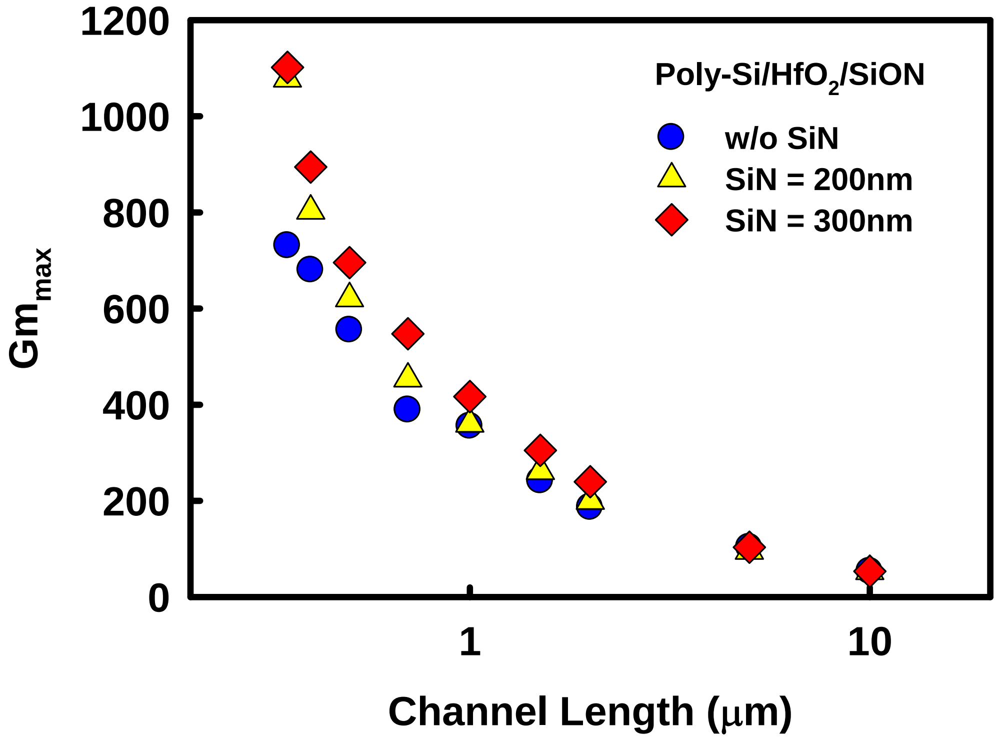


Fig. 2-32 The channel length dependences on $G_{m.MAX}$. The enhancements of strain effect were apparently observed in short channel length.

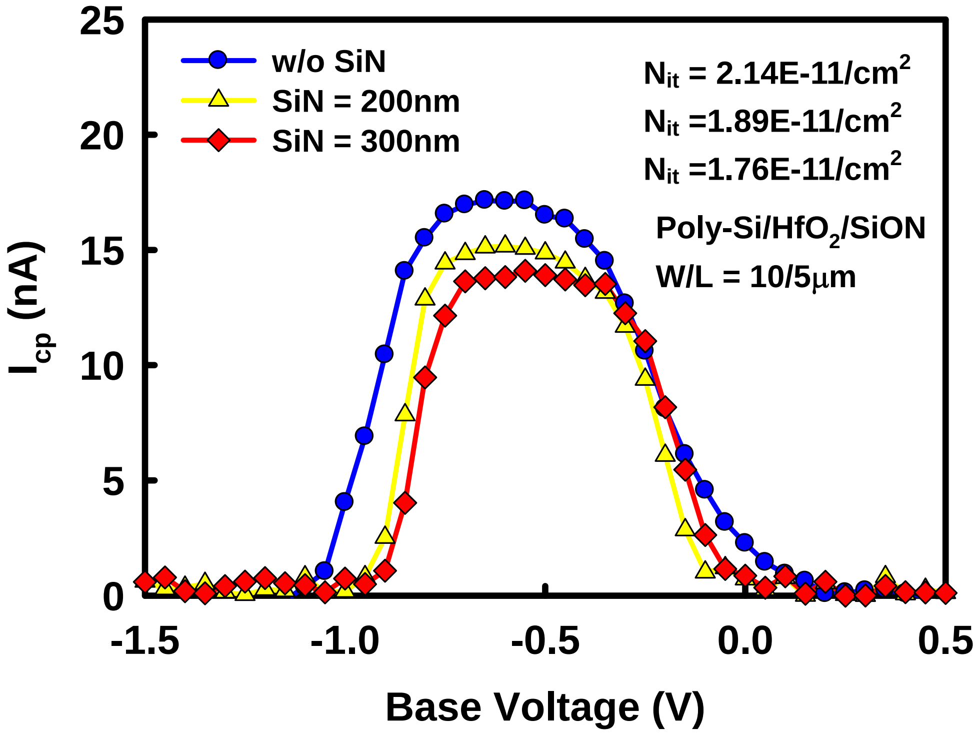


Fig. 2-33 Interface properties at SiON/Si-substrate were investigated through charge pumping method. A reduces of donor-like traps and interface states were found because a hydrogen passivation was conducted during SiN deposition by PECVD.

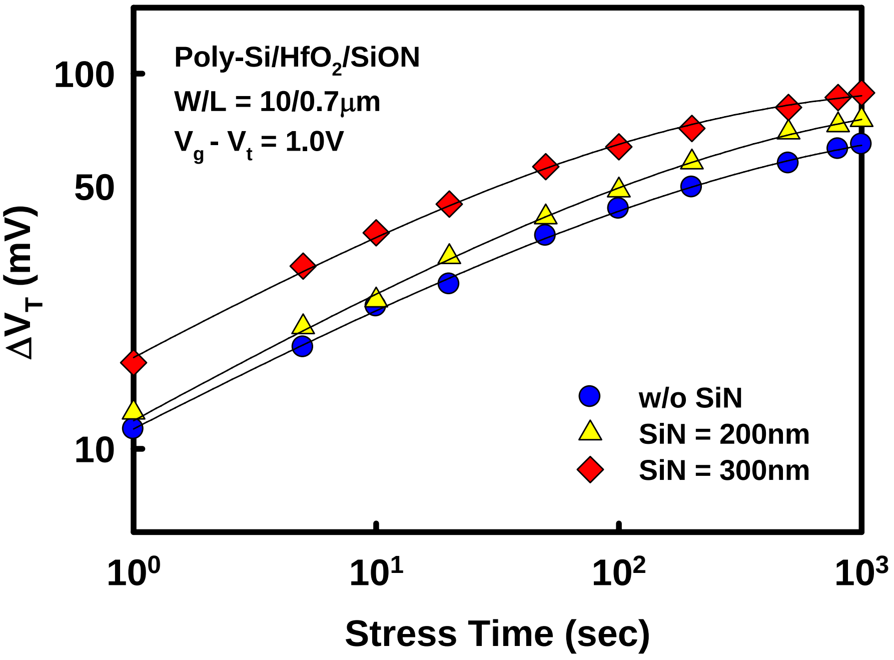


Fig. 2-34 The PBTI degradation was investigated with respect to CESLs strain conditions. The experimental results were fine fitting with charge trapping model [35].

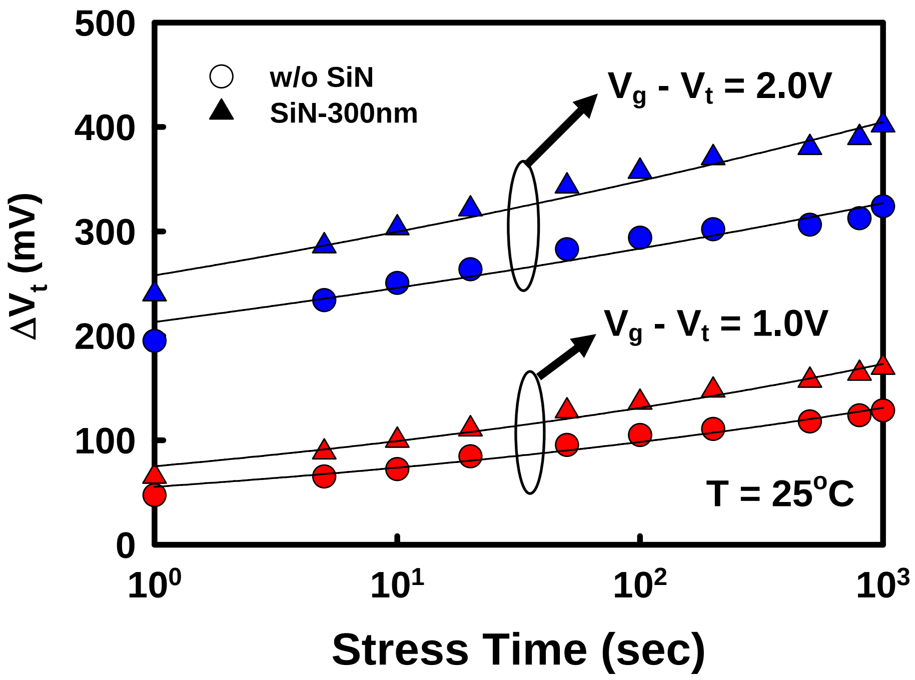


Fig. 2-35 The dependences of stress voltage were also investigated in PBTI degradation.

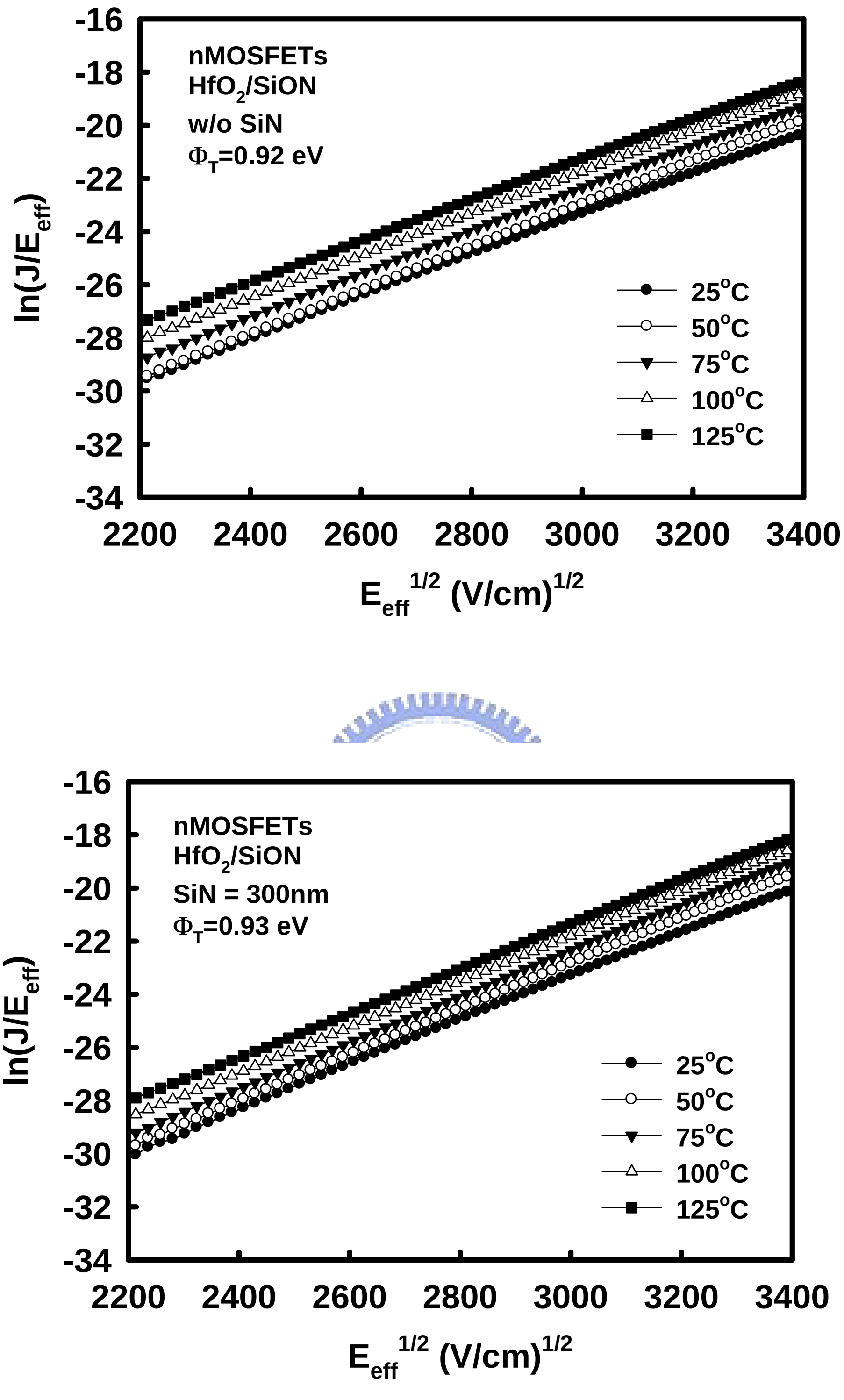


Fig. 2-36 Frenkel-Poole emission fitting was modeled for samples (a) w/o SiN capping. (b) 300nm SiN capping. The trap energy level with respect to conduction band of HfO_2 was extracted as 0.92 eV for w/o SiN capping and 0.93 eV for 300nm SiN capping.

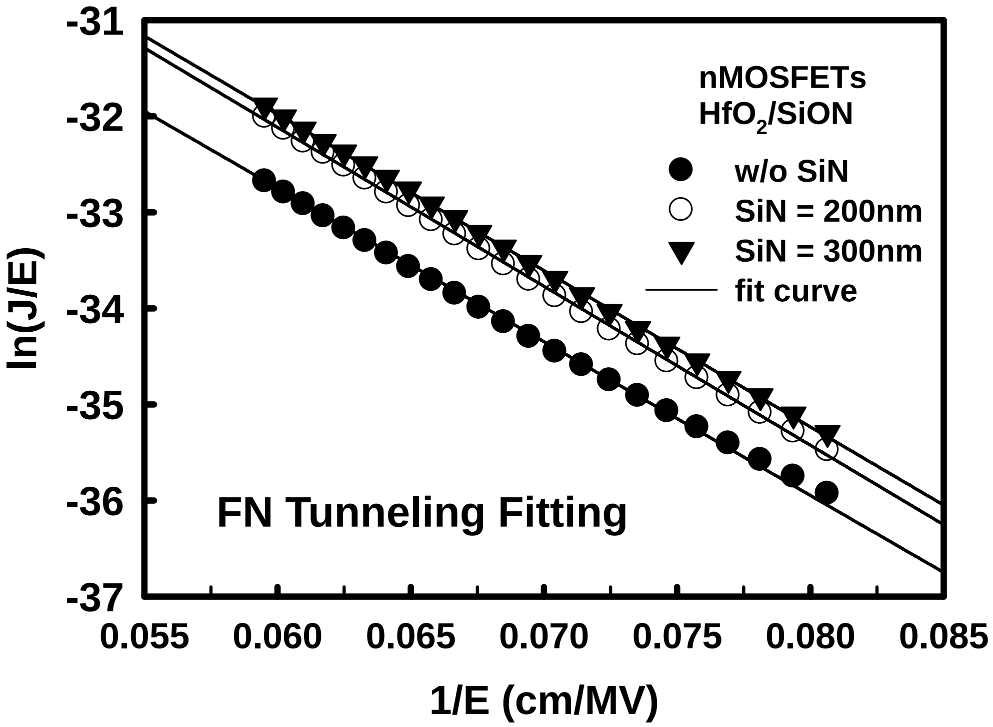


Fig. 2-37 Fowler-Nordheim tunneling fitting was modeled for samples w/o SiN capping and with 300nm SiN capping. The nearly identical slopes of FN-tunneling fitting indicated that CESLs strain effect did not change the trap energy levels and charge trapping behaviors in HfO_2.

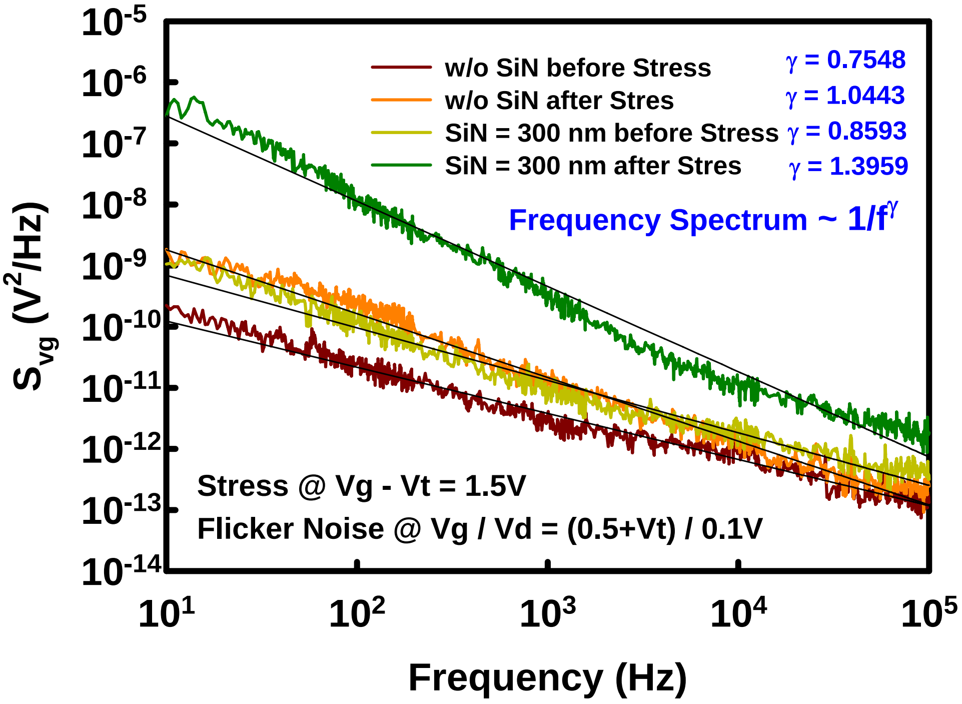


Fig. 2-38 Flicker noise results were investigated in samples w/o SiN and with 300nm SiN. The elevated γ value extracted from flicker noise signal indicated the increase of trap density after PBTI degradation.

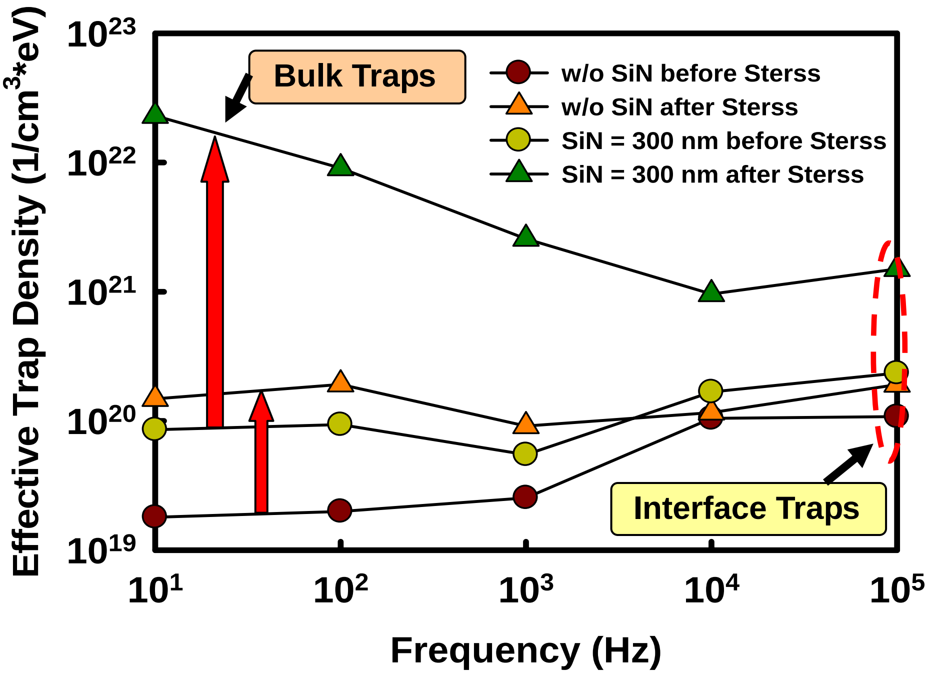


Fig. 2-39 The effective trap density was transformed from flicker noise signal. The experimental results implied that samples with SiN capping had a severe charge trapping in high-κ bulk, and it led to more significant PBTI degradation.

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Chapter 3

Charge Trapping Behavior in High-κ Gate Dielectrics

3.1 Introduction

High-κ gate dielectrics have been extensively investigated on CMOS technology nowadays. Compatible device fabrication process and effective improvements of restraining large direct tunneling gate leakage current through gate dielectrics have been successfully conducted in various Hf-based high-κ gate dielectrics [1-5]. As the result, it is imperative to adopt the high-κ materials as the gate dielectrics in next CMOS generation. In the way of investigations on high-κ gate dielectrics, many critical issues and difficult challenges were surely found during the progress of advanced semiconductor technology. As the most significant concerns of high-κ gate dielectrics, three critical problems have been paid much attention during the developments of the high-κ integration including Fermi-level pinning effect [6-7], channel mobility degradation [8-9], and charge trapping/de-trapping phenomena [10-12]. The Fermi-level pinning effect has been successfully suppressed by introduction of metal gate [13]; the channel carrier mobility has also been enhanced by applications of metal gate and strain technology [13-15]. However, the most specific challenges of charge trapping/de-trapping have been still waited for more effective solutions to improve this troublesome problem. Therefore, the ways of suppressing charge trapping/de-trapping have become the most important concerns for the developments of high-κ integration in CMOS technology.

In order to understand the fundamental of charge trapping/de-trapping behaviors, many key factors such as stress voltage, stress time, and crucial temperature conditions all have been studied to realize the dynamics of charge trapping/de-trapping. In this chapter, we focus on the charge trapping behavior in nMOSFETs with Hf-based high-κ gate dielectrics first of all. Many electrical characteristics were appropriately extracted in the related measurements to effectively analyze the physical mechanism of charge trapping behavior. Finally, we have developed an universal model to well explain charge trapping kinetics and realize its impact on device performance and reliability.

3.2 Experimental Procedures

In this study, nMOSFETs were fabricated on (100) p-type Si wafers. After a standard RCA cleaning with a final HF-dip, a based oxide SiO_2 (0.8 nm and 1.4 nm) was thermally grown to be thin interfacial layer. A 3.2 nm HfO_2 layer was deposited by ALD system, followed a high temperature post deposition annealing (PDA) to optimize the film quality. Finally, a metal gate with workfunction (Φ_B) = 4.2 eV was conducted by PVD technique to perform the gate stack, then the following stand CMOS process were implemented to complete the total device fabrication. The electrical characteristics were investigated through the techniques of keithley Model 4200-SCS semiconductor characterization system and keithley pulse IV measurement.

3.3 Results and Discussions

3.3.1 Modeling of Charge Trapping Behavior

Charge trapping effect is an inevitable trouble for the applications of high-κ gate dielectrics on CMOS technology. Fig. 3-1(a) and Fig. 3-1(b) represented the impacts of charge trapping on the degradation of device performances. We can realize the significant issues accompanied with the application of utilization of high-κ gate dielectrics through the degradations of threshold voltage (V_t) and the transconductance (G_m) during a PBTI stress. According to the plenty of bulk trap density in high-κ gate dielectrics, charge trapping is believed to be the predominant dynamics led the reliability degradation in high-κ gate dielectrics instead of the reaction-diffusion model (R-D model) that fine describes the BTI degradation in SiO_2 [16-18]. In order to verified the influences of charge trapping on high-κ reliability, the charge trapping behavior were carefully analyzed as the following model reported by Sufi Zafar et al. [19]:

$$\frac{dn_T}{dt} = \frac{(N_{tot} - n_T)}{\tau_c} \tag{3.1}$$

$$\Delta V_T = \Delta V_{\max}\left[1 - \exp(-(\frac{t}{\tau_{c0}})^{\gamma})\right] \quad where \quad \Delta V_{\max} = \frac{q \cdot N_{tot} \cdot x_{eff}}{\varepsilon \cdot area} \tag{3.2}$$

$$n_T = N_{tot}\left[1 - \int \frac{\rho(\tau_c)}{N_{tot}} \cdot \exp(-\frac{t}{\tau_c}) \cdot d\tau_c\right] = N_{tot}\left[1 - \exp(-(\frac{t}{\tau_{c0}})^{\gamma})\right] \tag{3.3}$$

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Figure 3-2 showed the modeling of the PBTI degradation under various stress conditions. The fine fitting results strongly demonstrated that the electron trapping mainly dominate the whole PBTI degradation in nMOSFETs with HfO_2/SiON gate stack. The related fitting parameters including: ΔV_{MAX} (maximum of trapping charges in high-κ gate dielectrics), τ_0 (trapping time constant), and γ (related trap distribution) were summarized in Table 3-1, and plotted in Fig. 3-3(a)-(c) to describe the dependence on stress voltage. As we can observe in Fig. 3-3(a) and Fig. 3-3(b), a tendency of Power Law behavior indicated that the ΔV_{MAX} and τ_0 is strong dependent on stress voltage. On the other hand, in Fig. 3-3(c), the γ parameter exhibited a linear decrease with elevated stress voltage to imply an extensive trap distribution in the regime of high stress voltage (small γ, wide trap distribution) that was consistent with the charge trapping behaviors of larger ΔV_{MAX} and smaller τ_0 value at high stress voltage. In Sufi Zafar's works, the quantity of high-κ bulk traps is considered to be a conserved value and the charge trapping is just filling these pre-existing traps without additional trap generation [20]. A concept related to the conversation of pre-existing traps under various stress conditions in high-κ gate dielectrics was shown in Fig. 3-4 [21]. However, in our experimental data, the distinct results were discovered to imply that new trap generation occurred at high stress voltage during PBTI degradation in Fig. 3-5. Therefore, the charge trapping model is modified as below:

$$\Delta V_T = \Delta V_{\max}\left[1 - \exp(-(\frac{t}{\tau_{c0}})^{\gamma})\right]$$

$$where \ \ \Delta V_{\max} = \frac{q \cdot N_{tot} \cdot x_{eff}}{\varepsilon \cdot area}, N_{tot} = N_{tot}(V_{g,stress}) \qquad (3.4)$$

A dependence of stress voltage on total charging traps in the bulk of high-κ gate dielectrics is claimed in our studies to appropriately describe the charge trapping behavior, especially at extremely large stress voltage.

3.3.2 Two-Stage Charge Trapping Behaviors under Positive Bias Stress in High-κ Gate Dielectrics

The charge trapping in high-κ gate dielectrics under an electrical stress process usually reveals the distinct behaviors on two stages of time demarcation that trapping with fast and slow responses on the first and second stages, respectively. In general, these two types of charge trapping are qualitative and quantitative difference during a BTI degradation. Especially, the charge trapping on the first stage usually brings a large number of trapping density instantly and greatly changes the threshold voltage which is clearly observed in Fig. 3-1(a). In order to realize the origins and the impacts of these distinct charge trapping phenomena in earlier and later time demarcations, the PBTI degradation was conducted in the nMOSFETs with HfO_2/SiO_2 gate stack. In Fig. 3-6, a definition of fast trapping (t = 0 ~ 1.78 sec) and slow trapping (t = 1.78 ~ 100 sec) was established in our studies for the PBTI measurements with the conventional DC method. For the experimental data, the fast trapping, slow trapping, total trapping are extracted form the V_t shift in the stress time of t = 0 ~ 1.78 sec, t = 1.78 ~ 100 sec, t = 0 ~ 100 sec, respectively. Fig. 3-7(a) showed analysis of fast trapping, slow trapping, and total trapping in the nMOSFETs with HfO_2 (3.2 nm)/SiO_2 (0.8 nm) gate stack under various stress voltages. The quite different behaviors are apparently observed that the fast trapping is obvious to dominate the whole PBTI degradation in the entire regime of stress voltage while the slow trapping seems to reach a saturation level when stress voltage is beyond a critical voltage as V_g = 1.6 V. In Fig. 3-7(b), the same phenomenon is also found in the devices with a based SiO_2 = 1.4 nm which the critical voltage is as V_g = 2.0 V. In Fig. 3-8(a), the charging behavior of fast trapping was investigated in the comparison with the total trapping. [A fast/total trapping ratio is defined as (fast trapping)/(total trapping) × 100% in our studies]. The experimental results exhibited the comparison of fast/total trapping close to an invariant ration of 60% before the critical voltage, V_g = 1.6 V. However, the fast/total trapping ratio presented a totally different behavior with a linear increase when the stress voltage was over the V_g = 1.6 V. For based SiO_2 = 1.4 nm, the fast/total trapping ratio also revealed the identical value of 60% as the same as based SiO_2 = 0.8 nm before its critical voltage as V_g = 2.0 V. Moreover, the same tendency after critical V_g = 2.0 V was observed, too. For further detailed understanding, the comparisons of both based SiO_2 = 0.8 nm and 1.4 nm were illustrated in Fig. 3-9(a) and Fig. 3-9(b). It is considered that the difference of fast trapping is according to the distinct charge tunneling ability with respect to different interfacial layer (IL) thickness. Besides, the same saturation levels of slow trapping are believed to be associated with the intrinsic properties of high-κ materials themselves.

From the aspect of fast/total trapping ratio, an identical ratio of 60% observed before the critical voltage for both IL = 0.8 nm and 1.4 nm is believed to be related to those shallow traps in HfO_2 that are responsible for the fast trapping behavior. Therefore, this phenomenon is considered to be related to some factors, such as material phase (ex: amorphous, crystal), types of high-κ materials (ex: HfO_2, ZrO_2, silicate, other element-incorporation), and deposition technologies (ex: ALD, MOCVD), which would affect the intrinsic properties of those traps in high-κ gate dielectrics.

In order to further realize the carrier transport in the regime of stress voltage, the predominant conduction mechanisms were carefully investigated in a wide region of gate voltage in Fig. 3-10. In the regimes of middle gate voltage ($0.6 \text{ V} < V_g < 1.6 \text{ V}$) and high gate voltage ($V_g > 2.0 \text{ V}$), the conduction mechanisms are dominated by Frenkel-Poole emission (F-P) and Fowler Nordheim tunneling (FN-tunneling), respectively. When gate voltage is in between $1.6 \text{ V} < V_g < 2.0 \text{ V}$, these two main conduction mechanisms complete with each other in this regime. Furthermore, the trap barrier height (Φ_B) was extracted from the Frenkel-Poole emission fitting under various gate voltages. The extracted Φ_B is 0.36 ~ 0.85 eV which is consistent with the energy levels of oxygen vacancies (Vo^{2+}, Vo^{-}, Vo^{2-}) and grain boundary defects (g.b defects) , those roles of “shallow traps” which are responsible for the “fast trapping” behaviors [22-25]. The related fitting results of Frenkel-Poole emission and Fowler Nordheim tunneling were illustrated in Fig. 3-11(a)-(c) and Fig. 3-12(a)-(b), respectively. The charge trapping was also described through the band diagrams under various stress V_g conditions in Fig. 3-13. When stress $V_g = 1.2$ V (low stress V_g condition), the electrons are captured form a behavior of direct tunneling into the “shallow traps” near the conduction band of HfO_2, and then electrons have large probability to drop into deeper energy levels as the “deep traps” after longer stress time. When stress $V_g = 1.5$ V (close to critical voltage condition), a band bending leads the carrier transport be much close to the FN-tunneling. When stress $V_g = 1.8$ V (high stress V_g condition), the predominant transport turns into the FN-tunneling. The electrons will tunnel through the based SiO_2 and the triangle barrier height of HfO_2 first, and then they will be captured from the conduction band of HfO_2 by those high-κ bulk traps (shallow traps). It is believed that the difference of capturing injected electrons in high-κ gate dielectrics would be the main reasons for the distinct trapping behaviors over the critical voltage. As the result, once the FN-tunneling occurs beyond the critical voltage, this type of capturing injected electrons would result in an significantly elevated quantity of fast trapping without any extra contribution of slow trapping. That also explains that the ratio of fast/total trapping turns form an invariant value of 60% into a linear increase when applied voltage is over the critical voltage. Fig. 3-14(a) and Fig. 3-14(a) showed the modeling of charge trapping before and after FN-tunneling, respectively. The distinct fitting results of the Power Law behavior and the linear behavior further demonstrate the difference of charge trapping mechanisms before and after the occurrence of FN-tunneling. The related fitting results are exhibited in Table 3-2.

In Fig. 3-15(a), the concept of "deep traps" was understood through the time dependence of charge trapping behavior with a short-time stress condition (0 ~ 2 ms). A "step from" of charge trapping phenomena revealed the distinct trapping mechanisms in various time demarcations. A charging saturation is considered to imply the respondences of longer trapping time constant which charges transit to those deeper energy levels associated with a similar concept of "U-traps" model [26]. In Fig. 3-15(b), the same phenomena with identical time constants (7e-4, 1.2e-3, 1.8e-3 sec) were observed at greater stress voltage ($V_g = 1.6$V) to strongly demonstrate those are the intrinsic properties of charge trapping behavior in high-κ gate dielectric despite stress conditions (*). In additional, a time dependence on the variation of charge trapping behaviors was also investigated through long-time stress condition (0 ~ 1×10^4 sec) in Fig. 3-16(a). The diverse logarithmic fitting results in each decade revealed the change of charge trapping behaviors during the stress progress which was consistent with the results in the pulse measurement in Fig. 3-15(a). Furthermore, in Fig. 3-16(b), a tendency of the charge trapping behaviors exhibited the predominant trapping mechanism changed form fast trapping to slow trapping. It showed the importance of slow trapping during a longer time stress and firmly demonstrated the impacts of deeper traps with respect to the concept of U-traps model.

(*) Another assumption of charge recombination in high-κ bulk was also in our considerations to explain the time dependence of charge trapping effect. We thought that the holes may inject from the gate electrodes to recombine the trapped electrons at those bulk trap centers and lead to the saturation phenomena we observed.

3.4 Summary

In our studies, we have systematically investigated the charge trapping behaviors in nMOSFETs with HfO_2/SiO_2 gate stack. The fine modeling fitting demonstrated that the charge trapping in high-κ gate dielectrics is the major of leading the PBTI degradation. The total trapping density in high-κ gate dielectrics is demonstrated as a function of stress voltage rather than a conserved quantity of charge filling in the pre-existing high-κ bulk traps. Furthermore, the charge trapping in high-κ gate dielectrics are also carefully investigated through the analysis of fast trapping and slow trapping. An identical value (60%) and a linear increase of fast/total trapping ratio are discovered before and after the critical voltage, respectively. This phenomenon is observed in both based SiO_2 = 0.8 nm and 1.4 nm that indicates the universal charge trapping behavior in HfO_2. The identical value of 60% is considered to be responsible for those shallow traps (oxygen vacancies, Vo^{2+}, Vo^{-}, Vo^{2-} and grain boundary defects) in HfO_2 which are consistent with the related trapping energy levels. Besides, once the FN-tunneling occurs over the critical voltage, the capture of injected electrons from conduction band of HfO_2 would bring on an significantly elevated quantity of fast trapping without any extra contribution of slow trapping. Finally, the concept of deep traps in high-κ gate dielectrics is investigated on the aspect of energy levels. A time dependence of charge trapping behaviors apparently reveals the charge transition into deeper energy levels with respect to the distinct respondence of time constant. The experimental results complete the charge trapping behaviors over several decades (10^{-4} sec $< t < 10^{4}$ sec) and the trap distribution in high-κ gate dielectrics associated with the aspect of energy levels.

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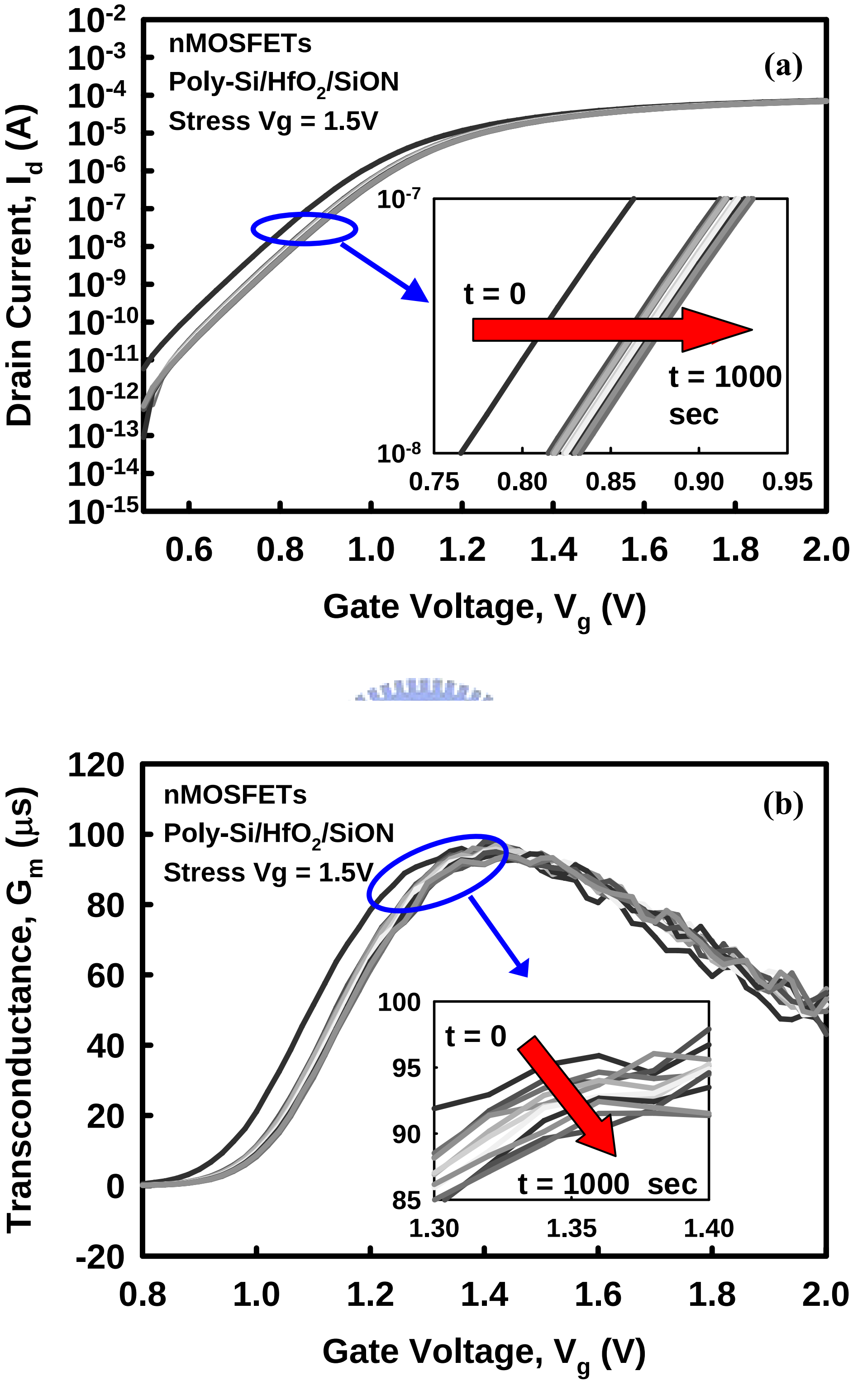

Fig. 3-1 Impacts of charge trapping on (a) Threshold voltage instability and (b) Transconductance, G_m .

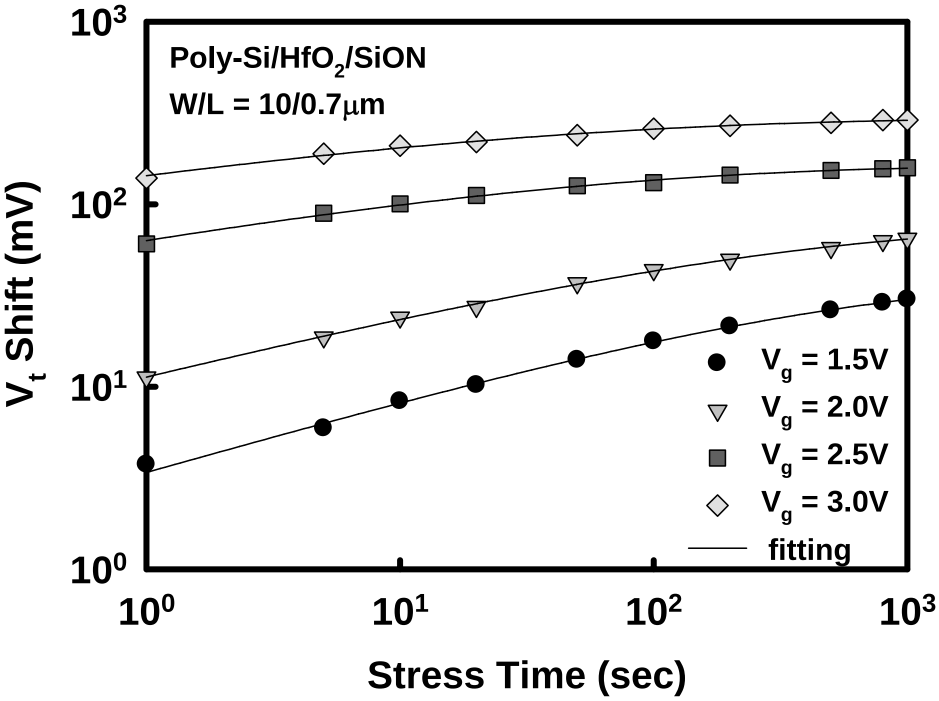

Fig. 3-2 The PBTI degradation under various stress voltages as a function of stress time.

stress Vg parameters	V_g = 1.5V	V_g = 2.0V	V_g = 2.5V	V_g = 3.0V
ΔV_{max} (mV)	37	75	163	296
τ_{c0} (sec)	297.50	159.93	12.81	5.49
γ	0.41	0.36	0.28	0.24

Table 3-1 Fitting parameters in modeling of charge trapping in nMOSFETs with Poly-Si/HfO_2/SiON gate.

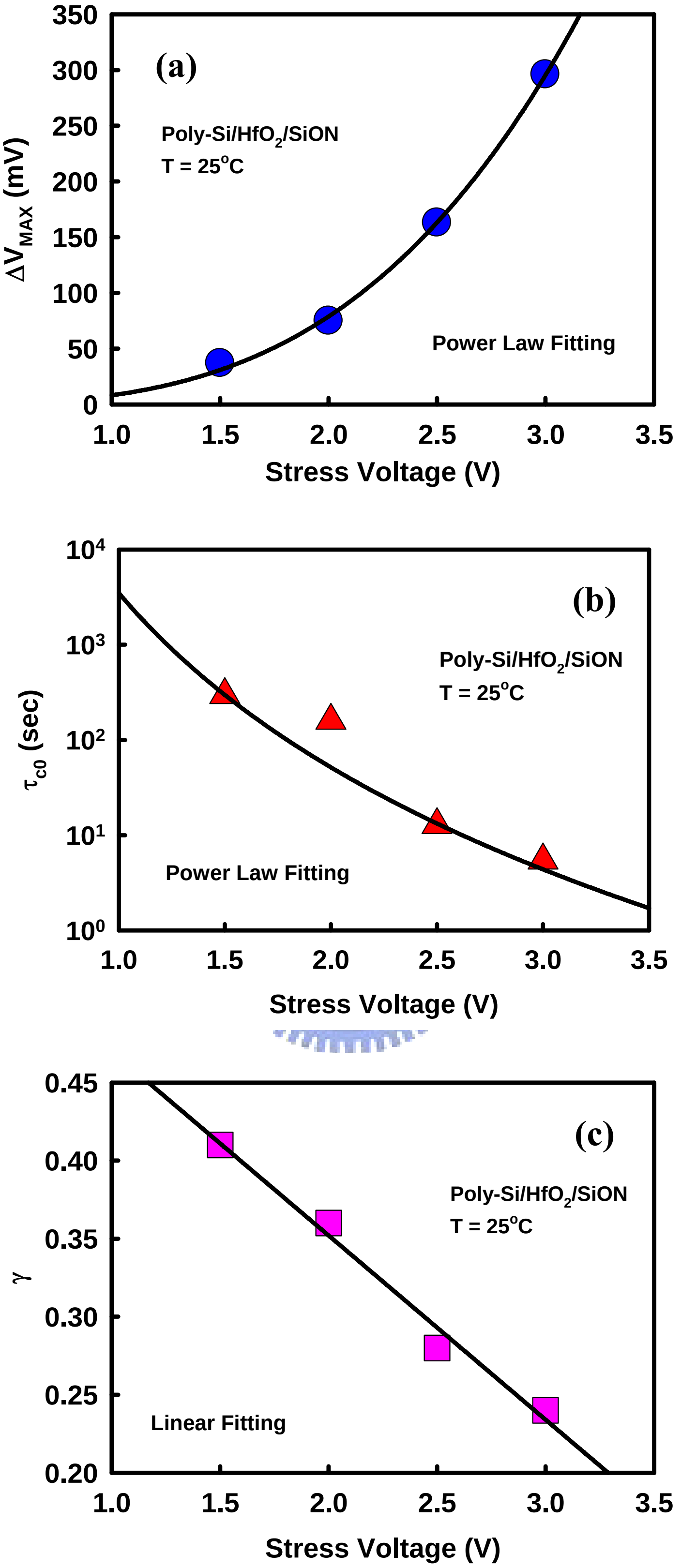

Fig. 3-3 Modeling of charge trapping in nMOSFETs with Poly-Si/HfO_2/SiON gate stack. (a) Maximum of trapping charges, ΔV_{MAX} (b) Trapping time constant, τ_0 (c) Related trap distribution, γ.

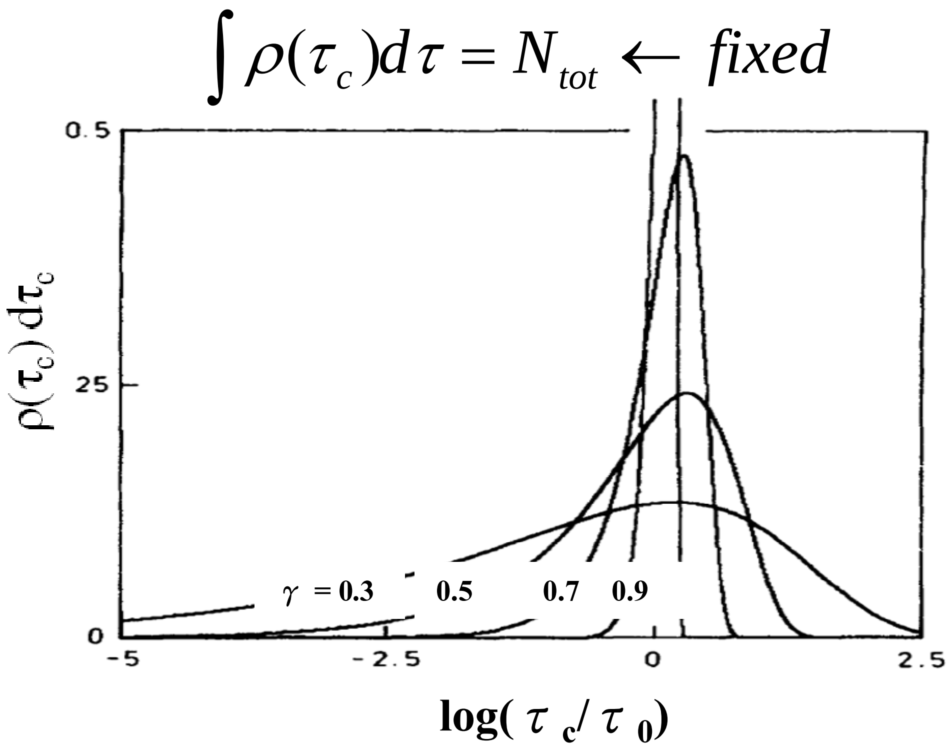

Fig. 3-4 A concept related to the conversation of pre-existing traps under various stress conditions (with respect to each γ.value) in high-κ gate dielectrics. The associated trap distribution is revealed by fitting parameter, γ.

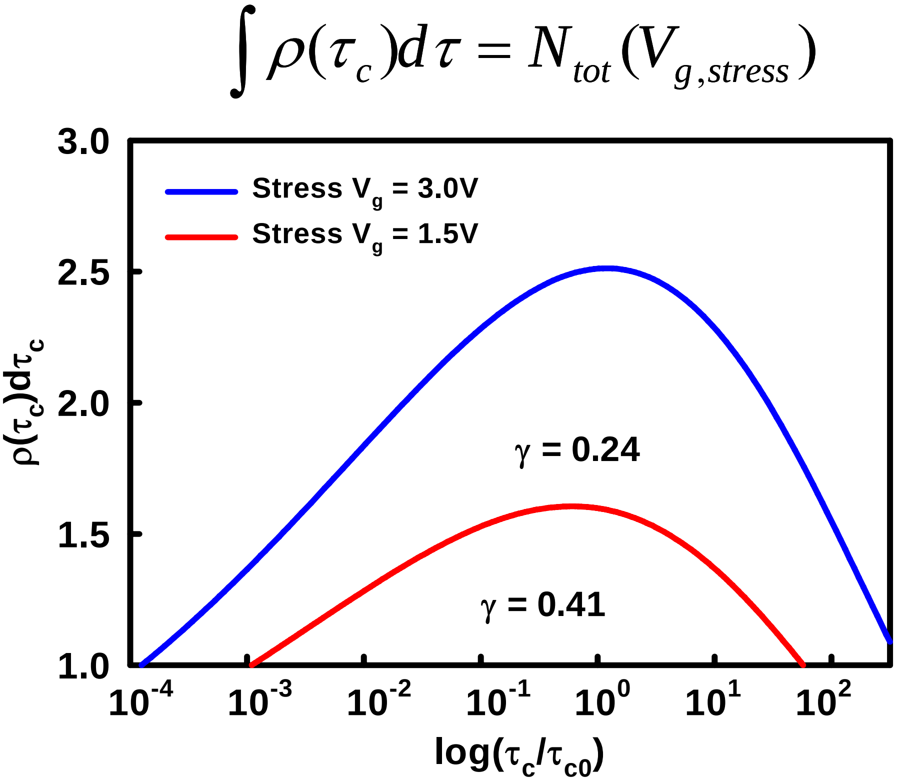

Fig. 3-5 A newly experimental results related to the traps generation under various stress voltages in high-κ gate dielectrics. The associated trap distribution is revealed by fitting parameter, γ.

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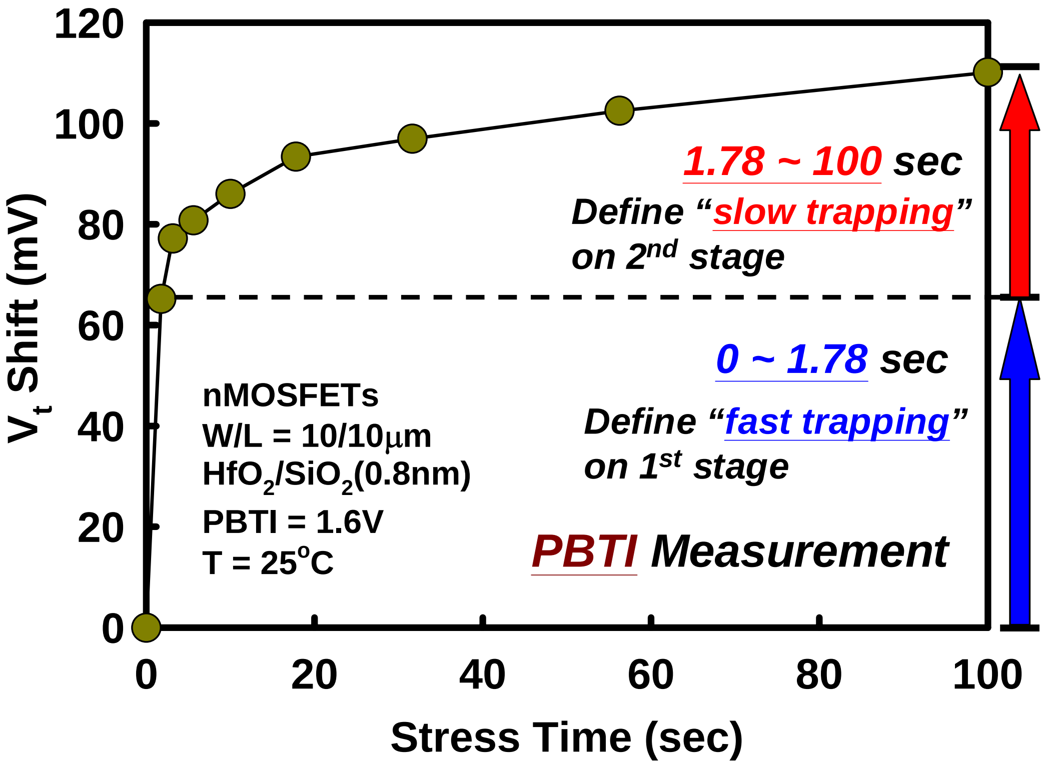
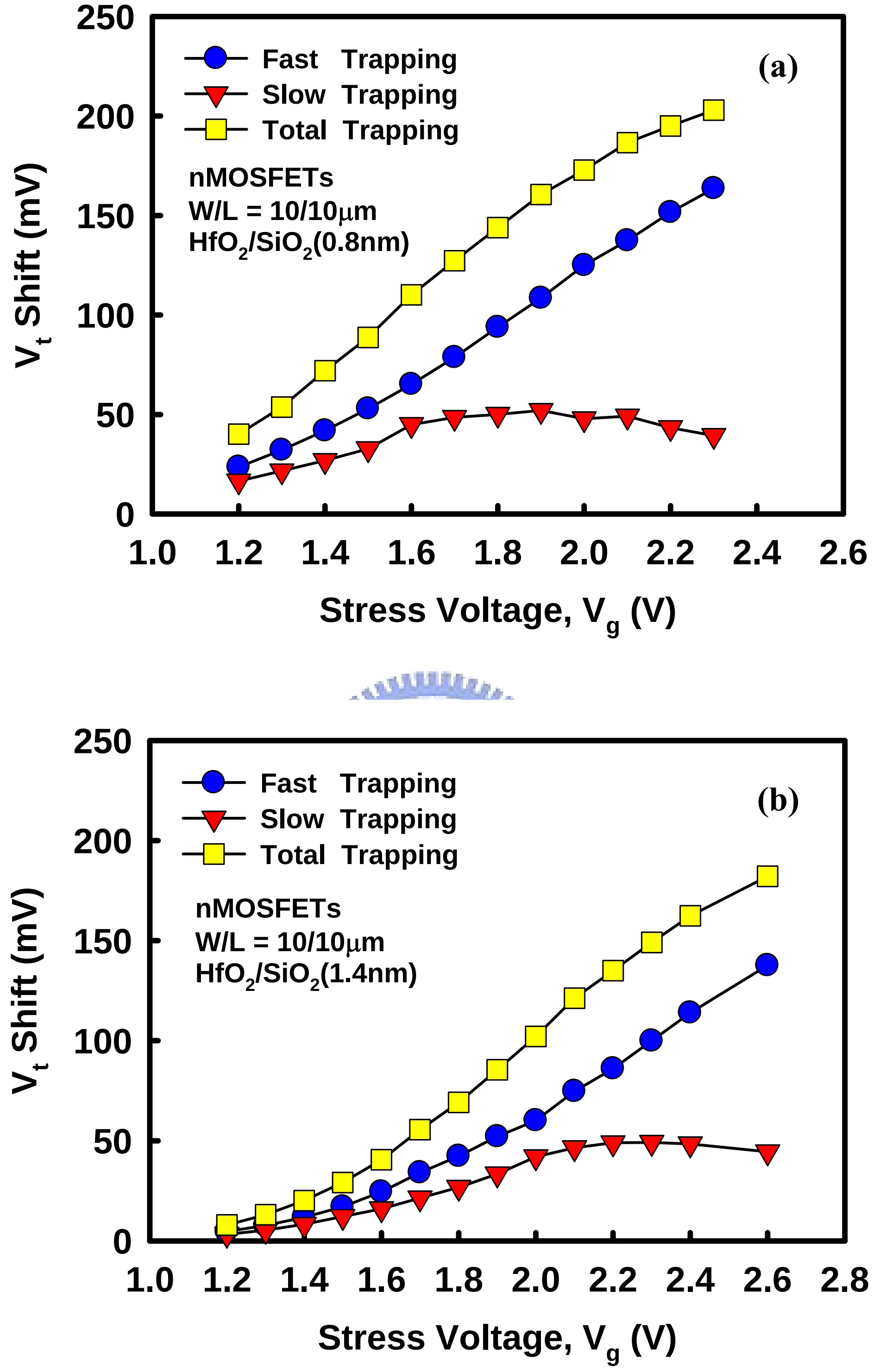


Fig. 3-6 A definition of fast trapping (t = 0 ~ 1.78 sec) and slow trapping (t = 1.78 ~ 100 sec) in our studies for the PBTI measurement with the conventional DC method.



v

Fig. 3-7 Analysis of fast trapping, slow trapping, and total trapping under various stress voltages (a) Based SiO_2 = 0.8 nm (b) Based SiO_2 = 1.4 nm.

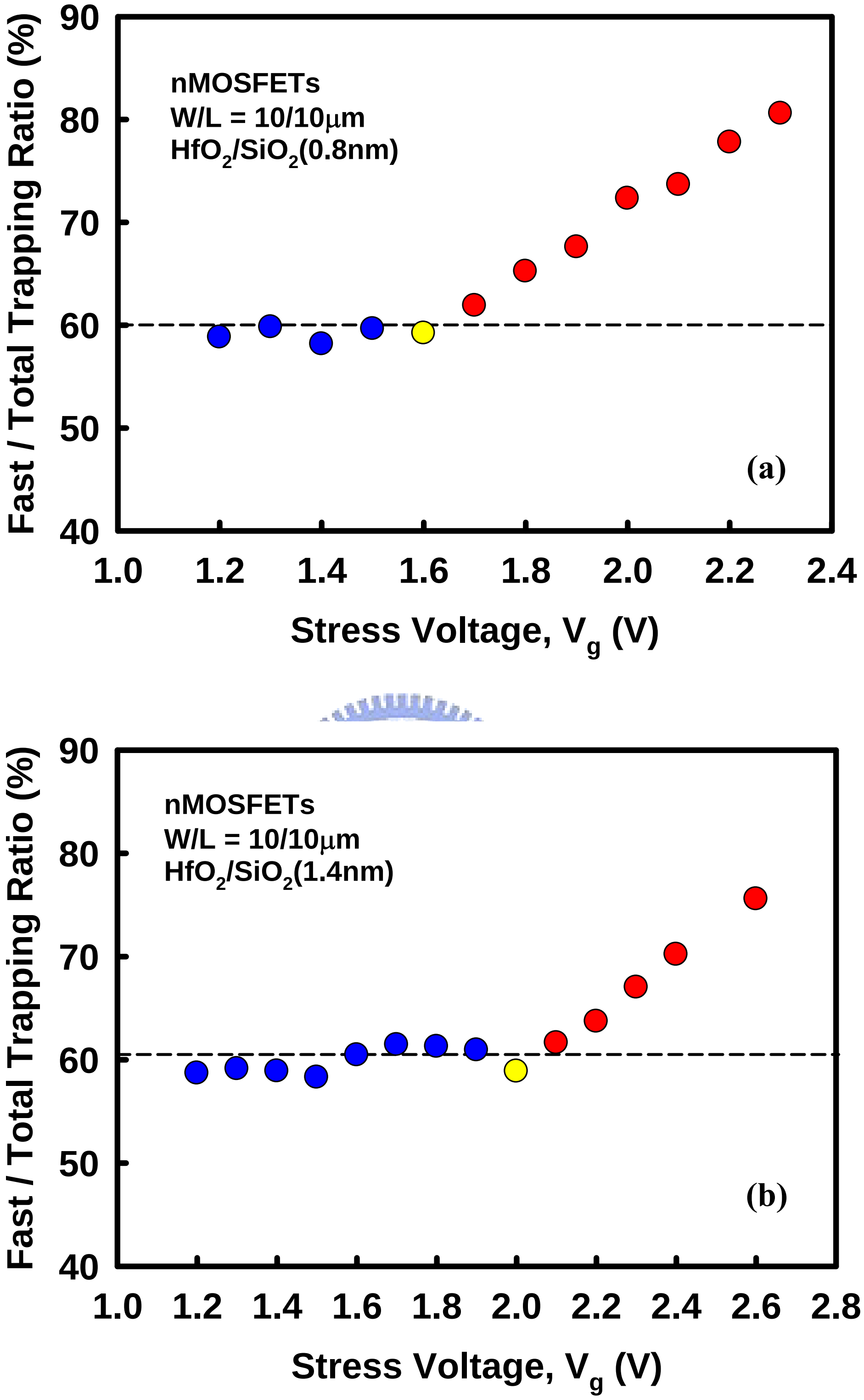


Fig. 3-8 Fast/total trapping ratio during whole PBTI degradation under various stress voltages (a) Based SiO_2 = 0.8 nm (b) Based SiO_2 = 1.4 nm. [A fast/total trapping ratio is defined as (fast trapping)/(total trapping) × 100% in our studies]

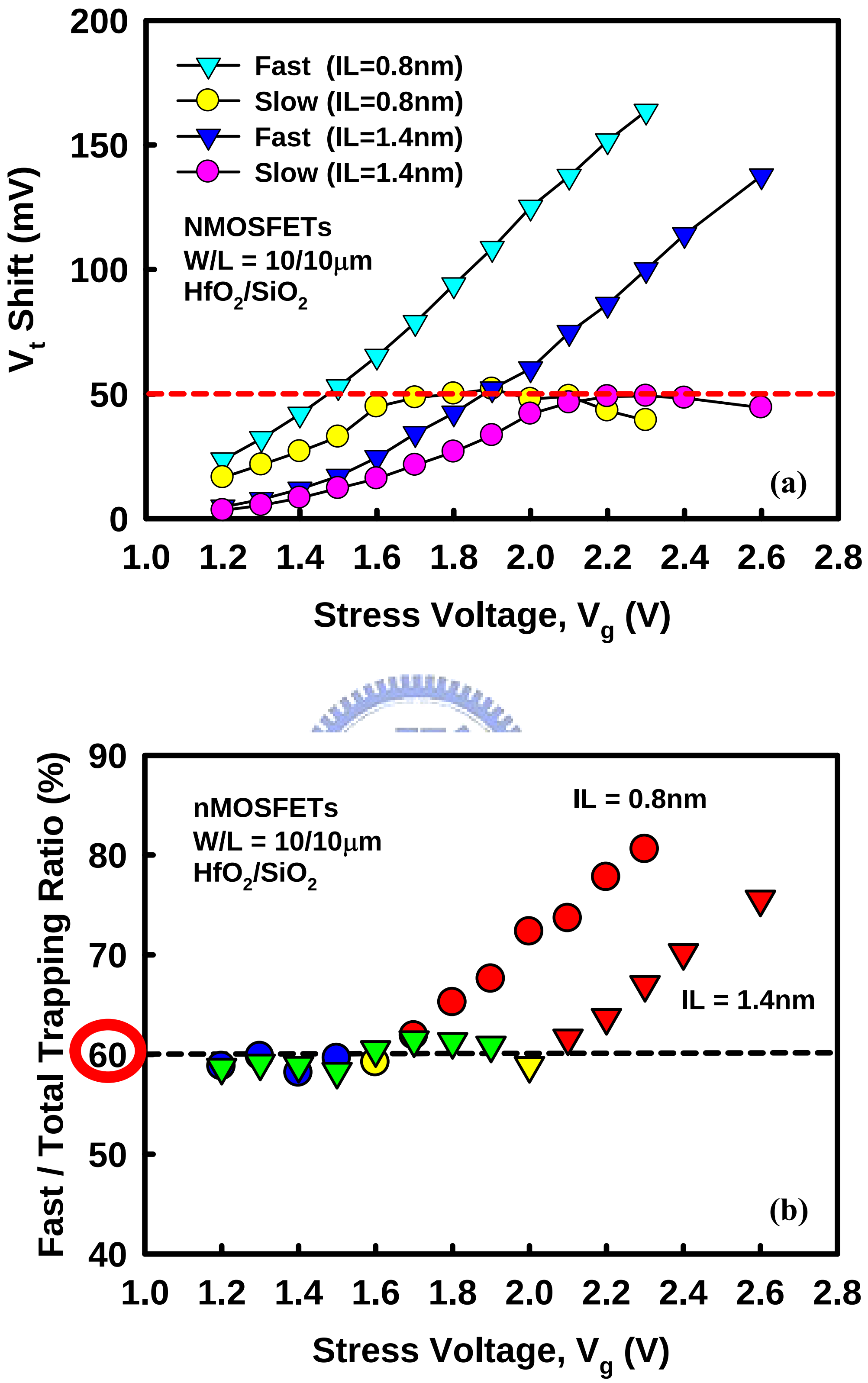


Fig. 3-9 Comparisons of all charge trapping behaviors. (a) Fast trapping and slow trapping (b) Fast/total trapping ratio.

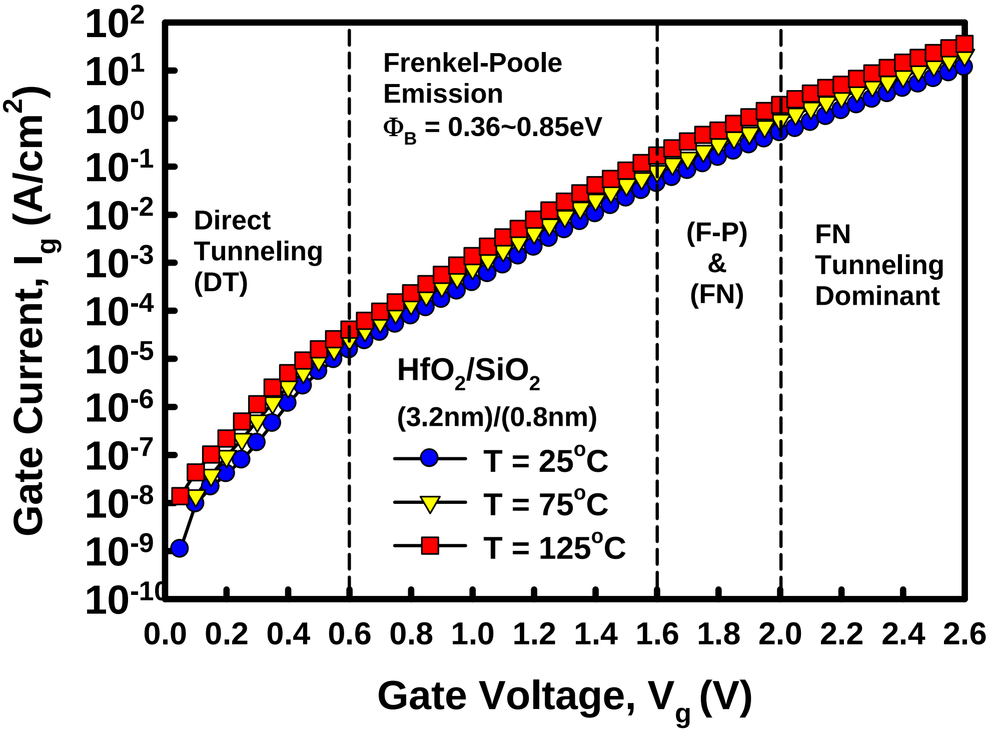


Fig. 3-10 The predominant conduction mechanisms in the gate voltage regime.

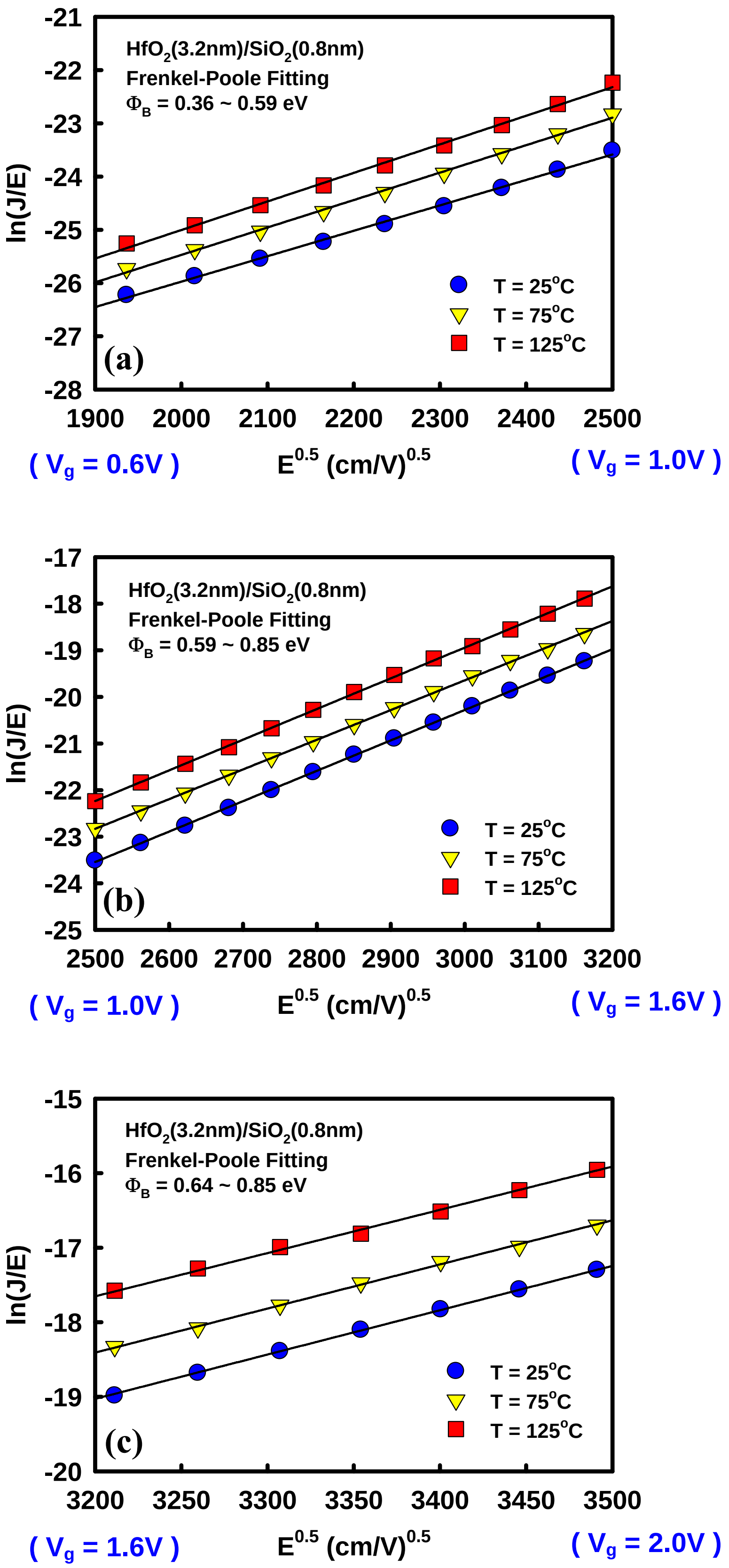


Fig. 3-11 Frenkel-Poole emission (F-P) Fitting in the regime of stress voltage (a) Stress $V_g = 0.6 \sim 1.0V$ (b) Stress $V_g = 1.0 \sim 1.6V$ (c) Stress $V_g = 1.6 \sim 2.0V$.

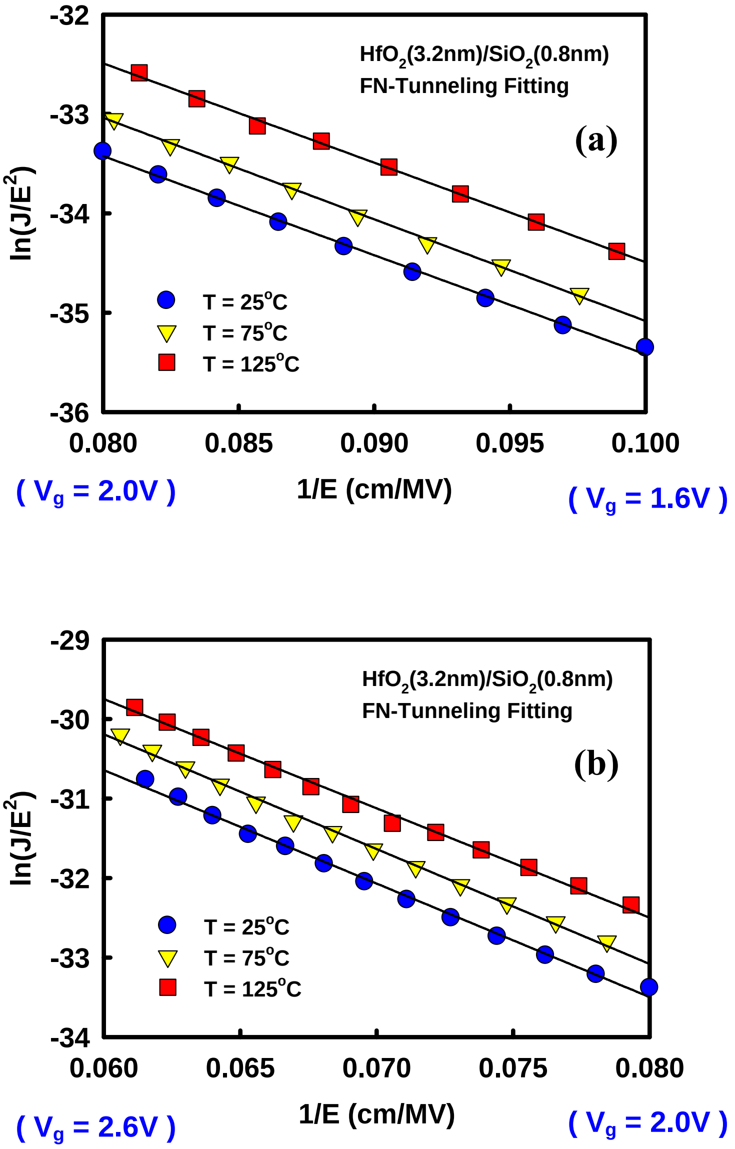


Fig. 3-12 Fowler Nordheim tunneling (FN) Fitting in the regime of stress voltage (a) Stress $V_g = 1.6 \sim 2.0V$ (b) Stress $V_g = 2.0 \sim 2.6V$.

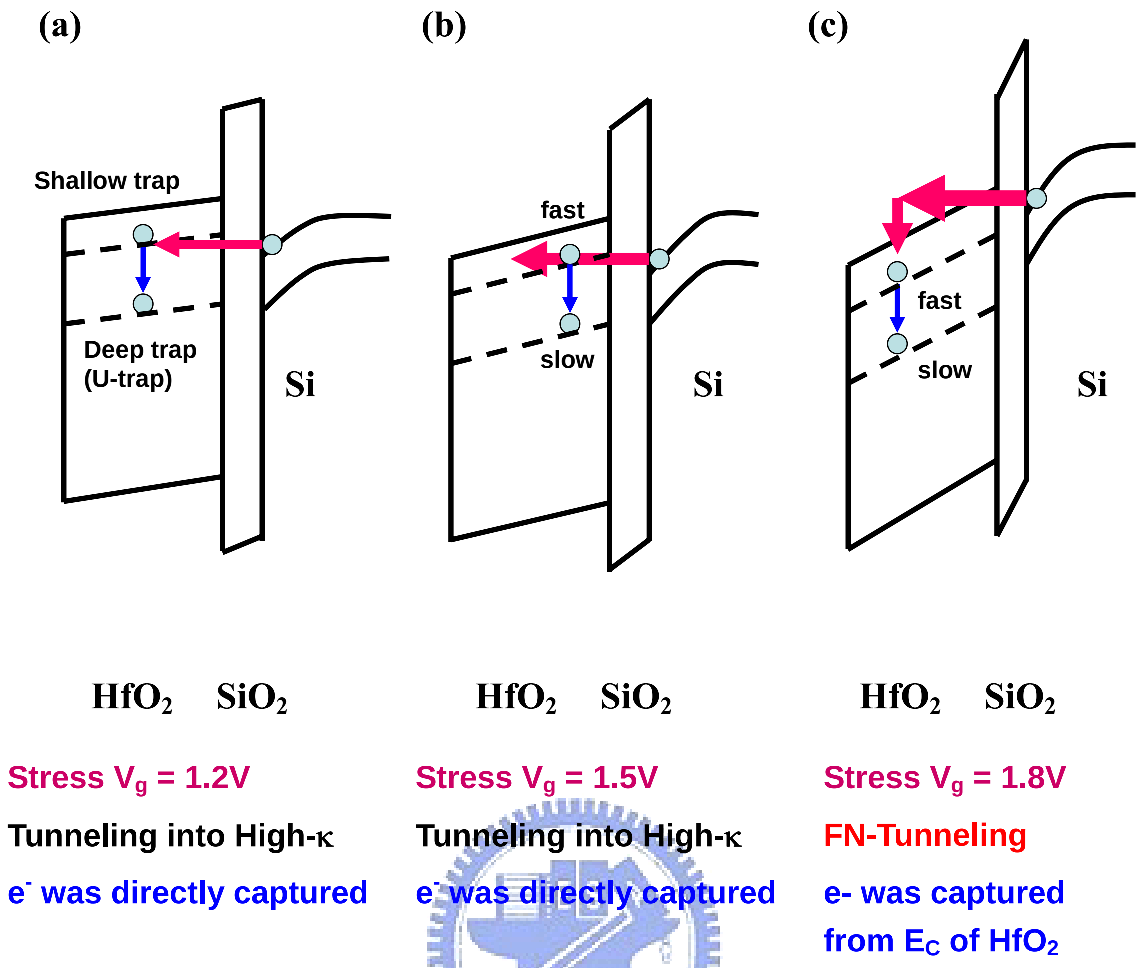

(a)
Shallow trap
Deep trap (U-trap)
Si
HfO₂
SiO₂
Stress Vg = 1.2V
Tunneling into High-κ
e⁻ was directly captured
(b)
fast
slow
Si
HfO₂
SiO₂
Stress Vg = 1.5V
Tunneling into High-κ
e⁻ was directly captured
(c)
fast
slow
Si
HfO₂
SiO₂
Stress Vg = 1.8V
FN-Tunneling
e- was captured from EC of HfO₂

Fig. 3-13 Band diagram of charge trapping under various stress V_g conditions. (a) Stress $V_g = 1.2V$ (b) Stress $V_g = 1.5V$ (c) Stress $V_g = 1.8V$.

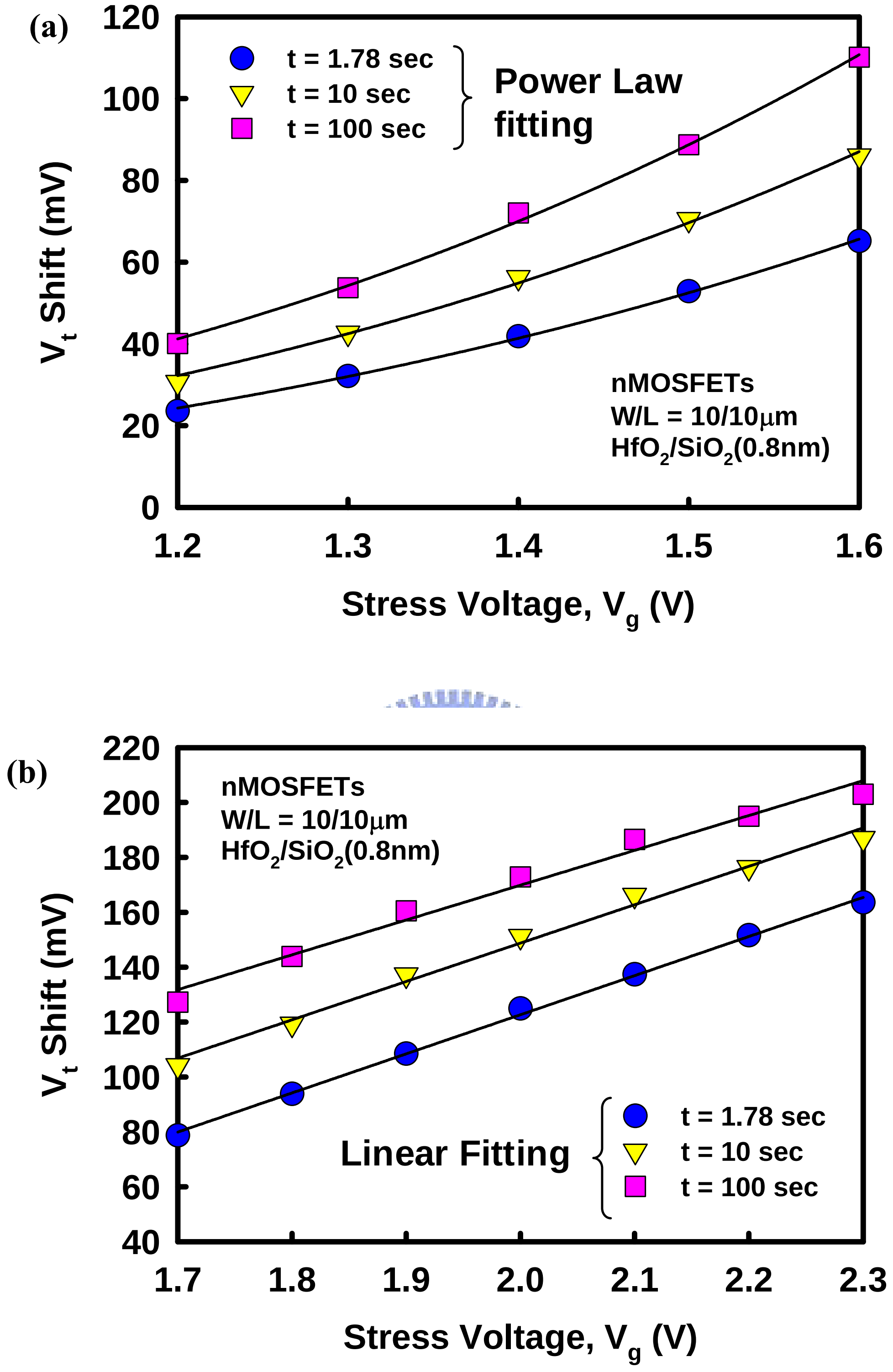


Fig. 3-14 Modeling of charge trapping at various stress time as a function of stress voltage. (a) Before FN-tunneling, stress V_g = 1.2 ~ 1.6V (b) After FN-tunneling, stress V_g = 1.6 ~ 2.0V.

Stress V_g / Time	V_g < 1.6V	V_g > 1.6V
Fast t < 1.78 sec	Trapping (before FN) Power Law	Trapping (after FN) Linear
Slow t > 1.78 sec	Trapping (before FN) Power Law	Trapping (after FN) Linear

Table 3-2 Modeling fitting of charge trapping before and after FN-tunneling.

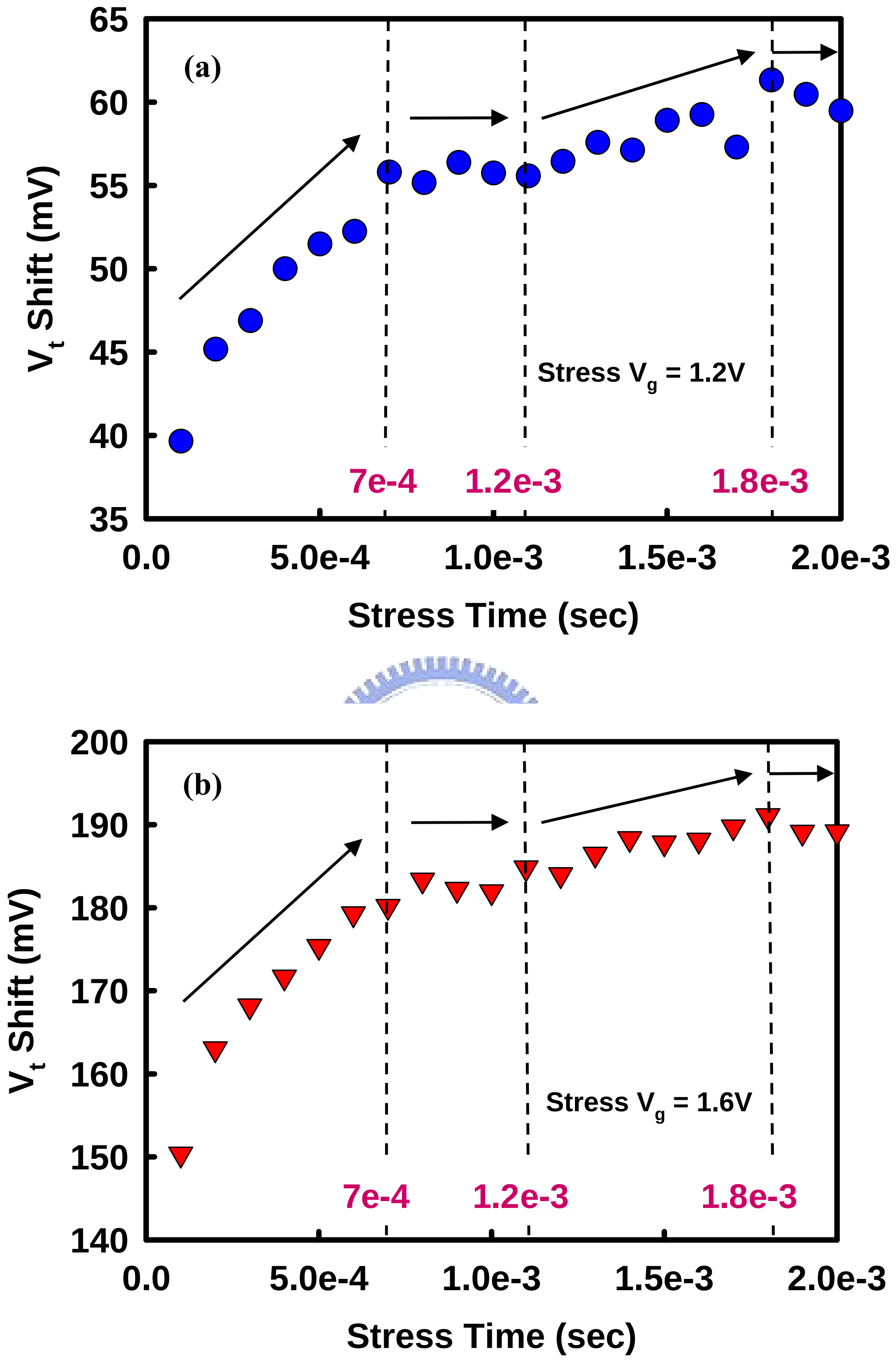


Fig. 3-15 A time dependence on the charge trapping effect (short-time stress, up to 2 ms)
(a) Stress V_g = 1.2 V (b) Stress V_g = 1.6 V.

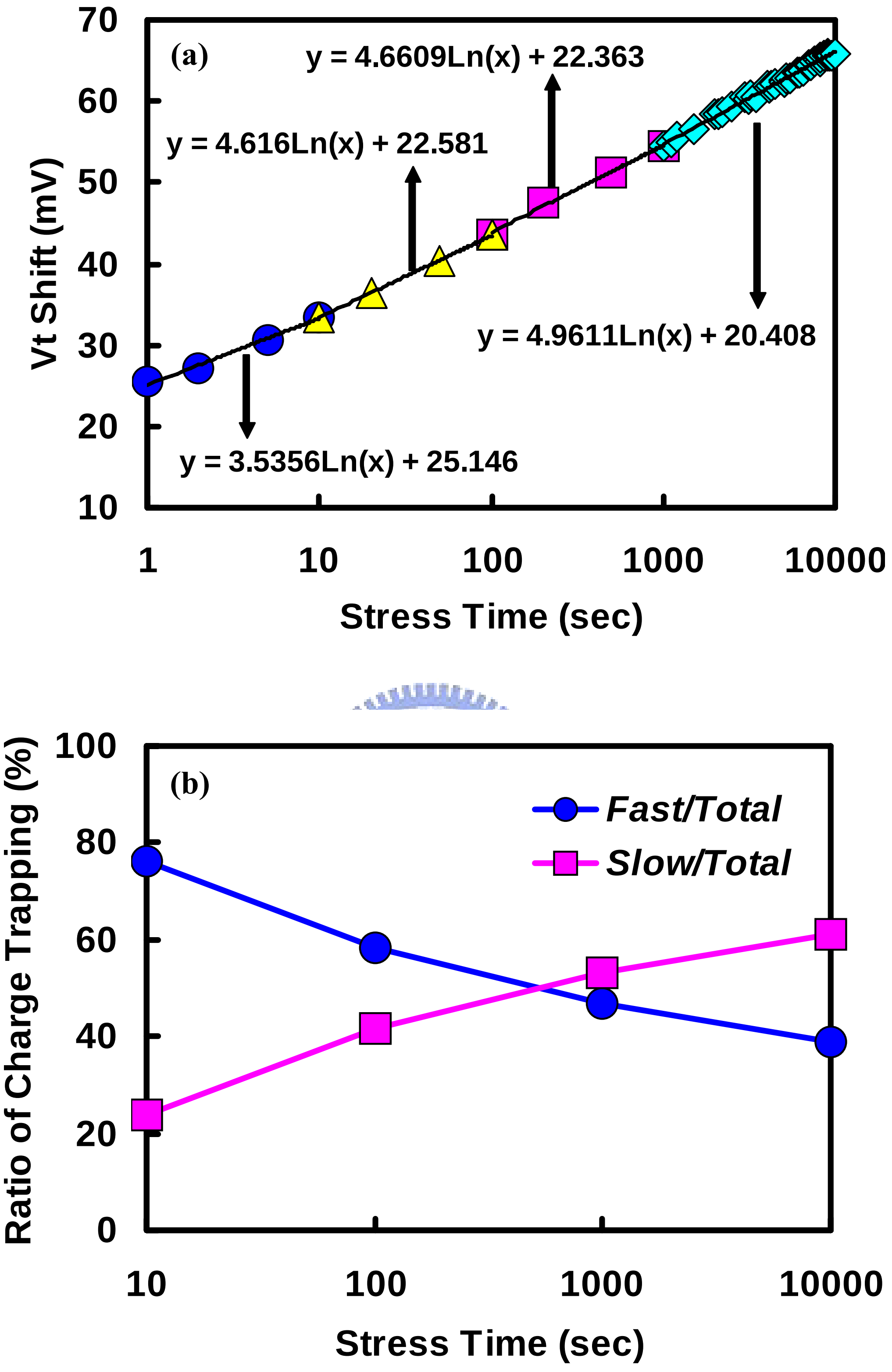


Fig. 3-16 A time dependence on the charge trapping effect (long-time stress, up to 10^4 sec) (a) Threshold voltage shift in PBTI degradation (b) Fast trapping and slow trapping behaviors versus stress time.

Chapter 4

Charge De-trapping Behavior in High-κ Gate Dielectrics

4.1 Introduction

High-κ gate dielectrics have been considered as the most potential candidate to replace conventional SiO_2 in next generation of CMOS technology due to the superior ability of suppressing the large direct tunneling gate leakage current [1-2]. Numbers of related researches and practical achievements have been published to demonstrate the feasibility and compatibility for both of fabrication process and device performance, especially for Hf-based high-κ gate dielectrics [3-6]. However, several critical issues, such as Fermi-level pinning effect, channel mobility degradation, and charge trapping/de-trapping phenomena have attracted a lot of attentions on the integration challenges of high-κ gate dielectrics [7-9]. In chapter 3, we have mentioned that the Fermi-level pinning effect and the channel mobility degradation can be effectively improved by means of some practicable methods (metal gate and strain effect). Nevertheless, the charge trapping/de-trapping are still the significant issues that we have concerned much, and numbers of related researches such as trap properties [10-13], appropriate measurements [14-18], impacts of device performance and reliability [19-20] all have still kept on high-k gate dielectrics. In the previous works, we have systematically analyzed the physical mechanism of charge trapping behavior in high-κ gate dielectrics. However, high-κ gate dielectrics not only have significant charge trapping effect but also have critical charge de-trapping according to the charge relaxation occurred inevitably during device operation [21-25]. For high-κ gate dielectrics, the intrinsic properties of a large number of imperfect atomic bonding are responsible the significant charge trapping/de-trapping phenomena [26-28]. Therefore, both charge trapping/de-trapping are inevitable to suffer with the introduction of defect-much high-κ materials.

In this chapter, the charge de-trapping behavior in nMOSFETs with Hf-based high-κ gate dielectrics was carefully investigated through stress voltage, recovery voltage, and based SiO_2 thickness to realize the dynamics of charge de-trapping. Similar to the investigations of charge trapping behavior, the charge de-trapping behavior were also analyzed in the aspects of both fast de-trapping and slow de-trapping in order to realize the influences on high-κ gate dielectrics. The electrical characteristics were appropriately extracted in the related measurements to effectively analyze the physical mechanism of charge de-trapping behavior. Finally, we also have developed an universal model to well explain charge de-trapping kinetics and realize its impact on device performance and reliability.

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4.2 Experimental Procedures

In this study, nMOSFETs were fabricated on (100) p-type Si wafers. After a standard RCA cleaning with a final HF-dip, a based oxide SiO_2 (0.8 nm and 1.4 nm) was thermally grown to be thin interfacial layer. A 3.2 nm HfO_2 layer was deposited by ALD system, followed a high temperature post deposition annealing (PDA) to optimize the film quality. Finally, a metal gate with workfunction (Φ_B) = 4.2 eV was conducted by PVD technique to perform the gate stack, then the following stand CMOS process were implemented to complete the total device fabrication. The electrical characteristics were investigated through the techniques of keithley Model 4200-SCS semiconductor characterization system and keithley pulse IV measurement.

4.3 Results and Discussions

4.3.1 Modeling of Charge De-trapping Behavior

Charge de-trapping effect is a non-neglected problem for the stabilities of device performance and reliability. In this chapter, the chare de-trapping behavior was also modeled as the same as charge trapping behavior due to the attentively considerations for the intrinsic properties of numbers of bulk defects in high-κ gate dielectrics themselves. The related physical mechanism was analyzed as the following model:

$$\frac{dn_{de}}{dt}=\frac{(n_{de,MAX}-n_{de})}{\tau_e} \qquad (4.1)$$

$$n_{de}=n_{de,MAX}\left[1-\int\frac{\rho(\tau_e)}{n_{de,MAX}}\cdot\exp(-\frac{t}{\tau_e})\cdot d\tau_e\right]=n_{de,MAX}\left[1-\exp(-(\frac{t}{\tau_{e0}})^{\gamma})\right] \qquad (4.2)$$

$$where\quad n_{de,MAX}=n_{de,MAX}(V_{G,recovery})$$

$$\Delta V_T=\Delta V_{\max}-\Delta V_{de}=\Delta V_{residue}+\Delta V_{de,MAX}\cdot\exp\left[-(\frac{t}{\tau_{e0}})^{\gamma}\right] \qquad (4.3)$$

$$where\quad \Delta V_{\max}=\frac{q\cdot n_{T,MAX}\cdot x_{eff}}{\varepsilon\cdot area},\Delta V_{de,MAX}=\frac{q\cdot n_{de,MAX}\cdot x_{eff}}{\varepsilon\cdot area},\Delta V_{residue}=\Delta V_{\max}-\Delta V_{de,MAX}$$

Fig. 4-1 showed a linear relation between the V_t shift and normalized $I_{d.sat}$ degradation under static PBTI stress, which can be equally applied to various stress voltages (stress Vg = 1.5 ~ 2.0V). Hence the modeling of charge de-trapping behaviors can be transferred form threshold voltage degradation into saturation drain current degradation as the following equations:

The original equation of (4.3)

$$\Delta V_T=\Delta V_{residue}+\Delta V_{de,MAX}\cdot\exp\left[-(\frac{t}{\tau_{e0}})^{\gamma}\right]$$

The transformed equation as below:

$$\Delta I_{d,sat} / I_{d0,sat} \approx \Delta I_{residue} + \Delta I_{MAX} \cdot \exp\left[-(\frac{t}{\tau_{e0}})^{\gamma} \right] \tag{4.4}$$

In Fig. 4-2 the charge de-trapping behavior in HfO$_2$/SiON gate stack was successfully modeled under various stress voltages. The decreasing fitting parameters γ indicated much numbers of recovered chares with respect to greater quantity of injected charges at higher stress voltage conditions. On the other hand, the charge de-trapping behavior was also successfully modeled under various recovery voltages in Fig. 4-3. The tendency of fitting parameters γ revealed a wide distribution (= large probability) of chare recovery at greater recovery force (^{ex} V_r = -1.4V). Both fine fitting results in the PBTI degradation under various stress voltages and recovery voltages strongly demonstrated that the apparent charge relaxation occurred in high-κ gate dielectrics indeed led the great impacts of charge de-trapping behavior on device reliability.

4.3.2 The Influences of Stress Voltage on Charge De-trapping Behaviors in High-κ Gate Dielectrics

The charge de-trapping in high-κ gate dielectrics under an electrical recovery process also reveal the distinct behaviors on two stages of time demarcation that de-trapping with fast and slow responses of discharging time constant. As the same as the charge trapping behavior, charge de-trapping induces a large number of trapping density instantly in the initial of recovery process, and reveals the qualitative and quantitative difference during a recovery process. Fig. 4-4 shows a definition of fast de-trapping (time scale at t = 100 ~ 101.78 sec) and slow de-trapping (time scale at t = 101.78 ~ 200 sec) established in our studies for the recovery measurement with the conventional DC method. In order to analyze the experimental data, the fast de-trapping, slow de-trapping, total de-trapping are extracted form the V_t shift in the recovery time of t = 0 ~ 1.78 sec, t = 1.78 ~ 100 sec, t = 0 ~ 100 sec, respectively. Fig. 4-5(a) and Fig. 4-5(b) showed analysis of fast de-trapping, slow de-trapping, and total de-trapping in the nMOSFETs with HfO_2 (3.2 nm)/SiO_2 (0.8 nm) and HfO_2 (3.2 nm)/SiO_2 (1.4 nm) gate stacks under various stress voltages. The fast de-trapping is apparent to dominate the whole recovery process for all stress voltages under recovery V_r = -1.6V while the slow trapping only has less contribution to recovered charges. The difference of interfacial layers (IL) thickness would affect the charge tunneling probability between the high-κ bulk and Si-substrate. In Fig. 4-6(a), the distinct impacts of IL thickness on charge recovery were represented by the recovered charge under various stress voltages. The greater numbers of recovered charged were found in the based SiO_2 = 0.8 nm to clearly explain larger tunneling probability in the thinner interfacial layer. However, in Fig. 4-6(b), the close quantity of non-recoverable charges discovered under various stress voltages is considered to be the responsibility of “slow traps” in high-κ bulk. In Fig. 4-7(a), the impacts of IL thickness were also shown on the recovery (%) under various stress voltages. [A recovery (%) was defined as (total charge de-trapping)/(total charge trapping) × 100% in our studies]. As expectations, thicker IL thickness represented lower recovery (%) according to lower charge tunneling probability. Moreover, an apparent degradation of recovery (%) found with elevated stress voltage was referred to greater numbers of injected charge at higher stress voltage which caused the difficulty of charge recovery and the increase of residual charges in high-κ gate dielectrics. In addition, an independence of IL thickness was found in the fast/total de-trapping ratio under the same recovery force of V_r = -1.6V in Fig. 4-7(b). [A fast/total de-trapping ratio is defined as (fast de-trapping)/(total de-trapping) × 100% in our studies] The results are considered to be attributed to the intrinsic properties of those “shallow traps” in HfO_2 which are responsible for the “fast” trapping/de-trapping behaviors thus fast/total de-trapping ratio is independent of IL thickness. In chapter 3, we have discovered that charge trapping behaviors are different before and after the occurrence of FN-tunneling. In order to realize fundamental mechanisms of fast/slow de-trapping behaviors in the entire regime of stress voltage, a modeling of charge recovery was analyzed in Fig. 4-8. The identical mathematical fitting (both are logarithmic behaviors) revealed the unique physical mechanism for both fast/slow de-trapping behaviors under all stress voltages because of the sole discharging conduction of charge tunneling from high-κ bulk to Si-substrate. The related fitting results were also represented in Table 4-1.

4.3.3 The Influences of Recovery Voltage on Charge De-trapping Behaviors in High-κ Gate Dielectrics

Fig. 4-9(a) and Fig. 4-9(b) showed analysis of fast de-trapping, slow de-trapping, and total de-trapping in the nMOSFETs with HfO_2 (3.2 nm)/SiO_2 (0.8 nm) and HfO_2 (3.2 nm)/SiO_2 (1.4 nm) gate stacks under various recovery voltages. The similar behaviors of fast de-trapping and slow de-trapping under all recovery voltages were shown in both IL = 0.8 nm and IL = 1.4 nm. Moreover, the fast de-trapping is still dominant in all conditions of recovery voltages as the same as the results investigated under various stress voltages. In Fig. 4-10(a) and Fig. 4-10(b), the comparisons of charge de-trapping behaviors between IL = 0.8 nm and IL = 1.4 nm under various recovery voltages were shown in the recovered charges and non-recoverable charges, respectively. Thinner IL thickness accompanies with larger tunneling probability to induce great numbers of injected charges which is responsible for considerable recovered charges and significant residual charges. On the other hand, thicker IL thickness suppress most of injected charges thus lower recovered charges and residual charges are observed in IL = 1.4 nm. In Fig. 4-11, the recovery (%) is as a strong function of recovery voltage, but it is almost independent of IL thickness. For further studying of charge recovery, the fast/trapping de-trapping ratio was illustrated in Fig. 4-12(a). The fast/trapping de-trapping ratio shows a strong dependence on recovery voltages when charge recovery is under significant recovery conditions (more negative: recovery V_r = -1.0V, -1.5V, -1.6V). However, the fast/trapping de-trapping ratio become to be the invariant value close 60% which is consistent with the fast/total trapping ratio under various stress voltages illustrated in Fig. 3-9(a) [Now in Fig. 4-12(a)] when charge recovery is under weaker recovery force (recovery V_r = -0.5V, 0V, 0.5V, 1.0V where stress V_g = 1.5V). In Fig. 4-13(a)-(c), the charge de-trapping behaviors were illustrated as the related band diagrams under various recovery conditions. When recovery V_r = 0V, the band bending is adverse for the occurrence of charge recovery with the considerations of self band adjustment according to the workfunction difference between gate electrode and Si-substrate. The available charge tunneling back to Si-substrate is only accessible for those shallow traps located close to conduction of HfO_2, but the charge tunneling for those deep traps all are forbidden due to the trapping levels are below the Fermi-level of Si-substrate. When recovery V_r = -0.5V which is close to the flat band condition, the capability of charge de-trapping is similar to V_r = 0V. Although the available tunneling levels for deep traps are increase, the small quantity of trapped charges at those deep trap centers has less contribution to charge recovery. When recovery V_r = -1.6V, both shallow and deep traps are satisfied with the available charge tunneling back to Si-substrate, thus highly recovery is observed at higher recovery voltage. Therefore, the efficiency of charge recovery is demonstrated to be decided by the available tunneling levels to Si-substrate under related recovery voltages. This concept is clearly displayed in a schematic illustration of V_r = 0V in Fig. 4-14. Besides, the comparisons of charge de-trapping between based

SiO_2 = 0.8 nm and 1.4 nm under various recovery voltages is shown in Fig. 4-15. [Charge de-trapping ratio (R) is defined as (Charge de-trapping in IL = 1.4 nm)/(Charge de-trapping in IL = 0.8 nm) in our studies]. The distinct tendencies is observed in the two regions decided at V_r = -0.5V. When recovery V_r = -1.0V, -1.5V, -1.6V (strong recovery force), an identical R value of 0.3 which is considered to be highly dependent on the intrinsic properties of those shallow traps (oxygen vacancies - Vo^{2+}, Vo^{-}, Vo^{2-} and grain boundary defects) in HfO_2 is observed [12-13, 29-34]. These shallow traps are responsible for the great quantity of fast trapping/de-trapping. Once the chare de-trapping is under the sufficient recovery force that allows almost all of trapped charges (for both shallow traps and deep traps ; the stress voltage is the same as 1.5V for all recovery conditions indicates the same quantity of injected charge for every recovery conditions) tunneling back to Si-substrate, thus the tunneling ratio between IL = 0.8 nm and IL = 1.4 nm is represented as an identical value of 0.3. On the other hand, a linear behavior of tunneling ratio between these two IL thickness is observed when V_r = -0.5V, 0V, 0.5V, 1.0V (weak recovery force). Because lower tunneling probability in these crucial recovery conditions which has been explained through the schematic diagrams of related band bending induces the magnitude of charge de-trapping to be quite low and close to each other. Therefore, a linear tendency the de-trapping ration between IL = 0.8 nm and IL = 1.4 nm would be toward to the value of “1.0” due to the difficulty of available charge tunneling under the insufficient recovery force.

4.4 Summary

In our studies, we have systematically investigated the charge de-trapping behaviors in nMOSFETs with HfO_2/SiO_2 gate stack. The fine modeling fitting demonstrated that the relaxation of trapped charges in high-κ gate dielectrics is mainly responsible for the charge recovery. The mathematical modeling fitting shows the only logarithmic relation in the regime of all stress voltages to indicate the asymmetric behaviors between charge trapping and charge de-trapping. Besides, the experimental results also verified predomination of fast de-trapping (shallow traps) in whole charge recovery as the same as the charge trapping behavior. Furthermore, the dependences of recovery voltages on the charge de-trapping behavior were carefully investigated to explain that the physical mechanism of charge de-trapping is with respect to the available charge tunneling back to Si-substrate. The fast/total de-trapping ratio shows an identical value of 60% which is consistent with the findings in charge trapping behavior under those weak recovery force (V_r = -0.5V, 0V, 0.5V, 1.0V) to firmly verify the above explanation. Therefore, those shallow traps (oxygen vacancies - Vo^{2+}, Vo^{-}, Vo^{2-} and grain boundary defects) in HfO_2 are not only mainly responsible for the fast trapping behavior but also as the predominant factor for the fast de-trapping. In the comparisons of charge de-trapping between different IL thickness, the defined ratio of (Charge de-trapping in IL = 1.4 nm)/(Charge de-trapping in IL = 0.8 nm) revealed the distinct tendencies in the regimes of strong recovery (V_r = -1.0V, -1.5V, -1.6V) and weak recovery (V_r = -0.5V, 0V, 0.5V, 1.0V), respectively. An identical ratio of 0.3 observed under strong recovery force is considered as the intrinsic properties with respect to those shallow traps in HfO_2 itself which is the strong evidences to confirm the above discussions of charge de-trapping. Finally, from these experimental results, a universal model of charge de-trapping has been established to firmly demonstrate the aspects of trap energy level distribution through the systematic investigations of recovery voltages on the charge de-trapping behavior.

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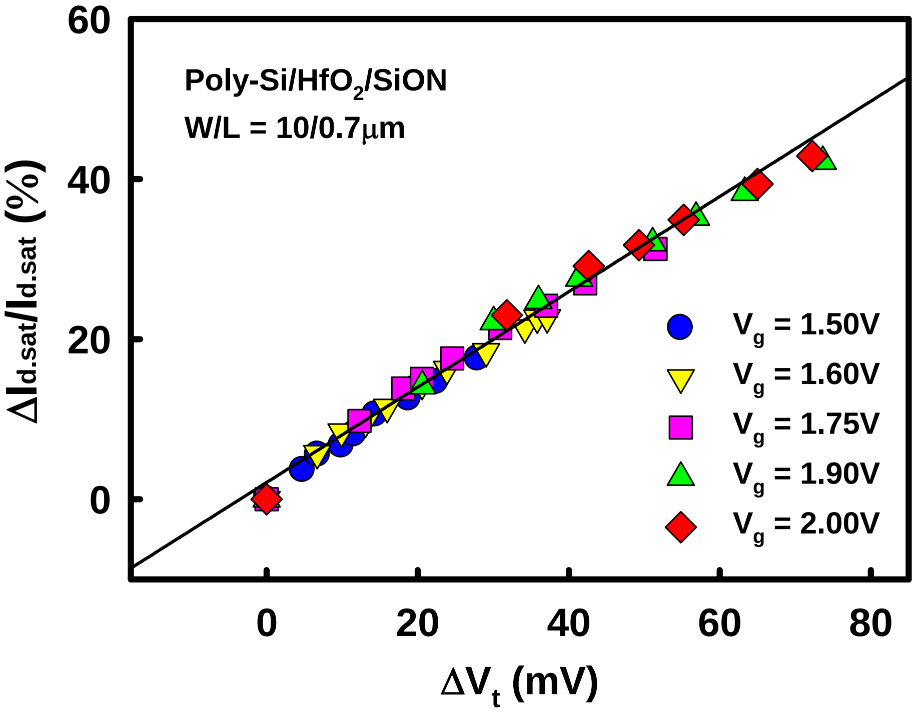

Fig. 4-1 Linear relation between normalized saturation drain current degradation and threshold voltage shift (ΔV_t) under various stress voltages.

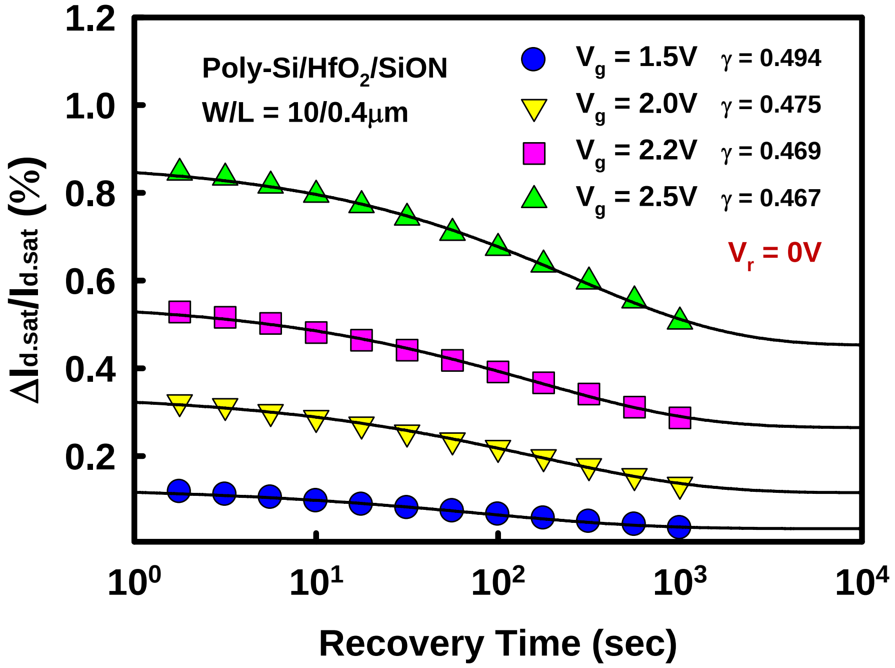

Fig. 4-2 Successful modeling fitting of charge de-trapping in HfO$_2$/SiON gate stack under various stress voltages.

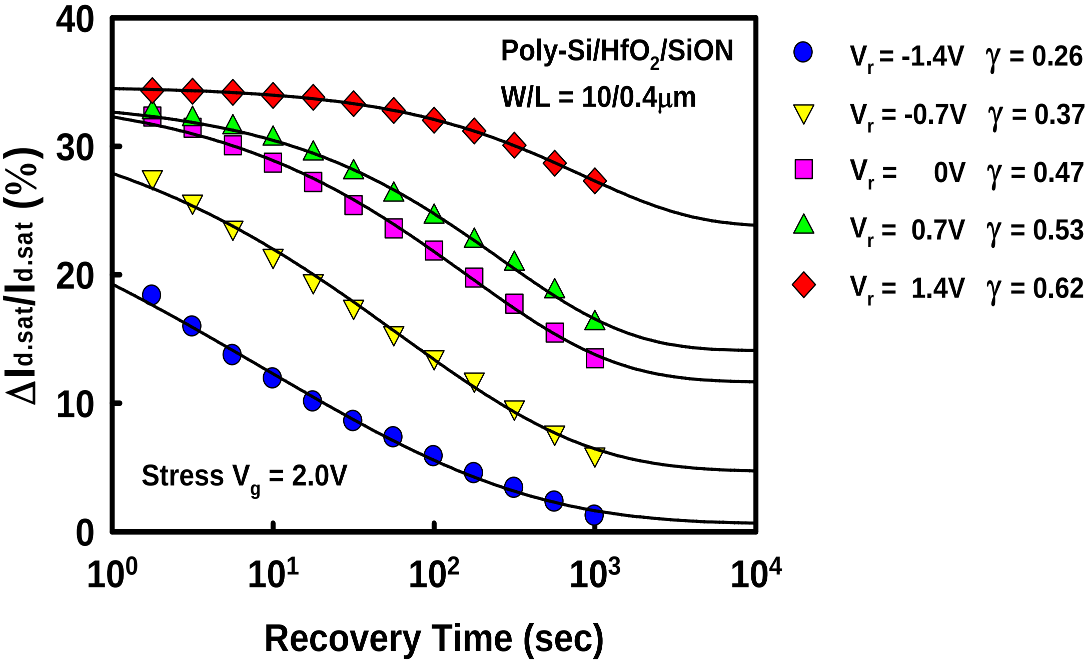

Fig. 4-3 Successful modeling fitting of charge de-trapping in HfO$_2$/SiON gate stack under various recovery voltages.

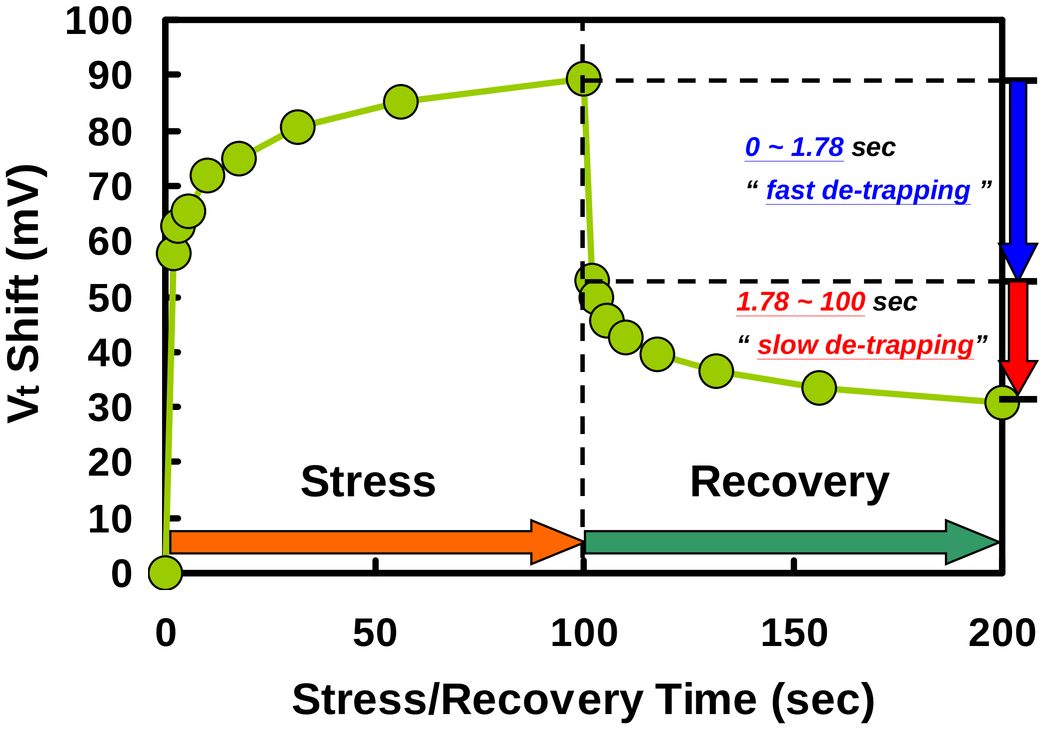

Fig. 4-4 A definition of fast de-trapping (t = 0 ~ 1.78 sec) and slow de-trapping (t = 1.78 ~ 100 sec) in our studies for the PBTI measurement with the conventional DC method.

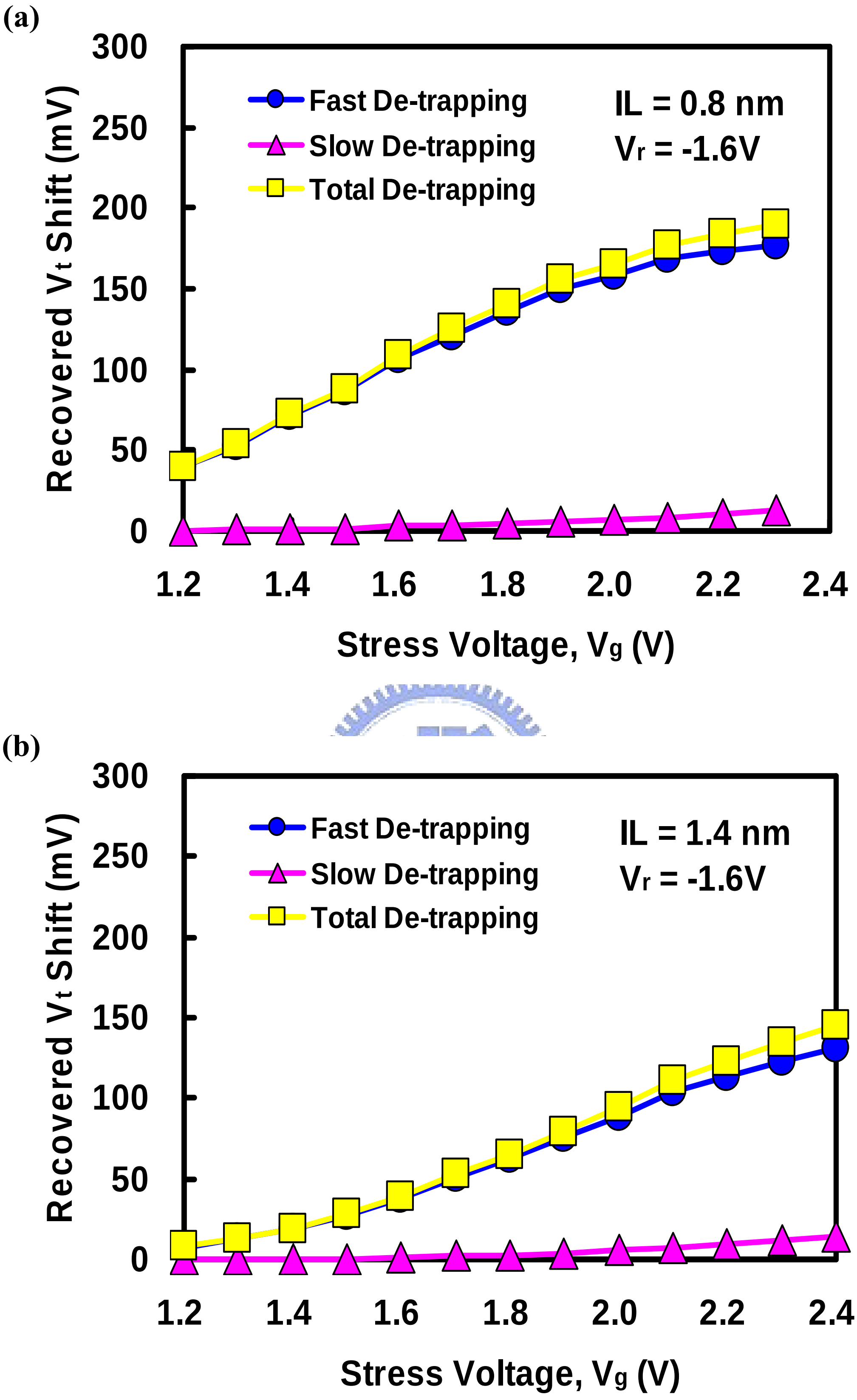

Fig. 4-5 Analysis of fast de-trapping, slow de-trapping, and total de-trapping under various stress voltages (a) Based SiO_2 = 0.8 nm (b) Based SiO_2 = 1.4 nm.

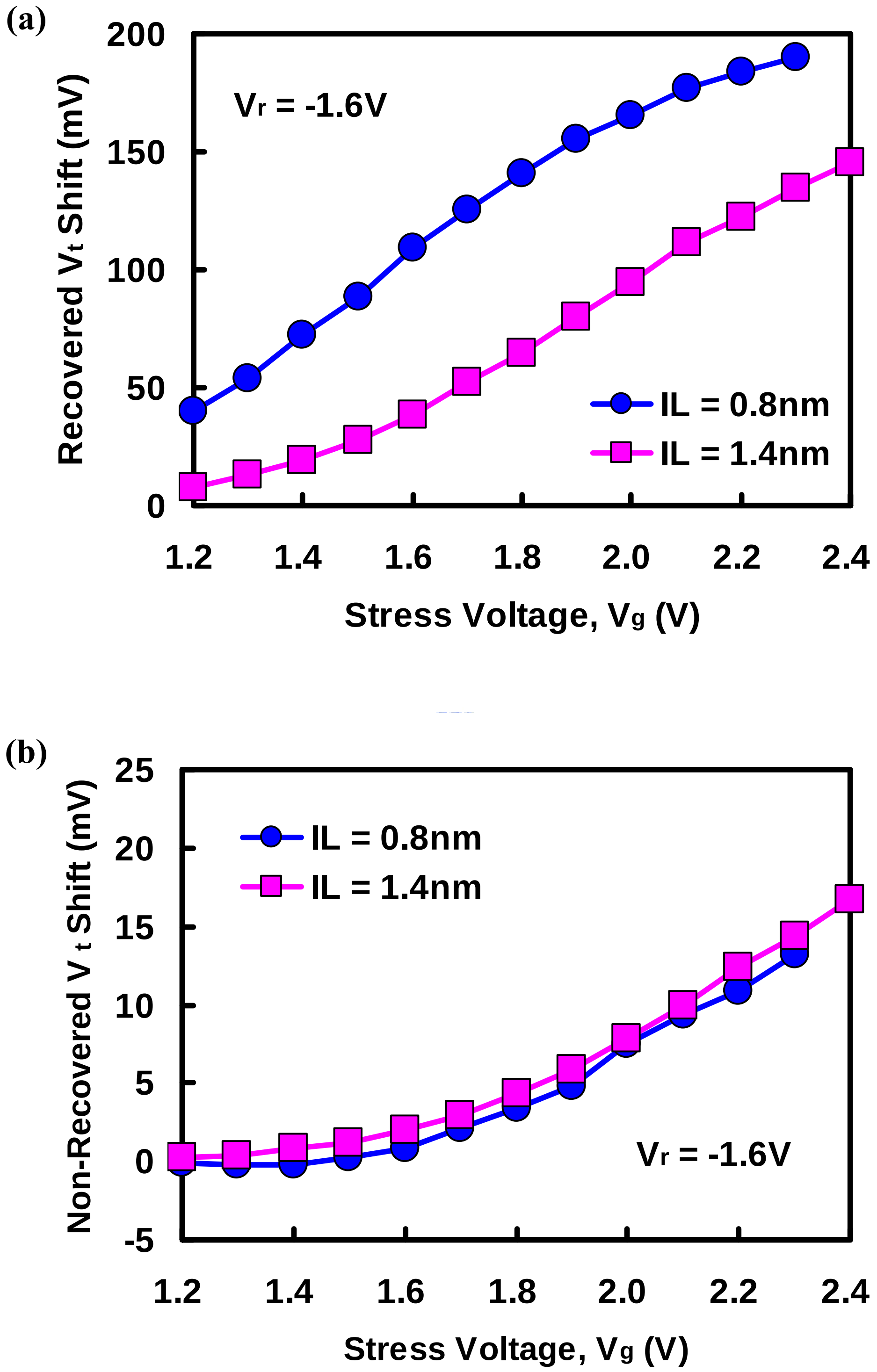

Fig. 4-6 Charge de-trapping behaviors in both based SiO_2 = 0.8 nm and 1.4 nm under various stress voltages (a) Recovered V_t shift (related to recovered charges) (b) Non-recovered V_t shift (related to non-recovered charges).

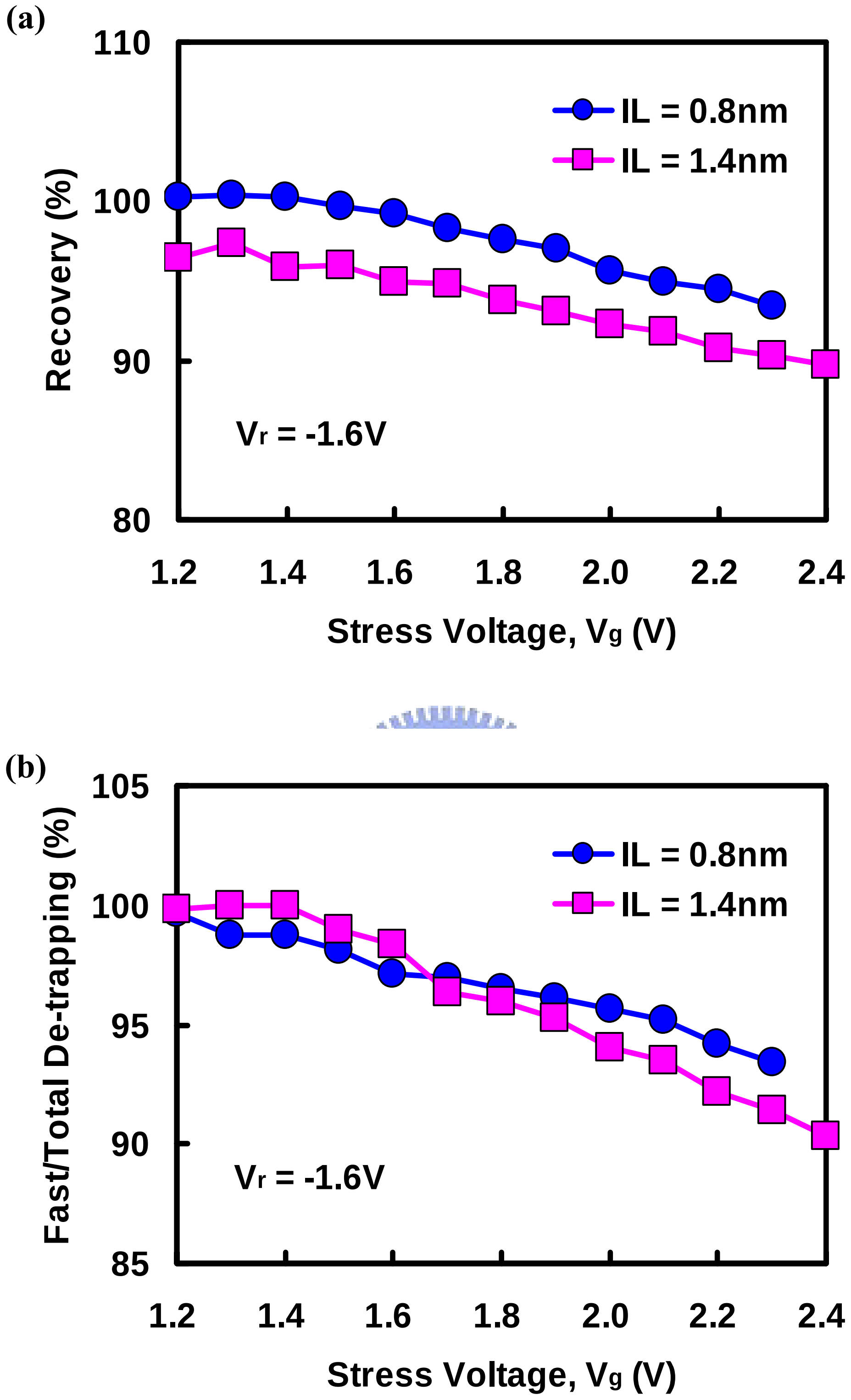

Fig. 4-7 Charge de-trapping behaviors in both based SiO_2 = 0.8 nm and 1.4 nm under various stress voltages (a) Recovery (%) (b) Fast/total de-trapping ratio. [A fast/total de-trapping ratio is defined as (fast de-trapping)/(total de-trapping) × 100% in our studies]

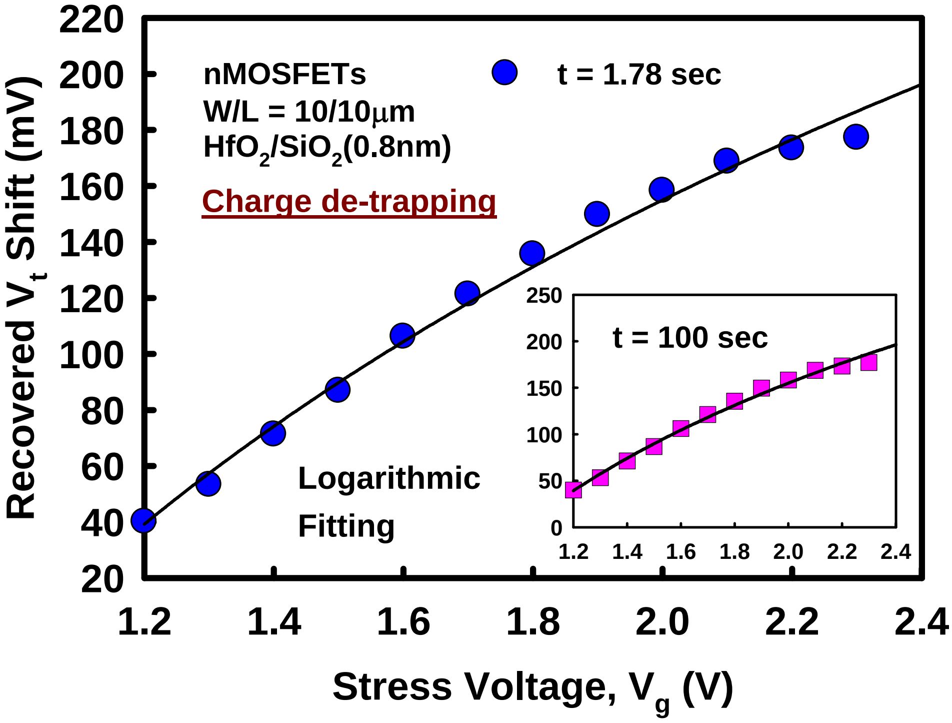

Fig. 4-8 Analysis of fast de-trapping, slow de-trapping, and total de-trapping under various stress voltages (a) Based SiO_2 = 0.8 nm (b) Based SiO_2 = 1.4 nm.

Stress V_g Time	All stress V_g
Fast t < 1.78 sec	de-trapping Logarithmic
Slow t > 1.78 sec	de-trapping Logarithmic

Table 4-1 Modeling fitting of charge de-trapping under all stress voltages.

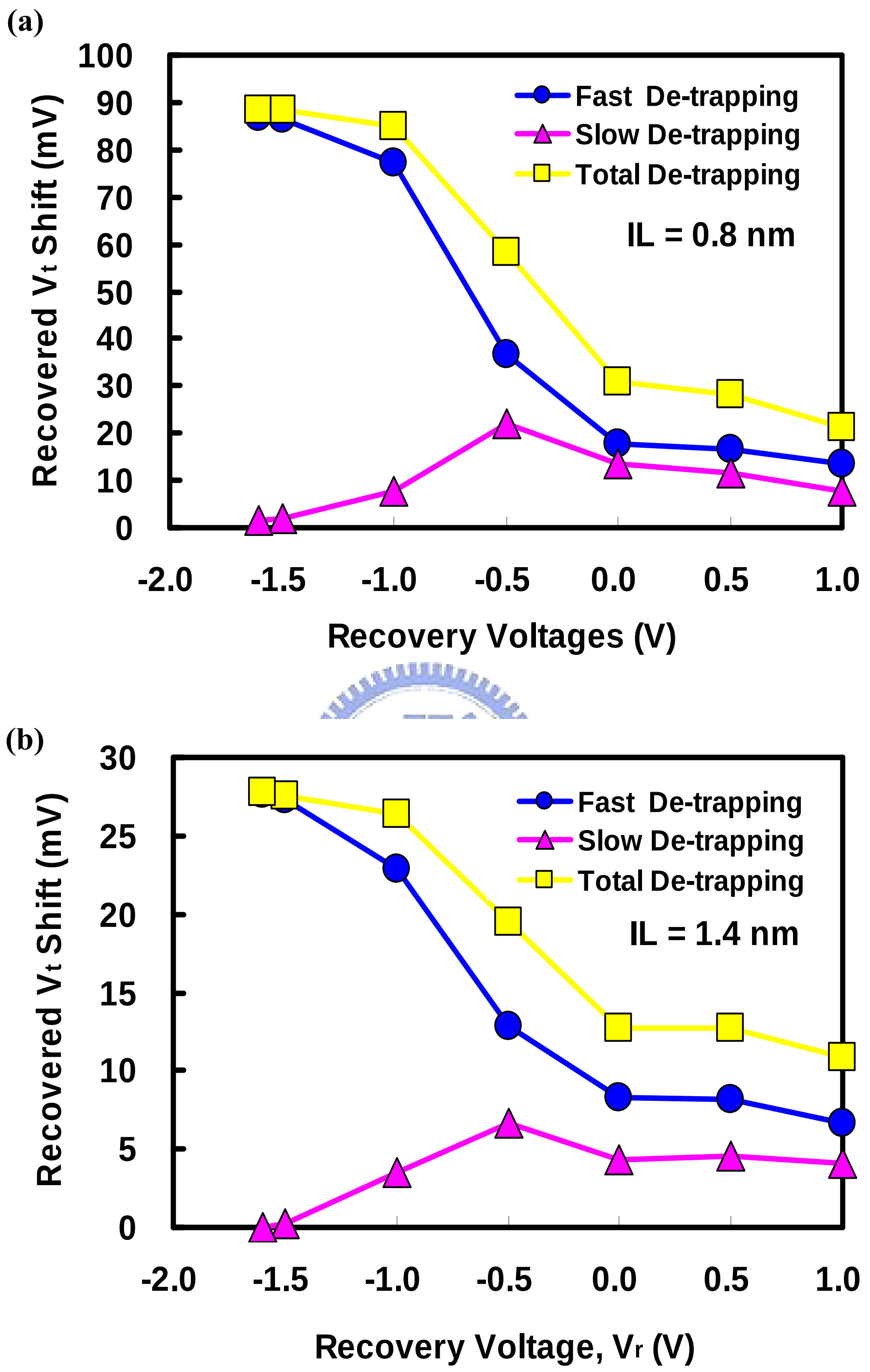

Fig. 4-9 Analysis of fast de-trapping, slow de-trapping, and total de-trapping under various recovery voltages (a) Based SiO_2 = 0.8 nm (b) Based SiO_2 = 1.4 nm.

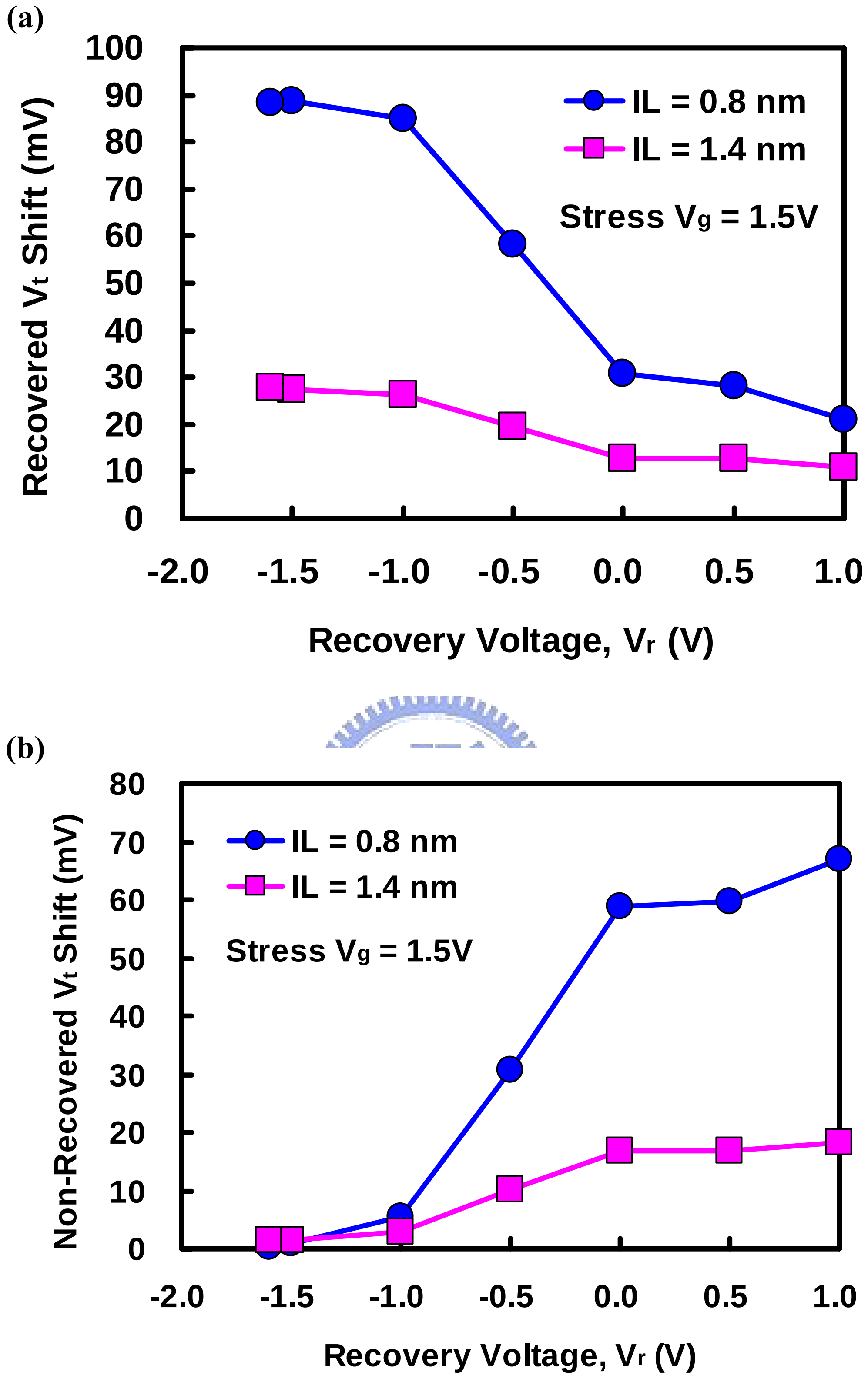

Fig. 4-10 Charge de-trapping behaviors in both based SiO_2 = 0.8 nm and 1.4 nm under various recovery voltages (a) Recovered V_t shift (related to recovered charges) (b) Non-recovered V_t shift (related to non-recovered charges).

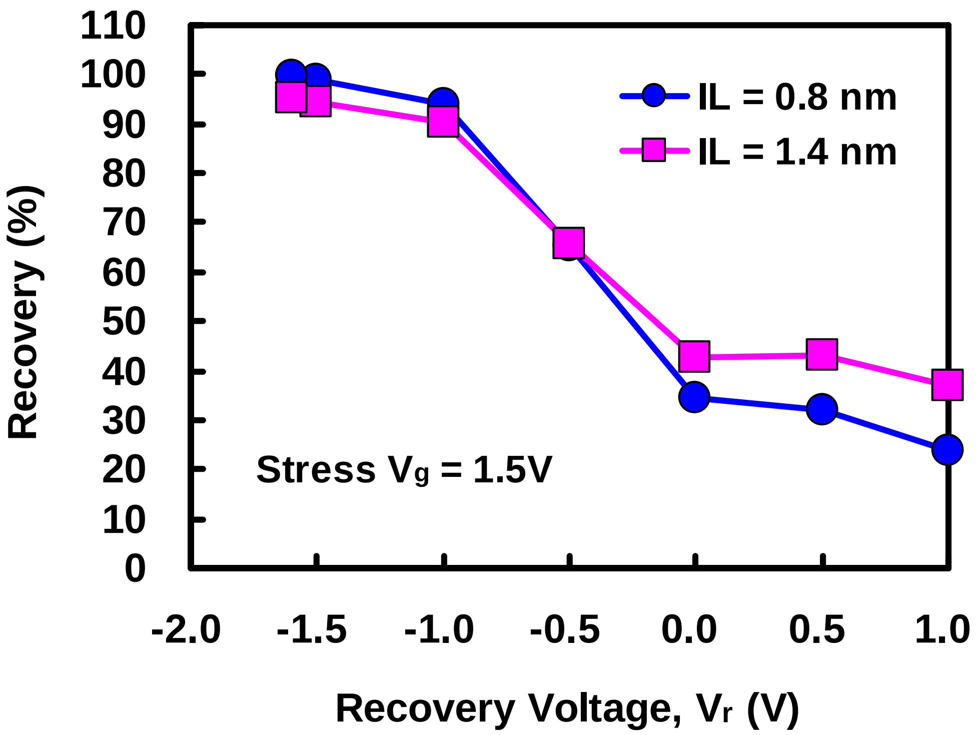

Fig. 4-11 Recovery (%) in both based SiO_2 = 0.8 nm and 1.4 nm under various recovery voltages. [Recovery (%) is defined as (total de-trapping)/(total trapping) × 100% in our studies]

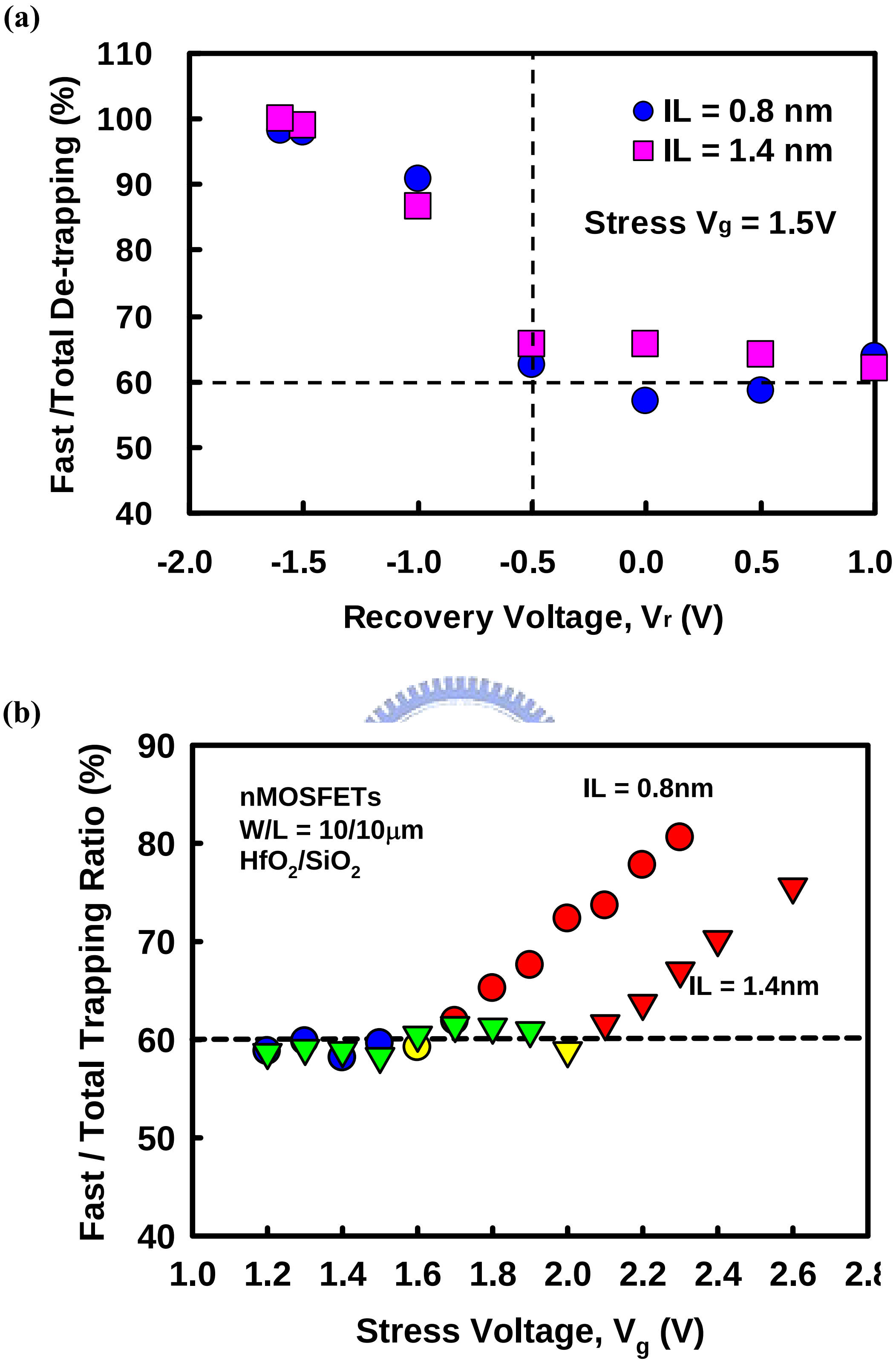

Fig. 4-12 (a) Fast/total de-trapping ratio under various recovery voltages. (b) Fast/total trapping ratio under various stress voltages illustrated in Fig. 3-9(a). [Fast/total de-trapping ratio is defined as (fast de-trapping)/(total trapping) × 100% in our studies]

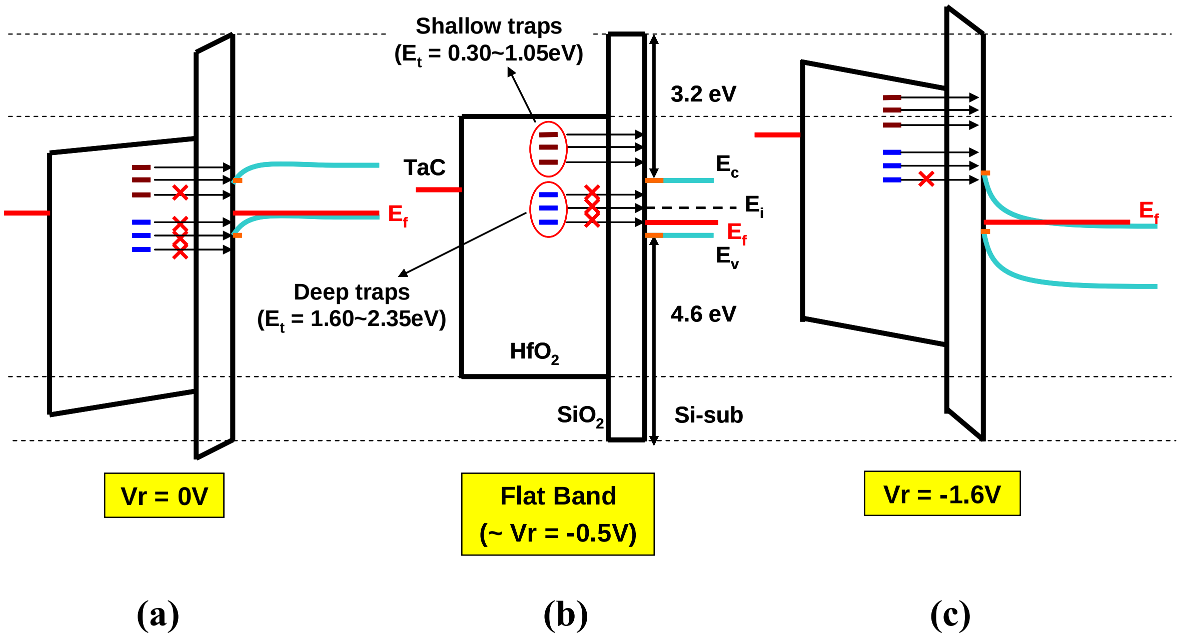
Shallow traps
(E_t = 0.30~1.05eV)
3.2 eV
TaC
E_c
E_i
E_f
E_v
E_f
E_f
Deep traps
(E_t = 1.60~2.35eV)
4.6 eV
HfO$_2$
SiO$_2$
Si-sub
Vr = 0V
Flat Band
(~ Vr = -0.5V)
Vr = -1.6V
(a)
(b)
(c)

Fig. 4-13 Band diagram of charge de-trapping under various recovery V_r conditions. (a) Recovery V_r = 0V (b) Recovery V_r = -0.5V (c) Recovery V_r = -1.6V.

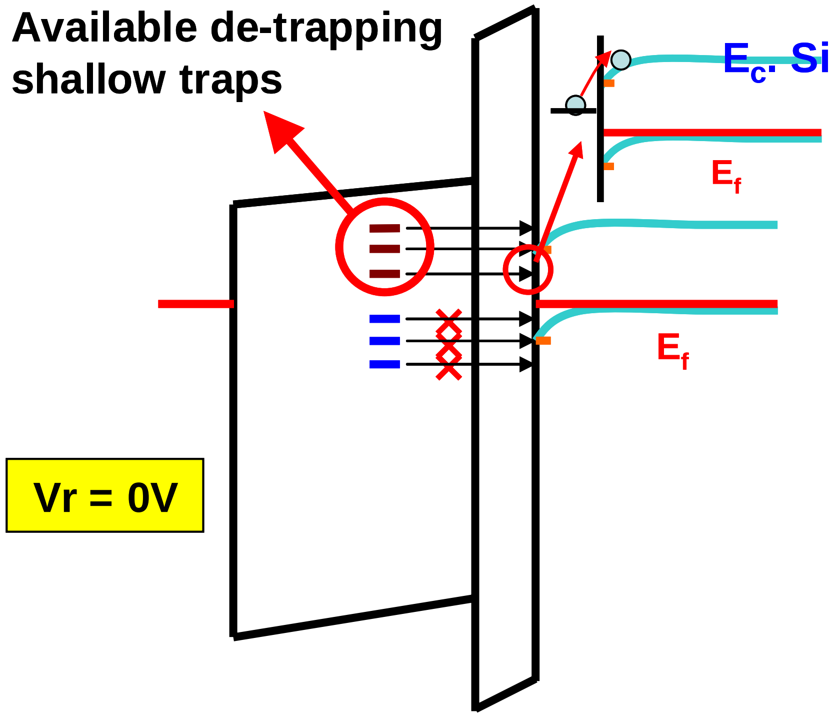
Available de-trapping shallow traps
E_c: Si
E_f
E_f
Vr = 0V

Fig. 4-14 A schematic illustration of available de-trapping shallow traps under recovery condition of $V_r = 0V$.

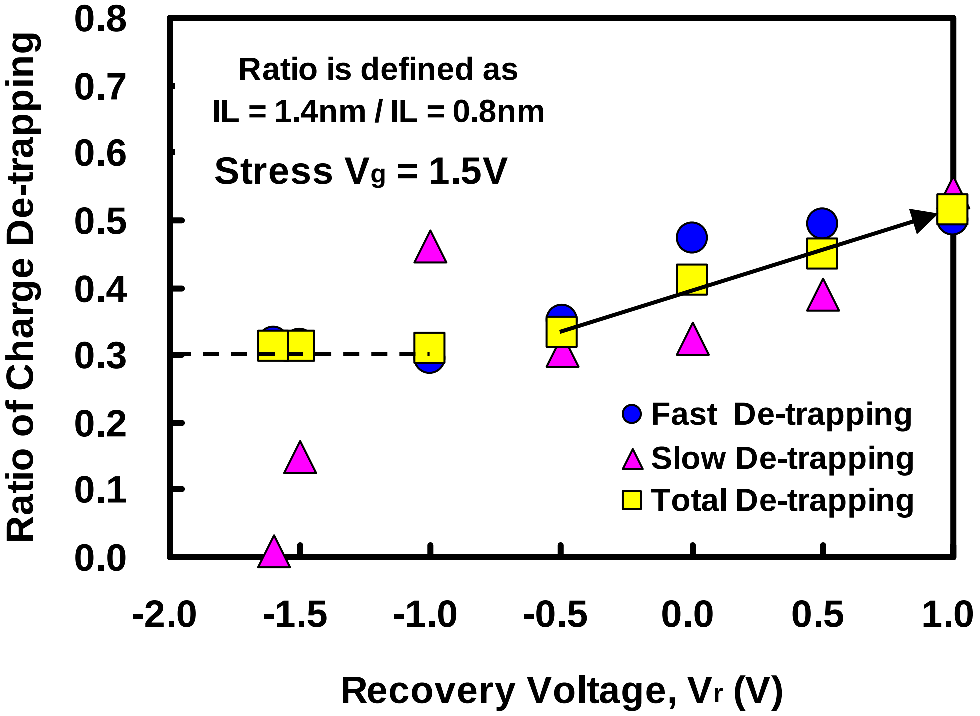

Fig. 4-15 The comparisons of charge de-trapping between based SiO_2 = 0.8 nm and 1.4 nm under various recovery voltages. [Charge de-trapping ratio is defined as (Charge de-trapping in IL = 1.4 nm)/(Charge de-trapping in IL = 0.8 nm) in our studies]

Chapter 5

Fast Transient Charge Trapping/De-trapping in High-κ Gate Dielectrics

5.1 Introduction

Charge trapping/de-trapping phenomena are two of the most critical issues for the application of high-κ gate dielectrics on the CMOS technology. In the recent years, numbers of research groups have done a lot of related investigations to further understand the fundamental characteristics and physical mechanisms about the charge trapping/de-trapping in high-κ gate dielectrics. Those include: J. C. Lee, B. H. Lee, and D. L. Kwong et al. (– University of Texas, USA; Integration of high-κ fabrication process) [1-3], S. Zafar et al. (– IBM, USA; Early modeling of charge trapping/de-trapping in DC measurements) [4-5], G. Ribes and C. Leroux et al. (– ST Microelectronics, France; Modeling of charge trapping/de-trapping in pulse technology) [6-9], J. Robertson et al. (– Cambridge University, UK; Atomic structure, and trap energy levels) [10-12], C. D. Young et al. (– SEMATECH, USA; Electrical methodologies for fast transient charge behaviors) [13-15], and T. Wang et al. (– National Chiao-Tung University, Taiwan; Modeling of charge trapping/de-trapping and their impacts on reliability issues) [16-17]. Many of electrical measurements have been adopted to analyze the electrical characteristics in high-κ gate dielectrics in order to realize the impacts of charge trapping/de-trapping on the device performance and the related reliability. In early years, the investigations of device performance and reliability are usually conducted through the DC measurements when the gate dielectric is SiO_2.

However, charge trapping/de-trapping effects in high-κ gate dielectrics are more significant and complex than they in SiO_2 [18-19]. Especially, the fast transient charge trapping/de-trapping behaviors in high-κ gate dielectrics might easily occur during only few micro-seconds (~μs) which those conventional DC methods can not monitor the "real" device characteristics in time [7, 20]. In other words, the charge trapping effect would quickly happen during a short interval between these sequences of DC measurements. Besides, the charge relaxation would also occur immediately once the electrical stress is removed form the devices.

In order to understand the real charge trapping/de-trapping behaviors without neglecting those fast transient charge trapping/de-trapping effects, a pulse IV measurement was adopted to character the real characteristics of charge trapping/de-trapping with a fine resolution of few nano-seconds (~ ns). In this chapter, the pulse IV measurements were systematically conducted through many critical factors such as stress voltages, stress time, recovery voltages, and temperatures in order to completely understand the true mechanisms of charge trapping/de-trapping within the fast transient behaviors. Besides, the influences of AC stress on PBTI degradation were also investigated through the practical applications of pulse IV measurements.

5.2 Experimental Procedures

In this study, nMOSFETs were fabricated on (100) p-type Si wafers. After a standard RCA cleaning with a final HF-dip, a based oxide SiO_2 (0.8 nm and 1.4 nm) was thermally grown to be thin interfacial layer. A 3.2 nm HfO_2 layer was deposited by ALD system, followed a high temperature post deposition annealing (PDA) to optimize the film quality. Finally, a metal gate with workfunction (Φ_B) = 4.2 eV was conducted by PVD technique to perform the gate stack, then the following stand CMOS process were implemented to complete the total device fabrication. The electrical characteristics were investigated through the techniques of keithley Model 4200-SCS semiconductor characterization system and keithley pulse IV measurement.

5.3 Results and Discussions

5.3.1 The Impacts of Fast Transient Charge Trapping/De-trapping in High-κ Gate Dielectrics and The Necessary of Pulse IV Measurements

In the past studies of CMOS technology, the conventional SiO_2 gate dielectrics is considered as “trapping-free” in those common DC measurements. In Fig. 5-1(a) and Fig. 5-1(b), the charge trapping effect was investigated on the nMOSFETs with SiO_2 gate dielectrics through both DC and pulse measurements. The fine matching of DC and pulse curves observed in the driving current, I_d-V_g, and G_m-V_g characteristics demonstrated the trapping-free properties for SiO_2. On the other hand, in Fig. 5-2(a) and Fig. 5-2(b), the same investigations were also conducted on the nMOSFETs with high-κ gate dielectrics. The degradation of DC results revealed the apparent influences of fast transient charge trapping while the pulse measurement has the sufficient ability avoid the critical issue. In addition, the deviation between DC and pulse measurement was found to be more significant with higher stress voltage in the saturation region that implied the charge trapping in high-κ gate dielectrics to be as the strong functions of the applied voltages (both V_g and V_d). In Fig. 5-3, the transient pulse-IV output waveforms were revealed under various stress voltages. The pulse IV results showed the trusty evidences to demonstrate the strong dependence of applied voltage on the charge trapping with the consideration of fast transient behavior. From the above discussions, the pulse measurement is considered to be a required methodology to exactly capture the real dynamics of charge trapping/de-trapping in high-κ gate dielectrics. The necessary of pulse measurement can be also understood through the electric measurements in high-κ gate dielectrics illustrated in Fig. 5-4 and Fig. 5-5. The pulse measurements do a real-time monitor to avoid the fast transient charge trapping effect in the I_d-V_g characteristic. Moreover, the pulse measurements also provided more accurate device reliability without the fast transient charge relaxation. Therefore, the pulse measurement is considered as the essentiality for the application of high-k gate dielectrics.

5.3.2 The Electrical Characteristics under Pulse IV Measurements

In Fig. 5-6, the PBTI degradations were investigated in HfO_2/SiO_2 gate stack through the pulse and DC measurements over several decades. It is apparent that the DC measurement can not represent the complete charge trapping behavior without the consideration of the fast transient effect below the scale of 10^0 sec while the pulse measurement can successfully do it and correctly describe the total charge trapping behavior. In Fig. 5-7(a) and Fig. 5-7(b), the DC and pulse results were modeled by the charge trapping model mentioned in chapter 3. Both of the DC and pulse showed the fine fittings to indicate that the charge trapping has a wide range of time scale over several decades. In Fig. 5-8(a) and Fig. 5-8(b), the fitting parameters of τ_0 and γ exhibited the highly similar tendencies in both DC and pulse measurements to imply that the chare trapping follows the same physical mechanism in both DC and pulse with the only difference of the respondence to trapping time constant. In order to further understand the charge trapping with the fast transient behavior, many key parameters mainly affected the high-κ gate dielectrics were extensively and systematically in pulse IV technique. In the aspect of stress voltage, the chare trapping is as a function of Power

Law behavior to indicate a strong dependence on the stress voltage in Fig. 5-9. In Fig. 5-10, larger quantity of recovered charges responded to the great numbers of injected charges at higher stress voltage which is also responsible for the significant residual charges under more crucial stress conditions. In our studies, the great impacts of applied gate bias on the quantity of trapped charges, recovered charges, and residual charges in high-κ bulk were surely confirmed through the pulse measurement with thinking about the fast transient behaviors. In Fig. 5-11, the impacts of stress voltage on the recovery (%) were also verified under various recovery voltages. The recovery force significantly determined the recovery (%) tendencies while the apparent independence of stress voltage conditions on the recovery (%) is observed in pulse results which are not fully consistent with the phenomena extracted form the DC measurement. It is considered that the de-trapping time constant (τ_0) is very close for the mostly shallow traps which are responsible for the fast discharging during the time scale of 100ms to 1ms despite any stress voltage. For the considerations of stress time, the chare trapping is as a function of logarithmic behavior which is associated with the charge tunneling behaviors and the related trap distribution in high-κ gate dielectrics in Fig. 5-12 [17, 21]. Besides, the logarithmic behavior also describes the charge trapping would be toward a saturation that satisfies with the concepts of chare filling at the relevant energy levels and further trapping at deeper levels with elevated time. In Fig. 5-13(a) and Fig. 5-13(b), the recovered charges and the non-recovered charges were represented to describe the relations between charge trapping and stress time. The recovered charges in the conditions of short stress time revealed the less injection charge under stress. However, a saturation was found to limit the charge de-trapping when stress time over 300 μs because the stress time over 300 μs may induced the extra deep traps that can not respond to the de-trapping time beyond 1 ms. On the other hand, the tendencies of increasing non-recovered charges demonstrated the apparent influences of stress time on charge trapping effect, and further confirmed the existence of extra deep charges with respect to the saturation phenomena in the findings of recovered charges. In Fig. 5-14, the recovery (%) showed a discrete charge de-trapping behavior with the elevated recovery time. A slower recovery rate observed in the more crucial stress conditions (longer stress time) implied the difficulty of recovery charge form deeper energy levels. Moreover, all conditions trended to reach an identical recovery (%) indicated that an universal dynamics is existing to determine the distributive quantity of trapped charges, recovered charges, and residual charges. The mechanism is believed to be associated with the probability of trapped charges dropping into deeper energy levels. This concept can appropriately explain all experimental data in the series of stress time investigations on charge recovery, and connect with the findings in charge trapping behaviors with DC measurements in chapter 3. The influences of recovery voltages on the trapped charges in high-k bulk were also investigated through pulse measurement. Fig. 5-15 showed the great impacts of recovery voltage on recovered charges and non-recovered charges. In Fig. 5-16, the recovery (%) revealed the strong dependence on the charge de-trapping which can be connected with the same concept of available tunneling energy level for recovered charges from high-k bulk back to Si-substrate in chapter 4. For understanding the charge transport mechanism, the temperature dependences on the both charge trapping/de-trapping behaviors were investigated in Fig. 5-17(a) and Fig. 5-17(b), respectively. Low activation energy (E_a) were observed to show the less dependence on temperature and the apparent evidences firmly demonstrate the charge tunneling to be the predominance in both charge trapping/de-trapping behaviors. In Fig. 5-18, the recovery (%) showed that the recovery voltages mainly dominated the charge de-trapping which is relevant to the charge tunneling probability determined by the available energy levels thus the resultant is in spite of the crucial temperature conditions.

5.3.3 The Impacts of AC stress on PBTI Degradation in High-κ Gate Dielectrics

Semiconductor devices are often operated under the AC conditions, thus the impacts of AC stress on the BTI degradation in high-κ gate dielectrics should be concerned with significant charge trapping/de-trapping effects. In our studies, the schematic input waveforms of DC mode and AC mode the pulse measurements were illustrated in Fig. 5-19. The comparisons between DC and AC behaviors in the charge trapping/de-trapping under various stress voltages were revealed through the trapped charges and the residual charges in Fig. 5-20(a) and Fig. 5-20(b), respectively. The experimental results demonstrated the slight impacts of AC stress on the PBTI degradation in the consistence with the other works [22-25]. The small quantity of trapped charges explained the apparent influences of input wave forms (or in the aspect of AC signal with a recovery level) on the charge trapping and reasonably had the slight residual charges. In Fig. 5-21, both DC and AC showed the identical recovery (%) under various stress voltages which is consistent with the previous results in Fig. 5-11. In addition, the charge trapping behavior expressed by the AC/DC ratio [defined as (Charge trapping in AC mode)/(Charge trapping in AC mode)] as a function of linear relation in Fig. 5-22. This resultant pointed out more significant charge trapping at higher stress voltage once again, and further demonstrated the apparent influences on the switch of AC to DC that we should pay more attentions to the application of high-κ gate dielectrics on device operation. Furthermore, the AC frequency dependence was also investigated to further confirm its impact on device reliability. In Fig. 5-23, the AC frequency was investigated through the pulse measurements with the specific simulation of 5 pulse periods with respect to each related AC frequency to demonstrate the impacts of charge trapping/de-tapping on the AC operation. In Fig. 5-24, the results of trapped charges, recovered charges, and residual charges presented the obvious PBTI degradation at lower frequency while a critical respondence of charge recovery was found to be close f = 1 M Hz in Fig. 5-25. The tendencies of recovery (%) apparently indicated a time limitation of distinguishable charge de-trapping behavior, and the elevated pulse periods firmly demonstrated the influences of AC frequency on the PBTI degradation in high-κ gate dielectrics.

5.4 Summary

In our studies, we have systematically analyzed the fast transient charge trapping/de-trapping behaviors in nMOSFETs with HfO_2/SiO_2 gate stack through the pulse measurements. The pulse technique is demonstrated to be necessary to effectively analyze the significant charge trapping/de-trapping phenomena in high-κ gate dielectrics with the considerations of fast transient behaviors. The electrical characteristics were systematically investigated on the aspects of stress voltage, stress time, and recovery voltage. The established physical mechanisms are consistent with those previous results in DC measurements. A Power Law behavior indicated the strong dependence of stress voltage on charge trapping, and a logarithmic behavior revealed the stress time dependence to be associated with the charge tunneling behaviors and the related trap distribution in high-κ gate dielectrics. Besides, the dominant recovery voltage in charge de-trapping behavior is considered to be referred to the concept of available tunneling energy levels for those recovered charge tunneled back to Si-substrate in the consistence with DC results in chapter 4. On the other hand, lower activation energy extracted form the temperature dependence demonstrated the charge tunneling is the predominance for both charge trapping/de-trapping dynamics. Finally, the experimental results firmly demonstrated that AC stress indeed apparently affected the PBTI degradation due to the distinct respondences of charge trapping/de-trapping to the DC and AC modes in the stages on input waveform and AC frequency. The AC/DC ratio pointed out the critical concerns of charge trapping in high-κ gate dielectrics on device operations switched between AC and DC modes. Besides, a critical respondence of charge recovery was found to be close f = 1 M Hz apparently indicated a time limitation of distinguishable charge de-trapping behavior in high-κ gate dielectrics.

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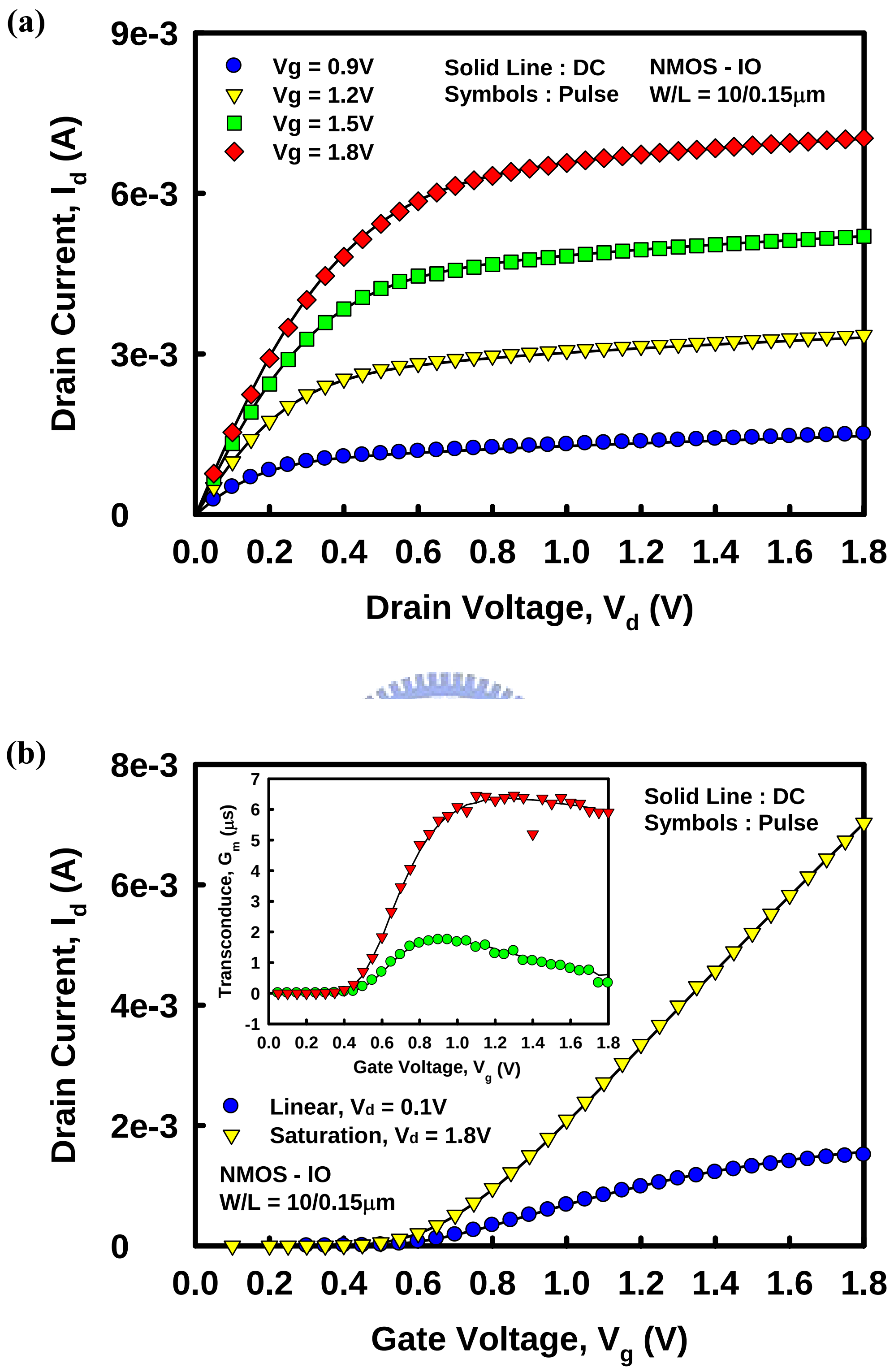

Fig. 5-1 The charge trapping investigations analyzed in the nMOSFETs with SiO_2 gate dielectrics through the comparisons of DC measurement and pulse measurement (a) Driving current characteristics (b) I_d-V_g and G_m-V_g characteristics. A trapping-free result revealed in the matching of DC and pulse curves.

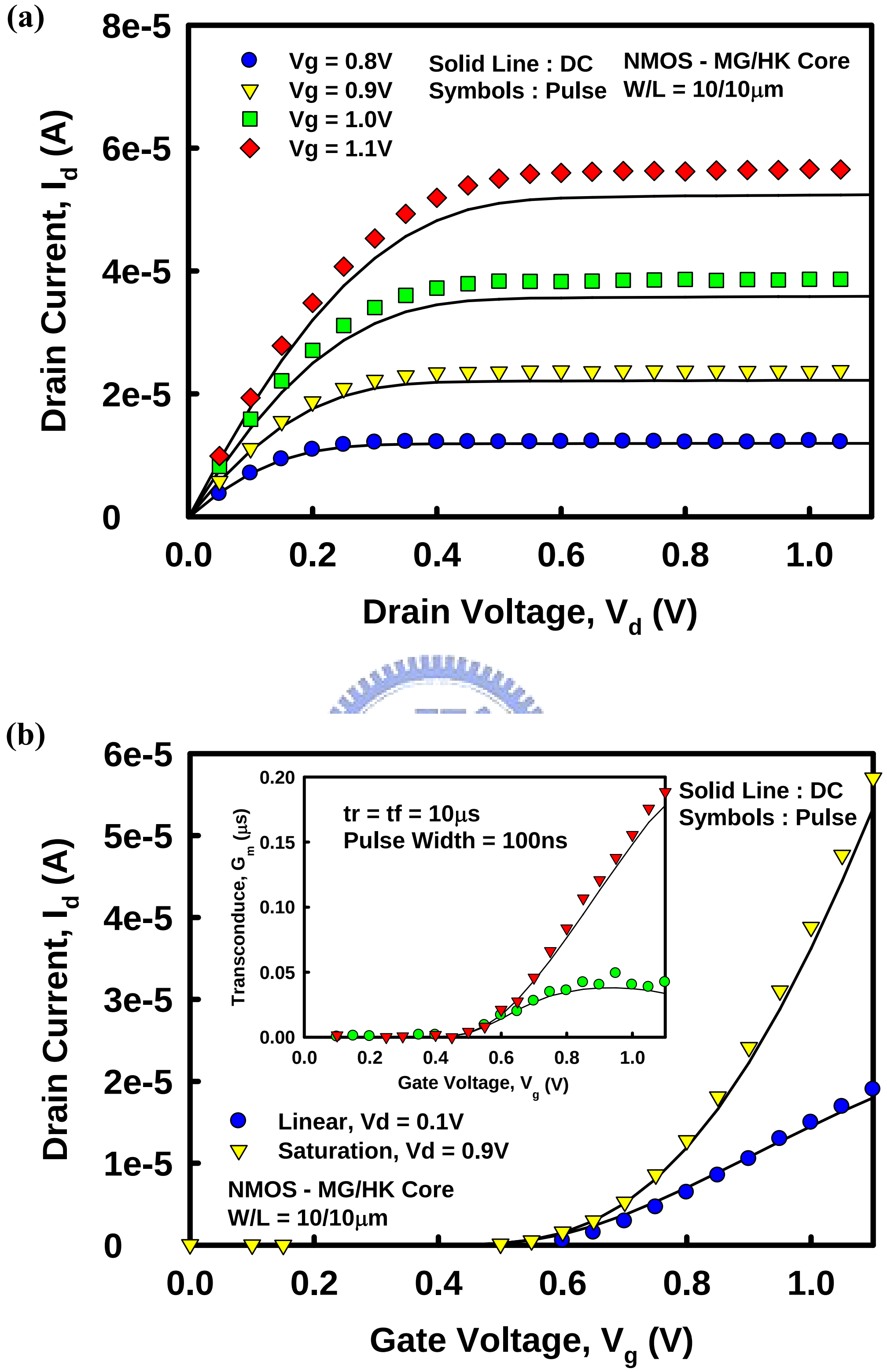

Fig. 5-2 The charge trapping investigations analyzed in the nMOSFETs with high-κ gate dielectrics through the comparisons of DC measurement and pulse measurement (a) Driving current characteristics (b) I_d-V_g and G_m-V_g characteristics. An apparent charge trapping effect revealed in the separation of DC and pulse curves.

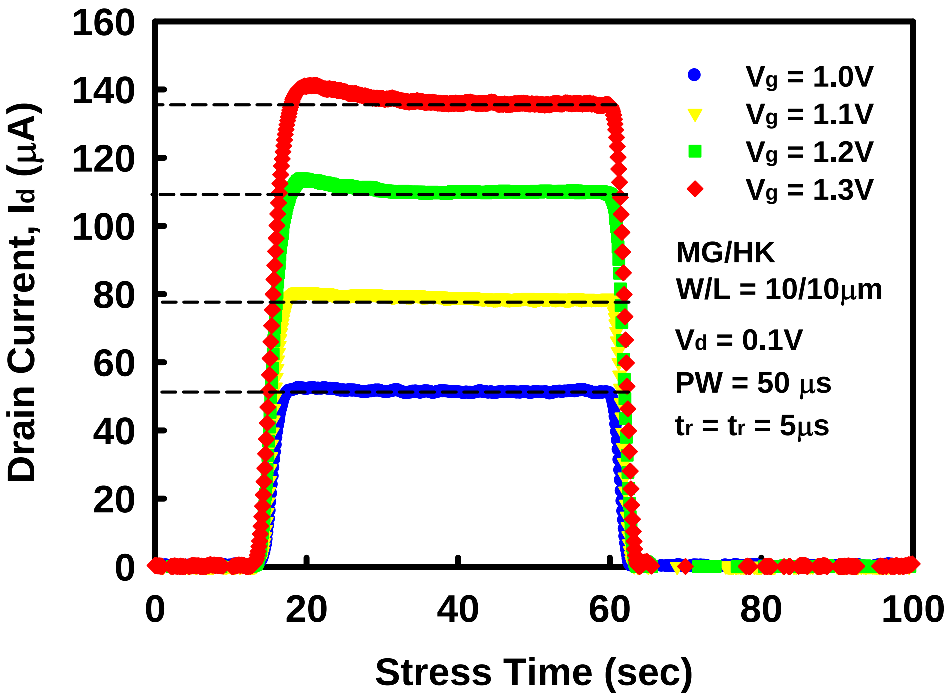

Fig. 5-3 The transient pulse-IV output waveform investigated under various applied gate voltages. The charge trapping becomes more significant with elevated stress voltages.

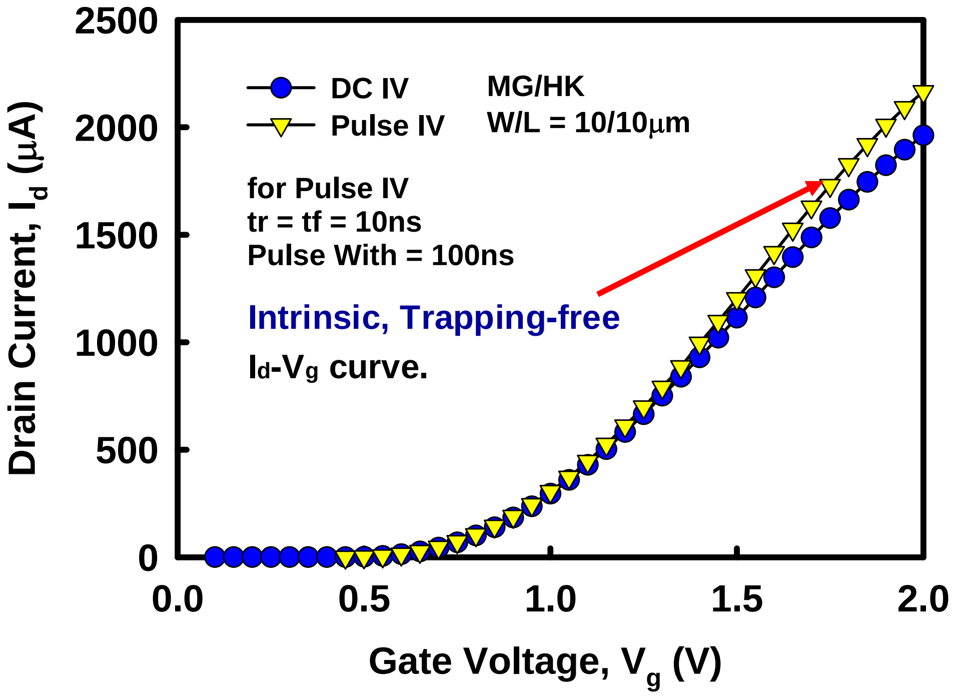

Fig. 5-4 The I_d-V_g characteristics were represented by DC and pulse measurements. The pulse measurements do a real-time monitor avoid the fast transient charge trapping effect.

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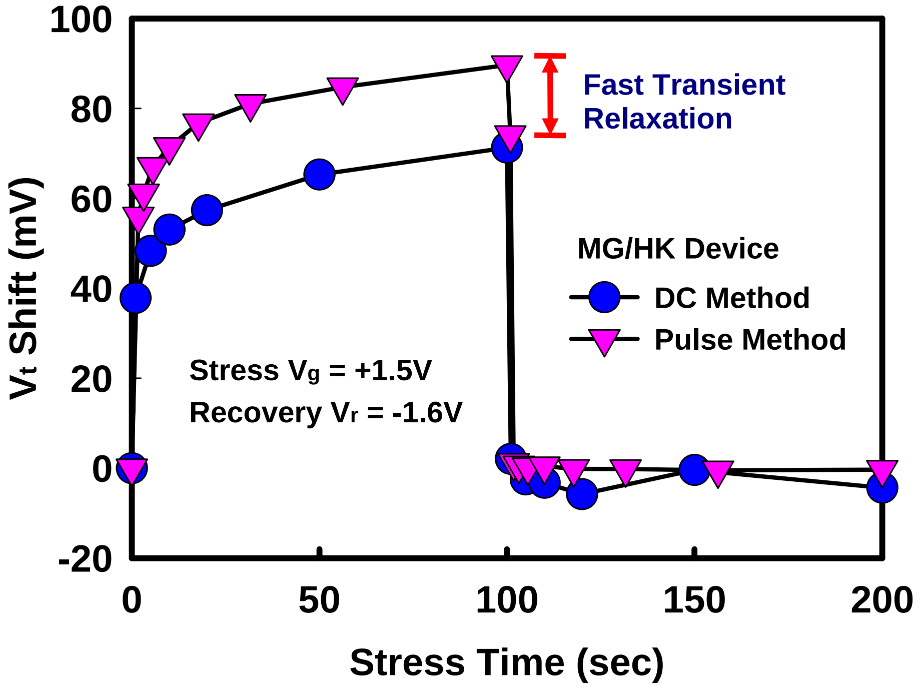

Fig. 5-5 Charge de-trapping during the PBTI degradation with the DC and pulse measurements. The pulse measurements do a real-time monitor avoid the fast transient charge de-trapping effect.

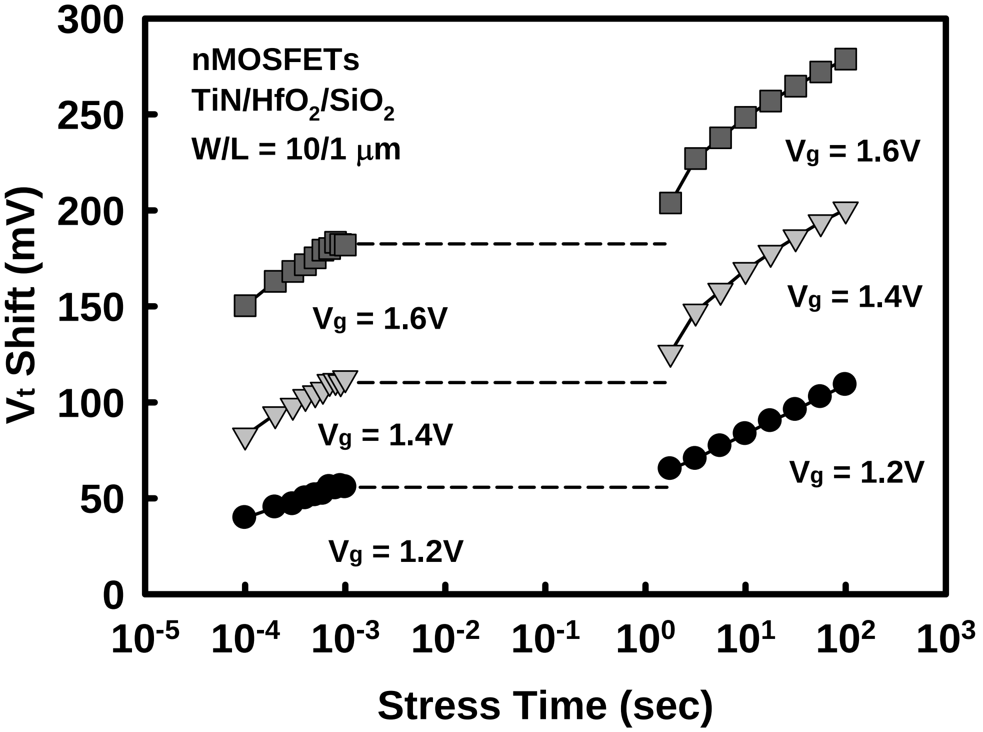

Fig. 5-6 PBTI degradation observed through the pulse measurements and the DC measurements over several decades.

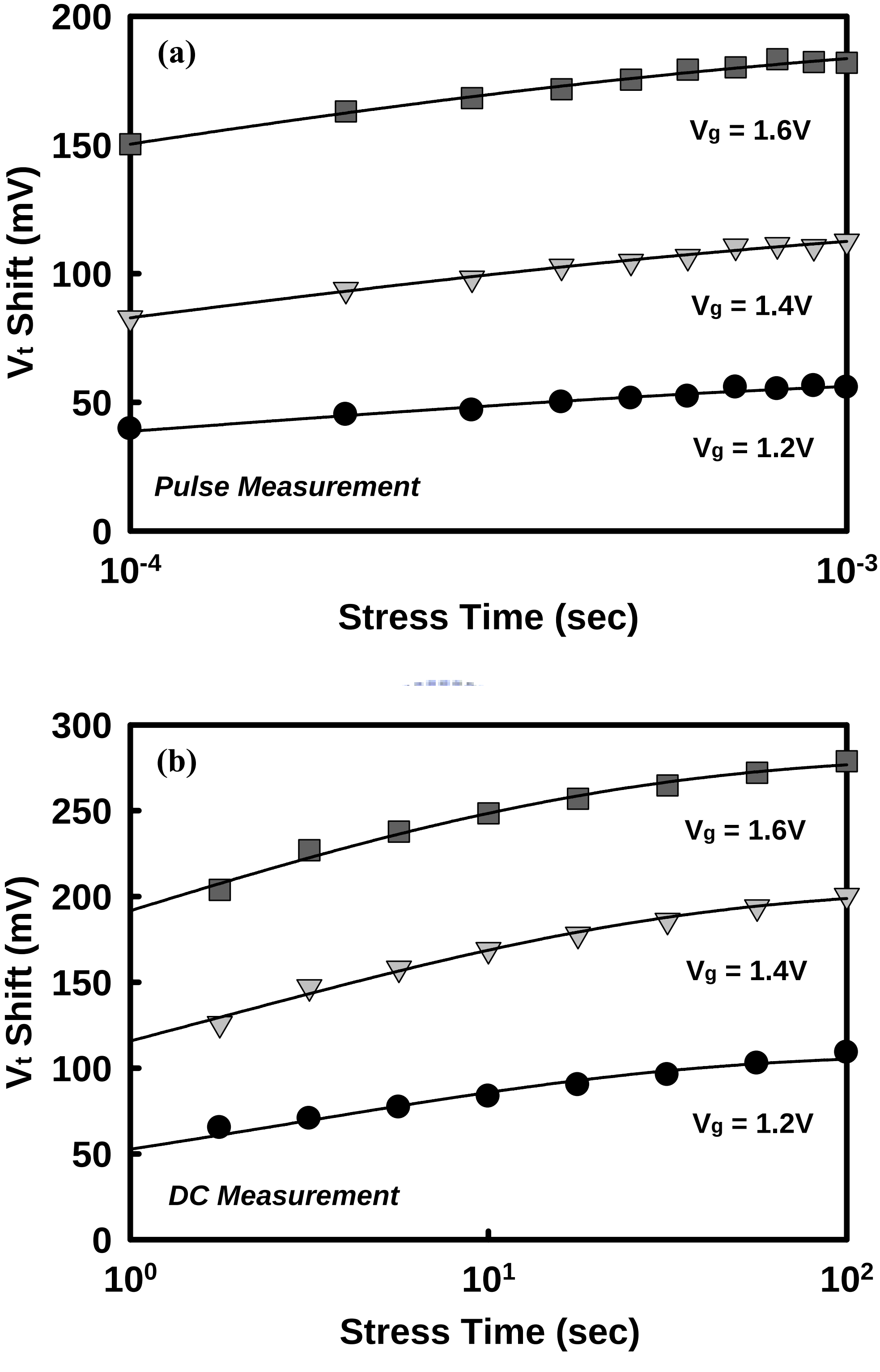

Fig. 5-7 Modeling fitting of charge trapping in HfO_2/SiO_2 gate stack under various stress voltages. (a) Pulse measurement (b) DC measurement.

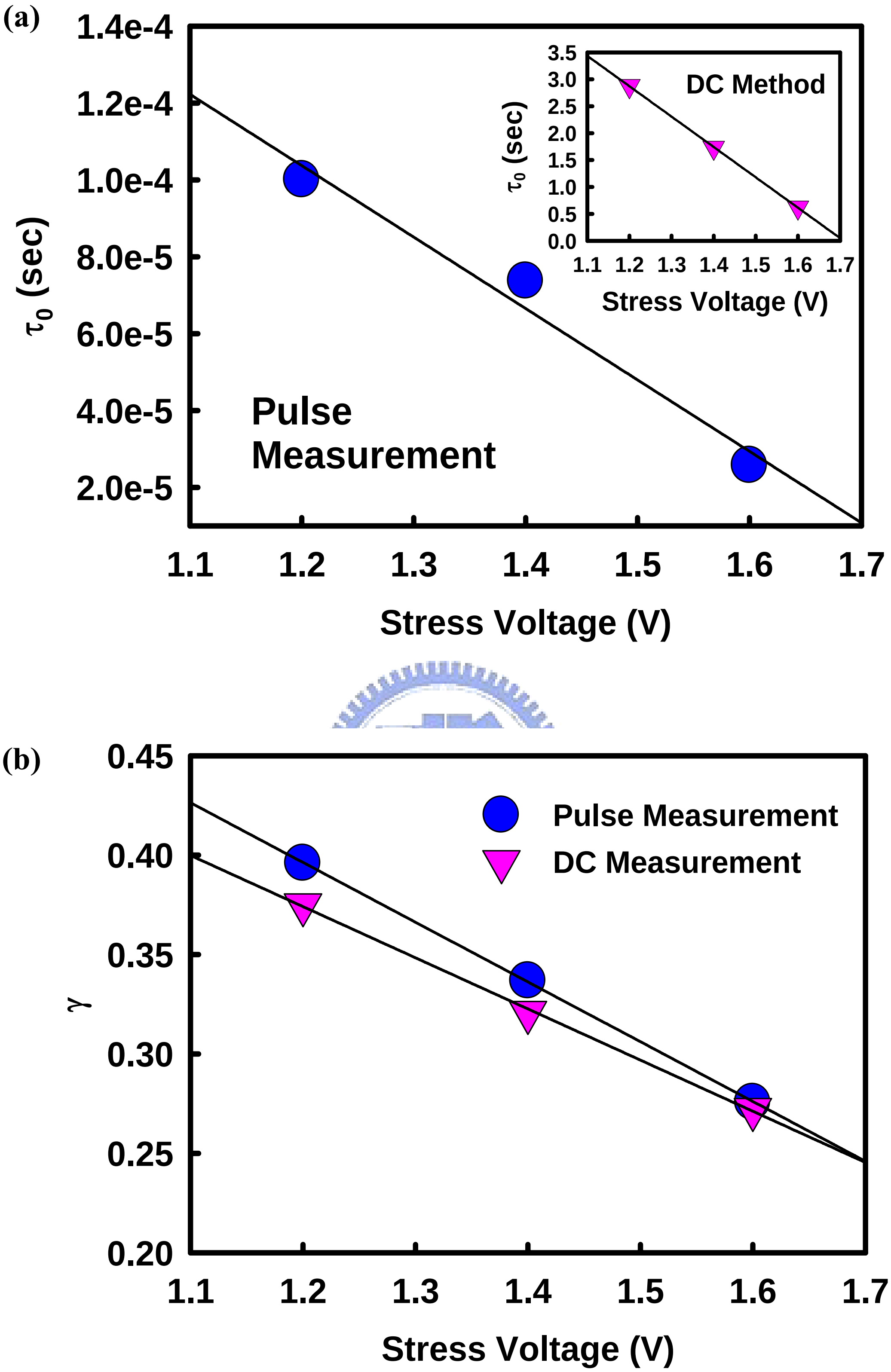

Fig. 5-8 Modeling fitting of charge trapping in HfO_2/SiO_2 gate stack with both pulse and DC measurements under various stress voltages. Fitting parameter (a) Trapping time constant, τ_0 (b) Related trapping distribution, γ.

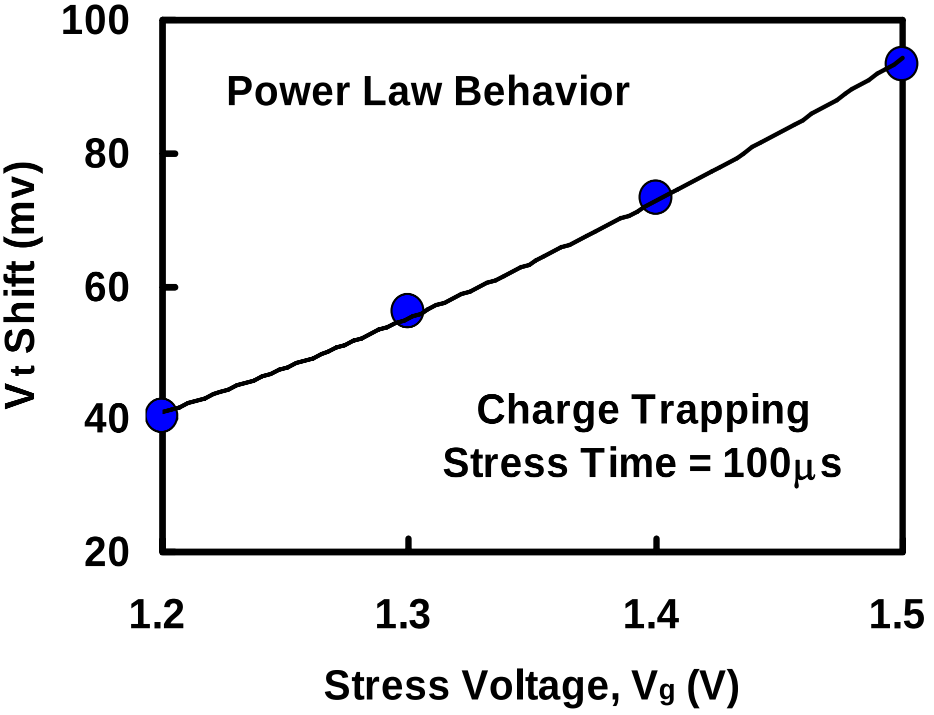

Fig. 5-9 The dependence of stress voltage on charge trapping in high-κ gate dielectrics as a function of Power Law behavior.

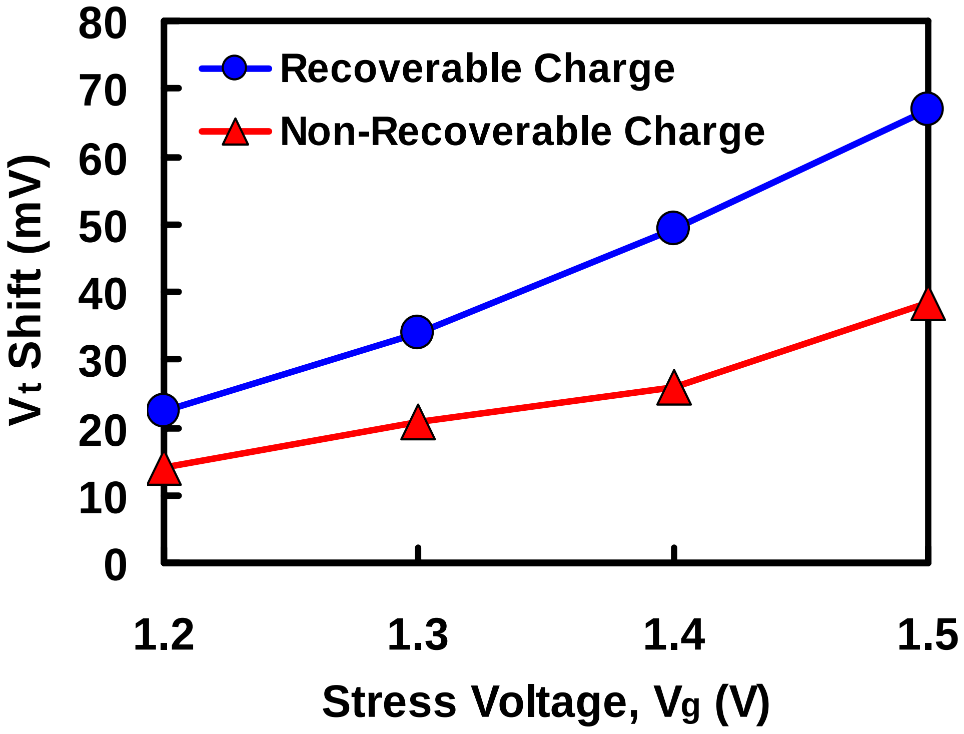

Fig. 5-10 The impacts of stress voltage on recovered charge and non-recovered charge in high-κ gate dielectrics.

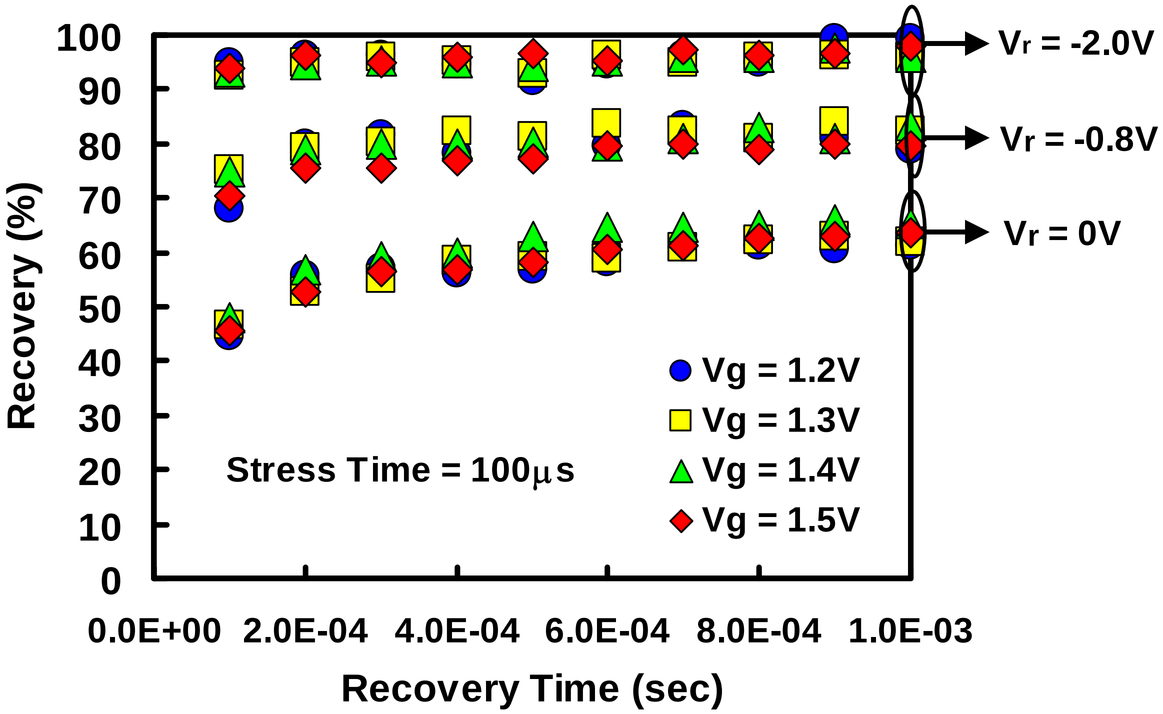

Fig. 5-11 The impacts of stress voltage on the recovery (%) under various recovery voltages.

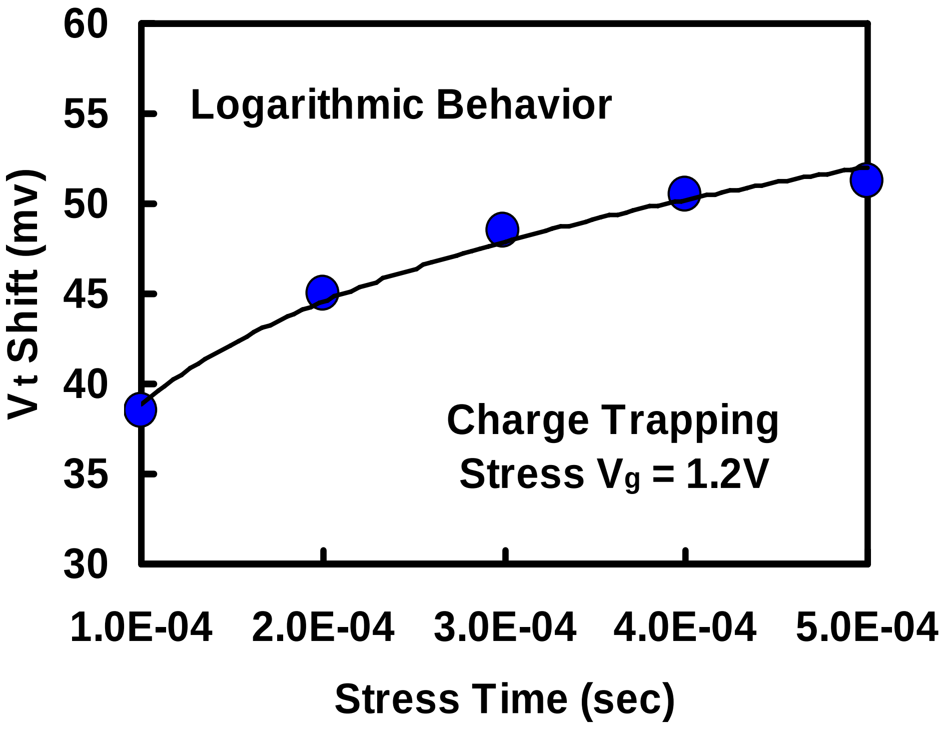

Fig. 5-12 The dependence of stress time on charge trapping in high-κ gate dielectrics as a function of Logarithmic behavior.

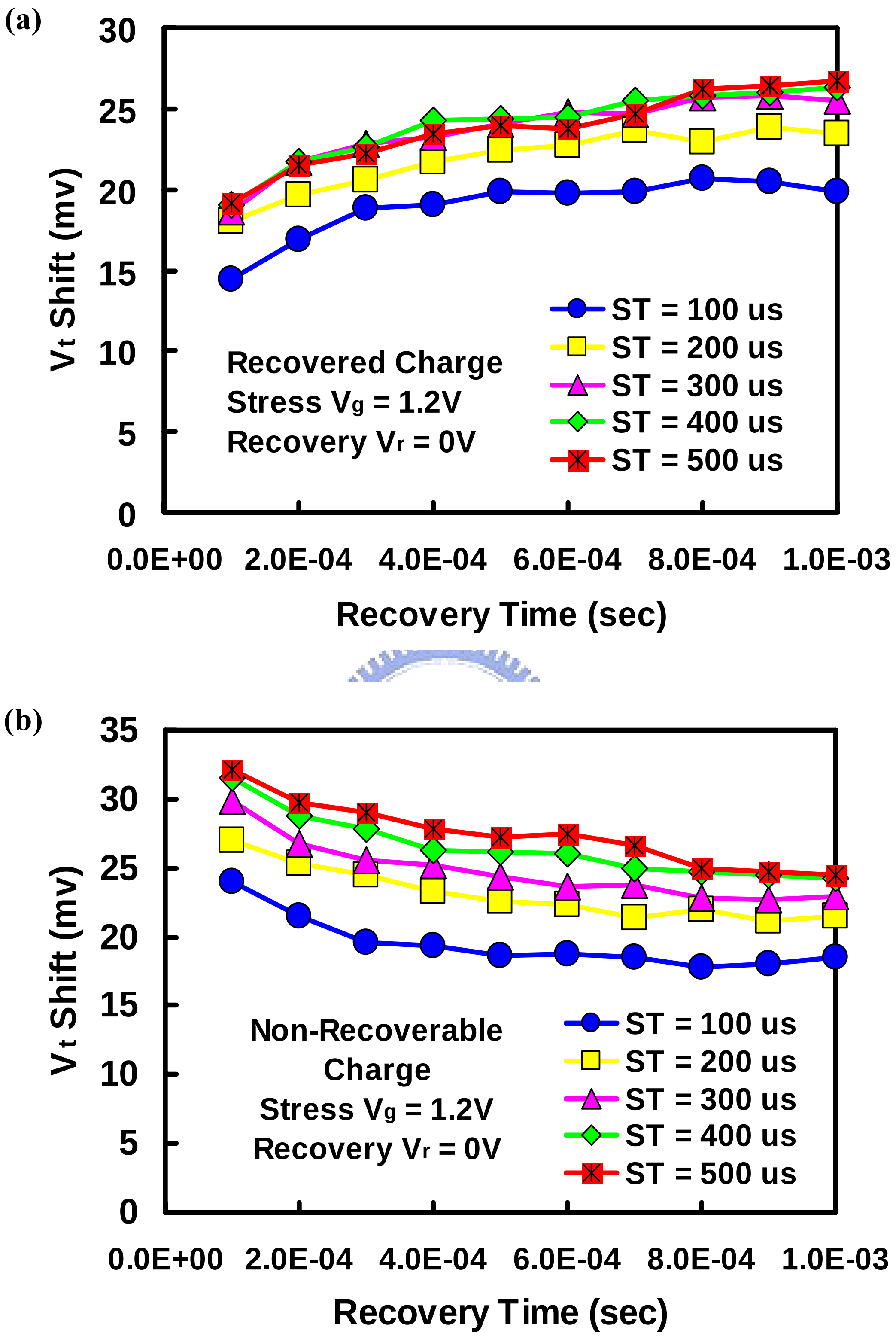

Fig. 5-13 The impacts of stress time on (a) Recovered charge and (b) Non-Recovered charge in high-κ gate dielectrics.

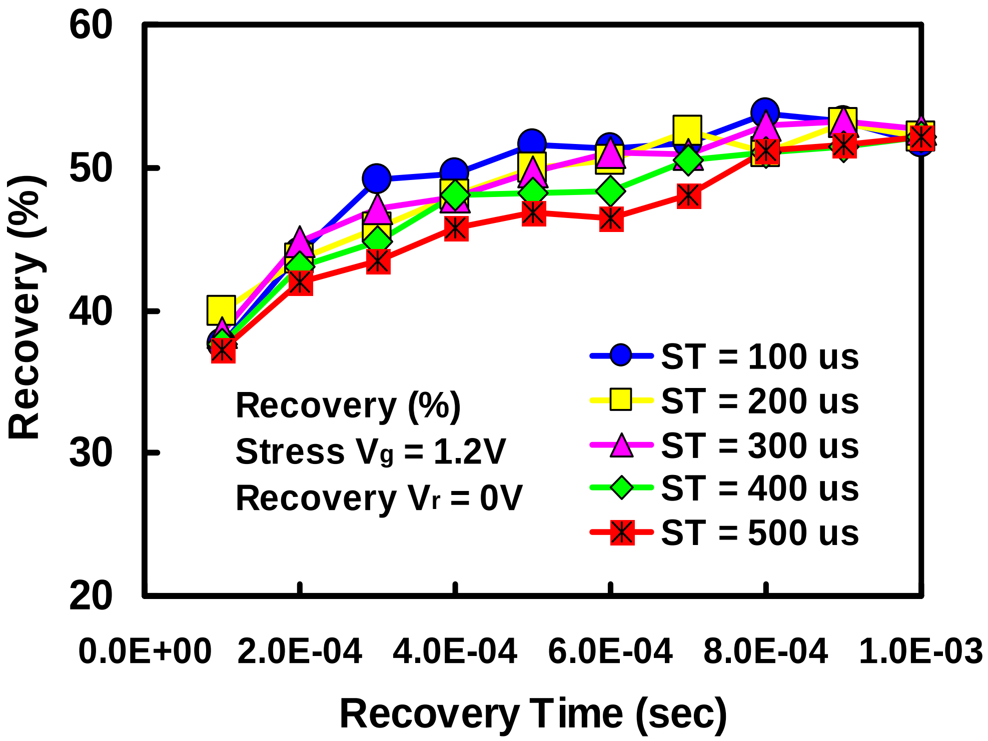

Fig. 5-14 The charge de-trapping behaviors revealed on the recovery (%) under various stress time conditions.

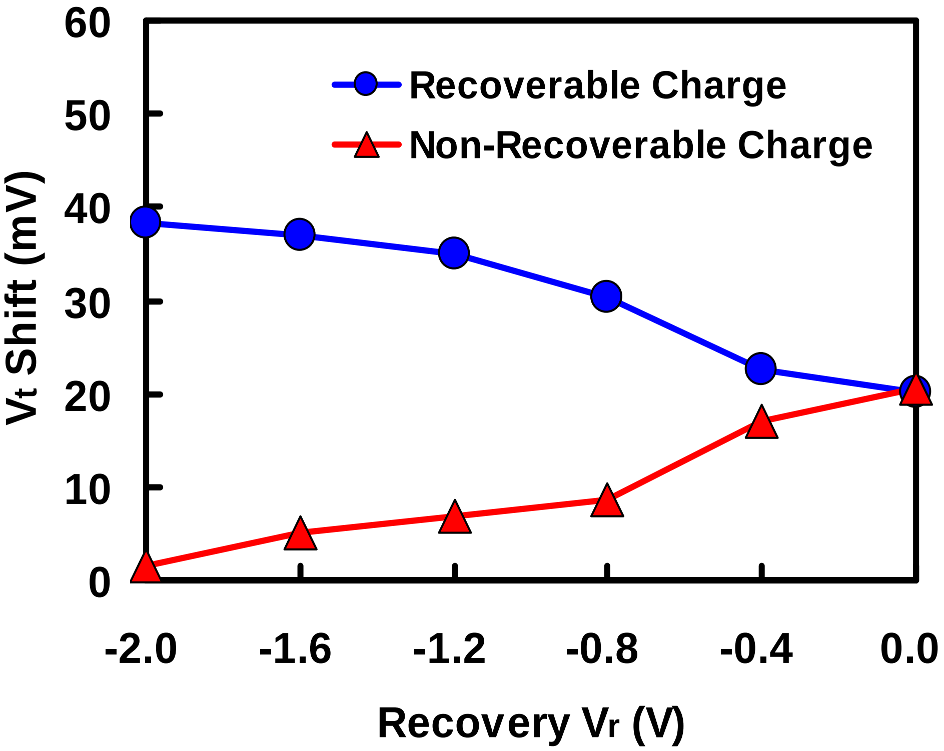

Fig. 5-15 The impacts of recovery voltage on recovered charge and non-recovered charge in high-κ gate dielectrics.

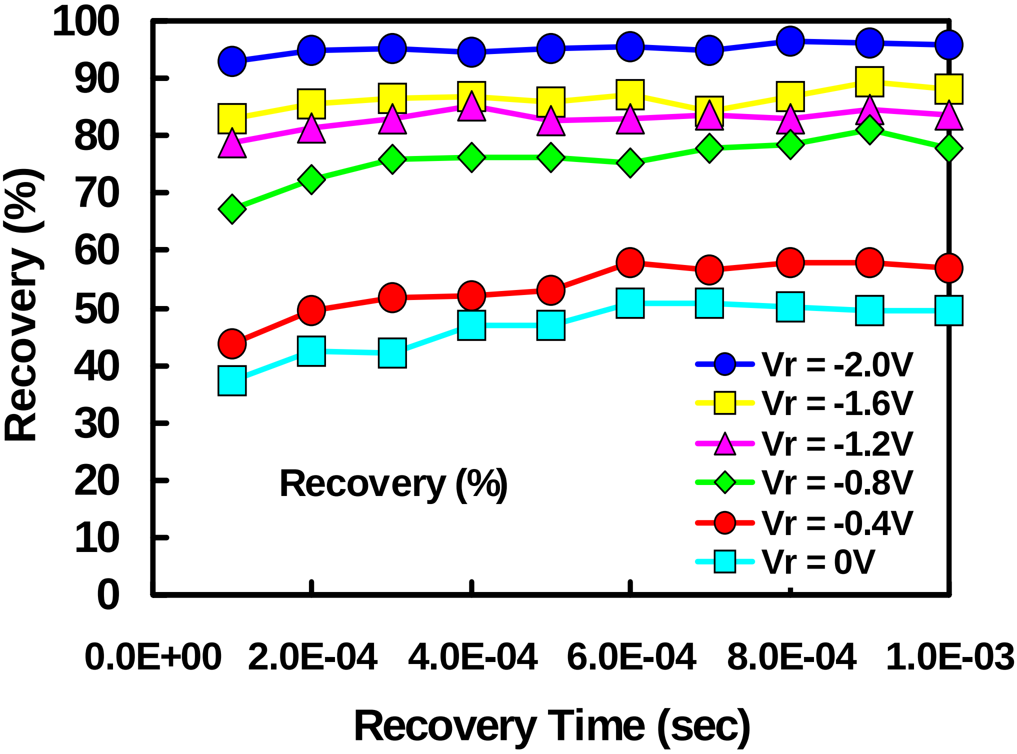

Fig. 5-16 The charge de-trapping behaviors revealed on the recovery (%) under various recovery voltage conditions.

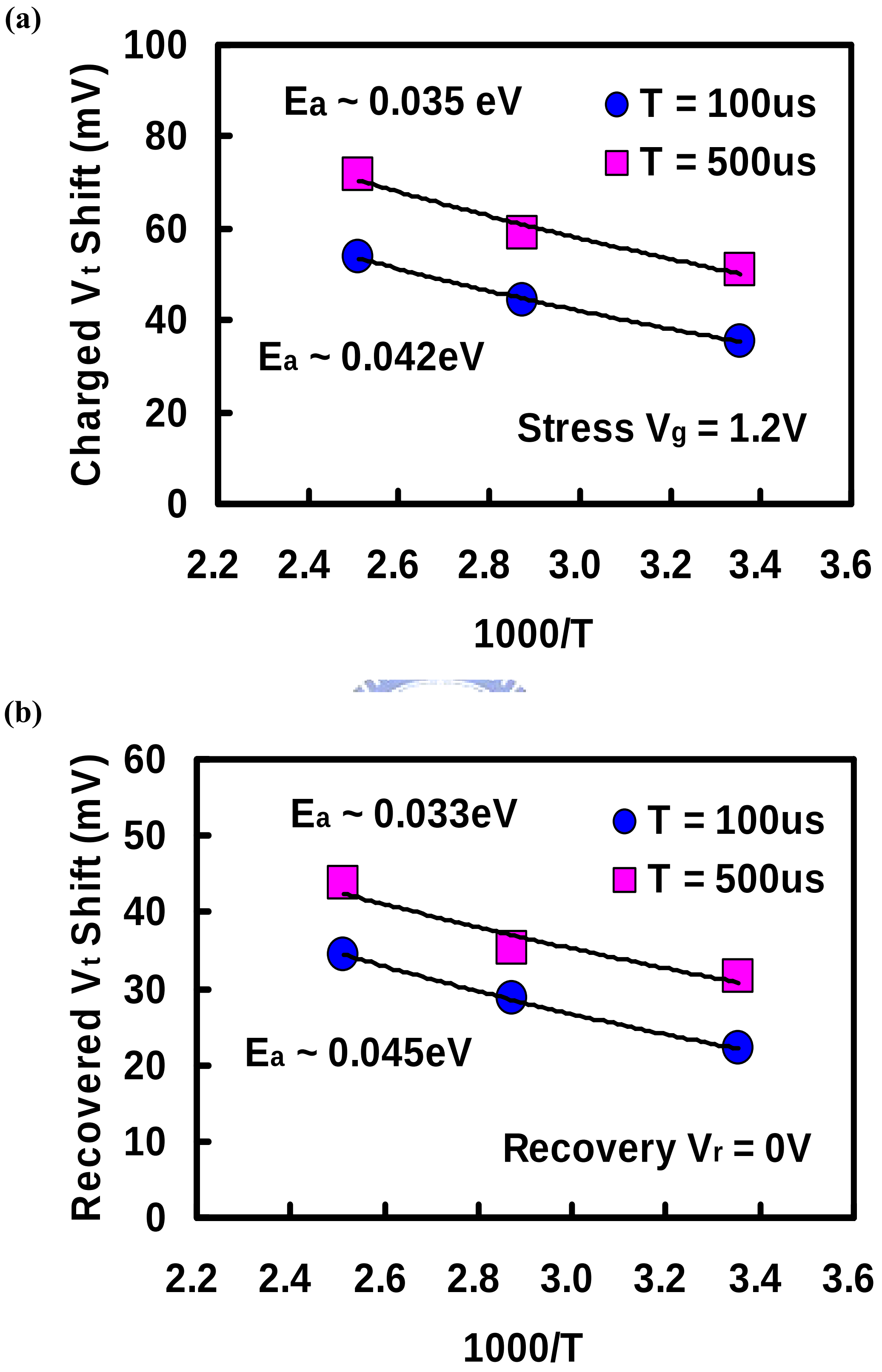

Fig. 5-17 The temperature dependence on charge trapping/de-trapping in high-κ gate dielectrics under various stress conditions (a) Charge trapping (b) Charge de-trapping.

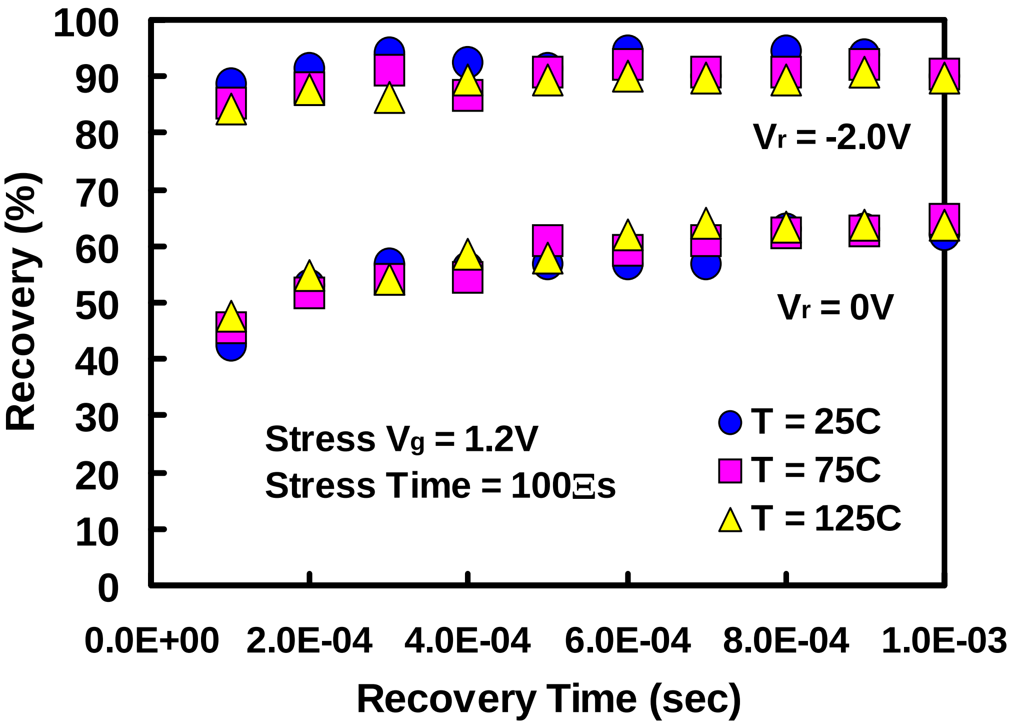

Fig. 5-18 The impacts of temperature on the recovery (%) under various recovery voltages.

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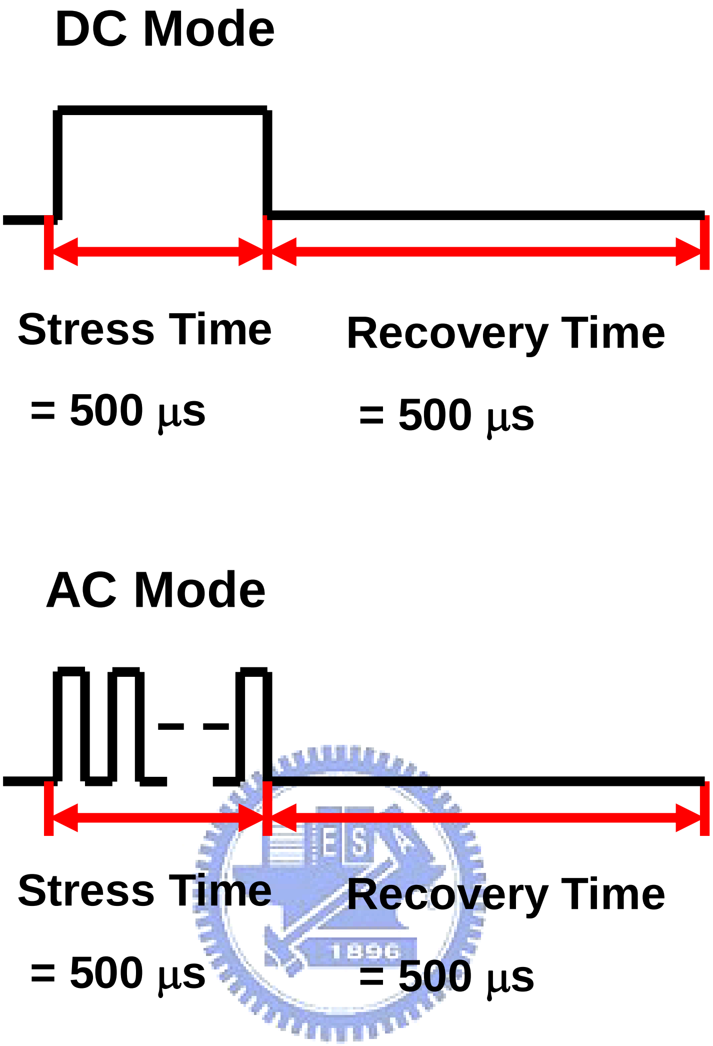

DC Mode
Stress Time
= 500 μs
Recovery Time
= 500 μs
AC Mode
Stress Time
= 500 μs
Recovery Time
= 500 μs

Fig. 5-19 The schematic input waveforms of DC mode and AC mode in the pulse measurements.

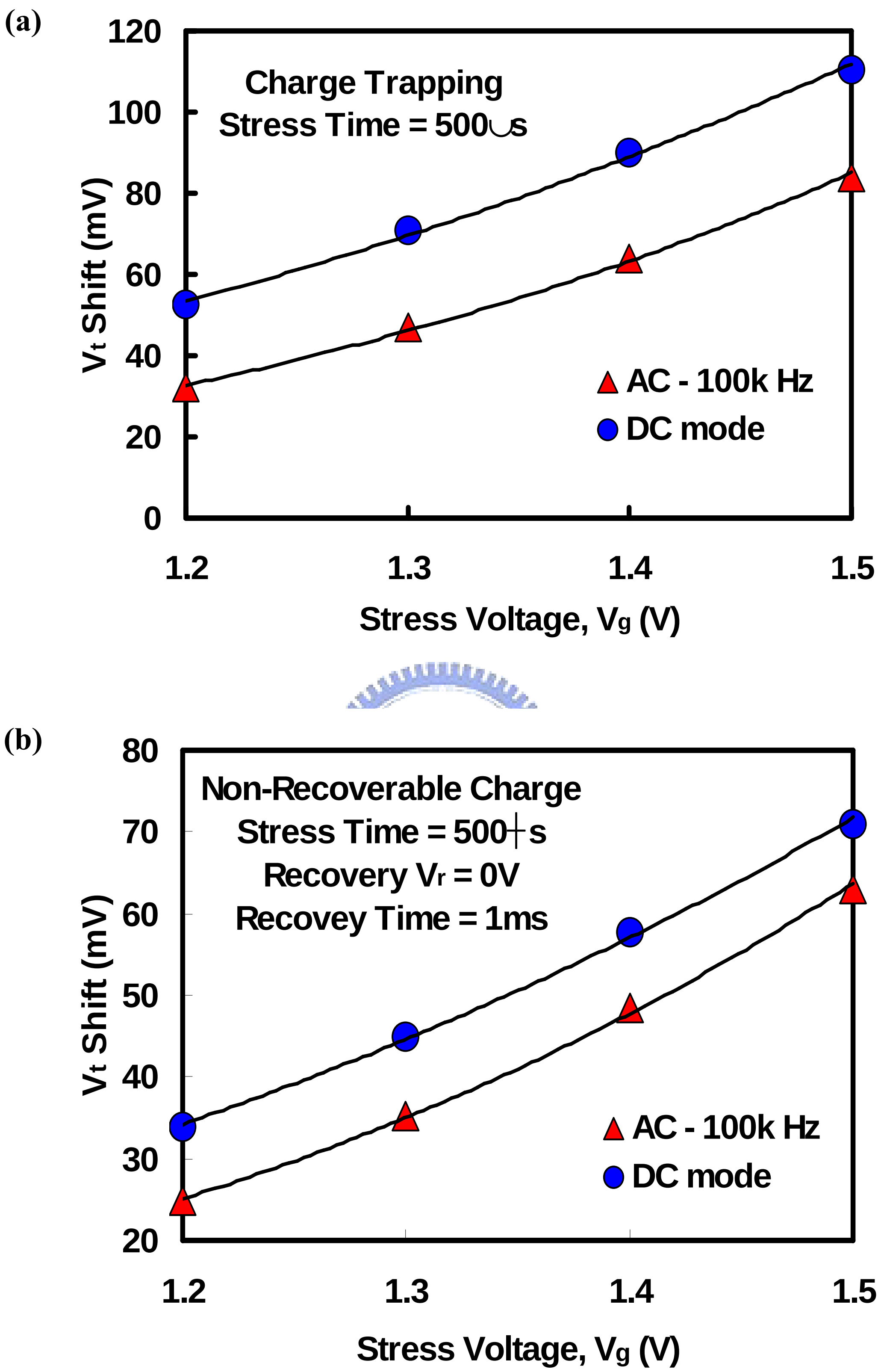


Fig. 5-20 The comparisons between DC and AC behaviors in the charge trapping/de-trapping under various stress voltages. (a) Trapped charges after stress (b) Non-Recovered charges after recovery.

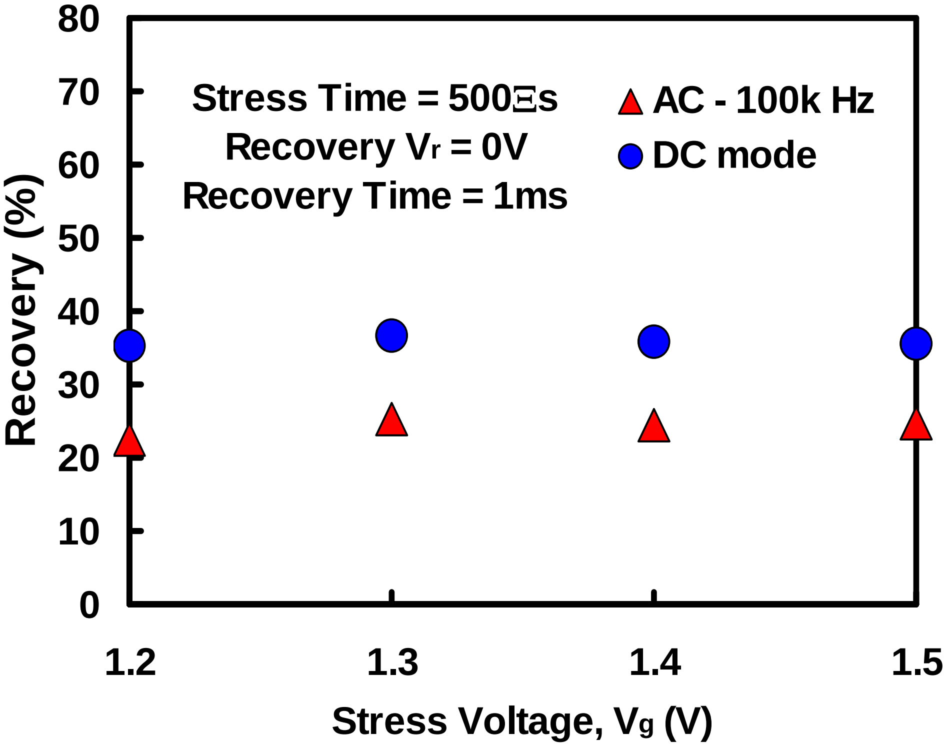


Fig. 5-21 The impacts of DC and AC modes on recovery (%) under various stress voltages.

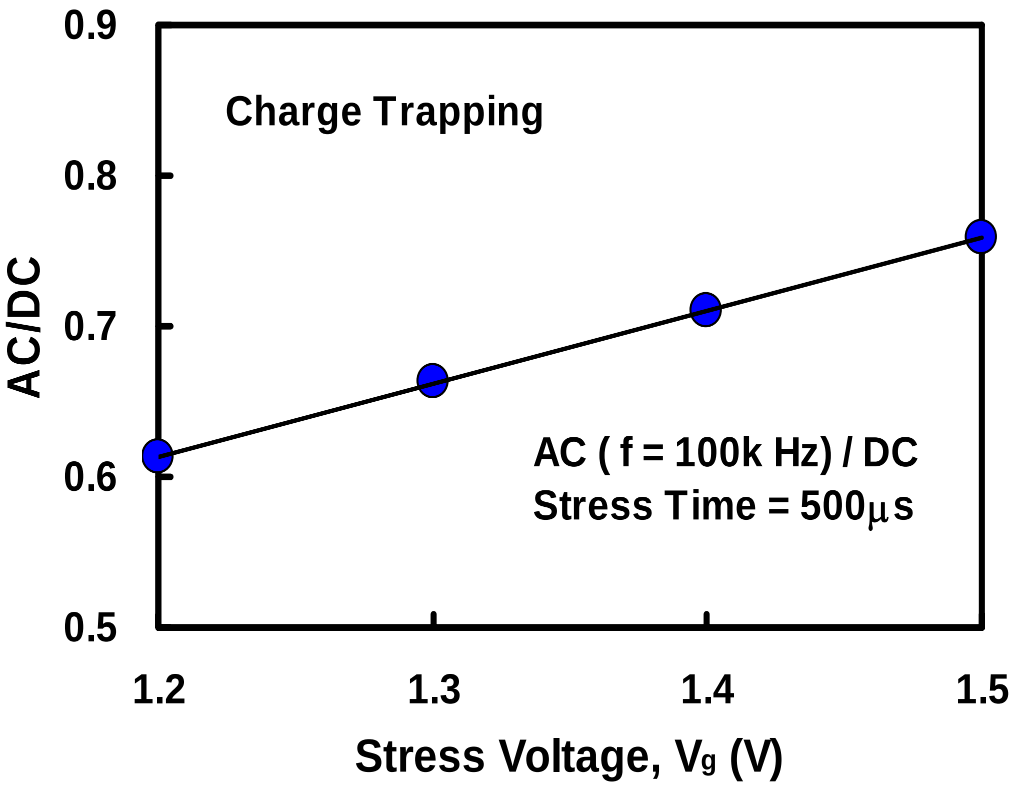
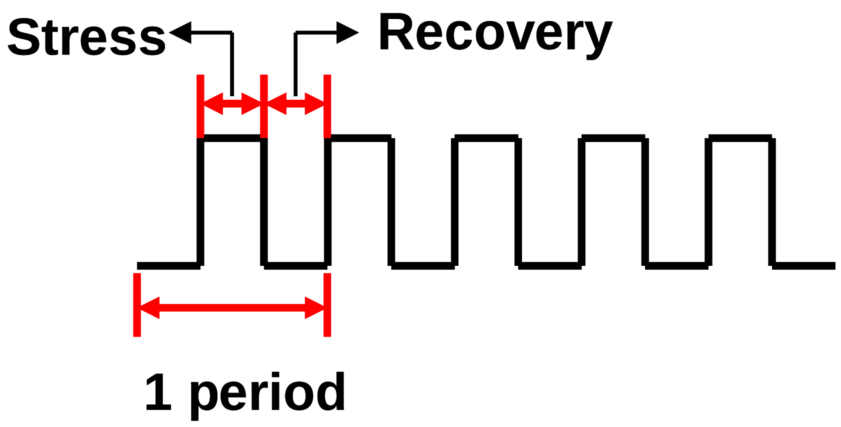


Fig. 5-22 The charge trapping behavior expressed by the AC/DC ratio as a function of linear relation.


Stress
Recovery
1 period

Duty Cycle = 50%

- **Period = 1 μs → f = 1 M Hz**
- **Period = 10 μs → f = 100 k Hz**
- **Period = 100 μs → f = 10 k Hz**
- **Period = 1ms → f = 1 k Hz**

Fig. 5-23 A schematic illustration of AC input waveform and related AC frequency.

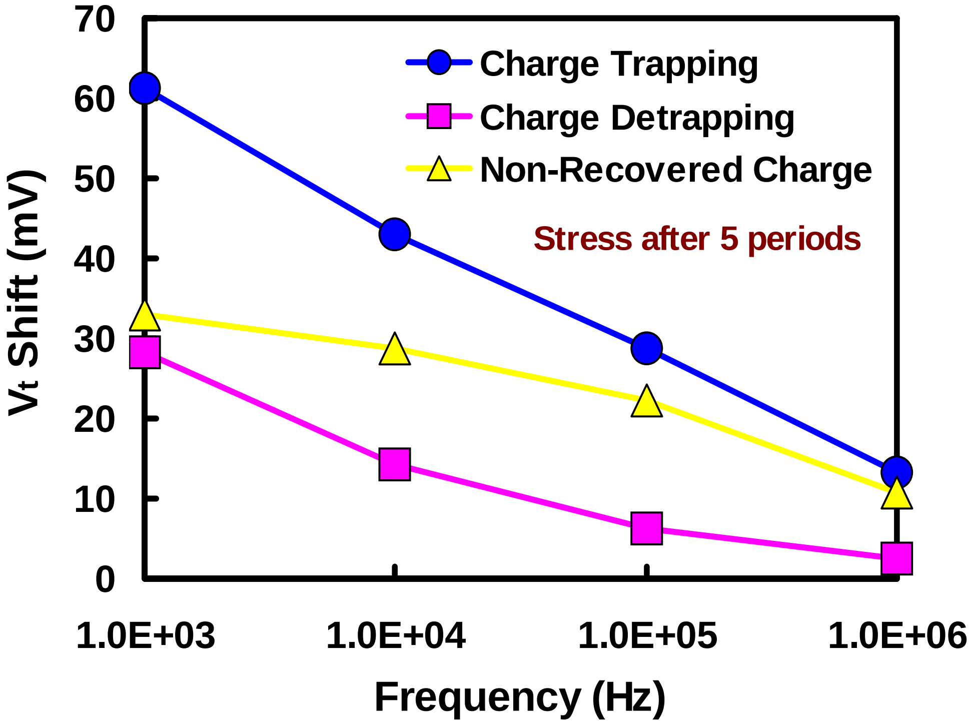


Fig. 5-24 The impacts of AC frequency simulated through the pulse measurements on the trapped charge, recovered charge, and non-recovered charge.

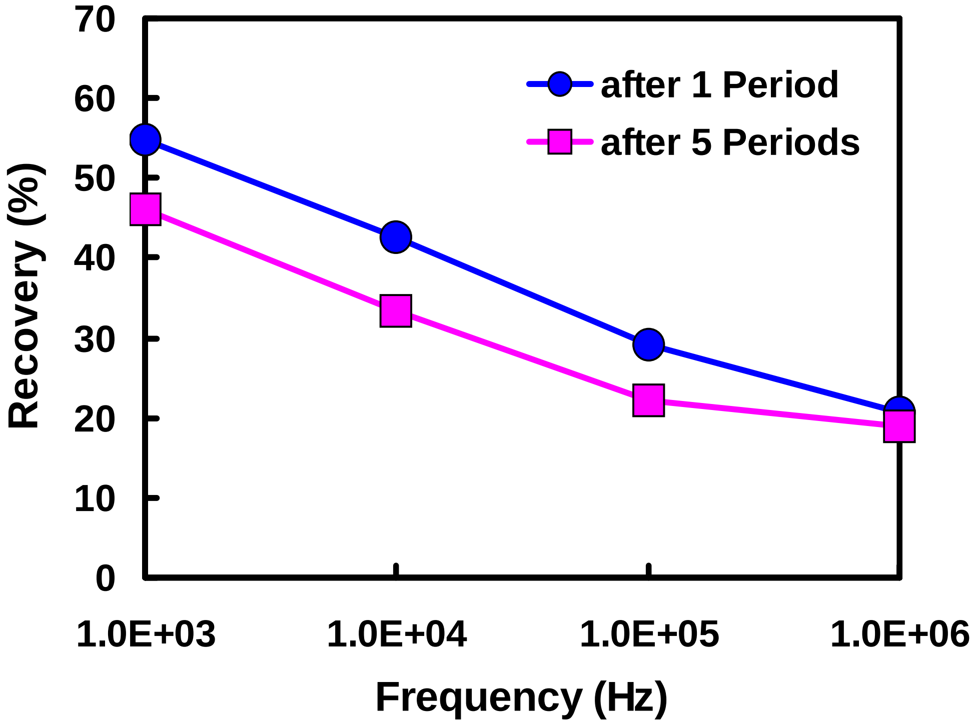


Fig. 5-25 The impacts of AC frequency on charge de-trapping behaviors represented by recovery (%). A de-trapping behavior was limited close to f = 1M Hz.

Chapter 6

Dynamic Positive Bias Temperature Instability Behavior in nMOSFETs with HfO_2/SiO_2 Gate Stack

6.1 Introduction

Significant charge trapping/de-trapping effects are the most urgent problems in the ways of developing the high-κ gate dielectrics to the advanced CMOS technology . In numbers of previous works, the charge trapping/de-trapping behaviors in high-κ gate dielectrics have been extensively investigated on the static bias temperature instability (Static-BTI) to explore the related impacts on device reliability [1-5]. As the previous results in chapter 4, the charge trapping effect would usually induce the non-recoverable charges in the high-κ bulk which are considered to apparently influence the electrical characteristics and device operations [6-9]. In numbers of related researches, the exist of residual charges is considered as the unsymmetry between charge trapping and charge de-trapping behaviors associated with the distinct time constants and related band diagrams [10-11]. As other reports, it has also claimed to be the origin of deeper level traps in high-κ gate dielectrics [8, 12-13]. Generally, the devices actually operate under a dynamic condition as often, not keep the static state as always. In some investigations on conventional SiO_2, the degraded tendency of dynamic bias temperature instability (dynamic BTI) is considered to be the contribution of the extra trap generation (SiO_2/Si interface, or high-k/poly-Si gate interface) during the stress process [14-17]. Although the bias temperature instability in high-κ gate dielectrics is different in SiO_2, the repetitions of charge trapping/de-trapping sequences which may cause more and more significant threshold voltage shift should be carefully concerned. Moreover, some experimental findings in high-κ investigations showed the non-increasing trapped charges during the dynamic BTI degradation when devices were with an appropriated recovery voltage [11, 18-19]. The reproducible evidences are believed to be much close to the aspect of the charge filling to the existing empty traps in the high-κ bulk and the successful charge recovering under a sufficient recovery force [20]. In order to clarify the authentic mechanism of the dynamic BTI degradation in high-κ gate dielectrics, numbers of related investigations including the dependences of stress voltage, recovery voltage, recovery time, and temperature have been conducted systematically through both DC and pulse measurements with the considerations of fast transient behaviors. Finally, we have established a related physical model to reasonably explain the actual mechanism of DPBTI behaviors, and further realize the impacts of residual charges on the DPBTI degradation.

6.2 Experimental Procedures

In this study, nMOSFETs were fabricated on (100) p-type Si wafers. After a standard RCA cleaning with a final HF-dip, a 0.8 nm based oxide SiO_2 was thermally grown to be thin interfacial layer. A 3.2 nm HfO_2 layer was deposited by ALD system, followed a high temperature post deposition annealing (PDA) to optimize the film quality. Finally, a metal gate with workfunction (Φ_B) = 4.2 eV was conducted by PVD technique to perform the gate stack, then the following stand CMOS process were implemented to complete the total device fabrication. The electrical characteristics were investigated through the techniques of keithley Model 4200-SCS semiconductor characterization system and keithley pulse IV measurement.

6.3 Results and Discussions

6.3.1 Dynamic PBTI in DC Measurements

In this study, the DC measurements were adopted to observe the DPBTI phenomena, firstly. In Fig. 6-1(a), the DPBTI was investigated on the nMOSFETs with the HfO_2/SiO_2 gate stack under various stress voltages. The V_r = -2.0V was took as a sufficient recovery force to eliminate the trapped charges from the high-κ bulk as completely as possible. From the experimental results, the charge trapping/de-trapping can be reproducible with the negligible residual charges in the condition of stress V_g = 1.2V and recovery V_r = -2.0V. The results demonstrated the assumption of the charges just filling the pre-existing trap centers in the high-κ bulk on the stress stage, and successful recovering out of the trapped sites in the recovery process without the time elevated trap generation. However, the residual charges gradually enhanced with the elevated stress voltage even though the trapped charges did not obviously increase at each stress condition. In Fig. 6-1(a), the invariant fast/total trapping ratio [defined as the ratio of (fast trapping)/(total trapping), discussed in chapter 3] revealed the identical charge trapping behavior in each stress sequence. In addition, the results also implied the reproducible phenomenon of charge filling in the pre-existing traps centers, and denied the consideration of additional trapping generation. In Fig. 6-2(a), the DPBTI was also studied on the stages of various recovery voltages with a stress voltage = 1.2V. Almost full recovery was achieved at the recovery voltage = -2.0V. However, the threshold voltage shift became more significant referred to the increase of residual charges once the recovery voltage could not provide the capability of charge de-trapping. Fig. 6-2(a) showed the fast/total de-trapping ratio [defined as the ratio of (fast de-trapping)/(total de-trapping), discussed in chapter 4]. The constant magnitude of the recovered charges in each recovery sequence implied that the elevation of threshold voltage shift was mainly according to the accumulation of residual charges. Besides, the increasing charge trapping during the DPBTI was considered as the slow trap generation in the consistence with the same concept of electrons dropping into a deeper trapping level with the elevated stress time. The charge filling model is still regarded as reasonable to describe the DPBTI degradation because the threshold voltage can be forced to return the original value with a sufficient recovery force (or longer recovery time in progress) with respect to the non-extra damage in high-κ gate dielectrics.

6.3.2 Dynamic PBTI in Pulse Measurements

For the further considerations of fast transient behaviors, the DPBTI degradations were also studied carefully through the pulse measurements (defined as Fast-DPBTI compared with the DPBTI in DC measurements). The stress/recovery time are defined as 100μs/100μs for a dynamic stress sequences, and the raising/falling time of the pulse voltage both are 0.1μs in order to prevent form the occurrence of the fast transient charging and discharging in the raising time and falling time, respectively. In Fig. 6-3, the recovered-threshold voltage shift was apparent independence of stress time to demonstrate the reproducible charge trapping/de-trapping behaviors in HfO_2/SiO_2 gate stack under such stress conditions (stress Vg = 1.2V, stress/recovery time = 100μs). The identical quantity of both trapped-threshold voltage shift (at the same stress V_g) and recovered-threshold voltage shift implied the charge filling model and further implied the impacts of residual charges in the consistence with DC results in Fig. 6-2. In Fig. 6-4, lower activation energy (E_a) extracted form the temperature dependence in the Fast-DPBTI degradation strongly confirmed the fast transient charge de-trapping behavior to be the tunneling mechanism under various recovery voltages. In the aspect of non-recoverable charges, the residual-threshold voltage shift was represented in Fig.

6-5. The experimental results provided the powerful evidences to exhibit the accumulation of residual charges during the Fast-DPBTI degradation once the recovery force is not sufficient to completely remove the trapped charges in high-κ gate dielectrics. On the other hand, the temperature dependence also revealed the slight increase of residual charges and recovered charges (in Fig. 6-4). The results are assumed that higher temperature enhanced the trap-assisted conduction mechanisms (^{ex} Frenkel-Poole emission, Trap Assist Tunneling) in high-κ gate dielectrics to result in the elevations of both charge trapping/de-trapping, thus the more significant residual charges and recovered charges were observed in Fig. 6-6 and Fig. 6-4, respectively. The further evidences were also apparently represented in Fig. 6-7. The trap-assisted conduction mechanisms were activated under the elevated temperature to enhance the accumulation of residual charges even though an almost full recovery can be achieved at room temperature under V_r = -2.0V. In addition, the more significant results were verified to occur under lower recovery voltage which is worse than the conditions of the crucial temperatures (75℃, 125℃), and the results also demonstrated the predominance of recovery voltage in the Fast-DPBTI degradation. In Fig. 6-8, the temperature assisted Fast-DPBTI degradations were also verified once again in the recovery (%) under a large recovery force (V_r = -2.0V). Furthermore, the less temperature dependence of recovery (%) found under a low recover voltage is referred to the predominance of recovery voltage although the temperature effect is apparent. The related physical model has been established to explain the influences of elevated temperatures on the charge trapping/de-trapping behaviors during the Fast-DPBTI degradation in Fig. 6-9. In the aspect of stress voltage, the impacts of the quantity of injection charges on the Fast-DPBTI degradation were carefully investigated as well. Fig. 6-10(a) and Fig. 6-10(b) showed the impacts of stress voltage (V_g) on the charge trapping/de-trapping behaviors during DPBTI degradation under various recovery voltages. The impacts of stress voltage are more distinguishable under larger recovery force (V_r = -2.0V), and the significant quantity of recovered charges is associated with the great number of injection charges at beginning of more crucial stress. However, the recovery efficiency is quite low under V_r = 0V to induce less recognition between stress V_g = 1.4V and 1.5V. On the other hand, from the viewpoint of trapped charges in Fig. 6-10(b), both stress V_g = 1.4V and 1.5V showed the identical behaviors of logarithmic tendencies of charge trapping under V_r = 0V and liner relation under V_r = -2.0V to implied accumulation of residual charges and the almost full recovery in each sequence. As the results, the influences of stress voltage are not as great as recovery voltage in the Fast-DPBTI degradation. In Fig. 6-11, the recovery (%) presented an apparent independence of stress voltages that is consistent with the pulse results observed in the static PBTI degradation in Fig. 5-11. The explanations is similar to the previous conclusion in chapter 5 which is with respect to the close de-trapping time constant in such short time scale (< 2 ms). However, the degraded recovery (%) is distinctly observed in Fast-DPBTI investigations that demonstrated the impacts of residual charges in the continuing device operation.

6.4 Summary

In our studies, the impacts of charge trapping/de-trapping were investigated systematically on the dynamic-PBTI degradation in nMOSFETs with HfO_2/SiO_2 gate stack through both DC and pulse measurements. The charge trapping exhibited the identical behaviors in each stress sequence when recovery voltage is sufficiently large. As similar to charge trapping, the charge de-trapping showed the invariant quantity of recovered charges in each recovery sequence that indicated the unique recovery at certain recovery voltage. Therefore, a reproducible dynamic-PBTI phenomenon is successful to fine fit with the model of charge filling in the pre-existing trap centers in the high-κ bulk. Once the recovery voltage does not have the sufficient capability to remove most of the trapped charges, accumulation of residual charges would have apparently influences on the DPBTI degradation. In addition, the elevated temperate would enhance both charge trapping/de-trapping effects. The trap-assisted conduction mechanisms would be activated under the crucial temperature to enhance the accumulation of residual charges even though an almost full recovery can be achieved at room temperature under Vr = -2.0V. Although the temperature-assisted the Fast-DPBTI degradation is apparent, the experimental results demonstrated that recovery voltage still dominated the whole DPBTI degradation. In the aspect of stress voltage, the charge trapping is as a strong function of stress voltage which is associated with the quantity of injection charges. However, the recovery behavior is less dependent on the stress voltage due to the close de-trapping time constant in such short time scale (< 2 ms). As all of above results, the residual charges occurred during the DPBTI degradations have been demonstrated as the main issue to have the great impacts on the continuing device operation with the high-κ gate dielectrics.

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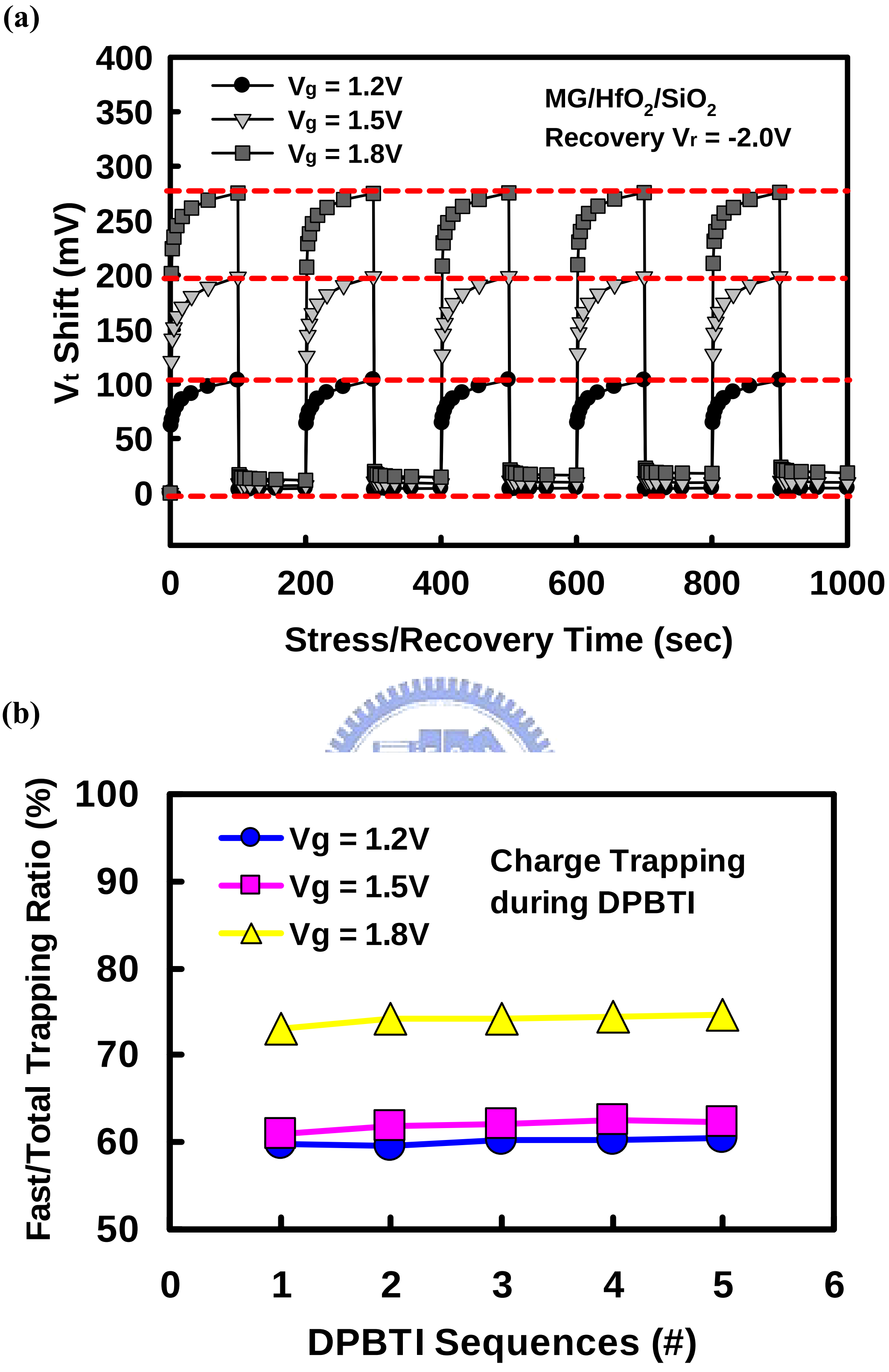

Fig. 6-1 The dynamic positive bias temperature instability (DPBTI) under various stress voltages (a) Threshold voltage shift during DPBTI degradation (b) Ratio of (fast trapping)/(total trapping) during DPBTI degradation.

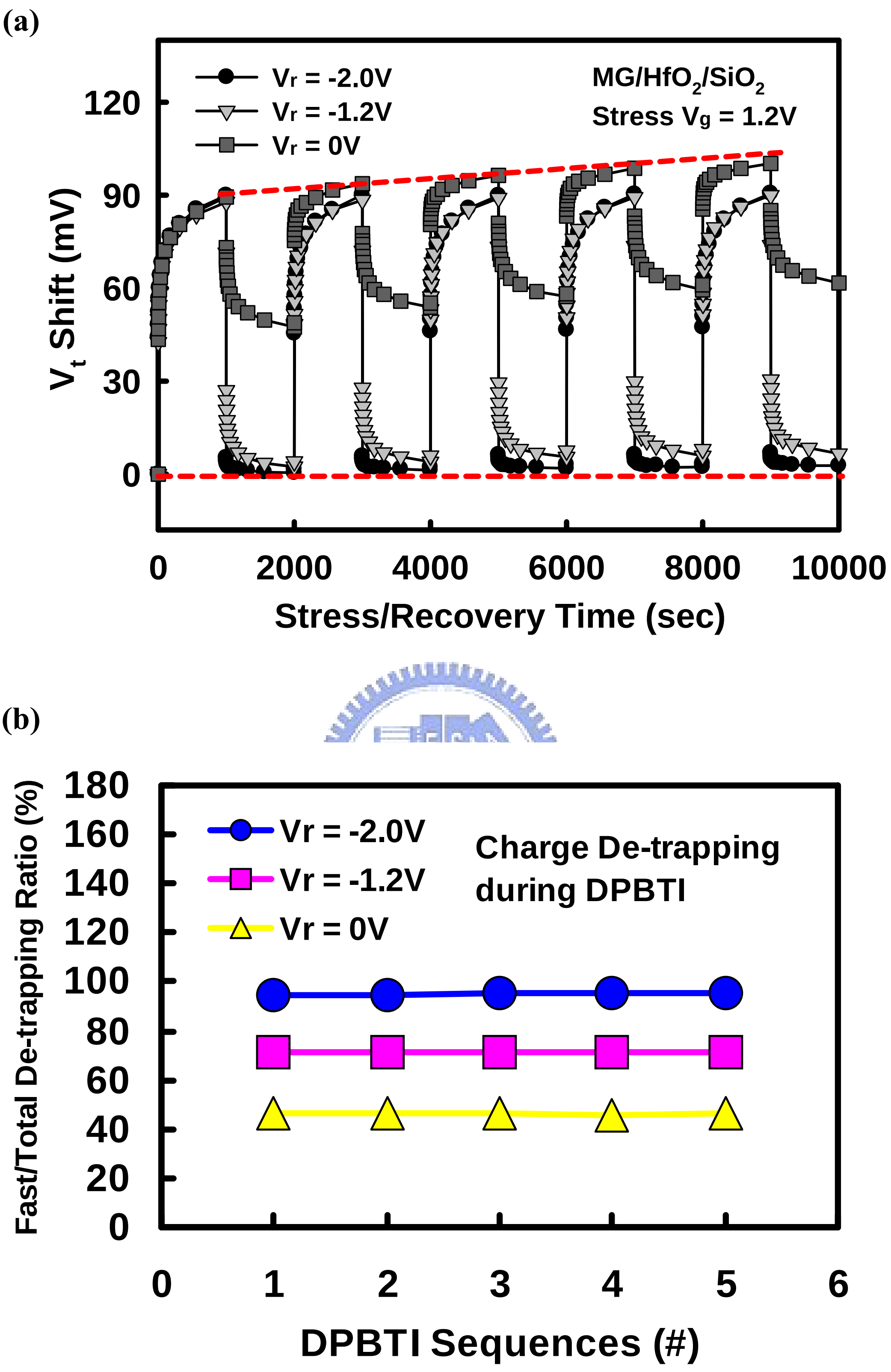

Fig. 6-2 The dynamic positive bias temperature instability (DPBTI) under various recovery voltages (a) Threshold voltage shift during DPBTI degradation (b) Ratio of (fast de-trapping)/(total de-trapping) during DPBTI degradation.

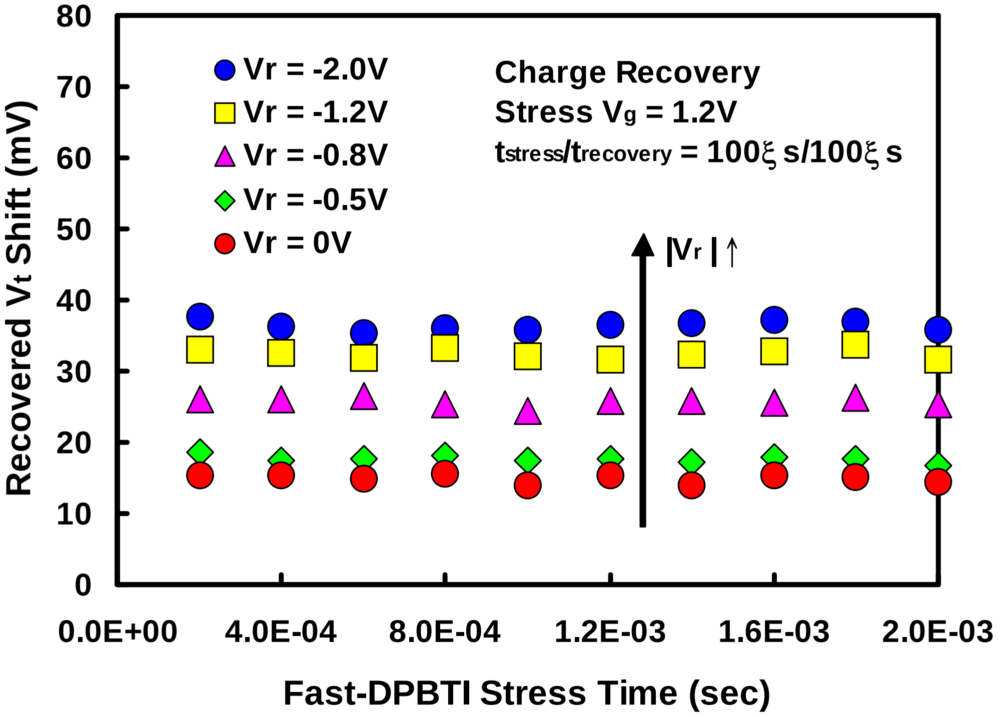

Fig. 6-3 The fast transient charge de-trapping during DPBTI degradation under various recovery voltages.

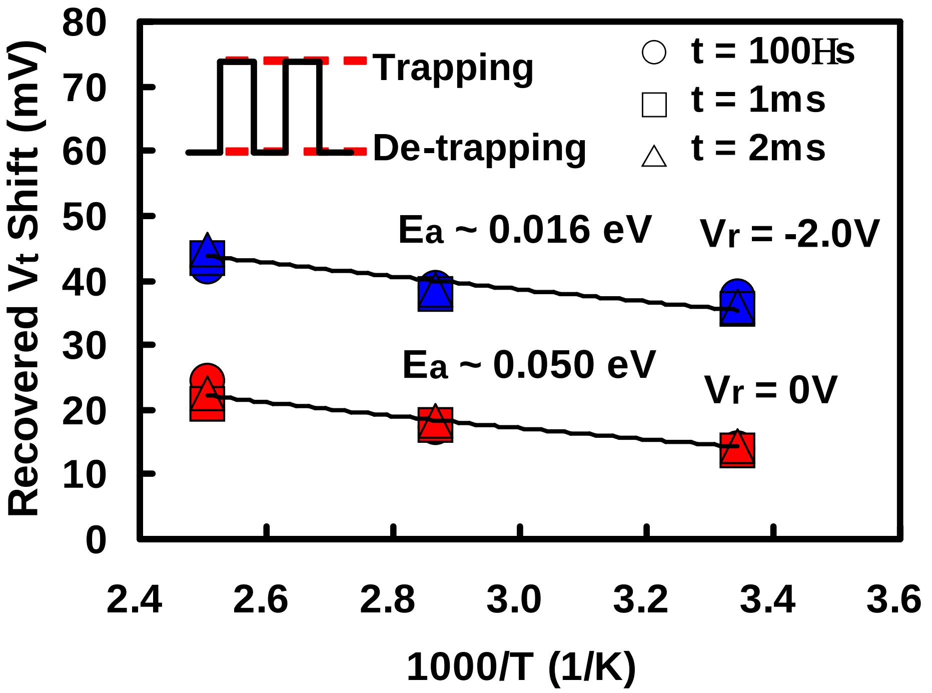

Fig. 6-4 The temperature dependence on fast transient charge de-trapping during DPBTI degradation under various recovery voltages.

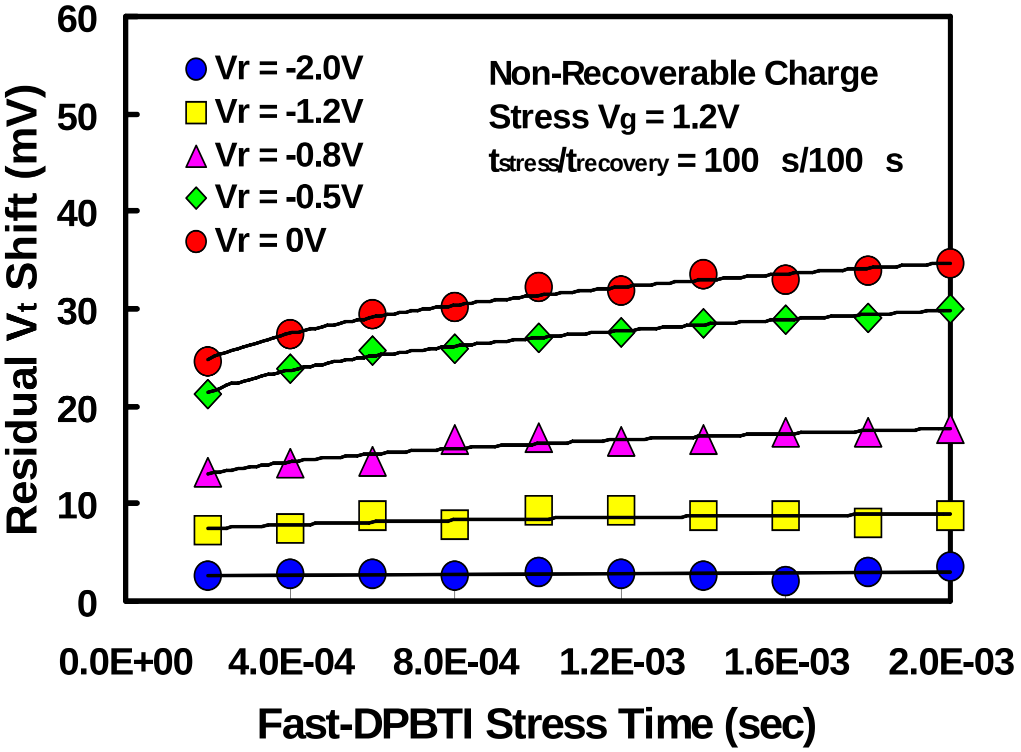

Fig. 6-5 The residual V_t shift (non-recovered V_t shift) as a function of stress time during DPBTI degradation under various recovery voltages.

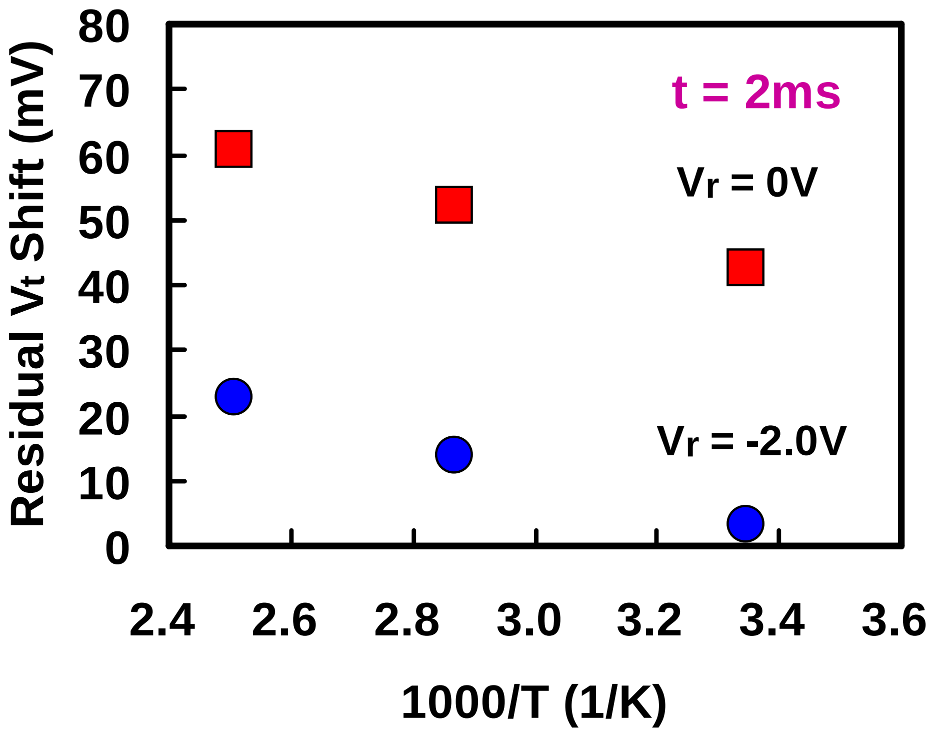

Fig. 6-6 The temperature dependence on residual V_t shift during DPBTI degradation under various recovery voltages.

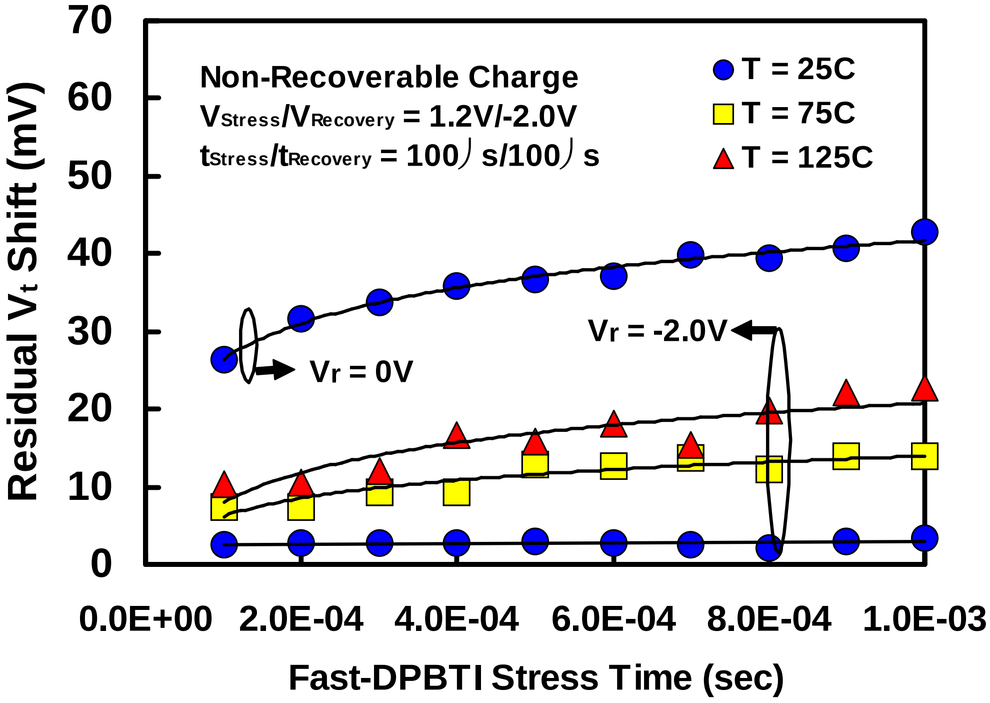

Fig. 6-7 The impacts of temperature on the residual V_t shift during DPBTI degradation. The result of $V_r = 0$ is the comparison with $V_r = -2.0$.

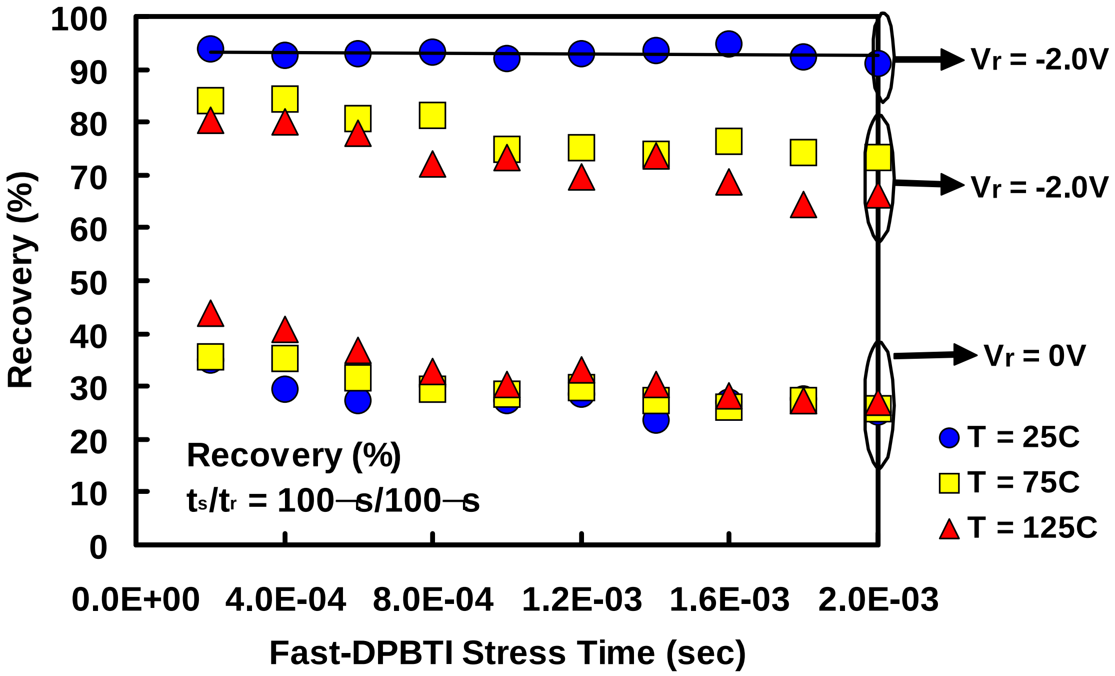

Fig. 6-8 The impacts of temperature on the recovery (%) during DPBTI degradation under various recovery voltages.

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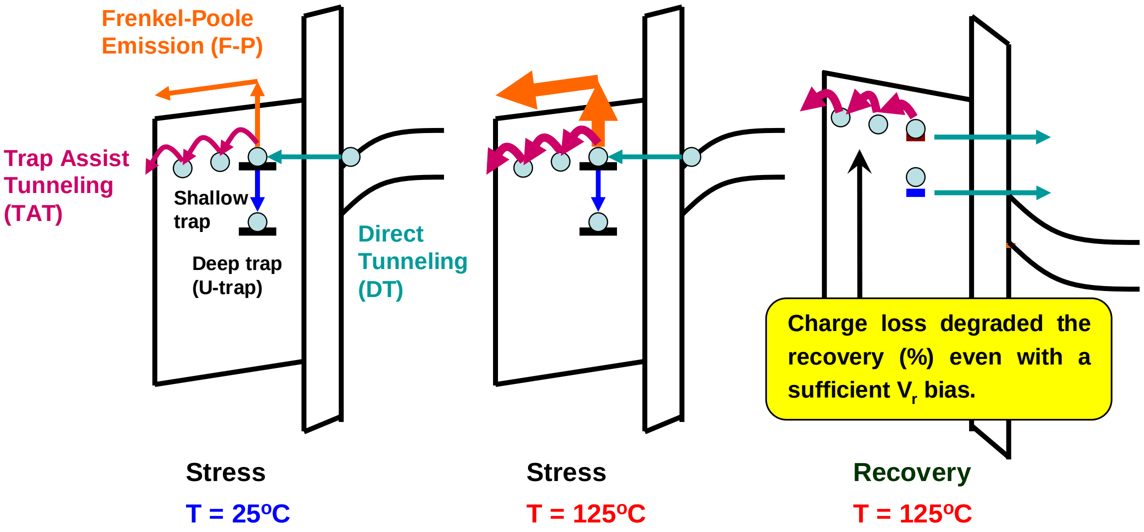
Frenkel-Poole
Emission (F-P)
Trap Assist
Tunneling
(TAT)
Shallow
trap
Deep trap
(U-trap)
Direct
Tunneling
(DT)
Charge loss degraded the recovery (%) even with a sufficient V_r bias.
Stress
T = 25ºC
Stress
T = 125ºC
Recovery
T = 125ºC

Fig. 6-9 The schematic band diagrams related to the influences of the elevated temperature on the fast transient charge trapping/de-trapping during the DPBTI degradation. The trap-assisted conduction mechanisms become more active at higher temperature.

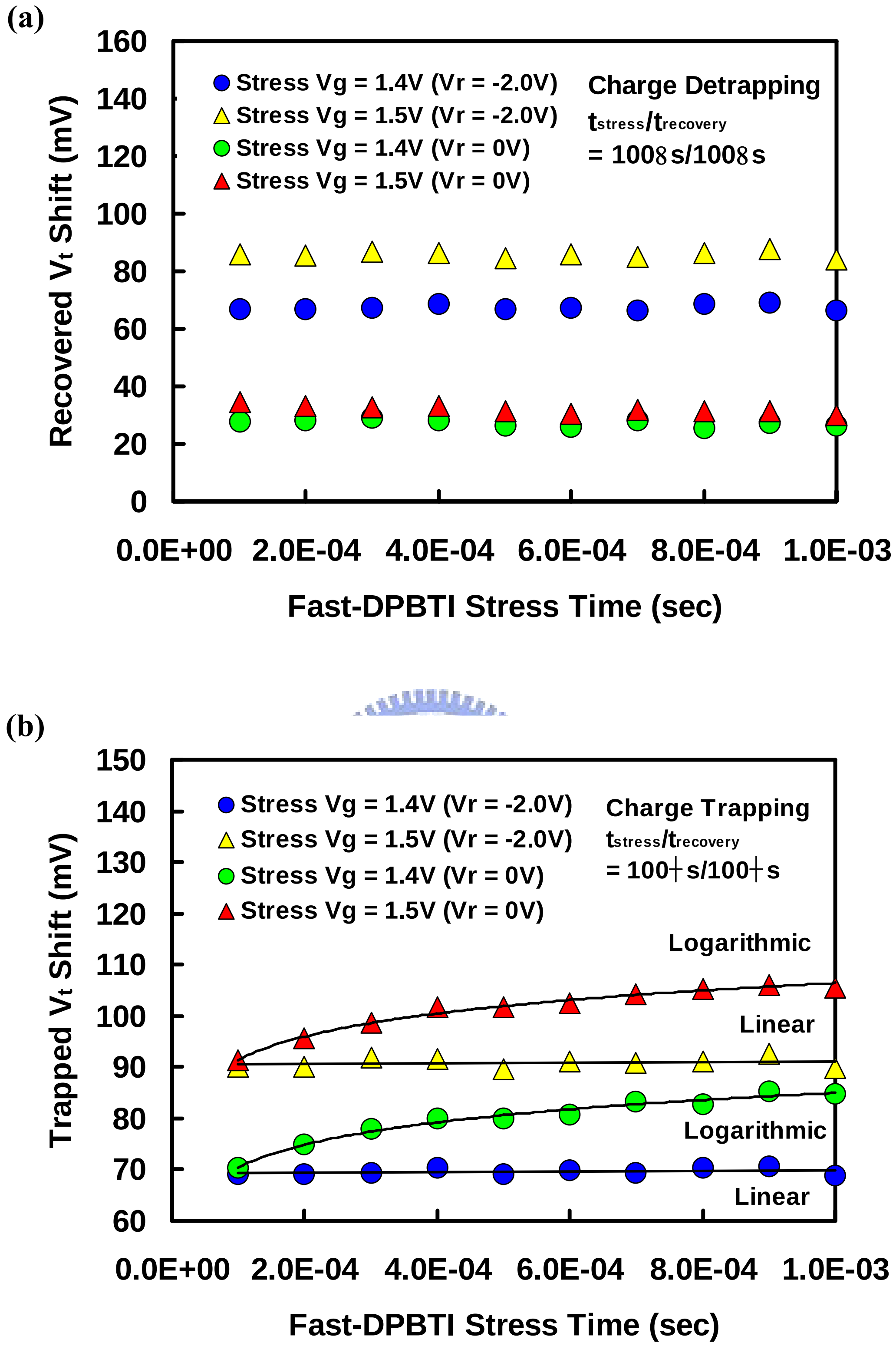

Fig. 6-10 The impacts of stress voltage (V_g) on the charge trapping/de-trapping behaviors during DPBTI degradation under various recovery voltages. (a) Recovered V_t shift (b) Residual V_t shift.

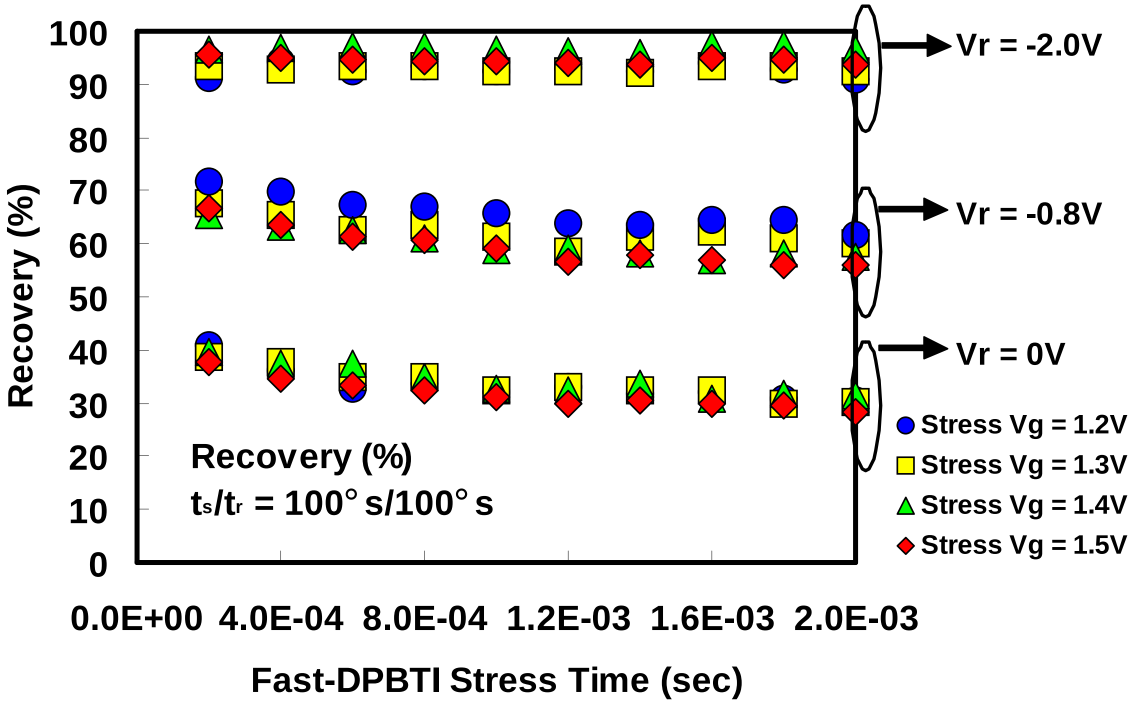

Fig. 6-11 The impacts of stress voltage on the recovery (%) during DPBTI degradation under various recovery voltages.

Chapter 7

Anomalous Negative Bias Temperature Instability Behavior in pMOSFETs with HfO_2/SiON Gate Stack

7.1 Introduction

High-κ materials are introduced as the alternative gate dielectrics since they can significantly suppress the intolerable leakage current presented in the ultra-thin conventional SiO_2 [1-2]. To date, although many related researches have been conducted to make great progress for high-κ gate dielectrics, some critical challenges still remain. One of the most critical issues in high-κ gate dielectric is the charge trapping effect in the high-κ bulk to significantly impact on device performance and reliability [3-5]. For the viewpoints of conventional pMOSFETs with the SiO_2 gate dielectric, negative bias temperature instability (NBTI) is one of the challenging issues faced by the device community in recent years because the phenomenon is more significant than positive bias temperature instability (PBTI) occurred in nMOSFETs [6]. Previously, the reaction-diffusion (R-D) model involving the concepts of the bond-breaking at SiO_2/Si-substrate and the hydrogen related species was commonly used to explain the specific features of NBTI [7-9]. In this model, Si-H bond breaking was assumed to occur at the Si interface. The resulting dangling bonds and hydrogen species that diffuse into gate dielectrics in turn caused threshold voltage shift (ΔV_{th}) and interface state generation (ΔN_{it}) [10]. It has been proven to be quite practical in predicting the behaviors both in voltage- and temperature-accelerated NBTI degradations [11-12]. However, in the above mentions of the charge trapping effect in high-κ dielectrics, this quite complicated issue will greatly deteriorate the characteristics of high-κ devices even leading the dominant of NBTI degradation [13-16]. In other words, the applications of high-κ gate dielectrics on CMOS technology make the R-D model be no longer as the unique physical mechanism in the aspect of NBTI degradation. Moreover, the considerations of charge trapping effect become to be more and more important in reliability concerns. Therefore, the investigations of the charge trapping effect in the high-κ dielectrics have attracted much attention in recent years, especially the specific impacts on reliability degradation. So far, most of the people still intuitively consider that the NBTI degradation in high-κ dielectrics has the similar mechanism with respect to SiO_2 through the entire stress voltage range and the lifetime prediction has been often done by the linear extrapolation

In this work, we systematically investigated the behaviors of charge trapping effect in pMOSFETs with HfO_2/SiON gate stack. Many methodologies were employed to evaluate its impact on the electrical properties and reliability of the pMOSFETs with HfO_2/SiON gate stack, including NBTI investigations, and measurements with DC and AC stresses. We found that the polarity of net trapped charge in high-κ dielectric was not the same in the regimes of applied gate voltages for DC stress. The distinct findings resulted in that the typical linear extrapolation does not work well for the lifetime extraction at different stress voltage. Moreover, we also discovered that the charge trapping in high-κ dielectrics was strongly dependent on the frequency and duration of AC stress.

7.2 Experimental Procedures

In this study, pMOSFETs were fabricated on (100) n-type Si wafers. After a standard RCA cleaning with a final HF-dip. The N_2O surface treatment performed a

0.7nm thin interfacial oxyntride layer (SiON) using rapid thermal processing at 700°C. A 3.0nm HfO_2 layer was deposited by MOCVD system at 500°C, followed a high temperature post deposition annealing in an N_2 ambient at 700°C for 20s to improve the film quality. A polycrystalline silicon layer was utilized to be the gate electrode, and the dopant activation was conducted at 950°C by rapid thermal annealing for 20s in an N_2 atmosphere. After passivation, contact holes formation, Al metallization and patterning, the forming gas annealing at 400°C was finally performed for 30 minutes to complete the device fabrication. The NBTI measurement was conducted as the sequences in Fig.7-1. The split table of stress voltage included -2.6V, -3.0V, -3.1V, -3.3V, -3.5V, and -4.0V. In NBTI investigations, the threshold voltage (V_t) and the interface trap density (N_{it}) were extracted by I_d-V_g measurement and charge pumping method, respectively. The increase of total trap density was calculated from $\Delta N_{tot} = C\Delta V_{th} / qA_G$, where C is gate capacitance and A_G is the gate area.

7.3 Results and Discussions

7.3.1 Anomalous NBTI Behaviors

The NBTI degradation investigated with various stress conditions was presented in Fig. 7-2(a). The resultant of threshold voltage shift (ΔV_t) was negative and it became more significant with elevated stress voltage when $|V_g| > 3.1V$. This experimental result has been well known as a result of the hole trapping in the bulk of high-k dielectrics [17-19]. Nevertheless, the tendency of NBTI results was not monotonic as we expected when we kept going on lowering the stress voltage. In Fig. 7-2(b), when $|V_g| < 3.1V$, an apparent turnaround phenomenon was observed that the ΔV_t turned negative trend into positive trend since the type of the dominant trapped charge in the dielectrics has changed from hole to electron. Furthermore, the NBTI degradation gradually turned into more significant with further deceasing stress voltage indicating that electron trapping dominates at lower applied gate voltages. This result strongly implies that the mechanism of NBTI degradation in the high-κ gate dielectrics is not unique for the charge trapping effect in the bulk of HfO_2 is distinct in different stress voltage regimes.

To consider the influence of interface degradation, Fig. 7-3 illustrated the degradation of ΔN_{it} that increased monotonically with increasing stress voltage and represented only relatively small influence on ΔV_t. For further carefully check, the interface properties during NBTI degradation was reviewed under elevated temperature. A severer interface degradation that can be explained by temperature-accelerated the bond-breaking at Si-interface was found in Fig. 7-4. On the other hand, in Fig. 7-5, the ΔV_t revealed a more serious hole trapping phenomenon under elevated temperature no matter the conditions of stress voltage since the electrons were considered to easily de-trap at higher temperature. Furthermore, the net charge of HfO_2 bulk traps was analyzed at stress $| Vg | < | -3.1V |$ and stress $| Vg | > | -3.1V |$ in Fig. 7-6(a) and Fig. 7-6(b), respectively. A decrease of electron trapping in the regime of stress $| Vg | < | -3.1V |$ under severer temperature further verified the distinct characteristics of electron de-trapping (or relative to the reinforcement of hole trapping) that was entirely consistent with the previous discussions about the temperature-enhanced electron de-trapping. From the above results, it is believed that the charge trapping in the bulk of HfO_2 has greater impacts than the interface degradation in whole NBTI. Thus the specific phenomenon of anomalous NBTI is closely related to the bulk traps rather than the interface states. The influences of number of injection charge under various stress conditions were exhibited in Fig. 7-7. The fine fitting results referred to S. Zafar et al. [20] were observed to further confirm the critical role of HfO_2 bulk traps in this anomalous NBTI phenomenon.

7.3.2 Charge Pumping Methodology

This charge trapping effects can be also verified by the charge pumping measurements shown in Fig. 7-8. As expected, the interface degraded much seriously with elevated stress voltage. However, a different charge trapping effects were found in charge pumping current, I_{cp}. As stress voltage = -3.0V, an apparent positive shift of I_{cp} indicated the evidence of electron trapping. On the contrary, as stress voltage = -3.3V and -3.5V, the negative shift of I_{cp} referred to the hole trapping. A turn around point with net trapping nearly free except the generation of interface sites was observed between these two different charge trapping mechanisms at stress voltage = -3.1V. The experimental result here is fully consistent with that presented in Fig. 7-2(a)-(b).

For the considerations of what does this anomalous NBTI phenomenon originate form? We thought it might be with respect to the intrinsic properties of high-κ materials themselves, or it was a universal behavior just related to charge trapping effect itself in all high-κ dielectrics. Fig. 7-9(a)-(c) illustrated the I_d-V_g characteristics to reveal the anomalous NBTI phenomenon found in other high-κ gate stack ($HfSiON/SiO_2$). As the same results, the transitional behaviors represented by V_t shift were also discovered from hole trapping at higher stress $|V_g|$ to electron trapping at lower stress $|V_g|$. Similarly, in Fig. 7-10(a)-(c), the charge pumping characteristics also exhibited the same results discovered in HfO_2/SiO_2 gate stack. These strong evidences are powerfully to confirm that anomalous NBTI phenomenon is independent of high-κ materials but it is a universal behavior about charge trapping effect.

Figure 7-11 showed the band diagrams under bias conditions of -3.5V and -2.6V, respectively. As stress voltage = -3.5V, large probability of hole injection from Si substrate induced significant negative ΔV_t according to the obvious band bending under large voltage. On the contrary, when stress voltage = -2.6V, the hole injection was suppressed by interfacial layer while the dominant mechanism changed from hole trapping to electron trapping. In Fig. 7-12, the HfO_2 bulk traps were carefully studied in NBTI degradation. A smile curve clearly described the different polarity of net trapped charge on the relationship of stress voltage. An anomalous NBTI behavior will occur in the regime accompanied electron trapping to demonstrate that the NBTI degradation does not obey an unique mechanism with the considerations of both electron trapping and hole trapping in high-κ bulk traps. Therefore, the NBTI behaviors reveal a strong dependence on applied gate voltage.

7.3.3 AC Characteristics

Figure 7-13(a)-(b) and Fig. 7-14(a)-(b) represented the ΔV_t and ΔN_{it} as a function of both frequency and duty cycle, respectively. We clearly observed that ΔV_t appears to be strongly dependent on frequency and duty cycle while ΔN_{it} depicts almost no frequency and duty cycle dependences. As a result, we again conclude that the strong dependences of NBTI degradation during AC stress on frequency and duty cycle are intimately related to the characteristics of bulk traps instead of interface states as what we have observed at DC stress. In the AC stress conditions, the distinct behaviors were considered as the diversity of time constant (τ_0) between electrons and holes relevant to charge trapping/de-trapping kinetics. Hence we can observe that the electrons easily follow the varying AC signal and get trapped during the on-period.

7.3.4 Lifetime Prediction

From all above experimental data, we conclude that electron and hole trappings are both likely to emerge in the high-κ dielectrics. The dominant trapped species will be determined by the magnitude of stress voltage, the testing temperature, and stress signal shape. Fig. 7-15 demonstrated that the modified lifetime prediction in pMOSFETs with

HfO_2/SiON gate stack will no longer be linear since the polarity of dominant trapped charge in high-κ dielectric is not the same different voltage regimes.

7.4 Summary

In our study, we systematically investigated the behaviors of NBTI of pMOSFETs with HfO_2/SiON gate stack. We demonstrated that an anomalous NBTI behavior was observed at a turn-around applied stress $V_g = -3.1V$ since the type of dominant trapped charge in the bulk of HfO_2 is not the same in whole regimes of stress voltages (electron trapping at stress $|V_g| < |-3.1V|$; hole trapping at stress $|V_g| > |-3.1V|$). The electrical characteristics of electron and hole for charge trapping effect revealed on the stages of stress voltage, temperature, and AC behaviors are extremely different. Electron easily de-traps at elevated temperature and has fast respondence to AC signal while hole has the totally contrary phenomena. Finally, for the most important implication of anomalous NBTI discovery, the linear lifetime extraction is not able to accurately predict the lifetime at normal operation with high-κ gate stack once we consider both electron trapping and hole trapping in high-κ bulk traps.

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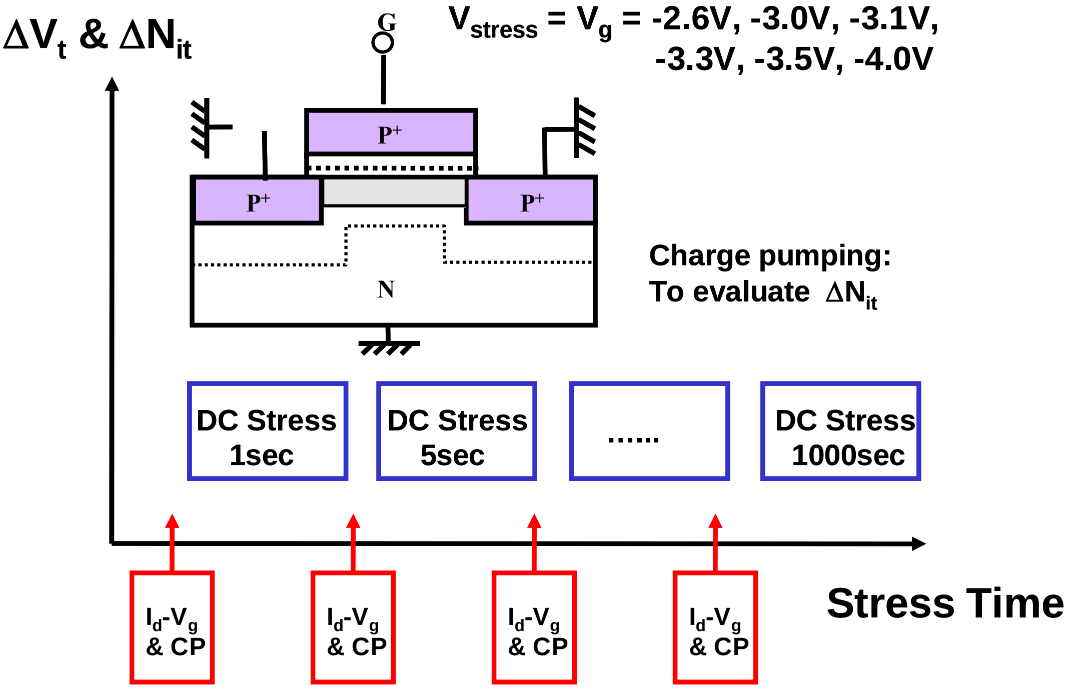
ΔV_t & ΔN_{it}
G
P^+
P^+
P^+
N
$V_{stress} = V_g$ = -2.6V, -3.0V, -3.1V, -3.3V, -3.5V, -4.0V
Charge pumping: To evaluate ΔN_{it}
DC Stress 1sec
DC Stress 5sec
……
DC Stress 1000sec
I_d-V_g & CP
I_d-V_g & CP
I_d-V_g & CP
I_d-V_g & CP
Stress Time

Fig. 7-1 Sequences of negative bias temperature instability (NBTI).

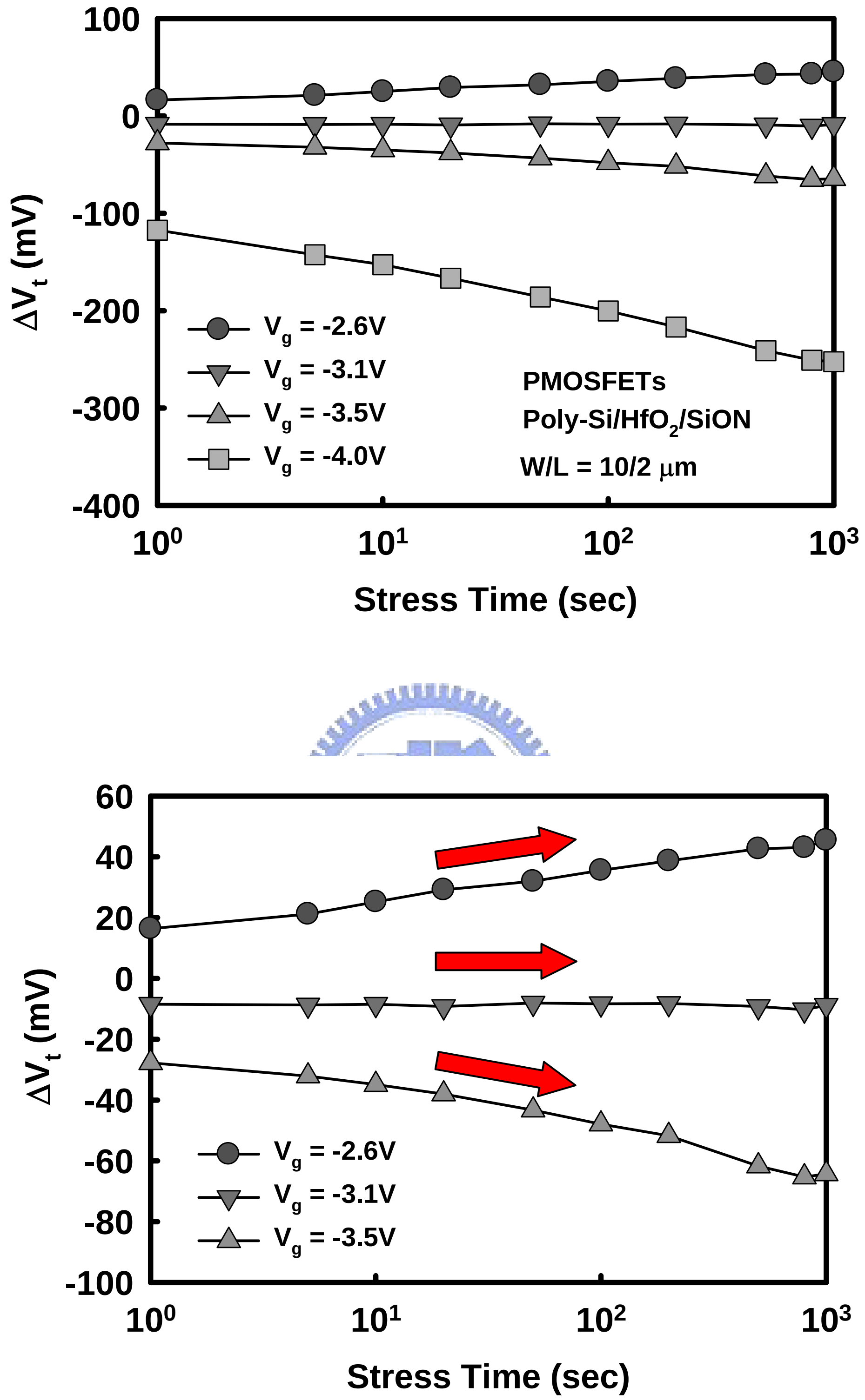

Fig.7-2 (a) The NBTI degradation under various stress conditions at 25℃. (b) Anomalous NBTI degradation showed in Fig.7-1(a).

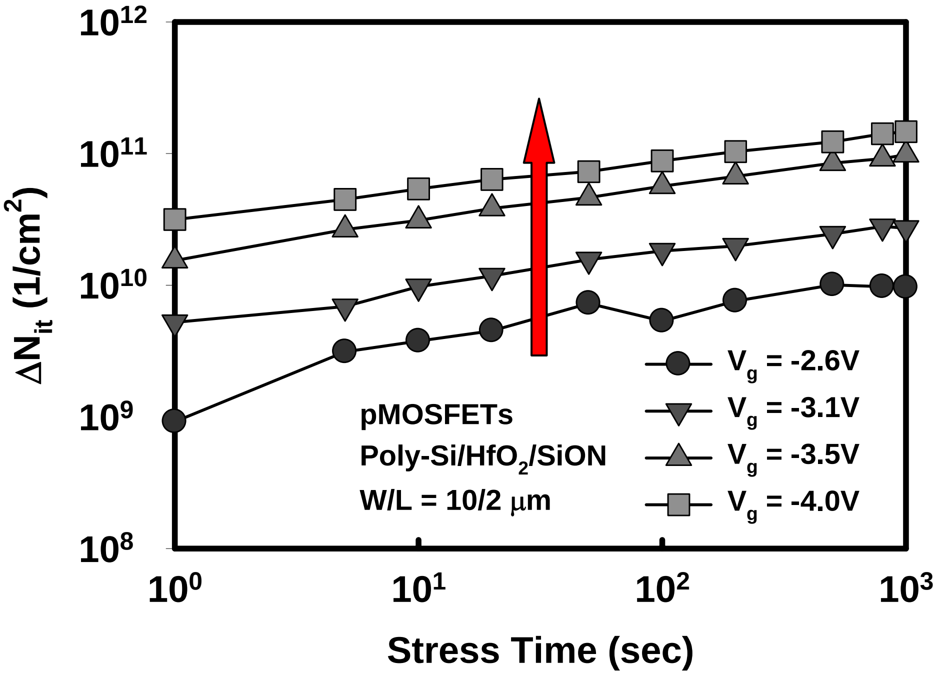

Fig. 7-3 Interface properties during NBTI degradation under various stress conditions at 25℃.

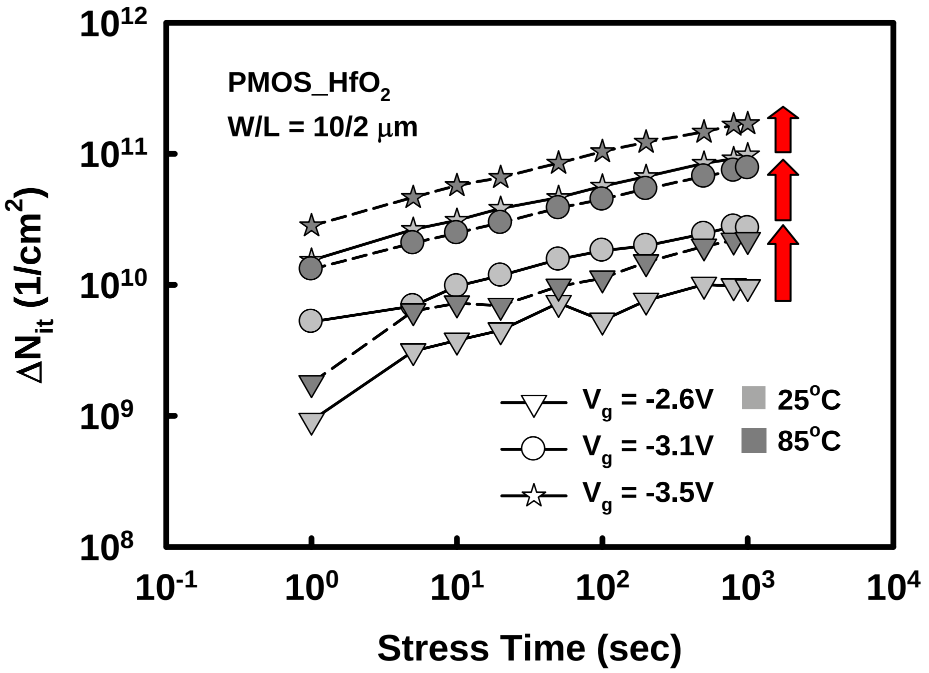

Fig. 7-4 Impact of temperature on threshold voltage shift during NBTI degradation.

1896

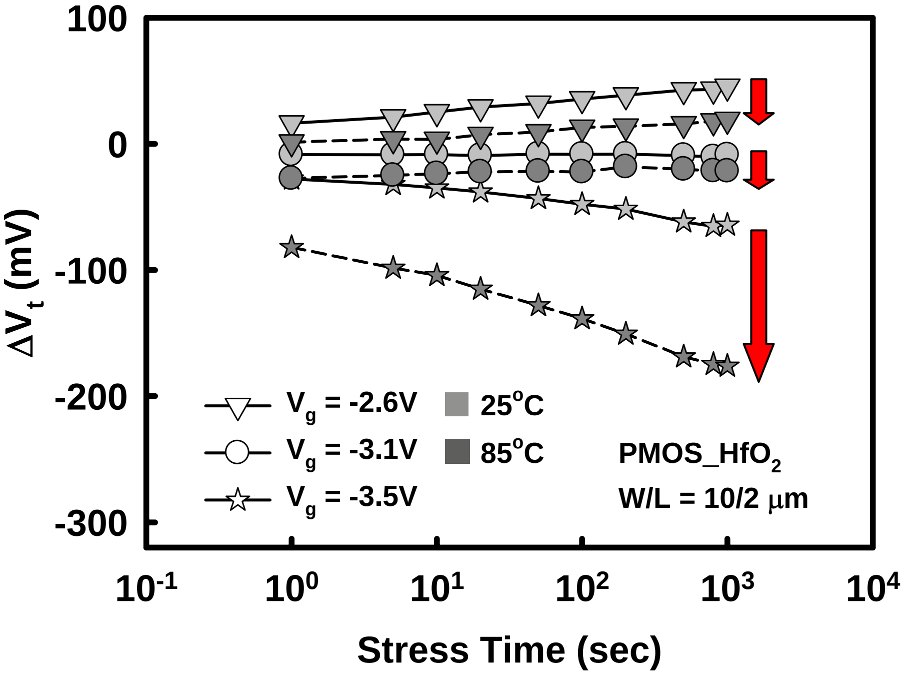

Fig. 7-5 Impact of temperature on interface degradation during NBTI process.

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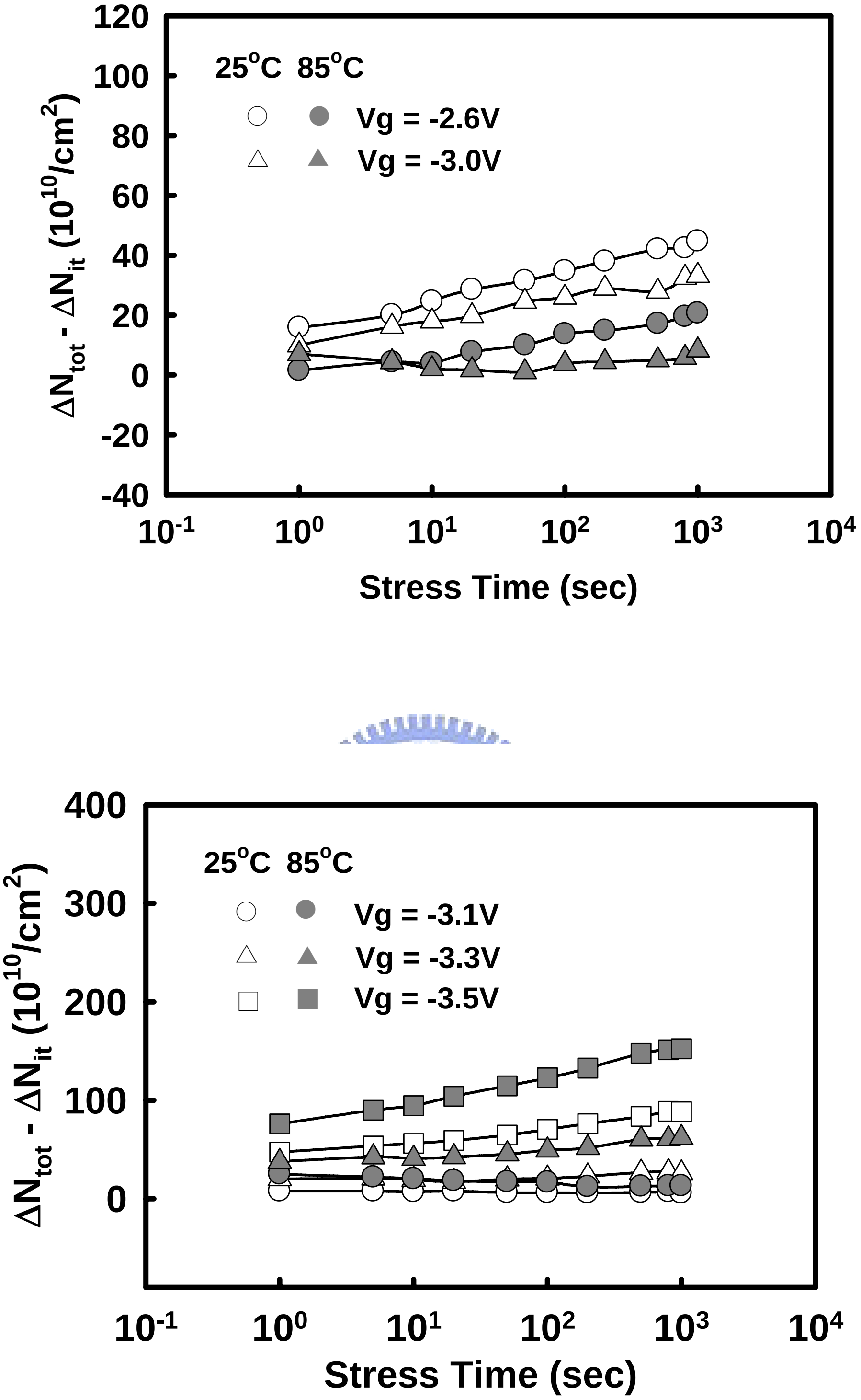

Fig.7-6 Impact of temperature on the generation of bulk traps in HfO_2 at (a) stress | Vg | < | -3.1V | (b) stress | Vg | > | -3.1V |.

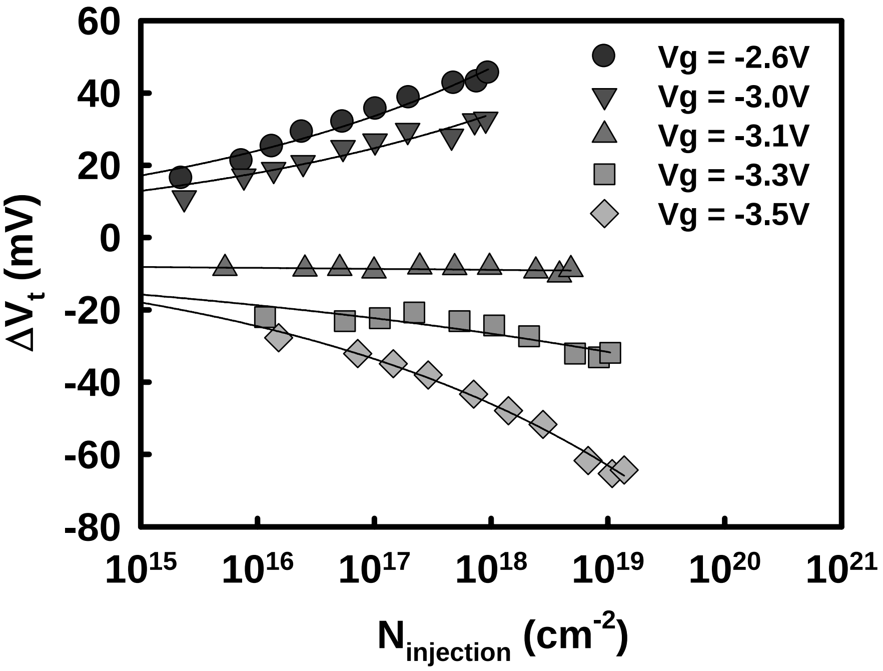

Fig. 7-7 Threshold voltage shift versus number of injection charge under various stress conditions at 25℃.

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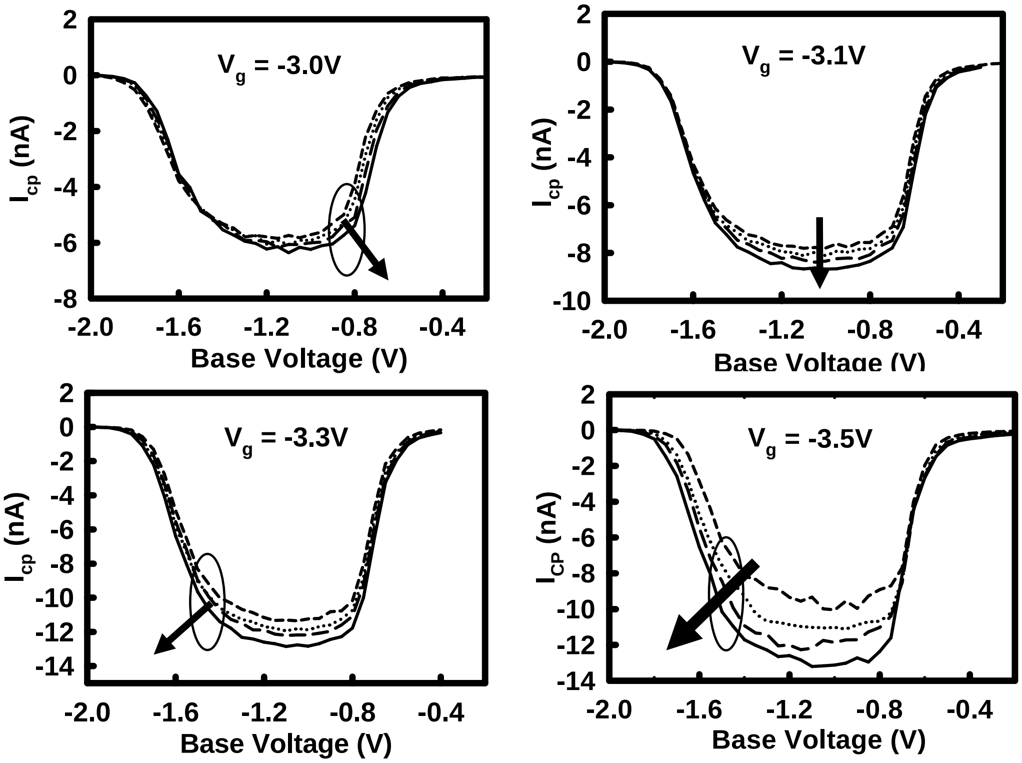

Fig. 7-8 Charge pumping results related to anomalous NBTI conditions.

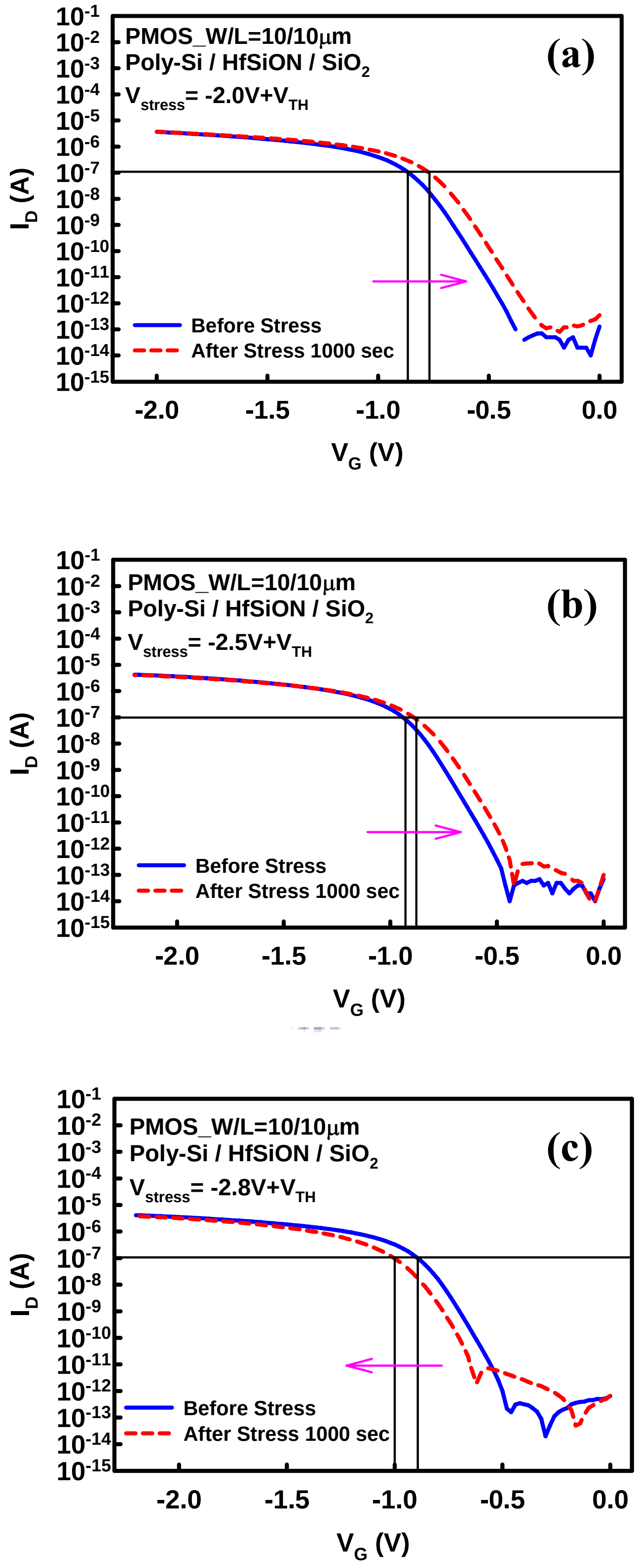

Fig. 7-9 Similar phenomena showed on I_d-V_g results in HfSiON/SiO$_2$ gate stack.
(a) Electron trapping (b) Transition (c) Hole Trapping.

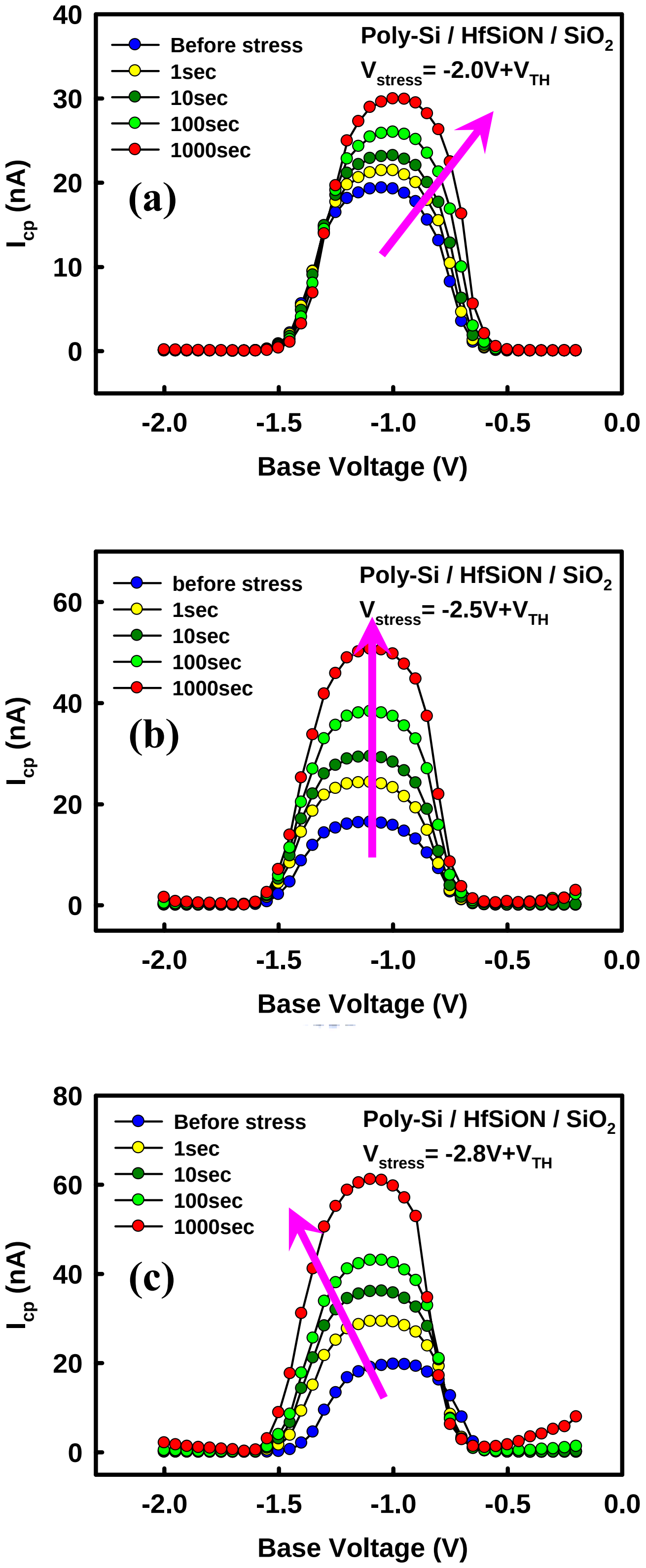

Fig. 7-10 Similar phenomena showed on charge pumping current results in another experiments. (a) Electron trapping (b) Transition (c) Hole Trapping.

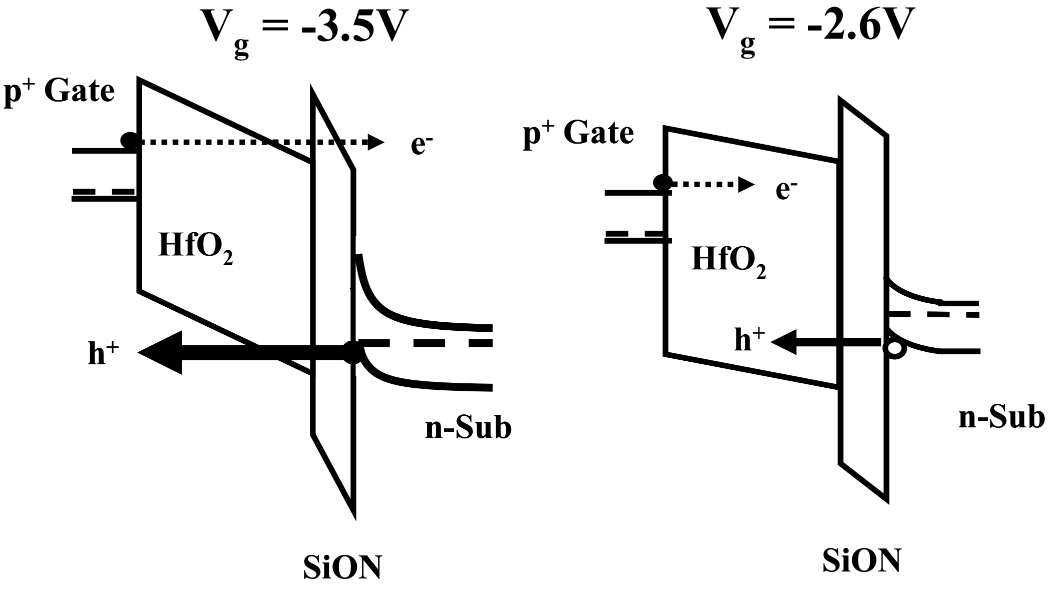
$V_g = -3.5V$
p^+ Gate
e^-
HfO_2
h^+
n-Sub
SiON
$V_g = -2.6V$
p^+ Gate
e^-
HfO_2
h^+
n-Sub
SiON

Fig. 7-11 Band diagram under various stress conditions with respect to distinct polarity of net trapped charge.

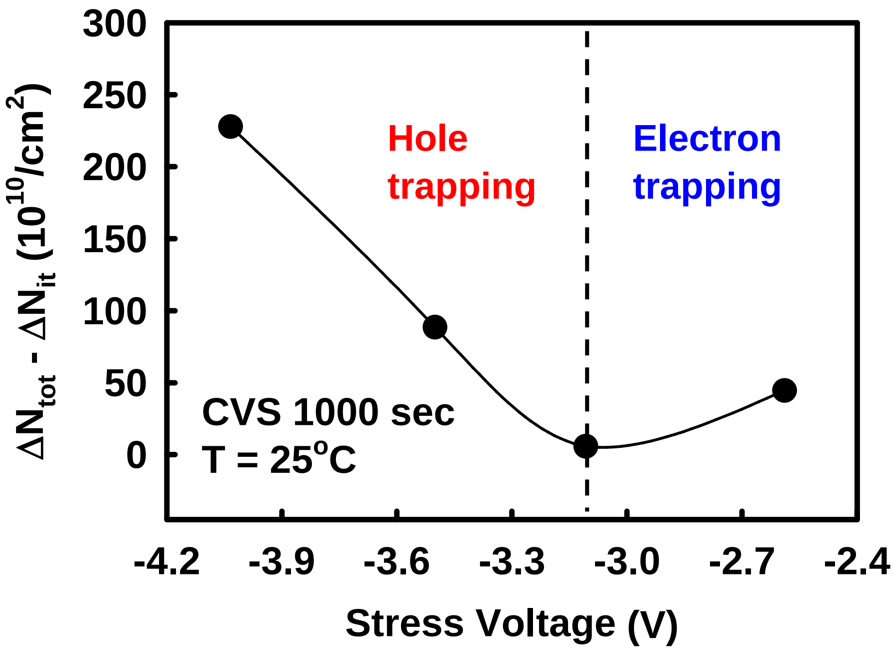

Fig. 7-12 Bulk traps in HfO_2 under various stress conditions.

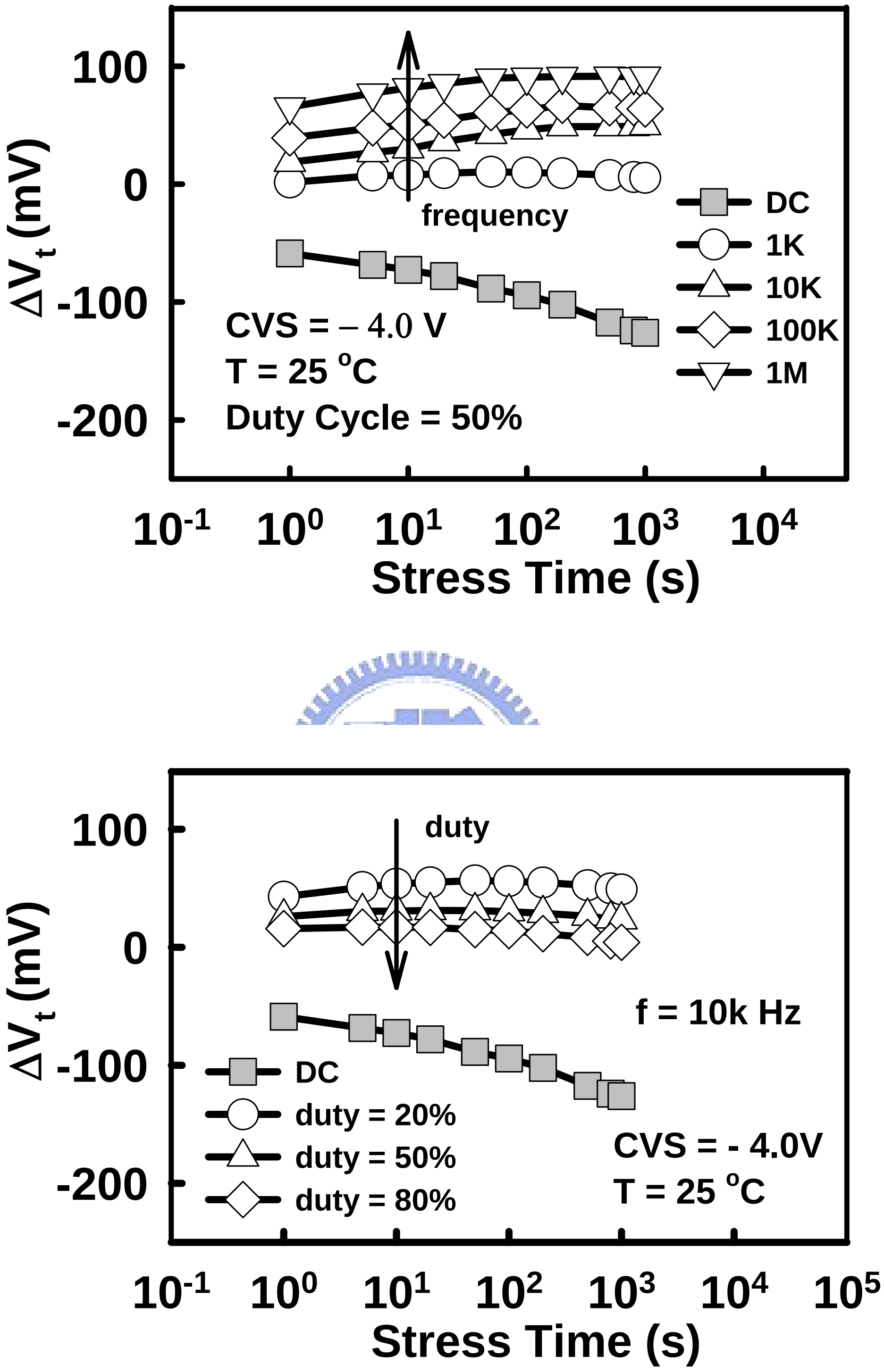

Fig.7-13 Impacts of (a) AC frequency (b) duty cycle on threshold voltage shift, (ΔV_t).

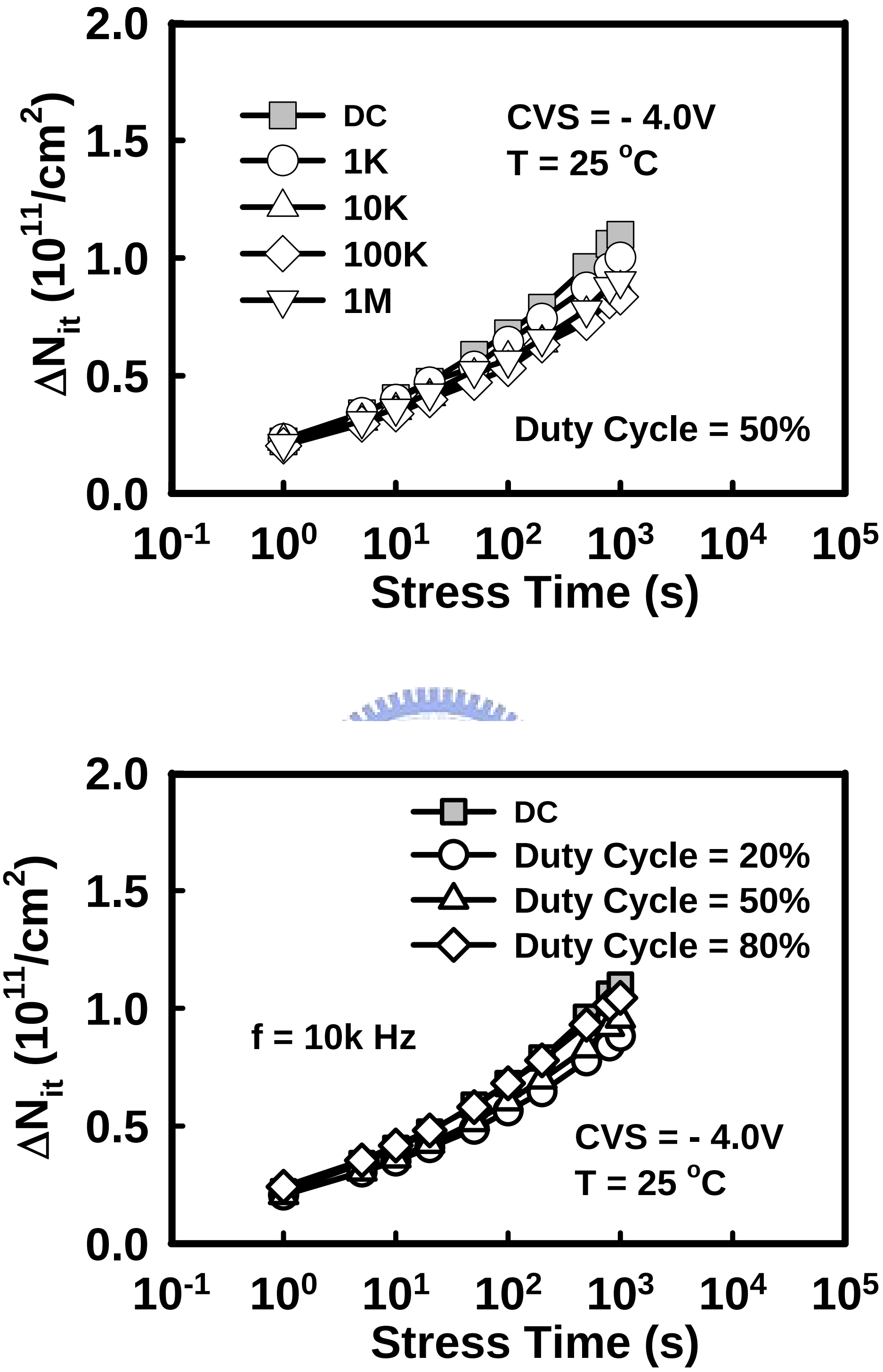

Fig.7-14 Impacts of (a) AC frequency (b) duty cycle on interface degradation, (ΔN_{it}).

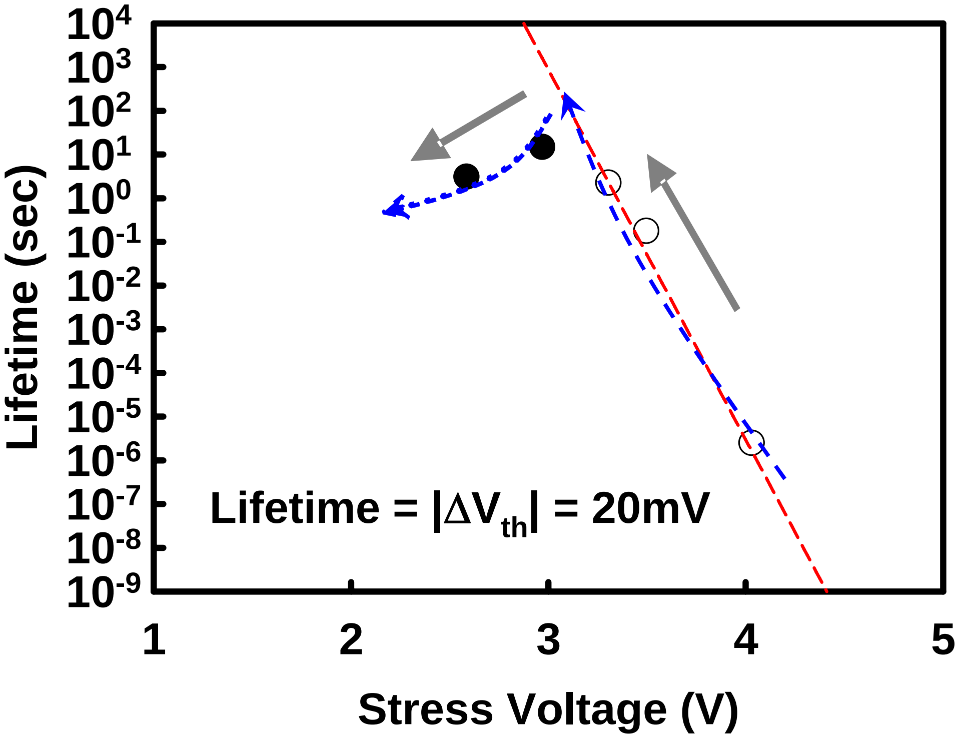

Fig. 7-15 Lifetime prediction with consideration of anomalous NBTI.

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Chapter 8

Conclusions and Future Works

8.1 Summary of Findings and Contributions

In the dissertation, numbers of studies have been conducted to completely understand the high-κ gate dielectrics in terms of various electrical characterizations. In the chapter 2, according to the essential issues of the high-κ gate dielectrics themselves, the device performances were enhanced through fabrication technologies. The ozone surface treatment provided a good quality based oxide with ultrathin thickness (< 1.0 nm), smooth interface, low leakage current, and less charge trapping improve the interfacial properties between high-κ gate dielectric and Si-substrate. Fluorine incorporation has been demonstrated to effectively reduce the bulk traps, and enhanced the device reliability in the pMOSFETs with HfO_2/SiON gate stack. The significant hole trapping is verified to lead the whole NBTI degradation. The tensile strain effect has been confirmed to successfully enhance the device driving current in the nMOSFETs with HfO_2/SiON gate stack. Although additional trap generation and significant PBTI degradation are observed in strained-samples during electrical stress, the strain effects have been demonstrated not to change the essential properties of HfO_2 bulk traps.

In the chapter 3, the charge trapping behavior has been carefully investigated on the PBTI degradation in nMOSFETs with HfO_2/SiO_2 gate stack. A mathematical modeling with the fine fitting results provide the strong evidences to successfully demonstrated that the electron trapping in high-κ gate dielectrics is the major of leading the PBTI degradation. The total trapping density in high-κ gate dielectrics is also demonstrated as a function of stress voltage rather than a conserved quantity of charge filling in the pre-existing high-κ bulk traps (for large electrical stress regime). An identical value (60%) of fast/total trapping ratio is considered to be responsible for the shallow traps (oxygen vacancies, Vo^{2+}, Vo^{-}, Vo^{2-} and grain boundary defects) in HfO_2 which are consistent with the related trapping energy levels in other literatures. Once the FN-tunneling occurs over the critical voltage, the ways of capturing injection electrons would change to be from conduction band of HfO_2 and further bring on a significant contribution of fast trapping. In addition, the time dependence results revealed the aspects of energy distribution for charge trapping behavior in the high-κ gate dielectrics.

In the chapter 4, the charge de-trapping behavior also has been well investigated on the PBTI degradation in nMOSFETs with HfO_2/SiO_2 gate stack. The fine modeling fitting demonstrated that the relaxation of trapped charges in high-κ gate dielectrics is mainly responsible for the charge recovery. The related investigations were conducted in two considerations of stress voltages and recovery voltages which are with respect to the quantity of injection charges and the capability of charge recovery, respectively. The fast de-trapping greatly dominated the discharging effect as similar as the role of fast trapping in charging effect. The fast/total de-trapping ratio under those weak recovery force (V_r = -0.5V, 0V, 0.5V, 1.0V) also shows an identical value of 60% which is consistent with the findings in charge trapping behavior. It further confirms the contributions of the shallow traps associated with oxygen vacancies and grain boundary defects in HfO_2 again. Furthermore, the concept of available charge tunneling back to Si-substrate is established to appropriately explain the physical mechanism of charge de-trapping in high-κ gate dielectrics.

In the chapter 5, the pulse measurement has been firmly demonstrated to be the necessary methodology in order to completely capture the charge trapping/de-trapping phenomena in high-κ gate dielectrics with the further considerations of fast transient behaviors. Plenty of related investigations were conducted on the stages of stress voltages, stress time, and recovery voltages to complete the physical mechanisms of charge trapping/de-trapping effects. Low activation energy observed form the temperature dependence demonstrated that the charge tunneling is the predominance for both charge trapping/de-trapping dynamics. Moreover, the AC stress has been verified to indeed affect the PBTI degradation through the investigations on input waveform and AC frequency. A linear AC/DC ratio also pointed out the critical concerns of charge trapping in high-κ gate dielectrics on device operations switched between AC and DC modes.

In the chapter 6, the impacts of charge trapping/de-trapping on the continuing device operation were analyzed systematically in the dynamic-PBTI (DPBTI) degradation with both DC and pulse measurements. The charge trapping/de-trapping revealed each identical behavior on the stages of stress and recovery, respectively. Hence, a reproducible DPBTI phenomenon is successful to fine fit with the model of charge filling in the pre-existing trap centers in the high-κ bulk. In the considerations of fast transient behaviors, a Fast-DPBTI measurement was also conducted with the pulse methodology. The accumulation of residual charges was confirmed to apparently influence the DPBTI degradation due to the insufficient recovery force. Furthermore, the recovery voltage is verified to be the primary predominance in the Fast-DPBTI degradation even though the elevated temperature would active the trap-assisted conduction mechanism to lead to much charge loss. From the experimental results in Fast-DPBTI, the residual charges occurred during the DPBTI degradations have been demonstrated as the critical influence on the continuing device operation with the high-κ gate stack.

In the chapter 7, a novel finding of the anomalous NBTI behavior was discovered in pMOSFETs with HfO_2/SiON gate stack. The NBTI degradation is on longer following the common major origin of injection holes due to the different types of dominant trapped charges found in the high-κ bulk through a variety of electrical characterizations such as threshold voltage shift, charge pumping results, and NBTI measurements. The hole trapping and electron trapping are demonstrated to be individual responsible for the distinct tendencies of threshold voltage shift at a turn-around applied stress V_g = -3.1V. Therefore, for the most important implication of anomalous NBTI discovery, the lifetime extraction is necessary to be with the further considerations of both electron trapping and hole trapping in the high-κ gate stack.

8.2 Suggestions for Future Works

From the plentiful experiences in a series of related high-κ investigations, there are some suggestions which are considered to be helpful to the realization and promotion of high-κ gate dielectrics applied on the CMOS technology as below:

(1) Although the effective contributions of strain effect are demonstrated to enhance the device performance, the associated mechanisms are unknown on high-κ reliabilities. The origin of additional high-κ bulk traps induced by strain effect is especially necessary to be concerned since the strain technology is evaluated to be one of the most potential methodologies to improve the device performance with the considerations of high-κ gate stack.

(2) From the dissertation, the oxygen vacancies (Vo^{2+}, Vo^{-}, Vo^{2-}) and grain boundary defects are considered as those shallow traps in HfO_2 to be responsible for the fast trapping/de-trapping behaviors which greatly impact the device reliability. From the basic aspects of the high-κ materials, it is worth to further think about how to

effectively reduce those shallow traps while mentioning the desirable characteristics of high-κ gate dielectrics. Numbers of methodologies about the high-κ gate growth and related fabrication technologies are considered as the possible ways to success.

(3) In the charge trapping, it is hard to distinguish form the charge filling in the pre-existing traps and the additional trap generation. Although the chare filling model has successfully fine fitted many experimental results, the quality of trapped charges is verified to be as a strong function of stress voltage. Therefore, the model is indeed necessary to carefully explore the detail and further construct a complete physical mechanism.

(4) The exact trap distribution is always confusing in high-κ gate dielectrics. A large number of experiments have been conducted to establish the proper physical models through the aspects of energy distribution or spatial distribution, respectively. However, it is found that these present models are not really complete to explain the charge trapping/de-trapping behaviors in all considerations associated with both energy and spatial concepts. For example, the time dependence of BTI degradation has been demonstrated to appropriately explain the spatial distribution of traps in high-κ gate dielectrics, but the U-trap model also has been adopted to successfully describe the charge trapping phenomenon through the viewpoint of energy distribution. Therefore, it is necessary to do more efforts on the clarification of the trap distribution and its association with device characteristics and related reliability issues.

(5) In most charge trapping/de-trapping investigations, the roles of electrons (holes) in PBTI (NBTI) are usually the major concerns in the reliability degradation. It is often simplified as a single vision to consider the charge transport of majority

carriers from one way of the gate stack or Si-substrate. Actually, many complex mechanisms such as the electron exchange and oxygen formation in the Fermi-level pinning effect might also have some critical impacts and need to pay more attention. Consequently, it is necessary to consider the majority and the minority carriers injected form both ways of Si-substrate and gate electrodes together in order to approach the truly physical mechanisms.

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國立交通大學電子研究所博士班

（92 年 9 月～98 年 1 月）

博士論文題目：

高介電係數閘極介電層在金氧半電晶體中之電特性及其可靠度研究

A Study of Electrical Characteristics and Reliability in CMOSFETs with High-κ Gate Dielectrics

Publication List

(A) International Journal :

[1] **[2 點，長文]** **S. C. Chen**, J. C. Lou, C. H. Chien, P. T. Liu, and T. C. Chang, “An Interfacial Investigation of High-Dielectric Constant Material Hafnium Oxide on Si Substrate,” *Thin Solid Films*, 488, Issues 1-2, pp. 167-172, 2005.

[2] **[2 點，長文]** **S. C. Chen**, Y. Y. Chen, Y. T. Chang, J. C. Lou, K. T. Kin, and C. H. Chien, “Improvements of Ozone Surface Treatment on The Electrical Characteristics and Reliability in HfO_2 Gate Stacks,” *Microelectronic Engineering*, 84, Issues 9-10, pp. 1898-1901, 2007.

[3] **[3 點，短文]** **S. C. Chen**, C. H. Chien, and J. C. Lou, “Anomalous Negative Bias Temperature Instability Behavior in p-Channel Metal-Oxide-Semiconductor Field-Effect Transistors with $HfSiON/SiO_2$ Gate Stack,” *Applied Physics Lett.* 90, Issues23, pp. 233505-1 - 233505-3, 2007.

[4] **[2 點，長文]** **S. C. Chen**, C. H. Chien, and J. C. Lou, “Impact of Charge Trapping Effect on Negative Bias Temperature Instability in P-MOSFETs with $HfO_2/SiON$ Gate Stack,” *Journal of Physics*, 100, pp. 042045-1 - 042045-4, 2008.

(B) International Conferences :

[1] **S. C. Chen**, J. C. Lou, C. H. Chien, P. T. Liu, and T. C. Chang, “The Interfacial Investigation of High-κ Material Hafnium Oxide on Si Substrate,” *International Conference on Metallurgical Coatings and Thin Films*, p. 65, San Diego, California, USA, April 19-23, 2004.

[2] **[1 點，國際研討會] S. C. Chen**, Y. Y. Chen, B. H. Ji, C. F. Yeh, J. C. Lou, and C. H. Chien, “Effects of SiN Capping Layer on NMOSFETs with HfO_2/SiON Gate Stack,” *International Electron Devices and Materials Symposia*, pp. 254-255, Tainan, Taiwan, December 7-8, 2006.

著作總點數：**10** 點 **(依新法計算)**