Chapter 1
Introduction

1.1 Overview of Transistors for RF Applications

Currently, the communication systems transmit, process, and receive great amounts of data in very short time intervals and operate in the GHz range. Microwave transistors are the backbone of these modern wireless communication systems, and the widespread use of mobile phones in recent years created the real mass market for microwave transistors. Microwave transistors are used in a large number of different circuits such as low-noise amplifiers, power amplifiers, mixers, frequency converters and multipliers, attenuators, and phase shifters. Although the requirements on transistor performance differ from application to application, microwave transistors in principle can be distinguished into two groups as small-signal low-noise transistors and power transistors. For microwave electronics, on the other hand, a large variety of different semiconductor materials have been employed, such as Si, SiGe, GaAs, InP, further III-V compounds, and wide bandgap materials.[1-4]

In recent years, silicon-based microwave transistors (such as SiGe HBTs and CMOS) have attracted much attention due to their optimization work for cost and performance. Unlike compound semiconductor technology, a silicon-based technology derives its advantage by its ability to integrate various functions on a single chip (system-on-a-chip; SOC), thereby reducing cost.

1.2 Issues on SiGe Hetero-junction Bipolar Transistors

SiGe BiCMOS technologies provide cost-effective solutions that can meet power-performance requirements set by various products. The value proposition of a SiGe BiCMOS is that the CMOS devices are compatible to a foundry offering to enable the reuse of logic libraries and layout cells. At the heart of the market success of SiGe BiCMOS is the ease of integration of high-performance SiGe HBTs with the state-of-the-art CMOS and passive elements.

1.2.1 Basic Concept of Hetero-junction Bipolar Transistor

The SiGe Hetero-junction Bipolar Transistor (HBT) is a bipolar transistor with a basic structure similar to that of a Si BJT, as shown in Fig. 1.1, and with an additional material of SiGe in the base layer. Like the BJT, it has three terminals, namely emitter, base, and collector, and consists of either an npn or pnp layer sequence. The main difference between the two devices is that in HBTs, the emitter and the base are made of different materials, with the bandgap in the emitter being larger than that in the base. Thus, the emitter-base junction of HBTs is “hetero-junction”. As mentioned above, the basic structure of HBTs is similar to that of BJTs. While the BJT consists of only one semiconductor material (Si), the HBT is formed of layers of different semiconductor materials. HBTs can be either single hetero-junction bipolar transistors (SHBTs) or double hetero-junction bipolar transistors (DHBTs). To the topic here, for SiGe HBTs, not only the base and the emitter are made of different materials but also the base and the collector, thereby SiGe HBT is unconditionally belonging to a double one.

HBTs can be further classified into the spike HBT, which has a spike conduction band at the emitter-base hetero-interface, and the smooth HBT, which has a smooth band at the emitter-base hetero-interface. In general, SiGe HBT is of the second kind. Most HBTs are formed with materials having the same lattice constant, and the hetero-junctions are lattice-matched. In SiGe HBTs, however, the SiGe base is a strained layer because the lattice constant of SiGe is larger than that of Si. Finally, an HBT can either be a npn or pnp transistor. Because almost all HBTs are of the npn type, the remaining discussions in the following sections will be focused on npn HBTs.[5]

1.2.2 Physical Improvements of HBTs

The hetero-structure effect exploited in HBTs can be explained based on Fig. 1.2. The key part of an HBT is the emitter-base hetero-junction with the bandgap of the emitter being larger than that of the base. Because of the different bandgaps and the resulting bandgap difference ΔE_G, electrons moving from the emitter to the base encounter a smaller energy barrier to be surmounted than holes traveling from base to emitter. Thus hole's injection from the base into the emitter is strongly suppressed, and higher current gains compared to those in homo-junction BJTs can be obtained. The emitter injection efficiency β of an HBT describes the ratio of the desired electron injection to the undesired hole-injection at the emitter-base junction. It is connected to the current gain and obeys the relation (for a smooth hetero-junction):

$$\beta \propto \frac{v_b^e N_e \exp(\frac{-E_e}{k_B T})}{v_e^h P_b \exp(\frac{-E_h}{k_B T})} \propto \frac{N_{DE}}{N_{AB}} \exp(\frac{\Delta E_G}{k_B T}) \qquad (1\text{-}1)$$

,where N_{DE} and N_{AB} are the emitter and base doping concentrations, k_B is the Boltzmann constant, and T is the absolute temperature in the device. In equation (1-1), it is clear that the potential barrier for electrons is smaller than that for holes by ΔE_G. Thus, the undesired hole-injection from the base to the emitter is effectively suppressed and an acceptable current gain can be obtained, even if the base doping is equal to or higher than the emitter doping. This offers the device engineer a new degree of freedom in transistor design. Large emitter-injection efficiency automatically leads to a large common-emitter current gain β_0, and HBTs with current gains of several thousands can be easily realized.

However, a very large current gain is typically not the primary design goal for microwave transistors. Instead, a more important issue is that an acceptable current gain is achievable with $N_{DE} << N_{AB}$, and the base doping concentration can be made very high. A high doping density in the base layer is desirable for microwave transistor operation. First, it allows for a very thin base without running the risk of having base punch-through. A narrow base, in turn, leads to a small base transit time and thus to a high cutoff frequency. Second, the high doping density in the base layer leads to a small intrinsic base resistance R_{Bi}, which gives rise to a high maximum frequency of oscillation and an improved high-frequency noise performance. A low emitter doping density is also beneficial for high-speed operation. It leads to a smaller emitter-base space-charge region capacitance and therefore a smaller emitter-base delay time τ_{EB}. To take the above-mentioned advantages, HBTs frequently employ a base doping density exceeding the emitter doping density. The material composition in the base may be either homogeneous or graded. A graded material composition results in a graded bandgap in the base. If the bandgap is larger at the emitter-base junction and decreases toward the collector-base junction, a built-in field arises in the base which enhances the electrons transport across the base. Consequently, the base

transit time is reduced and the cutoff frequency is further increased. Like in the Fig. 1.3, the profile of the SiGe base is frequently graded with a small Ge content near the emitter-base junction and an increasing Ge content toward the base-collector junction. Therefore, the bandgap in the base decreases toward the collector junction and a built-in field exists. The built-in field acts as an additional driving force for accelerating the electrons passing across the quasi-neutral base toward the collector. So, the graded-profile of the SiGe HBT is indeed an improvement for the operating performance. [6-8]

1.3 Introduction to RF CMOS

Another silicon-based RF technology is the advanced CMOS technology. Thanks to the advanced exploitation of logic CMOS technologies, the scaling technique lets Si-FETs approach to a higher RF performance dramatically in recent years. RF CMOS technologies will be the optimal choice where the SiGe HBT performance is not fully required and cost is paramount.

In recent years, steady improvement in the RF performance of CMOS is linked to improvement in digital performance via scaling and innovation [9]-[13]. However, unlike SiGe HBTs where most analog/RF parameters improve with scaling, the CMOS transistor scaling presents challenges for analog/RF designs. In this section, we will review some electrical parameters of interest in MOSFETs and how they evolve as digital CMOS shrinks.

Firstly, transconductance (g_m) which is benefited from the advanced scaling technology is the main factor of CMOS. In saturation operation, it can be shown that g_m is inversely proportional to the gate length (L_{gate}) and effective gate dielectric thickness (t_{ox}). In addition g_m is also influenced by the source drain series resistance

(R_{ds}). For short channel FETs in the velocity saturated regime, drain current (I_{dsat}) per unit device width can be approximated as $I_{dsat} = C_{ox} V_{sat}(V_{gs}-V_t)$, where C_{ox} is the effective gate capacitance and V_{sat} is the carrier velocity. As a result g_{msat}, stated as $v_{sat}\varepsilon / t_{inv}$ has been strongly increasing with scaling but will be challenged as the gate dielectric thickness scaling slows down due to leakage considerations. For RF designers, the relatively lower self-gain (g_m/g_{ds}) in scaled CMOS technology presents a challenge. For short channel device, g_{ds} is related to drain induced barrier lowing (DIBL) which results from electric field at the source side of the FET under conditions of high drain bias. Basically, g_{ds} is proportional to V_{DS}/L_{gate} and is slightly increasing with scaling, since L_{gate} is reducing faster than VDD. However, g_{ds} depends on the geometry design for RF CMOS, especially on the finger numbers and its single finger width. In advanced CMOS technologies, gate leakage restricts the scaling of oxide thickness so that L_{gate} and t_{ox} can not reduce proportionally. This results in a precipitous drop in the self-gain. Of course, methods to overcome such issues were developed in many literatures and by foundry engineers [14]-[18].

Finally, as to RF main figures-of-merit (FOM), a simple indicator of performance gains with scaling is the increase in f_T which can be shown to be proportional to the inverse of gate length (L_{gate}) in velocity saturation limit. A more comprehensive indicator of usable power gain of the transistor is its f_{MAX}. RF nFETs can deliver unilateral gain comparable to the SiGe HBTs [19]-[21] with less power consumed in the device.

1.4 Motivation

Recently, SiGe HBTs have attracted much attention for RF power applications

because of their excellent microwave power performance and thermal conductivity. By optimizing the device process, the microwave power applications of SiGe-based HBT under development have move from L-, S-, and C-band operations to X-band operation. However, due to the high electric field at the base-emitter junction caused by high doping levels of SiGe HBTs, the hot-carrier (HC) reliability has become a major concern for such advanced devices used in commercial products [22]-[24]. So, it is worth investigating the effects of hot-carrier on the high-frequency and especially on the RF power performances of SiGe HBTs. Most literatures on HC effects deal mainly with the dc characteristics and/or the low-frequency noise behavior. In this thesis, we investigate hot-carrier effects on the degradations of high-frequency application and for "the first time" on "RF power" characteristics of SiGe HBTs with different bias conditions.

As well as the RF reliability of SiGe HBTs, RF CMOS technologies also suffer from the reliability issues for their products. With the scaling MOS transistor technology, the hot-carrier reliability becomes an important concern while keeping a relatively high drain voltage for both the digital and analog applications. Hot carrier generation and its effects on the characteristics of MOS transistors have been known for a long time. Research workers have been discussing reliability issues on RF behaviors of MOS transistors, especially on the degradation of S-parameters (scattering parameters), and the RF FOM like cut-off frequency and maximum oscillation frequency. However, RF performances of advanced MOS transistors are concerned to the power delivery from the input source to the output load, and it might be interesting and should be considered as well. In our thesis, we also addressed the reliability issues including the hot-carrier and gate oxide dielectric breakdown on MOS transistors from DC to AC behaviors, especially extended to the RF power performance.

1.5 Thesis Organization

The content in this thesis includes the following parts.

Chapter 1 introduces the silicon-based transistors for RF applications. We also review the performances of SiGe HBT and MOS transistor, individually. Then is the motivation of our thesis.

In Chapter 2, we introduce the concepts of main issues in the electric parameters of silicon-based transistors. Basic concepts of degradation mechanisms for RF reliability of SiGe HBT and MOS transistor are also addressed in this chapter.

Chapter 3 presents the electrical stress effects on the high-frequency and RF power performances of SiGe HBTs. The hot-carrier stress is applied by a so-called OC stress (reversed emitter-base junction, and open collector). We discuss the hot-carrier effects on RF characteristics of SiGe HBTs, especially the RF power behaviors.

Chapter 4 presents a new electrical stress effects on SiGe HBTs. Simultaneously applying a high collector current density and a high collector-base voltage on SiGe HBTs, the hot carrier will be induced to degrade the device performance. This stress condition is like the DC bias conditions of a current source RF power amplifier, and is termed as a “mixed-mode” stressing.

In Chapter 5, we discuss the reliability issues on the high-frequency characteristics of advanced RF CMOS. The hot-carrier effects and oxide breakdown on the RF figures-of-merit, and RF noise performance are addressed in this chapter. A modified small-signal model was also constructed to explain the mechanism of reliability issues.

In Chapter 6, we examine the power characteristics of MOS transistors under the

hot carrier stressing and critical gate-oxide breakdown. In addition, the influence of stress on the device linearity is also addressed in this chapter.

Finally, the conclusions of this thesis are given in Chapter 7.

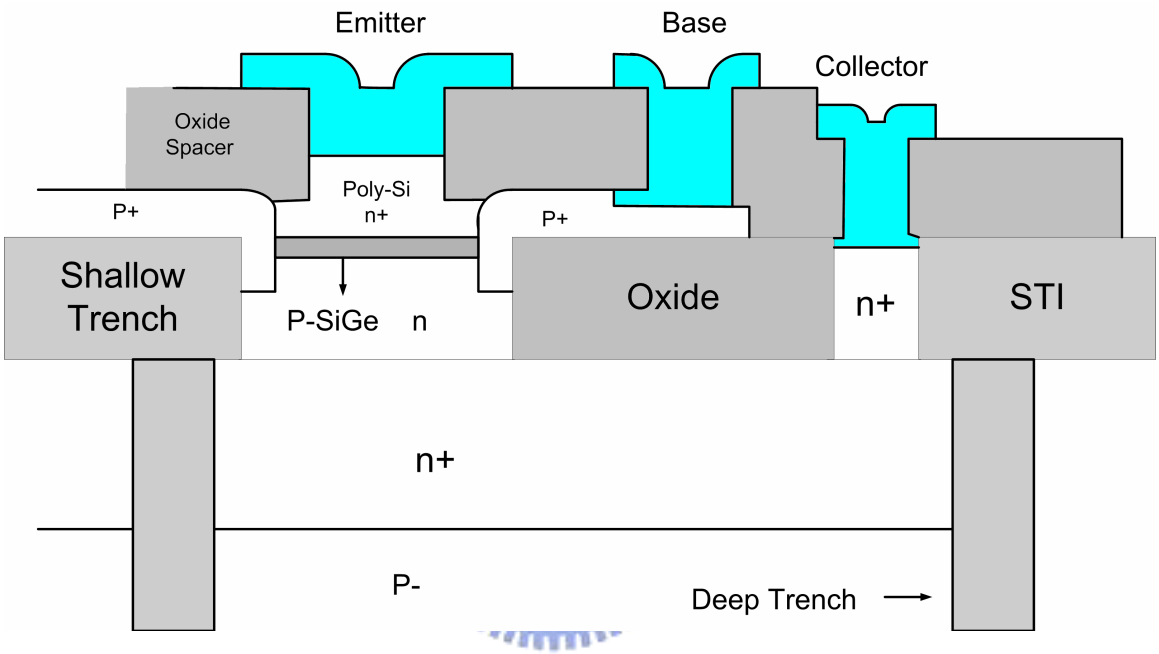


Fig. 1.1 Cross-section of a typical Si/SiGe HBT.

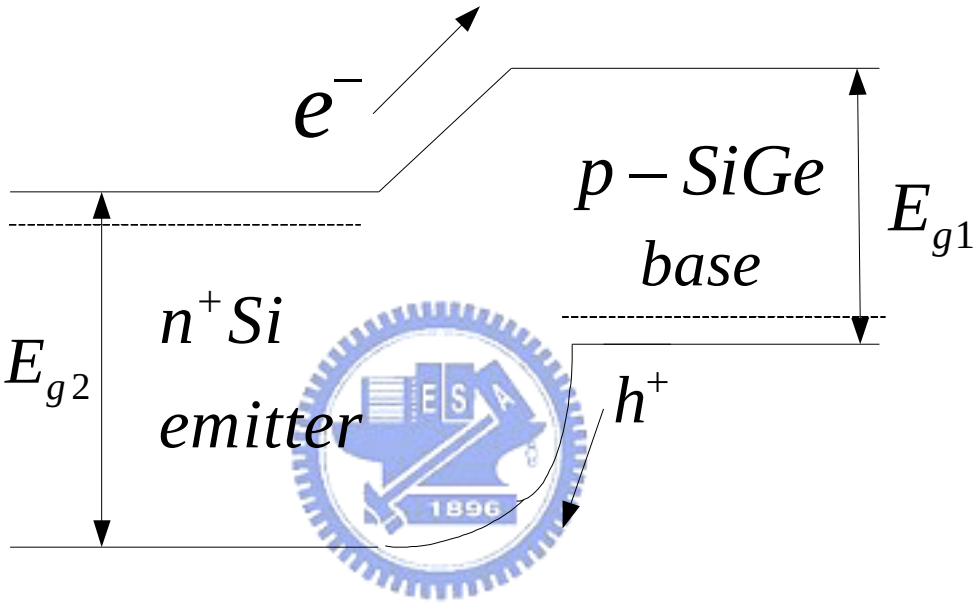


Fig. 1.2 The bandgap diagram of emitter and base junction in SiGe HBTs

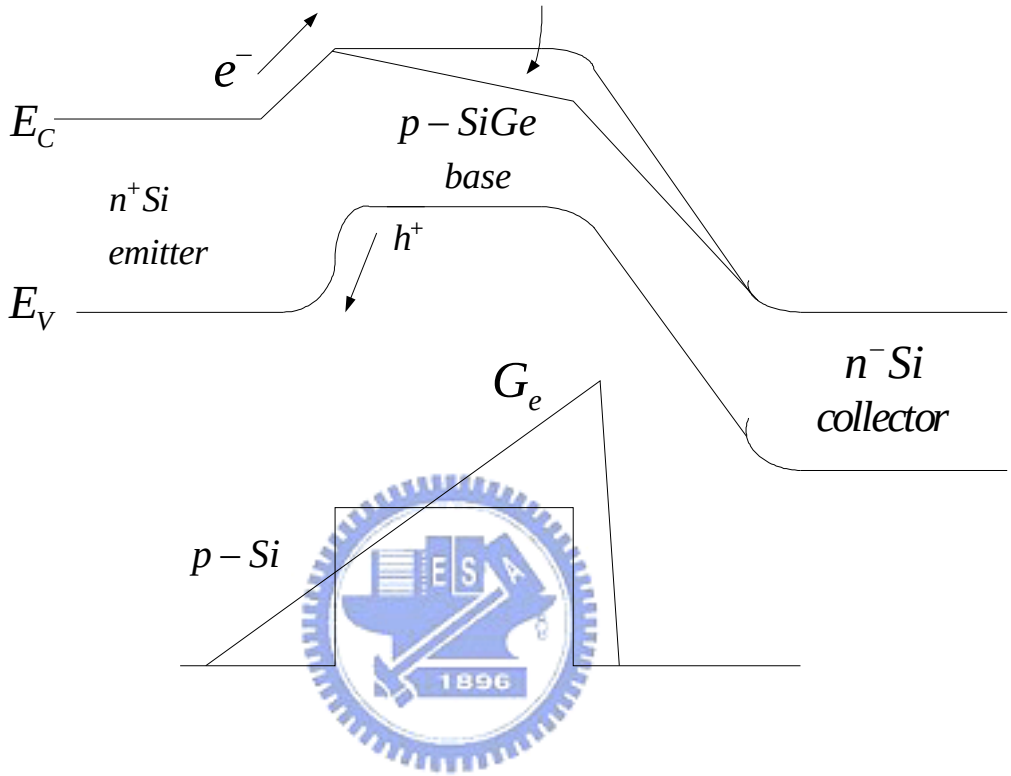


Fig. 1.3 The bandgap in the base decreases toward the collector junction and a built-in field exists.

Chapter 2
Reliability Degradation Mechanisms in Si-Based Transistors

2.1 Introduction

Clearly, any device technology (Si-based or otherwise) being sold in the commercial market must be proven to be "reliable." That it is, under typical circuit operating conditions, the circuits, and importantly, the systems constructed from those circuits, must not wear out or degrade to a level at which they fail in the field over the functional life of the system. In integrated circuit circles, reliability of a given technology begins with assurance not only of the underlying building block devices; the active transistors certainly, but also passive elements like inductors or capacitors, and interconnects linking the various elements. For brevity, in this chapter we will focus on the main issues of the silicon-based transistors: SiGe HBT reliability and CMOS reliability.

2.2 Reliability Issues on Si/SiGe Bipolar Transistors

From a transistor perspective, one ensures adequate reliability by subjecting the devices to extreme operating conditions for a given length of time, which, for a "bipolar" technology, historically encompasses two different operating scenarios: (1) hot-carrier (hot electron or hot holes or both) stressing associated with "reversed biasing of the emitter-base (EB) junction, and (2) high forward collector current

density (J_C) stressing. Both reliability "modes" will generally be conducted under "accelerated" conditions or so-called "overstress" consisting of higher emitter-base voltage (V_{EB}) and J_C than the device would normally encounter during "typical use" circuit conditions, and will likely be performed at either elevated or reduced temperatures to invoke worst-case stress conditions. Recently, a new reliability damage mechanism in SiGe HBTs was reported, which was termed as "mixed-mode" degradation, since it results from the simultaneous application of high J_C and high collector-base voltage (V_{CB}), and which differs fundamentally from conventional bipolar device reliability damage mechanism associated with either reverse emitter-base stress, or high forward current density stress.

2.2.1 Reverse Emitter-Base Junction Stressing (OC Stress)

Hot-carrier degradation under emitter-base reverse-bias stress is one of the major reliability concerns in bipolar transistors. Emitter-base reverse-bias stress with an open-collector is often used in determining the time-to-failure (TTF) of a transistor. TTF is defined as the time it takes after accelerated stress to decrease the common-emitter current gain, β, by 10% at a certain base-emitter voltage (e.g., 0.8 V). An accurate and rapid TTF methodology is desirable to monitor new device technologies and designs during development. The conventional accelerated stress scheme which is called the voltage-accelerated stress or open-collector stress (OC stress) uses a stress voltage much higher than the normal operating voltages [25], [26].

Under OC stress, the emitter reverse current is dominated by the tunneling of the valance band electrons in the p-base into unoccupied conduction band states in the n^+ emitter [27]. The tunneling occurs mainly at the peak electric field location in the

device at the emitter edge, because the tunneling rate is a strong function of the local electric field. It indicates the peak electric field occurs close to the emitter edge in the emitter-base space charge region. The tunneling electron leaves behind a hole and this hole is then accelerated by the applied emitter-base reverse-bias, $V_{EB\text{-}stress}$, as shown in Fig. 2.1. Figure 2.1 shows the schematic band diagram of an npn transistor under OC stress (emitter-base junction reverse bias and collector left open). The high-energy holes move in parallel with and adjacent to the SiO_2/Si interface toward the p-base boundary of the emitter-base space charge region, causing device performance degradation by generating interface traps at the oxide-silicon interface. Thus, under OC stress, the performance degradation in a device is mainly owing to hot holes. The kinetic energy of those hot holes is $qV_{EB\text{-}stress}$ since the holes are accelerated by $V_{EB\text{-}stress}$ [26].

2.2.2 Forward Collector-Base Junction Stressing (FC Stress)

Another accelerating stress method is the forward-collector stressing (FC) achieved at low reverse EB voltage and high forward-current density. Fig. 2.2 shows a schematic band of an npn transistor with emitter-base junction reverse biased and collector-base junction forward biased (FC stress) drawn through the peak electric field at the device periphery [26], [28]. Forward biasing the collector-base junction injects electrons into the base thus making the hot electron current dominate over tunnel-injected and space charge region (SCR) accelerated hot hole current. The injected electrons get accelerated toward the conduction band of the emitter by a voltage equal to $V_{EB\text{-}stress} + V_{EB\text{-}bi}$. The kinetic energy of the hot electrons is thus approximately $q(V_{EB\text{-}stress} + V_{EB\text{-}bi})$. The FC stress methodology makes a fundamental assumption that hot electrons and hot holes with the same kinetic energy dependence

generate the same number of traps. This assumption served as the original basis for using FC stress to mimic OC stress. In [29]-[32], some literatures have examined the validity of this assumption in UHV/CVD SiGe HBT's by comparing the degradation in dc current gain and low-frequency noise by hot electrons and hot holes. Although the FC stress method can mimic OC stress for acceleration, the mechanisms of degradation by hot electrons and hot holes in FC and OC stresses are different [25]-[29]. In addition, as to the SiGe HBTs which is improved in a higher performance than typical Si BJT by adding the Ge content, literatures also addressed that either the shape or the position of the Ge profile in the base of a SiGe HBT, it has no significant impact on reliability [33]. The similar degradation in base current seen in both Si and SiGe devices indicates that trap generation processes are the same in both the devices.

2.2.3 Mixed-Mode Stressing (MM Stress)

A new reliability damage mechanism in SiGe HBTs was recently reported [34], [35], which was termed as "mixed-mode" degradation. By simultaneously applying a high J_C and high V_{CB}, the mixed-mode stressing is like the actual bias application for real products. To carefully control the total injected charge during mixed-mode stressing, a robust time-dependent stress methodology was used which operates the transistor in common-base mode under variable forced I_E and V_{CB} conditions. The band diagram under mixed-mode stressing is shown in Fig. 2.3. The mixed-mode stressing produces interface traps at both the emitter-base spacer, and the shallow-trench edge and subsequent generation and recombination (G/R) base leakage current. The base current leakages were observed from the forward and reverse gummel-plots in [34], [35]. For both the emitter-base spacer and shallow-trench

damage regions, it was found that injection current density is clearly present and dominated by hot electrons (hot holes exit but in smaller numbers).

2.3 Reliability Issues on MOS Transistors

2.3.1 Hot Carrier Mechanism

Hot Carriers are a result of the high electric fields inside the MOSFETs when high biasing voltages are applied to a short-channel length device. Electrons in the inversion layer can get high energies in the high electric field. It is possible that carriers with high energy (i.e. hot carriers) have sufficient energy to overcome the potential barrier between the silicon and silicon dioxide and penetrate into the gate oxide. Some of them may get stuck inside the gate oxide at the defect sites or traps, denoted by N_{ox}. Hot carriers also can break the atomic bonds at the interface of the silicon substrate and the gate oxide and generate new traps which are called interface traps, denoted by N_{it}. The difference between these two types of traps is that interface traps can be in charge exchange with channel whereas the oxide traps cannot be in direct charge exchange with charges in the channel. These two types of traps will degrade the quality of gate oxide and affect the device electric parameters.

As shown in Fig. 2.4(a), when the MOSFET is operated in the saturation region, the channel electrons will gain high energy on their way from source to drain and penetrate into gate oxide. The hot carriers are called channel hot electrons (CHE). The event of a carrier gaining energy and entering the gate oxide is a statistical phenomenon. The maximum numbers of hot carriers which penetrate into gate oxide occur when $V_G \cong V_D$ [36].

Another effect that can be caused by energetic carriers in the channel is that

carriers on the way toward drain collide with lattice atoms and generate new electron-hole pairs. These electron-hole pairs can also gain high energy in the electric field and produce new electron-hole pairs, similar to avalanche process in a reversed biased p-n junction. This process is called drain avalanche hot-carriers (DAHC), which is shown in Fig. 2.4(b). During the same process, the energetic carriers can impinge on the atomic bonds at the interface of the substrate and gate oxide or inside the oxide, and break them. Therefore new electronic states N_{it} are created at the interface. In an NMOSFET, the extra electrons generated in avalanche process are absorbed by drain, and the extra holes are absorbed by substrate terminal which form the substrate current component (I_{sub}). It is known that generation of electron-hole pairs in an avalanche process is proportional to both strength of electric field and the number of primary carriers initially flowing in the channel. For low values of gate voltage (V_G) above the threshold, the transistor is in deep saturation and a pinch-off region is formed near the drain which results in a strong lateral electric field in that region. Also at low values of V_G the drain current is low. As V_G increases, the drain current (I_d) increases, but transistor comes out of saturation region gradually. This causes that a maximum value for I_{sub} appears at some particular value of V_G. It is reported that at $V_G \cong \frac{1}{2}V_D$ the maximum I_{sub} is generated in MOSFETs [37].

The third mechanism of hot carriers is called substrate hot electrons (SHE). Unlike the cases of CHE and DAHC, which were caused by lateral electric field in the channel, SHE is caused by the vertical electric field between gate and the substrate. As shown in Fig 2.4(c), the electrons which are thermally generated in the region below the gate, drift toward the silicon-silicon dioxide interface and gain kinetic energy in the electric field below the gate. Some of these electrons penetrate into oxide and cause a uniform distribution of trapped charge in the oxide. SHE is not a

major problem in short channel devices as most of the electrons are absorbed into source and drain region and a smaller fraction of them reaches the device surface, compared to the long channel devices.

2.3.2 Critical Gate-Oxide Breakdown Mechanism

Generally, in advanced MOS devices, there are two breakdown mechanisms observed in gate dielectric materials. One is called HBD (Hard-Breakdown) and has a permanently distortion in gate oxide dielectric. It results in a dramatic increase of the output currents due to the increasing gate leakage current. The other breakdown mechanism is called SBD (Soft-Breakdown), and the breakdown process shows smoothly and slightly. The physical mechanism involved in, and leading to, the dielectric breakdown process are very complex. They involve impact ionization in the oxide layer, injection of holes from the anode, creation of electron-hole pairs in the oxide, electron and holes trapping, creation of surface state at the oxide-silicon interface, and the interaction of many or all of these processes.

The mechanism of tunneling into an electron trap can be explained by Fig. 2.5(a). As electrons tunnel into an oxide layer, some of the electrons can get trapped. The trapped electrons modify the oxide field so that the field near the cathode is decreased, while the filed near the anode is increased. Hence the tunneling current will reach a stable value in Soft Breakdown.

As electrons travels in the conduction band of an oxide layer, it gains energy from the oxide filed. If the voltage drop across the oxide layer is larger than the band-gap energy of silicon dioxide, the electron can get enough energy to cause impact ionization. As shown in Fig. 2.5(b), when a tunneling electron arrives to the anode, it could cause impact ionization in the anode near oxide-anode interface.

Depending on the energy of the tunneling electron, the hole thus generated could be from deep down in the valence band, and thus could be “hot”, a hot hole in the silicon–oxide interface can have a high probability of been injected into oxide layer. On the other hand the injected hole can be trapped in the oxide layer as it travels towards the cathode.

The trapped holes in the oxide layer caused an increase in the oxide field near the cathode and a decrease in the oxide field near the anode. This could be illustrated in Fig. 2.5(c) which is according to the F-N tunneling. A small increase in the oxide field near the cathode can cause a large increase in the tunneling current. Thus, hole-trapping in the oxide near the cathode provides positive feedback leading to the electron tunneling process. Dielectric hard breakdown occurs when the positive feedback leads to a run away of the electron tunneling current at some local weak spots of the oxide [38]. It appears as a current prominence in current-versus-time plots.

2.4 Summary

In this chapter, we introduce the reliability degradation mechanisms in SiGe HBTs and MOS transistors. Firstly, in addition to two general hot-carrier stressing methods in SiGe HBTs (OC stress and FC stress), we also address a “mixed-mode” stressing method, where the stress conditions approach to the real bias conditions of products. Moreover, critical gate dielectric breakdown is an important reliability issue on advanced MOS transistors. We also examine the basic physical mechanisms of gate oxide breakdown. Those effects on the RF characteristics of transistors will be discussed in the following chapters.

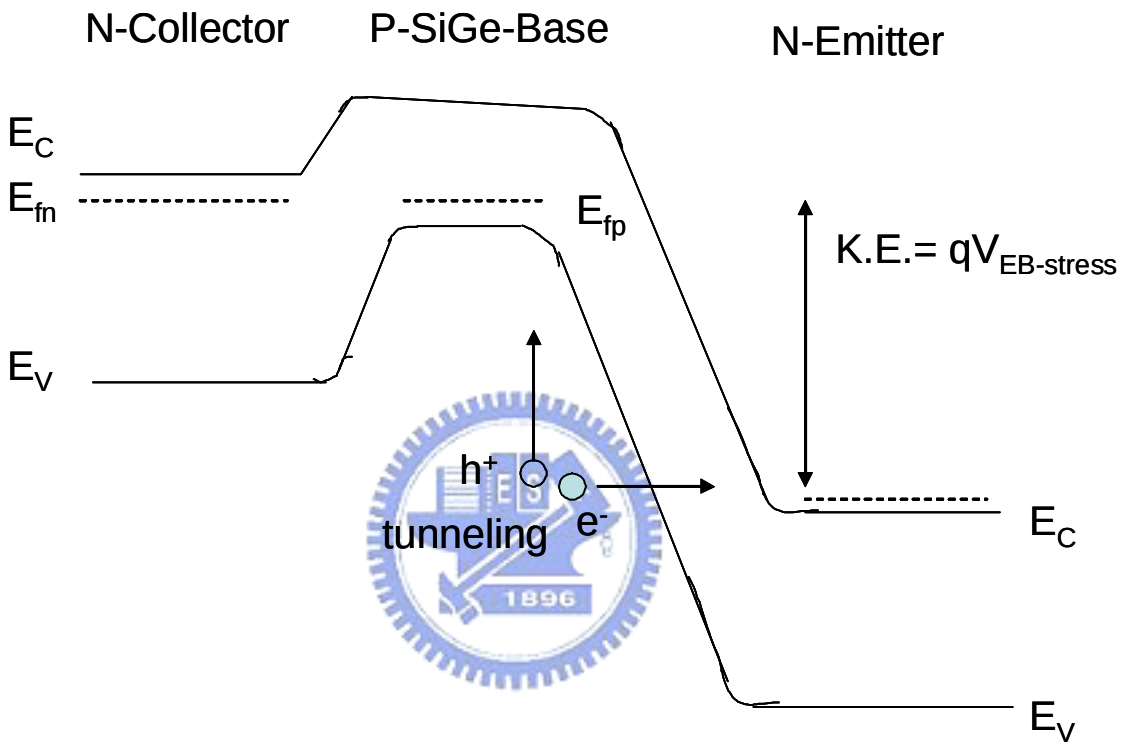


Fig. 2.1. The band diagram of an npn-Si/SiGe HBT under OC stress

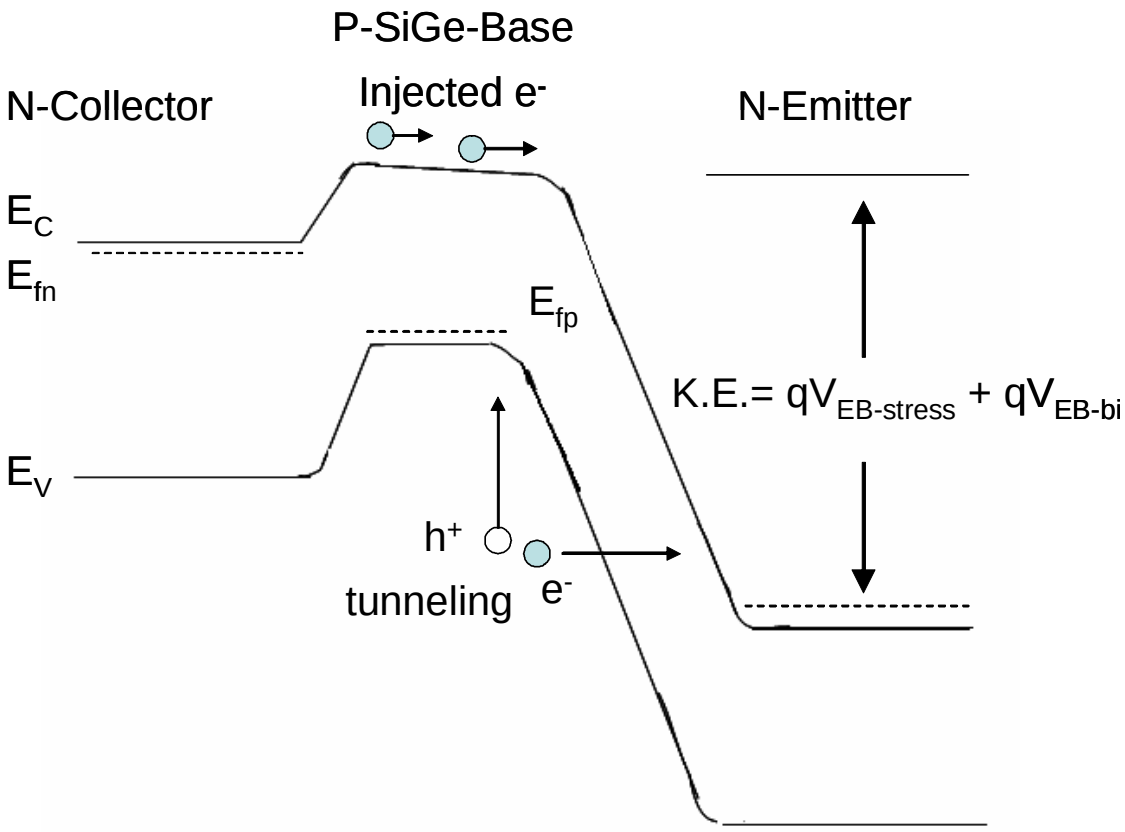


Fig. 2.2. The band diagram of an npn-Si/SiGe HBT under FC stress

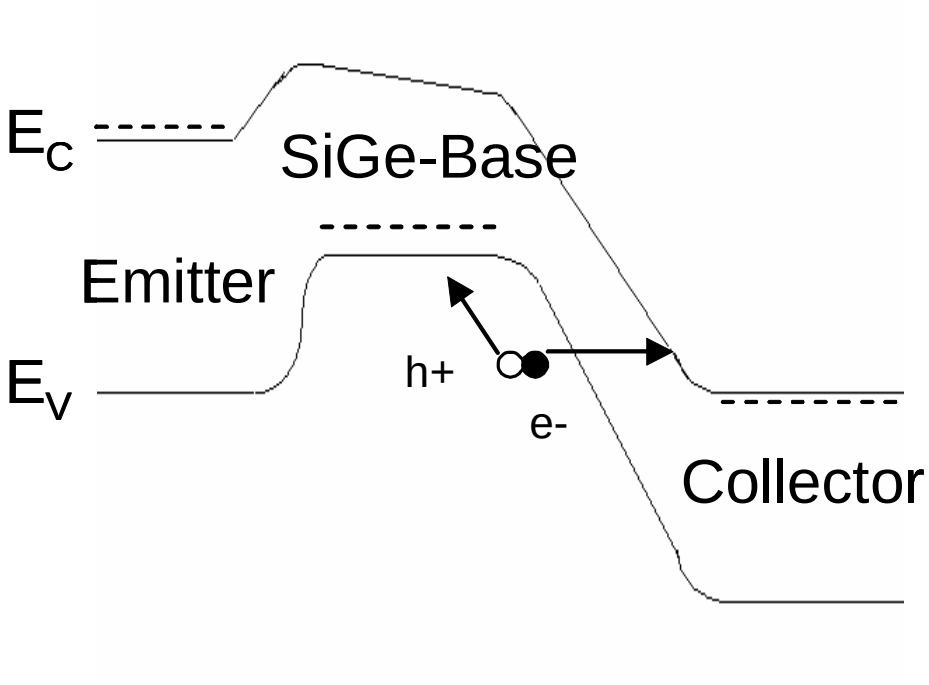
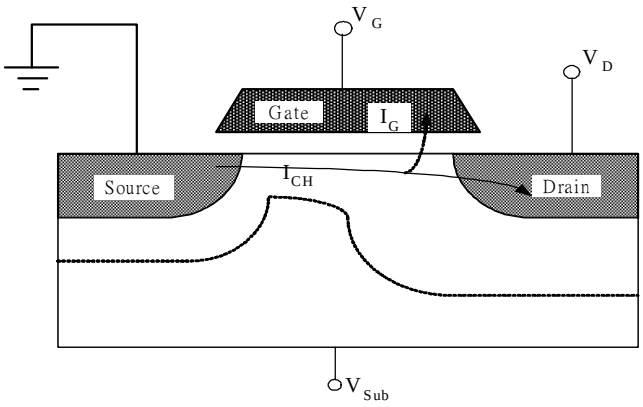


Fig. 2.3. The band diagram of an npn-Si/SiGe HBT under MM stress



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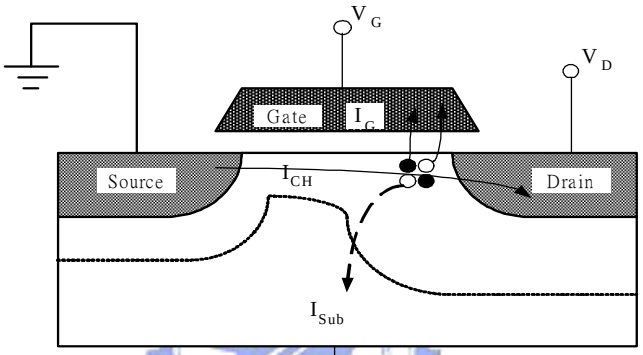

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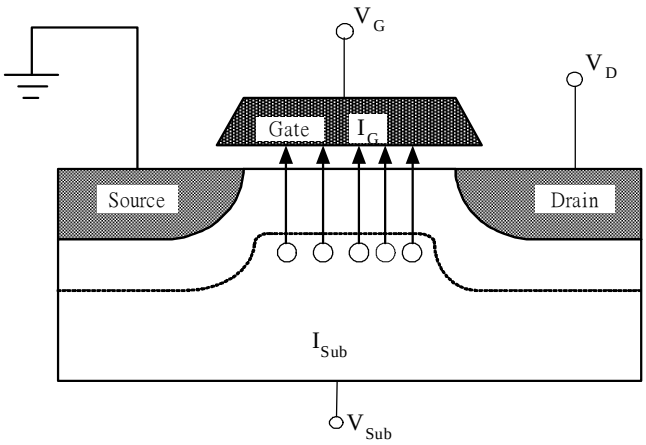

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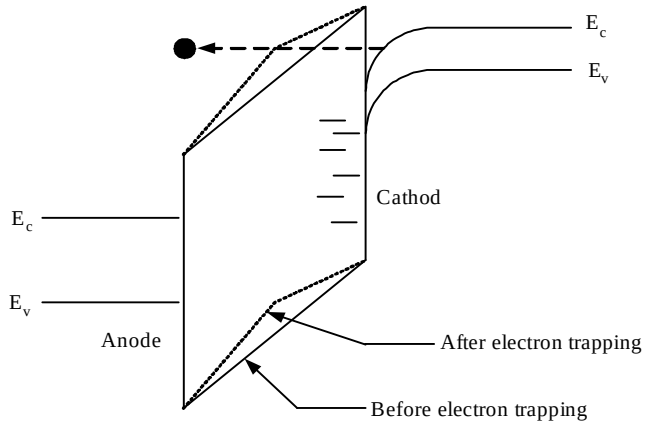
Fig. 2.4: (a) Channel hot electrons (b) Drain avalanche hot carriers (c) Substrate hot electrons



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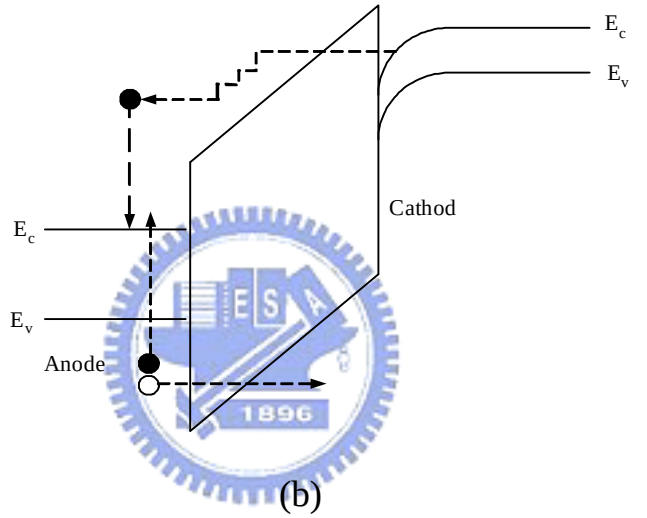

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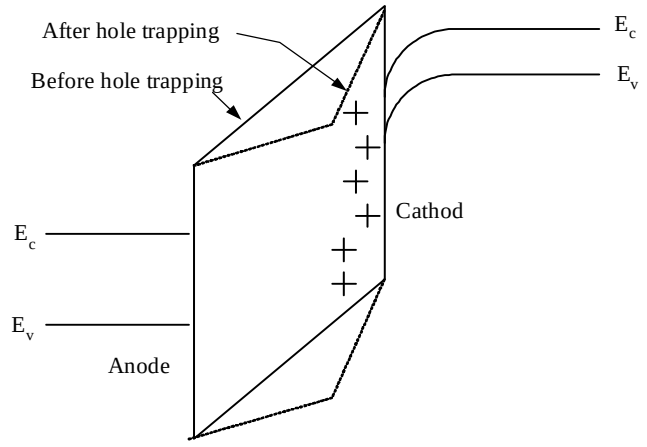


(c)

Fig. 2.5: (a) Schematic illustrating the trapping of tunneling electrons. (b) Schematic illustrating the generation of an electron-hole pair in the anode by a tunneling electron. (c) Schematic illustrating the trapping of holes in the oxide layer.

Chapter 3
Electrical Stress Effects on SiGe HBTs for High-Frequency Applications

3.1 Introduction

With recent technology advancements that push cutoff frequency and maximum oscillation frequency over 200GHz [39], [40], Si/SiGe heterojunction bipolar transistors (HBTs) have become viable candidates for most microwave applications. It is known that SiGe HBTs are suited ideally for large-volume manufacturing of RF transceiver systems at and beyond 2.4GHz, at which the silicon homojunction technologies lack performance and where SiGe HBTs provide higher integration levels than III-V component technologies. Recently, SiGe HBTs have attracted much attention for RF power applications because of their excellent microwave power performance and thermal conductivity.

Due to the high electric field at the base-emitter junction caused by the high doping levels of SiGe HBTs, the hot-carrier (HC) reliability has become a major concern for such advanced devices used in commercial products [41]-[43]. So it is worth investigating the effects of hot-carrier on the high-frequency and RF power performances of SiGe HBTs. However, the most literatures on HC effects deal mainly with the dc characteristics and/or the low-frequency noise behavior [44]-[46], and seldom addressed the RF characteristics [47], [48]. In this chapter, by a using a small-signal model under classical OC stress (reversed emitter-base junction, and open collector), we systematically investigate hot-carrier effects on the degradations

of high-frequency and RF power characteristics of SiGe HBTs with different bias conditions.

3.2 Hot-Carrier Effects on High-Frequency Performance

Firstly, the test-chips we used in this work are multi-finger Si/SiGe HBTs fabricated with a typical 0.24 μm high-voltage SiGe HBT process. The devices feature an emitter-width of 1 μm and emitter-length of 32 μm with 4 strip-fingers. DC current gain is up to 181 and the BV_{CEO} is 5.3V. The cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) are about 23GHz and 40 GHz, respectively. In order to discuss the electrical stress effects, the hot-carrier stress was carried out by applying a reverse-biased base-emitter voltage (V_{EB}) of 3.5V up to 1000 seconds at room temperature, and with the collector left open. This so-called open-collector (OC) stress is conventionally used for time-to-failure prediction under reverse emitter-base stress. The band diagram of an npn-Si/SiGe HBT under such OC stress is shown in Fig. 3.1. Under OC stress, the emitter reverse current is dominated by tunneling of the valance-band electrons in the p-base region into unoccupied conduction band states in the n^+ emitter. As a result for the electrical performance, the Gummel plot of a typical SiGe HBT measured before and after hot-carrier stress is shown in Fig. 3.2(a). The main effect of HC stress on the dc characteristics is an increase of the non-ideal base current and leaving the collector current unaffected, thus resulting in a degradation in the current gain of the transistor. In the inset of Fig. 3.2(a), the emitter-base junction reversed bias is approaching to the junction breakdown voltage in order to enhance the hot-carrier occurrence. Hot-carrier degradation under emitter-base reverse-bias stress is one of the major reliability concerns in bipolar transistors. Reverse-biasing the emitter-base junction develops a very high electric field across the emitter-base

junction, thus accelerating electrons and holes to very high velocities. These high-energy or “hot” carriers generate interface traps at the sidewall-spacer oxide and silicon interface leading to an increase in the recombination component of the base leakage-current [49]. Therefore, the dc current gain is decreased after the hot-carrier stressing as shown in Fig. 3.2(b).

Since the current gain is reduced after HC stress, the high frequency and power characteristics of the transistor should be affected as well. In addition, due to the different responses of base and collector currents under stress as shown in Fig. 3.2, the comparison of microwave properties under HC stress will be taken by constant base-current and constant collector-current measurements.

Figure 3.3 shows the HC stress effects on the S-parameters of a transistor with different bias measurements. The frequency range is from 0.1 GHz to 20 GHz. The S-parameters are the most important parameters, which are widely used for discussing the properties of microwave transistors [50]. In Fig. 3.3(a), we observe that S11 has a deviation under stress at low frequencies, it indicates the input impedance has been changed with HC stress. At 2.4 GHz, S11 has only a minor change as the collector current was kept constant, while S11 still has an obvious deviation as the base current was kept constant due to the reduction of the transconductance (g_m), which is resulted from the reduction of collector current. This phenomenon is different from that observation mentioned in ref [47], which showed the S11 has no changes under stress regardless of whether the base or the collector current was kept constant. When applying a simple equivalent hybrid-π model in our work, we can directly extract the intrinsic element values (see Table I) from the HBT S-parameters after de-embedding the extrinsic parasitic. Additionally, from the S-parameters of HBT, we can translate those matrixes to y-parameters for convenient extraction. We now evaluate the y-parameters using this simplified small-signal equivalent circuit shown in Fig. 3.4.

For simplicity, we assume that r_b is negligibly small compared to the input impedance of the intrinsic transistor, which holds for RF frequencies of interest. The y-parameters are rapidly obtained by examining the small-signal *I-V* relation,

$$Y_{11} = \frac{g_m}{\beta} + jw(C_\pi + C_u) \tag{3.1}$$

$$Y_{12} = -jwC_u \tag{3.2}$$

$$y_{21} \approx g_m \tag{3.3}$$

$$y_{22} = jwC_u \tag{3.4}$$

,where $g_m = I_C/qkT$. Here, C_π consists of the EB depletion capacitance, and the EB diffusion capacitance. C_u is the total CB junction capacitance.

After HC stress, the dynamic base resistance (r_π) referred to the SiGe HBT increases from 72Ω to 83Ω and reduces to 49Ω with the constant base-current and constant collector-current measurements respectively. The HC stress in base-emitter junction induces an increasing base current, and reduces the slope of the base current versus base-emitter voltage. Thus it increases the value of r_π for constant base-current measurement. On the other hand, as to a constant collector-current measurement, the r_π is reduced due to the increasing base-current. In addition, after HC stress, the base-emitter capacitance (C_π) shows a slightly change with the constant collector-current measurement, but a large variation with the constant base-current measurement. This is resulted from the reduction of the base-emitter diffusion capacitance under a constant base-current measurement. The changes of the r_π and C_π under stress are consistent with the variation of S11.

Since S22 is a function of output bias, the S22 of a transistor with constant

base-current measurement shows a large deviation after stress due to the reduction of collector current, while that with constant collector-current measurement is changed slightly, as shown in Fig. 3.3(b). Furthermore, with a constant base-current measurement, the increased output resistance (r_{out}) of the transistor can also validate this observation (see Table I). In Fig. 3.3(c), the S21, which represents the transformed gain of RF input signal, also exhibits a deviation after HC stress. Under a constant base-current measurement, the S21 deviation is larger than that under constant collector-current measurement due to the larger change of transconductance (g_m).

To validate the HC effects on the cut-off frequency (f_T) of the transistor, we calculated the small-signal current gain (h_{21}) from the S-parameters. Fig. 5 shows the effects of HC stress on the h_{21} versus frequency. When the transistor was measured at a fixed collector current of 52 mA, it can be seen that the magnitude of h_{21} decreases after stress at low frequency regime, while remains essentially unchanged for f > 1 GHz. The small-signal current gain h_{21} related to frequency (ω) in an equivalent hybrid-π model can be expressed as [44]

$$|h_{21}| = \frac{g_m r_\pi}{\sqrt{1+\varpi^2 C_\pi^2 r_\pi^2}} . \tag{3.5}$$

$$\text{When } w \to 0 \quad , \ |h_{21}| \cong g_m r_\pi = \beta = I_C / I_B \tag{3.6}$$

$$w \to \infty , \quad |h_{21}| = \frac{g_m}{\varpi C_\pi} \tag{3.7}$$

,and then

$$f_T \cong \frac{g_m}{2\pi(C_\pi + C_u)} \tag{3.8}$$

At low frequency regime, $|h_{21}|$ approaches to the dc current gain ($\beta \fallingdotseq g_m r_\pi$) expressed as (3.6), which will decrease under stress. The reduction of h_{21} at low frequency is consistent with the degradation of the dc current gain. However, at high frequency regime, $\omega^2 C_\pi^2 r_\pi^2 >> 1$, and the magnitude of h_{21} approaches to $g_m/\omega C_\pi$ in (3.7), so it shows unchanged after HC stress. On the other hand, for a constant base-current measurement as shown in Fig.3.5 (b), $|h_{21}|$ derivation occurs after stress over the entire frequency range. This is due to the reduction of collector current after HC stress.

Finally, the HC effects on the cutoff frequency (f_T) versus collector and base currents are shown in Fig. 3.6. It is shown that when the f_T is measured at constant collector currents, its values remain unchanged at low and medium currents, and only reduce slightly at high currents after stress (see Fig. 3.6(a)). On the other hand, when the f_T is measured at constant base currents, the stress-induced degradation of f_T is significant at low and medium currents, as shown in Fig.3.6 (b), due to the reduction of collector current as mentioned previously. In high current regime, where the Kirk effect might be occurred, because the device after stress has lower collector current at constant base-current measurement, it needs higher base current to enter the Kirk effect region. As a result, the measured f_T after stress is higher than that before stress. Since the normal device operation usually would not be biased in high current region, we can conclude that the constant collector current is a better bias condition than the constant base current to reduce the HC effect on the high-frequency performance.

3.3 Hot-Carrier Effects on RF Power Behavior

3.3.1. RF Power Characteristics

As well as the high-frequency characteristics, the microwave power characteristics are also affected by the HC stress. Fig. 3.7 (a) shows the effects of HC stress on the output power and power gain of a transistor measured at a fixed collector current of 52mA. The optimized matched source and load impedances are essentially unchanged after HC stress. After HC stress, the output power and power gain decrease slightly in the small input power regime, but show no noticeable change in the high power regime. For Class A operation, the linear power gain G_P, and power added efficiency (PAE) can be expressed as [51]

$$G_p = \frac{1}{8\pi C_{bc}(r_e + r_b + \pi f_T L_e)}\left(\frac{f_T}{f^2}\right), \tag{3.9}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \eta_C\left(1 - \frac{1}{G_p}\right) \tag{3.10}$$

where r_e is the emitter resistance, L_e is the emitter lead inductance, C_{bc} is the base-collector capacitance, and f is the operating frequency. In addition, in Eq. (3.10), the P_{DC} shows the dc-consumption power, and P_{out} and P_{in} present the input and output powers of the two port terminals respectively. From Eq. (3.9), we know the linear power gain is proportional to f_T approximately. Therefore, the minor reduction of linear power gain after stress is due to the minor change of f_T as shown in Fig. 3.5 (a). After gain compression, because the collector current is kept at a constant value, the output power and power gain even show no noticeable change under stress.

When the measurements were carried out by keeping a constant base current as shown in Fig. 3.7 (b), the output power and power gain show significant degradations after stress. It is due to the large deviation of f_T after stress, as shown in Fig. 3.5 (b). It

is worth noting that the optimized matched conditions have been changed after stress due to the change of the collector current. If we fixed the source and load impedances, the degradation of power performance after stress would be worse. Since the collector current is reduced after stress, it will limit the maximum magnitude of the output waveform to lower values, and thus the compression point will shift to lower output power. Hence the degradation in power gain and output power will be more pronounced in the high power regime. Although the power gain is reduced after stress, the power-added efficiency (PAE) changes only slightly (from 44% to 43%), due to the concomitant reduction of dc output power dissipation.

Figure 3.8 shows the linear power gain versus collector current and base current before and after stress. Comparing the measured results of Fig. 3.5 and Fig. 3.7, we know the f_T and power gain have similar trend with HC stress for all bias conditions, hence the f_T is indeed a dominant factor in Eq. (3.8) which affects the power gain under stress. As shown in Fig. 3.8 (a), a little deviation of power gain can be observed under stress when the measurements were carried out by keeping a constant collector current due to the minor change of cutoff frequency. Unlike the Fig. 3.8 (a), the effects of the HC stress on power gain will be more serious with the base driving currents, especially in the low and medium base current regimes. As shown in Fig. 3.8 (b), the power gain degrades dramatically after stress at low and medium currents, due to the f_T degradation. In high base current regime, the power gain shows it just slightly increases under the HC stress. From Fig. 3.8, it suggests that the power gain has higher immunity for hot-carrier effect when the power amplifier is biased at constant collector current.

3.3.2 RF Linearity

In practical, SiGe HBTs have a good linearity performance due to the almost

complete cancellation between the output nonlinear currents generated by the emitter-base and base-collector current sources [52]. To study the HC stress effects on the linearity of a microwave system, the two-tone load-pull measurement was also carried out [53]. As shown in Fig. 3.9, the third-order intercept point, at which the output power and third-order intermodulation (IM3) are equal, is commonly used to characterize the linearity. For low distortion operation, the third-order intercept point should be as high as possible. While the before-stress value of input third-order intercept point (*IIP3*) is about 6.8dBm, the after-stress *IIP3* reduces to 3.33dBm and -2.46dBm for constant collector-current and constant base-current measurements, respectively.

The major nonlinear elements in a bipolar transistor are the collector current (i_C), base current (i_b), base-emitter charge (q_{be}), and base-collector charge (q_{bc}) as expressed in Eq (3.11-13) [54]:

$$i_c = g_m v_{be} + g_{m2} v_{be}^2 + g_{m3} v_{be}^3 \tag{3.11}$$

$$i_b = g_{be} v_{be} + g_{be2} v_{be}^2 + g_{be3} v_{be}^3 \tag{3.12}$$

$$q_{be} \approx \tau_F i_C = \tau_F g_m v_{be} + \tau_F g_{m2} v_{be}^2 + \tau_F g_{m3} v_{be}^3 \tag{3.13}$$

,where the g_{m2} and g_{m3} are the two-order and the third-order derivatives of transconductance, respectively. The g_{be2} and g_{be3} are the two-order and the third-order derivatives of base-emitter conductance, respectively.

Since the HC stress does not affect the base-collector junction, we only need to consider the distortion from the non-linear exponential functions of collector current, base current and base-emitter charge. Moreover, it is believed that in low current region, the distortion is dominated by the nonlinear contributions from transconductance [55]. As the current is increased, g_m nonlinearities are decreased due

to the increase of g_m and the feedback effect of emitter and base resistances. When measured at the same collector current, the transconductance is changed slightly and it still has a high value before and after stress. Nevertheless, the ideality factor of base current (n_b) has changed drastically from 1.005 to 1.52 after stress, while the ideality factor of collector current is still about 1. It indicates that partial IM3 cancellation, which has been attributed to the interaction of i_b and i_c, or i_c and q_{be}, has been reduced [54]. So the reduction of *IIP*3 after stress is mainly due to the reduced cancellation effect. As to the constant base-current measurement, not only n_b increases to 1.67, but the related collector current also reduces to a lower value after HC stress. Those changes of the ideality factors, transconductance and *IIP3* mentioned above were highlighted and summarized in Table. II. Consequently, the degradation of linearity measured at constant base current is much worse than that measured at constant collector current.

3.4 Summary

In this work, we have investigated in detail the hot-carrier effects on the high-frequency and RF power characteristics of Si/SiGe HBTs. Due to the increase of non-ideal base current after stress, the current gain will be decreased. Consequently, we find that the cutoff frequency, output power, power gain and linearity are suffered by the HC stress. By comparing stress effects at various bias conditions, we observe that the performance degradation is much smaller under constant collector-current measurement, compared to constant base-current measurement. Because of the increased ideality factor of the base current and the reduced collector current after stress, the high-frequency and power characteristics show larger stress-induced degradations for constant base-current measurements. It therefore suggests that the

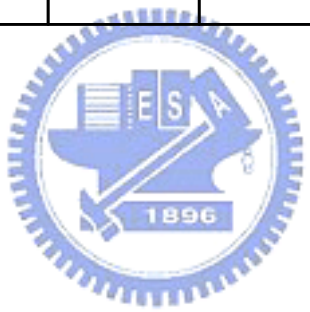
Si/SiGe amplifier performance can be made more robust to HC effects by biasing the HBT at constant collector current.

Table 3-I Equivalent hybrid-π model elements for a typical SiGe transistor before and after stress. V_{CE} = 3V.

	g_m (A/V)	r_π (Ω)	r_{out} (Ω)	C_π (pF)	C_u (pF)
Before stress (I_C=52mA,I_B=0.34mA)	2.01	72	155	19.2	0.23
After stress (I_B=0.34mA)	1.16	83	368	9.55	0.2
After stress (I_C=52mA)	1.82	49	160	18.96	0.22

Table 3-II Summary of changes for the ideality factors, transconductance and RF linearity (*IIP3*) for the base-current and collector-current before and after stress.

	*IIP*3 (dBm)	n_b	n_c	g_m (A/V)
Before stress	6.8	1.005	1	2.01
After stress (I_B=0.34mA)	-4.7	1.67	1.01	1.16
After stress (I_C=52mA)	3.5	1.52	1	1.82



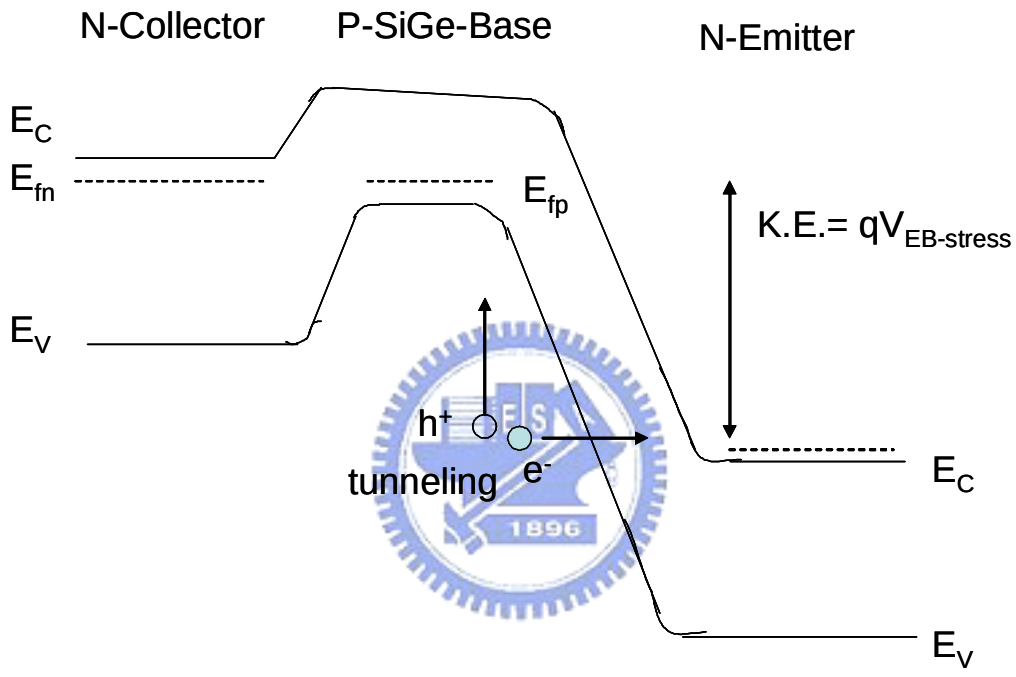


Fig. 3.1. The band diagram of an npn-Si/SiGe HBT under OC stress.

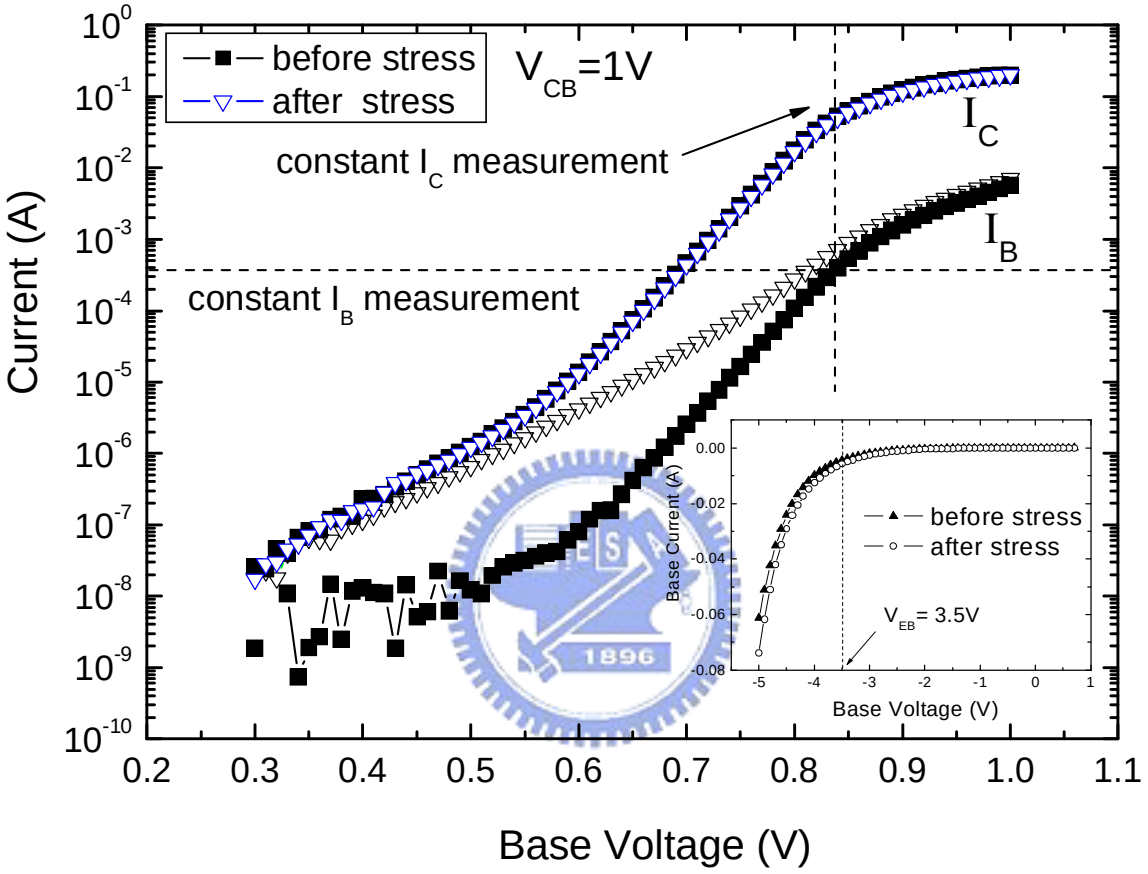


Fig. 3.2(a). Gummel plot of a typical SiGe transistor before and after stress. For power characterization, the collector current I_C and base current I_B are 52 mA and 0.34 mA, respectively, before stress. After stress, I_B changes to 0.7 mA under constant collector current measurement, while I_C changes to 24 mA for constant base current measurement.

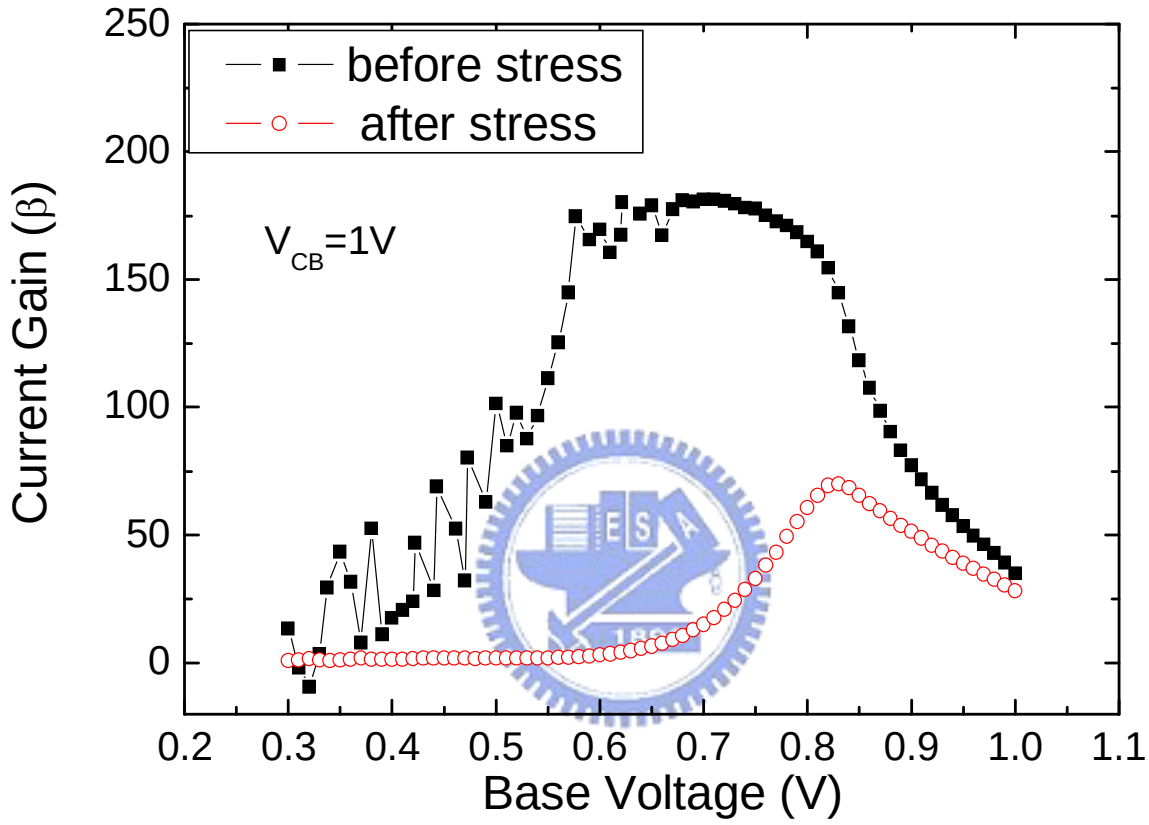


Fig. 3.2(b). DC current gain (β) measured before and after stress.

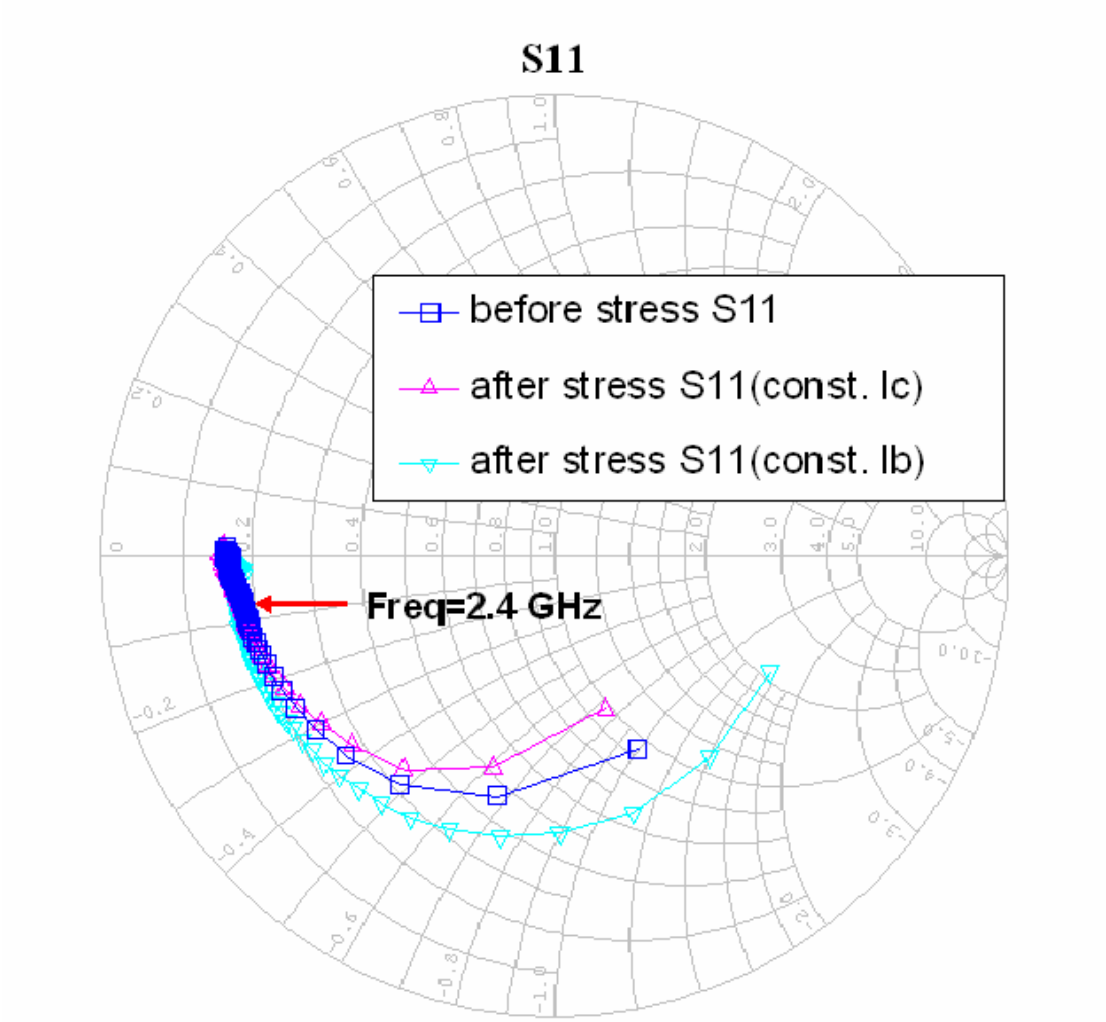


Fig. 3.3 (a) The measured S11 before and after stress at constant base-current and constant collector-current measurements.

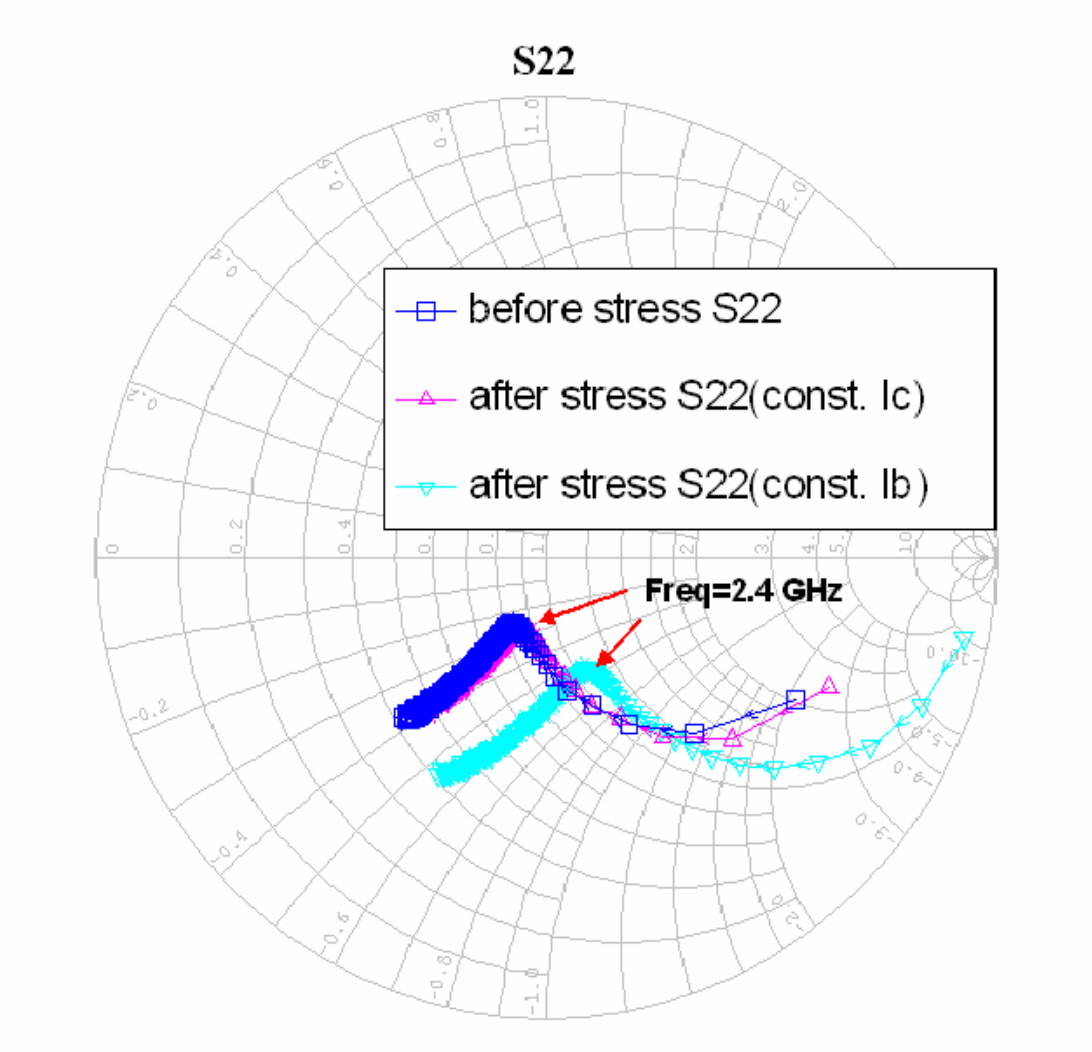


Fig. 3.3 (b) The measured S22 before and after stress at constant base-current and constant collector-current measurements.

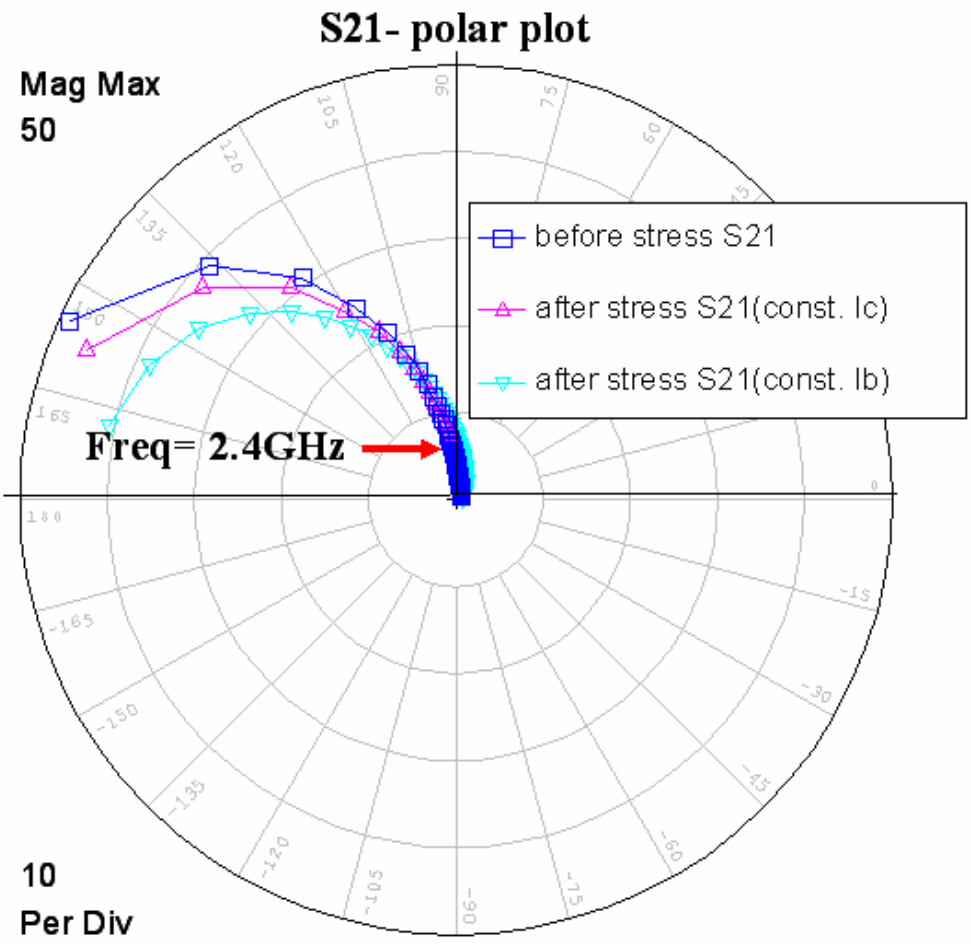


Fig. 3.3 (c) The measured S21 before and after stress at constant base-current and constant collector-current measurements.

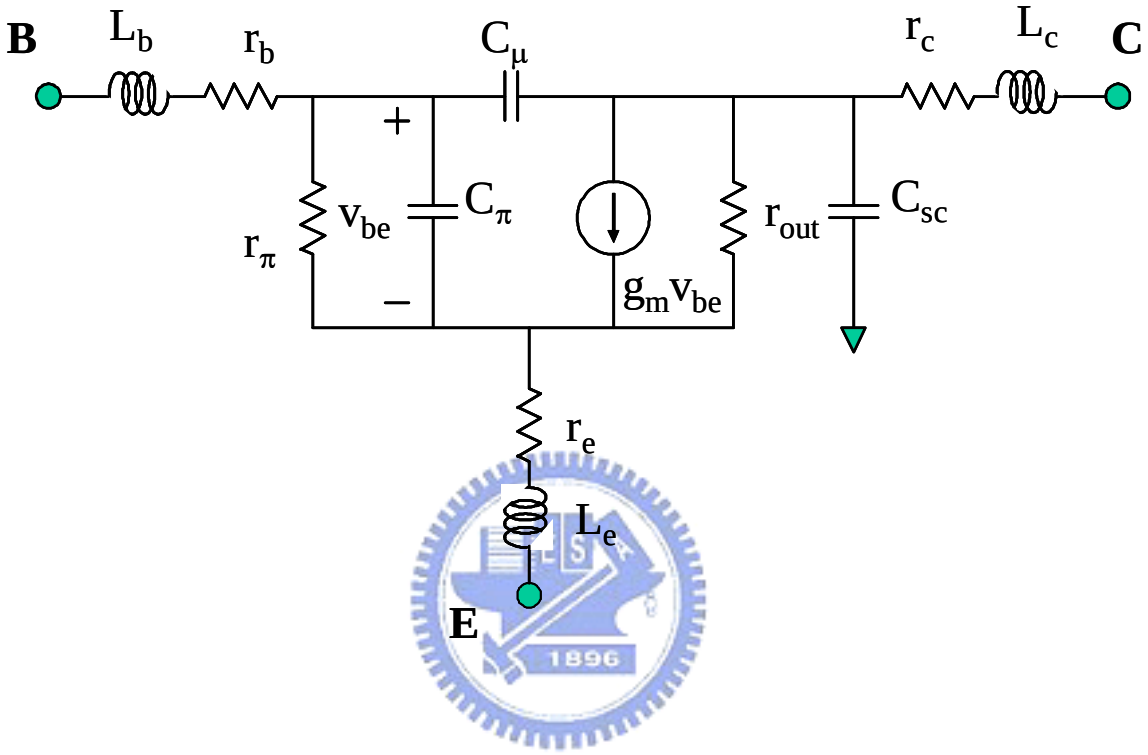


Fig. 3.4 A simple equivalent hybrid-π model of Si/SiGe HBT.

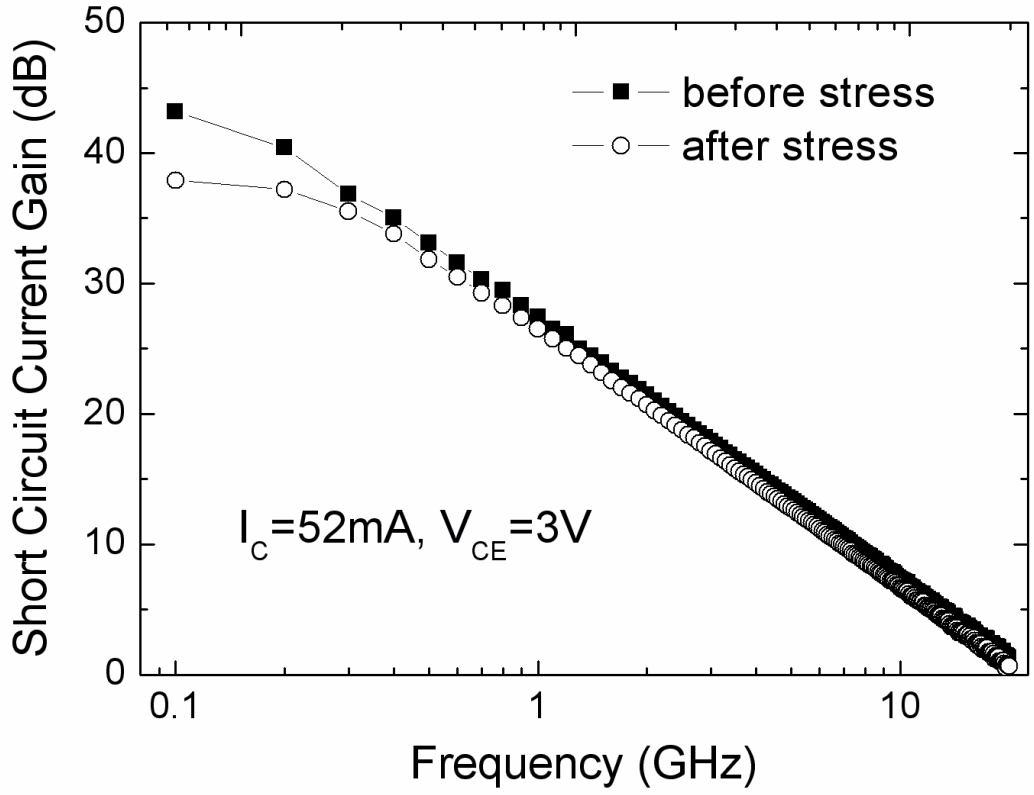


Fig. 3.5 (a) The $|h_{21}|$ versus frequency before and after stress measured at a fixed collector current of 52mA.

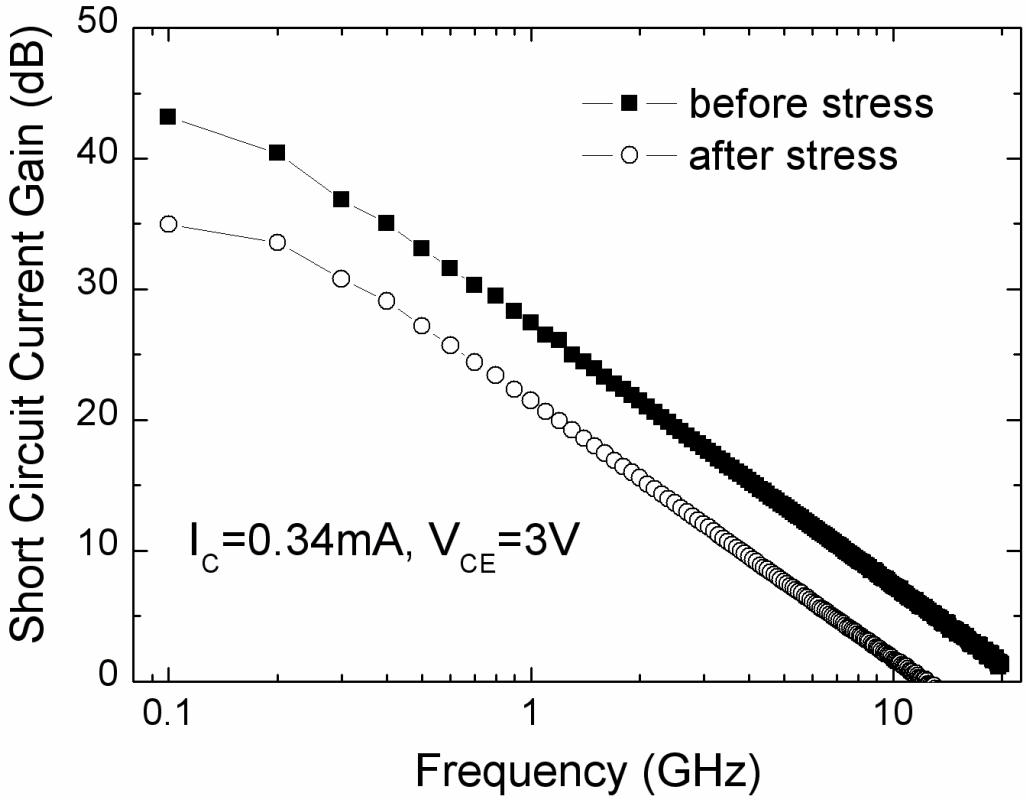


Fig. 3.5 (b) The $|h_{21}|$ versus frequency before and after stress measured at a fixed base current of 0.34mA.

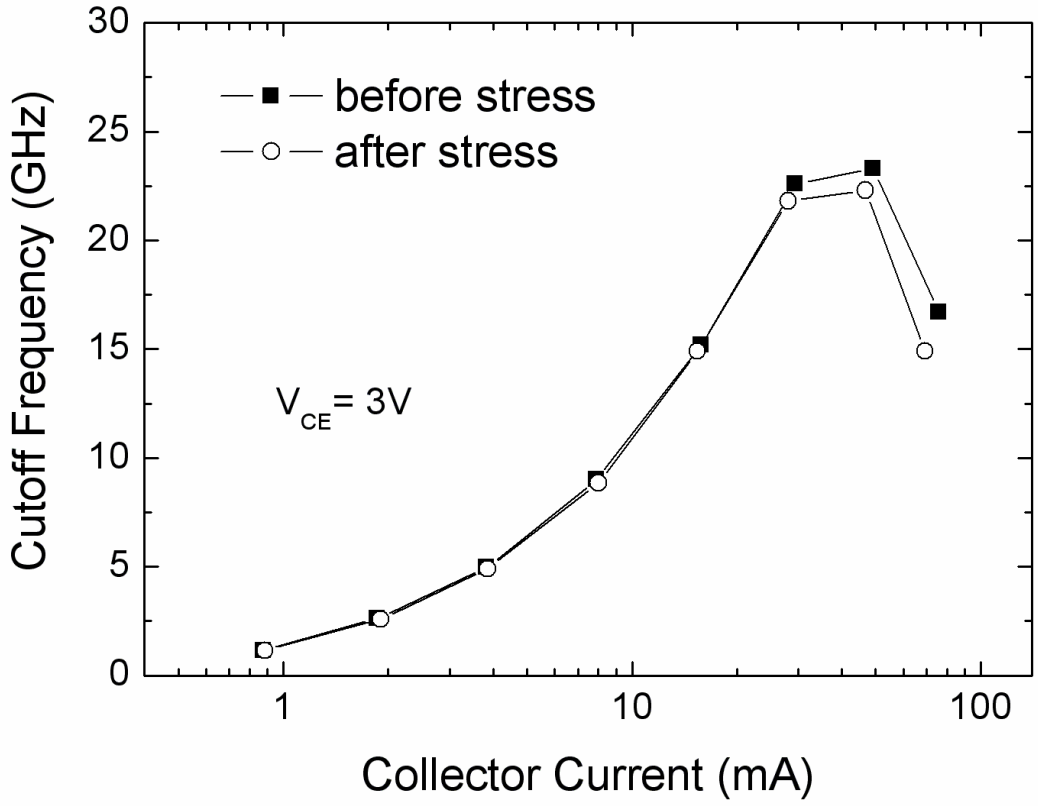


Fig. 3.6 (a) Cutoff-frequency versus collector current measured before and after HC stress.

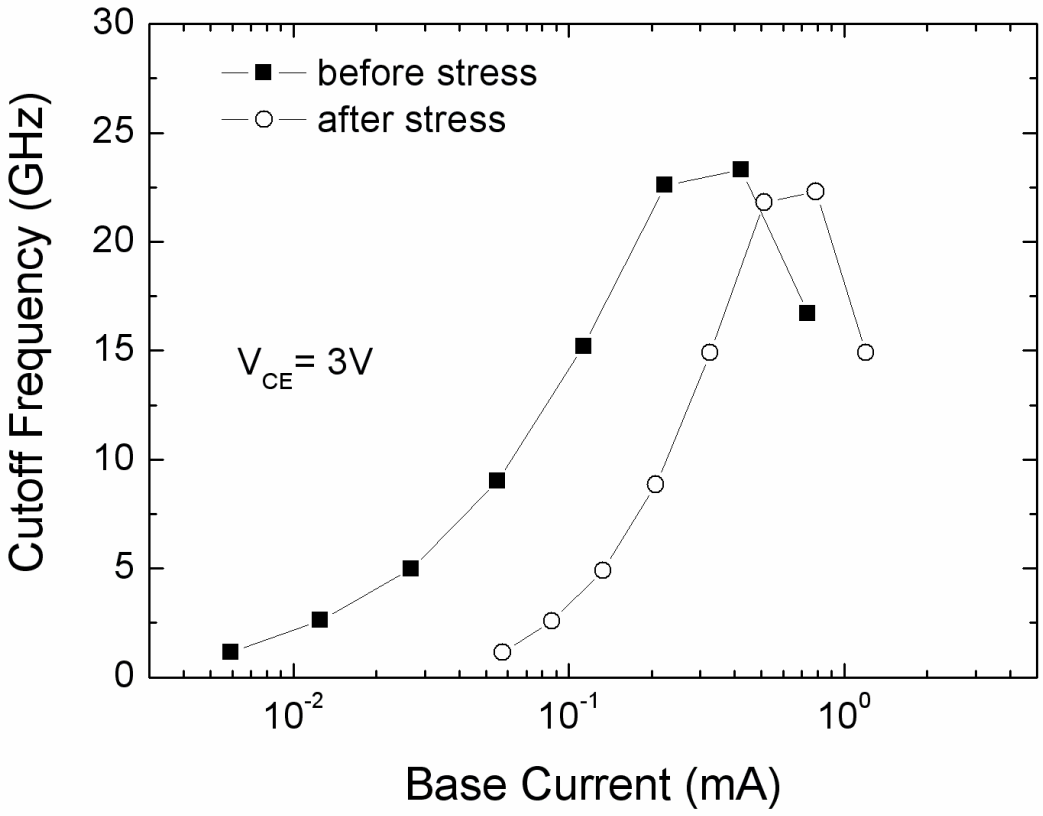


Fig. 3.6 (b) Cutoff-frequency versus base current measured before and after HC stress.

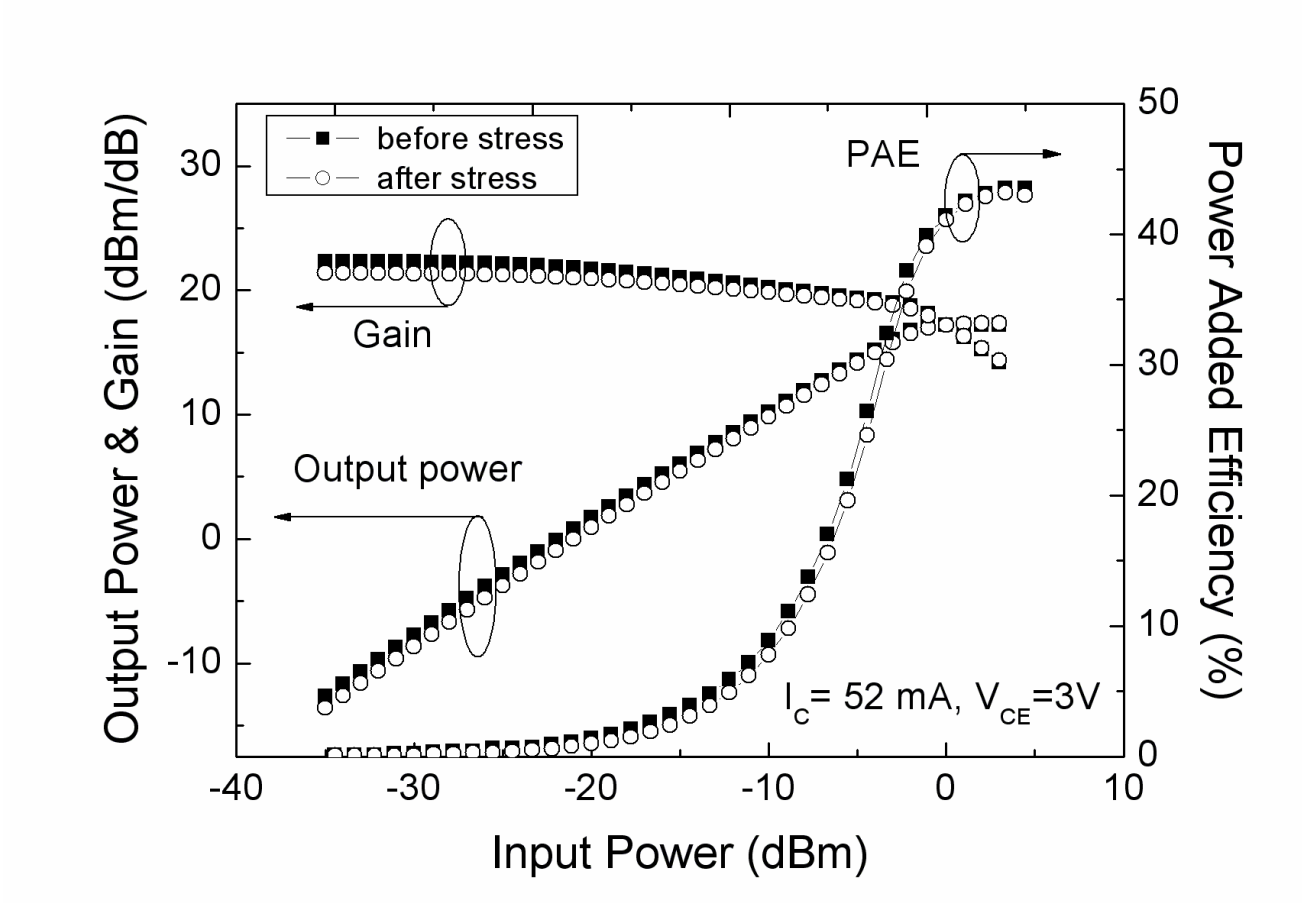


Fig. 3.7 (a) Linear power gain versus collector current before and after stress measured with P_{in}= -30dBm.

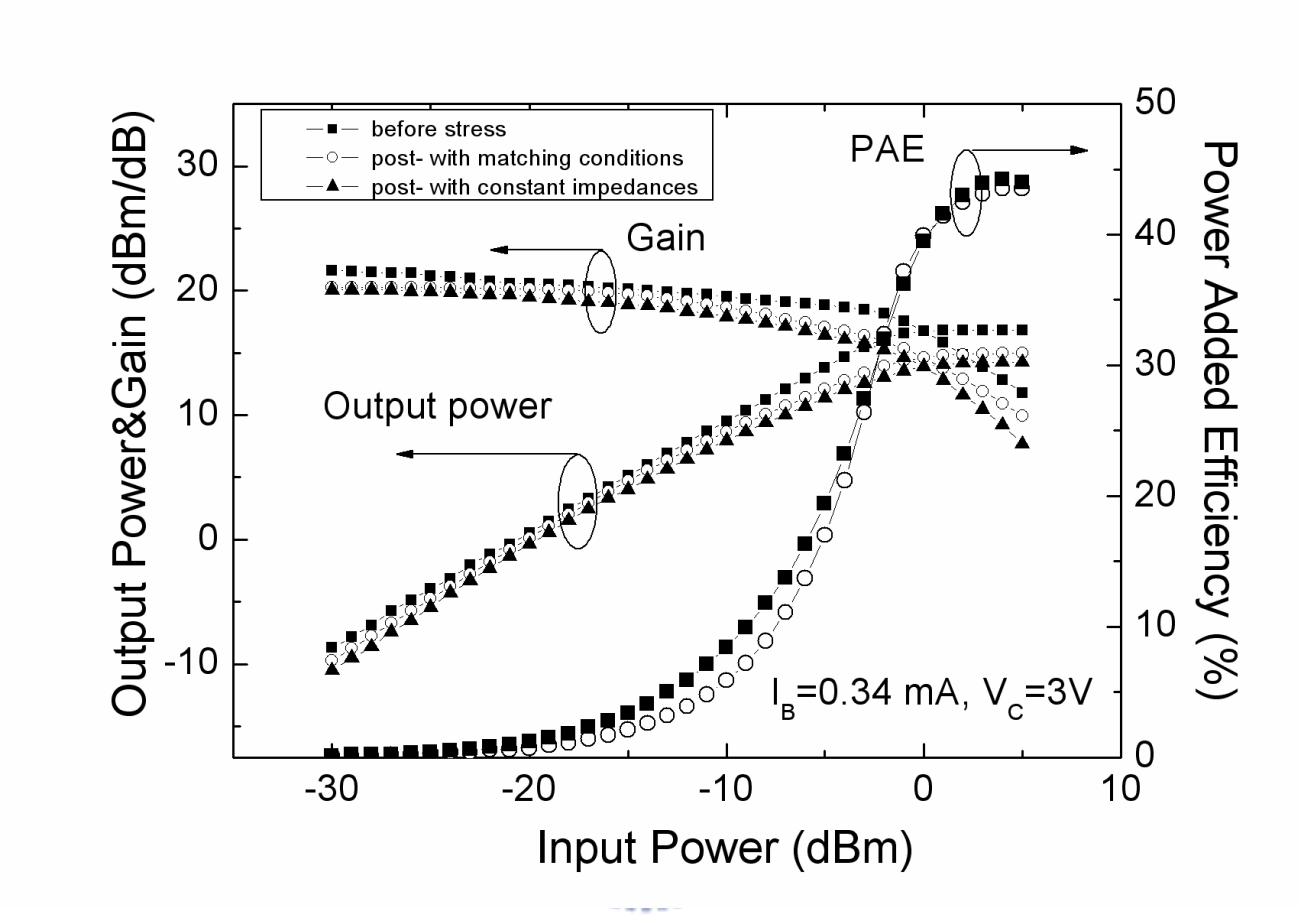


Fig. 3.7 (b) Linear power gain versus base current before and after stress measured with P_{in}= -30dBm.

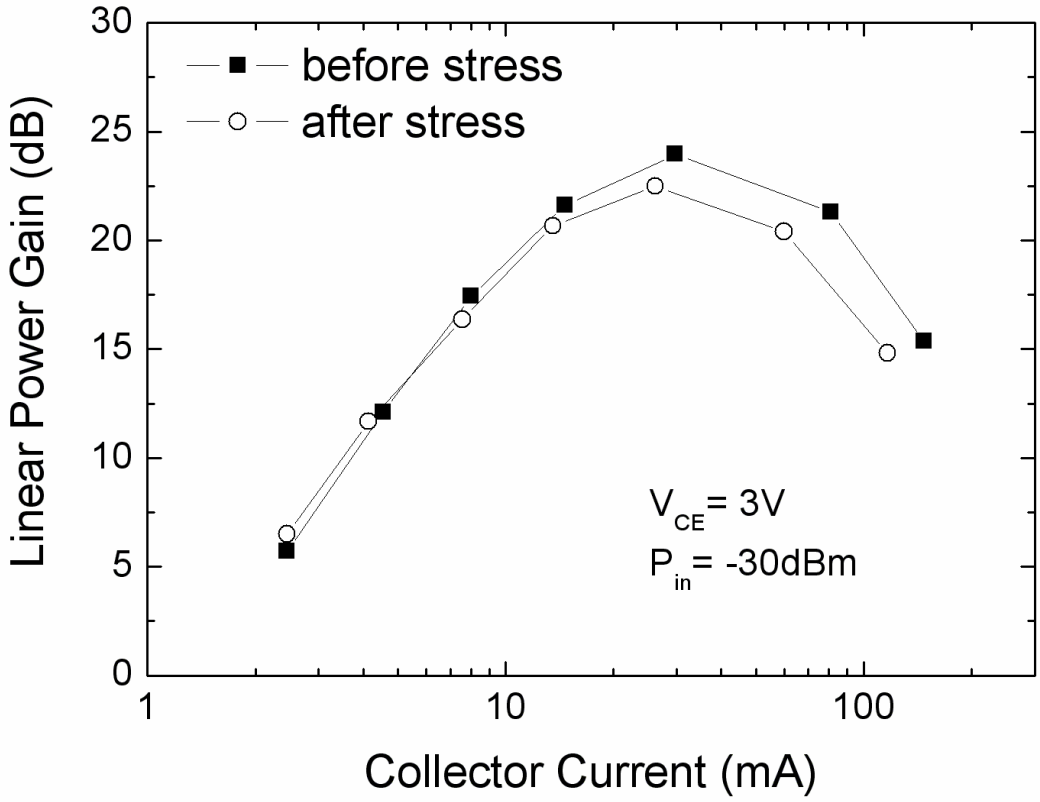


Fig. 3.8 (a) Output power, power gain and PAE versus input power before and after stress measured at a fixed collector current.

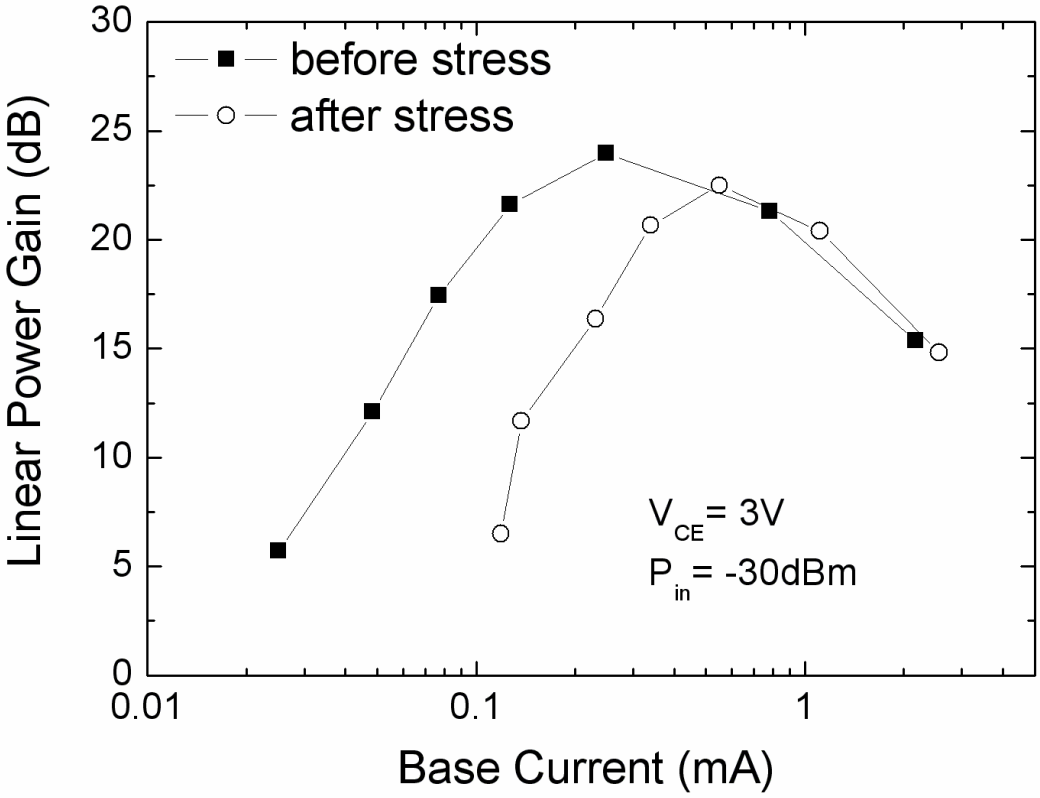


Fig. 3.8 (b) Output power, power gain and PAE versus input power before and after stress measured at a fixed base current.

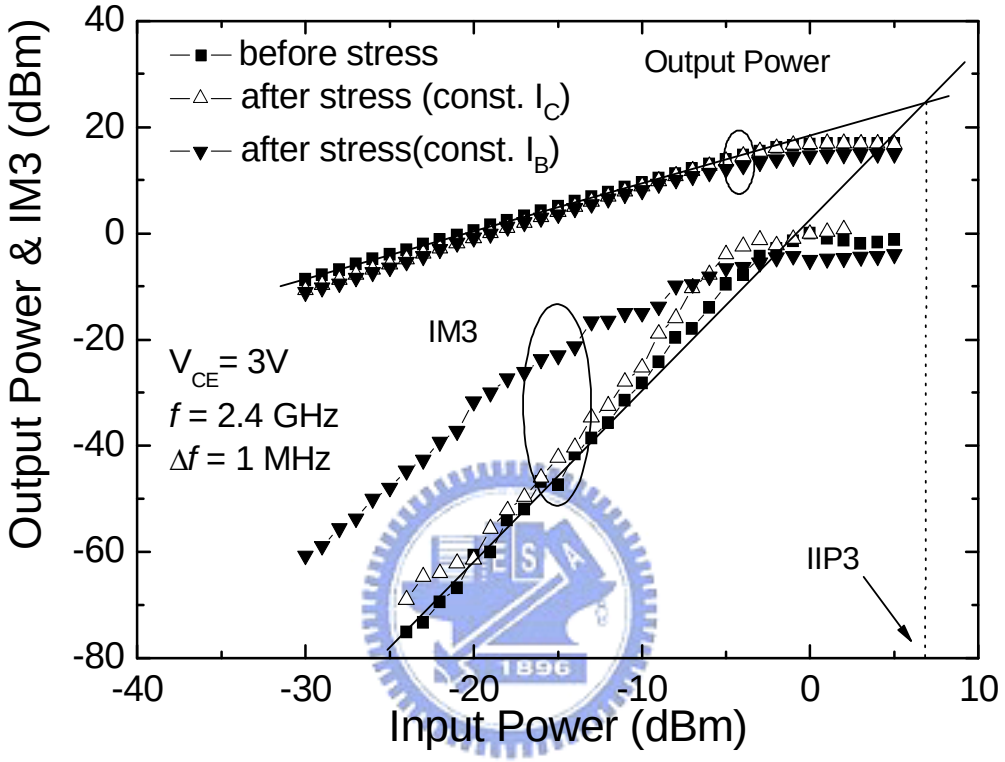


Fig. 3.9 Output power and third-order intermodulation power versus input power for a SiGe HBT before and after stress.

Chapter 4

"Mixed-mode" Stress Effects on SiGe HBTs for High-Frequency and RF Power Applications

4.1 Introduction

Traditionally, bipolar reliability for electrical stressing includes two different techniques [56]-[59]: high forward collector current density (J_C) stress, and emitter-base reverse-bias stress. For high forward collector current stress, it is normally conducted under a large J_C near peak cut-off frequency and is usually at elevated temperatures. This kind of stress degradation is generally associated with the electromigration induced changes in the emitter contact. For emitter-base reverse-bias stress, the device degradation is due to the hot carriers injecting into the emitter-base spacer oxide, which induce G/R center traps, and lead to excess non-ideal base currents.

In real products application, a new reliability degradation mechanism was reported [60]-[62], and termed as a "mixed-mode" stress degradation. It occurs when high collector current density (J_C) and high collector-base (CB) voltage are imposed simultaneously on the device. It is very interesting to us, because this stress condition is approaching to a real bipolar-power amplifier operations; especially, for the topologies Class A, B, AB and C, in which the active devices are worked as a controlled current source.

In this chapter, we investigate the "mixed-mode" electrical stress effects on the dc, high-frequency and RF power characteristics of SiGe HBTs with different bias

conditions. In addition, by applying a commercial VBIC large-signal model, the high-frequency behavior, RF power performance and linearity are also described completely.

4.2 Mixed-mode Stress Effects on High-Frequency Performance

Multi-finger Si/SiGe HBTs were fabricated with a high-voltage 0.18μm BiCMOS process. The nominal emitter width of the 4-finger-stripe device was 1 μm, and the length was 32 μm. The Ge content features a triangle profile in the base layer to speed up the transport of electrons across the device. Those transistors exhibit a dc current gain up to 181 and the BV_{CEO} is 5.3V. The typical cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}) are about 26 GHz and 37 GHz, respectively. The electrical stress was carried out by applying a high collector current density J_C=2mA/μm^2 and a high collector-base voltage V_{CB}=3.7V simultaneously with a final stressing time up to 1500 seconds at room temperature. The S-parameter measurements were performed by using an HP8510 network analyzer. The output power, power gain, and linearity were measured using the load-pull system, which consisted of HP85122A and ATN LP1 (power parameter extraction software), while the source and load impedances were tuned for maximum output power. For the load-pull measurements, the operating frequency was chosen at 2.4GHz, a frequency commonly used in wireless communication.

The typical Gummel plot of a SiGe HBT measured under mixed-mode stress with different stressing times is shown in Fig. 4.1. The value of base current (I_B) leakage rises significantly with the stressing time in forward Gummel plot. In addition, unlike the conventional emitter-base reverse-bias stress, which does not create any I_B leakage in the reverse-mode operation of SiGe HBT, the mixed-mode stress creates an excess

I_B leakage current component in reverse Gummel plot, as indicated in Fig. 4.2. These results show that the mixed-mode stress induces traps not only in the emitter-base (EB) space-charge region, but also in the collector-base (CB) space-charge region [60], [61]. It is clear that the base leakage current shifts to a higher value while the collector current is nearly unchanged after mixed-mode stress. This results in a degradation of the dc current gain as shown in Fig. 4.3. Therefore, there will be some interesting different device electric performance under "mixed-mode stressing" compared to traditional OC stressing. The comparison of physical mechanism between OC stress and "mixed-mode" stress are summarized in Table 4-I.

Since the dc performance of a SiGe HBT degrades after the electrical stress, it will certainly influence the figures-of-merit (FOM) of RF characteristics. The cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}), which indicates the limitations of high-frequency current gain and power gain, respectively, are the most common RF FOM of RF transistors and those can be expressed as:

$$f_T \approx \frac{1}{2\pi \times \left(\frac{KT}{qI_E}(C_{EB} + C_{CB}) + R_C C_{CB} + \tau_B + \tau_C \right)} \tag{4.1}$$

$$f_{MAX} \approx \sqrt{\frac{f_T}{8\pi \times R_B \times C_{BC}}} \tag{4.2}$$

,where C_{EB} and C_{CB} are emitter and collector capacitances, respectively. R_C is the collector resistance. $(KT/qI_E)(C_{EB}+C_{CB})$ is the charging relation of diffusion capacitance, τ_B is the base transit time, and τ_C is the collector space-charge transit time. Fig. 4.3 shows the cutoff frequency as a function of collector current before and after electrical stress. As expressed in eq. (4.1), the cutoff frequency is just associated with the transit times and emitter currents. It is obvious that the mixed-mode stress has slight effects on the cutoff frequency. For the low bias region in Fig. 4.3, the cutoff

frequency seems to be unchanged after electrical stressing. This can be ascribed to the nearly unchanged collector current after stress. At higher biases (I_C>50mA), the cutoff frequency increases after stress. This is due to the decreasing emitter resistance (R_E) that has been known in bipolar transistors operating in high J_C. The decrease of emitter series resistance is relating to hydrogenation of electronic traps [62],[63]. Additionally, in our case, this effect maybe owing to the native oxide in the interface of poly-emitter and epi-layer of SiGe-base is punctured by stressing under such a higher current density. These observations are different from that under emitter-base reverse-bias stress (in Chapter 3), where the cutoff frequency was also unchanged at low currents but only slightly decreased at high currents after stress. It may be due to the emitter resistance was unchanged under emitter-base reverse-bias stress.

Figure 4.4 shows the maximum oscillation frequency as a function collector current. The maximum oscillation frequency is a power gain index for RF transistors, and is relating to the output resistance, base resistance, and isolation capacitance between base and collector junction of Si/SiGe HBTs. In Fig. 4.4, the f_{max} decreases in low and medium bias regions not only due to the increasing base leakage currents, but also due to the increasing base resistance (R_B) after electrical stress. In addition, the result of stress-induced change in base resistance is either caused in the extrinsic base region, or in the base contact. On the other hand, the mixed-mode stress simultaneously imposes high collector current and high reversed V_{CB} bias, it will lead to an accumulation of charges located in base-collector regions [65]. But, the change of the base-collector capacitance (C_{BC}) is negligible in our measurement after the electrical stress.

4.3 Mixed-mode Stress Effects on Power Performance

As well as the high-frequency characteristics, the microwave power characteristics are also affected by the electrical stress. In order to reach a higher output power under a limitation of breakdown voltage and reasonable power consumption, the voltage drop of output terminal and the output current should be as high as possible. Thus, in normal operation of a power amplifier, there exists the risk of hot-carrier induced degradations on the RF power performance.

The influence of the electrical stress on RF power performance is shown in Fig. 4.5. Different measurement conditions are compared (constant I_C and constant I_B), the compared currents are chosen for the maximum cutoff frequency and approaching to maximum current gain before stress. The mixed-mode electrical stress condition is like the actual operation of SiGe HBT's power amplifiers. As shown in Fig. 4.5(a), when the collector current was kept to a constant value of 34mA, we observed a slight change on output power and power gain. However, the power-added-efficiency (PAE) which terms as $100\% \times (P_{out}-P_{in})/P_{DC}$ increases after electrical stress due to the reducing emitter resistance (R_E) after stress. When the measurement was carried out by keeping a constant base-current (I_B = 40 μA), the power performances degrade after electrical stress (see Fig. 4.5(b)). The increasing base leakage current after stress leads a voltage drop of V_{BE} to a less value to keep a constant base-current of 40 μA. However, it results in a decreased value of collector-current than that before electrical stress. The change of linear power gain is due to the decreasing collector current after electrical stress with a constant base-current measurement. Owing to the decreasing collector current after stress, the PAE shows an increasing trend. Besides, it is noted that the power gain increases gradually with increasing input power level before gain compression for device after stress. The gain expansion takes place as device operates near cutoff region [72]. Because the negative duty cycle of output I-V waveform will suffer cutoff clipping effect after compression point, the average output current

increases with the increasing input large-signal power. For device after stress, the base voltage was biased at lower value with constant base current (see Fig. 4.1), hence the average output current increases more rapidly than that before stress. As a result, the PAE decreases after compression point.

Actually, SiGe HBTs have a good linearity performance due to the almost complete cancellation between the output nonlinear currents generated by the emitter-base and base-collector current sources [67]. To study the electrical stress effect on the linearity of SiGe HBTs, the two-tone load-pull measurement was also carried out [68]. Fig. 4.6 presents the RF linearity of a SiGe HBT before and after electrical stress. The third-order intercept point, at which the output power and third-order inter-modulation power (IM3) are equal, is commonly used to characterize the RF linearity, as shown in Fig. 4.6(a). For low distortion operation, the third-order point should be as high as possible. From Fig. 4.6(a), we observed that the third-order inter-modulation power (IM3) of a SiGe HBT under constant base-current measurement increases after stress and then results in degradations of input and output third-order intercept points (IIP3 and OIP3).

The major nonlinear elements in bipolar transistors are collector current, base current, base-emitter charge, and base-collector charge [69]. These elements are affected by the “mixed-mode” electrical stress. As indicated in Fig. 4.1, the ideality factor of base current (n_b) has changed drastically after electrical stress, while the ideality factor of collector current is still about 1. It indicates that the partial IM3 cancellation, which has been attributed to the interaction of collector current and base current, or collector current and base-emitter charge, has been reduced [69]. In addition, for constant base-current measurement, the related collector current also reduces to a lower value after stress. Consequently, the linearity measured at a constant base current will be degraded after stress. For constant collector-current

measurement, the nonlinearity of collector current is unchanged, so the measured IM3 only changes slightly, as shown in Fig. 4.6(b).

4.4 Device Modeling after Mixed-mode Stress

To examine the stress effects on the high-frequency and power behavior of a SiGe HBT, a large-signal model was built in this work. A commercial VBIC model was used to extract the main parameters which are affected more seriously by mixed-mode electrical stress. VBIC model is typically a four terminals model with a substrate network. Compare to the traditional Gummel-Poon model, VBIC model includes some advantages describing device behaviors [70]. In Fig. 4.7 (a), and (b), those show the simulated gummel-plots result with the measured data before and after electrical stress. In Fig. 4.8, it shows the DC current gain with measured and simulated data before and after stress. From the dc and ac characteristics, we can extract the model parameters before and after electrical stress. In addition, by using the matrix of co-relation function, we can compare the effects of DC degradation and RF figures-of-merit as the function of (4.3).

$$\begin{bmatrix} \Delta f_T \\ \Delta f_{\max} \\ \Delta G_p \\ \Delta V_{ip3} \\ \cdots. \end{bmatrix} = \begin{bmatrix} \frac{\partial f_T}{\partial g_m} & 0 & 0 & \frac{\partial f_T}{\partial C_{be}} & \frac{\partial f_T}{\partial C_{bc}} & 0.... \\ \frac{\partial f_{\max}}{\partial g_m} & 0 & \frac{\partial f_{\max}}{\partial R_{out}} & \frac{\partial f_{\max}}{\partial C_{be}} & \frac{\partial f_{\max}}{\partial C_{bc}} & \frac{\partial f_{\max}}{\partial R_b} .... \\ \frac{\partial G_p}{\partial g_m} & 0 & \frac{\partial G_p}{\partial R_{out}} & \frac{\partial G_p}{\partial C_{be}} & \frac{\partial G_p}{\partial C_{bc}} & \frac{\partial G_p}{\partial R_b} .... \\ \frac{\partial V_{ip3}}{\partial g_m} & \frac{\partial V_{ip3}}{\partial g_{m3}} & 0 & 0 & 0 & 0.... \\ \cdots\cdots & \cdots\cdots & \cdots\cdots & \cdots\cdots & \cdots\cdots & \cdots\cdots \end{bmatrix} \begin{bmatrix} \Delta g_m \\ \Delta g_{m3} \\ \Delta R_{out} \\ \Delta C_{be} \\ \Delta C_{bc} \\ \Delta R_b \\ \cdots\cdots. \end{bmatrix} \quad (4.3)$$

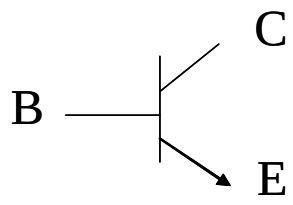
By using a topology of class-A power amplifier structure as shown in Fig. 4.9(a),

the simulated and measured power characteristics of our established model are shown in Fig. 4.9(b). The simulated results agree with the measured results. Consequently, in Fig. 4.10 we used this large-signal model and the class-A topology to simulate the power characteristics of SiGe HBTs after electrical stressing with a constant base-current measurement. The main parameters, which are affected by electrical stress more seriously, are listed in Table II. The ideality factor of base current increases apparently from 1.01 to 1.74 after mixed-mode stress. In addition, from the reverse Gummel-plot, the ideality factor of reversed base leakage current also increases after mixed-mode stress due to the traps located in the collector region. Since the ideality factors are changed after electrical stress, RF linearity will also be affected after stress, as discussed in section IV. The emitter resistance (R_E) reduces from 1.4 Ω to 1.2 Ω, and thus slightly increased the collector current at higher V_{BE} after mixed-mode stress. In addition, the base resistance ($R_B=R_{BX}+R_{BI}$), which includes the extrinsic and intrinsic parts, shows a rising value from 21.7 Ω to 48.2 Ω after electrical stress. As shown in Fig. 4.11, the cross-section of a typical SiGe HBT simply features the locations of the hot-carrier damages. The stress-induced damage is particularly located at the extrinsic base surface close to the emitter, even if some degree of damage is also induced in the intrinsic zone of the base-emitter junction. This effect can be explained and clarified through the measurement of low frequency noise like that of 1/*f* noise [70]-[73]. In addition, on the basis of some literatures, some effects like the observed increase in the access resistance is suggested owing to the passivation of base dopant impurities after hydrogen atoms releasing during the electrical stress [73]-[75]. The reason is possibly the previously pointed out increase of R_B after the mixed-mode stressing. The variation of base resistance R_B will also affect the maximum oscillation frequency and RF power performance. From Table II, finally, we know that the stress does not influence the capacitance parameters.

4.5 Summary

We have investigated the hot-carrier effects, which are induced from the mixed-mode stress, on the high-frequency and RF power characteristics of Si/SiGe HBTs. Simultaneously applying a high collector current density and a high collector-base voltage on the device, the hot carrier will be induced to degrade the device performance. From the extracted parameters of VBIC model, we know that the degradations of high-frequency and power characteristics are also affected by the change of base resistance, emitter resistance, and ideality factor of base current. By comparing the stress effects at various bias conditions, we observe that the stress-induced degradation under constant base-current measurement is much larger than that under constant collector-current measurement, due to the reduction of collector current. It then suggests that SiGe HBTs can be operated more robust to electrical stress by biasing devices under a constant collector current.

Table 4-I. Some VBIC model parameters for a SiGe transistor before and after stress. V_{CE}=3V.



Electrical Stress:	OC stress	Mixed-mode stress
Stress conditions:	• Reversed emitter-base V_{BE} stress, and open collector. • Change temperatures to accelerate.	• High collector current density J_C, and high reversed V_{CB} stress. • At room temperature.
Physic mechanism:	Inject hot electrons (or holes) into EB spacer oxide, introducing G/R center traps.	Inject traps not only in EB spacer oxide, but also in STI near BC junction.
General results: (Forward gummel-plot)	Increasing obvious G/R base leakage current.	Increasing obvious G/R base leakage current.
General results: (Reverse gummel-plot)	Slightly variation or non-changed.	G/R base leakage current.
Geometry effects:	J_B~P/A	J_B~A/P

Table 4-II. Some VBIC model parameters for a SiGe transistor before and after stress. V_{CE}=3V.

Main model Parameter	C_{BE} (pF)	C_{BC} (pF)	C_{SC} (fF)	R_{CX} (Ω)	R_{CI} (mΩ)	R_{BX} (Ω)	R_{BI} (Ω)	R_E (Ω)	NF	NEI	NEN	NR	NCI	NCN
Before stress	1.13	0.16	95	2.03	1.27	4.6	17.1	1.4	0.99	1.01	1.92	0.98	0.98	1.356
After stress	1.16	0.16	98	6.03	9	4.02	44.2	1.2	1.03	1.74	0.91	1.1	1.18	1.245

AC Parameter	Before stress	After stress
TF (psec)	3.02	3.3
ITF (A)	0.9	0.796
VTF (V)	1.31	1.554
QTF (u)	6.9	8.63
XTF	113.6	225.4
TD (psec)	3	1.2
TR (psec)	350	370

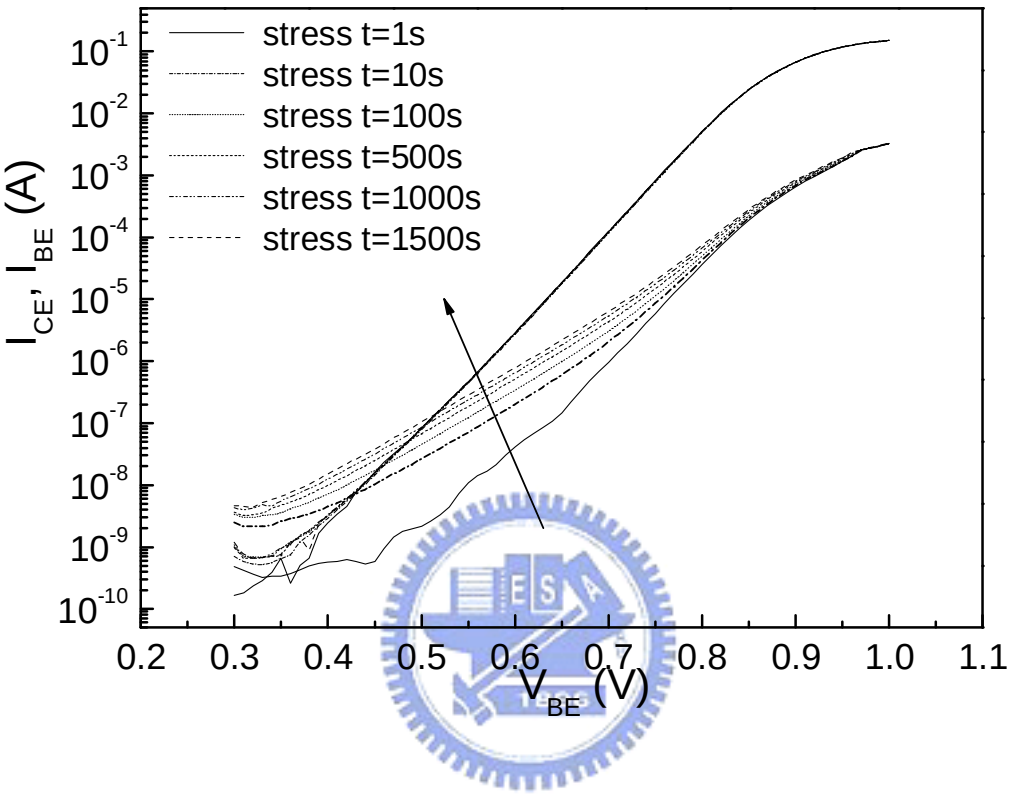


Fig. 4.1 Typical Gummel plot of a SiGe transistor under mixed-mode stress with different stressing times.

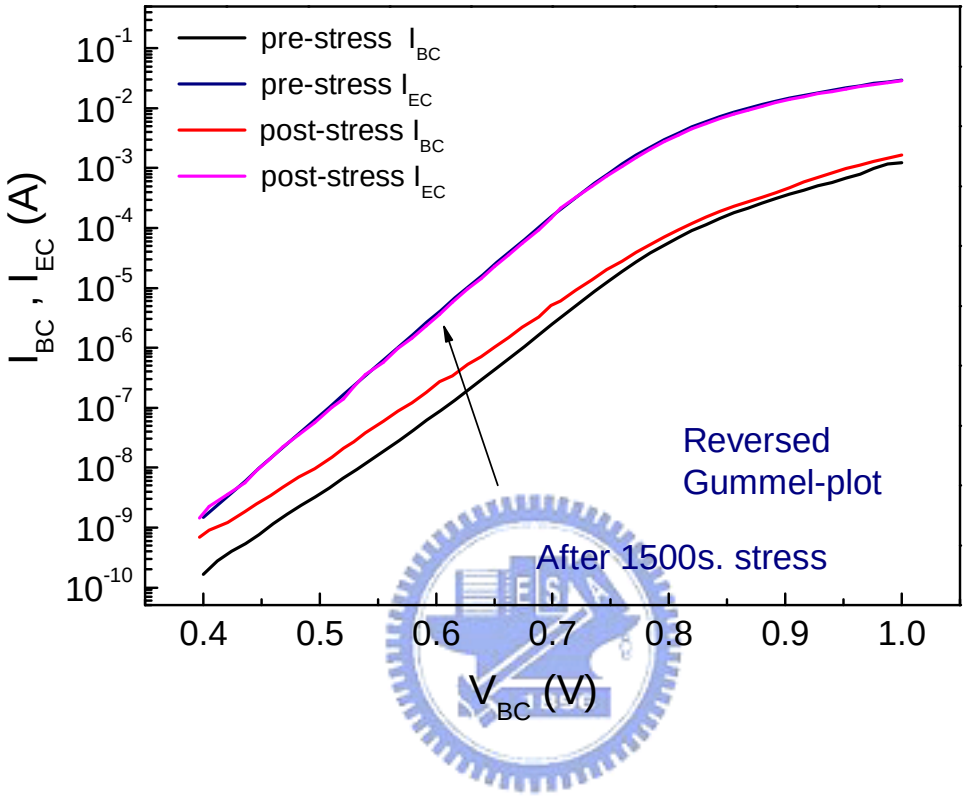


Fig. 4.2 An excess I_B leakage current component in reverse Gummel plot after mixed-mode stress.

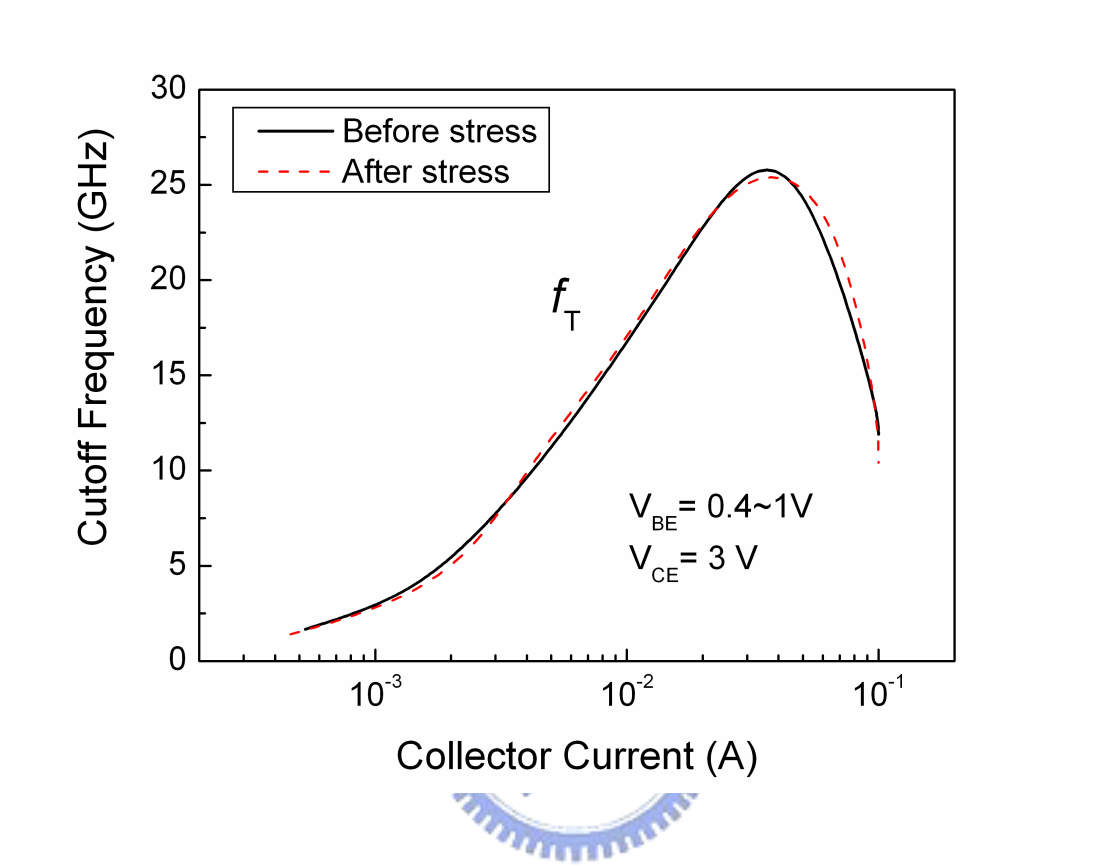


Fig. 4.3 Cutoff-frequency versus collector current before and after stress.

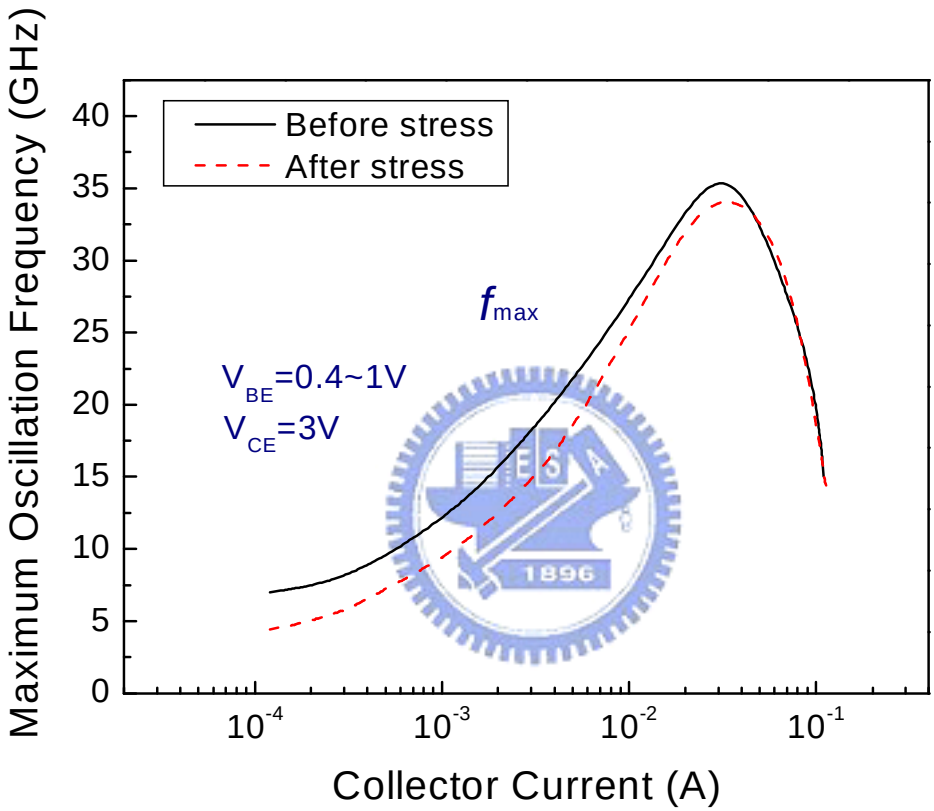


Fig. 4.4 Maximum oscillation frequency versus collector current before and after stress.

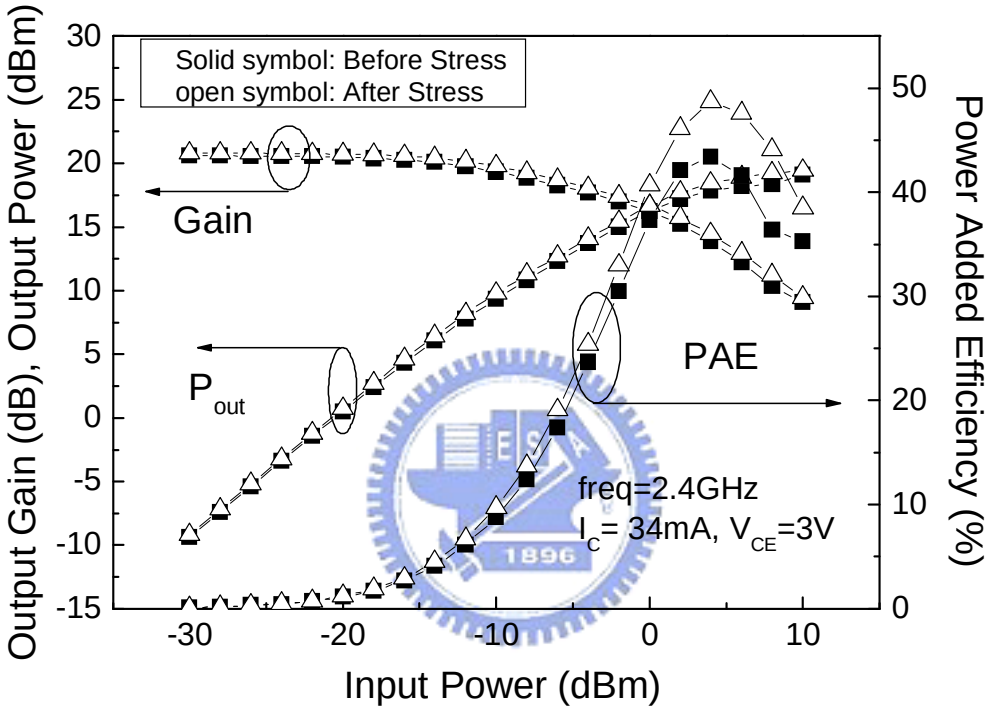


Fig. 4.5 (a) Output power, power gain, and PAE versus input power before and after stress measured at fixed collector current (34mA).

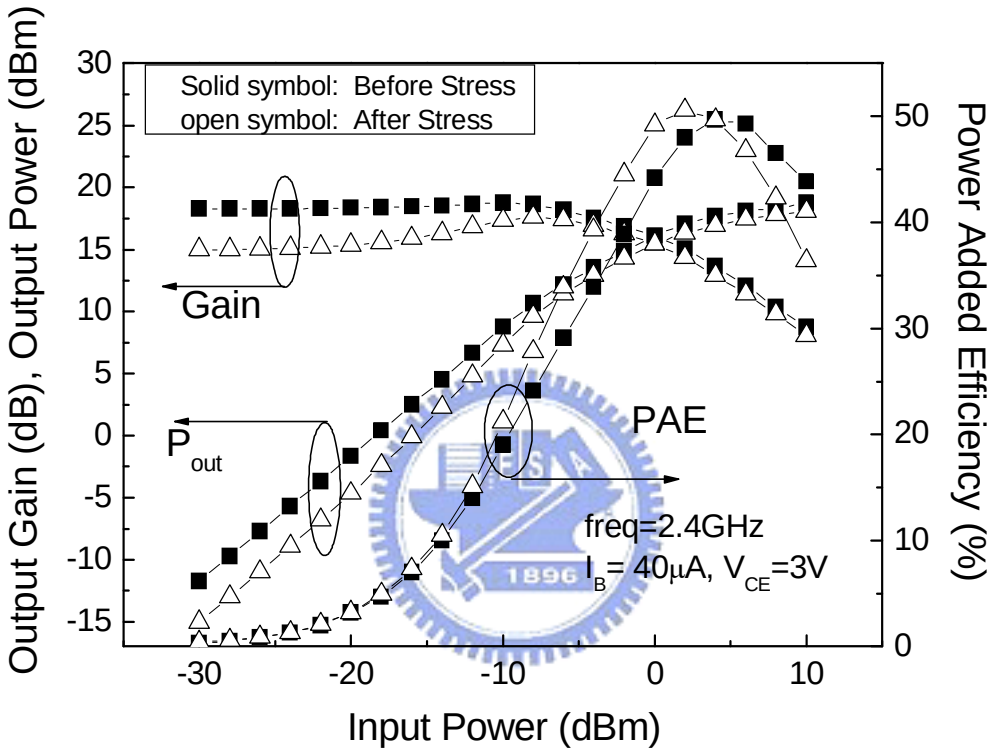


Fig. 4.5 (b) Output power, power gain, and PAE versus input power before and after stress measured at fixed base current (40μA).

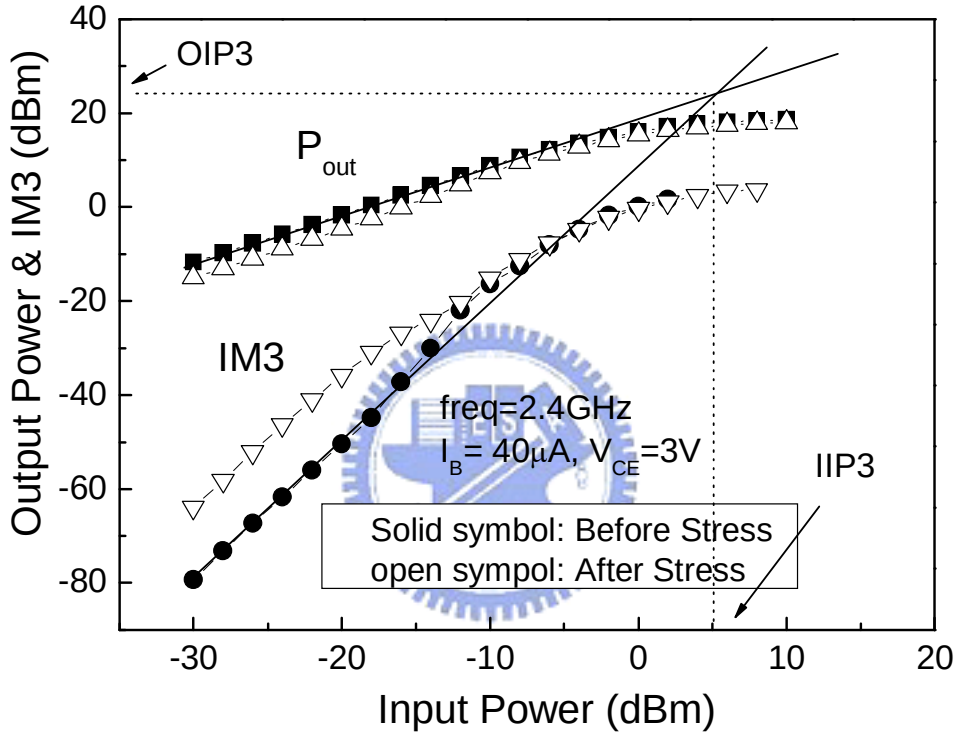


Fig. 4.6 (a) Output power and third-order intermodulation power versus input power for a SiGe HBT before and after stress under constant base-current measurement.

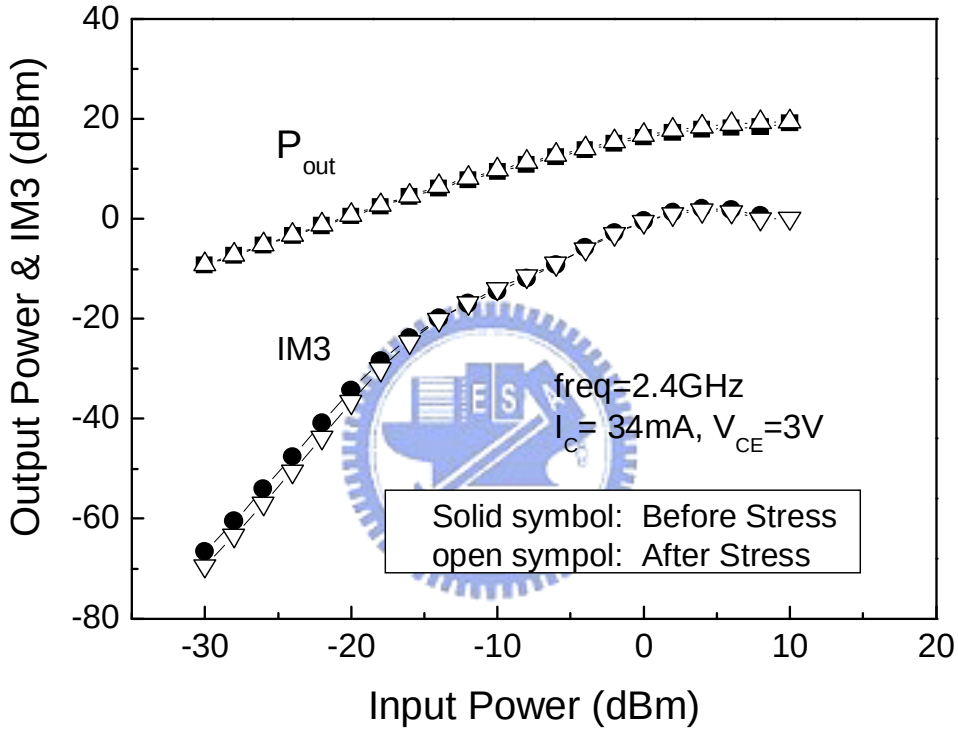
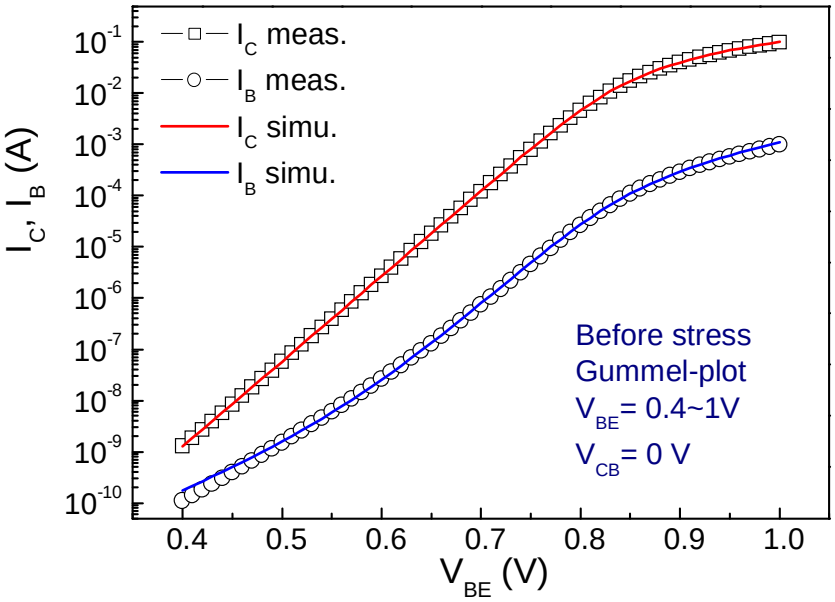
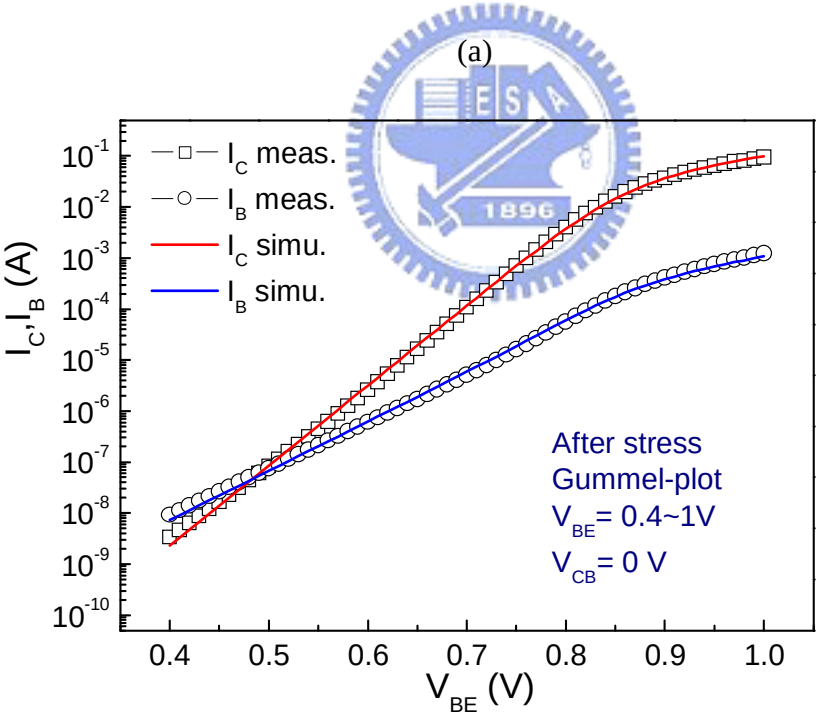


Fig. 4.6 (b) Output power and third-order intermodulation power versus input power for a SiGe HBT before and after stress under constant collector-current measurement.



(a)



(b)

Fig. 4.7 Measured and simulated forward Gummel plot of a SiGe HBT (a) before and (b) after stress.

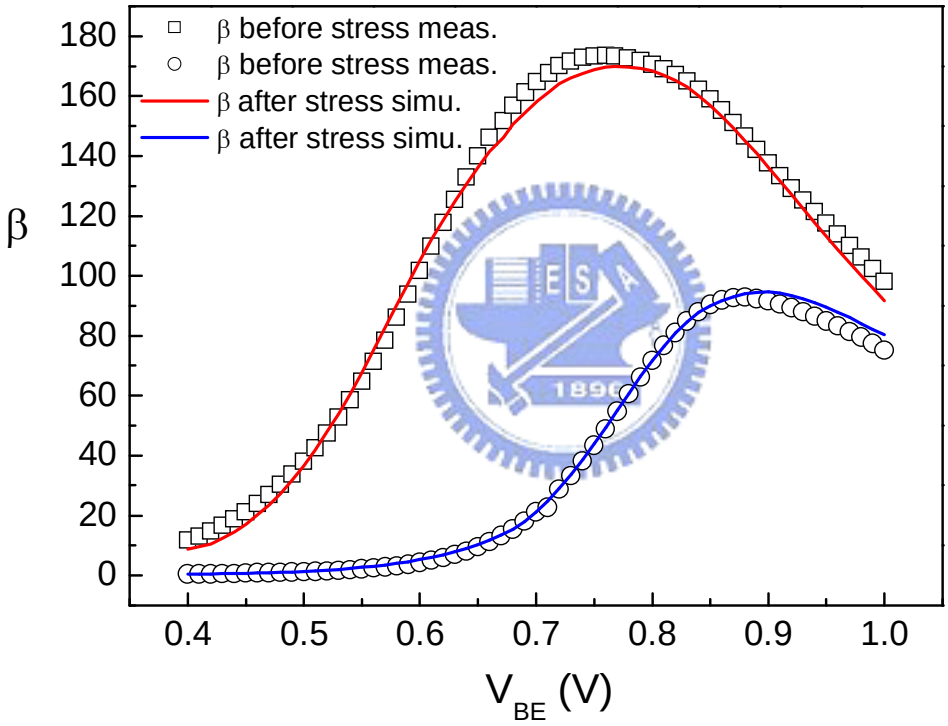
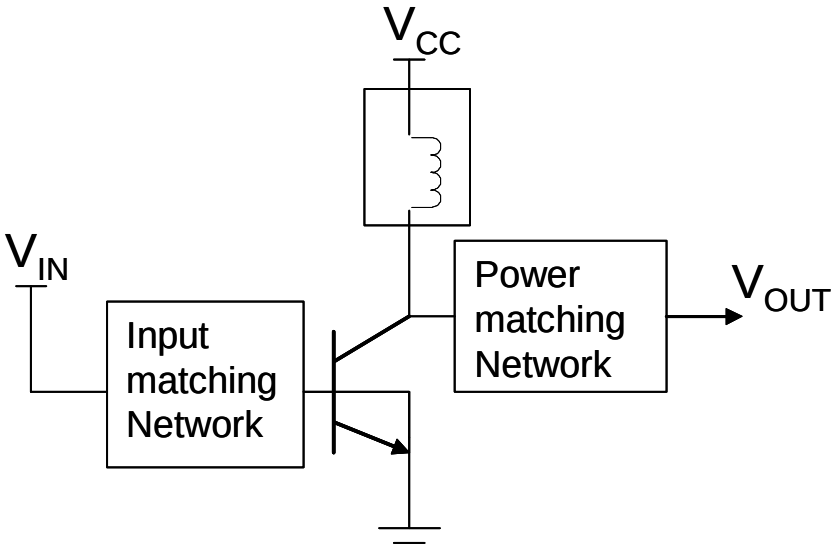
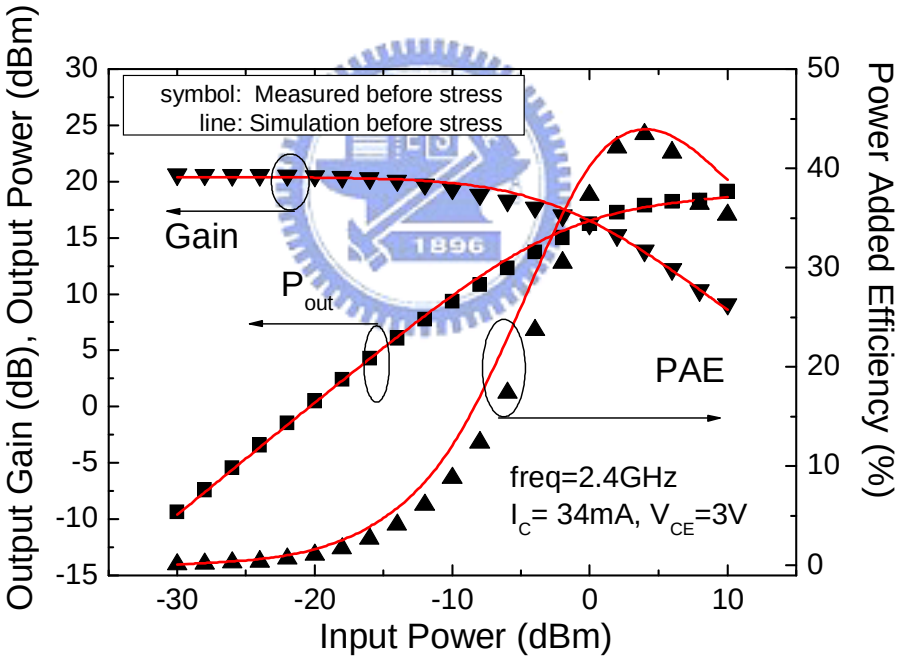


Fig. 4.8 The current gain before and after stress.



(a)



(b)

Fig. 4.9 (a) A topology of Class-A power amplifier. (b) Measured and simulated output power, power gain, and PAE before stress with a collector current kept to a constant.

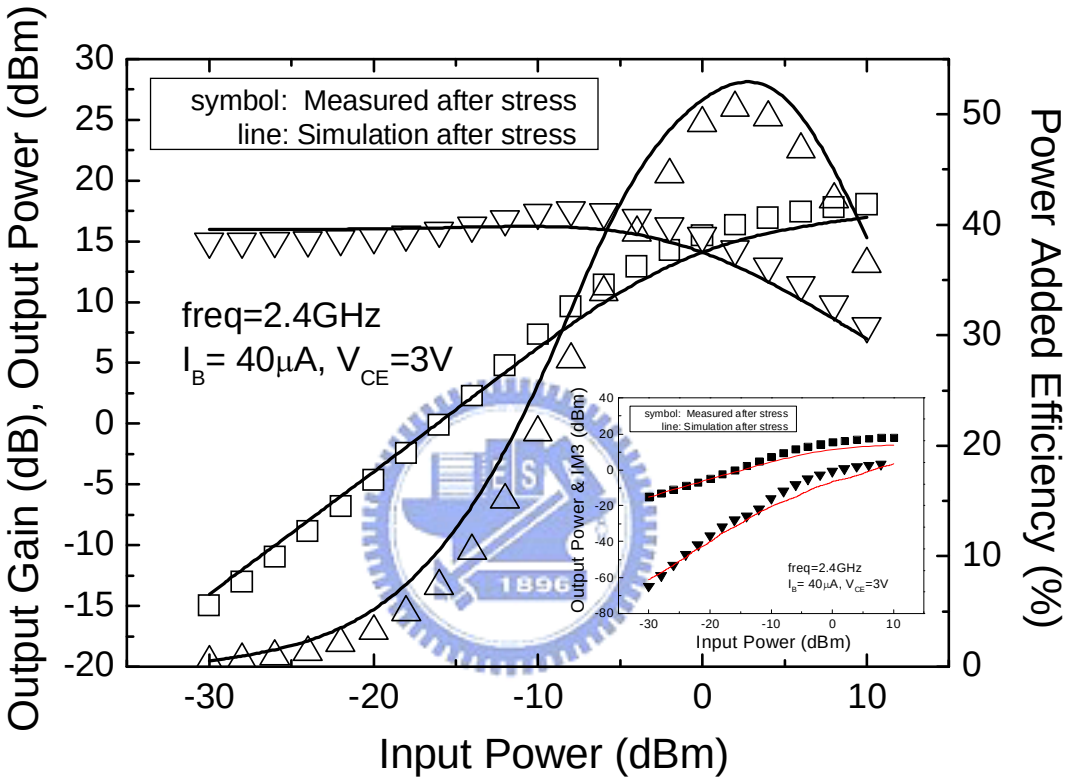


Fig. 4.10 Measured and simulated output power, power gain, PAE and IM3 after stress. The base current was kept to a constant.

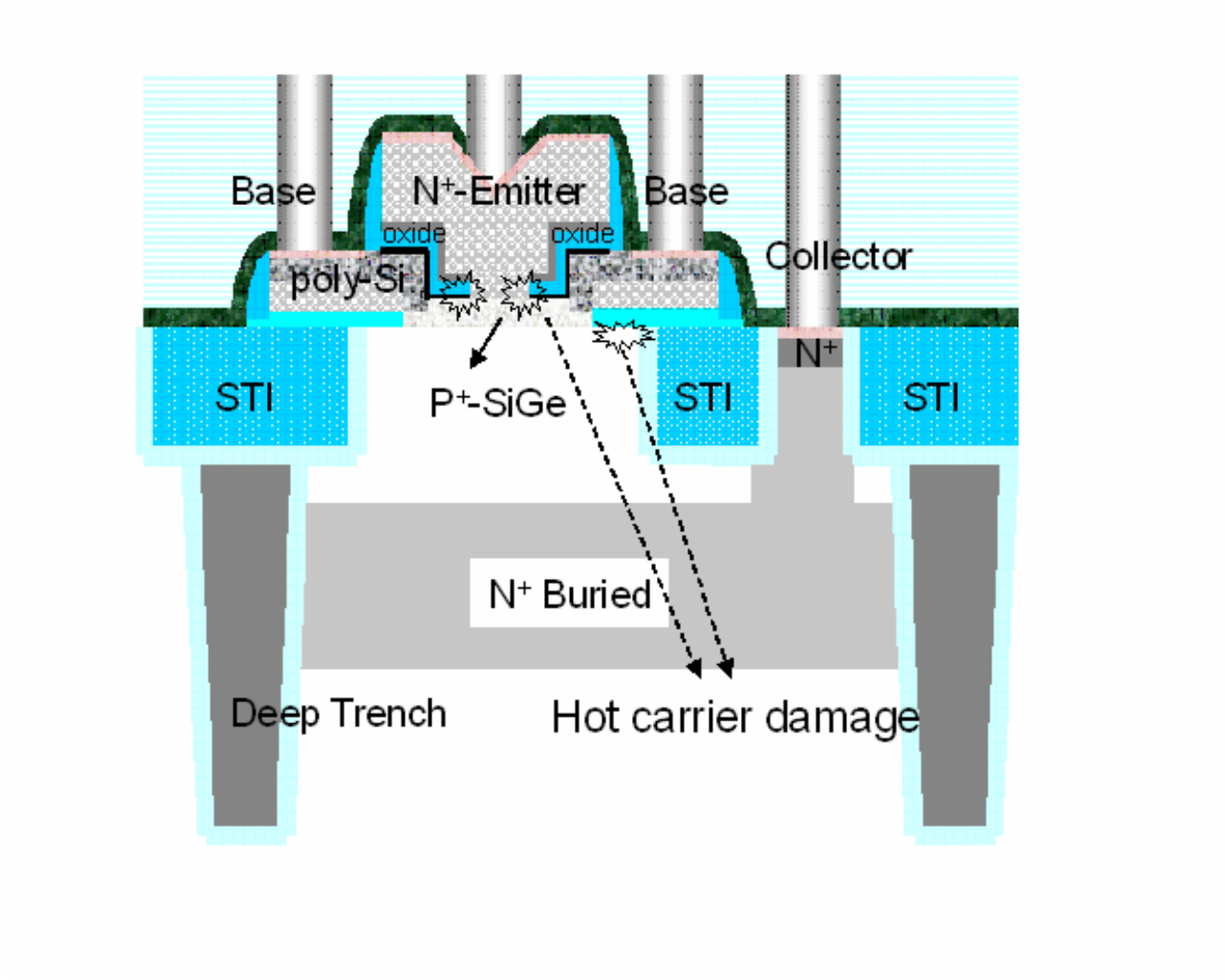


Fig.4.11 Cross-section of SiGe HBT in this work.

Chapter 5
Characterization and Modeling of RF MOSFETs under Hot Carrier Stress and Oxide Breakdown

5.1 Introduction of HCS and OBD on RF MOSFETs

CMOS technologies appear to be particularly suitable for short range, wireless system and low gigahertz applications [76], [77]. For front-end RF applications, some topologies of amplifiers can be operated in a very high drain voltage and suffer hot carrier stress (HCS) significantly. Hot-carrier generation and its effects on the characteristics of MOS transistors have been known for a long time. It is a result of high electric fields present inside the MOS transistors which naturally appear when biasing voltages are applied to a short-channel device. The general damages from the hot-carriers on a MOS transistor include the shift of the threshold voltage (ΔV_{th}), the drain current degradation (ΔI_D), and the decreasing transconductance (Δg_m). Moreover, scaling of the SiO_2-based gate dielectric in advanced MOS transistors causes a huge reduction of time to the first oxide breakdown (OBD). Consequently, the chip reliability margin shrinks dramatically [78]. In practice, some dielectric breakdown events can be tolerated by devices without causing the circuit failure. However, those post-breakdown events still degrade the RF performance of devices like noise figure, maximum oscillation frequency and linearity [79]. In this chapter, we dealt with both HCS and OBD effects on RF characteristics of MOS transistors, and in the final, we constructed a small-signal model to examine those effects on high-frequency and RF

noise performances.

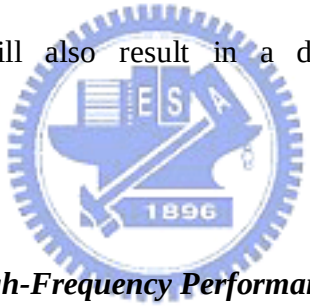
5.2 HCS and OBD Experiments

The devices under test were fabricated using a 0.13μm RF CMOS technology with channel length L= 0.12 μm and total width W_t = 158.4 μm. The gate oxide thickness was 2.2 nm. For the hot-carrier stress, the gate and drain were biased at 1.2 V and 2.4 V, respectively. This HC stress mechanism causes drain-avalanche hot carriers near the drain junction. The final HC stress time in our experiment was about 7000 seconds. For gate oxide stress, the gate terminal was subjected to a constant voltage stress under 3.9 V with source, drain and bulk terminals shorted to ground. The oxide breakdown was defined using a threshold on-stress current of 1mA.

5.3 Results and Discussion

Fig 5.1(a) shows the effects of HCS and OBD on the DC characteristics of output drain current (I_{ds}) and transconductance (g_m) of MOSFETs. After HCS, due to the generation of interface states and oxide trap charges, the drain current (I_{ds}) and transconductance (g_m) decrease and the threshold voltage (V_{th}) shifts to higher values [80]-[82]. The degradation of saturation drain current in our experiments is about 17%, and the threshold voltage is shifted from 0.42 V to 0.52 V (see Fig. 5.1 (b)). In Fig 5.1(a), the transconductance (g_m) reduces significantly, and the maximum value of g_m shifts to higher gate voltage after HC stress. We also found that g_m and drain current reduction are more serious in low gate bias region and this phenomenon is possibly due to the interface state generation and the oxide trap charge. After OBD, the drain current and transconductance also degraded due to the less control-ability of gate

electrode. In addition, it was observed that the “off” current increases dramatically after OBD. It is because of the contribution of the gate leakage currents, and it will increase the static power consumption of a MOS transistor in operation. As to the output characteristics, Fig 5.2 (a) shows the hot carrier effects on the device dc output performance. It shows an increased output conductance g_{ds} (reduced R_{out}) after hot carrier stress. Output conductance is determined from the slope of I_{DS}-V_{DS} characteristics, and it also indicates that the output gain (g_m/g_{ds}) is degraded under the hot carrier stressing. Fig 5.2 (b) shows the device dc output performance before and after oxide breakdown. We find that the drain currents after OBD decreased consistently with various gate biases, it is possibly owing to the constant leakage paths after oxide breakdown. Since the HCS and OBD affect the dc characteristics of a MOS transistor, those will also result in a degradation of high-frequency performance.



5.3-1. HCS Effects on the High-Frequency Performance of RF MOSFETs

As shown in Fig.5.3, the reduction of transconductance ($\Delta g_m/g_m$) and the increase of output conductance ($\Delta g_{ds}/g_{ds}$) with hot-carrier stressing time will result in a degradation of the output performance. The S-parameters measured for high frequency characteristics also indicate those effects. As shown in Fig. 5.4, the values of S_{11} and S_{12} are almost unchanged with increasing HC stressing time. It implies that the input reflection coefficient and isolation of the RF MOSFETs are affected slightly by HC stress. On the other hand, S_{22} and S_{21} changed more obviously under HC stressing. The degradations of S_{22} and S_{21} can be explained and highlighted again by the decrease of transconductance (g_m) and the increase of the output drain conductance (g_{ds}). It also implies that the output reflection coefficient and the voltage

gain of the RF MOSFET are affected seriously after HC stress. Moreover, it is worthwhile to pay attention to the degradation of S_{22}. The low frequency value of S_{22} strongly depends on the output impedance. After HC stress, there are a lot of defects generated by impact ionization near the drain region and those defects provide acceptor states in NMOSFETs [83]-[85]. Therefore, the electric field near the drain region will increase and the drain current is more controlled by V_D by the shielding effect on V_G from those acceptor states. As a result, the output impedance decreases, especially while biasing at high V_G shown in Fig. 5.5. However; while biasing at low V_G, owing to the reduction of the depth of depletion region, the output impedance decrease more slightly initially. After a long period of stressing time, the increase of oxide trapped charge raises the threshold voltage dramatically (see Fig. 5.1(b)), so the output impedance becomes to increase.

As to the high-frequency figures-of-merit of MOS transistors, the cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) can be expressed as a function of g_m, input intrinsic capacitances and output conductance as the following equations [86]:

$$f_T = \frac{g_m}{2\pi C_{in}} \tag{5-1}$$

$$f_{\max} \approx \frac{f_T}{\sqrt{g_{ds} \times (R_i + R_d + R_s) + 2\pi \frac{g_m C_{gd}}{C_{gs} + C_{gd}}}} \tag{5-2}$$

,where g_{ds} means the channel conductance from the source to the drain junctions, C_{gs} is gate to source capacitance, C_{gd} is gate to drain capacitance, and C_{in} is the input total capacitance. The maximum oscillation frequency, f_{max}, is a characteristic of the extrinsic device (which includes series source, drain, input, and gate resistance, R_s, R_d,

R_i, and R_g; see typical AC MOS-transistor model of Fig. 5.6). As a consequent, the degradations of dc parameters will affect the high frequency performances of transistors.

In addition to the change of g_{ds} and g_m after HC stress, the intrinsic input capacitances have also been changed, as shown in Fig.5.7. C_{gd} is less affected by HCS effects; however, the non-uniform negative trap charges result in an increase of C_{gs} after HCS. For a fresh device, there are few negative trap charges near the drain junction, hence the electric small-signal passes uniformly from source to drain terminal. However, due to the appearing negative trap charges under HCS, the C_{gs} increases dramatically with the increasing electron-hole pairs [87], [88]. Those changes after HCS will result in a more serious degradation of the RF performance.

Fig.5.8 shows the degradations of f_T and f_{max} as a function of g_m degradation. The degradation of f_T is almost proportional to g_m degradation after HCS, indicating that the f_T degradation is mainly contributed from g_m degradation. Form eq.(5-2), f_{max} is related to $g_m^{1/2}$, g_{ds} and the ratio of C_{gd}/C_{gg}.

5.3-2. A Constructed Small-Signal Model of RF MOS transistors under OBD

Due to the generation of the interface states and oxide traps after oxide breakdown (OBD), the “on” drain current and transconductance all decrease. After oxide hard breakdown, the degradation of saturation drain current is about 9% and threshold voltage is shifted from 0.42V to 0.48V (see Fig. 5.1 and Fig.5.2). Moreover, it is obvious that the “off” current increases dramatically after hard breakdown due to the contribution of the gate leakage current. It will increase static power consumption of a MOSFET in digital operation. To examine the HCS and OBD effects on the RF characteristics, we re-constructed a small-signal model as shown in Fig.5.9, where the

$g_m=g_{m0}\exp(-jw\tau)$ is varied with the frequency response. After de-embedding the pad parasitic parameters, the cold-FET method was adopted in this model to extract the parasitic resistances R_g, R_d and R_s [89]. Then, the substrate associated parameters like R_{bk} and C_{bk} can be extracted by using a curve-fitting method [90]. The main intrinsic network parameters of this model can be directly extracted by the transformed Y parameters as the following equations [91]:

$$C_{gs} = \frac{1}{\omega}\mathrm{Im}(Y_{i,11} + Y_{i,12}) \tag{5-3}$$

$$C_{gd} = \frac{-1}{\omega}\mathrm{Im}(Y_{i,12}) \tag{5-4}$$

$$C_{ds} = \frac{1}{\omega}\mathrm{Im}(Y_{i,22} + Y_{i,12}) \tag{5-5}$$

$$R_{ds} = \frac{1}{R_e(Y_{i,22})} \tag{5-6}$$

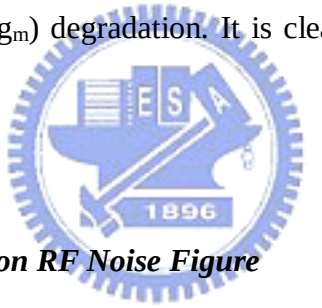
$$g_{m0} = Magnitide(Y_{i,21} + Y_{i,12}) \tag{5-7}$$

$$\tau = -\frac{1}{\omega}Phase(Y_{i,21} - Y_{i,12}) \tag{5-8}$$

Due to the gate leakage induced after OBD, we can assume that there are two leakage paths generated from gate to source and gate to drain regions. Therefore, we added a gate-to-source resistance (R_{gs}) and a gate-to-drain resistance (R_{gd}) into the modified small-signal model after OBD. The extracted parameters of the constructed model were listed in Table 5-1. Under the HCS, the main affected parameters are the transconductance (g_m) and gate-to-source capacitance (C_{gs}). For device after OBD, R_{gs} and R_{ds} are not infinite, so the eq.(5-1) and eq.(5-2) should be modified. Based on the modified model, the cutoff frequency can be approximated as:

$$f_T \approx \frac{g_m - \frac{2}{R_{gd}} - \frac{1}{R_{gs}}}{2\pi(C_{gs}+C_{gd})} \qquad (5\text{-}9)$$

As shown in Fig.5.10, not only the f_T is deceased by the OBD; since f_{max} is directly proportional to the power gain of the MOS transistor, the new leakage paths in the gate oxide result in the power loss and the degradation of f_{max}. Moreover, compare the effects of HCS and OBD on the MOS transistor's high-frequency performance in Fig. 5.11, the cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) reduce significantly after oxide breakdown than that after the hot carrier stress at the same dc (g_m) degradation. It is clearly owing to the existence of R_{gs} and R_{gd}.



5.3-3. HCS and OBD Effects on RF Noise Figure

Noise is one of the major concerns of RF devices, and it is sensitive to g_m and resistance parts of a MOS transistor. Fig. 5.12 shows the minimum noise figure (NF_{min}) measured before and after hot carrier stress and oxide breakdown. The NF_{min} increased after HCS mainly due the reduction of transconductance (g_m). However, it can be observed that NF_{min} increased more significantly after OBD than that after HCS. This is because not only the decreasing g_m occurred after oxide breakdown, but also the resistant paths of gate leakage currents appeared. The impact of so-called gate shot noise ($2qI_G$) is associated with the gate leakage current in MOS transistors. Gate shot noise is usually neglected in MOS transistors. The gate leakage currents in typical MOS transistors are always controlled well for state-of-the-art CMOS

products. However, in this case of RF MOSFET after OBD, the gate shot noise would play a non-disregarded role in determining the high frequency noise in a MOS transistor [92], [93]. In order to analyze the main trends of RF noise figure related HCS and OBD on MOS transistors, we adopt a lumped-element common-source equivalent circuit and limit our attention to the intrinsic MOSFET as shown in Fig. 5.13. It indicates that the resistant noise generators include the drain noise current, induced-gate noise current and gate shot noise current as shown in Fig. 5.13(a). The equivalent input noise generators of Fig. 5.13(b) and the correlation admittance Y_C (5-10) are evaluated first; then the analytical expressions for the two-port common-source noise parameters (noise resistance R_n, optimum admittance Y_{OPT}, minimum noise factor F_{min}) are determined.

$$Y_C = \overline{i_n v_n^*} \Big/ \overline{v_n^2} = G_C + jB_C \tag{5-10}$$

$$Y_{OPT} = G_{OPT} + jB_{OPT} \tag{5-11}$$

$$R_n = \frac{\overline{v_n^2}}{4kT\Delta f} \approx R_g + \frac{S_{id}}{4KTg_m^2} + R_g^2 \frac{S_{ig}}{4KT} \tag{5-12}$$

Then,

$$G_{OPT} = \sqrt{\overline{i_n^2} \Big/ \overline{v_n^2} - B_{OPT}^2} = wC_{gs}\sqrt{\frac{\delta\alpha^2(1-c_G^2)}{5\gamma} + \frac{g_m\alpha(2qI_G)}{4kT\gamma(w^2C_{gs}^2)}} \tag{5-13}$$

$$F_{\min} \approx 1 + 2R_nG_{OPT} \tag{5-14}$$

, where $\alpha \equiv g_m/g_{d0}$, with g_{d0} being the drain conductance for V_{DS}=0V. γ, δ and c_G are parameters for the models for drain noise and induced gate noise. Notice that R_n is

dominated by the drain thermal noise current and depends on the value of device transconductance (g_m). In addition, G_{OPT} presents contributions from induced-gate noise current and from the gate shot noise current. Therefore; two limit cases of RF noise before and after HCS and OBD in our experiments can be recognized.

1) In the case of typical MOS transistor before and after HCS, the gate leakage (I_G) is relatively small; then, the G_{OPT} and F_{min} are dominated by the drain and induced gate thermal noise. So, (5-14) simplifies to (5-15), and is increasing with frequency, and can be lessoned by device cutoff frequency (f_T).

$$F_{\min} \approx 1 + 2(\frac{f}{f_T})\sqrt{\frac{\gamma\delta(1-c_G^2)}{5}} \tag{5-15}$$

2) On the other hand, if I_G/w^2 is large enough, gate shot noise becomes dominant in the expression for G_{OPT}, and (5-14) leads to (5-16).

$$F_{\min} \approx 1 + \sqrt{\frac{2qI_G\gamma}{kT\alpha g_m}} \tag{5-16}$$

In Fig. 5.14(a), it shows the equivalent noise resistance (R_n) before and after HCS and OBD. We found the R_n increased more dramatically under HCS than OBD due to the much decreased g_m after HCS. Moreover, Fig. 5.14(b) presents the optimum input reflection coefficient. The magnitude of G_{OPT} shows a value of 0.68 after OBD, which is much less than the value of 0.94 before stress. This is owing to the appearance of leakage current path of resistance $R_{leakage}$, which we departed into R_{gs} and R_{gd}. In addition, G_{OPT} also shows no dependence of frequencies after oxide breakdown.

5.4 Summary

In this chapter, we examined the effects of hot carrier stress (HCS) and oxide breakdown (OBD) on the RF characteristics of MOS transistors. By using a constructed small-signal model, we can clarify the effects of hot carrier and oxide breakdown. In addition, a gate-to-source resistance and a gate-to-drain resistance were added to the constructed small-signal model to illustrate the effects of gate leakage currents after oxide breakdown. From the experimental observations in Table 5-2, HCS and OBD induced degradations on RF performance should be taken into consideration in the design of RF CMOS integrated circuits.

Table 5-1 Small-signal model parameters before and after HCS and OBD.

	R_g (Ω)	R_d (Ω)	R_s (Ω)	R_{ds} (Ω)	R_{bk} (Ω)	C_{gd} (pF)	C_{gs} (pF)	C_{ds} (pF)	C_{jd} (pF)	C_{bk} (fF)	g_{mo} (mS)	R_{gs} (Ω)	R_{gd} (Ω)
Fresh	1.7	7.71	3.51	75	1400	0.0574	0.215	0.38	0.358	3	270	--	--
After HCS	1.7	7.89	3.52	76.2	1400	0.0578	0.239	0.38	0.358	3	240	--	--
After OBD	1.84	7.76	3.51	68.7	1400	0.0578	0.221	0.38	0.358	3	253	6540	33k

Table 5-2 Comparison of DC and RF parameters before and after HCS and OBD.

(1) DC parameter deviation:

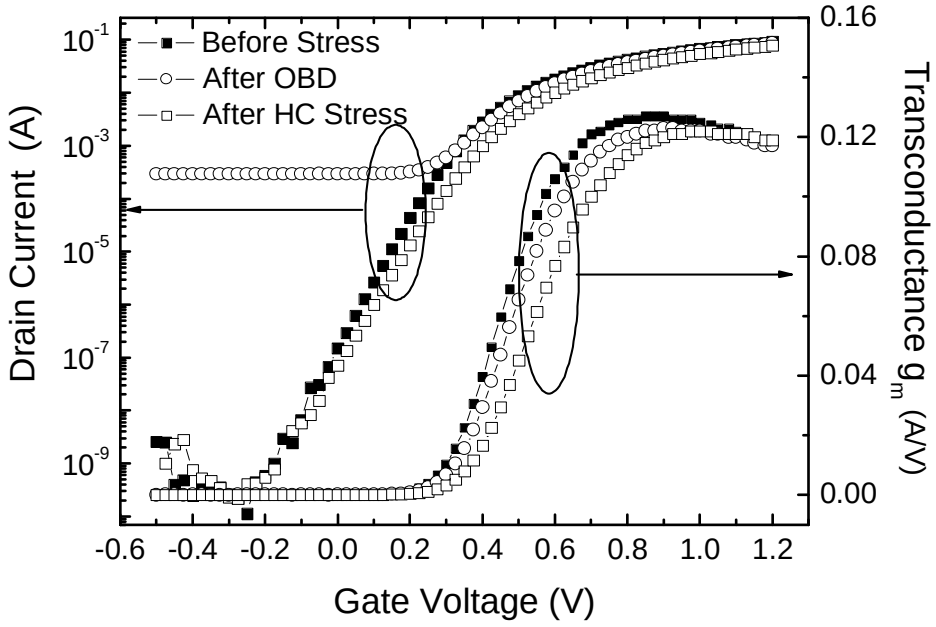
	I_d	g_m	V_{th}	g_{ds}	C_{gs}	C_{gd}
HCS	-17%	-11%	0.1V	9.2%	12%	0.7%
OBD	-9%	-6%	0.06V	2%	2.7%	-

(2) RF figures-of-merit deviation:

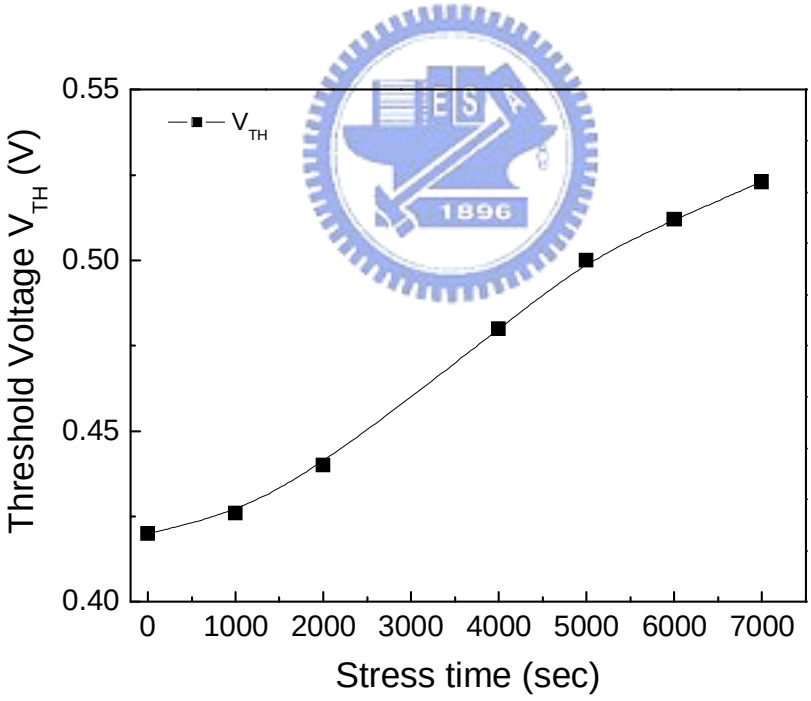
	f_T	f_{max}	NF_{min} (dB)	R_n (Ω)
Initial	-	-	0.18	18.6
HCS	-9.7 %	-4.2 %	0.43	27
OBD	-7.6 %	-3 %	0.66	21

(3) Co-relation between DC parameters and RF FoM.

$$\begin{bmatrix} \Delta f_T \\ \Delta f_{\max} \\ \Delta NF_{\min} \\ \Delta V_{ip3} \\ .... \end{bmatrix} = \begin{bmatrix} \frac{\partial f_T}{\partial g_m} & 0 & 0 & \frac{\partial f_T}{\partial C_{gs}} & \frac{\partial f_T}{\partial C_{gd}} & 0.... \\ \frac{\partial f_{\max}}{\partial g_m} & 0 & \frac{\partial f_{\max}}{\partial g_{ds}} & \frac{\partial f_{\max}}{\partial C_{gs}} & \frac{\partial f_{\max}}{\partial C_{gd}} & \frac{\partial f_{\max}}{\partial R_g}.... \\ \frac{\partial NF_{\min}}{\partial g_m} & 0 & \frac{\partial NF_{\min}}{\partial g_{ds}} & \frac{\partial NF_{\min}}{\partial C_{gs}} & \frac{\partial NF_{\min}}{\partial C_{gd}} & \frac{\partial NF_{\min}}{\partial R_g}.... \\ \frac{\partial V_{ip3}}{\partial g_m} & \frac{\partial V_{ip3}}{\partial g_{m3}} & \frac{\partial V_{ip3}}{\partial g_{ds}} & 0 & 0 & 0.... \\ ..... & & & & & \end{bmatrix} \begin{bmatrix} \Delta g_m \\ \Delta g_{m3} \\ \Delta g_{ds} \\ \Delta C_{gs} \\ \Delta C_{gd} \\ \Delta R_g \\ ..... \end{bmatrix}$$

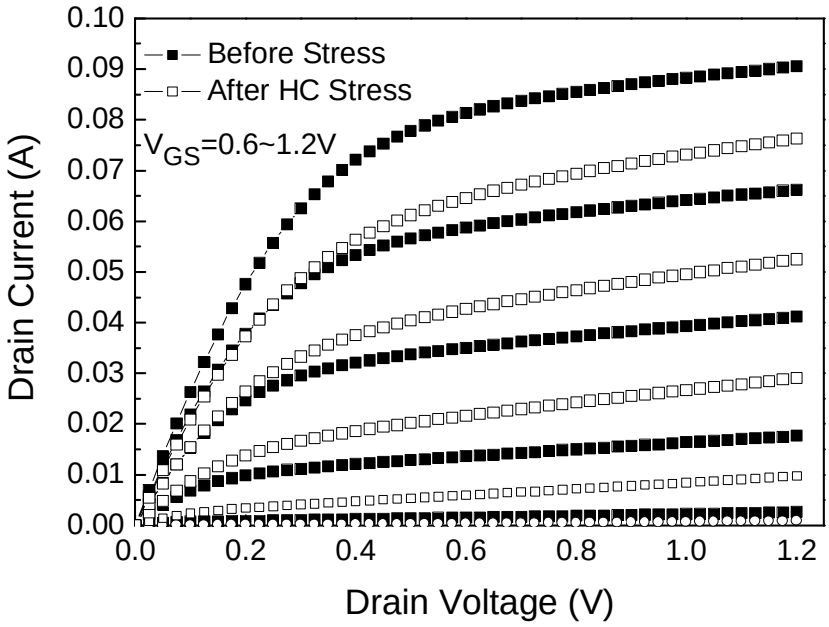


(a)

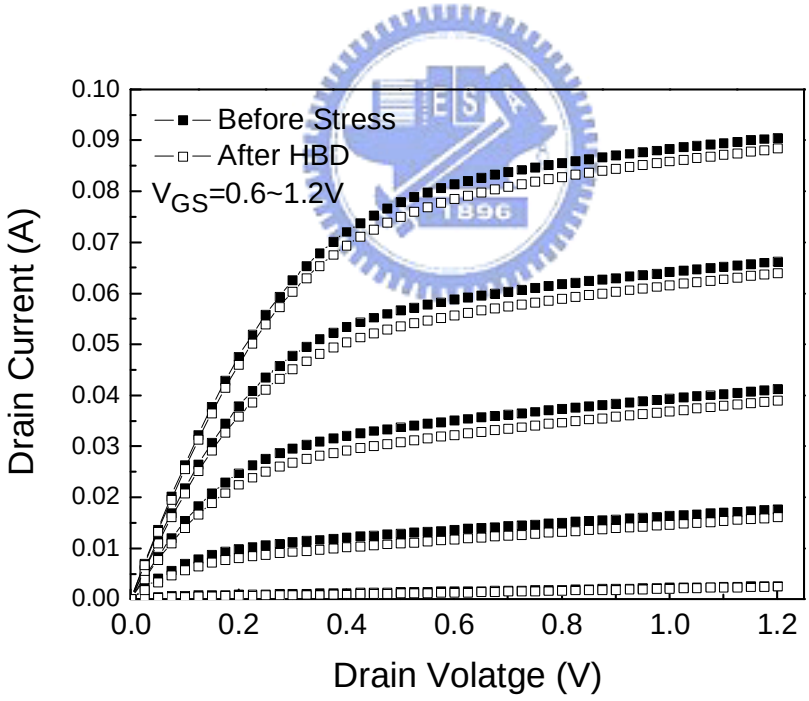


(b)

Fig. 5.1 (a) DC characteristics of a MOSFET before and after hot carrier stress and oxide breakdown. (b) The threshold voltage measured with the HC stressing time.



(a)



(b)

Fig. 5.2 Output I-V characteristics of MOS transistor (a) after hot-carrier stress, (b) after oxide breakdown.

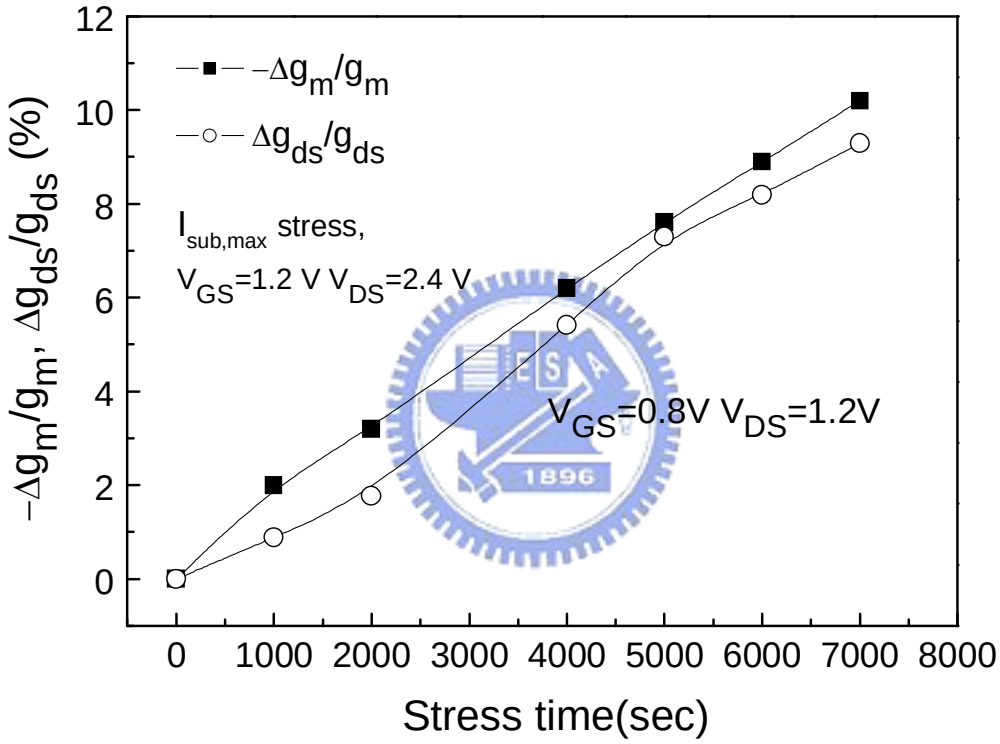
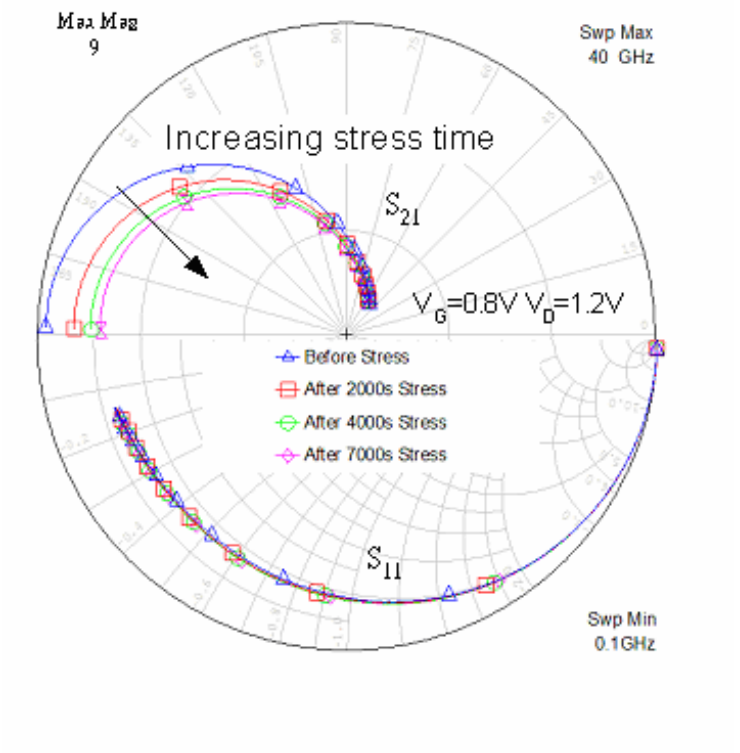
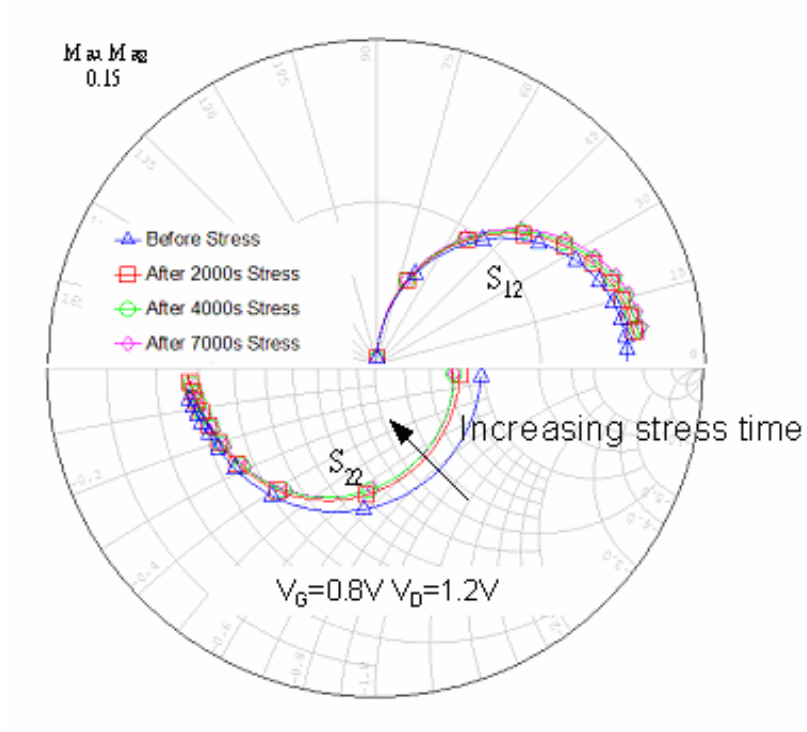


Fig. 3 Variations of the extracted transconductance and output conductance with increasing HC stressing time.



(a)



(b)

Fig. 5.4 S-parameters measured with the HC stressing time.

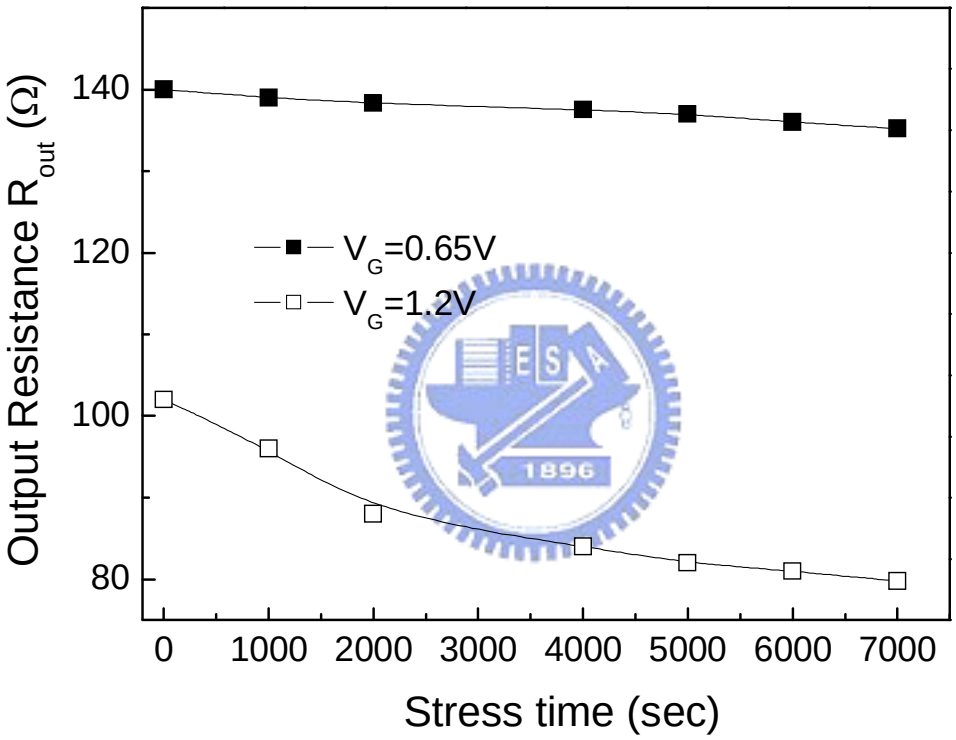


Fig. 5.5 Output impedance versus stress time at different bias condition.

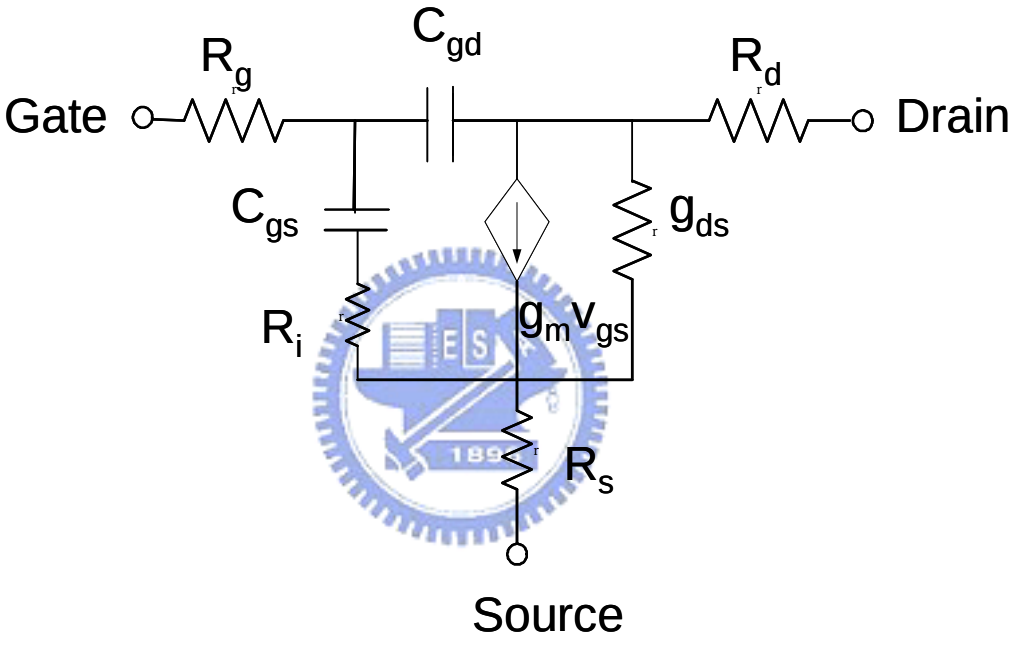


Fig. 5.6 A constructed small-signal model for MOS transistor.

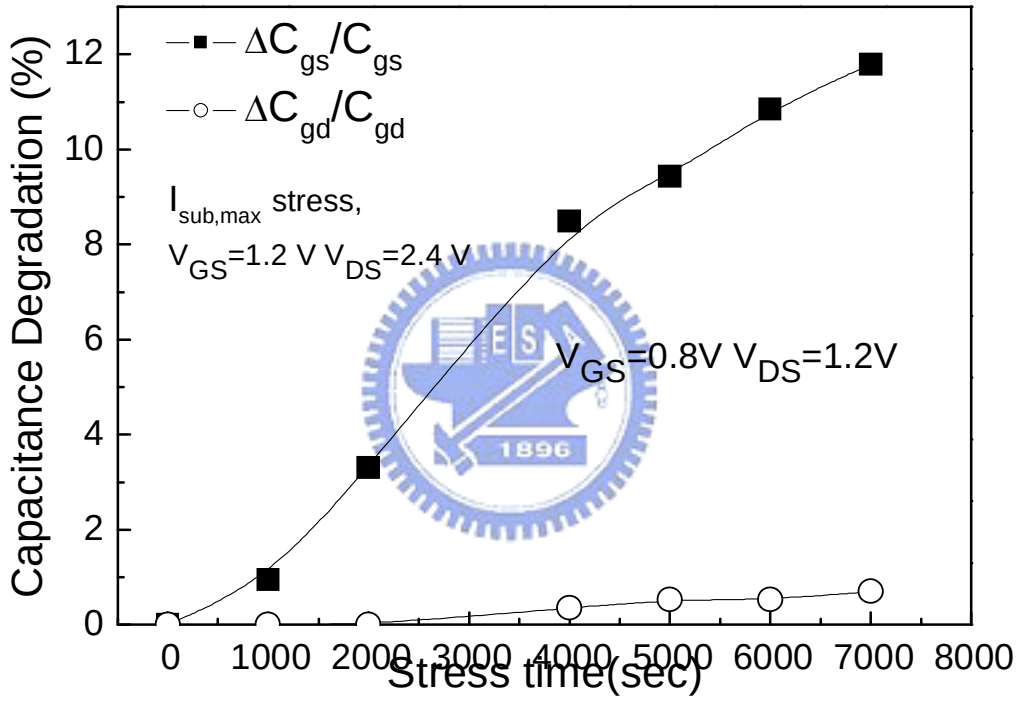


Fig. 5.7 Capacitance degradation with increasing HC stressing time.

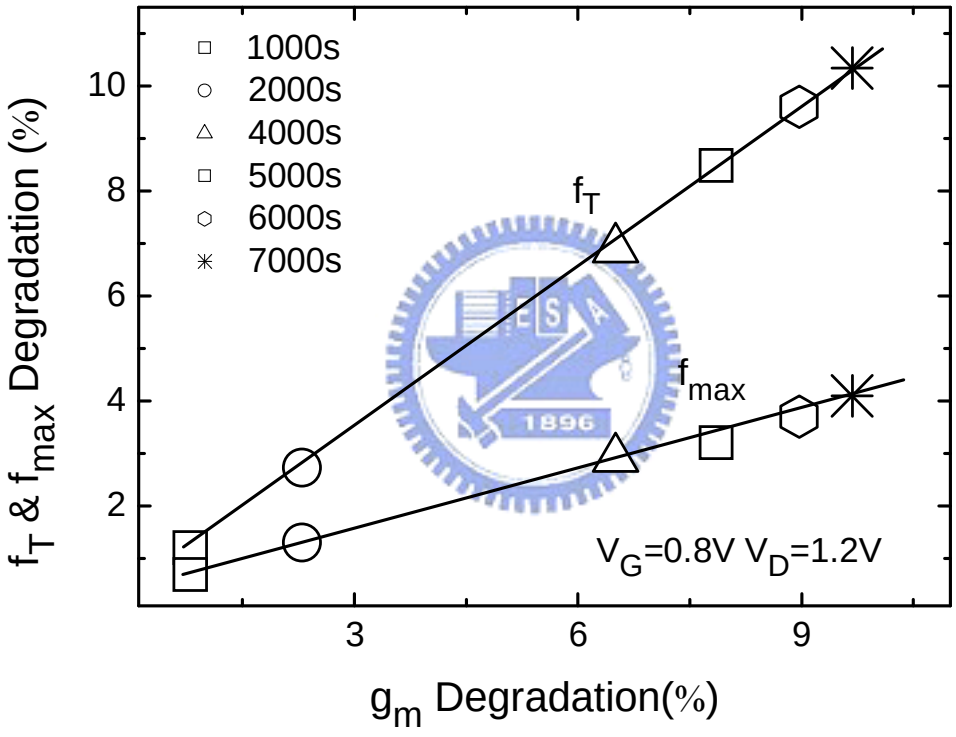


Fig.5.8 Relation between f_T and f_{max} degradations and g_m degradation.

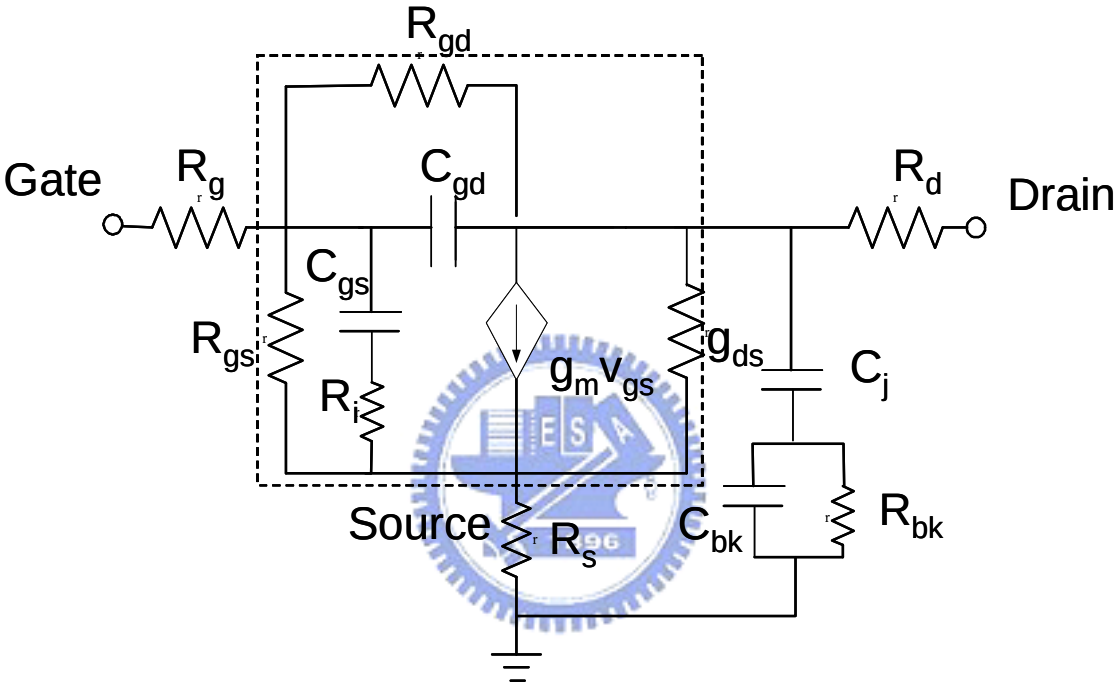
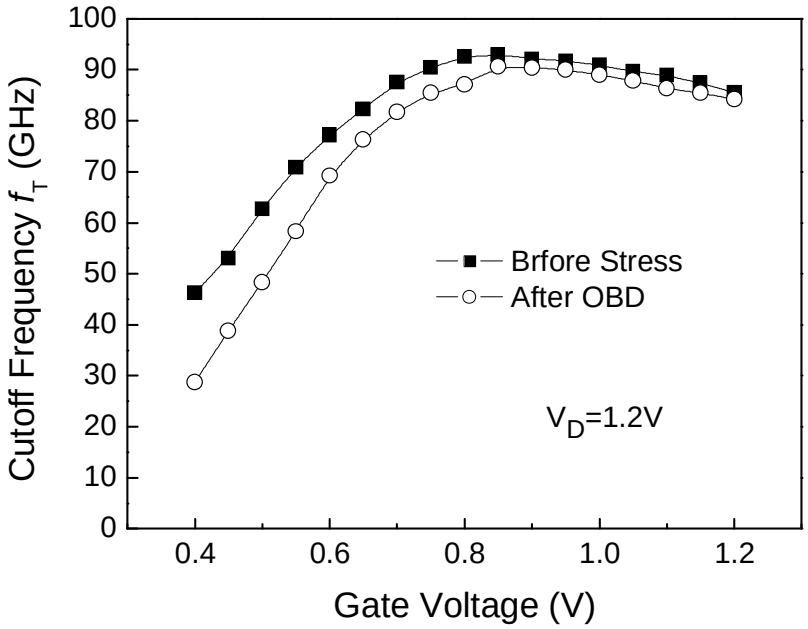
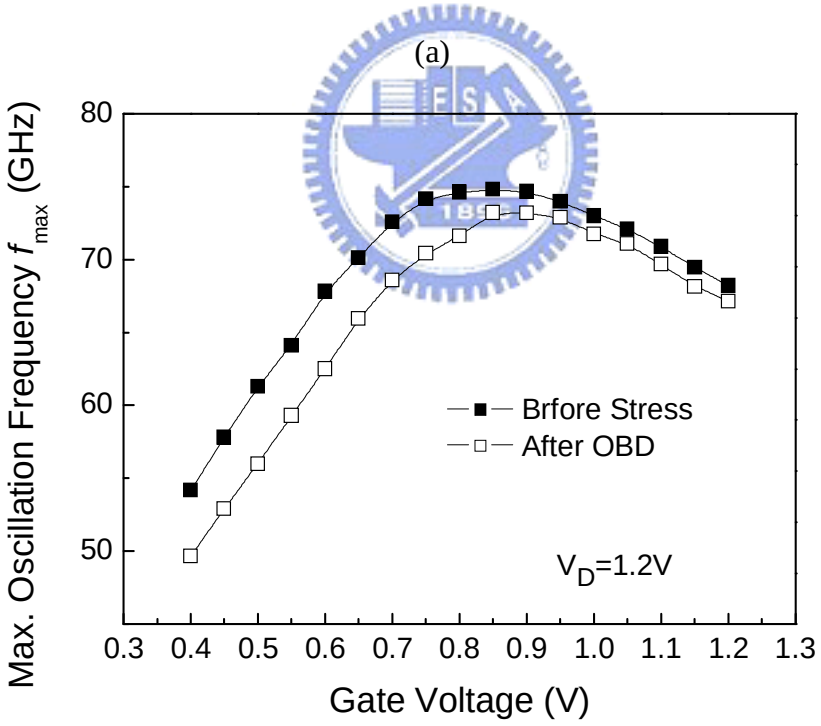


Fig. 5.9 A re-constructed small-signal model for MOS transistor with the leakage current paths of R_{gs} and R_{gd}.



(a)



(b)

Fig. 5.10 (a) Cutoff frequency and (b) maximum oscillation frequency measured with the gate voltage before and after oxide breakdown.

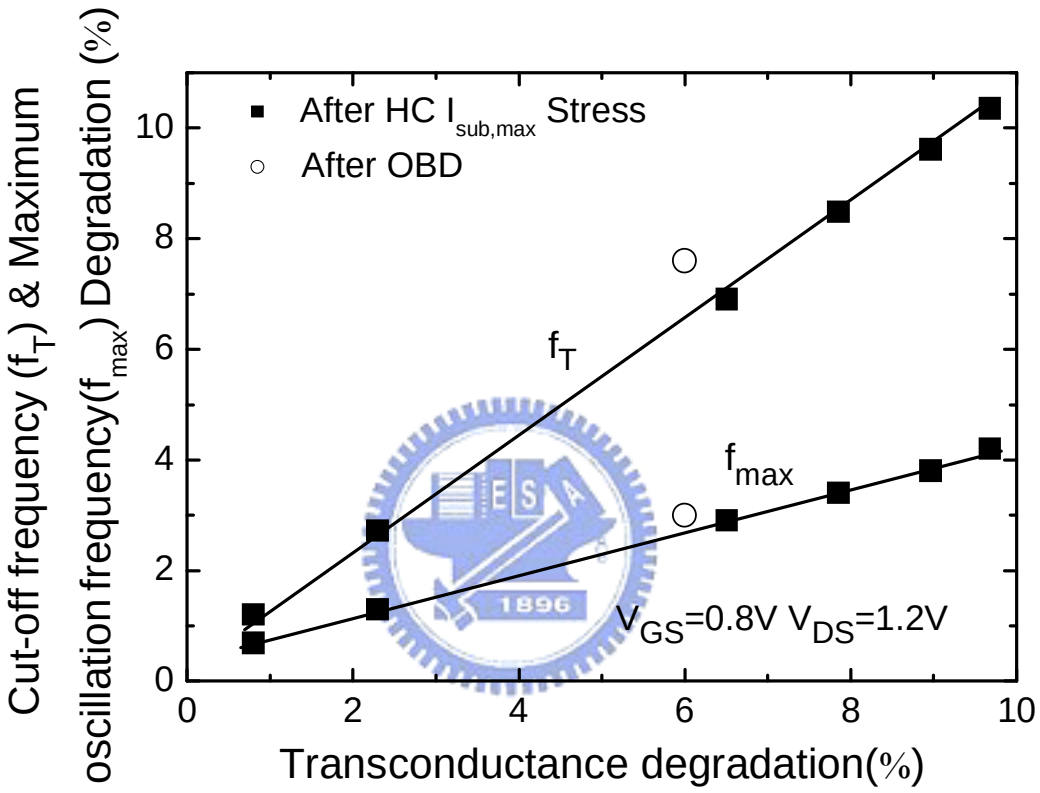
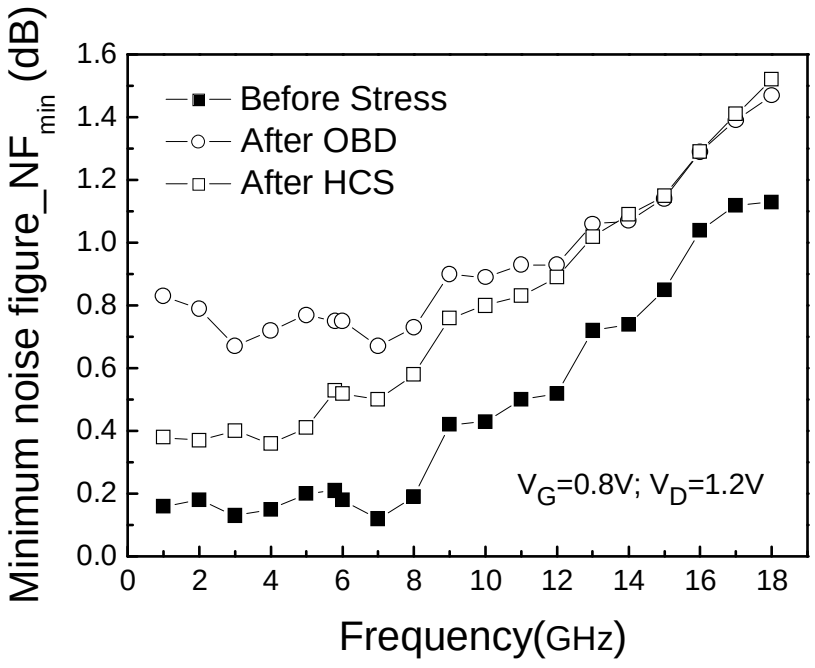
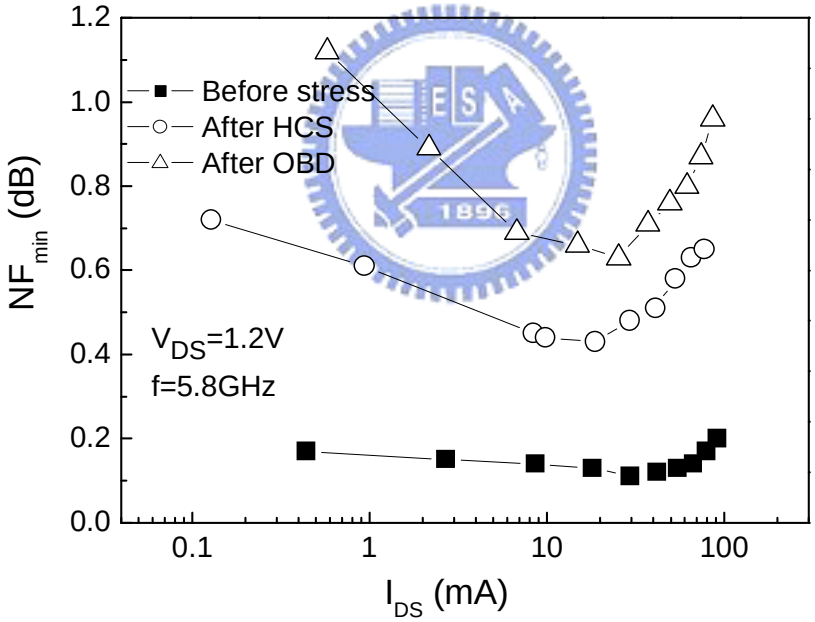


Fig. 5.11 Relation between f_T and f_{max} degradations and g_m degradation after hot carrier stress and oxide breakdown.

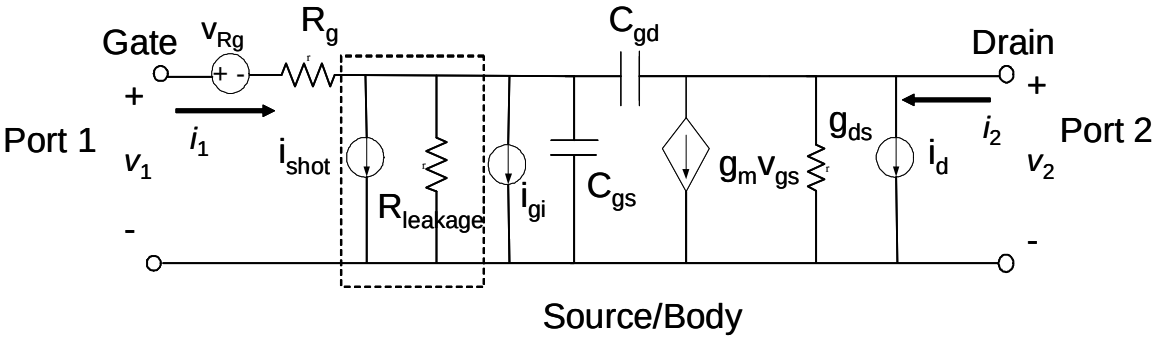


(a)



(b)

Fig. 5.12 Minimum Noise Figure degradations before and after hot carrier stress and oxide breakdown with increasing (a) frequencies, (b)I_{DS}.



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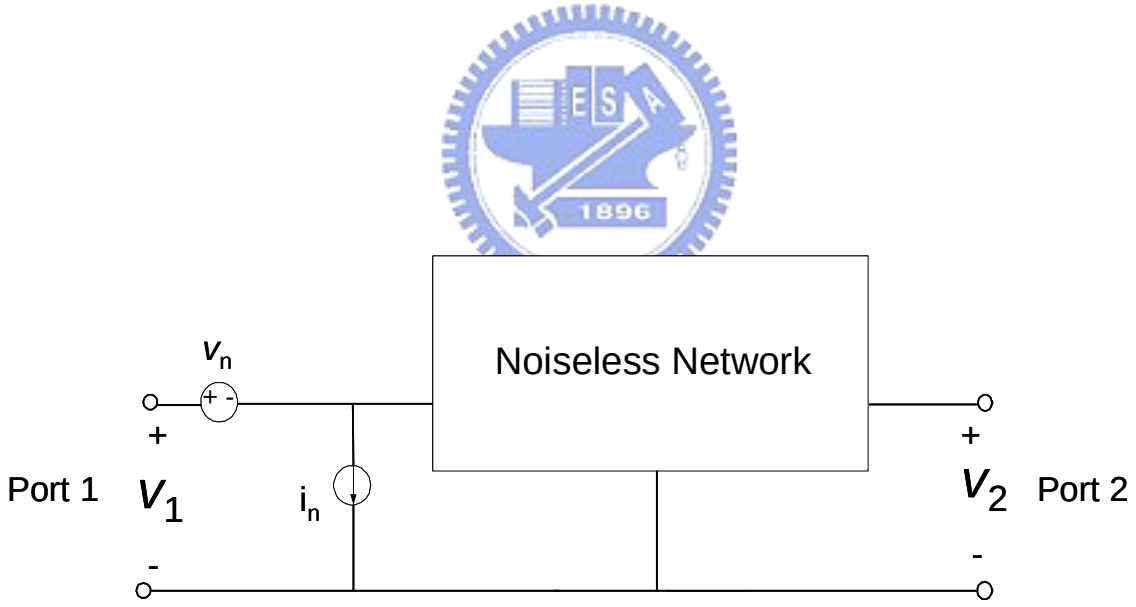
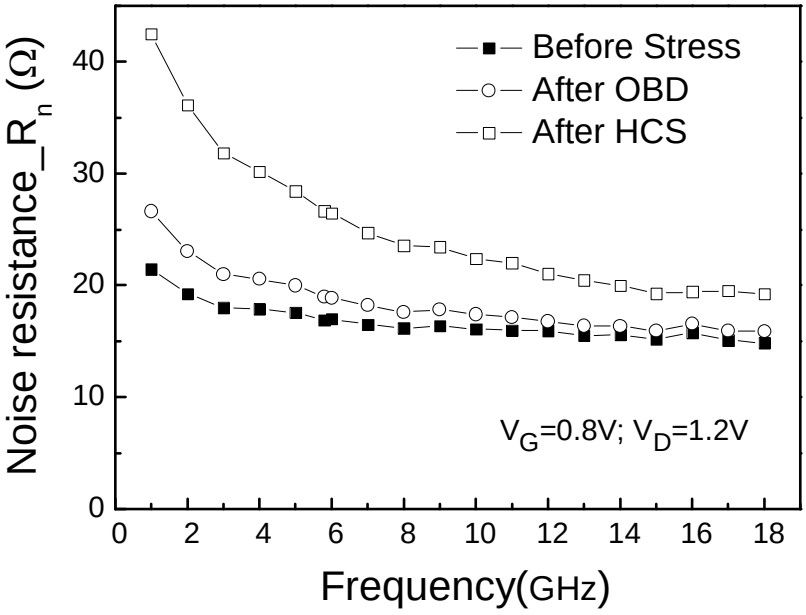
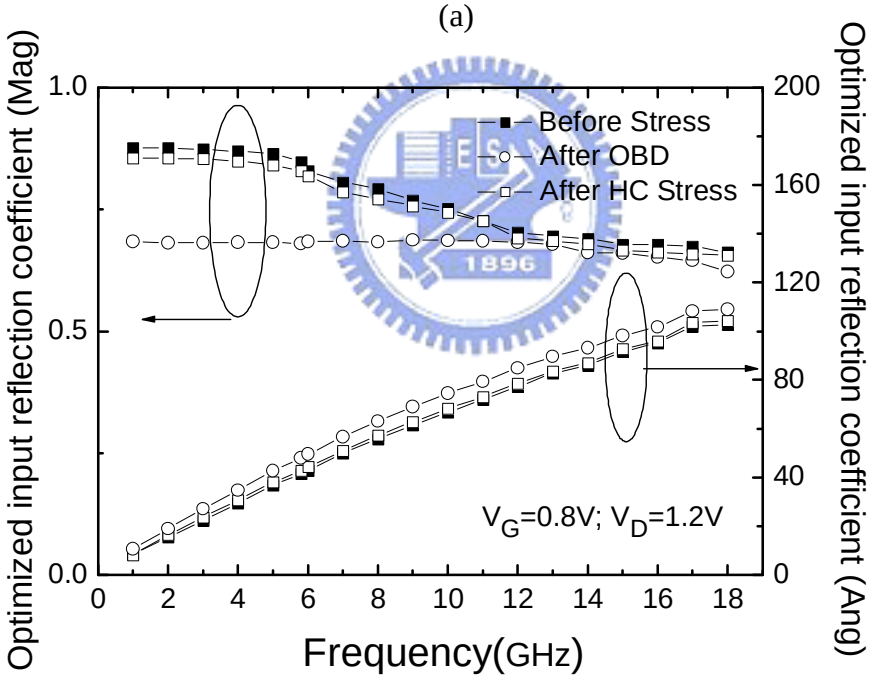


(b)

Fig. 5.13 (a) Equivalent linear lumped-element circuit for MOS transistor including noise sources. (b) Equivalent noiseless network with input referred voltage and current generators.



(a)



(b)

Fig. 5.14 (a) Equivalent noise resistance and (b) Optimized input reflection coefficient before and after HCS and OBD.

Chapter 6

Impact of Reliability issues on Power Characteristics of RF MOS transistors

6.1 Introduction

In this chapter, we investigate reliability issues including the HCS and OBD on the RF power and linearity characteristics of a MOS transistor by using load-pull measurement. With the scaling technologies of advanced MOS transistors in recent years, some of the electrical parameters like transconductance (g_m), output conductance (g_{ds}), input resistance (R_g), and AC capacitances (gate-to-source, gate-to-drain, and gate-to-bulk; C_{gs}, C_{gd}, and C_{gb}) are getting much more sensitive to high-frequency characteristics, especially to the high-frequency power performance [94]-[96]. RF performances of an advanced MOS transistor are concerned to the power delivery from the input source to the output load, which is really concerned for an analog/RF circuit designer. It is worth to be considered, while the output current, threshold voltage, transconductance and output conductance are degraded by the reliability issues. In this chapter, we examined two of the main reliability issues, hot-carrier stress and critical gate-oxide breakdown, on the RF power characteristics of advanced MOS transistors [97], [98].

6.2 Experiments of HCS and OBD

Multi-finger MOS transistors used in this work were fabricated using a 0.13 μm

baseline technology with channel L=0.12 μm and the channel width W=7.2(μm)×16(finger). The oxide thickness t_{ox} is 20 Å. The devices depict RF characteristics with the cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) up to 110 GHz and 90 GHz, respectively. During the hot carrier stress, the gate and drain of the test transistors were biased at 1.4V and 2.4V, respectively, with a stressing time 15000 seconds. The critical gate oxide stress is under a constant voltage stress (V_g=3.9V) with other terminals are subjected to ground. The oxide breakdown was defined using a threshold on-stress current of 1mA. The dc device characteristics were tested by an Agilent 4156B precision semiconductor parameter analyzer, while the output power and RF linearity were measured using an ATN load-pull system with two-tone mode. The measurement frequency and tone spacing were 2.4 GHz and 1 MHz, respectively.

6.3 Results and Discussion

6.3.1 Hot Carrier Effects on Power Performance

The general effect of HC stress on the dc performance of MOS transistors is shown in Fig. 6.1. After HC stress the degradation of saturation drain current in our experiment is 25%, and the threshold voltage is shifted from 0.39 V to 0.42 V. In Fig. 6.2, it shows the g_m degradation after HC stress. We found that the g_m reduction is more serious in low gate bias regions. The degradation of dc parameters could be suggested possibly to the interface state generation and the oxide trapped charges [101], [105]. Furthermore, due to the non-uniform distribution of defects after HC stress, the output drain conductance increases especially in higher gate voltage biases

[106]. Those all influence the behavior of RF performance and power characteristics of MOS transistors. The effect of HC stress on the output power of a MOS transistor is shown in Fig. 6.3. It was measured at gate voltage V_{GS}=0.8 V and drain voltage V_{DS}=1.2 V, where the g_m is the maximum value in device saturation regions, and the frequency was operated at 2.4 GHz. The source and load impedances are matched for maximum output power before stress. Because the fundamental output power of a MOS transistor is basically correlated to g_m/g_{ds}, the HC-induced degradation of the dc parameters will lead to a reduction of output power and gain. After HC stress the output conductance has changed, the load impedance will deviate from the maximum output power condition, making the further reduction of output power [99]-[101].

In Fig. 6.4, it shows the power gain as a function of gate voltage biases. The power gain reduces after HC stress. However, as the gate voltage bias increases to a higher value, the power gain which was degraded by the HC effect shows a consistent value with the fresh one. As the source and load impedances are matched for maximum output power, the available power gain can be expressed as eq.(6-1)

$$Ga,\max = \frac{f_T^2}{4f^2(2\pi \cdot f_T \cdot R_g \cdot C_{gd} + G_{ds} \cdot R_{in})} \tag{6-1}$$

,where, f_T is the cut-off frequency, and R_g, C_{gd} are the gate resistance and gate-to-drain capacitance of the MOS transistor, respectively. From eq.(6-1), we can find the maximum available power gain is proportional to f_T thus is correlated to g_m. Therefore, after HC stress the power performance in Fig. 6.4 shows a consistent curve with the transconductance in Fig. 6.2. It also suggested that biasing at a higher gate voltage is more robust to HC stress. However, in order to reduce static power consumption in analog/RF applications, they are going to be biased at much lower V_{GS} than digital

devices thus are more vulnerable to HC stress.

6.3.2 Hot Carrier Effects on Linearity

To characterize the linearity, the third-order intercept point (*IP3*), at which the output power and third-order intermodulation (IM3) power are equal, is commonly used. For low distortion operation, the third-order intercept point should be as high as possible. As shown in Fig. 6.3, by the two-tone test, the output *IP3* (*OIP3*) reduces from 21 dBm to 15.8 dBm after HC stress, while the input referred *IP3* (*IIP3*) reduces from -3.6 dBm to -6 dBm. Hence, the RF linearity degrades under HC stress when the MOSFET operates at a fixed gate bias. RF linearity of devices doesn't change much with frequency related to the much linear voltage dependence of gate capacitance, so it can be well analyzed from the dc and ac characteristics of devices. The third-order point of gate voltage amplitude, where the fundamental and IM3 output amplitude of drain current are equal, can be given as [103]

$$VIP3 = \sqrt{\frac{4g_m}{3g_{m3}}} \tag{6-2}$$

,where g_{m3} is the third-order Taylor expansion coefficient of drain current versus gate voltage. It gives a good indication of device linearity even at high frequency [103]. The parameters, g_m and g_{m3}, can be directly extracted from the dc characteristics. Actually, the equation (6-2) is obtained without considering the non-linearity of output conductance. Because the amount of output conductance non-linearity is much smaller than that of transconductance when devices operate in saturation region, it can

be negligible for low load impedance condition [102], [103].

Fig. 6.5 shows the *VIP3* measured with V_{GS}-V_{TH} (V_{TH} is the threshold voltage) of a MOSFET before and after stress. With a fixed $V_{GS} - V_{TH}$ bias condition, we can ignore the shift of the threshold voltage, and observe that the *VIP3* shows a slightly change after stress with a typical analog bias conditions, i.e. 0.1V< $V_{GS} - V_{TH}$ < 0.6V. It indicates that the degradation of linearity after stress at a constant gate bias condition is mostly due to the shift of threshold voltage. The observation in Fig. 6.5 is interesting and indicates that although the hot carrier stress affects the transconductance and threshold voltage of the device, its effects on linearity of the transistor can be alleviated as $V_{GS} - V_{TH}$ is kept at a constant. That is to say, RF linearity is less affected by HC stress if biasing the MOSFET at constant drain currents as shown in Fig. 6.6. We found that *OIP*3 and *IIP*3 only show a slightly change after stress for the device measured at a fixed output drain current. It is noted that *OIP3* decreases slightly on middle drain currents due to the decreased power gain after stress.

From Fig. 6.5, we observe the *VIP3* increases after HC stress at low bias condition, which can be explained by the increase of linearity at lower drain currents. Because the HC stress will affect the threshold voltage, channel mobility, subthreshold swing, and source/drain resistance, their effects on *VIP3* have to be studied. In general, the effective channel mobility in strong inversion region can be expressed as [107]

$$\mu_{eff} = \frac{\mu_0}{1+\theta(V_{GS}-V_{TH})} \tag{6-3}$$

, where μ_0 is the low field mobility and θ is the mobility degradation coefficient due to high electric field. From the simulated results of an I-V model [104], we found that the most important parameters affecting *VIP*3 at fixed $V_{GS} - V_{TH}$ are subthreshold swing (S.S.) and θ, as shown in Fig. 6.7. With increasing S.S., *VIP*3 will increase in weak inversion region. With reducing θ, *VIP3* will increase at 0.05 V< $V_{GS} - V_{TH}$ <0.2 V, and decrease at $V_{GS} - V_{TH}$ >0.2 V. It should be noted that μ_0 has no effects on *VIP*3. This is because μ_0 contributes equally to g_m and g_{m3}, so its effects are cancelled out in g_m/g_{m3}. The observation in Fig. 6.7 can also be predicted by Volterra series calculation as reported in [104]. For the transistor in our work, after HC stress, S.S. increases from 82.6 to 92.6 mV/decade, and θ decreases from 1.54 to 0.68 V^{-1} (see the inset of Fig. 6.5), so *VIP*3 increases in the low bias region, as shown in Fig. 6.5.

6.3.3 Effects of oxide breakdown on RF Power Performance

The critical gate-oxide breakdown is an important reliability issue for the design of power amplifiers, especially for the large-signal applications. Fig. 6.8 shows the linear power gain measured with the gate voltages before and after OBD. It shows a slight deviation in higher gate bias regions. The degradation of linear power gain is also corresponded to the g_m degradation (see Fig. 5.1). It also suggested that the device biasing at higher gate voltage is more robust to OBD. However, it is not usually the bias point for an analog/RF designer, who usually biases the active device before or under the g_{mmax} for high gain and high speed applications.

The degradations of output power, power gain and power-added efficiency (PAE) are shown in Fig. 6.9. The PAE can be expressed by:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}}(1 - \frac{1}{G}) \quad (6\text{-}4)$$

At low input power, the PAE is less changed under stress due to the output power and drain current, and thus the power dissipation reduce simultaneously. When input power is larger than 1-dB compression point (P_{1db}), the degradations of PAE become serious. Because a part of the AC-signals on the DC drain current will be cut off as the input power becomes large enough. For this reason, the average drain current will increase with the increasing input power. Since the bias current of the device after oxide breakdown and HC stress is lower than that of the fresh one, the negative duty cycle of output waveform would enter the cut off region earlier. As a result, the power dissipation of stressed device is higher than that of the fresh one, leading to a lower PAE. Owing to the DC degradation is more serious after HC stress, the degradations of PAE under HCS is more serious in our case.

Since the dc behaviors are changed, the linearity would be affected by the oxide breakdown. In Fig. 6.10, we found that RF linearity (*IIP3* and *OIP3*) suffers less degradation. This is because not only the g_m shows degradation after oxide breakdown, the g_{m3} also decreases simultaneously after OBD (see Fig. 6.11). Then the ratio of g_m/g_{m3} was not changed dramatically under OBD. Compare with Fig. 6.10, in which the power terms of *IIP3* and *OIP3* present less affected by OBD with the increasing output currents; the voltage term of *VIP3* in Fig. 6.12 also proves the same phenomenon with the fixed V_{GS}-V_{TH}. That is to say, RF linearity is less affected by OBD if biasing the MOS transistors at constant currents even under the subthreshold regions or saturation regions.

6.4 Summary

In this paper, we have examined the effects of HC stress and OBD on RF power and linearity of MOS transistors. HC effects reduce the transconductance, output drain current and enlarge the threshold voltage of the NMOSFET. Consequently, the RF output power will degrade after HC stress. However, we found that the RF power performance is more robust to HC effects by biasing the gate voltage to higher values. Thus, it results in a trade-off between the vulnerability to HC stress and the static dc power consumption. Moreover, we compare the HC effect on RF linearity with various bias conditions. At fixed gate bias, the linearity is degraded after HC stress due to the shift of threshold voltage, however, it only change slightly at fixed $V_{GS} - V_{TH}$. That is to say, RF linearity is less affected by HC stress if biasing the MOS transistor at constant drain currents. When the transistor operates at a fixed $V_{GS} - V_{TH}$, only the subthreshold swing and mobility degradation coefficient will impact the linearity. Therefore the linearity for circuit design is robust to the HC effects by biasing the MOS transistors under constant drain currents. In addition, the RF power performance under OBD also presented degradations due to the decreased g_m and increased g_{ds}. But, it showed less affected on RF linearity after OBD, due to the simultaneously decreased g_m and g_{m3}. Moreover; in subthreshold regions, after OBD the linearity performs differently with that under HC stressing, since the subthreshold swing of a MOS transistor is not affected after OBD.

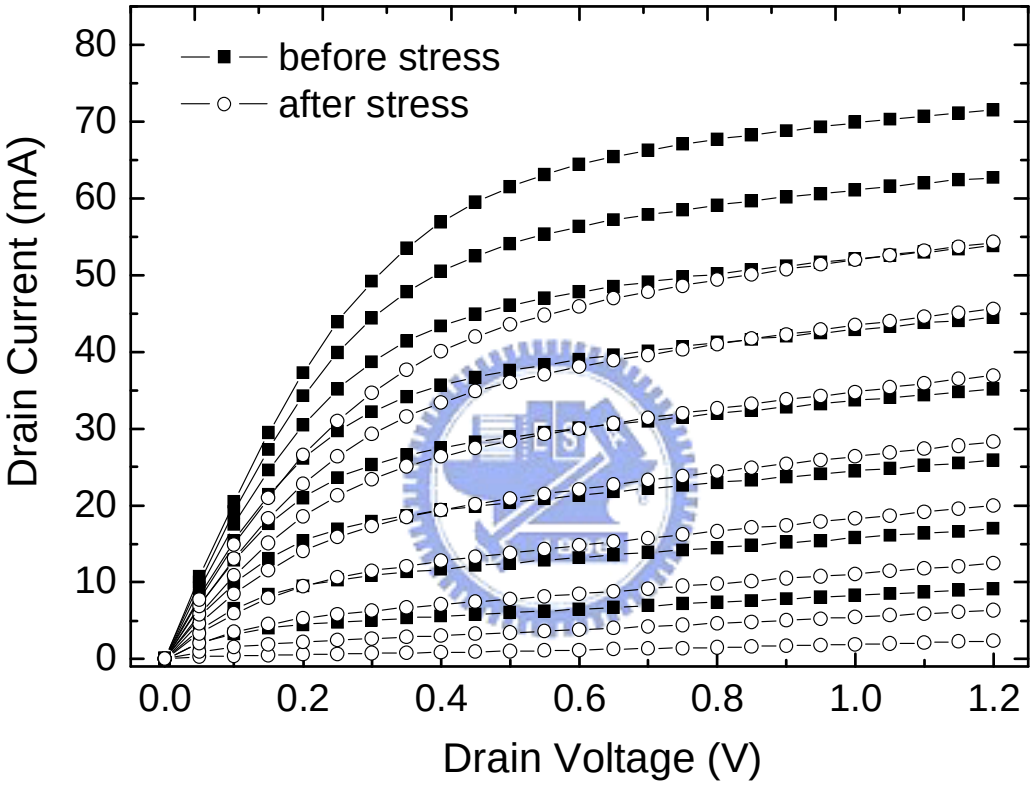


Fig. 6.1. Output characteristics of a MOSFET before and after HC stress. Output conductance (g_{ds}) is determined from the slop of I_{DS}-V_{DS} characteristics.

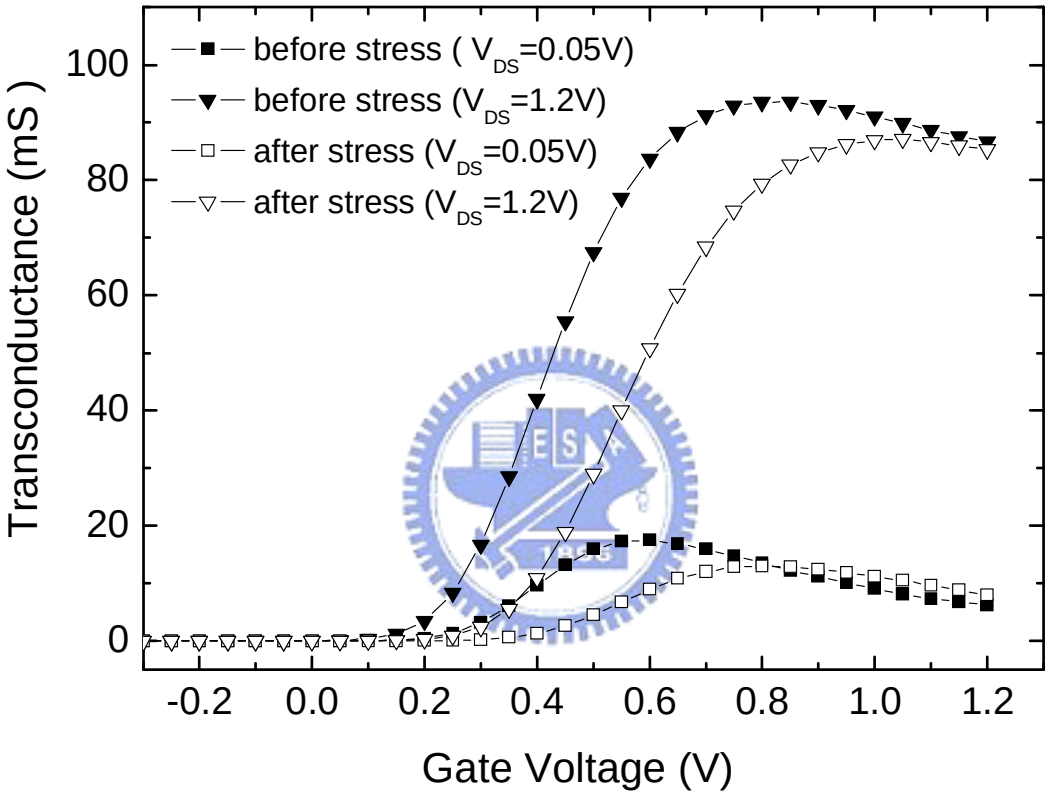


Fig.. 6.2. Transconductance (g_m) versus gate biases for a MOSFET before and after HC stress.

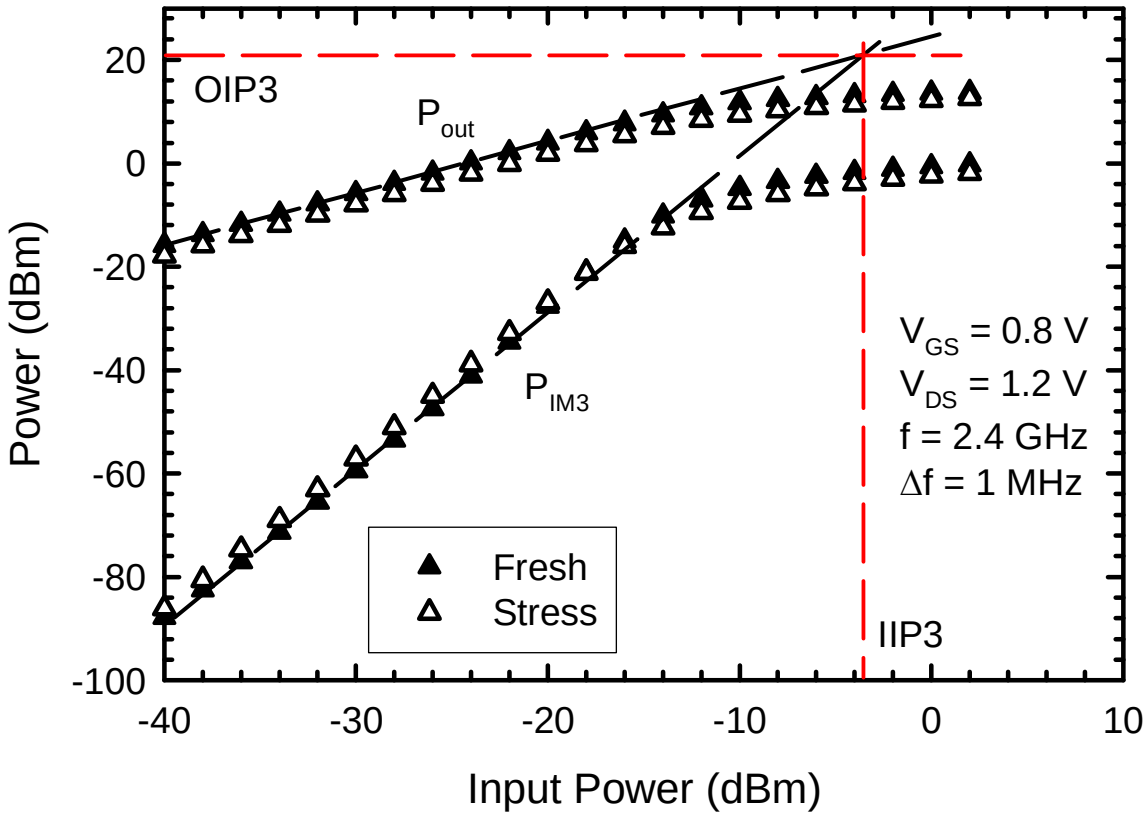


Fig. 6.3. Output power and third-order intermodulation power versus input power for a MOSFET before and after stress measured at a fixed V_{GS} = 0.8 V.

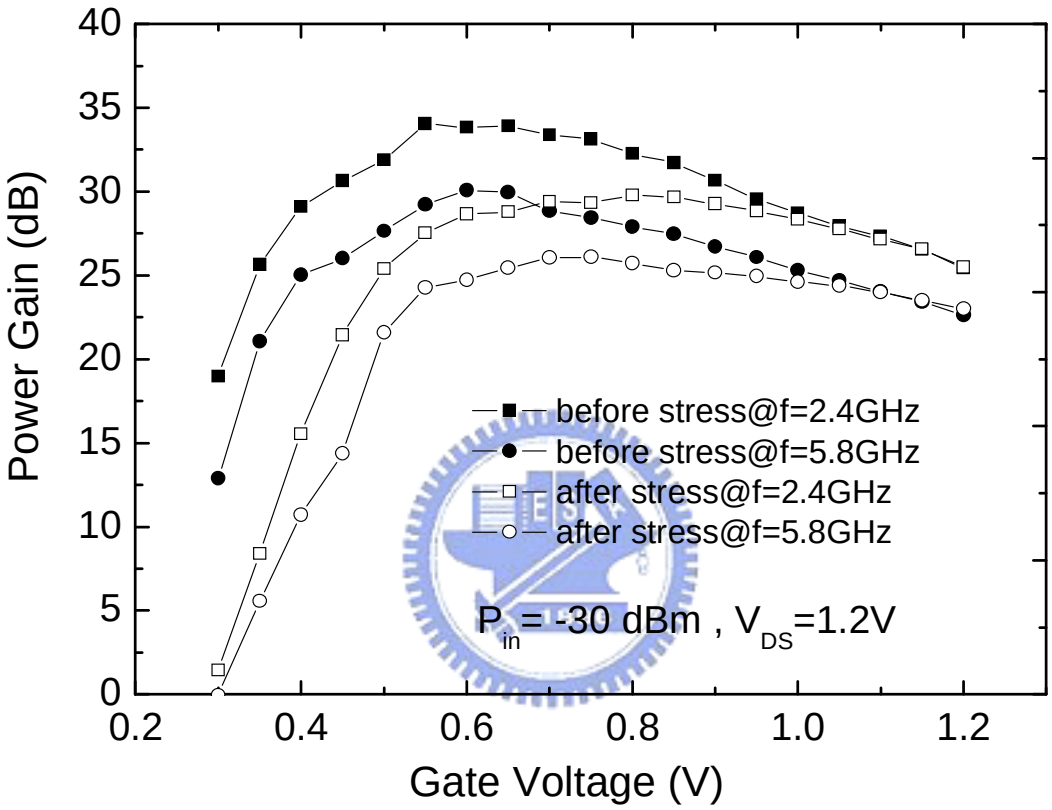


Fig. 6.4. Power gain versus gate bias voltage for a MOSFET before and after stress measured at a fixed V_{DS} = 1.2V.

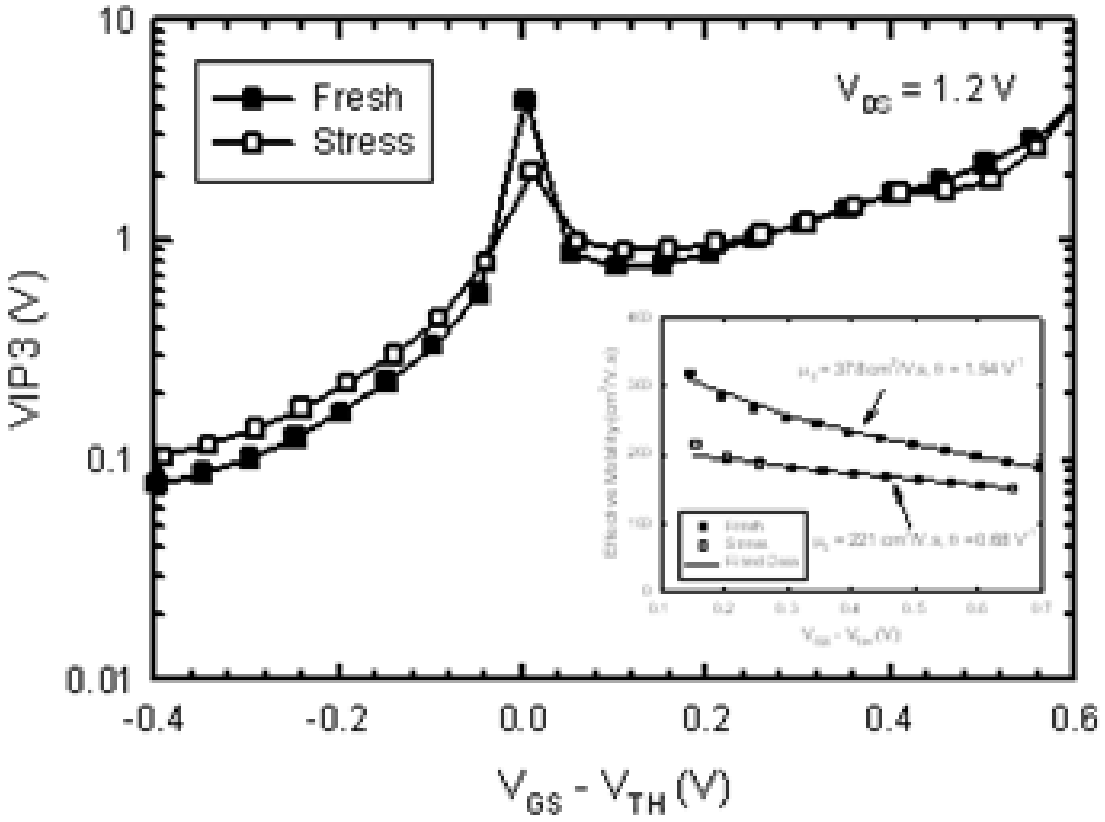


Fig. 6.5. *VIP3* versus $V_{GS} - V_{TH}$ for a MOSFET before and after stress. Inset is the effective channel mobility before and after stress.

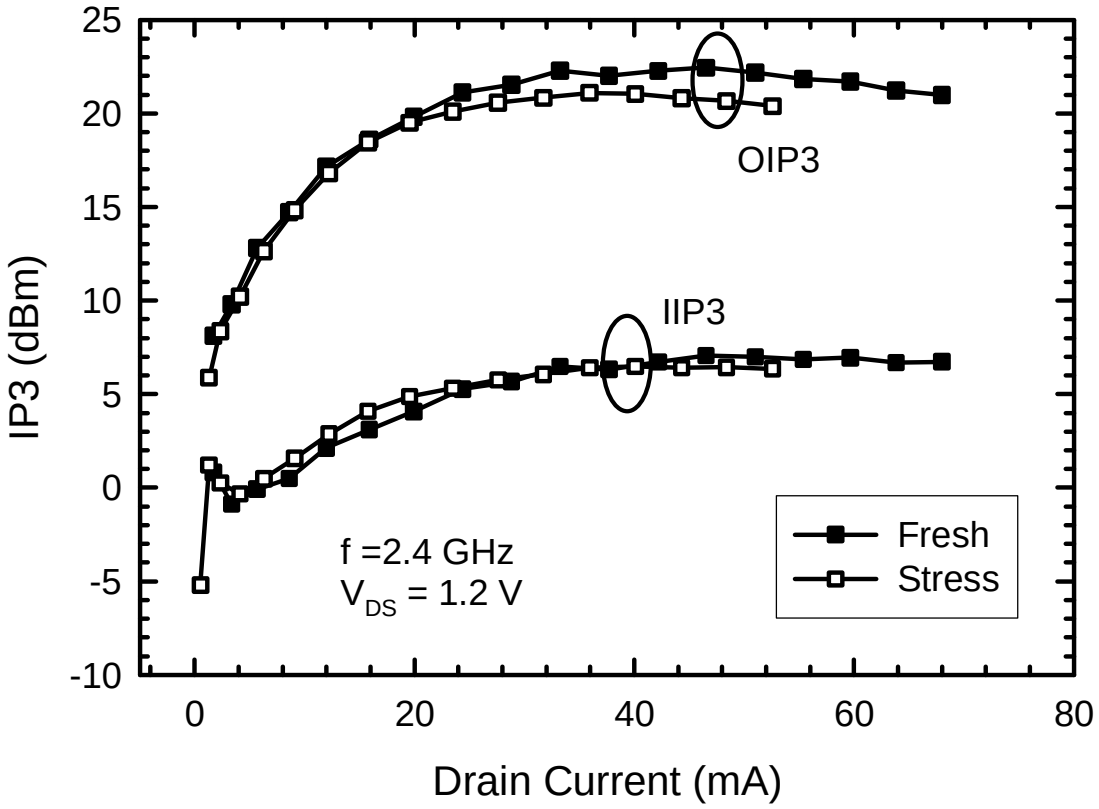


Fig. 6.6. Measured *OIP3* and *IIP3* versus drain current for a MOSFET before and after HC stress.

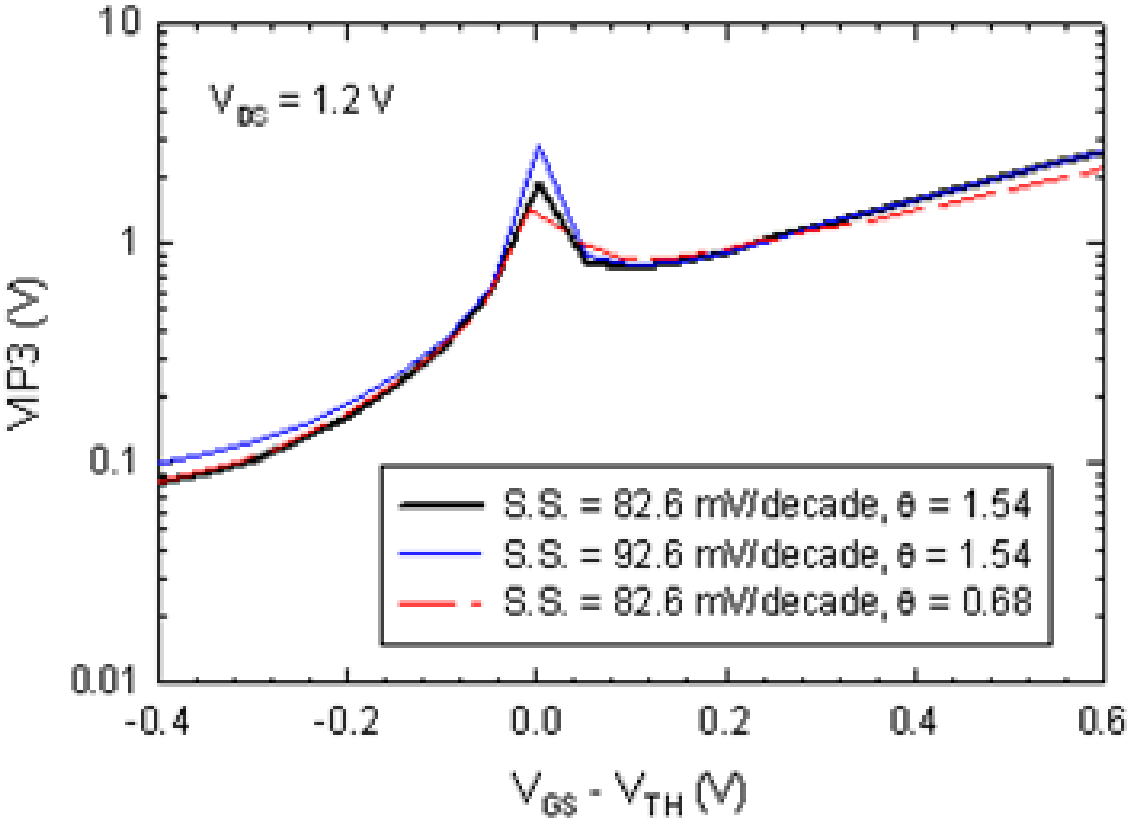


Fig. 6.7. Simulation results of *VIP3* with different subthreshold swings and mobility degradation coefficients.

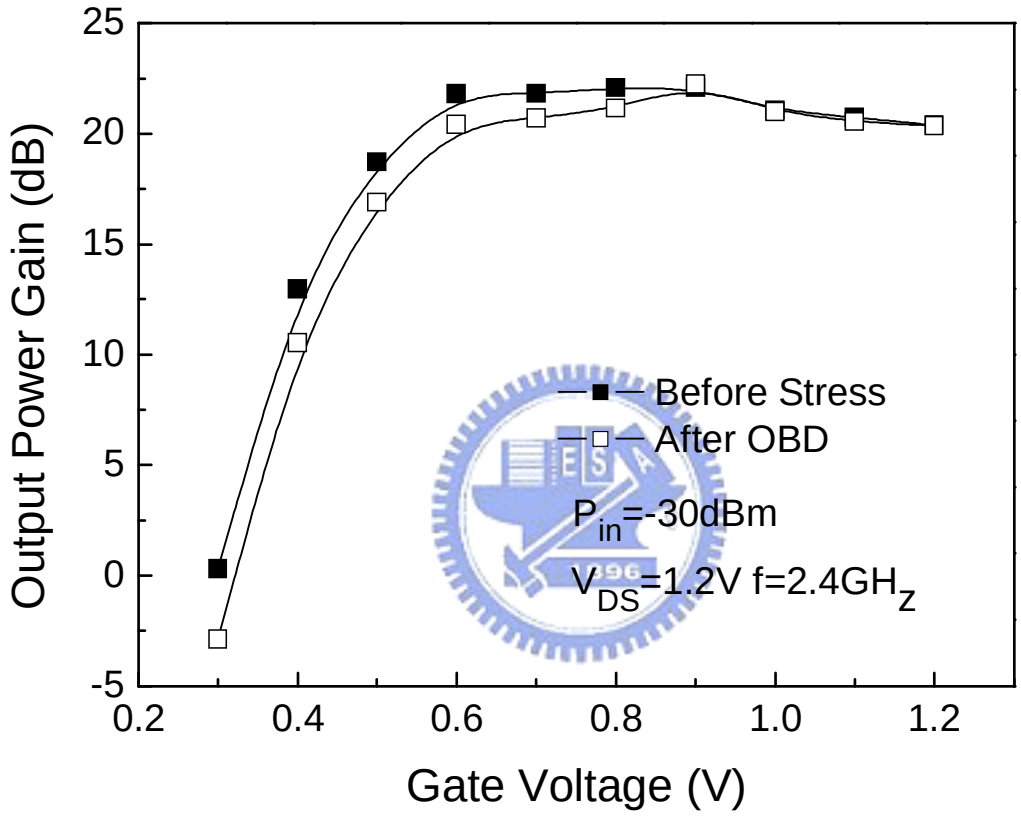


Fig. 6.8 Power gain versus gate bias voltages for a MOSFET before and after oxide breakdown at a fixed V_{DS} = 1.2V.

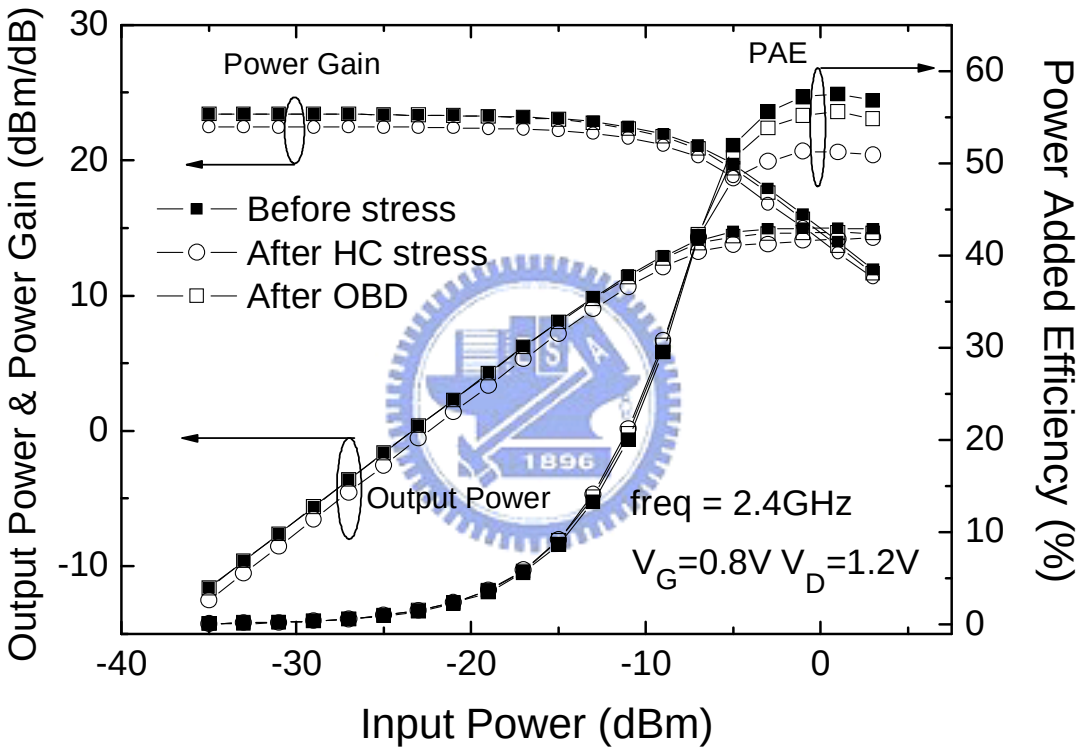


Fig. 6.9 Output power, power gain and PAE versus input power before and after oxide breakdown and HC stress.

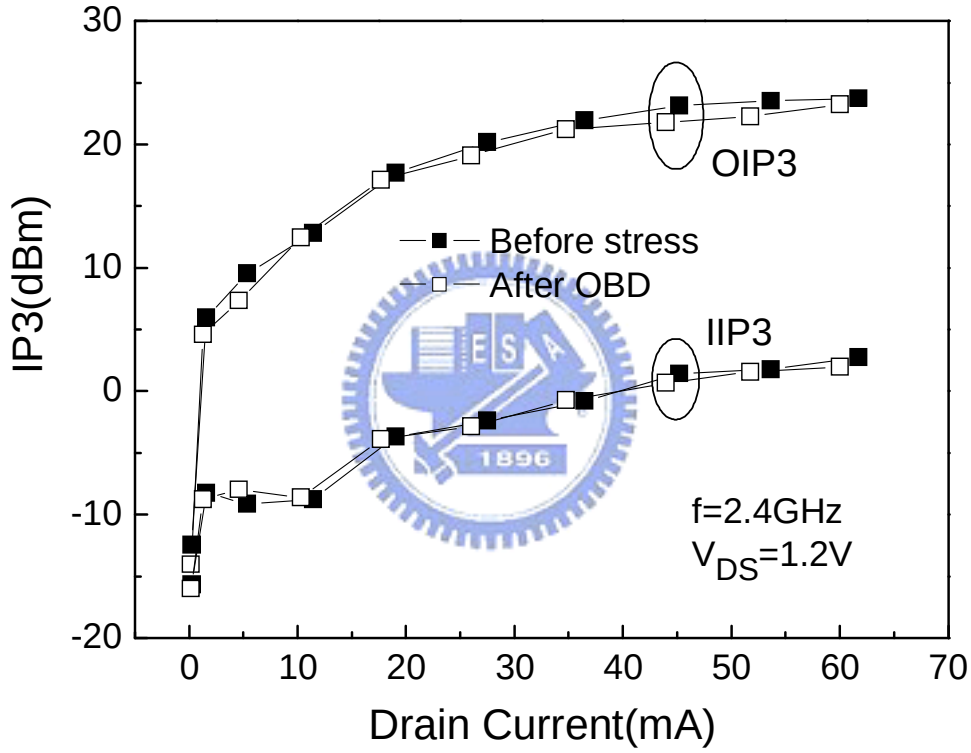


Fig. 6.10 Measured *OIP3* and *IIP3* versus drain current for a MOSFET before and after oxide breakdown

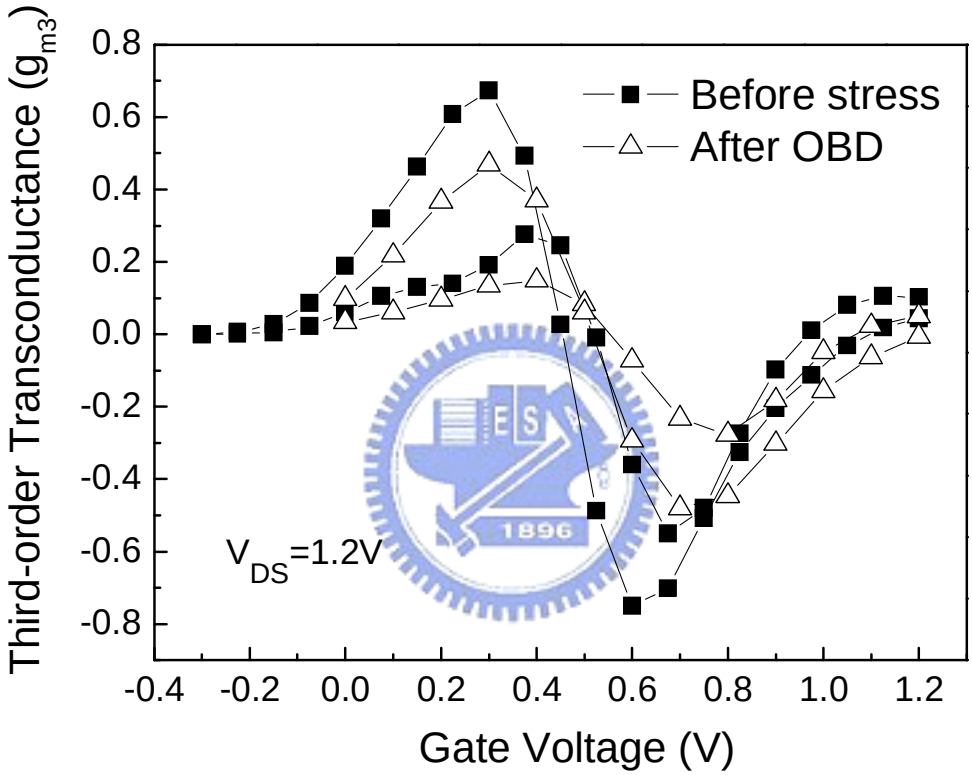


Fig. 6.11 Measured g_{m3} versus gate-biases for a MOSFET before and after oxide breakdown

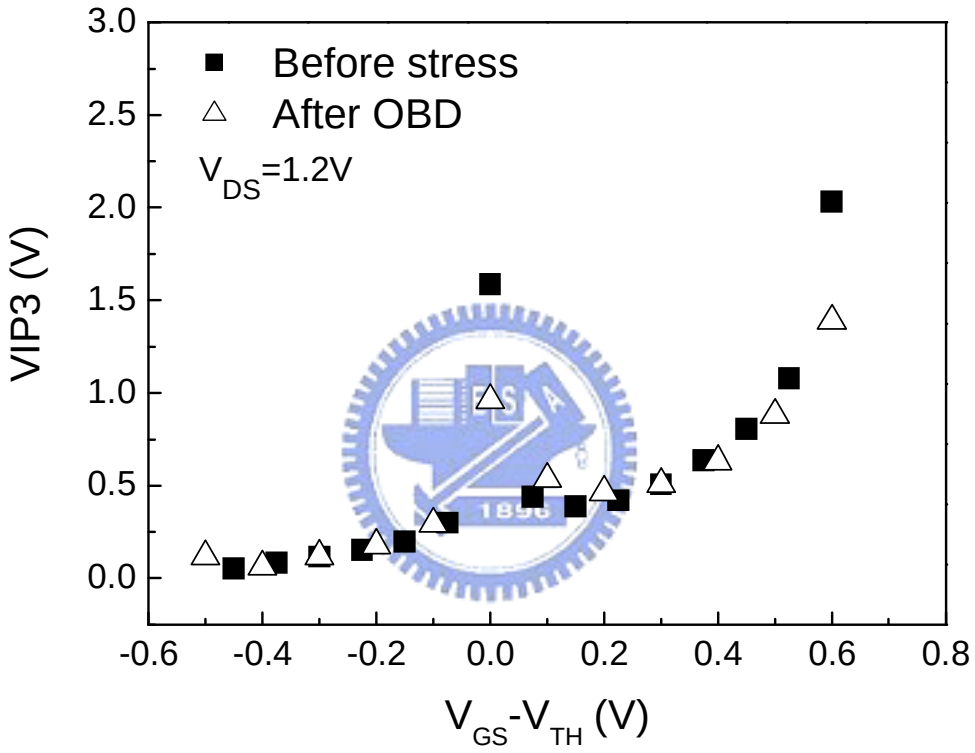


Fig. 6.12 Measured *VIP3* versus (V_{GS}-V_{TH}) for a MOSFET before and after oxide breakdown

Chapter 7
Conclusion and Suggestion for Future Work

7.1 Conclusion

Silicon-based devices have had acceptable device characteristics for high-frequency transceiver design for frequencies from 1 to 10 GHz since the early 1990s. The combination of low cost and superior integrated functions will make silicon CMOS and BiCMOS technologies of choice for RF circuits, if RF and system design goals can be realized. Until recently, research MOS transistors have lagged research SiGe HBTs in performance, but now they have over taken research SiGe HBTs with a transit cutoff frequency (f_T) at unit gain above 400 GHz [108]. However, this record of f_T in MOS transistors requires a feature size (gate length L) of 10 nm. Comparable results in a SiGe HBT can be accomplished at a feature size of approximately 100 nm, which can be manufactured today. While the III-V HEMT [109], [110], has a higher f_T, both MOS transistors and SiGe HBTs are easily integrated with VLSI digital functions. Of course, cost has been and will continue to be the motivating factor in utilizing CMOS technology for RF. At the lowest performance, MOS transistors are less expensive in production. SiGe BiCMOS is able to achieve comparable performance at twice the minimum geometry of CMOS.

With silicon-based transistors of CMOS and BiCMOS technologies capable of meeting technical requirements, time to market and overall system cost and performance will govern technology selection for RF market. In addition, the reliability issues are getting more and more important, especially in the varied operations of RF systems, in which the spec. demands the noise, linearity, power gain

and so on… Those specs are sensitive, and easily to be altered when the characteristics of device are changed by some electrical issues. With the advanced scaling technologies, the introduction of SiGe HBTs has opened new perspectives with respect to high-speed applications. In addition, MOS transistors are capable and suitable for future high-frequency system applications. However, owing to the high electric field at the base-emitter junction caused by the high doping levels of SiGe HBTs, the hot-carrier (HC) reliability has become a major concern for SiGe HBTs used in commercial products. Moreover, device scaling in combination with higher electrical field and current densities has consequences for the reliability issues under real product operations. As a result, the reliability issues of silicon-based transistors must be considered when they are operated in high-frequency and high-speed analog applications as well as in DC/logic operations. In this thesis, we discussed the reliability issues on the silicon-based transistors: SiGe HBTs and MOS transistors; especially, on their high-frequency characteristics, RF noise performance, linearity and RF power applications. For brevity, we separated this thesis into two main topics of SiGe HBTs and MOS transistors.

In chapter 3, we have addressed the classical OC stress (reversed emitter-base junction, and open collector) effects on SiGe HBTs by using a small-signal model, and we systematically investigated hot-carrier effects on the degradations of high-frequency and RF power characteristics of SiGe HBTs with different bias conditions. In chapter 4, an approaching stress methodology to real product operation was discussed for their reliability issues on SiGe HBTs. It occurs when high collector current density (J_C) and high collector-base (CB) voltage are imposed simultaneously on the device. In addition, by applying a commercial VBIC large-signal model, the high-frequency behavior, RF power performance and linearity are also described completely in this chapter. By comparing the stress effects at various bias conditions,

we observe that the stress-induced degradation under constant base-current measurement is much larger than that under constant collector-current measurement, due to the reduction of collector current. It then suggests that SiGe HBTs can be operated more robust to electrical stress by biasing devices under a constant collector current.

As to the MOS transistors, in chapter 5, we examined the effects of hot carrier stress (HCS) and oxide breakdown (OBD) on the RF characteristics of MOS transistors. By using a constructed small-signal model, we can clarify the effects of hot carrier and oxide breakdown. In addition, a gate-to-source resistance and a gate-to-drain resistance were added to the constructed small-signal model to illustrate the effects of gate leakage currents after oxide breakdown. Moreover, in chapter 6, we described the RF power characteristics for MOS transistors under HCS and OBD. The RF power, power gain, power added efficiency and linearity were addressed in detail before and after HCS and OBD. From the experimental observations, HCS and OBD induced degradations on high-frequency and RF performance should be taken into consideration in the design of RF CMOS integrated circuits.

7.2 Suggestion for Future Work

Since the silicon-based transistors are getting mature in commercial foundry work. The high-frequency and high-speed RF/analog circuits are embedded with baseband/logic circuits in SOC. The reliability issues of high frequency applications are relatively less addressed in real products applications. Moreover, there is not any high-frequency model associated with reliability issues till now. So, we suggest somebody who is interested in RF reliability topics to investigate the sensitive electrical parameters associated with reliability issues, and furthermore, to build the RF model either in small-signal or in large signal applications. The procedure can be

suggested to be followed by (1) Analysis of DC degradation, physical and electrical field model in VBIC/BSIM; (2) Construct an external RF parasitic model co-related to this DC model. (3) Aging model parameters should be involved in the RF-DC model. (4) Circuits simulation and applications.

In addition, silicon-base technology is well-known for their lack in RF power performance, especially in CMOS structures. In this moment, we also suggest somebody to do some research on the topic of RF high-voltage power transistors to reach to the goal of embedding RF power amplifiers in SOC. Even you can use the process design, layout design like in Fig. 7.1, which we have proposed in 2007 IMS. The HV-MOS transistors can be designed by altering the doping profile and structures of the output drain terminals. By different RF power applications, you can also use the circuit design to get higher power efficiency. By the way, of course, the cost efficiently design for RF power transistors is more popular for mankind's anxiety.

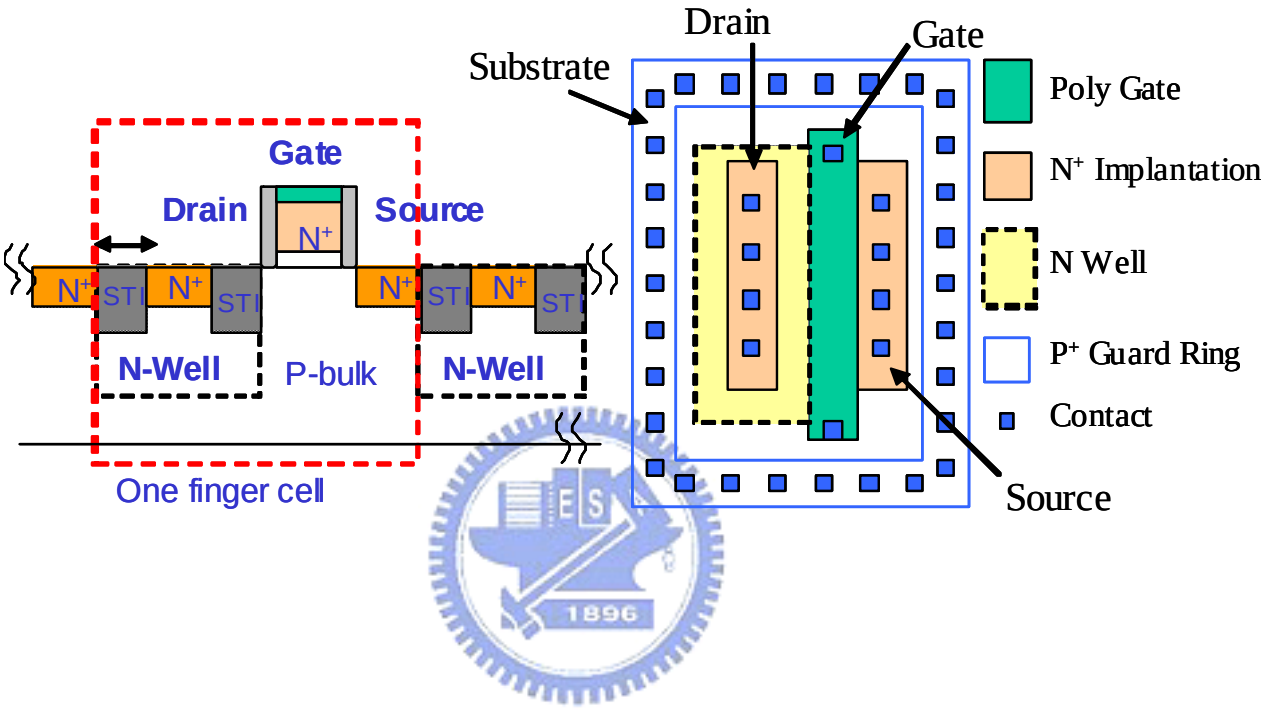


Fig. 7.1. Cross-section and layout design of one finger cell of “series-parallel” RF power MOS structure.

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