國立交通大學

電子工程學系電子研究所

博士論文

多相位時序歪斜校正技術及其於時序交錯類比
數位轉換器之應用

Multi-Phase Timing Skew Calibration and Its Application to Time-Interleaved ADCs

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研究生 ： 王仲益　　Student ： Chung-Yi Wang

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博士論文

A Dissertation
Submitted to Department of Electronics Engineering
and Institute of Electronics
College of Electrical and Computer Engineering
National Chiao-Tung University
in partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electronics Engineering
December 2010
Hsin-Chu, Taiwan, Republic of China

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摘要

　　高速電路廣泛應用於各種電子產品中，隨著 MOS 電晶體的通道長度越來越短，電晶體的寄生效應也因此隨之變小，這樣可以大大提升其操作速度以及節省功率消耗。然而也是因為通道長度的縮短，使得各種電晶體的非理想性使得類比電路設計的難度越來越高，讓類比電路的效能面臨嚴峻的考驗。

　　本篇論文描述一個多相位時序校正技術，並將其應用在時序交錯式類比數位轉換器上。針對我們所提出的校正技巧，推導出其數學模型，藉以分析應用該系統所需要的最佳參數。

　　我們實現了一個 65 奈米金氧半場效電晶體製程的 6-bit 、 16GS/s 435mW 之時序交錯類比數位轉換器，他利用我們所提出的校正技術，將時序歪斜校正至最低，在輸入訊號頻率為 3GHz 左右、等校取樣頻率為 16GHz 時，可將原本 19dB 的 SNDR 改善至 28dB 。而由時序歪斜所造成的失真訊號則是由 28dB 改善至 49dB 。
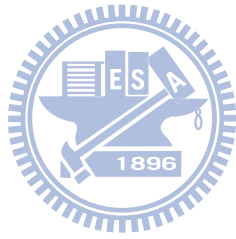
Multi-Phase Timing Skew Calibration and Its Application to Time-Interleaved ADCs

Student : Chung-Yi Wang   Advisor : Jieh-Tsorng Wu

Department of Electronics Engineering

and Institute of Electronics
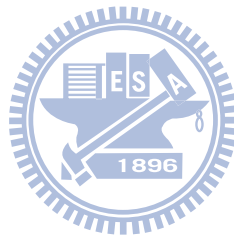
National Chiao-Tung University

Abstract

High speed data converter has been applied for many electrical. With the channel length of MOS transistor is smaller and the parasitic is also reduced. These characteristics make the transistor be able to be operated in higher frequency and lower power dissipation. However, non-ideal effects aslo occur in the short channel device and the analog design becomes more and more difficult.

A timing skew calibration technique for multi-phase system will be introduced in the thesis and we will apply it on the time-interleavd ADCs. In this thesis, the mathematical model for proposed calibration technique will be analyzed and simulated for optimization of design parameters of calibration scheme.

With optimized design parameters, a 6-bit, 16GHz time-interleaved ADC has been demostrated with 65nm CMOS technology. With proposed calibration scheme, the timing

skew error has been minimized. With input signal is about 3GHz, sampling rate 16GHz, the SNDR of output signal has been improved from 19dB to 28dB. The distortion harmonic tones due to timing skew has been improved from -28dB to -49dB.
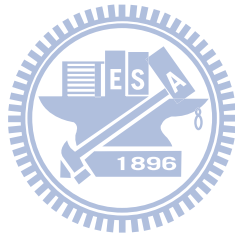
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Chapter 1

Introduction

1.1 Motivation

A multi-phase clock generator generates a set of clocks that have identical frequency but different phases [1][2]. Many applications, such as time-interleaved analog-to-digital converters (TI ADCs)[3][?], require the clock phases to be uniformly spread over one clock period. Figure 1.1 shows a M-channel sampling system including a multi-phase clock generator. The M-phase clocks are generated using a delay line consisting of M cascaded delay units with equal delay, U_j, where $1 \leq j \leq M$. The delay of U_j is usually controlled by a phase-locked loop or a delay-locked loop. For each j, the B_j buffer is connected to the output of U_j and generates the ϕ_j clock that drives the SAH$_j$ sample-and-hold circuit. For a TI ADC, the time interval between two consecutive samplings must remain constant. Any timing skew in the multi-phase sampling clocks can yield sampling interval variation [4][5] and degrade the overall signal-to-distortion-plus-noise ratio (SNDR) performance of the ADC. The timing skews are caused by the device mismatches in the delay units and the clock buffers, as well as the mismatches among clock signal routes. For an 8-channel 6-bit 16 GS/s TI ADC as Figure 2.6, the skew must be less than 0.31 psec so that the ADC can attain 37 dB SNDR. This skew requirement is difficult to achieve even for chips fabricated by today's advanced integrated-circuit technologies.

There are calibration techniques to correct the timing skews. A useful calibration scheme must be able to detect the timing skew first and then make the necessary correc-
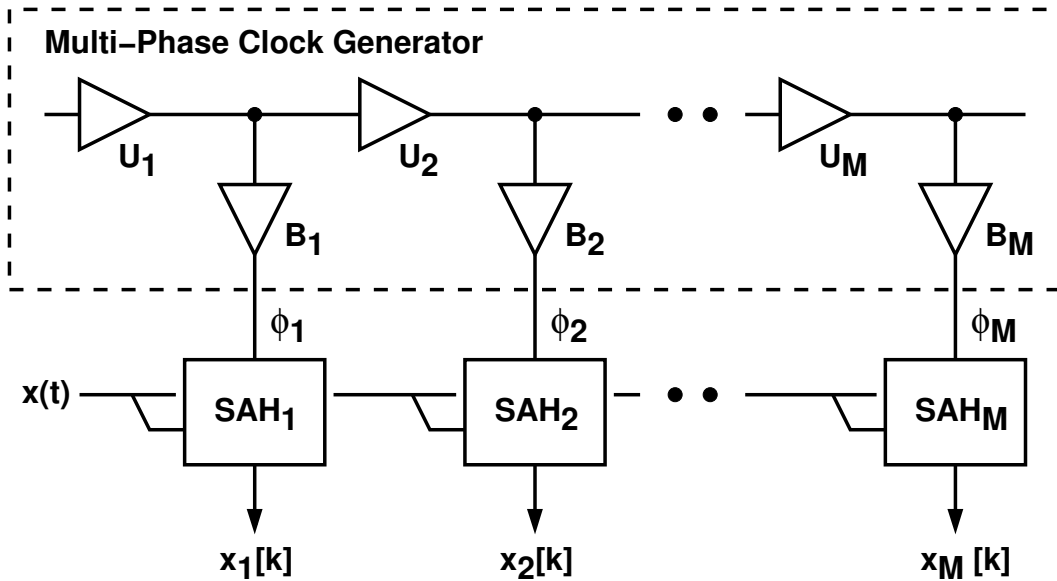
Figure 1.1: A multi-phase sampling system.
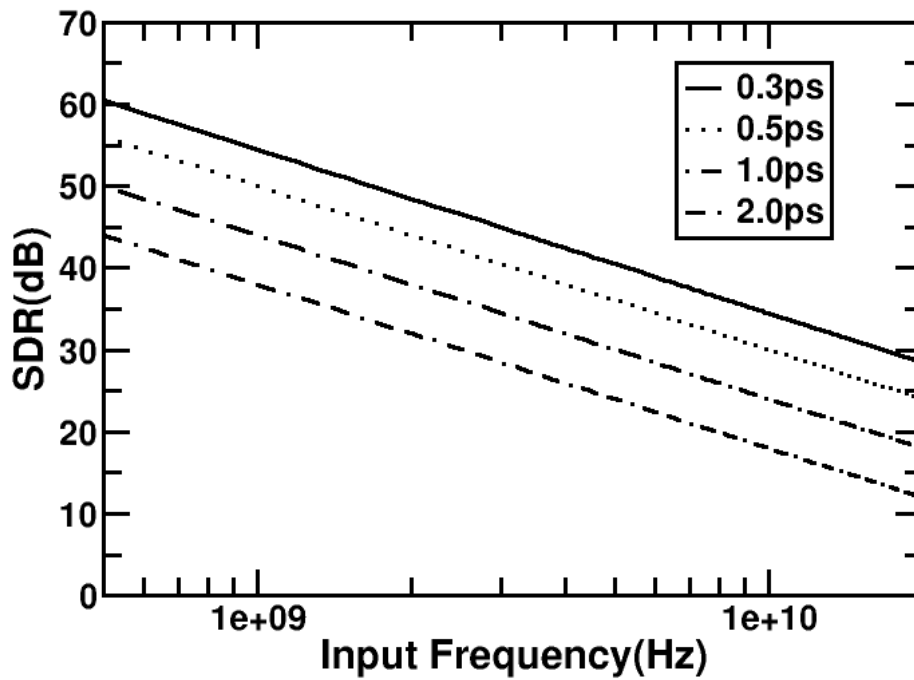
Figure 1.2: Signal-to-distortion ratio degradation due to timing skew.

tion. Most timing-skew detection techniques acquire the timing information from a reference signal. For TI ADCs, if the reference is narrow-band so that it does not cause aliasing in each analog-to-digital (A/D) channel, digital signal processing algorithms, such as Fourier transform [6] or cross correlation [7, 8], can be applied for skew detection. If the reference is well-defined and rich in timing information, such as a ramp signal, the skew can be detected without complex signal processing [9, 10]. However, a high-speed high-precision reference is difficult to generate. All the above skew detection techniques need to use the multi-bit A/D channels in the TI ADC to digitize the reference. Thus, it is not trivial to perform the calibration in the background without interrupting the normal A/D operation. To enable background calibration, the scheme of [9] adds a ramp reference to the ADC's input. This precise signal summation is difficult to implement and degrades signal dynamic range. On the other hand, the scheme of [10] requires an additional A/D channel and employs complex channel switching.

The timing skew can also be detected by counting the rising (or falling) edges of an asynchronous reference [11, 12, 13]. The scheme needs only simple hardware, such as flip-flops and adders. Its fundamental principle was expanded as zero-crossing detection [14]. Although stringent specifications for the references are not required, these techniques are sensitive to the input-referred offsets of the comparators used in the zero-crossing detectors. In some schemes, flip-flops serve as the comparators.

There are calibration schemes for TI ADCs that directly use the input of the ADC as the reference for timing-skew detection [7, 14]. Those schemes inherently operate in the background. The scheme of [7] restricts the input to be narrow-band so that it cannot cause aliasing in each A/D channel. This narrow-band restriction can be lifted by the clock-phase random-chopping technique [14]. However, the required clock choppers are difficult to implement. The mismatches among clock choppers can degrade the effectiveness of the technique. Furthermore, the effectiveness of these input-reference schemes depends on the richness of timing information residing in the inputs. For example, a dc input contains no timing information. No timing-skew calibration can function under such an input condition.

This thesis describes 6-bit, 16GHz time-interleaved ADC with a proposed timing-skew calibration technique whose clocking architecture is shown in Figure 1.3. For each
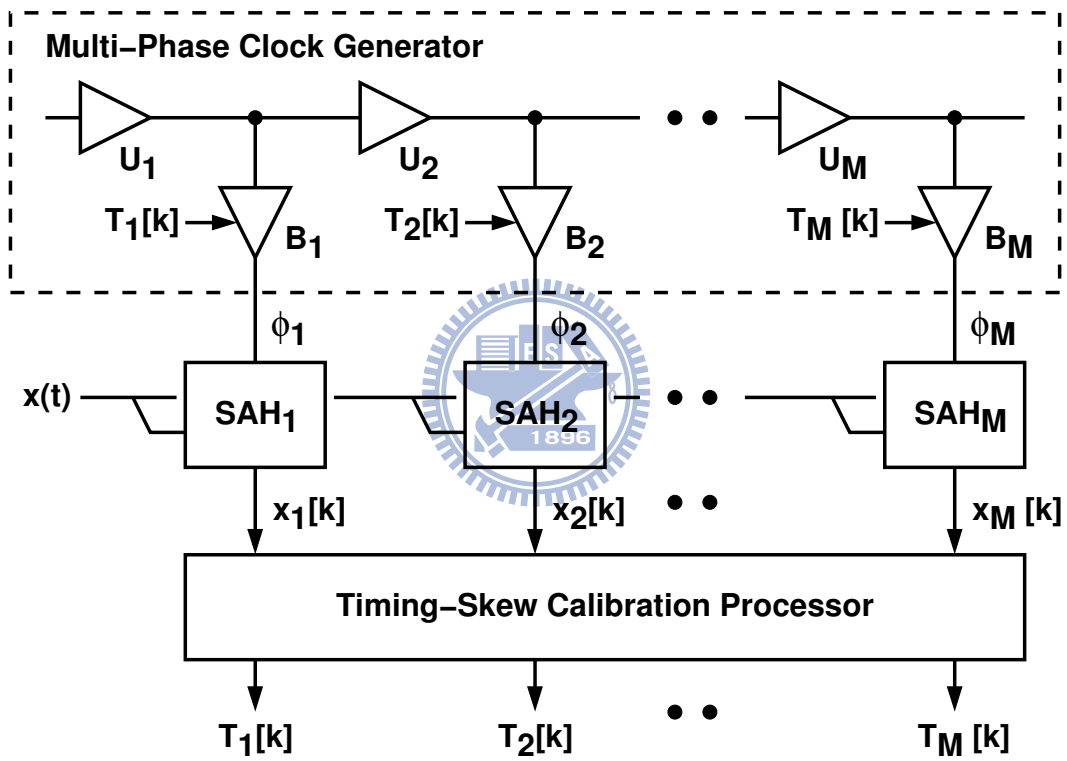
Figure 1.3: Proposed architecture for multi-phase timing-skew calibration.

j where $1 \leq j \leq M$, the SAH_j sample-and-hold circuit is driven by the ϕ_j clock from a multi-phase clock generator. The SAH_j receives the $x(t)$ reference signal and produces the $x_j[k]$ sampling sequence. From the sampling sequences, $x_1[k] \cdots x_M[k]$, the timing-skew calibration processor detects the timing skews between neighboring sampling channels. The $T_j[k]$ digital control signal from the calibration processor adjusts the delay of the B_j clock buffer. The objective is to equalize all sampling intervals defined by the multi-phase clocks. The timing-skew detection is based on the principle of zero-crossing (ZC) detection [14]. The ZC detection does not demand stringent specification for the $x(t)$ reference. It requires only one comparator per sampling channel. A new ZC detection scheme is proposed to reduce its sensitivity to comparators' offsets. Excluding comparators, the entire calibration processor can be realized by standard digital circuits.

The time-interleaved ADC in thesis contains $M = 8$ multi-phase clocks. Each clock has a clock period of T_c and a clock frequency of $f_c = 1/T_c$. Thus, the ADC's effective sampling interval is $T_s = T_c/8$ and the effective sampling rate is $f_s = 8f_c$. The ADC has an input range between ± 1, therefore, its magnitude resolution is defined as $V_{\text{LSB}} = 2/2^6 = 2^{-5}$. In addition, this time-interleaved (TI) ADC requires a timing resolution on the order of $T_{\text{LSB}} = T_s/2^6$.

1.2 Organization

The organization of the thesis is described as follow:

Chapter 2 draws the overview of multi-phase system, which includes fundamental function of system, and how the timing skew affects the system. Chapter 3 describes the techniques of timing skew detection. Frist draws the prior arts, and then introduce the principle of ZC detection technique. It demonstrates the mathematical equation to show the relation between zero crossing event and timing skew error. It aslo shows the constraint on zero crossing detection.

Chapter 4 shows the ZC-based timing skew calibration on TIADC. With mathematical analysis, the calibration settling time, system error after calibration can be evaluated, thus the optimized system design parameters can be calculated.

To verify the timing skew calibration configuration described in Chapter 4, a 65nm

6-bit 16GS/s time-interleaved flash ADC was demonstrated in Chapter 5. A background comparator offset calibration technique [15] has been applied to achieve a high performance single channel flash ADC.

Finally, conclusions and recommendations for future works will be given in Chapter 6.

Chapter 2

Multi-Phase System

2.1 Multi-Phase System
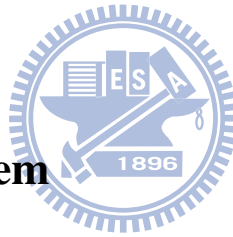
Shown in the Figure 2.1 is a multi-phsae sampling system. The signal $s(t)$ has been sampled by the multi-phases $\phi_1, \phi_2, \cdots, \phi_M$ and the respective sampled signals are $S_1[k]$, $S_2[k], \cdots, S_n[k]$, where k is the timing index in digital domain. The following MUX collects the signal $S_j[k]$, where $j = 1, 2, \cdots, M$ and generates the output signal $S[n]$, where n is the upsampling timing index in the digital domain and $n = M \times k + j$. With the uniform timing space between each adjacent phase ϕ_j and ϕ_{j+1}, the sampling rate can be improved by M times. However, mismatch occurs in the analog building block shown in Figure 2.2, which leads the non-uniform timing space, or timing skew error, then causes the sampling error as shown in Figure 2.3 and Figure 2.4. With the higher frequency signal, the sampling error is larger since the slope of signal is larger. The following section will describe the effect of timing skew error in detail.
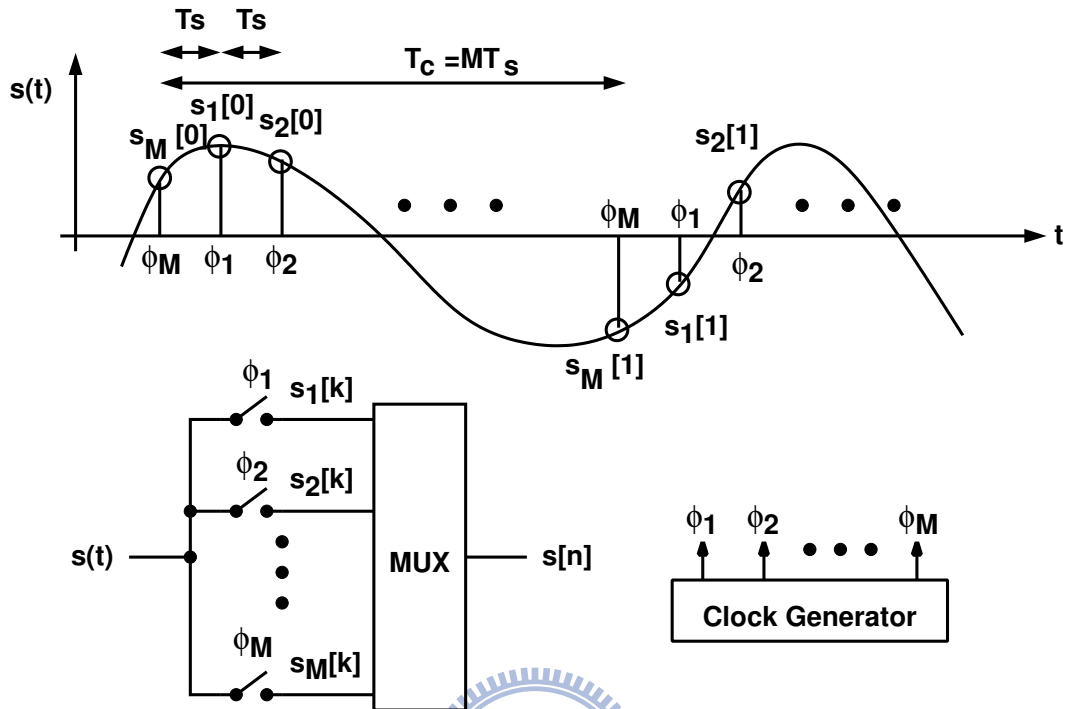
Figure 2.1: Multi-phase sampling system.
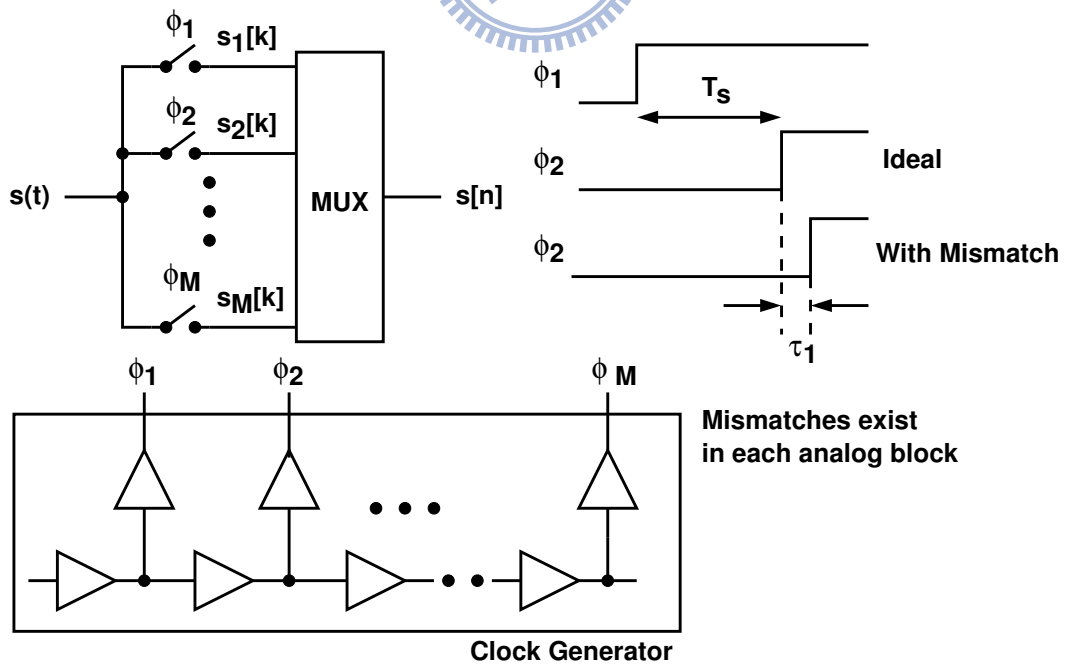
Figure 2.2: Timing skew periodically occurs when mismatches exist in the analog building block.
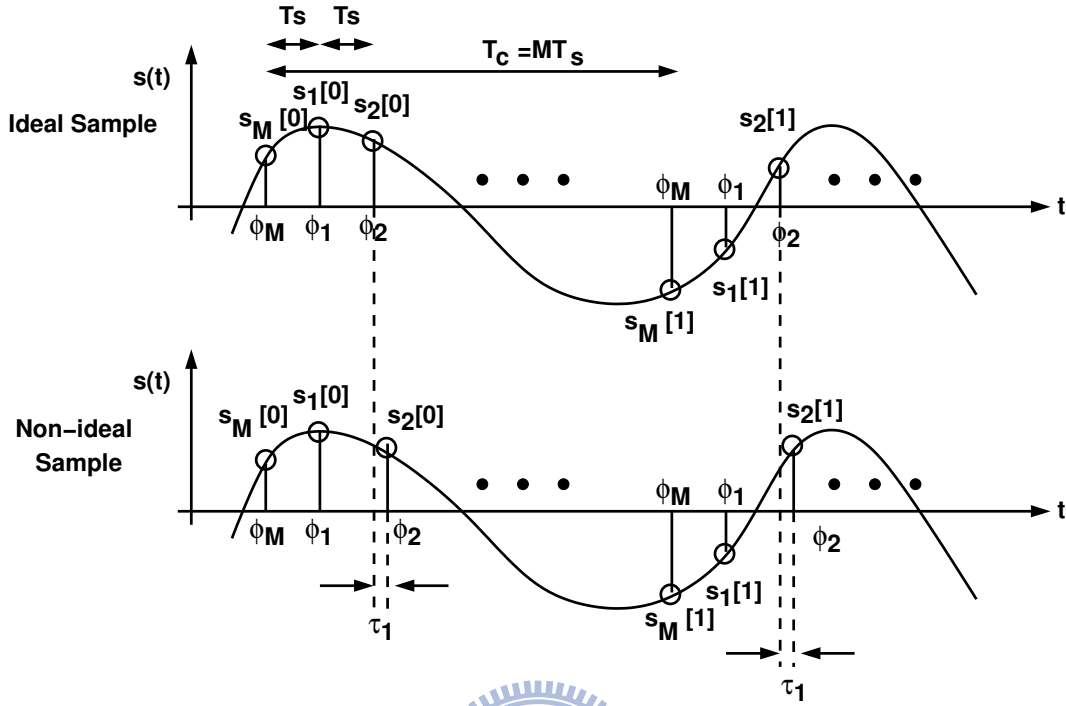
Figure 2.3: Timing skew in the multi-phase system.

2.2 Timing Skew on Multi-Phase (Time-Interleaved) System

Considering that f_c as single channel clock rate as described in the above section, the sampling time instant can be written as

$$t_m = mT_s + \tau_j \tag{2.1}$$

where $j = 1, 2, \cdots M$, and $T_s = 1/(Mf_c) = 1/f_s$, and $-T_s/2 < \tau_j < T_s/2$ shows the timing skew error among each channel. Assuming the analog input signal $s(t)$ to have the spectrum $S_a(\omega)$, the digital spectrum of the time-interleaved system can be expressed as (2.2)

$$S(\omega) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} \left(\frac{1}{M} \sum_{m=1}^{M} e^{-j\left(\omega - k\frac{2\pi}{MT_s}\right)\tau_m} e^{-jmk\frac{2\pi}{M}} \right) S_a \left(\omega - k\frac{2\pi}{MT_s} \right) \tag{2.2}$$

With no timing skew errors, $\tau_j = 0$ and (2.2) can be written as

$$S_{ideal}(\omega) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} S_a(\omega - 2\pi k) \tag{2.3}$$
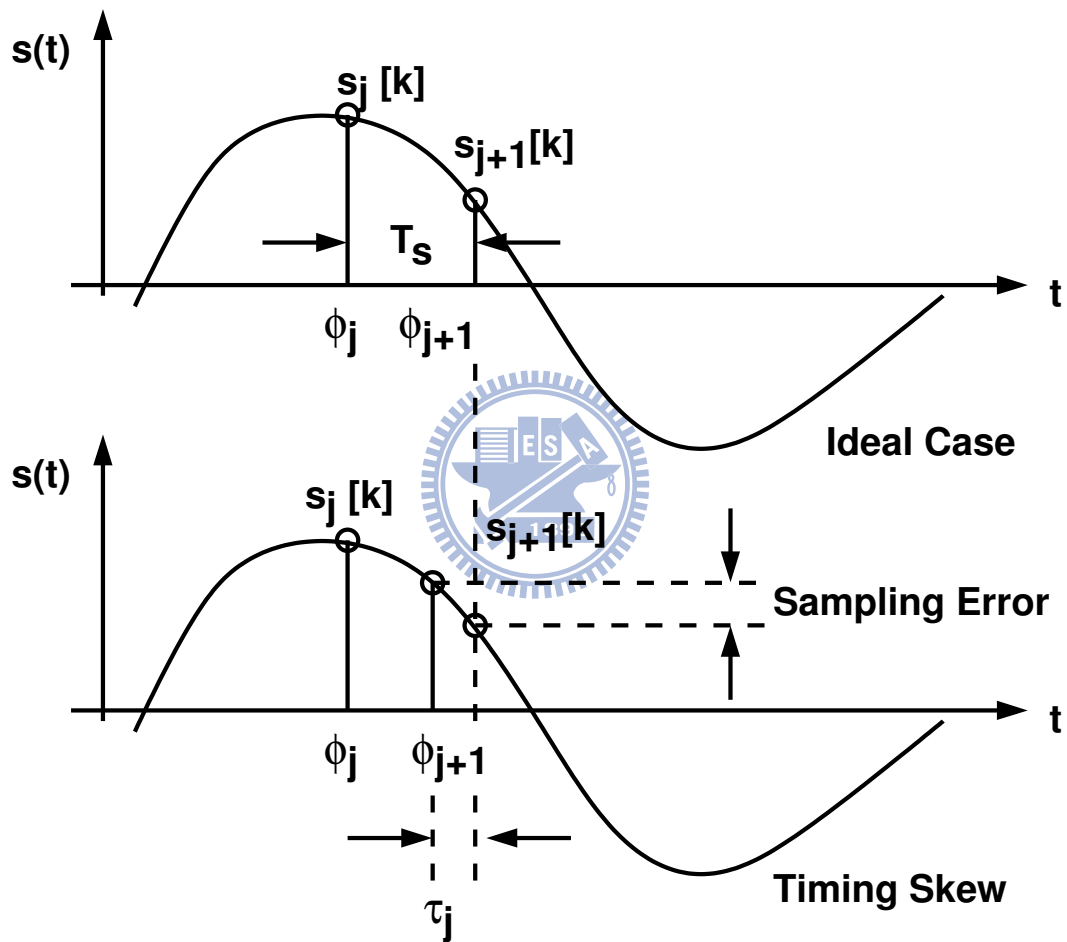
Figure 2.4: Timing skew causes the sampling error.

which corresponds to a siganl sampled at sampling rate T_s.

However, $\tau_m \neq 0, m = 1, 2, \cdot, M$, the timing skew error occurs. Considering a sinusoidal input signal with an amplitude of 1, angular frequency $\omega_0 = 2\pi f_0$, the digital spectrum of output is

$$S_{skew}(\omega) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} A(k) \cdot j\pi \left(\delta \left(\omega + \omega_0 - \frac{2\pi k}{MT_s} \right) - \delta \left(\omega - \omega_0 - \frac{2\pi k}{MT_s} \right) \right) \quad (2.4)$$

where

$$A(k) = \frac{1}{M} \sum_{m=1}^{M} \left(\frac{1}{M} e^{-j\omega_0 \tau_m} \right) \cdot e^{-j \frac{2\pi km}{M}} \quad (2.5)$$

The above equation shows that $A(k)$ includes the frequency components of $1/M, 2/M, \cdots .$, and the distortion tone for timing skew error will appears at signal frequency

$$f_0 + \frac{m}{MT_s}, f_0 - \frac{m}{MT_s}, m = 1, 2, \cdots, M - 1 \quad (2.6)$$

where the corresponding frequency shows the tune frequency of distortion. Morefurther, (2.4) also implies the timing skew error forms a sequence with repeating τ_j, and it has been modulated as phase modulation with carrier frequency f_0. If the timing skew errors are treated as Gaussian random variable with zero mean and a variance of σ_τ^2, the distortion power defines the timing skew requirement as following equation

$$P_{d,skew} = 2\pi^2 f_0^2 \sigma_\tau^2 < \frac{V_{LSB}^2}{12} \quad (2.7)$$

where the factor 12 is calculated by asuuming that signal around each ADC code is a uniform distribution over the range from $-0.5V_{LSB}$ to $+0.5V_{LSB}$. Thus we have defined the specification of timing skew errors.

Also we test the timing skew errors in time-interleaved ADC, where the resolution of ADC is 6-bit. The simulation result is shown in Figure 2.5, where the timing skew errors are zero mean and $0.05T_s$ standard deviation. The input signal is still a sine wave with frequency about 0.09 in digital domain. the distortion tone frequency occurs at $1/8 + 0.09, 2/8 + 0.09, \cdots$, which is the same as the result described in above mathematical equation. [?][16][17][18]

Shown in the Figure 2.6 draws how the timing skew affects the signal-to-distortion ratio when input frequency increases. For an 8-channel 6-bit 16 GS/s TI ADC, the skew
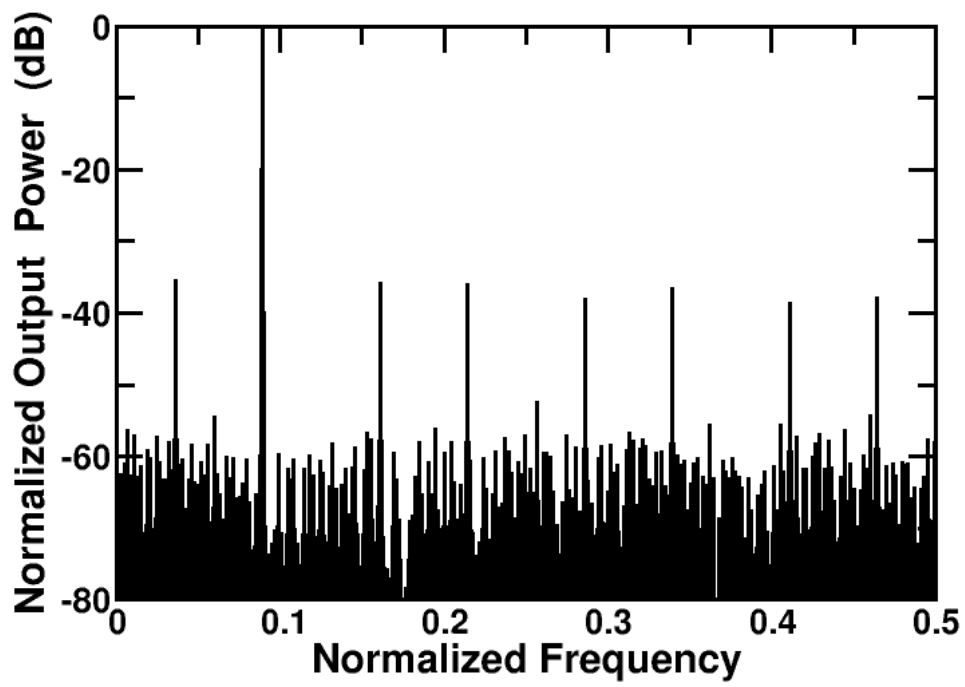
Figure 2.5: Time-interleaved output spectrum with timing skew errors.
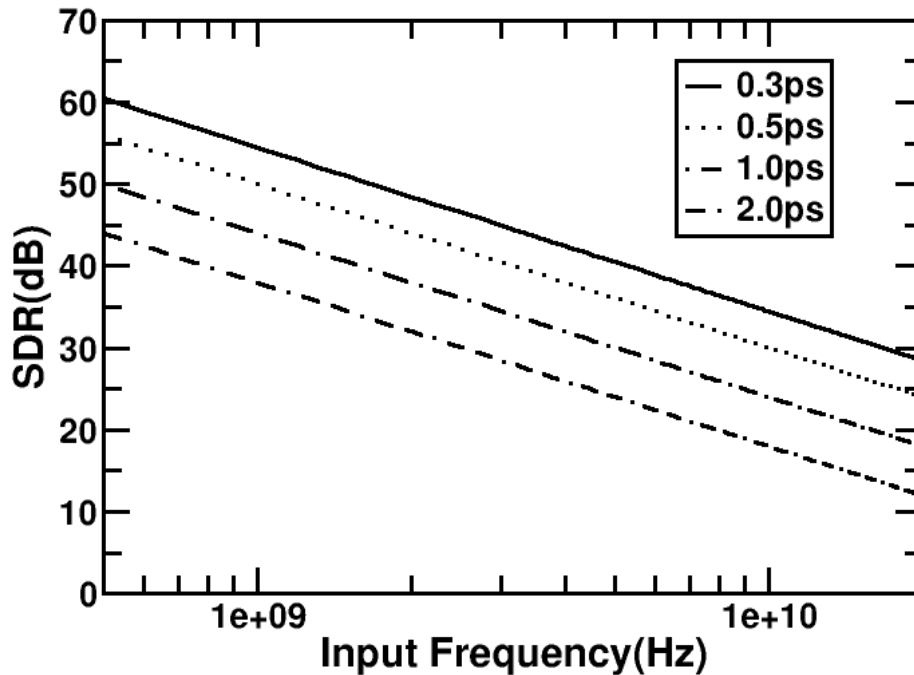
Figure 2.6: Signal-to-disortion ratio due to timing skew under different input frequency.

must be less than 0.31 psec so that the ADC can attain 37 dB SNDR. This skew requirement is difficult to achieve even for chips fabricated by today's advanced integrated-circuit technologies.

As the describe in the last chapter, since the timing skew error degrades the output signal performance acutely and it is hard to achieve the 0.3 psec timign skew specification in pure analog method, the timing skew detection and calibration is required. Figure 2.7 draws that the multi-phase system requires a timing skew detector to trim the timing delay, thus the performance of output signal can be improved.
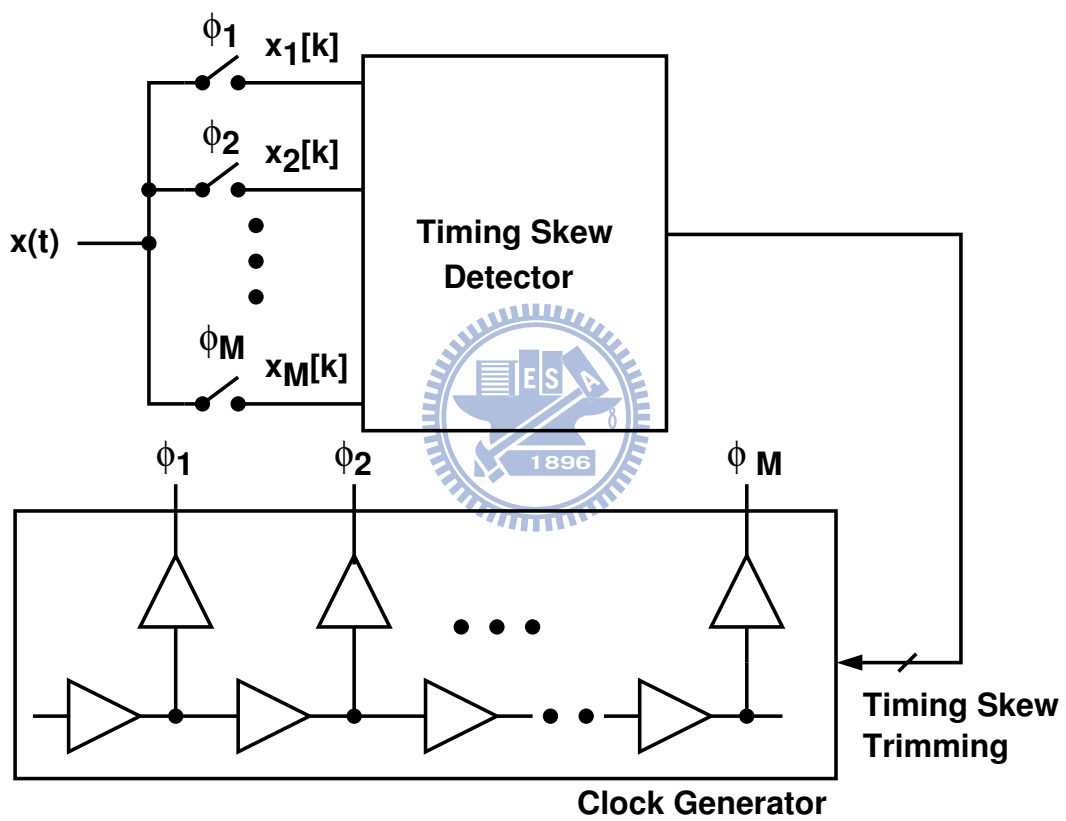
Figure 2.7: A timing skew detection is required in the multi-phase system.

Chapter 3

Timing Skew Detection

3.1 Prior Arts

In this section, the some timing skew detection techniques will be introduced. First is the FFT test, the second is the correlation based technique, following is the detection by reference signal and final is using edge detection technique to detect the timing skew.

3.1.1 FFT Testing

Shown in the Figure 3.1 is the FFT based timing skew detection technique. The reference signal $x(t)$ has been sampled by multiphase clocks, then obtains the sampled siganl $x_1[k]$, $x_2[k], \cdots$. With given sine wave signal of $x(t)$, using FFT of each subchannel signal $x_j[k]$, then the amplitude and phase of each $x(t)$ can be extracted. Therefore, by comparing the phase difference between each adjacent channels, the timign spacing can be measured and the timing skew has been detected. However, we should define the $x(t)$ as the narrow band
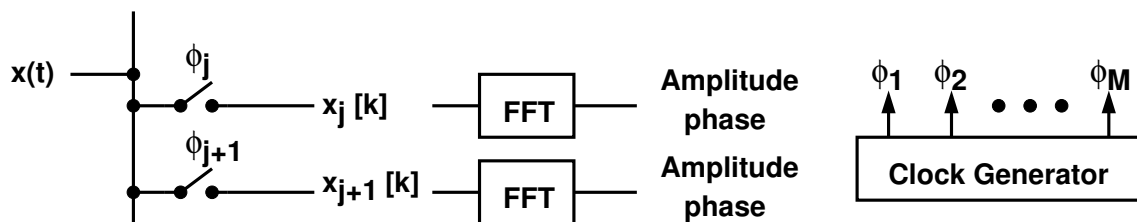
Figure 3.1: FFT testing in the multi-phase system.
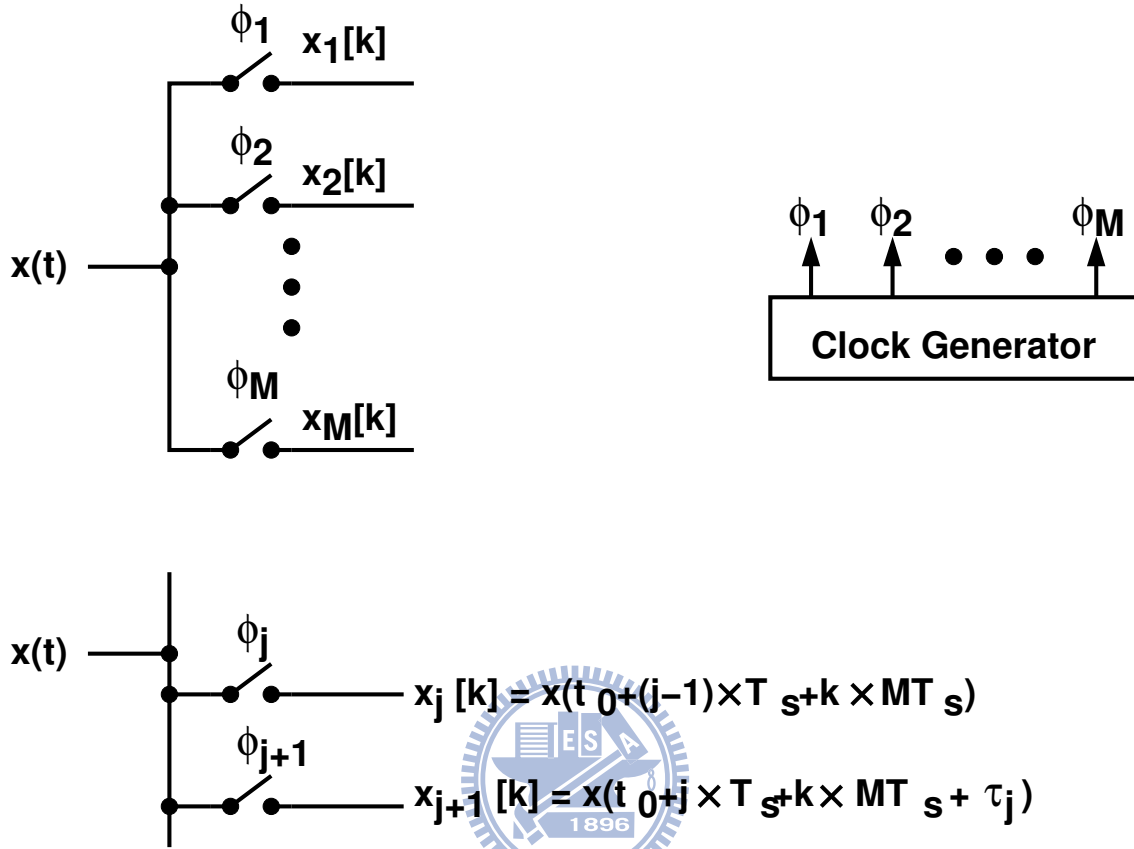
Figure 3.2: Sampling sequence in the multi-phase system.

signal such as sine wave. Besides, the multi-bits ADC and FFT module are required in this system.

3.1.2 Correlation Based Technique

Figure 3.2 shows the simple multi-phase system. The reference signal $x(t)$ has been sampled by ϕ_j, where $j = 1, 2, \cdots, M$. The following sampled signal is $x_j[k]$:

$$x_j[k] = x\left(t_0 + j \times T_s + k \times MT_s + \tau_j\right) \tag{3.1}$$

where t_0 is the initial time value, T_s is the ideal timing space between each adjacent channels. To simplify the mathematical derivation, considering that $x(t) = \cos(2\pi f_{in}t)$ only and then evaluating the expected value $E\left(x_j[k] \times x_{j+1}[k]\right)$ by the following equation:

$$E\left(x_j[k] \times x_{j+1}[k]\right)$$

$$= E\left(\cos\left(2\pi f_{in}T_s(Mn+j)\right) \times \cos\left(2\pi f_{in}T_s(Mn+j+1)\right)\right)$$

$$= E\left(\frac{\cos\left(2\pi f_{in}T_s(2Mn+2j+1)\right)}{2} + \frac{\cos\left(2\pi f_{in}T_s\right)}{2}\right) \quad (3.2)$$

$$= \frac{\cos\left(2\pi f_{in}T_s\right)}{2}$$

With timing skew error τ_j:

$$E\left(x_j[k] \times x_{j+1}[k]\right) = \frac{\cos\left(2\pi f_{in}(T_s+\tau_j)\right)}{2} \quad (3.3)$$

With above equation, the timing skew error can be detected by evaluating the mean of product $x_j[k] \times x_{j+1}[k]$ since the variable τ_j in the Equation (3.3) is a monotonic function [7].

However, the mean of product $x_j[k] \times x_{j+1}[k]$ may be not a monotonic function of τ_j when the bandwidth of $s(t)$ is too large. To understand this issue, considering Figure 3.3, the aliasing occurs when the bandwidth of $s(t)$ is larger than $f_c/2$. Since the data sequence the sampling clock of $S[Mn+j]$ is f_c, with bandwidth of $s(t)$ larger than $f_c/2$, aliasing occurs and the digital signal processing calculating will fail and the timing skew detection fail. We can define that the bandwidth of reference is small to overcome this problem. However, we still need a good enough ADCs to quantize ths reference signal and digital multiplier to evaluate the timing skew error.

3.1.3 Reference Signal Technique

Shown in the Figure 3.4 is an exmaple of timing skew detection using refernce signal[9]. The period of ramp signal $x(t)$ is T_c. Considering the input signal $s(t)$ is zero mean, the input signal $s(t) + x(t)$ of channel j has the mean value x_j. Since the reference signal is well known, when timing skew occurs, the average value of $s(t) + x(t)$ is different from ideal value, thus the timing skew can be detected by using the measured x_{j+1} substractes the adjacent channel's value x_j. Since with zero timing skew, the differences between each adjacent channels are the same. The difference between $x_{j+1} - x_j$ with different j implies the timing skew error.
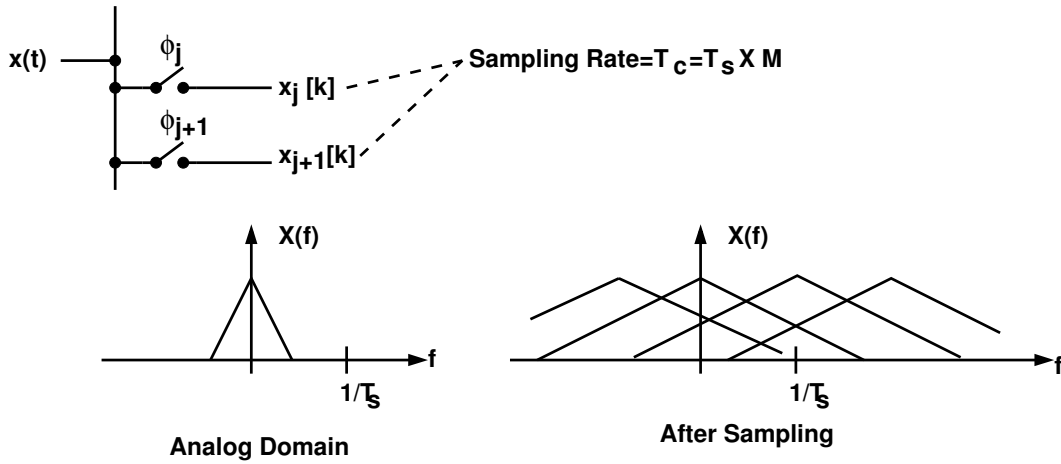
Figure 3.3: Aliasing of $s(t)$ with the downsampling clock f_c.
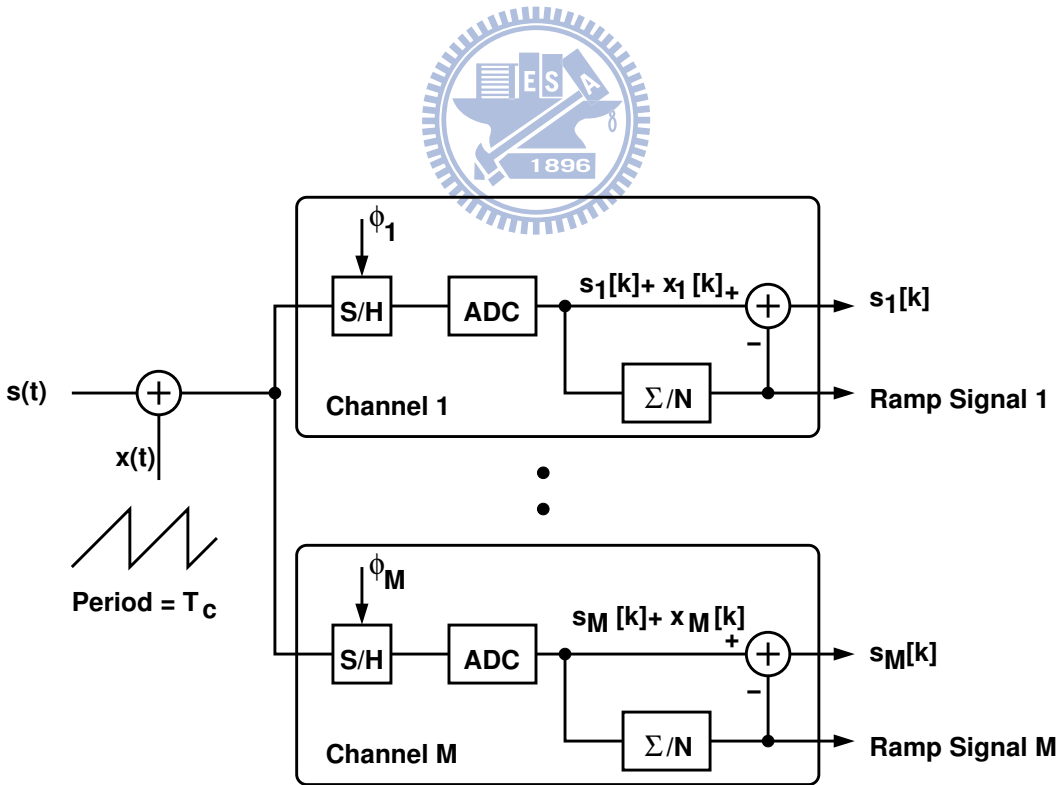
Figure 3.4: Using reference signal to find timing skew error.

However, the ramp signal is hard to generate perfectly, any non-ideal effect on ramp signal will cause the error of timing skew detection. Besides, the ramp siganl reduceds the dynamic range of $s(t)$ and the function of analog addition also produces the nor-ideal effect.

3.1.4 Edge Detection Technique

Figure 3.5 uses clock signal to detect the edge of reference signal. The reference signal $x(t)$ is a square wave and asynchronous to the clock signal ϕ_j. When the reference signal $x(t)$ has been sampled by the adjacent clocks ϕ_j and ϕ_{j+1}, the following NOR gate can detect if the rising edge of $x(t)$ occurs. When the NOR gate output signal bin=1, the implies edge of $x(t)$ occurs between the adjacent clocks ϕ_j and ϕ_{j+1}. Since the reference signal $x(t)$ is asynchronous to clock ϕ_j signal, the probability density of reference siganl $x(t)$ edge occurrence is a uniform distribution. Therefore, as shown in Figure 3.6, assuming that the period of $x(t)$ is larger than clock source, and the difference is ΔT the large timing space among tap $j+1$ and j leads large probability of $x(t)$ edge occurrence, and we can compare the accumulation of each edge occurrence among each channel to detect the timing skew error.

There are also many timing skew calibration method, such as [19] and [20] use analog phase detector to minimized the timing skew error and [21] use local phase detector in delay-locked loop to suppress the timing skew error.

3.2 Zero-Crossing (ZC)

Consider the M-channel sampling system shown in Figure 1.1. For each j where $1 \leq j \leq M$, the SAH$_j$ sampler triggered by the ϕ_j clock samples the $x(t)$ input and produces the $x_j[k]$ sampling sequence, where k is a discrete time index. Both $x(t)$ and $x_j[k]$ for $M = 4$ are illustrated in Figure 3.7. If SAH$_j$ is ideal, then $x_j[k]$ can be expressed as

$$x_j[k] = x\left(t_0 + (j-1) \times T_s + k \times MT_s + \tau_j\right) \tag{3.4}$$

In Equation (3.4), T_s is the nominal time interval between two consecutive samplings. The sampling rate for the entire system is $f_s = 1/T_s$. The time period of the ϕ_j clock
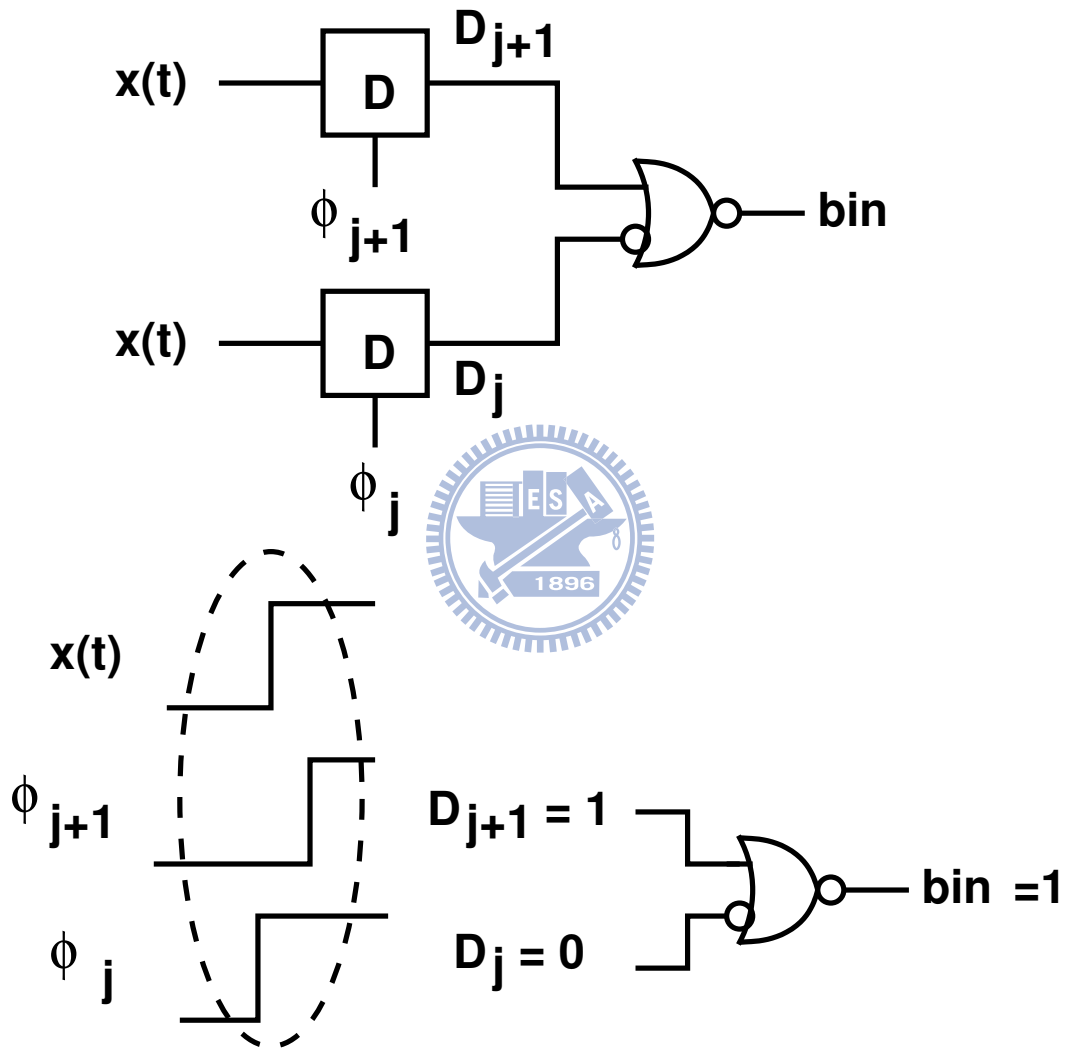
Figure 3.5: Edge detection of $x(t)$ using flip-flop and simple logic.
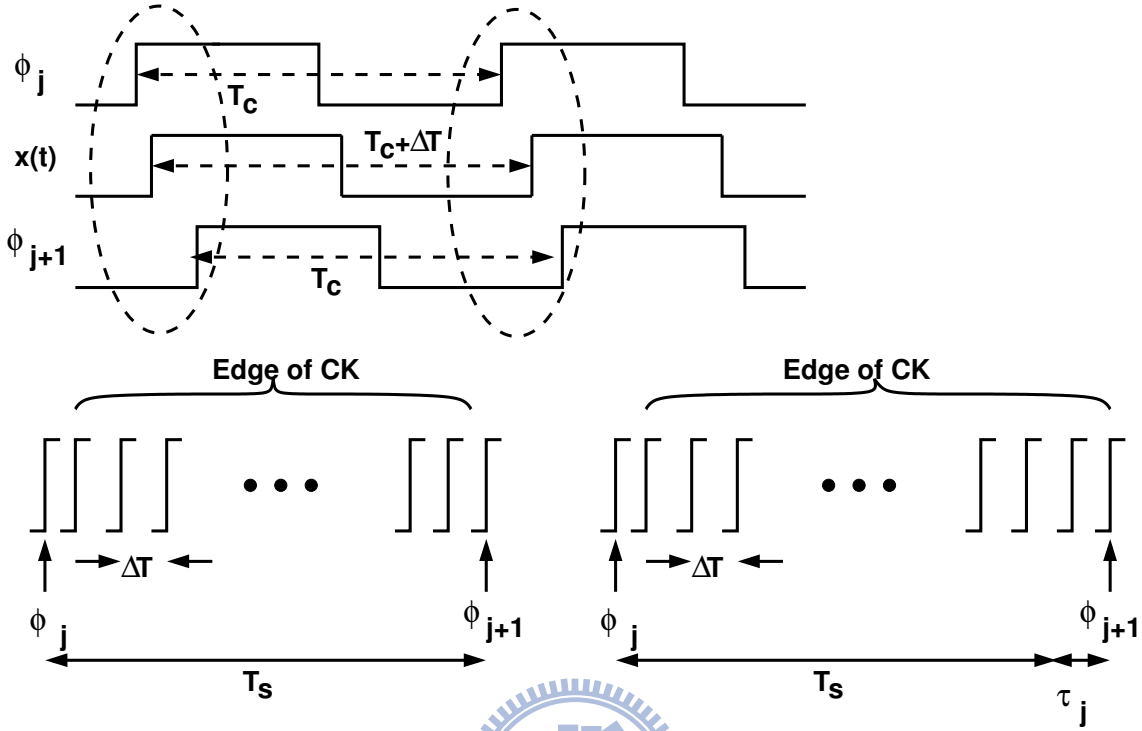
Figure 3.6: Illustration of timing skew detection using edge detector.

is $T_c = M \times T_s$. Its clock frequency is $f_c = 1/T_c$. The time position of $x(t)$ relative to the multi-phase clocks is represented by t_0, which is the sampling time of $x_1[0]$. The possible value of t_0 is between 0 and T_c. Lastly, τ_j is the individual timing offset of the ϕ_j clock. The value of t_0 is defined in such a way that the mean of τ_j is zero, i.e., $\tau_1 + \tau_2 + \cdots + \tau_M = 0$. A timing skew occurs between the clocks ϕ_j and ϕ_{j+1} if $\tau_j \neq \tau_{j+1}$.

Consider a $x(t)$ signal that is continuous in time and in magnitude. As time progresses, a zero crossing (ZC) occurs if $x(t)$ changes its polarity from positive to negative or from negative to positive. For example, in Figure 3.7, there is a ZC between $x_2[0]$ and $x_3[0]$, and another ZC between $x_2[1]$ and $x_3[1]$. There exists at least one ZC between $x_j[k]$ and $x_{j+1}[k]$ if $x_j[k] \times x_{j+1}[k] < 0$. If $x(t)$ is a stationary Gaussian process with zero mean, then the probability of $x_j[k] \times x_{j+1}[k] < 0$ for an arbitrary k is [22, 23, 24]

$$P^z_{j,j+1} = \frac{1}{2} - \frac{1}{\pi} \sin^{-1} \rho_{j,j+1} \tag{3.5}$$

with

$$\rho_{j,j+1} = \frac{E\left\{x_j[k] \times x_{j+1}[k]\right\}}{\sigma_j \times \sigma_{j+1}} \tag{3.6}$$
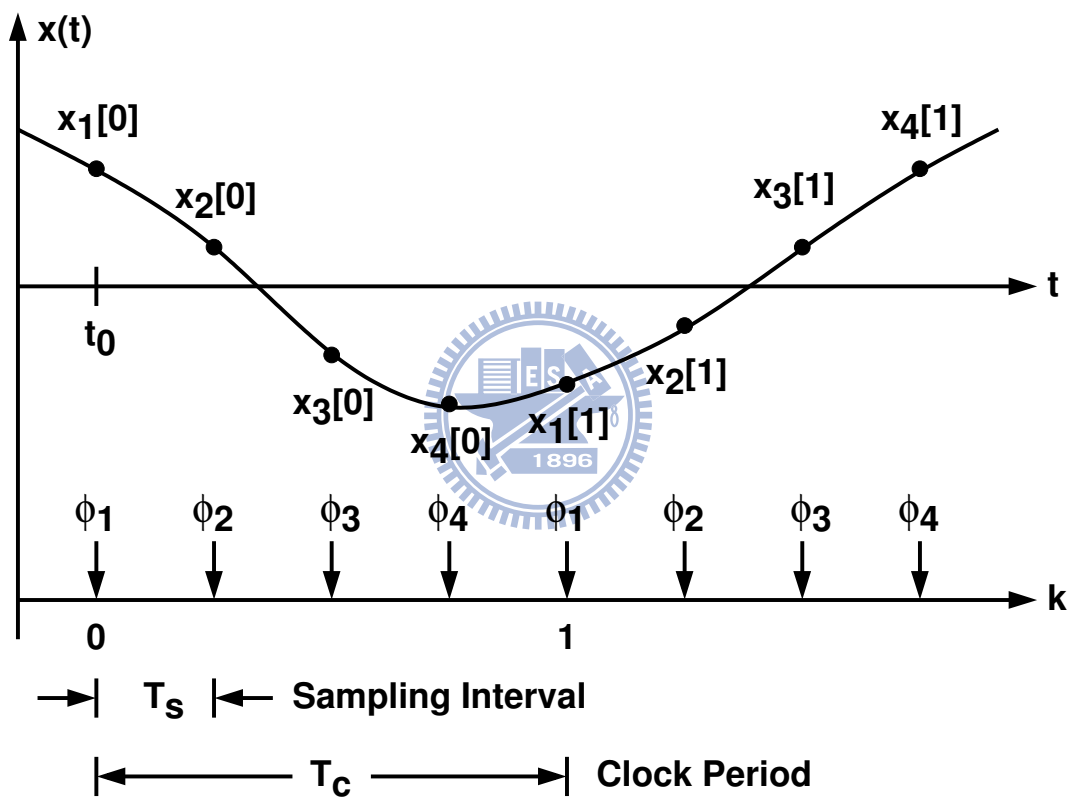
Figure 3.7: $x(t)$ and $x_j[k]$ sampled signal.
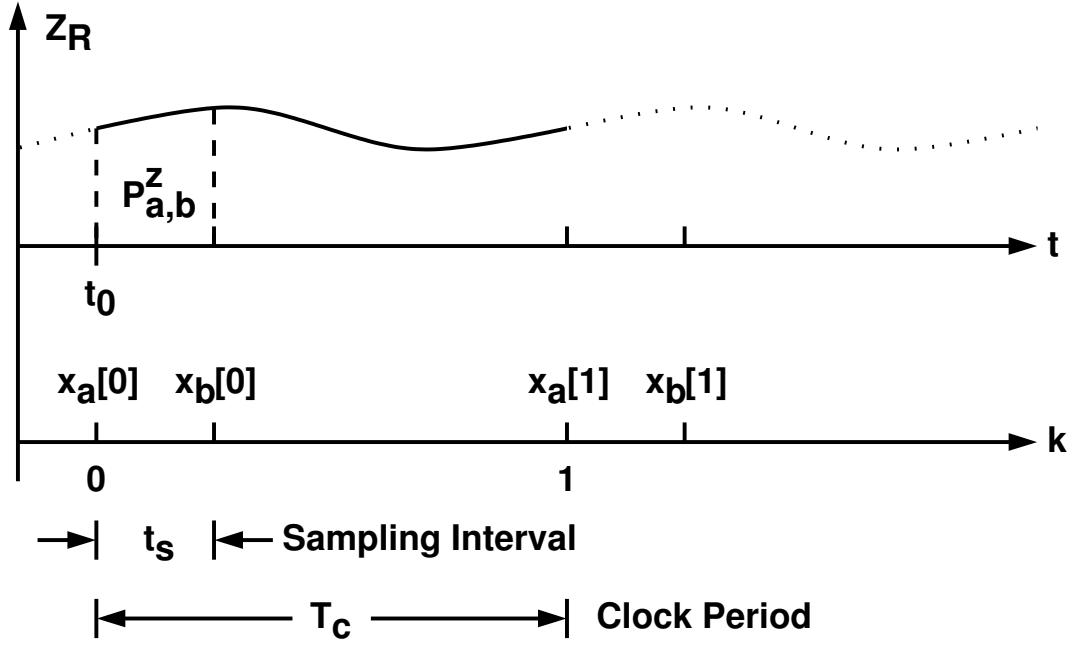
Figure 3.8: Zero-crossing density.

and

$$\sigma_j = \sqrt{E[x_j^2]} \qquad \sigma_{j+1} = \sqrt{E[x_{j+1}^2]} \tag{3.7}$$

where σ_j and σ_{j+1} are the standard deviations of $x_j[k]$ and $x_{j+1}[k]$ respectively. Furthermore, $\rho_{j,j+1}$ denotes the cross-correlation between $x_j[k]$ and $x_{j+1}[k]$. The value of $\rho_{j,j+1}$ is between $+1$ and -1. If $x(t)$ is a dc signal, then both $x_j[k]$ and $x_{j+1}[k]$ are constant, $x_j[k] = x_{j+1}[k]$, $\rho_{j,j+1} = 1$, and $P_{j,j+1}^z = 0$. Therefore, there is no ZC for a dc $x(t)$. If $x(t)$ is a single-tone sinewave with frequency at $1/(2T_s)$, then both $x_j[k]$ and $x_{j+1}[k]$ are also constant, but $x_j[k] = -x_{j+1}[k]$, $\rho_{j,j+1} = -1$, and $P_{j,j+1}^z = 1$, i.e., a ZC always occurs between $x_j[k]$ and $x_{j+1}[k]$ for every k.

Consider two sampling sequences, $x_a[k]$ and $x_b[k]$, as illustrated in Figure 3.8. Both sequences have an identical clock period of T_c. The sampling interval between $x_a[k]$ and $x_b[k]$ is t_s. The sampling time for $x_a[0]$ is t_0. For a generic $x(t)$ input, the cross-correlation of Equation (A.59) between $x_a[k]$ and $x_b[k]$ is denoted as $\rho_{a,b}(t_0, T_c, t_s)$. Note that $\rho_{a,b}(t_0, T_c, t_s)$ is a periodic function of t_0 and has a period of T_c. From Equation (3.5), the corresponding ZC probability between the two sampling sequences is $P_{a,b}^z(t_0, T_c, t_s)$.

The ZC density, defined as the ZC probability per unit t_s time, can be expressed as

$$
\begin{aligned}
Z_R(t_0, T_c) &\equiv \lim_{t_s \to 0} \frac{P_{a,b}^z(t_0, T_c, t_s)}{t_s} \\
&= \frac{1}{\pi} \times \sqrt{-\frac{\partial^2 \rho_{a,b}(t_0, T_c, t_s)}{\partial t_s^2}} \bigg|_{t_s=0}
\end{aligned}
\tag{3.8}
$$

For the sampling system of Figure 1.1, the ZC probability between $x_j[k]$ and $x_{j+1}[k]$ can be expressed as

$$
P_{j,j+1}^z = \int_{t_j}^{t_j+T_s} Z_R(t_0, T_c)dt_0
\tag{3.9}
$$

where $t_j = t_0 + (j-1) \times T_s$.

Consider $x(t) = A \sin(2\pi f_i t)$. The sinewave input has a frequency of f_i and an amplitude of A. The corresponding $\rho_{a,b}(t_0, T_c, t_s)$ is $\cos(2\pi f_i t_s)$, and the corresponding $Z_R(t_0, T_c)$ is

$$
Z_R(t_0, T_c) = \begin{cases}
2f_i & \frac{f_i}{f_c} \neq \frac{p}{q} \\
\frac{2}{q} \sum_{n=0}^{p-1} \delta\left(t_0 - n \times \frac{T_c}{p}\right) & \frac{f_i}{f_c} = \frac{p}{q} \quad q \text{ is even} \\
\frac{1}{q} \sum_{n=0}^{2p-1} \delta\left(t_0 - n \times \frac{T_c}{2p}\right) & \frac{f_i}{f_c} = \frac{p}{q} \quad q \text{ is odd}
\end{cases}
\tag{3.10}
$$

where $f_c = 1/T_c$ is the clock frequency, and p and q are two mutually prime positive integers. As shown in Figure 3.9, if the f_i/f_c ratio is irrational, i.e., $x(t)$ is asynchronous to the f_c clock, then Z_R is equal to $2f_i$ and independent of t_0 and T_c. If $f_i/f_c = p/q$, then $x(t)$ is synchronous with the f_c clock. In a synchronous case, ZCs occur only at certain instants if all clock periods are folded as one. There are p possible uniformly-spaced ZC instants if q is even. On the other hand, there are $2p$ possible uniformly-spaced ZC instants if q is odd.

The timing-skew calibration scheme proposed in this paper requires a $x(t)$ reference signal whose Z_R is nonzero and independent of t_0. One example is an asynchronous sinewave whose Z_R is $2f_i$ as described in Equation (A.67). As illustrated in Figure 3.10, if Z_R is constant, then the ZC probability between $x_j[k]$ and $x_{j+1}[k]$ is proportional to the T_s sampling interval, i.e., $P_{j,j+1}^z = Z_R \times T_s$. If timing skew occurs and the sampling interval becomes $T_s + \Delta\tau_j$, the ZC probability is deviated by an amount of $\Delta P_{j,j+1}^z = Z_R \times \Delta\tau_j$. By comparing $P_{j,j+1}^z$ and $P_{j+1,j+2}^z$, one can determine whether the sampling interval between
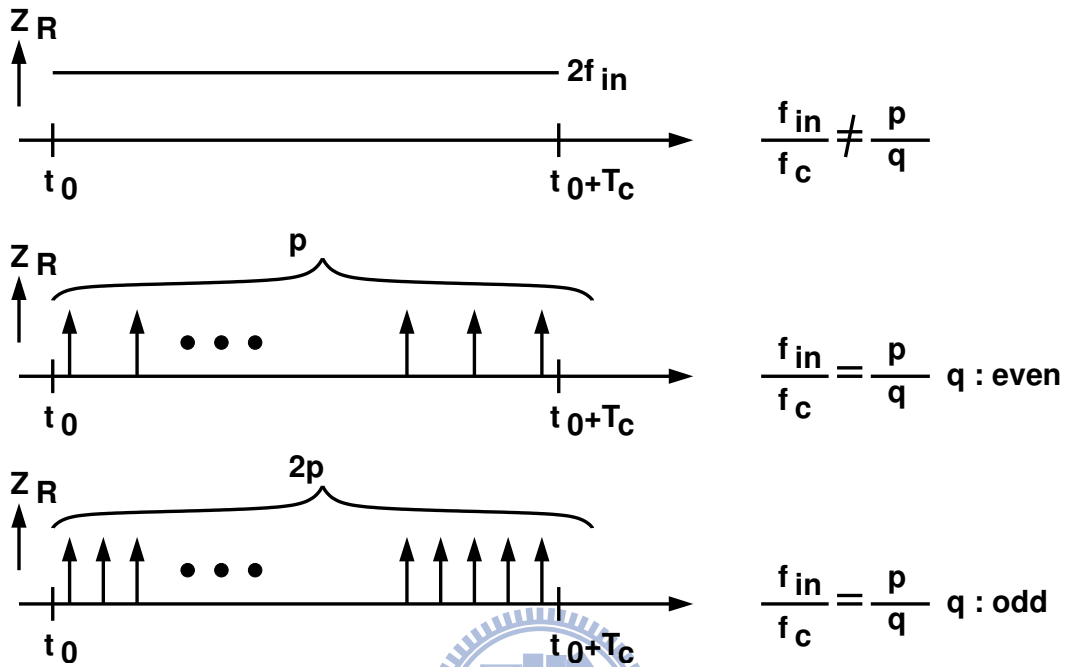
Figure 3.9: Zero crossing density of sine wave.
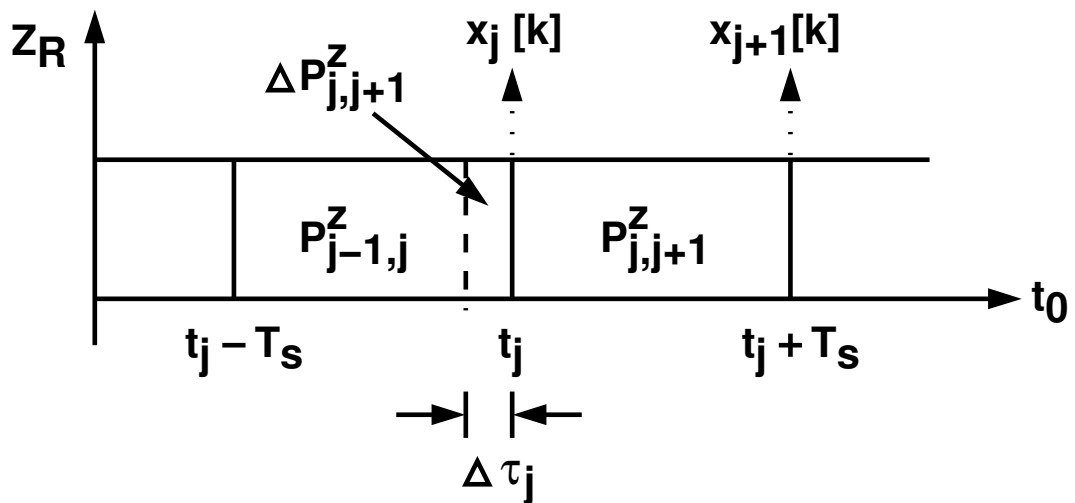
Figure 3.10: Constant zero-crossing density and timing-skew detection.
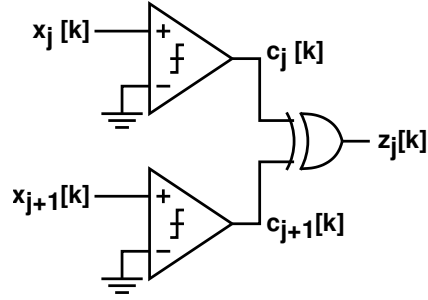
Figure 3.11: A simple zero-crossing detector (ZCD1).

$x_j[k]$ and $x_{j+1}[k]$ is larger or smaller than the sampling interval between $x_{j+1}[k]$ and $x_{j+2}[k]$.

The $x(t)$ reference signal required by the proposed calibration scheme is not restricted to single-tone sinewaves. Any $x(t)$ signal can have a Z_R independent of t_0 if it is narrow-band and asynchronous to the sampling clocks. Referring to Figure 3.8, assume both $x_a[k]$ and $x_b[k]$ are sampling sequences with $T_c = 1/f_c$ sampling interval. If the bandwidth of $x(t)$ is less than $f_c/2$ so that it does not cause aliasing, then both $x_a[k]$ and $x_b[k]$ observe the same signal but with different delays. As a result, $\rho_{a,b}(t_0, T_c, t_s)$ is only a function of the t_s delay difference. From Equation (A.63), the corresponding Z_R is independent of t_0.

A $x(t)$ signal is said to be synchronous with the sampling clocks if it consists of only single-tone sinewaves that are synchronous with the sampling clocks. Its $Z_R(t_0, T_c)$ will comprise δ-functions similiar to those in Equation (A.67). Under the synchronous $x(t)$ condition, the proposed calibration scheme can still function if the $Z_R(t_0, T_c)$'s δ-functions have the same magnitude and are uniformly spread over one T_c period. The spacing between the δ-functions must be smaller than the desired calibration timing resolution.

3.3   Zero-Crossing (ZC) Detection

3.3.1   Simple ZC Detector (ZCD1)

Figure 3.11 shows a simple zero-crossing detector (ZCD1) to determine if a ZC occurs between $x_j[k]$ and $x_{j+1}[k]$. Both samples are compared with a zero reference to determine their polarities. If the $x_j[k]$'s polarity is different from the $x_{j+1}[k]$'s polarity, then the

detector issues $z_j[k] = 1$, otherwise, $z_j[k] = 0$. The probability of $z_j[k] = 1$ is the $P^z_{j,j+1}$ of Equation (3.5) or Equation (A.65). This ZC detection scheme is simple but sensitive to comparators' offsets. Detailed analysis is provided in Appendix A.1. Assume the two comparators exhibit the input-referred offsets O_j and O_{j+1} respectively, as shown in Figure A.1. The resulting $P^z_{j,j+1}$ is deviated from Equation (3.5) by an amount of $\Delta P^z_{j,j+1}$, which can be approximated by

$$\Delta P^z_{j,j+1} \approx \frac{\rho_{j,j+1}}{2\pi \sqrt{1 - \rho^2_{j,j+1}}} \left(\frac{O^2_j}{\sigma^2_j} + \frac{O^2_{j+1}}{\sigma^2_{j+1}} - \frac{2}{\rho_{j,j+1}} \frac{O_j}{\sigma_j} \frac{O_{j+1}}{\sigma_{j+1}} \right) \qquad (3.11)$$

The $\Delta P^z_{j,j+1}$ variation depends not only on the normalized offsets, O_j/σ_j and O_{j+1}/σ_{j+1}, but also on the cross-correlation, $\rho_{j,j+1}$. For a slow-varying $x(t)$, $\rho_{j,j+1} \approx 1$, $\sigma_j \approx \sigma_{j+1}$, then $\Delta P^z_{j,j+1}$ is proportional to $(O_j - O_{j+1})^2$. The resulting $P^z_{j,j+1}$ probability is sensitive to the offset mismatch. For a single-tone $x(t)$ with frequency close to $1/(2T_s)$, $\rho_{j,j+1} \approx -1$, $\sigma_j \approx \sigma_{j+1}$, then $\Delta P^z_{j,j+1}$ is proportional to $(O_j + O_{j+1})^2$. The offset sensitivity is reduced when large $x(t)$ is applied, since large $x(t)$ leads to large σ_j and σ_{j+1}.

When using a ZCD1 to measure the sampling interval between $x_j[k]$ and $x_{j+1}[k]$ of the sampling system shown in Figure 1.1, the $\Delta P^z_{j,j+1}$ due to offsets can lead to skew measurement error, $\Delta \tau_{j,os}$. The relationship can be expressed as

$$\Delta P^z_{j,j+1} = Z_R(t_0, T_c) \times \Delta \tau_{j,os} \qquad (3.12)$$

where $Z_R(t_0, T_c)$ is the ZC density defined in Equation (A.63). Consider the 8-channel 6-bit TI ADC defined in Chapter 1. Assume the input $x(t) = \sin(2\pi f_i t)$ is a full-range single-tone sinewave asynchronous to the f_c clock. To illustrate a low f_i case, let $f_i \approx 0.25 f_c$, then we have $Z_R = 2f_i \approx 0.5 f_c$, $\rho_{j,j+1} = +0.98$, and $\sigma^2_j = 1/2$. The resulting $\Delta \tau_{j,os}$ versus $|O_j - O_{j+1}|$ is shown in Figure 3.12. The solid line is obtained using Equation (3.11) and Equation (3.12). The black circles are time-domain simulation results. In the simulations, a sinewave with f_i frequency is served as the $x(t)$ input. In each simulation, $P^z_{j,j+1}$ is obtained by calculating the ratio of the number of times $z_j[k] = 1$ to the total number of k. In Figure 3.12, $\Delta \tau_{j,os}$ and $|O_j - O_{j+1}|$ are normalized with T_{LSB} and V_{LSB} respectively, where T_{LSB} and V_{LSB} are defined in Chapter 1. To achieve $\Delta \tau_{j,os} < 1 \, T_{\text{LSB}}$, the offset requirement for the ZCD1 is $|O_j - O_{j+1}| < 1.27 \, V_{\text{LSB}}$. On the other hand, to
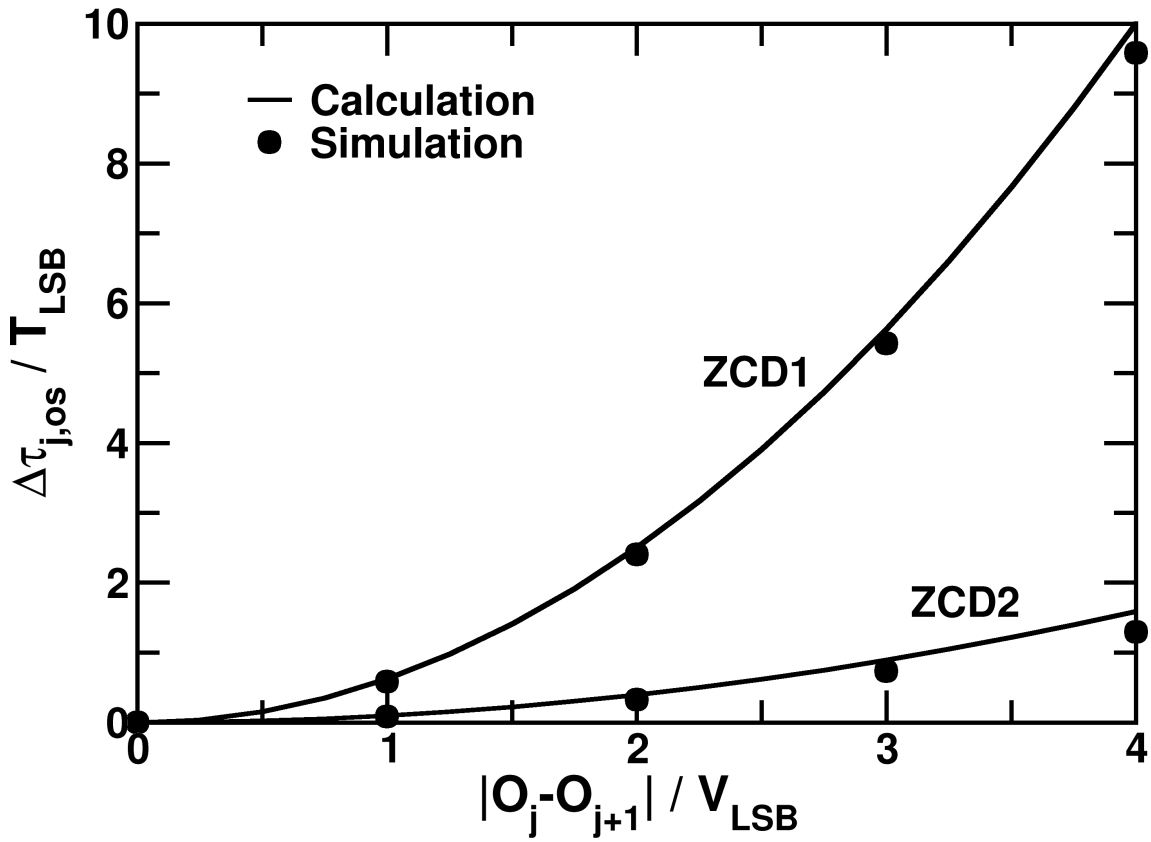
Figure 3.12: Skew measurement error due to comparators' offsets. Low-frequency case with $f_i \approx 0.25 f_c$. The ZCD2 curve is plotted with $O_{j+1} = 0$ so that $O_j - O_{j+1} = O_j + O_{j+1}$.
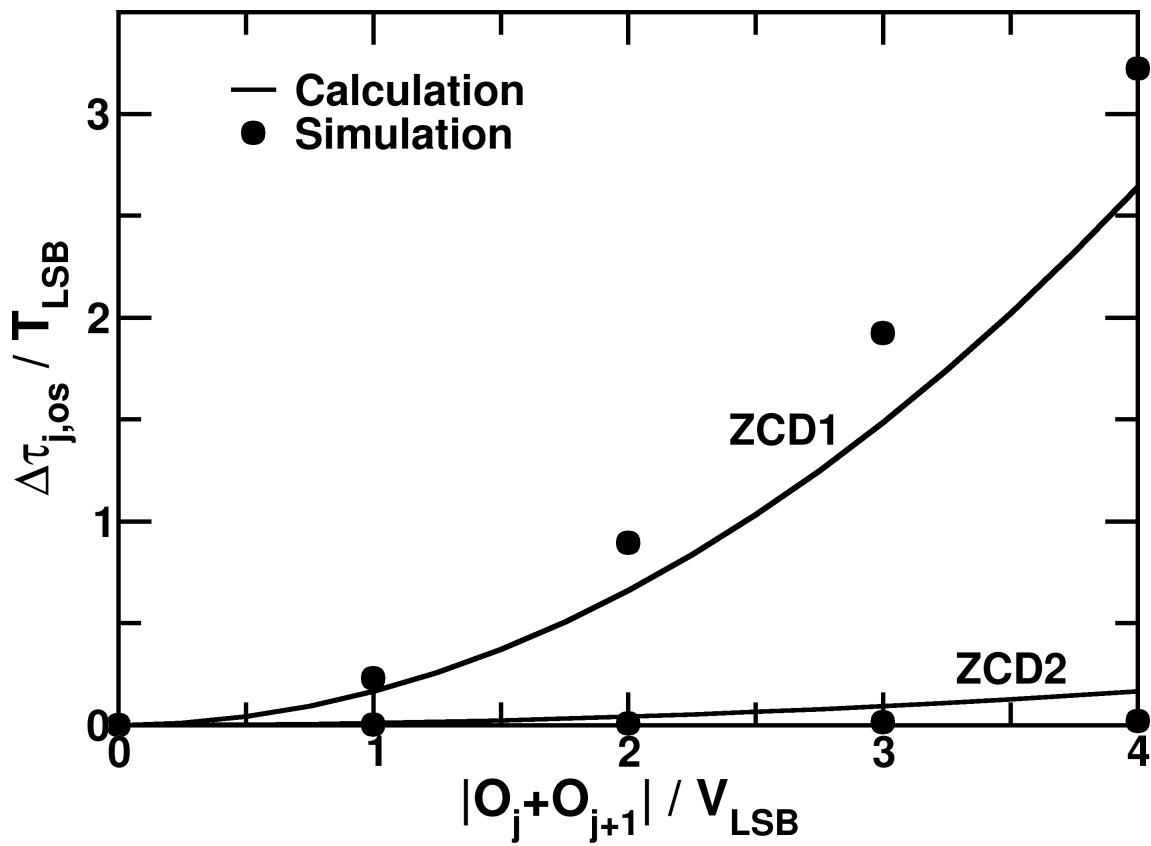
Figure 3.13: Skew measurement error due to comparators' offsets. High-frequency case with $f_i \approx 3.75 f_c$.
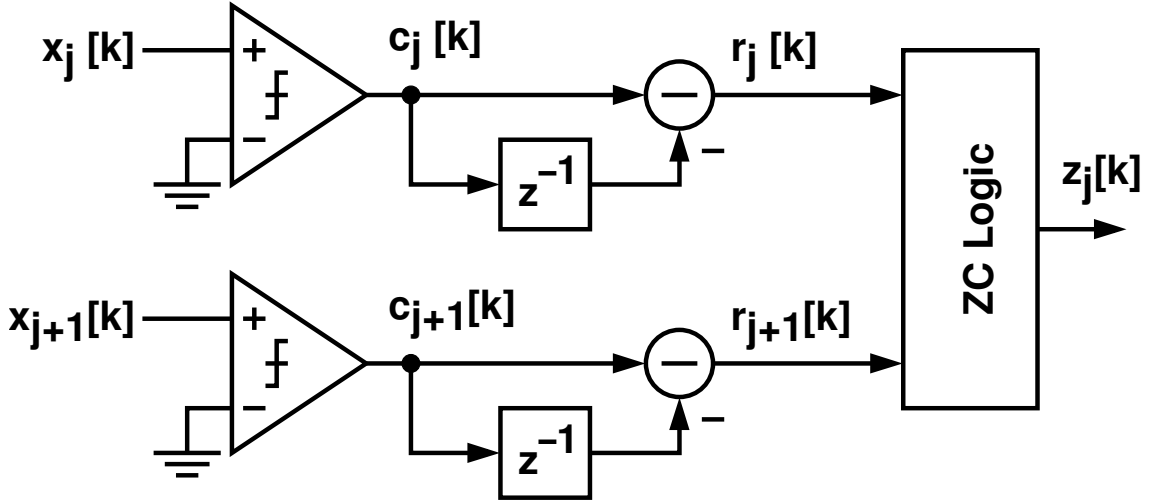
Figure 3.14: A pseudo zero-crossing detector (ZCD2).

illustrate a high f_i case, let $f_i \approx 3.75 f_c$, then we have $Z_R = 2 f_i \approx 7.5 f_c$, $\rho_{j,j+1} = -0.98$, and $\sigma_j^2 = 1/2$. The resulting $\Delta \tau_{j,os}$ versus $|O_j + O_{j+1}|$ is shown in Figure 3.13. To achieve $\Delta \tau_{j,os} < 1 \ T_{\mathrm{LSB}}$, the offset requirement for the ZCD1 is $|O_j + O_{j+1}| < 2.4 \ V_{\mathrm{LSB}}$. Although its offset requirement is more stringent than that of a high f_i case, a low f_i case is usually preferred. A lower f_i frequency implies a slower circuit for realizing the $x(t)$ signal generator. In addition, the $x(t)$ signal leakage due to capacitor coupling is less severe if a lower f_i is chosen.

Previous analyses assume that the mean value of the $x(t)$ signal is zero. The effect of $x(t)$'s dc offset is also analyzed in Appendix A.1. As described in Equation (A.9) and Equation (A.10), both $P_{j,j+1}^z$ and Z_R are reduced by the dc offset, O_x. Since its effect is identical to all ZC detectors in the proposed timing-skew detection scheme, the O_x does not affect its accuracy. As described in the next section, timing skew is detected by measuring the $P_{j,j+1}^z$ difference between the ZC detectors. The absolute value of $P_{j,j+1}^z$ is irrelevant.

3.3.2   Pseudo ZC Detector (ZCD2)

Figure 3.14 shows the proposed pseudo ZC detector (ZCD2). Two $1 - z^{-1}$ high-pass filters are added after the comparators to reduce the detection sensitivity to comparators' offsets.

Outputs from the comparators are $c_j[k]$ and $c_{j+1}[k]$. Their binary values are $\{0, 1\}$. Thus, the outputs of the filters, $r_j[k]$ and $r_{j+1}[k]$, have triple values $\{-1, 0, +1\}$. The ZC logic determines the $z_j[k]$ output as follows. The output $z_j[k] = 1$ if $r_j[k] \times r_{j+1}[k] \leq 0$, otherwise $z_j[k] = 0$. In other words, $z_j[k] = 0$ if both $r_j[k]$ and $r_{j+1}[k]$ are $+1$ or both are -1.

To gain an insight of the ZCD2 operation, one can approximate the comparators as linear amplifiers with random quantization noises. Thus, the ZCD2 becomes a ZC detector that detects the ZC in the $x(t) - x(t - T_c)$ signal. The comparators' offsets are removed by the $1 - z^{-1}$ operation, resulting in a reduced ZC detection sensitivity to offsets.

Unlike the ZCD1, whose output follows the ZC probability $P_{j,j+1}^z$ of Equation (3.5) and the ZC density $Z_R(t_0, T_c)$ of Equation (A.63), it is difficult to derive the explicit $P_{j,j+1}^z$ and $Z_R(t_0, T_c)$ expressions for the ZCD2. The ZCD2 detection is no longer a simple detection of ZC in $x(t)$. It detects certain events that cause $z_j[k] = 1$. A simplified analysis for the cases with low f_i frequency is provided in Appendix A.2. In such cases, $\rho_{j,j+1} \approx 1$, and the probability for $z_j[k] = 1$ can be approximated by Equation (A.19). As explained in Appendix A.2, the $Z_R(t_0, T_c)$ of Equation (A.63) can be used to analyze the behaviors of both ZCD1 and ZCD2 in the low-f_i scenario of the proposed timing-skew detection scheme. The effect of comparators' offsets on the ZCD2 is also analyzed in Appendix A.2. When offsets appear, the ZC probability $P_{j,j+1}^z$ is deviated from Equation (A.19) by an amount of $\Delta P_{j,j+1}^z$. Its upper bound can be expressed as

$$\Delta P_{j,j+1}^z \leq \frac{1}{4\pi} \left(\frac{O_j}{\sigma_j} + \frac{O_{j+1}}{\sigma_{j+1}} \right)^2 \tag{3.13}$$

Figure 3.12 and Figure 3.13 also show the ZCD2 timing skew measurement error due to the O_j and O_{j+1} offsets. It is clear from both figures that the ZCD2 is less sensitive to offsets. For the low-f_i scenario with $f_i \approx 0.25 f_c$, the ZCD2 requires $|O_j + O_{j+1}| <$ 3.1 V_{LSB} to achieve a skew measurement error less than 1 T_{LSB}.

Chapter 4

Timing Skew Calibration

Consider the M-phase sampling system of Figure 1.1. It samples the $x(t)$ reference and generates the $x_j[k]$ of Equation (3.4), where $1 \le j \le M$. Its nominal sampling interval is T_s. However, each ϕ_j clock has its own timing offset, τ_j. If two adjacent clocks, ϕ_j and ϕ_{j+1}, have different timing offset, i.e., $\tau_j \ne \tau_{j+1}$, then a timing skew occurs. The sampling interval between $x_j[k]$ and $x_{j+1}[k]$ becomes $T_s - \tau_j + \tau_{j+1}$. Figure 1.3 shows the proposed multi-phase timing-skew calibration architecture. A multi-phase timing-skew calibration processor (TSCP) is used to detect the timing skew between every adjacent clock pairs. For each j, the delay of the B_j clock buffer is controlled by the $T_j[k]$ output from the TSCP, such that

$$\tau_j[k] = \tau_{j,0} + \mu_t \times T_j[k] \tag{4.1}$$

where μ_t is the step size for the timing control and $\tau_{j,0}$ is the timing offset of the ϕ_j clock when $T_j[k] = 0$. The TSCP measures the timing skew between ϕ_j and ϕ_{j+1}, then adjusts $T_{j+1}[k]$ to minimize the skew.

Figure 4.1 shows the TSCP's block diagram. It includes M ZC detectors, which are deployed to measure the sampling intervals. Either the ZCD1 of Figure 3.11 or the ZCD2 of Figure 3.14 can be used as the ZC detectors. The $x(t)$ reference is assumed to be a narrow-band signal. Its center frequency f_i is near $0.25 f_c$ in order to establish a low-f_i scenario. For the j-th calibration channel, its ZC detector senses any ZC between $x_j[k]$ and $x_{j+1}[k]$, and generates a binary output, $z_j[k] \in \{0, 1\}$. The probability of $z_j[k] = 1$ is $P_{j,j+1}^z$, which can be calculated from the ZC density $Z_R(t_0, T_c)$ using Equa-
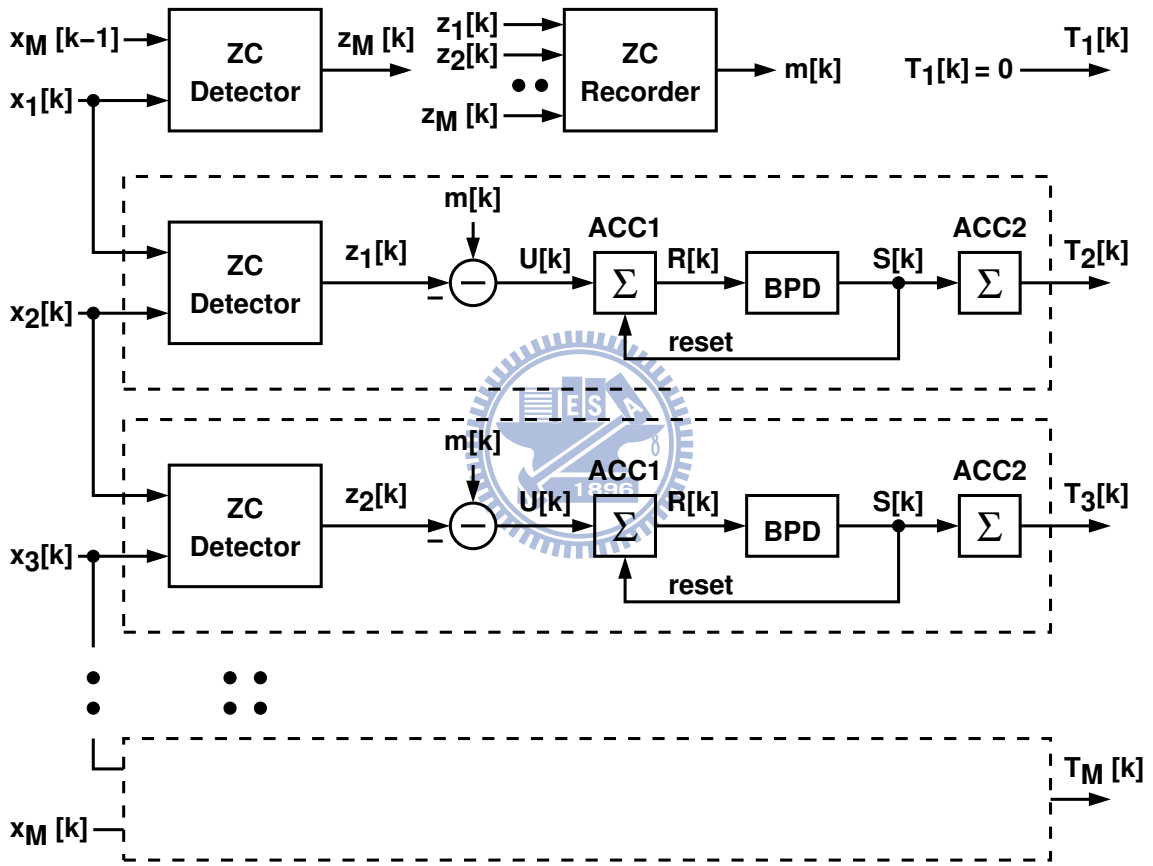
Figure 4.1: A multi-phase timing-skew calibration processor (TSCP).
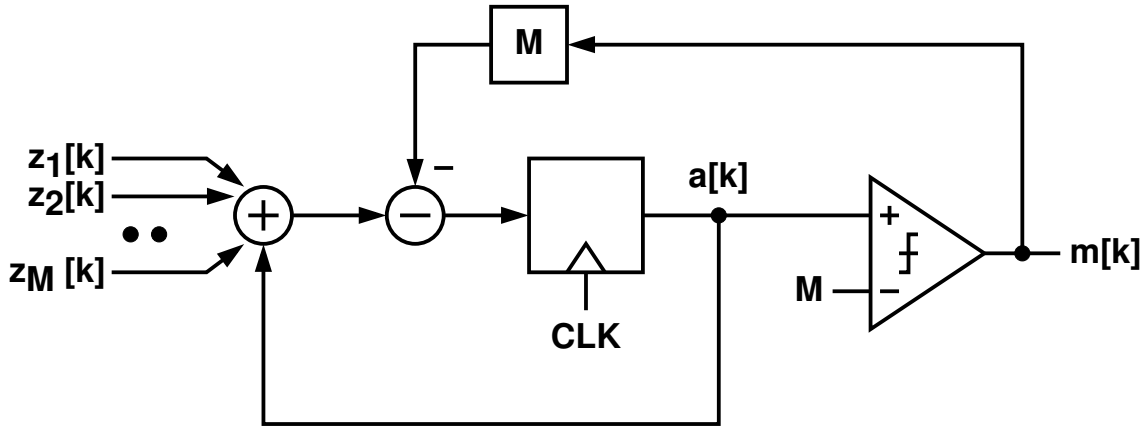
Figure 4.2: The ZC recorder.

tion (A.65). From Equation (A.67), a narrow-band asynchronous $x(t)$ reference has an uniform $Z_R(t_0, T_c)$ close to $2f_i$. Thus, the $P^z_{j,j+1}$ probability is proportional to the sampling interval between $x_j[k]$ and $x_{j+1}[k]$, which is denoted the j-interval. In Figure 4.1, the $z_j[k]$ sequence is integrated onto an ACC1 accumulator. The accumulator's output represents the average of $z_j[k]$, which is also proportional to the j-interval.

For each j, the TSCP compares the j-interval with the nominal sampling interval. The difference between the two intervals is the timing skew. The TSCP then adjusts $T_{j+1}[k]$ to minimize the skew. The nominal sampling interval is defined as the average of all j-interval where $1 \leq j \leq M$. In Figure 4.1, the timing skew is calculated as the difference between the accumulation of $z_j[k]$ and the accumulation of $m[k]$. The $m[k]$ sequence represents the average of the ZC occurrences among all sampling intervals. The $m[k]$ is generated from the ZC recorder shown in Figure 4.2. The recorder accumulates every ZC from all ZC detectors. A comparator compares the accumulation result $a[k]$ with M, and generates a binary $m[k] \in \{0, 1\}$ for every clock cycle. Whenever $a[k] \geq M$, the comparator issues $m[k] = 1$, and an amount of M is subtracted from the accumulation result during the following clock cycle. Note that $m[k]$ is a sequence of 0 and 1. Its mean value represents the nominal sampling interval. The operation of $m[k]$ averaging is provided by the ACC1 accumulator in each calibration channel. The proposed ZC recorder is simple and its hardware cost is low.

In the j-th calibration channel, the timing skew is calculated as $U[k] = m[k] - z_j[k]$.

A simple calibration loop can be formed by applying $T_{j+1}[k+1] = T_{j+1}[k] + \mu \times U[k]$ with $\mu < 1$. However, the resulting fluctuation in $T_{j+1}[k]$ is large unless a very small μ is chosen. In Figure 4.1, an additional accumulator is added to reduce the $T_{j+1}[k]$ fluctuation. The ACC1 accumulator integrates the $U[k]$ sequence, and generates the $R[k]$ output. A bilateral peak detector, BPD, monitors the value of $R[k]$ and generates a corresponding triple-valued output, $S[k] \in \{+1, 0, -1\}$. The BPD has two thresholds, $+N_C$ and $-N_C$. Whenever $R[k] \geq +N_C$, $S[k] = +1$. Whenever $R[k] \leq -N_C$, $S[k] = -1$. Otherwise, $S[k] = 0$. In addition, the ACC1 accumulator is reset to zero whenever $S[k] = +1$ or $S[k] = -1$. Thus, $-N_C \leq R[k] \leq +N_C$. Each time $S[k]$ is either $+1$ or -1, it can retain in such state for only one clock cycle. Finally, the ACC2 accumulator integrates the $S[k]$ sequence, and generates the $T_{j+1}[k]$ output. By adding the integration-and-dump operation of ACC1 and BPD, the fluctuation in $T_{j+1}[k]$ is reduced.

In the proposed calibration scheme, the ϕ_1 clock in Figure 1.3 is a designated reference phase. It is no need to adjust the corresponding $T_1[k]$ control. Thus, $T_1[k]$ is preset to 0 in the TSCP of Figure 4.1.

The proposed calibration scheme contains two system parameters, μ_t and N_C. To simplify analysis, we assume each calibration channel in the TSCP of Figure 4.1 employs identical μ_t and N_C. Together with the Z_R of $x(t)$, they affect calibration behaviors, such as calibration converging speed and timing fluctuation. In general, large μ_t and small N_C result in fast converging speed but large timing fluctuation. On the other hand, small μ_t and large N_C result in small timing fluctuation but also slow converging speed. The following two subsections give detailed analyses.

4.1   Convergent Speed

Consider the j-th calibration channel in Figure 4.1. Its ZC detector measures the sampling interval between the ϕ_j and ϕ_{j+1} clocks. According to Equation (3.4), the ϕ_j and ϕ_{j+1} clocks have the timing offsets τ_j and τ_{j+1} respectively. In Figure 4.1, the $U[k]$ signal is the difference between $z_j[k]$ and $m[k]$, representing the timing skew $\tau_j - \tau_{j+1}$. The $U[k]$ is used to update the $T_{j+1}[k]$ signal, which controls the $\tau_{j+1}[k]$ timing offset. In most cases, this calibration loop can be modeled as a continuous-time single-pole feedback system

like

$$d\tau_{j+1} = \mu_t \times \frac{(\tau_j - \tau_{j+1}) \cdot Z_R \cdot dk}{N_C}$$

The above equation states that, to update τ_{j+1} by one μ_t step, it takes dk sampling intervals during which the $\tau_j - \tau_{j+1}$ timing skew causes N_C zero crossings. Thus, we obtain the following differential equation for $\tau_{j+1}[k]$

$$\frac{d\tau_{j+1}[k]}{dk} = -\frac{\tau_{j+1}[k] - \tau_j[k]}{\tau_c} \tag{4.2}$$

where the system time constant τ_c is

$$\tau_c = \frac{N_C}{\mu_t} \times \frac{1}{Z_R} \tag{4.3}$$

For a M-channel system, Equation (4.2) with $1 \le j \le M - 1$ can be expanded into $M - 1$ coupled equations. In most practical case, τ_c is much larger than 1. Thus, by treating $\tau_j[k]$ as a constant, the transient behavior of $\tau_{j+1}[k]$ can be approximated by a simple exponential function with the τ_c time constant.

4.2 Timing Fluctuation

Consider the $\tau_j[k]$ of Equation (A.62). The TSCP measures the sampling interval between the ϕ_{j-1} and ϕ_j clocks, and then adjusts $T_j[k]$. Assume $T_{j-1}[k]$ remains constant and ϕ_{j-1} is fixed. The TSCP adjusts only $T_j[k]$ to force $\tau_j[k]$ moving toward 0. As the process converges, the behavior of $\tau_j[k]$ becomes a discrete random fluctuation around zero. Figure 4.3 illustrates a probability mass function for τ_j, $M(\tau_j)$. The discrete values for τ_j is $\tau_{j,0}, \tau_{j,\pm 1}, \tau_{j,\pm 2}, \ldots$, with $\tau_{j,0}$ being closest to zero. The distance between two adjacent discrete values is μ_t. The value of $\tau_{j,0}$ is between $-0.5\mu_t$ and $+0.5\mu_t$. The calibration loop forces the maximum value of $M(\tau_j)$ to occur at $\tau_{j,0}$. A mathematical treatment of $M(\tau_j)$ is included in Appendix A.3. The resulting standard deviation of τ_j, averaged over possible value of $\tau_{j,0}$, can be found as

$$\sigma^2(\tau) = \frac{1}{6}\mu_t^2 + \frac{4T_s}{3N_C}\mu_t \tag{4.4}$$

Obviously, smaller μ_t and larger N_C can reduce $\sigma^2(\tau)$.
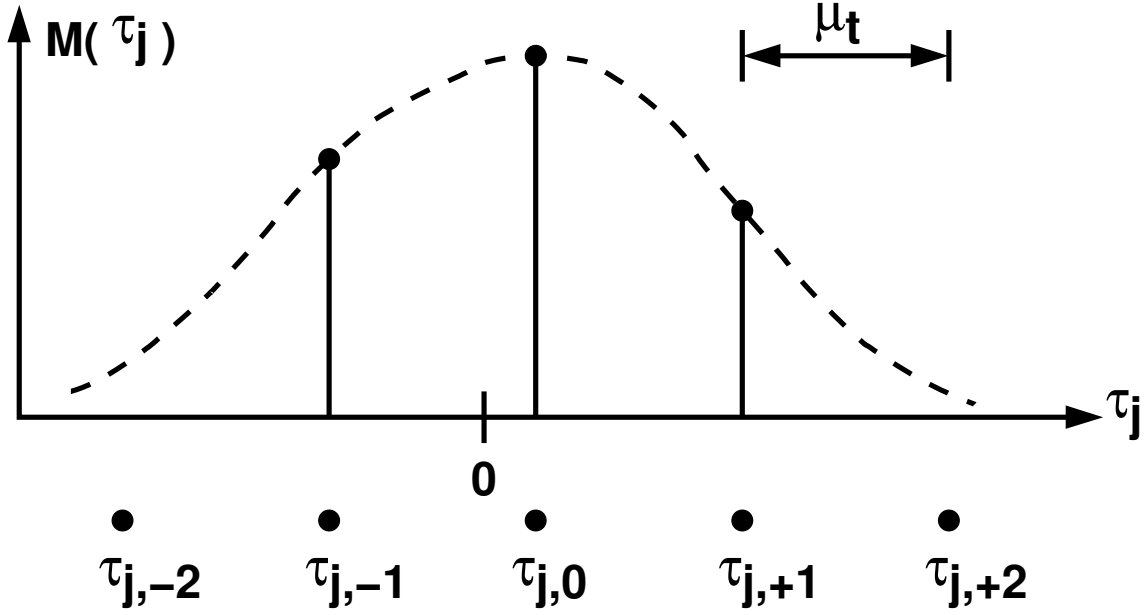
Figure 4.3: Probability mass function of τ_j, $M(\tau_j)$.

For the multi-phase calibration system shown in Figure 1.3 and Figure 4.1, the ϕ_1 clock with $T_1[k] = 0$ is chosen as the designated reference phase. All other clocks are adjusted by the TSCP to achieve uniform phase spacing. The timing skew between ϕ_1 and ϕ_2 is minimized by adjusting the delay of the ϕ_2 clock buffer through $T_2[k]$. The timing skew between ϕ_2 and ϕ_3 is minimized by adjusting the delay of the ϕ_3 clock buffer through $T_3[k]$. This calibration arrangement repeats for ϕ_4, ϕ_5, etc, and is referred as the linear referencing arrangement illustrated in Figure 4.4. Note that ϕ_1 does not fluctuate. The timing fluctuation of ϕ_2 is summarized by Equation (4.4). The timing fluctuation of ϕ_3 is larger than Equation (4.4), since it uses the fluctuating ϕ_2 as its phase reference. In fact, the timing fluctuation is accumulated along the reference chain. The standard deviation of the ϕ_j's timing fluctuation can be expressed as

$$\sigma^2(\tau_j) = (j - 1) \times \sigma^2(\tau) \qquad j \geq 2 \tag{4.5}$$

To reduce the overall timing fluctuation, the circular referencing arrangement shown in Figure 4.4 is suggested. In this scheme, both ϕ_2 and ϕ_8 use ϕ_1 as the reference for timing-skew calibration. Then ϕ_3 and ϕ_7 use ϕ_2 and ϕ_8 as the references respectively. In this arrangement, the maximum $\sigma^2(\tau_j)$ is reduced by half. The overall averaged timing fluctu-

Linear Referencing Scheme

ϕ_1 ϕ_2 ϕ_3 ϕ_4 ϕ_5 ϕ_6 ϕ_7 ϕ_8
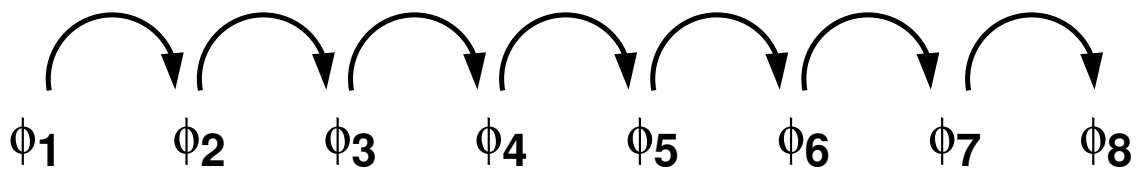
Circular Referencing Scheme
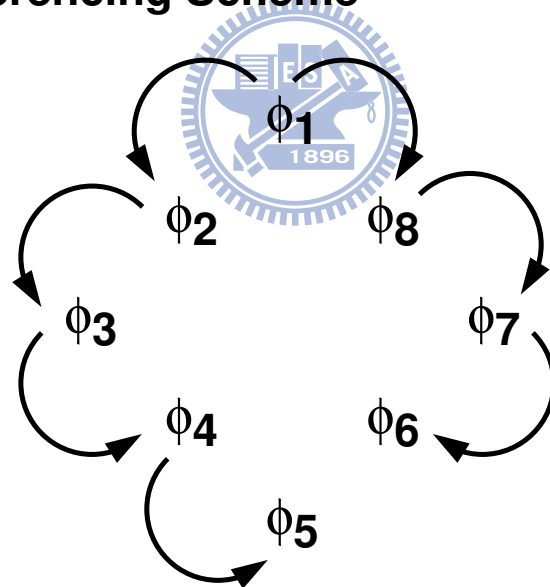
Figure 4.4: Referencing schemes for multi-phase clocks.

ation is

$$\sigma^2(\tau_T) \equiv \frac{1}{M} \sum_{j=1}^{M} \sigma^2(\tau_j) = \frac{M}{4}\sigma^2(\tau) = \frac{M}{24}\mu_t^2 + \frac{MT_s}{3N_C}\mu_t \tag{4.6}$$

where M is assumed to be an even number. For this multi-phase calibration system, $\sigma^2(\tau_T)$ is proportional to the number of phases, M.

To realize the circular referencing arrangement shown in Figure 4.4, the calibration processor of Figure 4.1 is modified as follows. The calibration channel that generates the $T_8[k]$ output takes $x_1[k]$ and $x_8[k]$ as its inputs. The calibration channel that generates the $T_7[k]$ output takes $x_8[k]$ and $x_7[k]$ as its inputs. The calibration channel that generates the $T_6[k]$ output takes $x_7[k]$ and $x_6[k]$ as its inputs. The calibration channels for $T_1[k], \cdots, T_5[k]$ remain unchanged. The extra ZC detector at the upper-left corner of Figure 4.1 now receives $x_5[k]$ and $x_6[k]$ as its inputs and generates the $z_5[k]$ output.

4.3   An 8-channel Time-Interleaved ADC System Simulation

Figure 4.5 shows an 8-channel time-interleaved ADC that employs the timing-skew calibration scheme described in Chapter 4. There are 8 A/D channels, i.e., ADC$_j$ where $1 \le j \le 8$. Each A/D channel samples and quantizes the $s(t)$ input and produces a corresponding $s_j[k]$ sequence. The $s_j[k]$ sequences from all channels are then multiplexed to generate the final $s[l]$ digital output. In the j-th channel, there are two samplers driven by the same ϕ_j clock. One sampler samples the $s(t)$ input to be quantized into $s_j[k]$. The succeeding quantizer (QTZ) has 6-bit resolution and an input range between ± 1. The other sampler receives the $x(t)$ reference and generates the $x_j[k]$ sequence. The $x_j[k]$ sequence is sent to the timing-skew calibration processor shown in Figure 4.1. Its $T_j[k]$ output controls the B_j clock buffer shown in Figure 1.3. For the 8-phase clock generator, the nominal timing interval between two adjacent phases is T_s. Each ϕ_j clock has a period of $T_c = 8T_s$ and a frequency of $f_c = 1/T_c$. The entire system is equivalent to a 6-bit ADC with a sampling rate of $f_s = 1/T_s = 8f_c$. As in Chapter 1, we define the magnitude resolution as $V_{\text{LSB}} = 2/2^6 = 2^{-5}$ and the timing resolution as $T_{\text{LSB}} = T_s/2^6$.
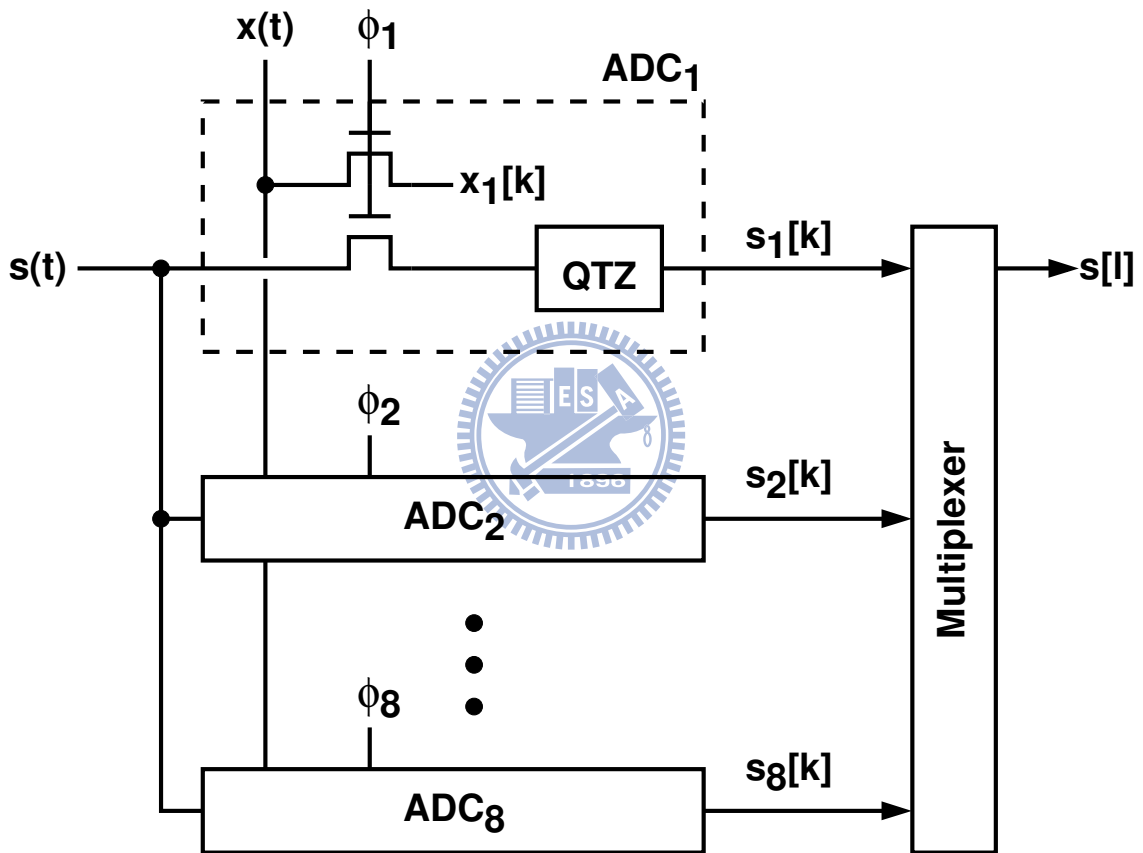
Figure 4.5: An 8-channel time-interleaved ADC.
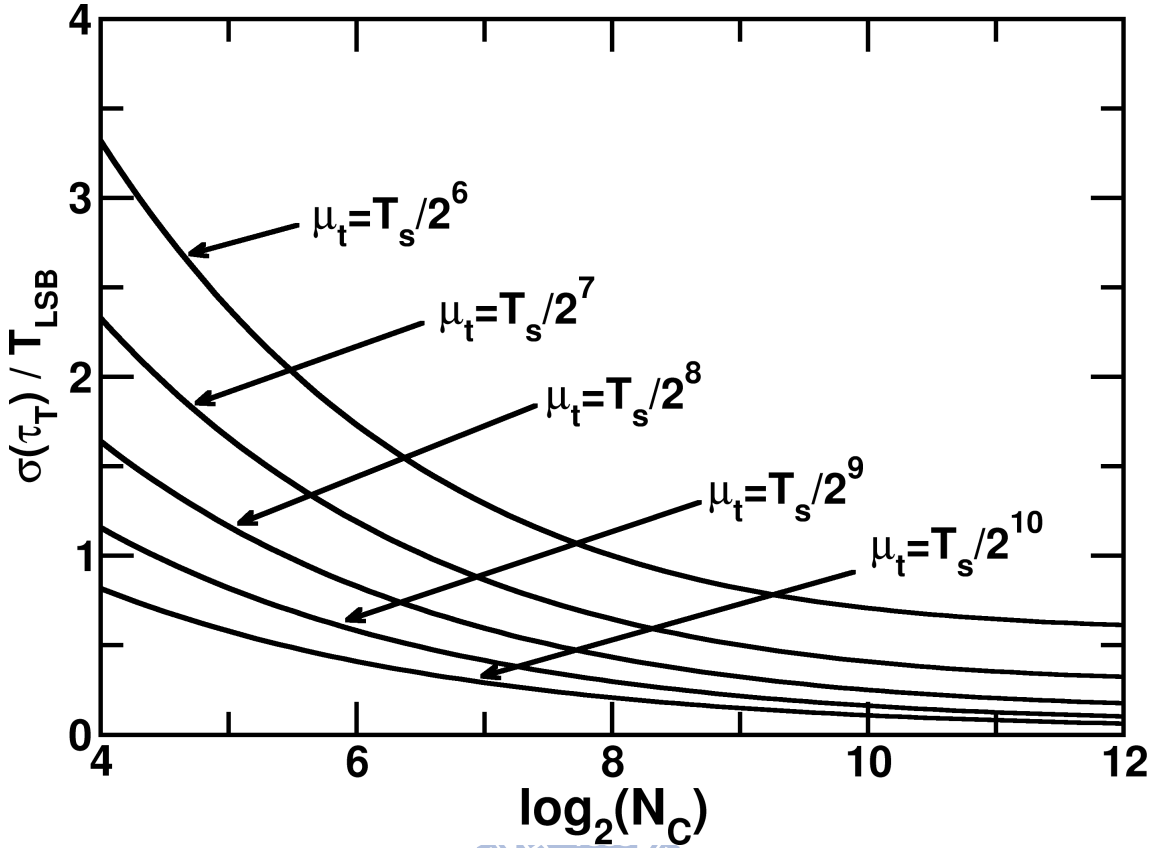
Figure 4.6: Timing fluctuation, $\sigma(\tau)$, versus N_C and μ_t for the TI ADC example.

In Figure 4.5, each A/D channel includes a $s(t)$ sampler and a $x(t)$ sampler to enable the robust background timing-skew calibration. The two samplers driven by the same clock must have the same sampling instant. To minimize mismatch, the two samplers should be placed in close proximity in the chip layout. The signal routes of $s(t)$ and $x(t)$ may also have to be matched. Furthermore, the clock edges that define the sampling instants should be made as steep as necessary.

For timing-skew calibration, the narrow-band $x(t)$ reference has a center frequency at $f_i \approx 0.25 f_c$, which meets the low-f_i scenario described in Section 3.3. From (A.67), the $x(t)$ reference has a ZC density of $Z_R = 2f_i \approx 0.5 f_c$. The resulting timing fluctuation variance averaged over the 8-phase clocks, $\sigma^2(\tau_T)$, can be calculated using Equation (4.6). Figure 4.6 shows the relationship between $\sigma(\tau_T)$ and N_C at various μ_t values. For this 6-bit ADC example, $\mu_t = T_s/2^8$ and $N_C = 2^{10}$ are chosen to achieve $\sigma(\tau_T) = 0.26 \, T_{LSB}$.
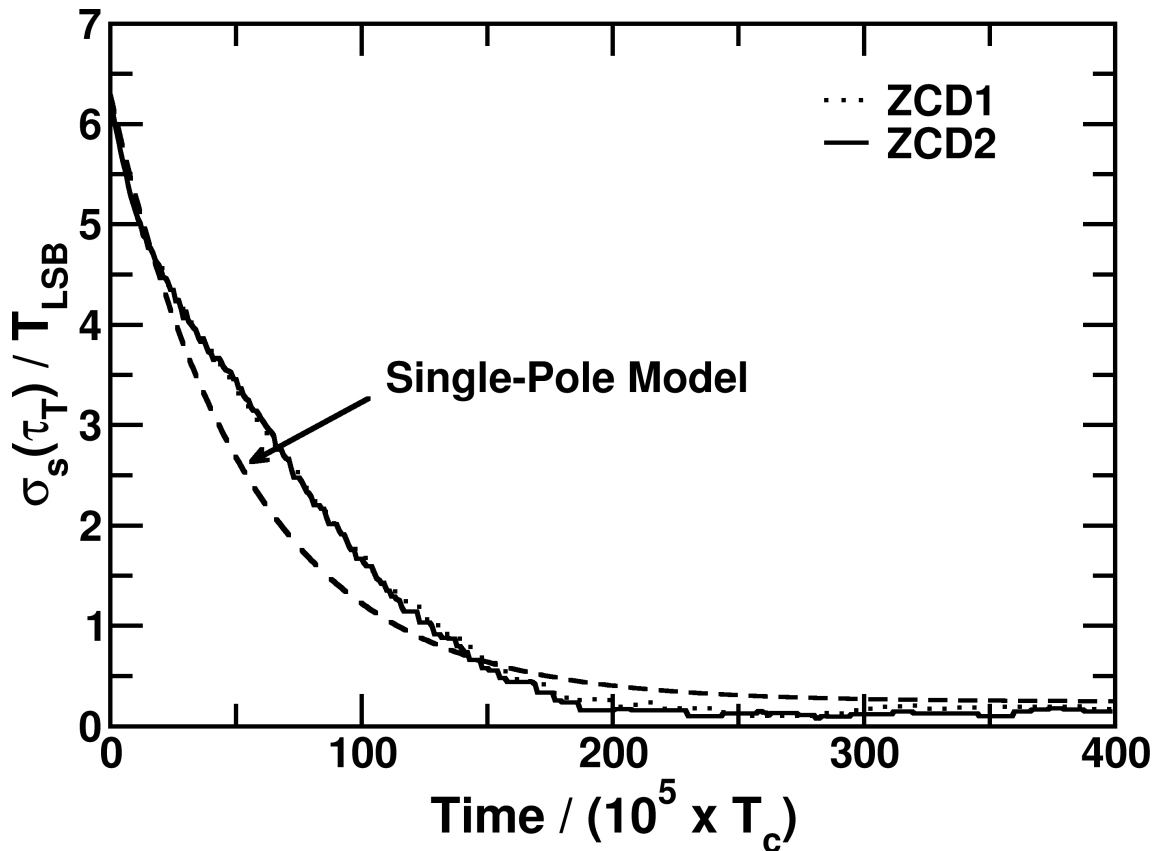
Figure 4.7: Settling behavior of $\sigma_s(\tau_T)$. The comparators in ZCD1 and ZCD2 are ideal.
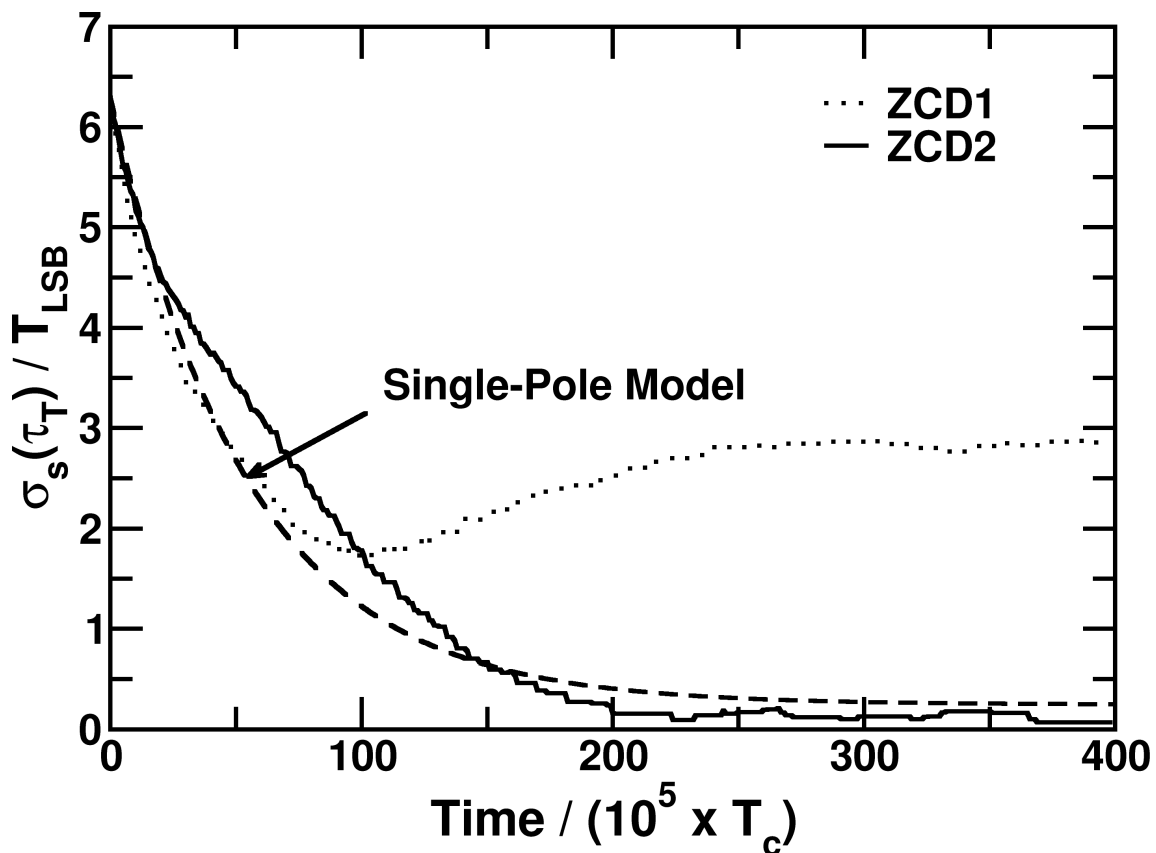
Figure 4.8: Settling behavior of $\sigma_s(\tau_T)$. The comparators in ZCD1 and ZCD2 have ran-

The behavior of this TI ADC is simulated using a C program. To illustrate that the proposed calibration scheme does not require a well-defined sinwave, the $x(t)$ reference used in the simulation is a full-swing phase-modulated sinwave

$$x(t) = \sin\left[2\pi f_i t + 0.1\sin(2\pi f_m t)\right] \tag{4.7}$$

where $f_i \approx 0.25 f_c$ and $f_m \approx 0.14 f_c$. Both the ZCD1 and the ZCD2 described in Section 3.3 are tested. Figure 4.7 shows the settling behavior of the ADC's timing-skew spatial standard deviation, $\sigma_s(\tau_T)$. For this figure, ideal comparators without offsets are deployed in the ZC detectors. Note that $\sigma_s(\tau_T)$ is the standard deviation of the $(\tau_1, \tau_2, \cdots, \tau_8)$ data set at a given time. For $1 \leq j \leq 8$, τ_j is the timing offset of the ϕ_j clock. A random number generator selects the initial value of τ_j. The $\sigma_s(\tau_T)$ is 6.3 T_{LSB} before calibration, and settles toward 0.22 T_{LSB} as calibration progressing. The 0.22 T_{LSB} value is obtained by averaging $\sigma_s(\tau_T)$ over a period from $250 \times 10^5 \times T_c$ to $400 \times 10^5 \times T_c$. Without comparator offsets, ZCD1 and ZCD2 exhibit similar behavior. Also shown in the figure is the transient response of a single-pole model with a time constant $\tau_c = 41.9 \times 10^5 T_c$, which is calculated from Equation (A.66). Figure 4.8 shows the effect of comparators' offsets. Random offsets generated from a random number generator are added to the comparators in ZCD1 and ZCD2. The standard deviation of the offsets is $\sigma(V_{OS}) = 3 V_{\mathrm{LSB}}$. For the calibration using ZCD1, the $\sigma_s(\tau_T)$ can only settle to 2.86 T_{LSB}. On the other hand, the $\sigma_s(\tau_T)$ can settle to 0.21 T_{LSB} by using ZCD2. The comparators' offsets have little effect on ZCD2. Note that the $\sigma_s(\tau_T)$ performance from simulations is better than the prediction of Equation (4.6). The timing fluctuation theory described in Appendix A.3 is derived from random process, which assumes a scenario more random than those used in the simulations.

Chapter 5

A 6-Bit 16 GS/s Time-Interleaved Flash ADC

5.1   Introduction

A 65nm 435-mW 6-bit 16-GS/s time-interleaved flash ADC was presented in this chapter. The calibration technique in previous chapter has been applied on this ADC. The circuit architectre and measurement results are shown in the follow sections. A simple logic calibration processor minimizes the timing skew error. Besides, a background offset calibrated comparator has been applied on sub-channel ADC. With the proposed calibration technique, the ADC can achieve ERBW 3GHz. At the frequency near ERBW, the SND is improved from 19.8dB to 28.0dB by timing skew calibration.

5.2   Time-Interleaved ADC Architecture

The ADC block diagram is shown in Figure 5.1. It consists of 8 time-interleaved identical A/D channels, ADC_1 to ADC_8. The A/D channels are driven respectivelly by 8 different clock with equally-spaced phase, ϕ_1 to ϕ_8. The clocks are generated from an on-chip delay-locked loop(DLL). The DLL can get better noise performance since there is no jitter accumulation in the loop. The ADC analog input is $s(t)$. It is sequentially sampled and digitized by each A/D channel to produce a 6-bit digital stream. The flash typed ADC
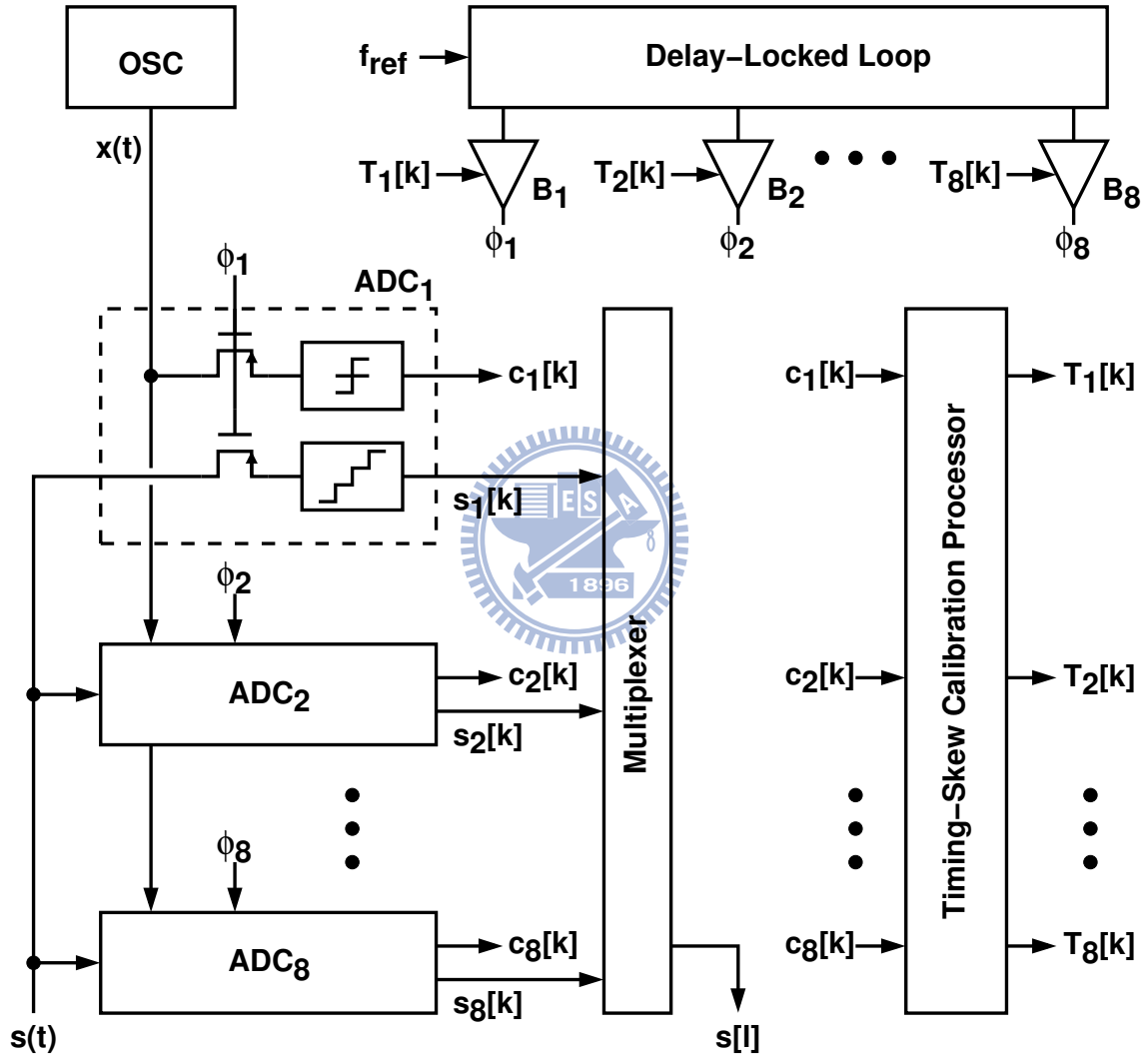
Figure 5.1: Time-interleaved ADC block diagram.
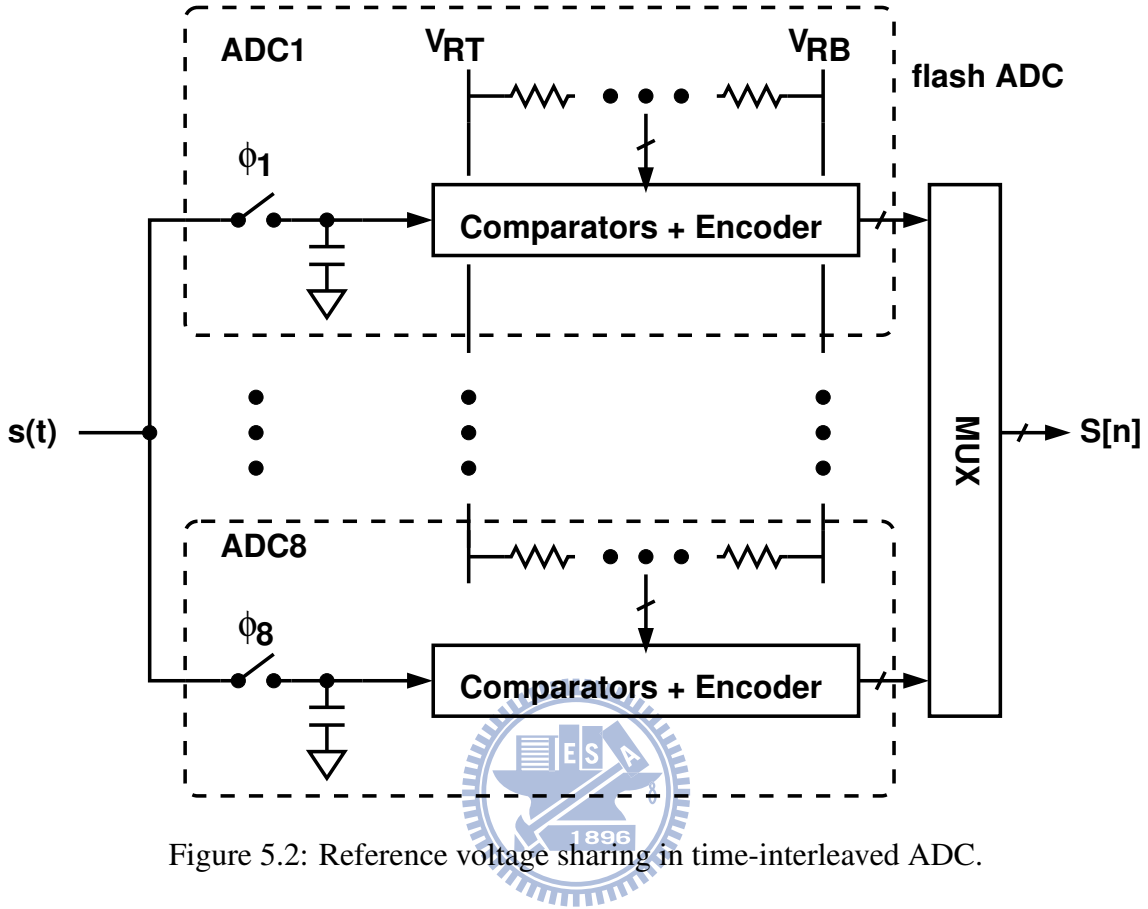
Figure 5.2: Reference voltage sharing in time-interleaved ADC.

has been adopt for high speed single channel A/D. The clock of each phase frequency is f_c. The digital streams from the 8 A/D channels, $s_1[k]$ to $s_8[k]$, are then multiplexed to generate the final ADC digital output, $s[l]$. The ADC equivalent sampling rate is $8 \times f_c$.

For a time-interleaved ADC in this thesis, the reference voltage of flash ADC has been shared for minimization of gain errors shown in Figure 5.2. Besides, the background comparator's offset calibration technique [15] has been applied on the flash ADC. Therefore, the offset of single channel ADC will be calibrated to zero, thus the offset among each A/D channel can be neglected. Therefore, the time-interleaved suffered the timing skew error significantly.

To minimize the mismatches among sampling intervals. In a high speed design, the sampling intervals are sensitvie to mismatches among clock driver and clock routes. In Figure 5.1, the delays of clock drivers, B_1 to B_8, can be independently adjusted by the digital control signals, T_1 to T_8. The resolution for the delay control is 0.4psec. The
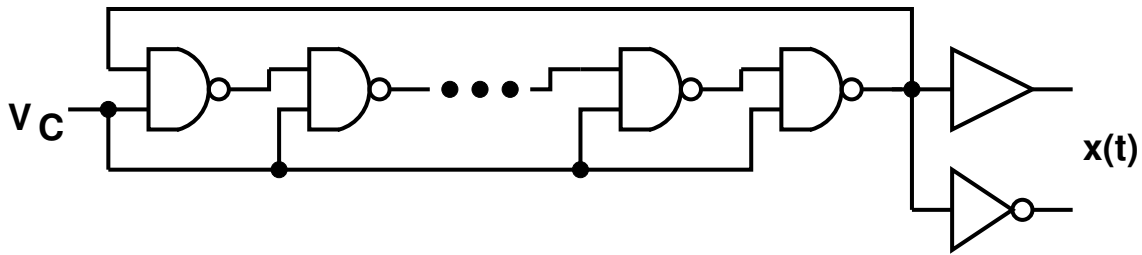
Figure 5.3: Simple ring oscillator in time-interleaved ADC.

control signals are generated from an on-chip timing-skew calibration processor (TSCP). An on-chip oscillator generates a testing signal $x(t)$. It is sampled and quantized in each A/D channel to produce 8 1-bit digital streams, $c_1[k]$ to $c_8[k]$. From those digital streams, the TSCP continuous counts the zero-crossing (ZC) occurences in every sampling interval as described in Chapter 4. In each A/D channel, the $x(t)$ signal path consists of only a replica sampler and a comparator, and is separated from the $s(t)$ signal path, which is the same as described in Chapter 4. The $x(t)$ is generator is a simplie ring oscillator which shown in Figure 5.3 free running about 400MHz with controlled voltage 1.2V, the frequency range is from 200MHz to 400MHz. This frequency is suitable for timing skew calibration since it is not very large, thus avoiding large coupling effect. It is also large enough to gain the timing information for timing skew calibration. In this system, we can also modulate the control voltage of oscillator to avoid the clock source is synchronous to reference signal. By analysis of $x(t)$ from TSCP, the optimized digital code T_1 to T_8 have been applied on the clock drivers to minimized the timing skew error. For saving power consumption, the downsampling clock $f_c/64$ has been applied in TSCP.

5.3   Circuit Implementation

5.3.1   Delay-Locked Loop

The delay-locked loop (DLL) shown in Figure 5.4, the input clock propagates into delay cell. With replica delay cell the phase detector judges the lead or lag of output phase compared with input phase, then generates the up or down pulse to control charge pump and the controlled voltage of delay cell[25][20][4][26][1]. With the negative feedback of
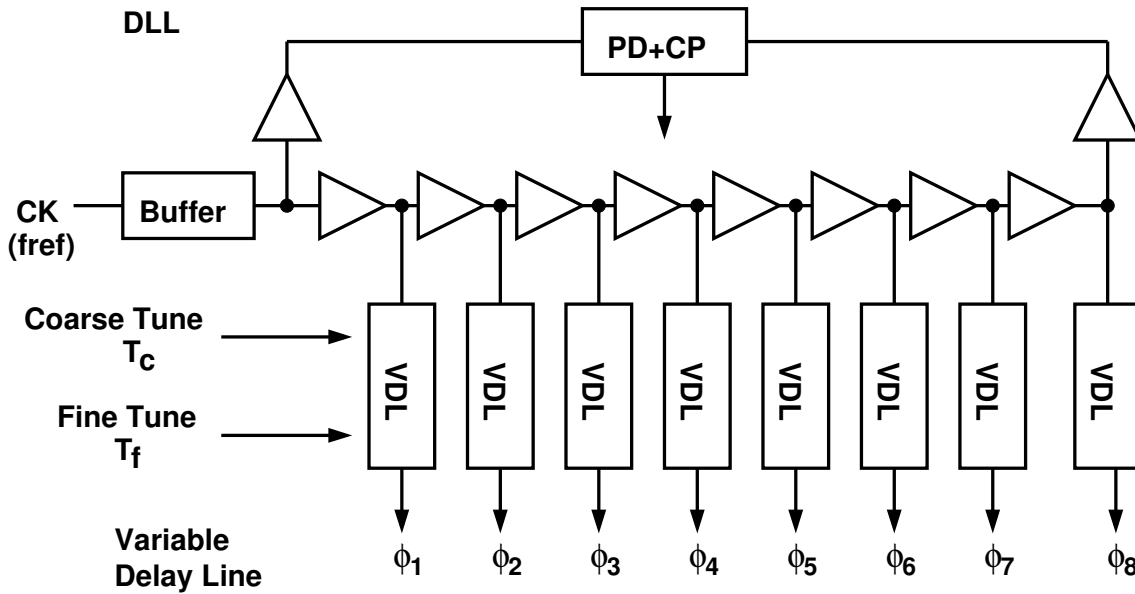
Figure 5.4: Delay-locked loop.

delay locked system, the output phase will be lag 360° from input phase, and the each phase ϕ_1 to ϕ_8 gets equally spacing. However, the dead lock occurs when the wide range delay cell has been applied. In this work, the clock rate is about 2GHz. Therefore, we can design the power on sequence on controlled voltage of DLL. When power goes to high, the controlled voltage has been tied to high, and then turn off the tie high switch and lets the DLL lock the controlled voltage.

Shown in Figure 5.5 is delay cell, the signal "pc" turn on after power ready, forces the fast dealy in the delay cell. Then the "pc" turn off and the DLL controls the voltage V_{cn} by itself. The MBN, MBP degenerate the speed of MP, MN for the required operating frequecny (2GHz), the MTN,MTP lowering the effect of MBN and MBP for low gain delay cell. The differential-to-single circuit converts the non-full-swing signal to the full swing, and passes to the variable delay line (VDL) shown in Figure 5.6. The digital-delay-controlled cell can be taken as clock buffer. Since the clock buffer is needed in each single A/D, the VDL can easily be embedded in the clock buffer of A/D. The simulated delay step in Figure 5.7 of VDL is about 0.4psec. The small jump of transfer function of VDL can not affect the proposed calibration scheme since the calibration scheme requirs only global monotoncity.
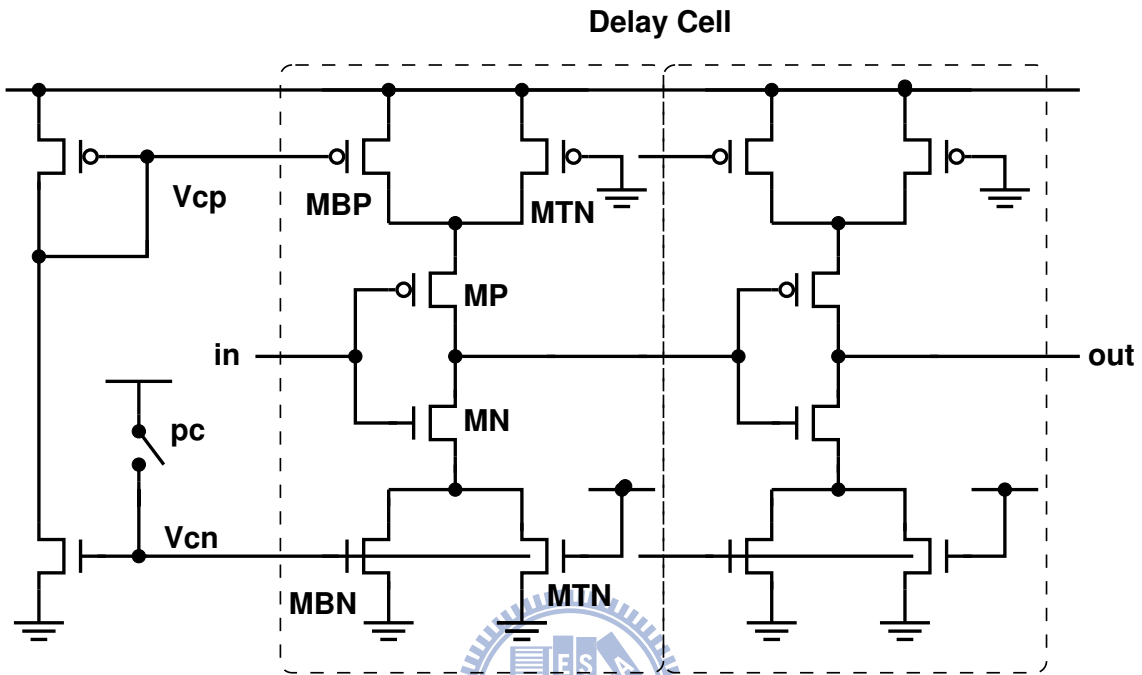
Delay Cell

Figure 5.5: Delay Cell.
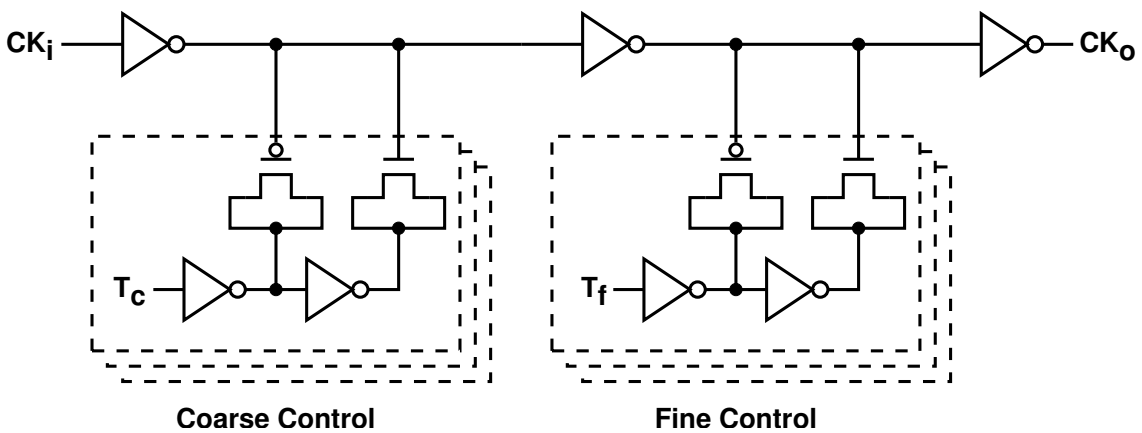
Figure 5.6: Digital controlled delay cell.
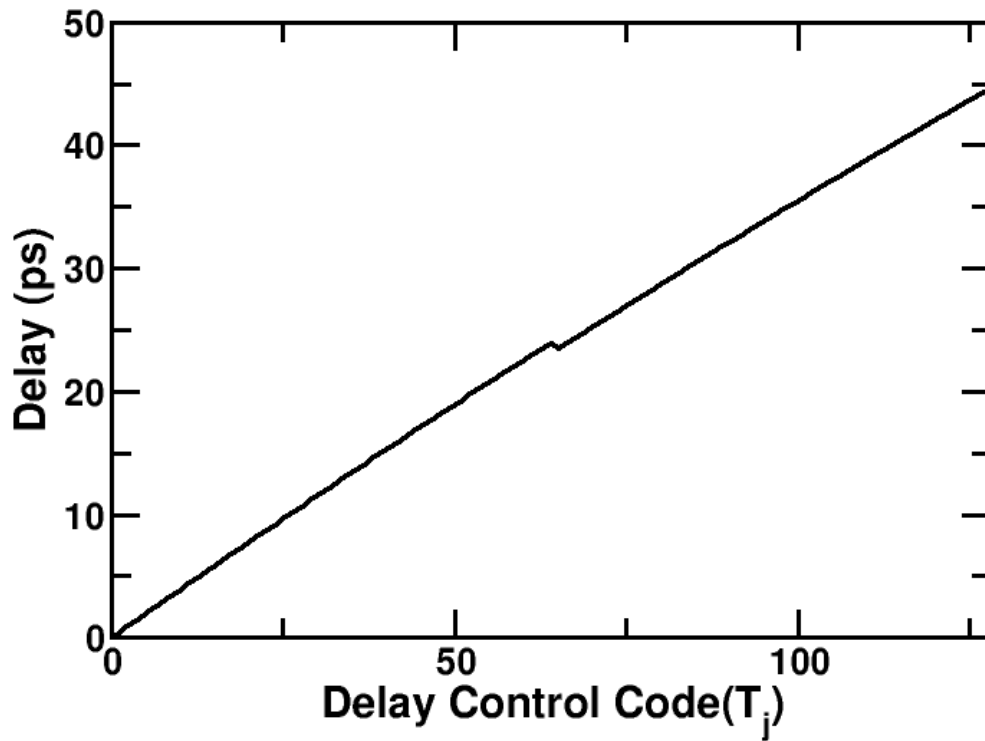
Figure 5.7: Transfer funtion of VDL.
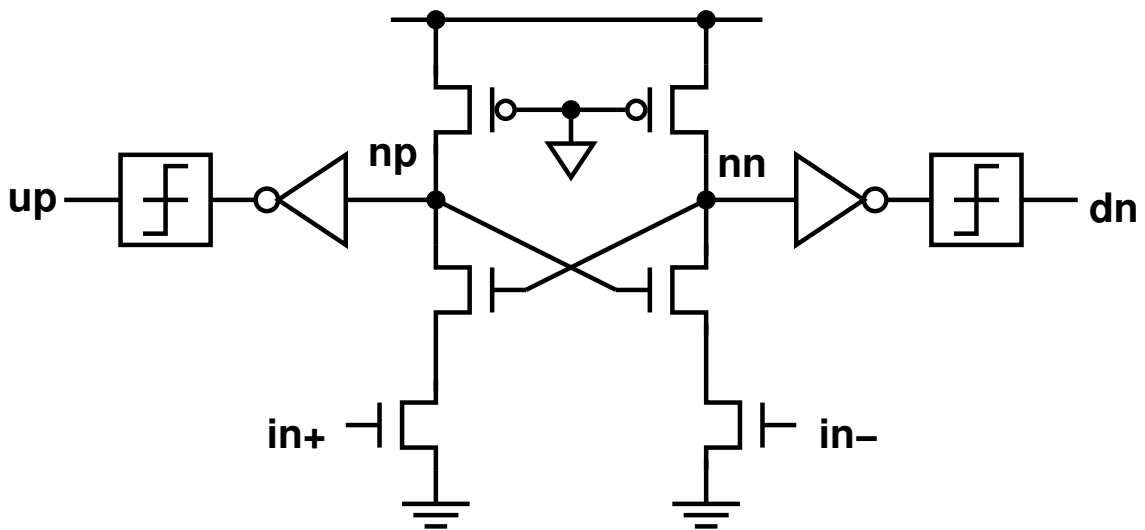
Figure 5.8: Phase detector of DLL.
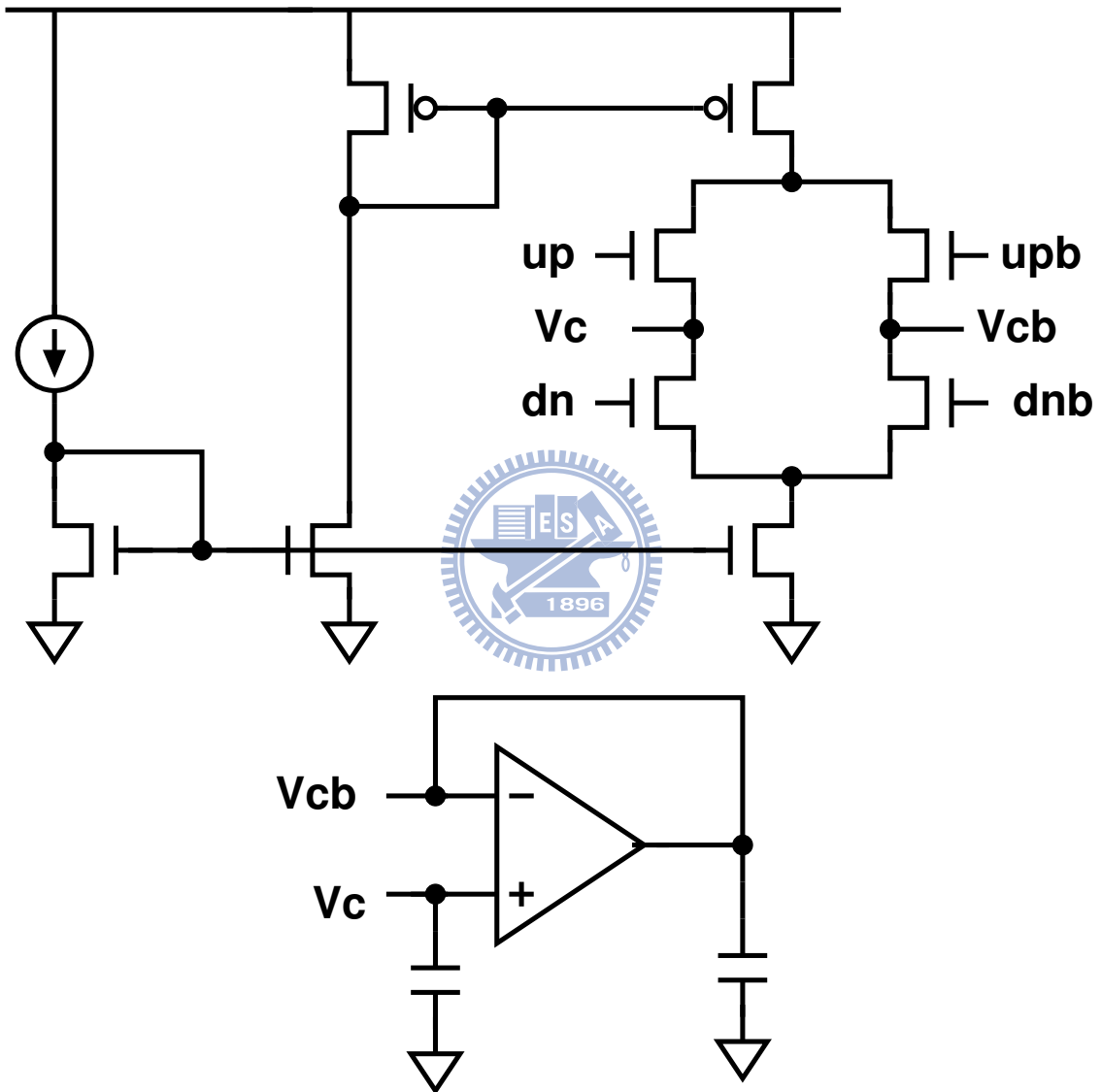
Figure 5.9: Charge pump of DLL.
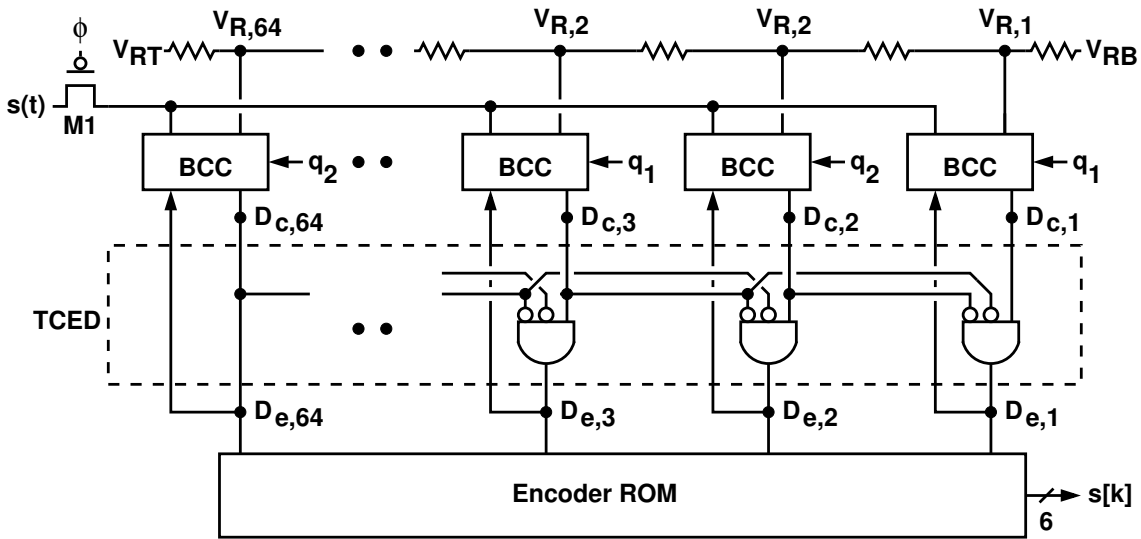
Figure 5.10: Single channel flash ADC.

The phase detector (PD) has been implemented by the arbiter architecture as shown in Figure 5.8. The input clock and output clock of DLL are applied on the input differnetial pair of PD. When the input and output clock is low, the gate tied ground PMOS will tie the node np and nn to VDD, thus makes the NMOS with largest Vds for maximum transconductance. When the lead phase comes, the postive feedback of NMOS will latch the node np and nn, then the following digital latch will generate the signal up, dn for the charge pump as shown in Figure 5.9. The up/dn signal turn on or turn off the switch, charges or discharges the controlled voltage Vc for delay cell. When up phase is active and dn phase is deactive, the current source of NMOS will be turned off, this makes the jitter be larger since dn need more time to active the NMOS current source. Therefore, the replica with inverted phsae of up/dn path makes the current sources always turn on, the OP buffer makes Vcb is the same Vc, thus keeps the balance of charge pump system. Finally, the bandwidth of DLL is about 5MHz to filter the noise from delay cell.

5.3.2 Flash ADC

Figure 5.10 shows the block diagram of a single flash A/D channel. It consists 64 background-calibrated comparators (BCC) [15]. Prceeding the comparators is a p-channel MOSFET M1 that functions as a sample-and-hold for the ADC. The comparators' output are con-
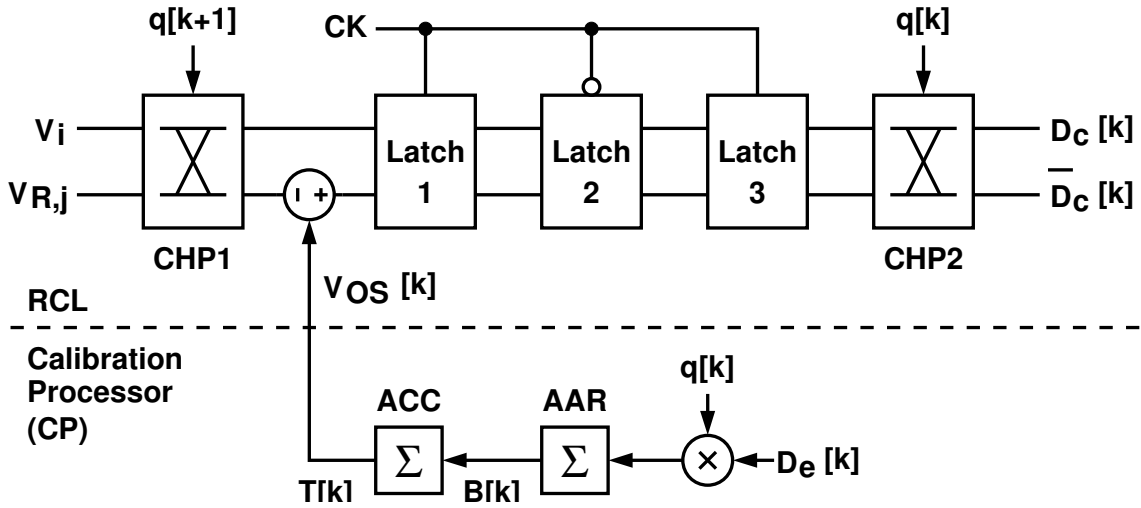
Figure 5.11: Background calibrated comparator (BCC).

nected to a thermometer-code edge detector (TCED), which is an array of 3-input AND gates. In normal operation, only on of the TCED outputs is active under low comparators' offset, and it indicates the location of the 1 to 0 transition in the input thermometer code. The TCED is the address decoder ofr the encoder ROM that genertaes the ADC output, $s[k]$. The TCED output, $D_{c,1}$ to $D_{c,64}$, is also used by the corresponding BCC for the offset calibration. A binary pseudo random sequence q_1 is applied to the odd-number BCCs, and uncorrelated random sequence q_2 is applied to the even-number BCCs. The uncorrelated random sequences can avoid the interlocking of calibration procedures that may occur between the neighboring BCCs.

Figure 5.11 shows the BCC block diagram. It consists of a random-chopping latch (RCL) and a digital calibration processor (CP). In the RCL, the two choppers CHP1 and CHP2 are ontrolled by a binary random sequence $q[k]$. The comparator is a 3 stages, cascaded latches to minimize the meta-stability effect. The pseudo random sequence changes the comparators' offset by the sequence, thus the offset has been spreaded in frequency domain by $q[k]$ by CHP1. CHP2 de-spreads the spreaded signal, $D_c[k]$ for ADC encoder. The $D_e[k]$ generated by TCED and $D_c[k]$, is the spreaded siganl, but the offeset of comparator still keeps a DC value, thus we can apply the accumulate-and-reset (AAR) to extract the offset polarity. AAR accumulates $D_e[k] \times q[k]$, and detects if the accumulated result reaches $+16$ or -16, the $B[k] = +1$ or $B[k] = -1$ when the accumulated result is
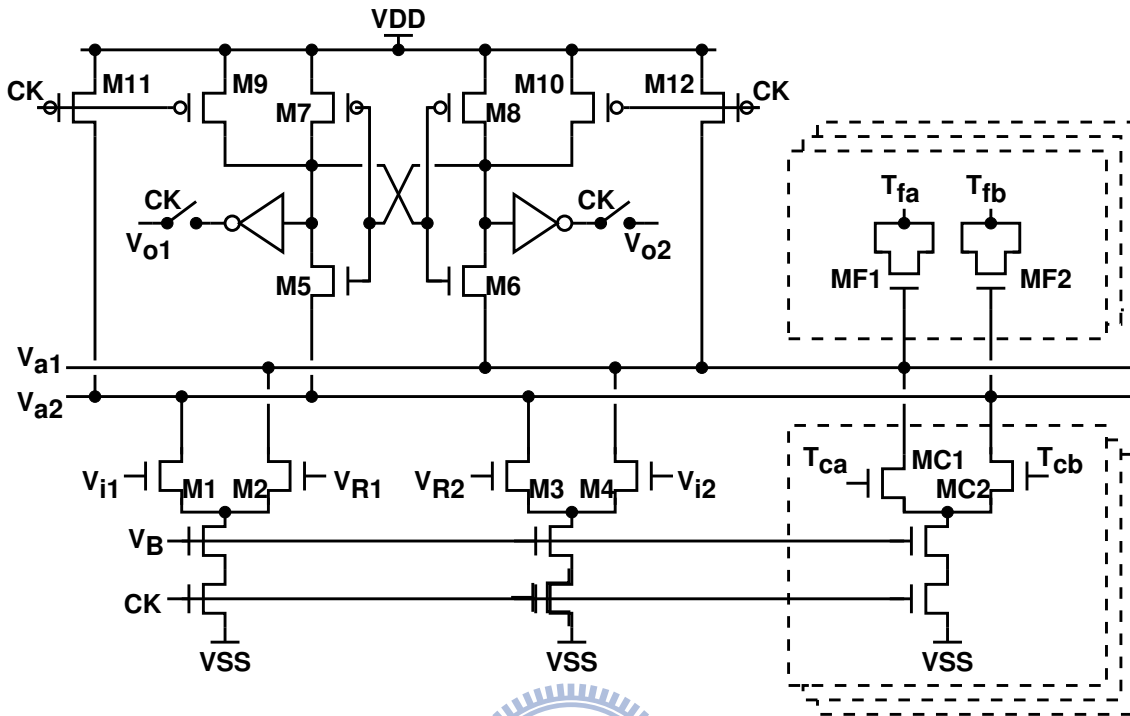
Figure 5.12: Latch schematic.

+16 or −16, then reset its content for removing memory effect. The offset can be adjust by $T[k]$, which is accumulated from $B[k]$ by accumulator (ACC).

The first stage of latch in comparator shown in Figure 5.12. The clock signal CK enable the bias current to improve the PSRR. The four input differential pairs amplify the signal and then the back-to-back inverter latches the output. The phase $CK = 0$ pulls up the V_{a1} and V_{a2} to VDD to enlarge the Vds of NMOS for large transconductance, thus minimizes the offset. For the offset adjustment, the coarse adjustment is provided by tge cyrrent switch, MC1 and MC2. The fine adjustment is provided by the capacitor pai, MF1 and MF2. The possible values for both digital control signal pairs, (T_{ca}, T_{cb} and T_{fa}, T_{fb} are $(0, 0)$, $(0, 1)$, $(1, 0)$. There are 4 identical current switches, providing a total of 9 offset coarse step, and each step is 32mV. The fine step is generated by 16 identical capacitor pairs, providing a total of 33 fine offset steps, and each step is 3.2mV.

The comparators' offset have been calibrated by coarse tune during the power-on state, then the background calibration controls only fine offset. Noted that the timing skew calibration is independent of the offset calibration since the TSCP takes the signal of $x(t)$
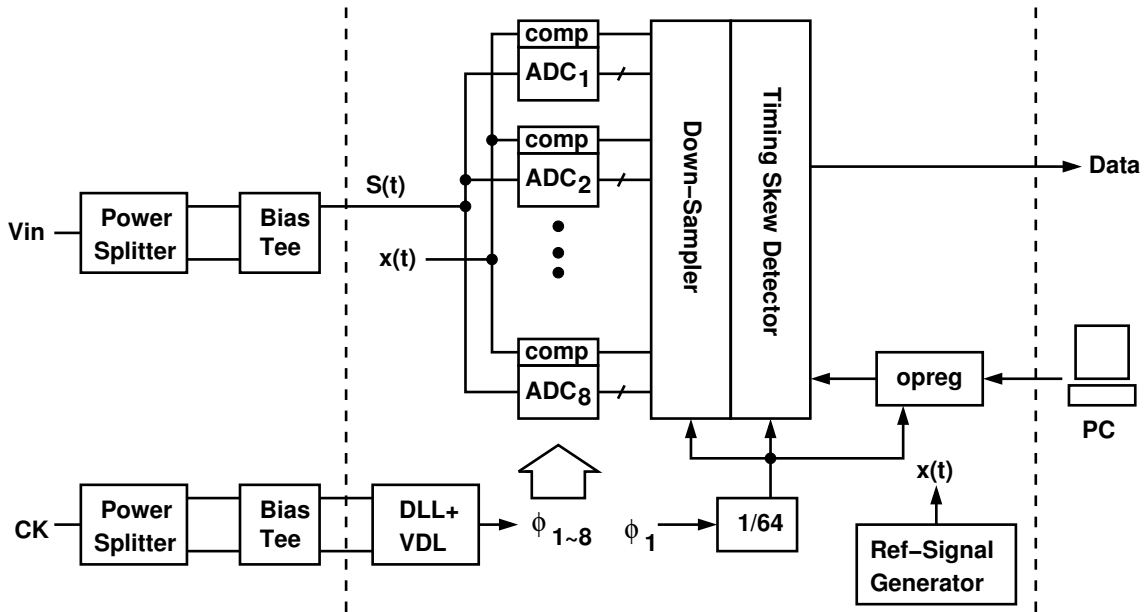
Figure 5.13: Testing enviornment of time-interleaved ADC.

for calibration.
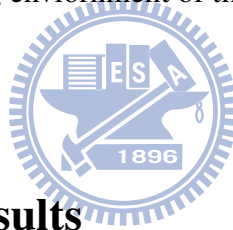
5.4 Measurement Results

The testing setup is shown in Figure 5.13. The Analog input is generated by HP 8648C and the clk source is generated by Agilent E4438C. To ensure the signal quality of the analog source, the output of 8648C passes by a power splitter and bias-Tee to achieve single-to-differential conversion. The clk source generates sinesoide waveform and its frequency is f_c. The opreg in chip controlled by PC print-port, sets the option register in the ADC to adjust the function of ADC.

The ADC chip was fabricated using 65nm CMOS technoloy, where Figure 5.14 shows its micrograph. The active area is $0.93 \times 1.58\text{mm}^2$. The supply voltage is 1.5V. The operating frequency is $f_c = 2GHz$, with 16GS/s equivalent sampling rate, the ADC consmes 435mW of power, excluding I/O. Each A/D channel consumes 54mW. The chip is mounted directly on a circuit board. The original ADC digital output down-sampled to 1/64.125 of f_c frequency when delivered off-chip.

Figure 5.15 shows the measured DNL and INL for a single channel ADC. Before
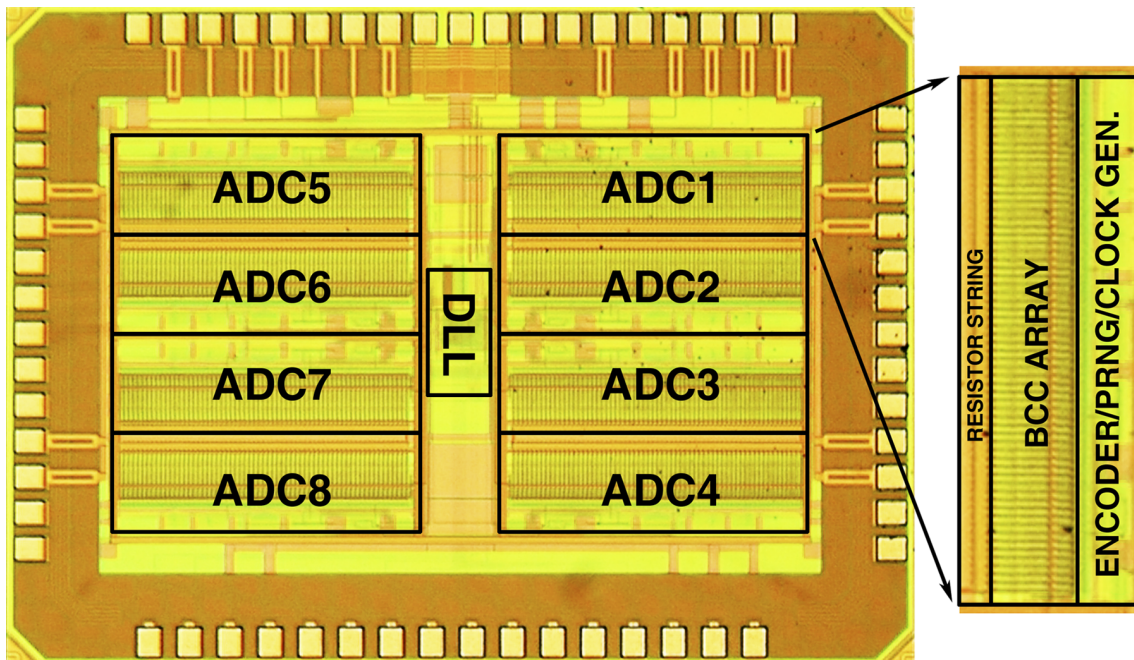
Figure 5.14: Diephoto of ADC.

activation the calibration, the DNL is -1.0/+4.9 LSB and the INL is -4.3/+5.4 LSB. There are missing codes. After activating the offset calibration, the DNL becomes -0.5/+0.6 LSB and the INL is reduced to -0.4/+0.7 LSB.

Figure 5.16 shows the measured output spectrum, where the input freqeucny is about 3GHz. Without timing skew calibration, the maximum distortion tone is about -28dB, which shows that timing skew error actuely degrades the overall performance. However, with timing skew calibration, the distortion tone from timing skew error has been suppressed to -49dB, and samplle-and-hold switches dominante the 2nd, 3rd, and more high order distortion tones.

Figure 5.18 shows the measured SNDR versus input frequency for the time-interleaved ADC. The equivalent sampling rate is 16GS/s. The effective resolution bandwidth (ERBW) is 3GHz, which is limited by the bandwidth of the sample-and-hold switches. At the frequency near ERBW, the SNDR is improved from 19.8dB to 28.0dB by the timing skew calibration. Figure 5.19 shows the measured SNDR versus sampling frequency, where the input signal frequency is 61MHz. The figure-of-merit (FOM), defined as power/($2^{\mathrm{ENOB}} \times 2 \times$ ERBW for this ADC is 2.6pJ/conversion-step. If the sampling rate is
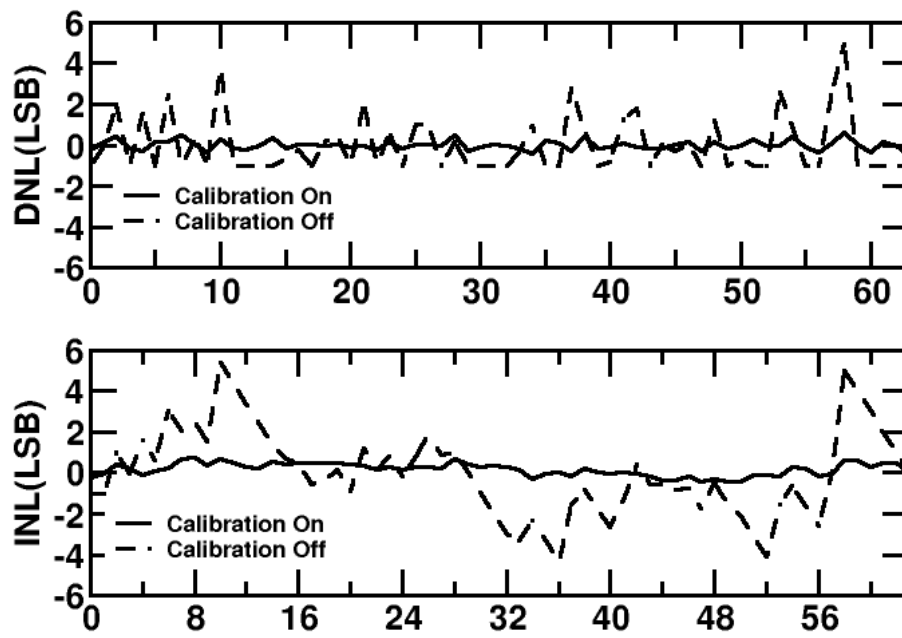
Figure 5.15: Measured DNL and INL of a single A/D channel.
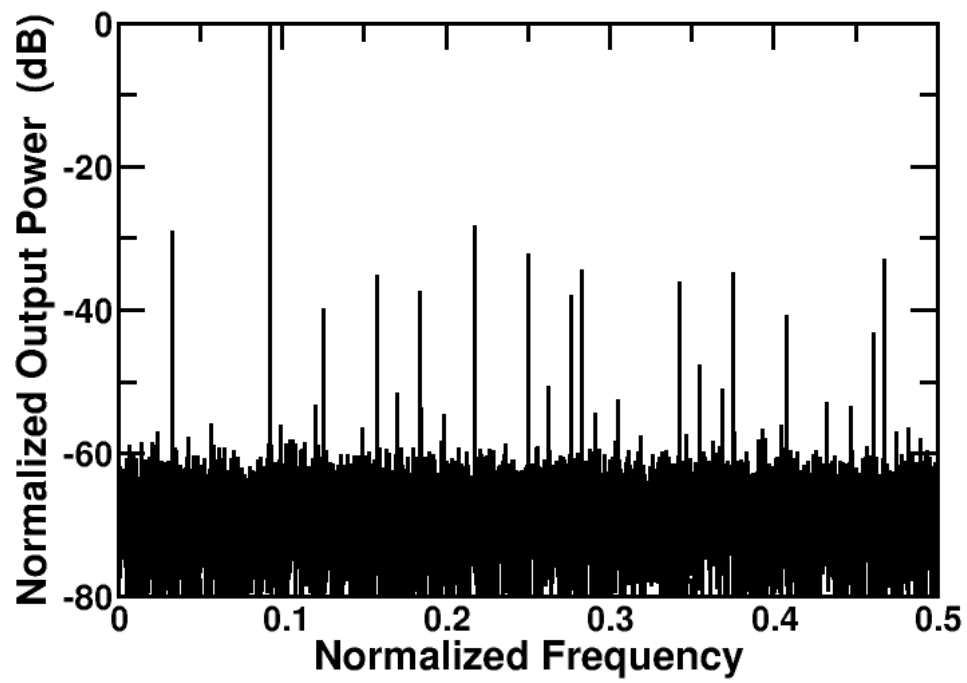
Figure 5.16: Measured specturm without timing skew calibration, where the input frequency is about 3GHz.
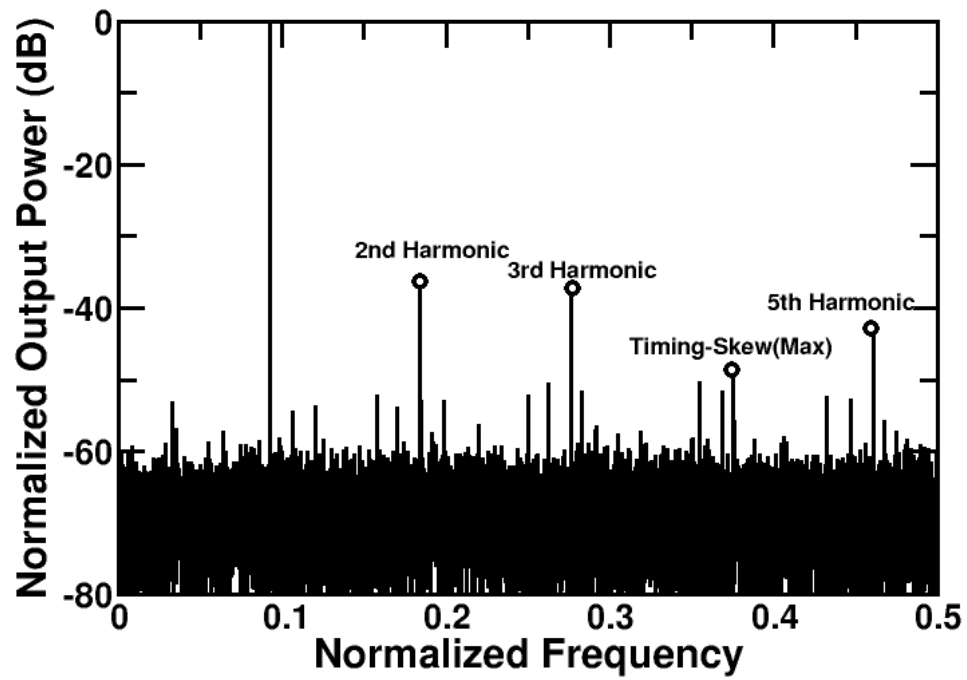
Figure 5.17: Measured specturm with timing skew calibration, where the input frequency is about 3GHz.
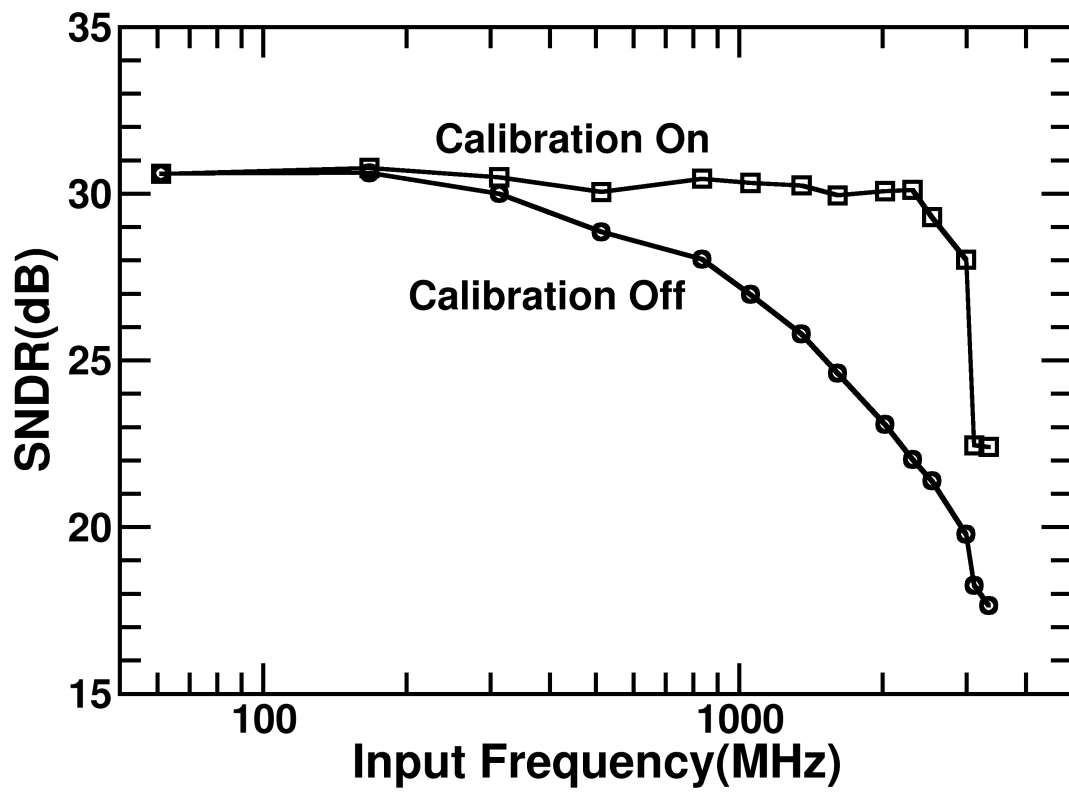
Figure 5.18: Measured SNDR versus input frequency.
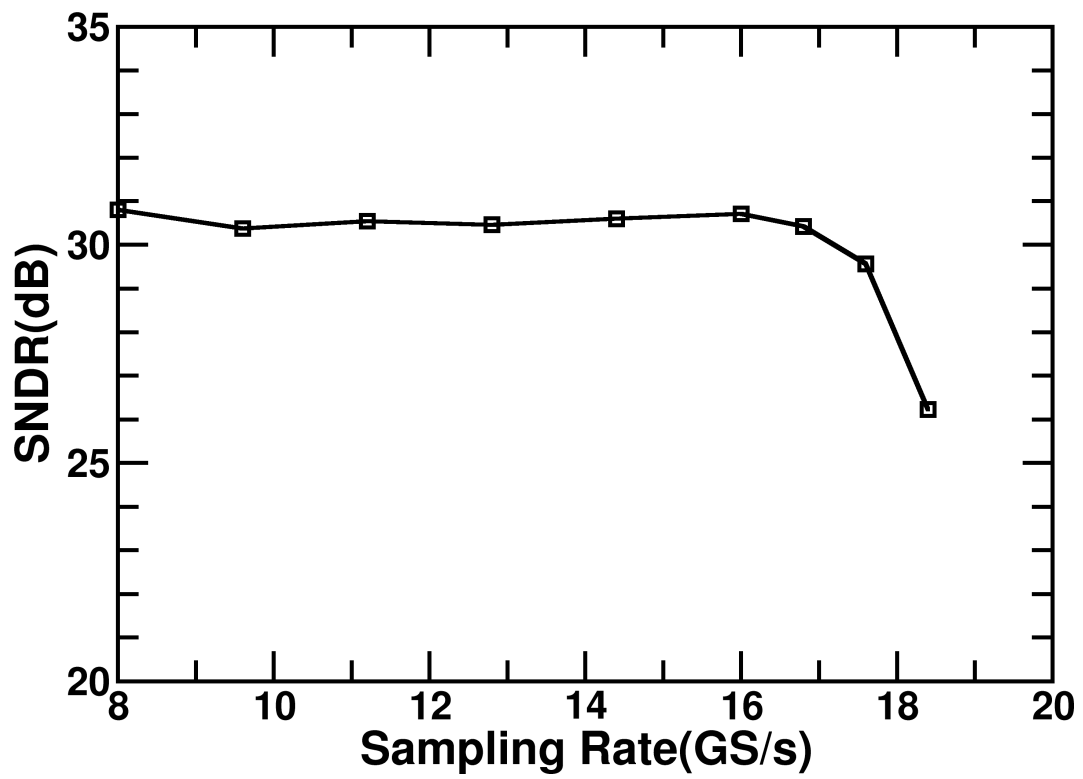
Figure 5.19: Measured SNDR versus sampling frequency. The input signal frequency is 61MHz.

Year	This Work	V'09[27]	I'08[28]	I'06[29]	I'04[30]	I'03[31]
Technology (nm)	65	90	90	180	180	180
Supply (V)	1.5	1.2	1.0	1.8	1.8	NA
Power (mW)	435	1600	1200	619	900	9000
F_s (GHz)	16	10.3	24	4	1.65	20
ERBW (GHz)	3	3.9	6	0.8	0.9	2
ENOB (bit@DC)	4.9	5.6	5	3.8	3	6
FOM (pJ/Step)	2.6	4.23	3.13	27.7	2.76	11.7

Table 5.1: Benchmark of very high speed ADCs.

reduced to 12GS/s, with ERBW=3GHz, the ADC FOM becomes 2.0pJ/conversion-step.

The following table is the benchmark between each very high speed ADCs. The self-calibration is always on, which can overcome the variation due to temperature.

5.5 Summary

A 435-mW 6-bit 16-GS/s time-interleaved ADC was fabricated using 65 nm CMOS technology. The ADC demonstrates a new timing skew calibration technique, which corrects timing skew error among each channel. The calibration technique is robust and immune to device mismatches. The timing skew calibration uses only simple counter and logic, which lowering the hardware complexity and power. In this work, the SNDR at 3GHz has been improved from 19.8dB to 28.0dB by the timing skew calibration and the the FOM is 2.6pJ/conversion-step. The distortion harmonic tones due to timing skew has been improved from -28dB to -49dB.

Chapter 6

Conclusions and Future Works

6.1 Conclusions

Time-interleaved architecture can increase the sampling rate by increase the number of channels. The timing skew among each A/D channel limits the overall performance when the sampling rate is around GHz order. The proposed timing-skew calibration technique described in this thesis is based on zero-crossing (ZC) detection. Although the ZC detection is a nonlinear operation, the ZC probability is related to the cross-correlation of the calibration reference. We have made theoretical study on the ZC detection principle and proved its robustness. The ZCD2 with digital high-pass filters provides a detection technique that is less sensitive to comparators' offsets. With proper reference input, the ZC detectors can be used to measure the phase spacing among multi-phase clocks. The ZC probability is proportional to the phase spacing. Based on this fact, we propose a digital calibration processor (CP). It receives outputs from the ZC detectors and adjusts the delays of clock buffers to equalize the phase spacings between adjacent clock pairs. We have also analyzed the CP's behaviors, including converging speed and timing fluctuation.

Although the proposed calibration scheme needs an extra reference signal, the requirement for this reference is loose. The reference does not need to have an accurate frequency or an exact waveform shape. It can be easily generated on a chip using simple circuitry. Most of the calibration procedures are performed in the digital domain, and require only adders and registers. An 8-channel 6-bit 16GS/s time-interleaved ADC has been demon-

strated with the proposed calibration technique. The SNDR is improved from 19.8dB to 28.0dB by the proposed TSCP. The distortion harmonic tones due to timing skew has been improved from -28dB to -49dB.

6.2   Recommendations for Future Investigation

This section presents several suggestions for future investigations in high performance time-interleaved ADC design.

- The delay locked loop does not accumulate jitter, thus gets the better noise performance than PLL. However the clean, high speed clock source is hard to generate. L-C tank oscillator can achieve higher noise performance, but the power consumption and area is large. The high speed and low noise clock generator is an important issue on high speed time-interleaved ADC design.

- The timing skew calibration processor requires a reference signal to get the timing information. [14] shows the timing skew calibration without reference signal, but the clock chopper is hard to generate in high speed circuit design. Therefore, a flexible modulation technique on input signal for detection of timing skew is an interesting topic.

- A high speed with high linearity sample-and-hold (SHA) or track-and-hold (THA) circuit is another important topic. In the very high speed application, linearity degrades acutely when operating at high frequency. In the deep sub-micron technology, low supply voltage is used to prevent the high-voltage stress on the thin gate oxide, thus the linearity of SHA or THA is more harder to achieve since the bias circuit is hard to mantain for large input voltage swing.

Appendix A

Appendix

A.1 Mathematical Analysis of ZCD1

Figure A.1 shows a ZCD1 whose two comparators exhibit O_j and O_{j+1} offsets respectively. The $x_j[k]$ and $x_{j+1}[k]$ are two $x(t)$ sampling sequences corresponding to the ϕ_j and ϕ_{j+1} sampling clocks respectively. Let $x(t)$ be a stationary Gaussian process with zero mean. Then $x_j[k]$ and $x_{j+1}[k]$ form a bivariate normal distribution. Its probability density function is [22, 23]

$$p_b = \frac{\exp\left[-\gamma/[2(1-\rho_{j,j+1}^2)]\right]}{2\pi\sqrt{1-\rho_{j,j+1}^2} \times \sigma_j\sigma_{j+1}} \tag{A.1}$$
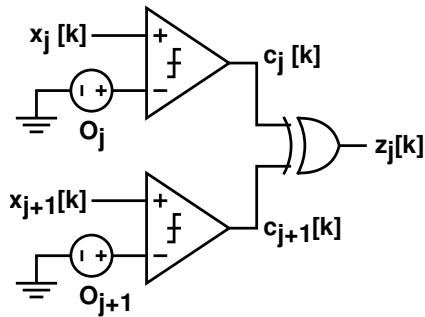
Figure A.1: ZCD1 with comparators' offsets.

with

$$\gamma = \frac{x_j^2}{\sigma_j^2} + \frac{x_{j+1}^2}{\sigma_{j+1}^2} - \frac{2\rho_{j,j+1} \cdot x_j x_{j+1}}{\sigma_j \sigma_{j+1}} \tag{A.2}$$

where σ_j and σ_{j+1} are standard deviations as defined in Equation (3.7) and $\rho_{j,j+1}$ the cross correlation between $x_j[k]$ and $x_{j+1}[k]$ as defined in Equation (A.59).

In Figure A.1, the comparators' outputs, $c_j[k]$ and $c_{j+1}[k]$, are determined by the $x_j[k] - O_j$ polarity and $x_{j+1}[k] - O_{j+1}$ polarity respectively. The $z_j[k]$ output is 1 only if (1) $x_j[k] > O_j$ and $x_{j+1}[k] < O_{j+1}$; or (2) $x_j[k] < O_j$ and $x_{j+1}[k] > O_{j+1}$. The probability of the first condition is

$$P_1 = \int_{-\infty}^{O_j} \int_{O_{j+1}}^{\infty} p_b \, dx_{j+1} dx_j \tag{A.3}$$

$$= \int_{-\infty}^{0} \int_{0}^{\infty} p_b \, dx_{j+1} dx_j$$

$$+ \left(\int_{0}^{O_j} \int_{0}^{\infty} - \int_{-\infty}^{0} \int_{0}^{O_{j+1}} - \int_{0}^{O_j} \int_{0}^{O_{j+1}} \right) p_b \, dx_{j+1} dx_j \tag{A.4}$$

In the last equation, the first term on the right-hand side is the probability with $O_j = O_{j+1} = 0$, and the second term is the effect of offsets. Similarly, the probability of the second condition is

$$P_2 = \int_{O_j}^{\infty} \int_{-\infty}^{O_{j+1}} p_b \, dx_{j+1} dx_j \tag{A.5}$$

$$= \int_{0}^{\infty} \int_{-\infty}^{0} p_b \, dx_{j+1} dx_j$$

$$+ \left(-\int_{0}^{O_j} \int_{-\infty}^{0} + \int_{0}^{\infty} \int_{0}^{O_{j+1}} - \int_{0}^{O_j} \int_{0}^{O_{j+1}} \right) p_b \, dx_{j+1} dx_j \tag{A.6}$$

Thus, the total probability of $z_j[k] = 1$ is

$$P_{j,j+1}^z(O_j, O_{j+1}) = P_1 + P_2 = P_{j,j+1}^z + \Delta P_{j,j+1}^z \tag{A.7}$$

where $P_{j,j+1}^z$ as defined in Equation (3.5) is the ideal ZC probability, and

$$\Delta P_{j,j+1}^z \approx \frac{\rho_{j,j+1}}{2\pi \sqrt{1 - \rho_{j,j+1}^2}} \left(\frac{O_j^2}{\sigma_j^2} + \frac{O_{j+1}^2}{\sigma_{j+1}^2} - \frac{2}{\rho_{j,j+1}} \frac{O_j}{\sigma_j} \frac{O_{j+1}}{\sigma_{j+1}} \right) \tag{A.8}$$

Equation (A.8), as repeated in Equation (3.11), is the effect of offsets.

Consider a $x(t)$ signal having a non-zero dc component. It is equivalent to the case that both comparators in ZCD1 exhibit identical offsets, i.e., $O_j = O_{j+1} = O_x$. From Equation (A.7) and Equation (A.8), the corresponding ZC probability becomes

$$P^z_{j,j+1} \approx \frac{1}{2} - \frac{1}{\pi} \sin^{-1} \rho_{j,j+1} - \frac{1 - \rho_{j,j+1}}{\pi \sqrt{1 - \rho^2_{j,j+1}}} \frac{O^2_x}{\sigma^2_j} \tag{A.9}$$

And the zero crossing rate becomes

$$Z_R(t_0, T_c) = \frac{1}{\pi} \left(1 - \frac{O^2_x}{2\sigma^2_j} \right) \sqrt{ - \frac{\partial^2 \rho_{a,b}(t_0, T_c, t_s)}{\partial t^2_s} } \Bigg|_{t_s=0} \tag{A.10}$$

Both $P^z_{j,j+1}$ and Z_R are reduced by O^2_x.

A.2 Mathematical Analysis of ZCD2

Consider the ZCD2 shown in Figure 3.14. To simplify denotation, define $x_j[k] = x_1$, $x_j[k-1] = x_2$, $x_{j+1}[k] = x_3$, and $x_{j+1}[k-1] = x_4$.

First consider the case of three random variables x_1, x_2, and x_3. Assume they form the trivariate normal distribution with given cross correlation $\rho_{i,j}$ as defined Equation (A.59), where $\{i, j\} \in 1, 2, 3$. Define P_a, P_b, P_c, and P_d probabilities as

$$\begin{aligned}
P_a &\equiv P(x_1 < 0, x_2 < 0, x_3 < 0) = P(x_1 > 0, x_2 > 0, x_3 > 0) \\
P_b &\equiv P(x_1 < 0, x_2 > 0, x_3 < 0) = P(x_1 > 0, x_2 < 0, x_3 > 0) \\
P_c &\equiv P(x_1 > 0, x_2 < 0, x_3 < 0) = P(x_1 < 0, x_2 > 0, x_3 > 0) \\
P_d &\equiv P(x_1 > 0, x_2 > 0, x_3 < 0) = P(x_1 < 0, x_2 < 0, x_3 > 0)
\end{aligned} \tag{A.11}$$

Obviously, $P_a + P_b + P_c + P_d = 1/2$, and

$$\begin{aligned}
P_a + P_b &= P(x_1 < 0, x_3 < 0) = \frac{1}{4} + \frac{\sin^{-1} \rho_{1,3}}{2\pi} \\
P_a + P_c &= P(x_2 < 0, x_3 < 0) = \frac{1}{4} + \frac{\sin^{-1} \rho_{2,3}}{2\pi} \\
P_a + P_d &= P(x_1 < 0, x_2 < 0) = \frac{1}{4} + \frac{\sin^{-1} \rho_{1,2}}{2\pi}
\end{aligned} \tag{A.12}$$

where $\rho_{1,3}$, $\rho_{2,3}$, and $\rho_{1,2}$ are correlations between x_1 and x_3, x_2 and x_3, and x_1 and x_2 respectively. The above equations can be solved to give

$$
\begin{aligned}
P_a &= \frac{1}{8} + \frac{1}{4\pi} \left(\sin^{-1} \rho_{1,2} + \sin^{-1} \rho_{1,3} + \sin^{-1} \rho_{2,3} \right) \\
P_b &= \frac{1}{8} + \frac{1}{4\pi} \left(-\sin^{-1} \rho_{1,2} + \sin^{-1} \rho_{1,3} - \sin^{-1} \rho_{2,3} \right) \\
P_c &= \frac{1}{8} + \frac{1}{4\pi} \left(-\sin^{-1} \rho_{1,2} - \sin^{-1} \rho_{1,3} + \sin^{-1} \rho_{2,3} \right) \\
P_d &= \frac{1}{8} + \frac{1}{4\pi} \left(\sin^{-1} \rho_{1,2} - \sin^{-1} \rho_{1,3} - \sin^{-1} \rho_{2,3} \right)
\end{aligned}
\tag{A.13}
$$

Now consider the case of four random variables, x_1, x_2, x_3, and x_4. It is difficult to solve the probabilities in the form of Equation (A.13). Simplified solution is provided for the low-frequency case as follows. Define P_A, P_B, and P_c as

$$
\begin{aligned}
P_A &\equiv P(x_1 < 0, x_2 > 0, x_3 < 0, x_4 > 0) \\
P_B &\equiv P(x_1 < 0, x_2 > 0, x_3 > 0, x_4 < 0) \\
P_C &\equiv P(x_1 < 0, x_2 > 0, x_3 > 0, x_4 > 0)
\end{aligned}
\tag{A.14}
$$

From Equation (A.13), we have

$$
\begin{aligned}
P_A + P_C &= P(x_1 < 0, x_2 > 0, x_4 > 0) \\
&= \frac{1}{8} + \frac{1}{4\pi} \left(-\sin^{-1} \rho_{1,2} - \sin^{-1} \rho_{1,4} + \sin^{-1} \rho_{2,4} \right)
\end{aligned}
\tag{A.15}
$$

$$
\begin{aligned}
P_B + P_C &= P(x_1 < 0, x_2 > 0, x_3 > 0) \\
&= \frac{1}{8} + \frac{1}{4\pi} \left(-\sin^{-1} \rho_{1,2} - \sin^{-1} \rho_{1,3} + \sin^{-1} \rho_{2,3} \right)
\end{aligned}
\tag{A.16}
$$

For the low-frequency case, $\rho_{1,3} = \rho_{2,4} \approx 1$ and $P_B \approx 0$. As a result, we can solve the above equations and obtain

$$
P_A = -\frac{1}{4\pi} \left(\sin^{-1} \rho_{1,4} + \sin^{-1} \rho_{2,3} - \sin^{-1} \rho_{1,3} - \sin^{-1} \rho_{2,4} \right)
\tag{A.17}
$$

Then, the probability of $z_j[k] = 1$ is

$$
\begin{aligned}
P_{j,j+1}^z &= 1 - 2P_A \\
&= 1 + \frac{1}{2\pi} \left(\sin^{-1} \rho_{1,4} + \sin^{-1} \rho_{2,3} - \sin^{-1} \rho_{1,3} - \sin^{-1} \rho_{2,4} \right)
\end{aligned}
\tag{A.18}
$$

The above equation can be rewritten as

$$P_{j,j+1}^z = \frac{1}{\pi} \sin^{-1} \rho_{a,b}(t_0, T_c, t_s)\Big|_{t_s = T_c} + \int_{t_j}^{t_j + T_s} Z_R(t_0, T_c) dt_0 \qquad \text{(A.19)}$$

where $Z_R(t_0, T_c)$ is defined in Equation (A.63). The $Z_R(t_0, T_c)$ is identical to the $Z_R(t_0, T_c)$ for ZCD1. Note that the first term on the right-hand side of Equation (A.19) is independent of T_s. Only the second term containing $Z_R(t_0, T_c)$ is relevant in the proposed timing-skew detection scheme. Thus, we state that both ZCD1 and ZCD2 show identical $Z_R(t_0, T_c)$ behavior in the proposed timing-skew detection scheme under the low-f_i scenario.

Now consider a ZCD2 with internal comparators exhibiting offsets. The following assumption is made in order to simplify analysis. There are two different cases regarding the relationship between $x_j[k]$ and $x_j[k + 1]$: weak correlation and strong correlation. For the weak-correlation case, we can assume that the probability of $x_1 = x_j[k] < 0$ and $x_3 = x_{j+1}[k] < 0$ is independent of the probability of $x_2 = x_j[k - 1] > 0$ and $x_4 = x_{j+1}[k - 1] > 0$. Thus

$$\begin{aligned} P_A &\equiv P(x_1 < 0, x_2 > 0, x_3 < 0, x_4 > 0) \\ &\approx P(x_1 < 0, x_3 < 0) \times P(x_2 > 0, x_4 > 0) \end{aligned} \qquad \text{(A.20)}$$

Define probabilities $P_{1,3} \equiv P(x_1 < 0, x_3 < 0)$ and $P_{2,4} \equiv P(x_2 > 0, x_4 > 0)$. When the comparators exhibit offsets, the corresponding probabilities becomes $P_{1,3}^O = P_{1,3} + \Delta P_{1,3}$ and $P_{2,4}^O = P_{2,4} + \Delta P_{2,4}$, where

$$\begin{aligned} \Delta P_{1,3} &= P(x_1 < O_j, x_3 < O_{j+1}) - P(x_1 < 0, x_3 < 0) \\ &= \int_{-\infty}^{O_j} \int_{-\infty}^{O_{j+1}} p_b \, dx_3 dx_1 - \int_{-\infty}^{0} \int_{-\infty}^{0} p_b \, dx_3 dx_1 \\ &= \left(\int_{0}^{O_j} \int_{-\infty}^{0} + \int_{-\infty}^{0} \int_{0}^{O_{j+1}} + \int_{0}^{O_j} \int_{0}^{O_{j+1}} \right) p_b \, dx_3 dx_1 \\ &\approx \frac{1}{2\sqrt{2\pi}} \left(\frac{O_j}{\sigma_j} + \frac{O_{j+1}}{\sigma_{j+1}} \right) \end{aligned} \qquad \text{(A.21)}$$

and

$$\begin{aligned} \Delta P_{2,4} &= P(x_2 > O_j, x_4 > O_{j+1}) - P(x_2 > 0, x_4 > 0) \\ &\approx -\frac{1}{2\sqrt{2\pi}} \left(\frac{O_j}{\sigma_j} + \frac{O_{j+1}}{\sigma_{j+1}} \right) = -\Delta P_{1,3} \end{aligned} \qquad \text{(A.22)}$$

Note that $P_{1,3} = P_{2,4}$. From Equation (A.20) and using $P^z_{j,j+1} = 1 - 2P_A$, the $P^z_{j,j+1}$ probability for ZCD2 is deviated from Equation (A.19) by

$$\Delta P^z_{j,j+1} = 2(\Delta P_{1,3})^2 = \frac{1}{4\pi}\left(\frac{O_j}{\sigma_j} + \frac{O_{j+1}}{\sigma_{j+1}}\right)^2 \tag{A.23}$$

The above equation is repeated in Equation (3.13).

For the strong-correlation case, we assume that, under the $z_j[k] = 1$ condition, the relationship between x_1 and x_2 is similar to the relationship between x_3 and x_4. Furthermore, $x_1 \approx x_3$ or $x_1 \approx -x_3$, and $x_2 \approx x_4$ or $x_2 \approx -x_4$. Thus,

$$\begin{aligned}
P_A &\equiv P(x_1 < 0, x_2 > 0, x_3 < 0, x_4 > 0) \\
&\approx P(x_1 < 0, x_2 > 0)
\end{aligned} \tag{A.24}$$

The probability variation due to O_j is

$$\begin{aligned}
\Delta P_{A,O_j} &\equiv P(x_1 < O_j, x_2 > O_j) - P(x_1 < 0, x_2 > 0) \\
\text{or} &\equiv P(x_1 > O_j, x_2 < O_j) - P(x_1 > 0, x_2 < 0) \\
&= \frac{1}{\pi}\sqrt{\frac{1 - \rho_{1,2}}{1 + \rho_{1,2}} \times \frac{O_j^2}{\sigma_j^2}}
\end{aligned} \tag{A.25}$$

The probability variation due to O_{j+1} is

$$\begin{aligned}
\Delta P_{A,O_{j+1}} &\equiv P(x_3 < O_{j+1}, x_4 > O_{j+1}) - P(x_3 < 0, x_4 > 0) \\
\text{or} &\equiv P(x_3 > O_{j+1}, x_4 < O_{j+1}) - P(x_3 > 0, x_4 < 0) \\
&= \frac{1}{\pi}\sqrt{\frac{1 - \rho_{3,4}}{1 + \rho_{3,4}} \times \frac{O_{j+1}^2}{\sigma_{j+1}^2}}
\end{aligned} \tag{A.26}$$

Thus, the total probability variation due to the offsets is

$$\begin{aligned}
\Delta P^z_{j,j+1} &= \Delta P_{A,O_j} + \Delta P_{A,O_{j+1}} \\
&= \frac{1}{\pi}\sqrt{\frac{1 - \rho_{1,2}}{1 + \rho_{1,2}} \times \frac{O_j^2}{\sigma_j^2}} + \frac{1}{\pi}\sqrt{\frac{1 - \rho_{3,4}}{1 + \rho_{3,4}} \times \frac{O_{j+1}^2}{\sigma_{j+1}^2}}
\end{aligned} \tag{A.27}$$

Comparing Equation (A.27) with Equation (A.23), the weak-correlation case shows larger probability variation than the strong-correlation case. Thus, we choose Equation (A.23) as the upper bound for $\Delta P^z_{j,j+1}$.
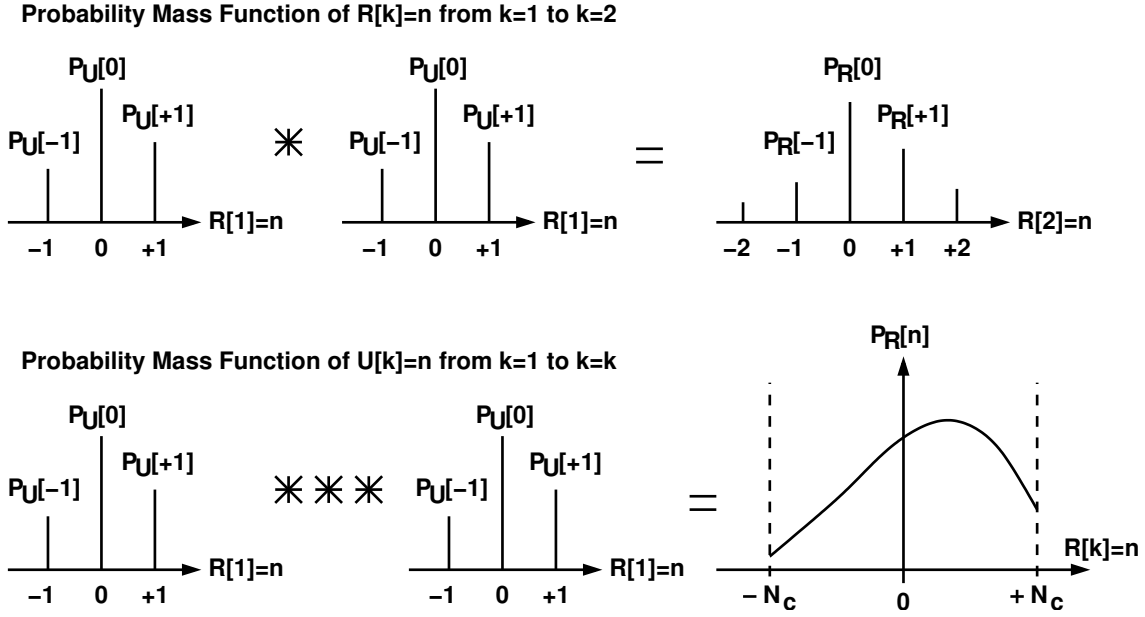
Figure A.2: Relationship between $P_R[n]$ and $P_U[n]$.

A.3 Timing Fluctuation Due to Skew Calibration

Consider the $(j-1)$-th calibration channel in the CP of Figure 4.1. It receives the $x_{j-1}[k]$ and $x_j[k]$ sequences and generates the $T_j[k]$ output to adjust τ_j. Its ACC1 accumulator takes $U[k] = m[k] - z_{j-1}[k]$ and generates $R[k]$. Define $P_U[n]$ as the probability function of $U[k] = n$ and $P_R[n]$ as the probability function of $R[k] = n$, where n is an integer. Since $z_j[k] \in \{0, 1\}$ and $m[k] \in \{0, 1\}$, $P_U[n] = 0$ for $n > 1$ or $n < -1$. $R[k]$ is generated by accumulating the $U[k]$ sequence. It is reset to 0 whenever $R[k] \geq +N_C$ or $R[k] \leq -N_C$. Thus, $P_R[n] = 0$ for $n > +N_C$ or $n < -N_C$. We can derive the relationship between $P_R[n]$ and $P_U[n]$ as follows. At $k = 1$, let $U[1] = R[1] = n$, then the probability mass function (PMF) of $R[1] = n$ is the same as the PMF of $U[1] = n$. At $k = 2$, the condition for $R[2] = 1$ is $U[1] = 1$ & $U[2] = 0$ or $U[1] = 0$ & $U[2] = 1$. Thus the probability of $R[2] = 1$ is $P_U[+1] \times P_U[0] + P_U[0] \times P_U[+1] = 2P_U[+1] \times P_U[0]$. From the same reasoning, the probability mass function of $R[2] = n$ is $P_U[n] * P_U[n]$, where $*$ is a convolution operator. As shown in Figure A.2, we can also derive that $P_R[n]$ is a consecutive k times convolution of $P_U[n]$, i.e.,

$$P_R[n] = P_U[n] * P_U[n] * \cdots * P_U[n] \tag{A.28}$$

When the calibration loop converges, it implies $k \rightarrow \infty$ and $P_R[n] * P_U[n] = P_R[n]$. However, the BPD following the ACC1 accumulator reset $R[k]$ to zero whenever $R[k] = +N_C$ or $-N_C$. This means $P_R[n] = 0$ for $n > +N_C$ or $n < -N_C$. The probability of $P_R[+N_C + 1] = P_R[+N_C] \times P_U[+1]$ is reset to zero and added to $P_R[0]$. The probability of $P_R[-N_C - 1] = P_R[-N_C] \times P_U[-1]$ is also reset to zero and added to $P_R[0]$. We can find $P_R[n]$ by solving the following recursive difference equations

$$P_R[+N_C] = P_R[+N_C - 1]P_U[+1] \tag{A.29}$$

$$P_R[-N_C] = P_R[-N_C + 1]P_U[-1] \tag{A.30}$$

$$P_R[+N_C - 1] = P_R[+N_C - 2]P_U[+1] + P_R[+N_C - 1]P_U[0] \tag{A.31}$$

$$P_R[-N_C + 1] = P_R[-N_C + 2]P_U[-1] + P_R[-N_C + 1]P_U[0] \tag{A.32}$$

$$P_R[n] = P_R[n - 1]P_U[+1] + P_R[n]P_U[0] + P_R[n + 1]P_U[-1] \tag{A.33}$$

where $-N_C + 2 \leq n \leq N_C - 2$.

The characteristic equation is

$$y = P_U[+1] + P_U[0]y + P_U[-1]y^2 \tag{A.34}$$

where y is the characteristic value for the above recursive equations. Solving the characteristic equation gives $y = 1$ or

$$y = \frac{P_U[+1]}{P_U[-1]} \equiv y_r \tag{A.35}$$

With this and $P_U[0] + P_U[+1] + P_U[-1] = 1$, the general form of $P_R[n]$ can be written as

$$P_R[n] = A + B(y_r)^n \tag{A.36}$$

The above recursive difference equations can be summarized as

$$P_R[n] = \frac{P_R[+N_C]}{P_U[+1](y_r^{-1} - 1)}\left(-1 + y_r^{-N_C+n}\right) \tag{A.37}$$

and

$$\frac{P_R[+N_C]}{P_R[-N_C]} = \frac{-1 + y_r^{+N_C}}{+1 - y_r^{-N_C}} \equiv \eta \tag{A.38}$$

where $-N_C + 2 \leq n \leq N_C - 2$ and $y_r \neq 1$. $P_R[+N_C]$ shows the probability of τ_j being increased and $P_R[-N_C]$ shows the probability of τ_j being decreased. The $y_r^{+N_C}$ and $y_r^{-N_C}$

terms in Equation (A.38) imply that the $P_R[+N_C]/P_R[-N_C]$ ratio is either very large or close to 0 if N_C is large. The above statement is still valid even when the difference between $P_U[+1]$ and $P_U[-1]$ is small.

When the timing-skew calibration loop converges, y_r is close to 1, Define $y_r = 1 + \Delta y$. From Equation (A.38), we have

$$\frac{P_R[+N_C]}{P_R[-N_C]} \approx \begin{cases} N_C \Delta y & \text{if } \Delta y > 0 \\ -1/(N_C \Delta y) & \text{if } \Delta y < 0 \end{cases} \tag{A.39}$$

Note that

$$\lim_{\Delta y \to 0^+} \frac{P_R[+N_C]}{P_R[-N_C]} \neq \lim_{\Delta y \to 0^-} \frac{P_R[+N_C]}{P_R[-N_C]} \neq \frac{P_R[+N_C]}{P_R[-N_C]} \Bigg|_{\Delta y = 0} \tag{A.40}$$

The case with $\Delta y > 0$ is symmetical to the case with $\Delta y < 0$. To ease discussion, only the $\Delta y > 0$ case is considered below. We have

$$P_R[+N_C] = \frac{\Delta P}{N_C - 1} \tag{A.41}$$

$$P_R[-N_C] = \frac{\Delta P}{N_C(N_C - 1)\Delta y} \tag{A.42}$$

where $\Delta P = P_U[+1] - P_U[-1]$ is a function of the τ_j timing skew.

Consider a $x(t)$ signal that has an uniform ZC density of Z_R. Let $\tau_{j,0} = \Delta y_0 T_s$. When the calibration loop converges, we have $P_U[+1] = Z_R(1 + \Delta y_0)$ and $P_U[-1] = Z_R$. Furthermore, the probability of τ_j jumping from $\tau_{j,i}$ to $\tau_{j,i+1}$ is equal to the probability of τ_j jumping from $\tau_{j,i+1}$ to $\tau_{j,i}$ [15], where i is an integer and $\tau_{j,i}$ is a discrete value of τ_j. Therefore,

$$M(\tau_{j,0})\frac{\Delta P(\tau_{j,0})}{N_C - 1} = M(\tau_{j,-1})\frac{\Delta P(\mu_t - \tau_{j,0})}{N_C - 1} \tag{A.43}$$

$$M(\tau_{j,0})\frac{\Delta P(\tau_{j,0})}{N_C(N_C - 1)\Delta y_0} = M(\tau_{j,+1})\frac{\Delta P(\mu_t + \tau_{j,0})}{N_C - 1} \tag{A.44}$$

$$M(\tau_{j,-2})\frac{\Delta P(2\mu_t - \tau_{j,0})}{N_C - 1} = M(\tau_{j,-1})\frac{\Delta P(\mu_t - \tau_{j,0})}{N_C(N_C - 1)(\mu_t/T_s - \Delta y_0)} \tag{A.45}$$

$$M(\tau_{j,1})\frac{\Delta P(\mu_t + \tau_{j,0})}{N_C(N_C - 1)(\mu_t/T_s + \Delta y_0)} = M(\tau_{j,2})\frac{\Delta P(2\mu_t + \tau_{j,0})}{N_C - 1} \tag{A.46}$$

Note that $\sum_{i=-\infty}^{\infty} M(\tau_{j,i}) = 1$. If N_C is large, only $M(\tau_{j,0})$, $M(\tau_{j,-1})$, $M(\tau_{j,1})$, $M(\tau_{j,-2})$ and $M(\tau_{j,2})$ are significant. We have

$$M(\tau_{j,-1}) = \frac{\tau_{j,0}}{\mu_t - \tau_{j,0}} M(\tau_{j,0}) \tag{A.47}$$

$$M(\tau_{j,1}) = \frac{T_s}{N_C(\mu_t + \tau_{j,0})} M(\tau_{j,0}) \tag{A.48}$$

$$M(\tau_{j,-2}) = \frac{\Delta t \times T_s}{N_C(\mu_t - \tau_{j,0}) \times (2\mu_t - \tau_{j,0})} M(\tau_{j,0}) \tag{A.49}$$

$$M(\tau_{j,2}) = \frac{T_s^2}{N_C^2(2\mu_t + \tau_{j,0})(\mu_t + \tau_{j,0})} M(\tau_{j,0}) \tag{A.50}$$

Then, $M(\tau_{j,i})$ can be approximated by

$$M(\tau_{j,0}) = \frac{\mu_t - \tau_{j,0}}{\mu_t} \tag{A.51}$$

$$M(\tau_{j,-1}) = \frac{\tau_{j,0}}{\mu_t} \tag{A.52}$$

$$M(\tau_{j,1}) = \frac{T_s}{N_C \mu_t (\mu_t + \tau_{j,0})} (\mu_t - \tau_{j,0}) \tag{A.53}$$

$$M(\tau_{j,-2}) = \frac{\tau_{j,0} \times T_s}{N_C \mu_t (2\mu_t - \tau_{j,0})} \tag{A.54}$$

$$M(\tau_{j,2}) = \frac{T_s^2}{N_C^2(2\mu_t + \tau_{j,0})(\mu_t + \tau_{j,0})} \frac{\mu_t - \tau_{j,0}}{\mu_t} \tag{A.55}$$

The mean variance of $\tau_{j,i}$ is

$$\begin{aligned}
\sigma^2(\tau) &\equiv \frac{1}{\mu_t} \int_{-\mu_t/2}^{+\mu_t/2} \sum_{i=-\infty}^{+\infty} \left[M(\tau_{j,i}) \times (\tau_{j,0} + i\mu_t)^2 \right] d\tau_{j,0} \\
&= \frac{2}{\mu_t} \int_0^{+\mu_t/2} \sum_{i=-\infty}^{+\infty} \left[M(\tau_{j,i}) \times (\tau_{j,0} + i\mu_t)^2 \right] d\tau_{j,0} \\
&\approx \frac{1}{6}\mu_t^2 + \frac{4T_s}{3N_C}\mu_t
\end{aligned} \tag{A.56}$$

The above equation is repeated in Equation (4.4). We can ignore the case with $y_r = 1$. In this case, $\tau_{j,0} = 0$, thus the integration in the above equation is zero, i.e., $\int_0^0 (\text{any function}) d\tau_{j,0} = 0$.
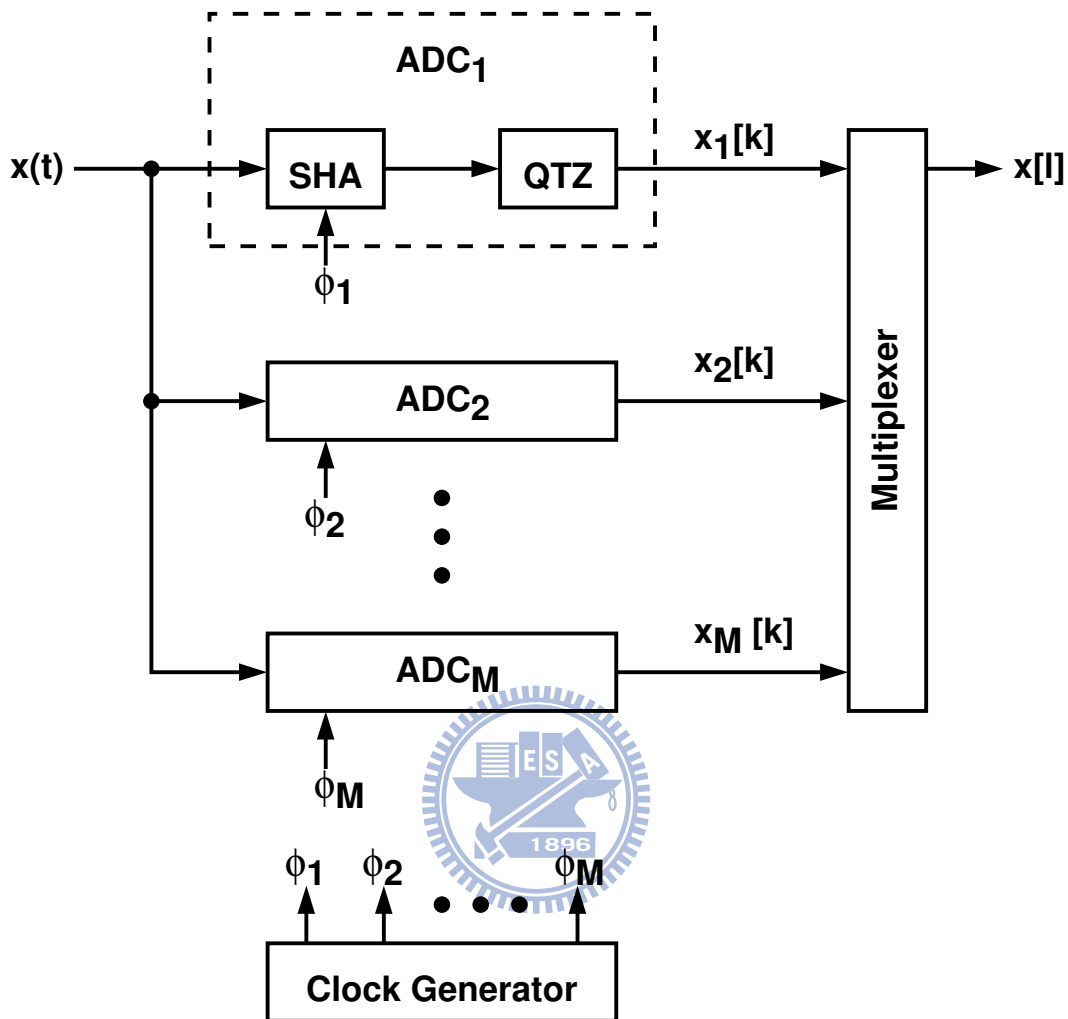
Figure A.3: A time-interleaved ADC architecture.

A.4   Timing Skew Calibration Using Clock Chopper

In this section, we will introduce the timing skew calibration using clock chopper. The concept of two-channel calibration technique will be described and it can be applied in multi-channel time-interleaved ADCs.

A.4.1   Timing-Skew Detection

Assuming all A/D channels shown in Figure A.3 are linear and without gain and offset errors, the digital output of the ADC $_j$ can be expressed as:

$$S_j[k] = s\left((M \times k + j)T_s + t_0 + \tau_j\right) \tag{A.57}$$

where $T_s = 1/f_s$ is the nominal sampling interval. The t_0 represents the initial sampling time at $k = 0$ for the ADC $_1$. The t_0 has a value between 0 and $M \times T_s$. The τ_j is the timing difference between the clock generator and the j-th SHA caused by routing. The t_0 is defined in such a way that the mean of τ_j, for $j = 1, 2, \cdots M$, is zero, i.e., $\tau_1 + \tau_2 + \cdots + \tau_M = 0$. A timing skew occurs when $\tau_a \neq \tau_b$ for $a \neq b$. Notable, the sampling interval for each A/D channel is $T_c = M \times T_s$, and the clock frequency is $f_c = 1/T_c$. Equation (A.57) neglects the effects of amplitude quantization.

First assume that the sampling rate, f_s, is larger than the Nyquist sampling frequency of the $s(t)$ input, i.e., larger than twice the $s(t)$'s bandwidth. Since $s(t)$ is continuous in time and in amplitude, there is one and only one moment between two consecutive sampling instant that the $s(t)$ crosses over the zero if the input's values sampled by the corresponding A/D channels, ADC $_j$ and the subsequent ADC $_{j+1}$, have opposite signs, i.e., $s_j[k] \times s_{j+1}[k] < 0$. Second, assume that the $s(t)$ is a stationary Gaussian process with zero mean. Then, the probability of a zero crossing between ADC $_j$ and ADC $_{j+1}$, $P^z_{j,j+1}$, is a bivariate normal distribution [22] [23], and can be expressed as:

$$P^z_{j,j+1} = \frac{1}{2} - \frac{1}{\pi} \sin^{-1} \rho_{j,j+1} \tag{A.58}$$

with

$$\rho_{j,j+1} = \frac{E[s_j \times s_{j+1}]}{\sigma_j \times \sigma_{j+1}} \tag{A.59}$$

where σ_j and σ_{j+1} are the standard deviations of the s_j and s_{j+1} random variables respectively. The $\rho_{j,j+1}$ of Equation (A.59) denotes the cross-correlation between s_j and s_{j+1}.

The upper half of Figure A.4 illustrates the proposed timing-skew detection scheme. Two choppers, a clock chopper and a data chopper, are placed at the outputs of clock generator and at the outputs of the A/D channels. The two choppers are controlled by a binary-valued random sequence, $q[k] \in \{-1, +1\}$. When $q[k] = +1$, the choppers'
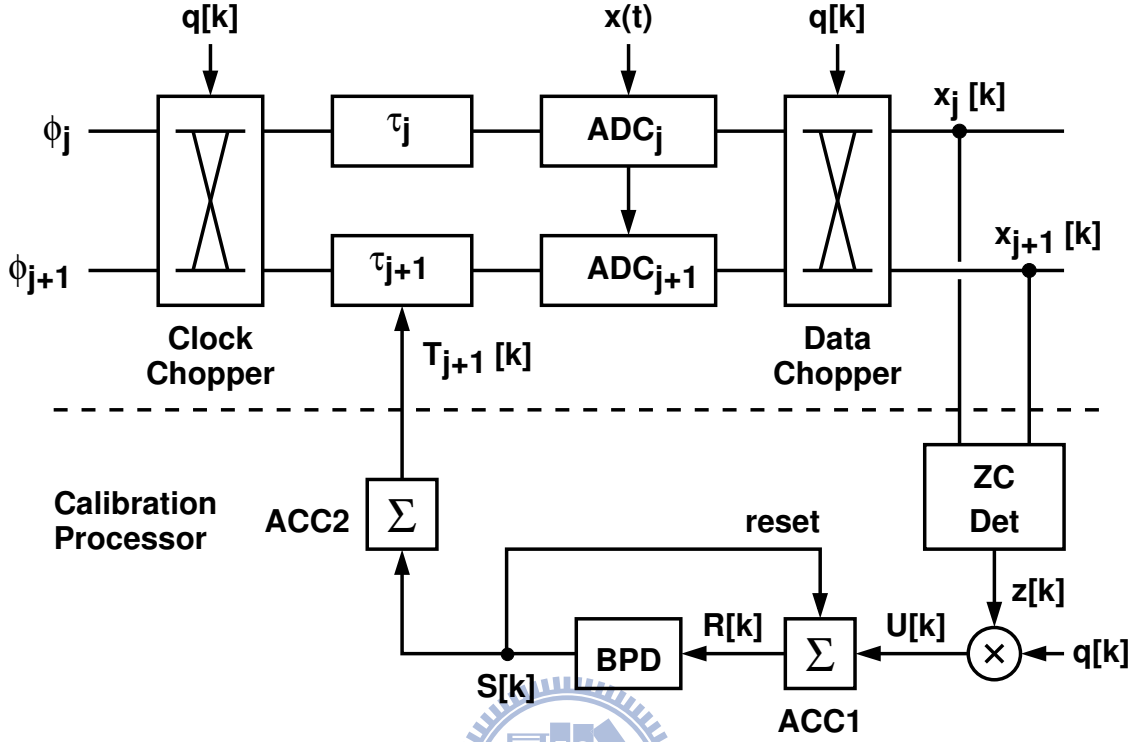
Figure A.4: Timing-skew detection and calibration for two channels.

outputs are the same as its corresponding inputs. When $q[k] = -1$, the choppers' outputs are exchanged. Thus, the sampling interval between the ADC $_j$ and the ADC $_{j+1}$ can be expressed as:

$$\Delta T_{j,j+1} = T_s + q[k] \times (\tau_j - \tau_{j+1}) \tag{A.60}$$

As manifested by Equation (A.63) and Equation (A.64) shown later, the $P_{j,j+1}^z$ is a monotonic function of $\Delta T_{j,j+1}$ for an $x(t)$ input with limited bandwidth. Thus, the polarity of the timing skew, $\tau_j - \tau_{j+1}$, can be detected by observing the change in $P_{j,j+1}^z$ whenever $q[k]$ changes. The $q[k]$ is chosen to be random to minimize the input dependence of the detection scheme. To ensure the detection accuracy, it is critical that the clock chopper in Figure A.4 does not introduce additional timing skew.

A.4.2 Two-Channel Timing-Skew Calibration

The bottom half of Figure A.4 shows the block diagram of the proposed timing-skew calibration processor (CP) between the two adjacent A/D channels, ADC $_j$ and ADC $_{j+1}$.

Since only the polarity of the $\tau_j - \tau_{j+1}$ timing skew can be detected, this CP empolys a similiar approach used in a comparator offset calibration scheme [15]. For the zero-crossing detector (ZC Det), its output $z[k] = 1$ whenever $x_j[k] \times x_{j+1}[k] < 0$, otherwise $z[k] = 0$. The $z[k]$ sequence is then correlated with the $q[k]$ sequence and integrated on the ACC1 accumulator. The ACC1's output is $R[k]$. The rate of long-term change in $R[k]$ is proportional to the probability difference, $\Delta P_{j,j+1}^z$,

$$\Delta P_{j,j+1}^z = P_{j,j+1}^z \big|_{q[k]=+1} - P_{j,j+1}^z \big|_{q[k]=-1} \qquad \text{(A.61)}$$

The bilateral peak detector (BPD) monitors the value of $R[k]$ and generates a corresponding triple-valued output, $S[k] \in \{+1, 0, -1\}$. The BPD has two thresholds, $+N_C$ and $-N_C$. When $R[k] > +N_C$, $S[k] = +1$. When $R[k] < -N_C$, $S[k] = -1$. Otherwise, $S[k] = 0$. In addition, the ACC1 accumulator is reset to zero whenever $S[k] = +1$ or $S[k] = -1$. Thus, $-(N_C + 1) \le R[k] \le +(N_C + 1)$, and $S[k]$ can only remain as $+1$ or -1 for one clock cycle. The $S[k]$ sequence is integrated by the ACC2 accumulator. Its output, $T_{j+1}[k]$, controls the digitally-controlled τ_{j+1} delay unit, such that:

$$\tau_{j+1}[k] = \tau_{j+1,0} + \mu_t \times T_{j+1}[k] \qquad \text{(A.62)}$$

where μ_t is the delay unit's step size for digital control and $\tau_{j+1,0}$ is the time delay of τ_{j+1} when $T_{j+1}[k] = 0$. The CP adjusts τ_{j+1} automatically to minimize the difference between τ_j and τ_{j+1}.

There are two design parameters in this calibration scheme, μ_t and N_C. Together with $P_{j,j+1}^z$ and $\Delta P_{j,j+1}^z$, they affect the calibration behaviors, such as the converging speed and the sampling jitter due to the disturbance of the $x(t)$ input. Detailed analyses have been given in [15]. Generally, large μ_t and small N_C result in fast converging speed but large timing jitter in τ_{j+1}. On the other hand, small and large N_C result in small timing jitter but also slow converging speed.

The calibration behaviors strongly depend on the property of the $x(t)$ input. For a generic $x(t)$ input, the cross-correlation of Equation (A.59) between two periodic sampling sequences, $x_a[k] = x(kt_c + t_0)$ and $x_b[k] = x(kt_c + t_s + t_0)$, can be expressed as $\rho(t_0, t_s, t_c)$. The t_c is the sampling interval for each of the sampling sequence, the t_s is the sampling time difference between the two sequences, and the t_0 is the initial sampling

time for $x_a[0]$. Notably, the $\rho(t_0, t_s, t_c)$ is a periodic function of t_0 with a period of t_c. In the case of a time-interleaved ADC, we also have $t_s \leq t_c/2$. From Equation (A.58), the corresponding zero-crossing probability between the two sampling sequences can be expressed as $P^z(t_0, t_s, t_c)$. Analogous to the probability density function, the zero-crossing density, defined as the zero-crossing probability per unit t_s time, can be expressed as:

$$Z_R(t_0, t_c) \equiv \lim_{t_s \to 0} \frac{P^z(t_0, t_s, t_c)}{t_s} = \frac{1}{\pi} \times \left[-\frac{\partial^2 \rho(t_0, t_s, t_c)}{\partial t_s^2} \right]^{1/2} \Bigg|_{t_s=0} \tag{A.63}$$

For a M-channel time-interleaved ADC with T_s sampling interval between the adjacent channels, the single-channel sampling interval is $T_c = M \times T_s$. Assume the timing skew between the ADC $_j$ and the ADC $_{j+1}$ is small, i.e., $\Delta \tau_j \equiv \tau_j - \tau_{j+1} \ll T_s$, the probability difference, $\Delta P^z_{j,j+1}$, can then be approximated by:

$$\Delta P^z_{j,j+1} = [Z_R(t_0, T_c) + Z_R(t_0 + T_s, T_c)] \times \Delta \tau_j \tag{A.64}$$

From Equation (A.63), it can be shown that $Z_R(t_0, t_c) \geq 0$. Thus, $\Delta P^z_{j,j+1}$ has the same polarity as $\Delta \tau_j$. Furthermore, the zero-crossing probability can be expressed as:

$$P^z_{j,j+1} = \int_{t_0}^{t_0+T_s} Z_R(t, T_c) dt \tag{A.65}$$

Both $P^z_{j,j+1}$ and $\Delta P^z_{j,j+1}$ are required in estimating the converging speed and timing jitter of the calibration process [15].

Consider the the system shown in Figure A.4. If $\Delta P^z_{j,j+1}/\Delta \tau_j = Z_R(t_0, T_c) + Z_R(t_0 + T_s, T_c)$ is a constant, then the system's transient behavior can be modeled as a single-pole system with a time constant expressed as [15]:

$$\tau_c = \frac{N_C}{\mu_t} \times \frac{2}{Z_R(t_0, T_c) + Z_R(t_0 + T_s, T_c)} \tag{A.66}$$

As an example, let $x(t)$ be a single-tone sine wave, i.e., $x(t) = A \sin(2\pi f_i t)$, which has a frequency of f_i and a constant amplitude of A. Its corresponding $\rho(t_0, t_s, t_c)$ is $\cos(2\pi f_i t_s)$, and the corresponding $Z_R(t_0, t_c)$ can be expressed as:

$$Z_R(t_0, t_c) = \begin{cases} 2f_i & \frac{f_i}{f_c} \neq \frac{a}{b} \\ \sum_{n=0}^{a-1} \frac{2}{b} \delta \left(t_0 - n \cdot \frac{t_c}{a} \right) & \frac{f_i}{f_c} = \frac{a}{b} \quad b \text{ is even.} \\ \sum_{n=0}^{2a-1} \frac{1}{b} \delta \left(t_0 - n \cdot \frac{t_c}{2a} \right) & \frac{f_i}{f_c} = \frac{a}{b} \quad b \text{ is odd.} \end{cases} \tag{A.67}$$
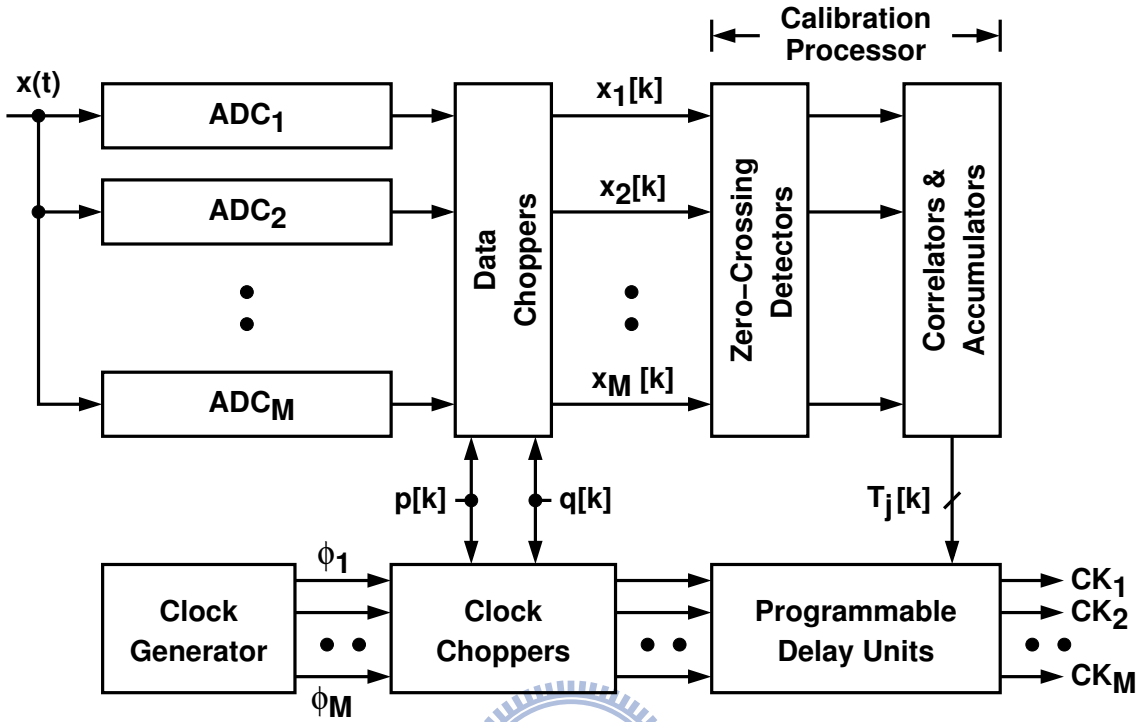
Figure A.5: Full-system timing-skew calibration.

where $f_c = 1/T_c$ is the sampling rate for a single channel, and *a* and *b* are two mutually prime positive integers. If the f_i/f_c ratio is irrational, i.e., $f_i/f_c \neq a/b$, the zero-crossing density, Z_R, is equal to $2f_i$, and independent of t_0 and t_c. If $f_i/f_c = a/b$, the input sine wave synchronizes with the f_c sampling clock. Thus, within any time period of the f_c clock, there are only a finite number of instants at which the zero-crossings can occur. If *b* is even, there are *a* possible uniformly-spaced zero-crossing instants. On the other hand, if *b* is odd, there are 2*a* possible uniformly-spaced zero-crossing instants. The proposed timing-skew calibration scheme cannot function properly with a synchronous input, unless the coressponding *a* is sufficiently large so that the time interval between the zero-crossings is smaller than the required timing resolution.

Figure A.6: Proposed pairing scheme for an 8-channel system.

A.5 Multi-Channel Timing-Skew Calibration With Clock Chopper

Figure A.5 shows the calibration scheme for the entire M-channel time-interleaved ADC. The clock generator produces M clocks wi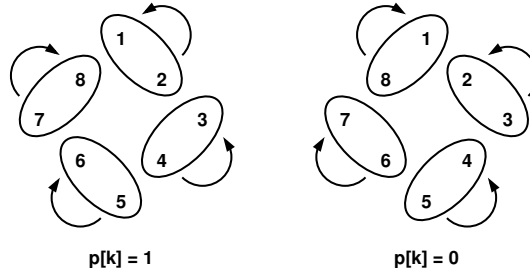th an identical frequency of f_c and equally-spaced phases. The clocks pass through the clock choppers and the digitally-controlled delay units to generate CK_1, CK_2, ..., CK_M which control the sampling timing of ADC $_1$, ADC $_2$, ..., ADC $_M$ repectively. The calibration processor (CP) adjusts the digitally-controlled delay units to minimize the timing skews among the A/D channels. The timing skews are caused by mismatches among the clock routes from the outputs of clock choppers to the sample-to-hold amplifiers in the A/D channels. The CP is pure digital and operate at a clock rate of f_c. It consists of only comparators, adders and registers, and requires no multi-bit multiplier.

A pairing scheme is proposed so that (1) the two-channel timing-skew calibration can be executed simultaneously on the selected pairs of A/D channels; (2) each clock chopper only swaps the sampling clocks of adjacent A/D channels; and (3) timing skews of all A/D channels are minimized relative to a single reference channel. As shown in Figure A.5, there are two independent random sequences, $p[k] \in \{-1, +1\}$ and $q[k] \in \{-1, +1\}$ for the control of the clock choppers and the data choppers. Figure A.6 illustrates the proposed pairing scheme for an 8-channel time-interleaved ADC. When $p[k] = +1$, the following calibration pairs are selected for simultaneous calibration: $(1, 2)$, $(3, 4)$, $(8, 7)$, $(6, 5)$. For each calibration pair, (a, b), the $q[k]$ sequence toggles the corresponding choppers to altenerate the sampling sequence of ADC $_a$ and ADC $_b$. The CP then adjusts the

b-th delay unit to minimized the timing skew between the two channels. When $p[k] = -1$, the following calibration pairs are selected for simultaneous calibration: $(2, 3)$, $(4, 5)$, $(1, 8)$, $(7, 6)$. This pairing scheme assigns ADC $_1$ as the reference channel. For other A/D channel, its corresponding delay unit is ajusted so that its timing skew with the reference channel is eventually minimized.

In the above pairing scheme, the sampling interval of each individual A/D channel is no longer a constant MT_s, due to the reordering of the sampling sequence. The two random sequences, $p[k]$ and $q[k]$, are operated at the f_c clock, and they can change state only after the present state has been applied to all A/D channels. If $p[k]$ is restricted to change only during $q[k] = +1$, the sampling interval for each A/D channel can be confined to vary between $(M - 1)T_s$ and $(M + 1)T_s$.

Consider only the timing jitter caused by the calibration process using the pairing scheme just described. Let ADC $_1$ be the reference channel in a M-channel ADC, and all calibration pairs employ identical μ_t and N_C parameters. Since ADC $_1$ is the reference channel, the corresponding τ_1 is not adjusted, thus its jitter standard deviation $\sigma(\tau_1) = 0$. For ADC $_2$, the corresponding τ_2 is adjusted toward τ_1, resulting in a jitter standard deviation of $\sigma(\tau_2)$. For ADC $_3$, the corresponding τ_3 is adjusted toward τ_2, resulting in a jitter standard deviation of $\sqrt{2}\sigma(\tau_2)$. In general, for ADC $_{j+1}$ where $j \geq 2$, the corresponding τ_{j+1} is adjusted toward τ_j, and its jitter standard deviation can be expressed as:

$$\sigma(\tau_{j+1}) = \sqrt{j} \times \sigma(\tau_2) \tag{A.68}$$

On the other side of ADC $_1$, ADC $_M$ has the same jitter standard deviation as ADC $_2$, ADC $_{M-1}$ has the same jitter standard deviation as ADC $_3$, and etc. In the 8-channel example, the ADC $_5$ has largest timing jitter. To reduce $\sigma(\tau_{j+1})$, the CP can use larger N_C value when calibrating the timing skew of the ADC $_{j+1}$.

In the proposed pairing sheme for multi-channel calibration, the use of the p random sequence increases the response time of the system by a factor of two. If $\Delta P^z_{j,j+1}/\Delta\tau_j = Z_R(t_0, T_c) + Z_R(t_0 + T_s, T_c)$ is a constant, then the system's transient behavior can also be modeled as a single-pole system with a time constant expressed as:

$$\tau_s = 2\tau_c \tag{A.69}$$

where τ_c is defined in Equation (A.66).

It is imperative to carefully choose the timing of $p[k]$ and $q[k]$ for controlling the clock choppers, so that undesirable glitches are not generated in the clocks when the choppers are toggled.
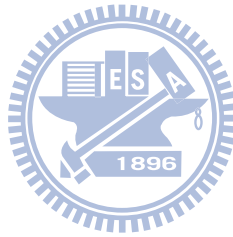
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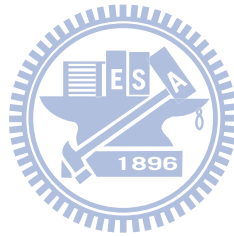
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Vita

Chung-Yi Wang was born in Tai-Chung, Taiwan, R.O.C.. He received the B.S. and the M.S. degree in electronics engineering from National Chiao-Tung University, Hsin-Chu, Taiwan, R.O.C. in 2002 and 2003, respectively. He worked toward the Ph.D. degree in National Chiao-Tung University from 2003 to 2009. His research interests in mixed-signal, high speed and high resolution integrated circuits design in data communication.

In 2008, he joined the Mediatek, where he was engaged in the design of analog and mixed-signal ICs.

住址: 新竹縣竹北市六家八街三號六樓

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Publication List

- Journal Paper:

    - **C.-Y. Wang**, and J.-T. Wu, "A Multiphase Timing Skew Calibration Technique Using Zero Crossing Detection ," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 6, pp. 1102–1114, June 2009.

    - **C.-Y. Wang**, and J.-T. Wu, "A Background Timing-Skew Calibration Technique for Time-Interleaved Analog-to-Digital Converters ," *IEEE Trans. Circuits Syst. II*, vol. 53, no. 4, pp. 299–303, April 2006.

    - J.-L. Fan, **C.-Y. Wang**, and J.-T. Wu, "A Robust and Fast Digital Background Calibration Technique for Pipelined ADCs," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 6, pp. 1213–1223, June 2007.

- Patent:

    - **C.-Y. Wang** and J-T Wu, "Time-interleaved analog-to-digital converter with background timing-skew calibration," US/TW patent no. 11/478,679.