國 立 交 通 大 學

電機與控制工程研究所

碩 士 論 文

具預先增強與準位自動校正之驅動電路

A Self-Calibrate Driver with Pre-Emphasis

研 究 生：陳冠羽

指導教授：蘇朝琴　教授

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研 究 生：陳冠羽　　Student : Kuan-Yu Chen

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摘　要

由於製程技術的進步，CMOS 積體電路的操作頻率及電路複雜度也隨著增加。使得晶片內部的邏輯閘以及連結外部的輸入/輸出介面之間的頻寬差距到達嚴重的比例。因此，連接晶片之間的傳輸通道時常限制了系統的效能，這些系統包括網路的切換器、路由器、處理器和記憶體之間的介面及多處理器的傳輸通道。

在此論文中，我們將簡單的介紹高速序列傳收機。我們提出一個可增強高頻區段訊號的預先增強電路，使資料在接收端能在操作頻率下維持一定值。接著，我們再加上自我校正功能，可以對輸出電壓準位做自動的調整，以防止製程漂移或溫度變化而造成輸出準位的誤差。再者，我們可以決定近端電阻與驅動電路的等效阻值使其輸出阻抗接近 50 歐姆，進而減少反射所造成的影響，實現此電路技術及設計概念也將再論文中說明。

論文中，我們將實現一個符合低電壓差動訊號標準 3.125 Gbps 的傳送器。此傳送器是使用台積電 0.18μm CMOS 製程製作且在 1.8V 的供應電壓下其功率消耗為 50 毫瓦。

關鍵字: 高速串列鏈結，低電壓差動訊號標準，預先增強，自我校正

A Self-Calibrate Driver with Pre-Emphasis

Student: Kuan-Yu Chen Advisor: Chau-Chin Su

Department of Electrical and Control Engineering

National Chiao Tung University

Abstract

Due to the scale-down of the process technologies, the operating frequency and circuit complexity of CMOS VLSI increase significantly. The growing gap between on-chip and off-chip I/O bandwidth is reaching the critical proportions. Therefore, the interconnections between chips often limit the performance of a system in applications such as network switches, routers, processor-memory interfaces, and multi-processor interconnects. For this reason, to integrate high speed serial links on chips can reduce the pin/wire count and power budget of a system significantly.

In this thesis, we will introduce a high-speed serial link. We will propose the pre-emphasis circuit that can enlarge the high frequency components, so the overall frequency response at the receiving end is uniform across the operation frequency. Then we add the self-calibration function to our driver so that it can calibrate itself automatically to deal with process or temperature variation. In order to reduce the reflection effect, we can determent the termination resistor value of near end and the equivalent resistors of the driver to make these resistors be equal to 50Ω in steady state. The circuit design will be described in detail.

In this thesis, a 3.125 Gbps transmitter has been designed. It is compatible with the LVDS standard. In a TSMC 0.18-μm 1P6M CMOS technology, the transmitter circuit consumes 50mW on a 1.8V power supply.

Keyword: High-speed serial link, LVDS, Pre-emphasis, Self-Calibrate

致　謝

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最後當然是要感謝我的家人-父親、母親、姐姐和弟弟，沒有他們在背後的鼓勵，也不會有今天的我，在此表示最誠心的感謝，感謝他們也感謝我生命中所有的人。

陳冠羽
2005/7/27

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Chapter 1

Introduction

1.1 CMOS High-Speed Serial Links

Traditionally, high-speed serial links in Gbps range are implemented in GaAs or bipolar technologies. The primary advantage of those technologies is the faster intrinsic device speed (higher f_T). However, CMOS technology is more widely available and allows higher integration than other technologies. Recently development has shown that CMOS is capable of achieving Gbit/s data rate[1,2]

Another motivation for CMOS implementation is the faster improvement of CMOS speed than the speed of other technologies due to the rapid scaling of it feature sizes. 0.18 μm CMOS technologies have speed comparable to a 0.5um GaAs technology. Although it is always possible to yield inherently better devices in non-transitional technologies, the momentum and investment in CMOS technology development is progressing toward making CMOS the fastest technology[3].

The standards for high-speed link are either over short distance in copper cable or long distances in optical fiber. The high bandwidth is provided by optical fiber over a lot long distances. But the optical fiber and necessary components also cost a lot. The optical links are not the only solution for high-speed communication over long distances. It is cheaper solution for high-speed communication to use cooper cables to replace optical fiber. But the length limits the bandwidth of cooper cable. Hence, cooper links, which are focus of this thesis, are usually used for short distance application, such as system-to-system interconnections in same room[4].

A typical link is comprised of three primary components: a transmitter, a channel, and a receiver. The transmitter converts digital bits into a signal stream that is propagated on the channel to the receiver. The receiver converts this analog signal back into binary data. Figure 1.1 shows the configuration.

Figure 1.1 Basic link components: the transmitter, the wire, and the receiver

A transmitter sends the data as analog quantities. The analog values are simply either a HIGH-level or LOW-level to represent a single bit, known as non-return-to-zero (NRZ). For example, in an optical system, they are the levels of different amounts of optical power. For electrical systems, these levels are of different signal voltages.

The channel is the medium where the data is propagated. This medium can be an optical fiber, a coaxial cable, an unshielded twisted-pair, a printed-circuit board (PCB) trace, or the chip package. Channel can attenuate or filter signal and introduce noise. It is difficult to overcome the attenuation and noise from the channel in transceiver design while transmitting high data rate.

To recover the signal from transmitter, the analog waveform is amplified and sampled. In order to recover the high-speed data, the receiver circuit has to be able to determine the high-speed small inputs from transmitter correctly. The time-recovery

circuit properly places the sampling strobe.

1.2 Motivation

Advances in IC fabrication technology have led to an exponential growth of the speed and integration levels of digital IC's. The bandwidth has increased the demand for higher inter-chip communication to maximize overall system performance.

There are two approaches to high-speed signaling, parallel buses and serial links. For parallel buses, many buses are implemented in a system to increase the signaling bandwidth. But the large buses increase the system e.g. cost, power consumption, and complexity. For serial links, it is to maximize the communication bandwidth and distance in a signal cable. Serial links offer a high-speed and low-cost solution to multi-gigabit per second rates over long distance. Applications such as computer-to-computer or computer-to-peripheral interconnection are several meters.

In this thesis, we will implement a system architecture which uses non-return-to-zero (NRZ) signaling techniques. A novel pre-emphasis circuit is proposed. A 3 Gbps transmitter with pre-emphasis to compensate loss of channels has been designed. A self-calibration function has been also implemented to compensate process and environmental variation.

1.3 Thesis organization

The thesis organization is described as follows:

Chapter 2: We will describe the basics of the high-speed link and channel analysis. We also introduce the basics concept of pre-emphasis.

Chapter 3: We will introduce the proposed transmitter architecture and explain the pre-emphasis method to overcome the limited channel bandwidth. We will also introduce self-calibration concept and algorithm in this chapter to deal with process variation.

Chapter 4: We will discuss the detail circuit design of the transmitter. Also, a novel pre-emphasis circuit and a self-calibration circuit are proposed. The implementation of the function blocks of the transmitter is also described in this

chapter. Finally the overall simulation results are summarized at the end.

Chapter5: The research is concluded in this chapter.

Chapter 2

Background Study

2.1 Signaling Techniques

This section describes two different approaches to high-speed signaling in digital systems. The first method is traditional high-swing signaling, such as TTL or CMOS. They have been used in most computer systems in the past years, especially for chip-to-chip communication. This conventional method limits the speed to 100MHz. The frequency is difficult to be scaled with improving process technology. As the speed in the modern digital system increases, the conventional method is, therefore, becoming a major bandwidth bottleneck.

The second method is discussed in this thesis. The point-to-point incident-wave signaling does not suffer from the limitation of the conventional method. So its data rate can be scaled with the process technology. The new signaling technique is emerging in high-speed systems due to the scaling.

2.1.1 Traditional Large-Swing Signaling

Traditional signaling systems are limited to data rates of about 100Mb/s per wire or less and dissipate large energy per bit transmitted and signaling rates do not scale with the improvement in the process technology. Many modern microprocessors operate their external buses at a small fraction of the internal clock rate due to the limitations. In traditional CMOS systems, a CMOS inverter is used both as the driver and receiver. The cable usually has a characteristic impedance of 50Ω to 100Ω. These signaling systems are slow because the high impedance driver is unable to switch the line voltage completely on the incident wave [5].

2.1.2 Point-to-Point Low-Swing Signaling

A signaling system that overcomes the limitations of traditional signaling is shown in Figure 2.1. A current-source transmitter drives the line with currents that

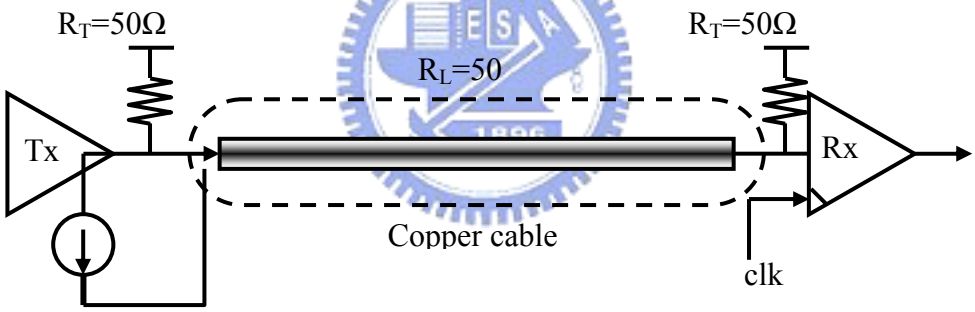


Figure 2.1 A point-to-point, low swing, incident-wave system

typically range from a couple of milliamperes to tens of milliamperes, resulting in a voltage swing range of 100mV to about 1V. The cable is terminated at both ends in its characteristic impedance. The receiver termination absorbs the incident wave, preventing any reflections. The source termination makes the systems more tolerant of crosstalk and impedance discontinuities.

A high-gain clocked regenerative receiver amplifier can be both low offset (~30-60mV) and high gain. With the improved receivers with low offset and high sensitivity, this system can operate reliably using very small swings. Therefore this signaling method also offers a considerable reduction in power dissipation of the system. The system described can also operate at data rates independent of the line

length. A new symbol can be driven onto the line before the previous symbol arrives at the receiver. This results in a system whose data rate, to a first approximation, scales linearly with the device speed[4].

2.2 Channel Loss

The approximate channel frequency response in dB accounting for both skin effect and dielectric loss is given by [5],

$$H(f,l)_{dB} = -(h_s \cdot \sqrt{f} + h_d \cdot f) \cdot l \qquad (2.1)$$

where l is the length of the channel, h_s and h_d are the skin effect and dielectric loss coefficients respectively.

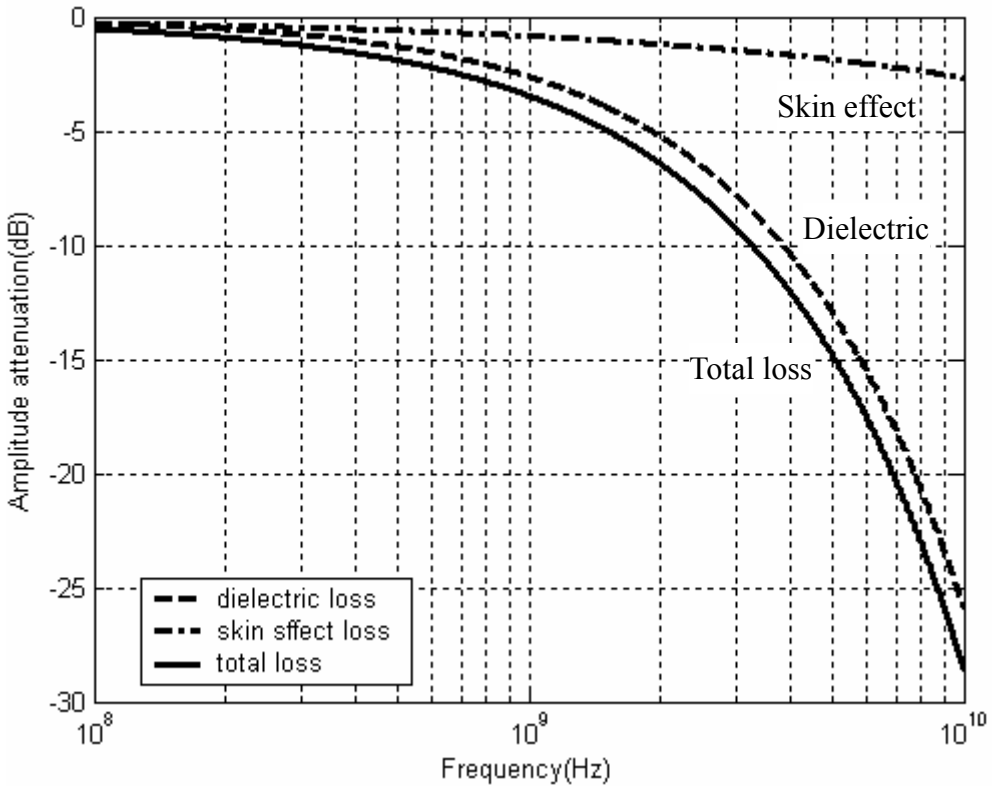


Figure 2.2 Frequency dependence of channel loss

Figure 2.2 shows the frequency response of a channel, with both skin-effect and dielectric loss components shown separately. The amplitude reduces 3 dB at 0.9 GHz.

Figure 2.3 shows the response of the channel for a 200ps 1V pulse with 50 ps rise time. The attenuation reduces the pulse amplitude by more than 30%. Moreover,

lower frequency attenuation results in the signal's long setting tail. The long setting tail can cause significant *inter-symbol interference* (ISI). When signal bandwidth above 0.9 GHz, a channel pre-emphasis or equalizer is needed in the transmitter or receiver [4]. The pre-emphasis or equalizer functions as a complementary high pass filter to counter the channel attenuation.

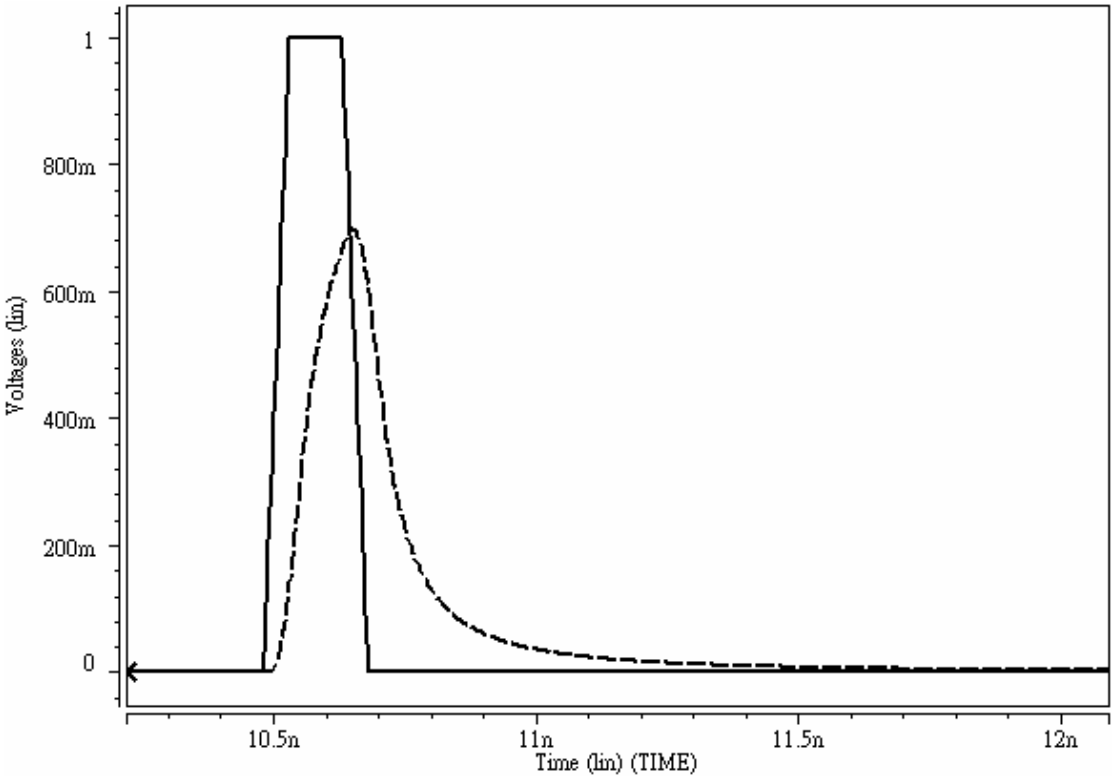


Figure 2.3 Pulse response of a 1.5-meter PCB trace

2.3 Transmitter Pre-emphasis

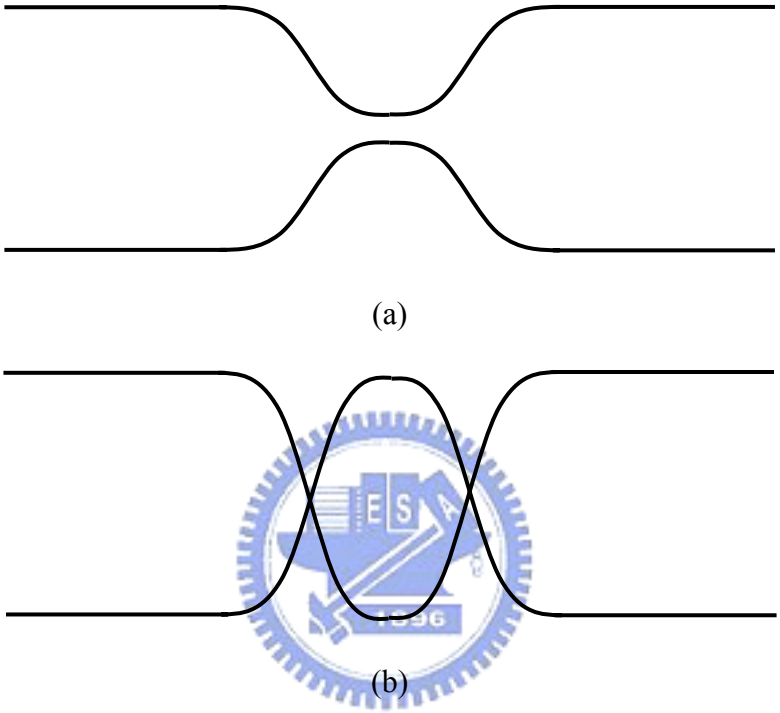
2.3.1 Transmit filter

Transmitter preshaping usually uses a symbol-space *finite impulse response* (FIR) filter integrated into the output main driver. It can be specified by the following equation:

$$V_0(n) = V_i(n) - a_1 \cdot V_i(n-1) - a_2 \cdot V_i(n-2) - ..... - a_N \cdot V_i(n-N) \qquad (2.2)$$

The inputs are the present and past transmitted symbols. The coefficients of the filter are dependent on the channel characteristics. The length of the filter N is

dependent on the number of past symbols which affect the present symbol. Hence, the output of the filter is the sum of the present symbol value and the past N symbols weighted value. Figure 2.4 (a) shows that there is no eye crossing because high frequency components are attenuated. We have to pre-shape signals in the transmitter to compensate for frequency response in order to get correct data. We can upper high frequency components to get good eye like Figure 2.4 (b).

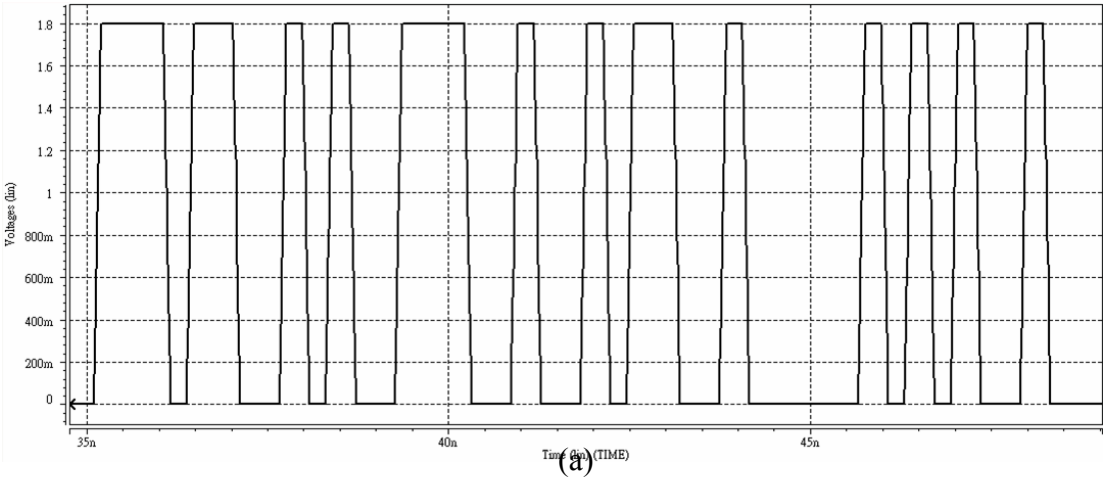


(a)

(b)

Figure 2.4 Signaling waveform (a) Without pre-emphasis (b) With 1-tap pre-emphasis

Figure 2.5 shows the injury to signals cause by channel loss and compensated by 1-tap pre-emphasis. The received voltage height is reduced by a channel with small loss. Hence, the goal of the pre-emphasis is to overcome channel loss effect.



(a)

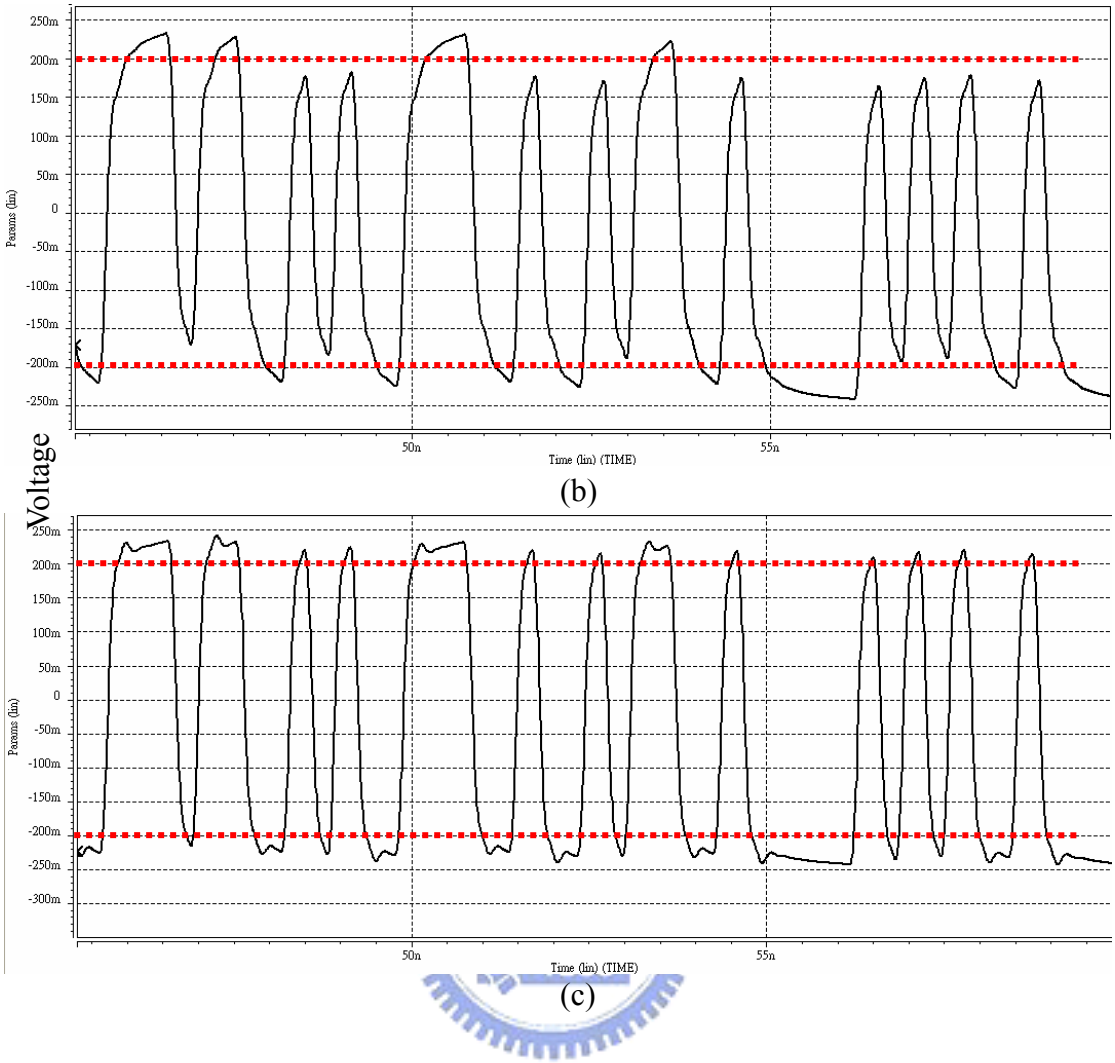


Figure 2.5 (a) The input signal in transmitter, output signal in receiver (b) with channel loss effect, (c) with 1-tap pre-emphasis

2.3.2 Design Techniques of Pre-emphasis

The first implementation of a N-tap transmit filter was implemented by Dally and Poulton [10]. In this architecture, all the FIR filter calculations are done by digital adders and a digital-to-analog converter (DAC) generates the output pulse. The architecture of this approach is shown for 5-tap filter in Figure 2.6. Driver parallelism is used to overcome the speed limitations of the process. The digital logic modules which have the present and the five previous bits calculate the amplitude of the current pulse that should be transmitted and each driver module is a 6-bit DAC to reduce the quantization error of the FIR filter This implementation incorporates a 4GHZ FIR pre-shaping filter into a differential transmitter and allows a serial channel to operate over copper wires a 4Gbps.

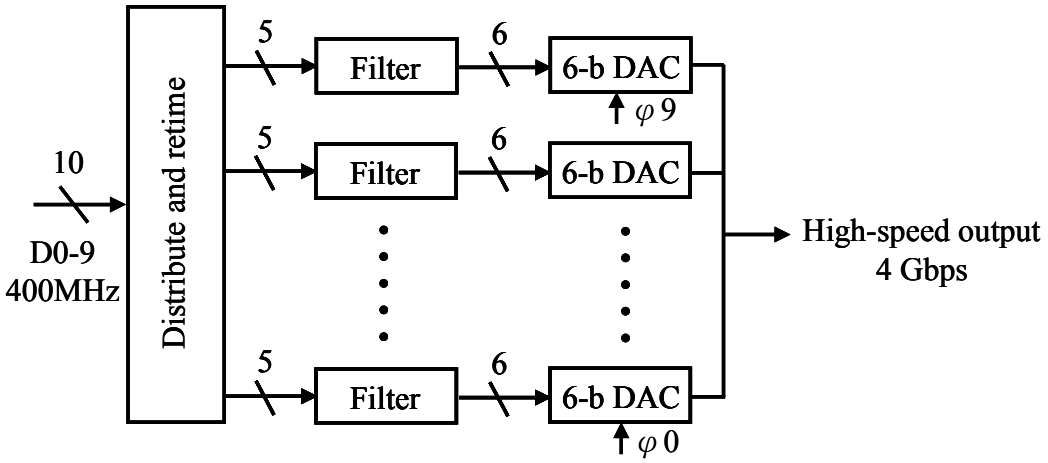


Figure 2.6 Block diagram of a preshaping parallel transmitter for MIT group [10]

The second implementation shows in Figure 2.7 with completely analog technique to realize the pre-emphasis filter. In this technique, the FIR N-tap filter is integrated into each driver module of the parallel transmitter. Each module uses the present and N previous bits to generate the complete preshaped pulse over N+1 bit periods directly and independently of all previously transmitted symbols. The individually preshaped symbols are summed at the transmitter output in an analog fashion. This implementation has 4-PAM pre-emphasis driver, and it can achieve 10Gbps over a pair of 10-meter PE142LL coaxial cables.

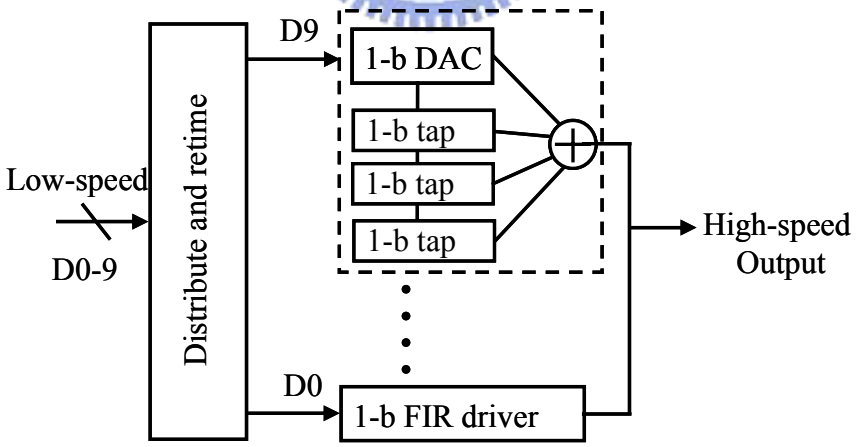


Figure 2.7 Block diagram of a pre-shaping parallel transmitter for Stanford group [4]

The third implementation shows in Figure 2.8. Pre-emphasis is implemented with the help of two auxiliary DACs (NDAC and PDAC). While active, PDAC generates a current proportional to the present symbol value. Similarly, NDAC generates a current of opposite polarity, proportional to the previous symbol. In this way, a pre-emphasis pulse is generated that is proportional to the change in the

transmit code, but without any digital computation. The reference current for NDAC and PDAC, as well as the pre-emphasis pulsewidth are programmable. The magnitude of the pre-emphasis current can be increased to compensate for greater attenuation over longer channels. This allows the transceiver to communicate over a range of track and cable lengths.

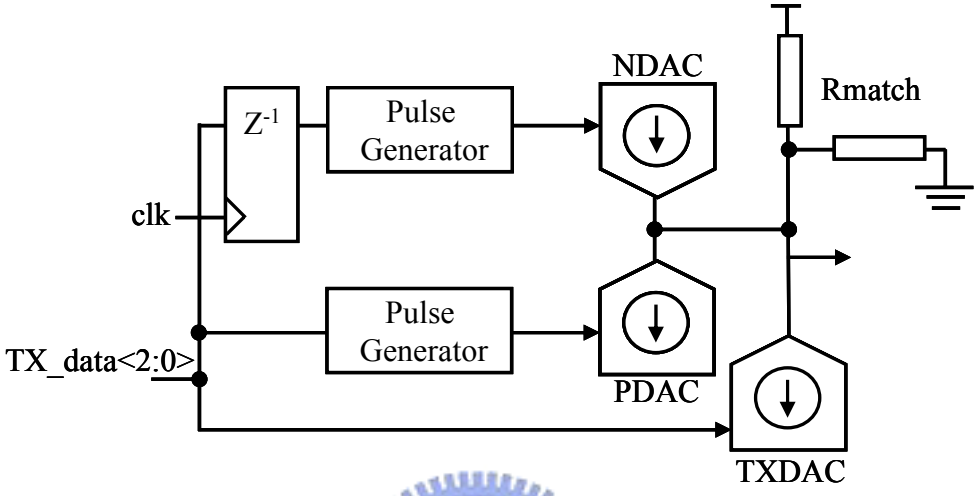


Figure 2.8 Transmitter block diagram [9]

Chapter 3

The Transmitter Architecture

3.1 Introduction

This chapter describes the proposed transmitter for a 3.125-Gbps serial link. This architecture contains a single to differential buffer, a controlled pre-driver module, a main driver, a self-calibrate mechanism, and a pre-emphasis module. In Figure 3.1, the multiplexer select Vdd or data to send to single-to-differential buffer which converts single ended data to differential ones. The top signal path is for pre-emphasis driver, the bottom one is for calibration driver and the middle one is for main driver. The top signals pass to the transition detector to detect whether signals transit or not. The transition detector decides to emphasize signals with transitionl. Besides, the output level is not guaranteed to have an expected voltage level due to the process variation or layout mismatch. So the controllable LVDS drivers can increase the output driver current to compensate the output voltage swing through the calibration driver as shown in Figure 3.1.

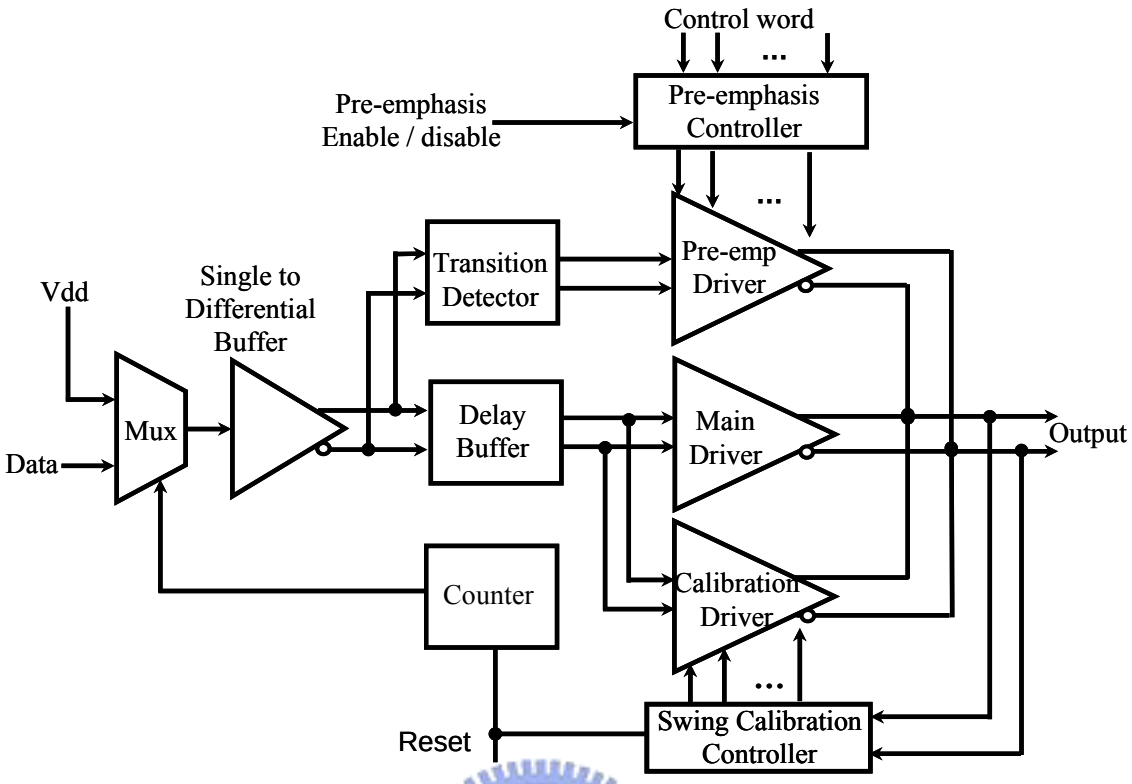


Figure 3.1 The overall transmitter architecture

The swing calibration controller is the *finite state machine* (FSM). The FSM control the compensated driver by another digital circuit (shift register). When output voltage is detected, the FSM calculates and controls the shift-register to decide compensation current. The self-calibration feedback does not always work all the time. When the transmitter is in the calibration mode, the input is always connected to Vdd. When the transmitter is in the data transmission mode, the multiplexer will switch the input to the data. We use a slow counter to change mode when the counter counts a pre determined period of time.

3.2 Functional Blocks

We will discuss the important functional blocks in this section.

3.2.1 Pre-Emphasis Module

As described in chapter 2, the transmission line is a low pass function. Pre-emphasis circuit plays a role of high pass function so that the frequency response is flatten within the bandwidth of our desired frequency range in the receiver. This

frequency response can be written as

$$H_c(f) \cdot H_{pre}(f) = constant \quad f \geq f_{op} \quad , \tag{3.1}$$

where $H_c(f)$ is the channel frequency response, $H_{pre}(f)$ is the pre-emphasis frequency response and f_{op} is the maximal operation frequency.

The pre-emphasis either amplify the high frequency component or attenuate the low frequency component as shown in Figure 3.2 [8]. In the diagram, the dotted line means the overall frequency response.

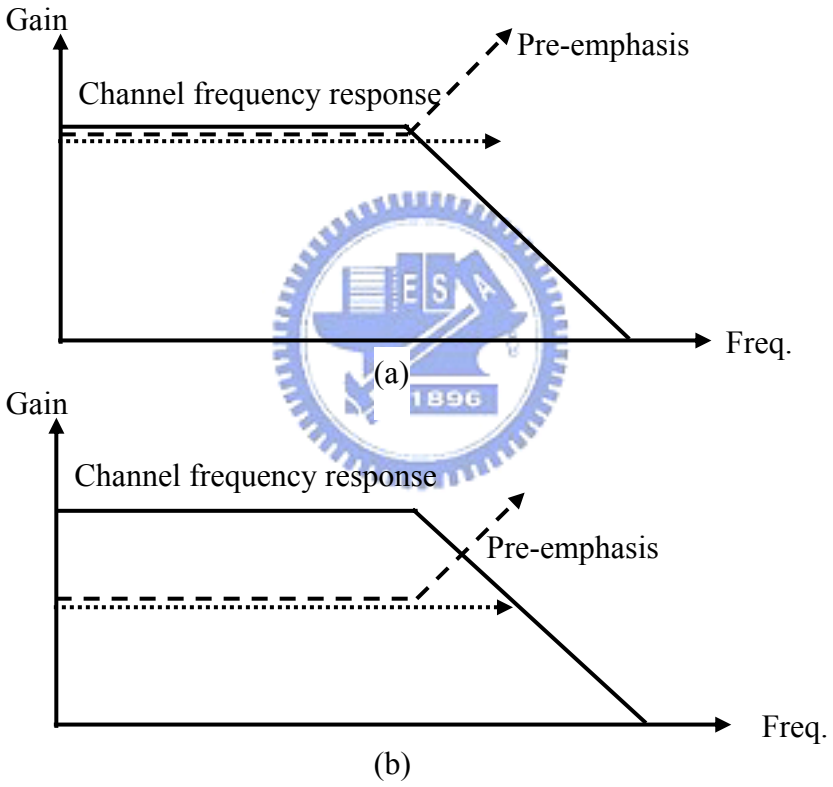


Figure 3.2 Frequency response, (a) the high frequency is amplified and (b) the low frequency is attenuated.

We use the scheme of Figure 3.2(a). The primary reason is that the low frequency component is attenuated and the voltage swing may not be large enough to recover data correctly at far end. This method increases the power of high frequency components. In order to increase the high frequency part, we can shape the transition of the signaling.

Traditionally, a tap of the pre-emphasis is a symbol space as shown in Figure 3.3 (a). The dashed line is the waveform of the receiver. There are some problems. We can not compensate the rising (falling) time and the steady state voltage level simultaneously. In many specifications, the rising (falling) time is requested. The first tap of the pre-emphasis decides the rising (falling) time. In order to reduce rising time in the receiver, the first tap has to increase more current to enhance the output voltage of the transmitter as shown in Figure 3.3 (b).

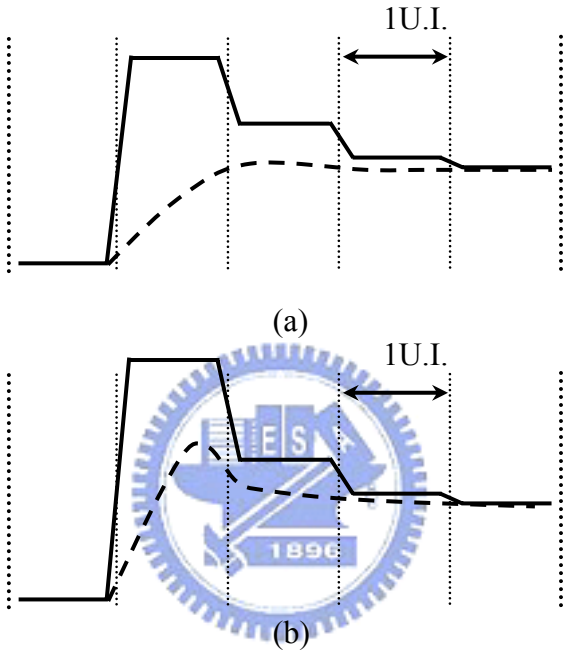


Figure 3.3 (a) The pre-shaped signal in the transmitter, (b) increasing current of the first tap

We can also see that there is an overshot waveform at far end. In the receiver eye diagram, the overshot waveform is the over compensation for steady state voltage level as shown in Figure 3.4(a). If we only compensate for steady state voltage level and no overshot waveform in the receiver, the rising time may not short enough to match the specifications as shown in Figure 3.4(b).

So we propose a new method to implement the pre-emphasis function as shown in Figure 3.5. A tap of the pre-emphasis which is only half symbol space is a feasible method to compensate for rising (falling) time and steady state voltage level simultaneously. If the first tap that controls the rising time is a symbol space, it may cause overshot waveform in the receiver. If we reduce it to half symbol space, the

overshot waveform is diminished and the rising (falling) time can be also compensate to match the specification.

In Figure 3.6, we can see that the overshot waveform is diminished in the receiver and the rising (falling) time can be easily controlled with increasing current by the first tap. Therefore, our new method of the pre-emphasis function is better than traditional one in overcoming the channel loss effect.

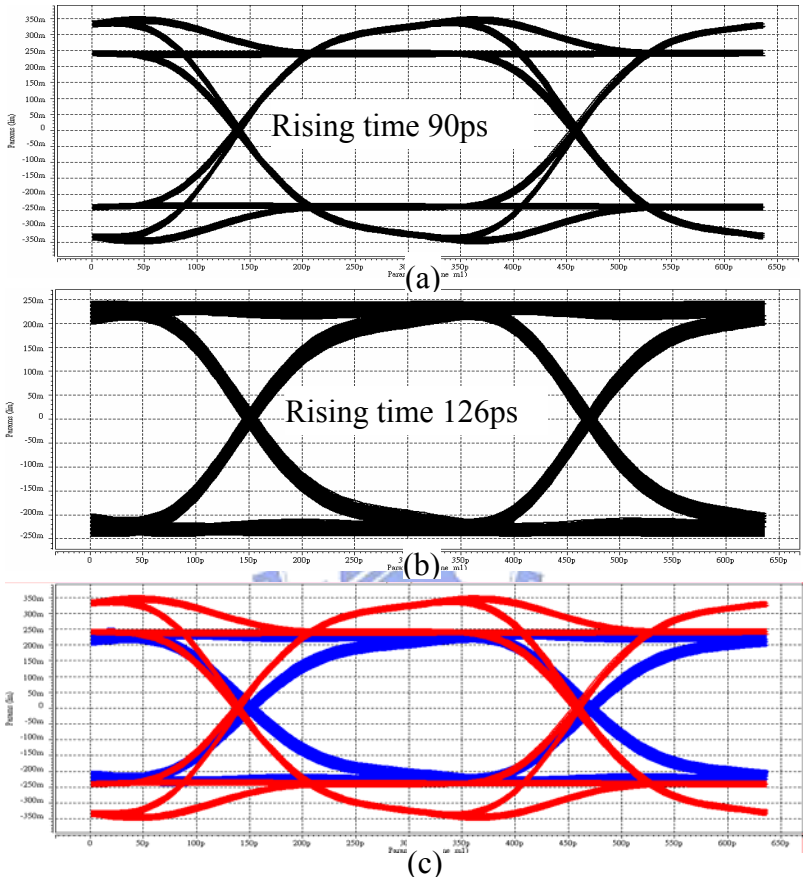


Figure 3.4 Eye diagram of the receiver, (a) over compensation for steady state with 1-tap of a symbol space (b) rising time is increased with non over compensation (c) comparison between (a) and (b)

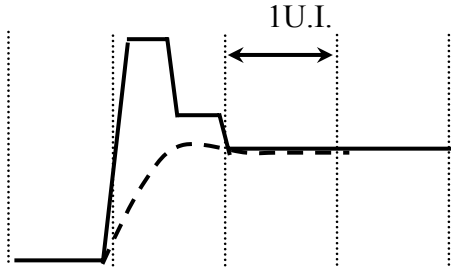


Figure 3.5 Proposed pre-emphasis function

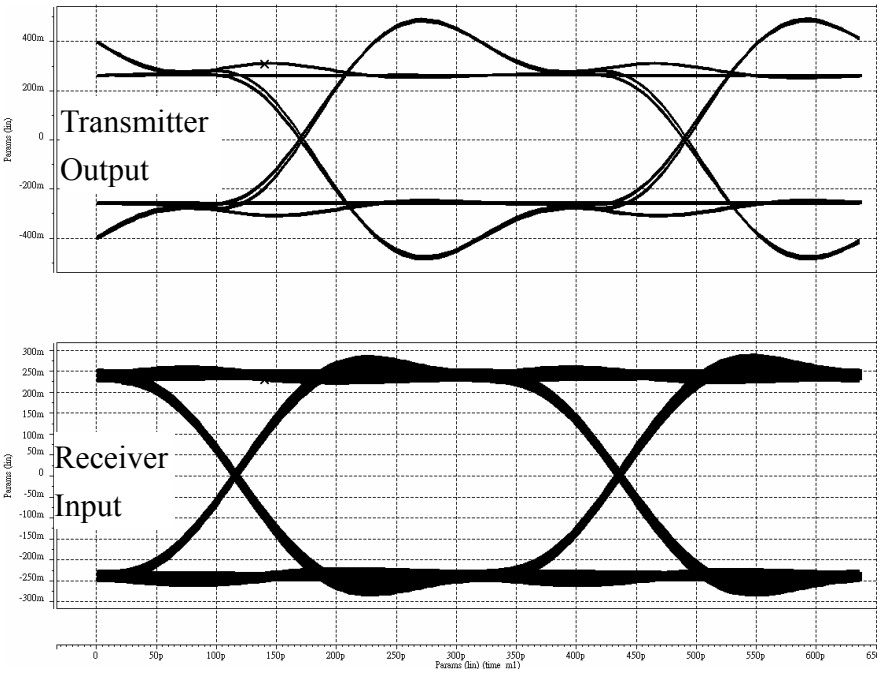


Figure 3.6 Eye diagram of the proposed pre-emphasis function

3.2.2 Pre-emphasis and Main Drivers

The architectures of pre-emphasis, main driver and calibration driver are almost the same. There is an advantage to implement by similar architecture. Because of the similar architecture, the pre-emphasis driver, main driver and calibration driver have the same delay time.

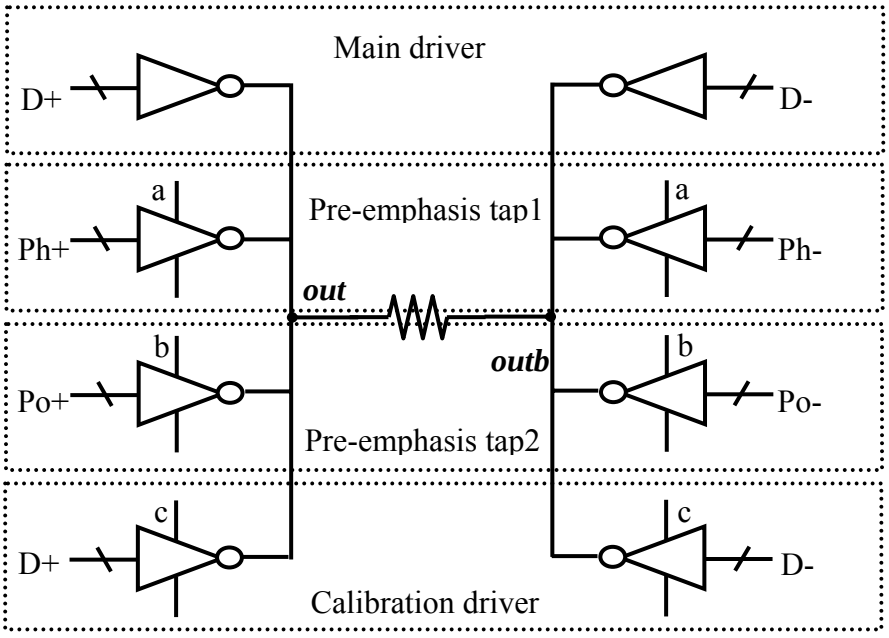


Figure 3.7 Driver architecture : main, calibration driver and pre-emphasis

The driver includes the circuit blocks of the main driver, calibration driver and pre-emphasis as shown in Figure 3.7. The strength of each tap is decided by channel length and channel loss. The relationship between current (I) and differential amplitude of the output of the transmitter (ΔV) is

$$\Delta V = I \cdot R_e \tag{3.2}$$

where R_e is the equivalent resistance.

From Equation (3-2). We know that the amplitude increases with current or R_e . In out system, R_e is constant because of the termination resistance. The main driver represents the circuit of the original driver, the calibration driver represents the calibration circuit to calibrate output voltage level (ΔV) and pre-emphasis represents the pre-shaping circuit to emphasize the high frequency components. The function of tap1 is shown in Figure 3.8. The circuit of tap1 operates when a data transition is detected and it supplies I_1 to enlarge ΔV .

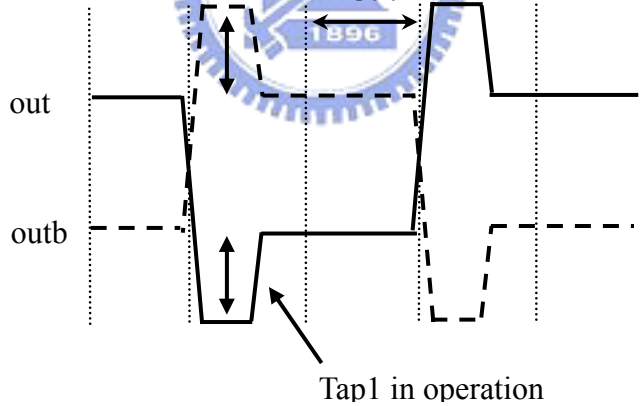


Figure 3.8 Signal waveform when Tap1 is operated

Tap1 is used to any transition and it only controls slew rate. So we need another tap to deal with the steady voltage level. Tap2 is essential in our design. Tap3 is required or not is determined by the receiver sensitivity, the area, and the loading overhead. In out system, if we have three tap, every tap is one third symbol space. It is a challenge to out design. So we only have two taps in our system. The function of the tap2 is shown in Figure 3.9.

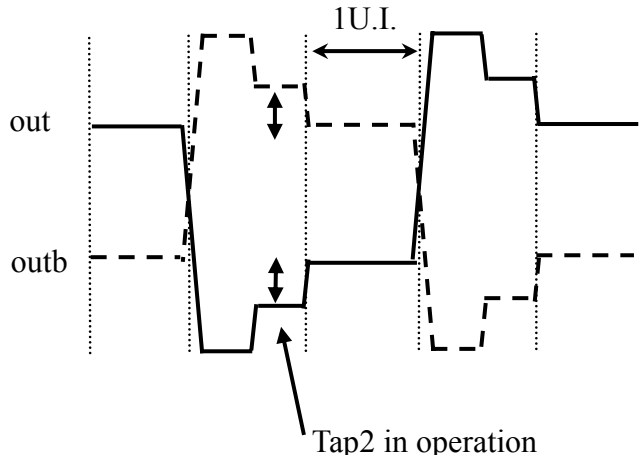


Figure 3.9 Tap2 function

Figure 3.10(a) is the simulation that only tap1 operates. We can see that the data is attenuated after transition. The tap2 circuit supplies enough current to compensate for attenuation as shown in figure 3.10(b).

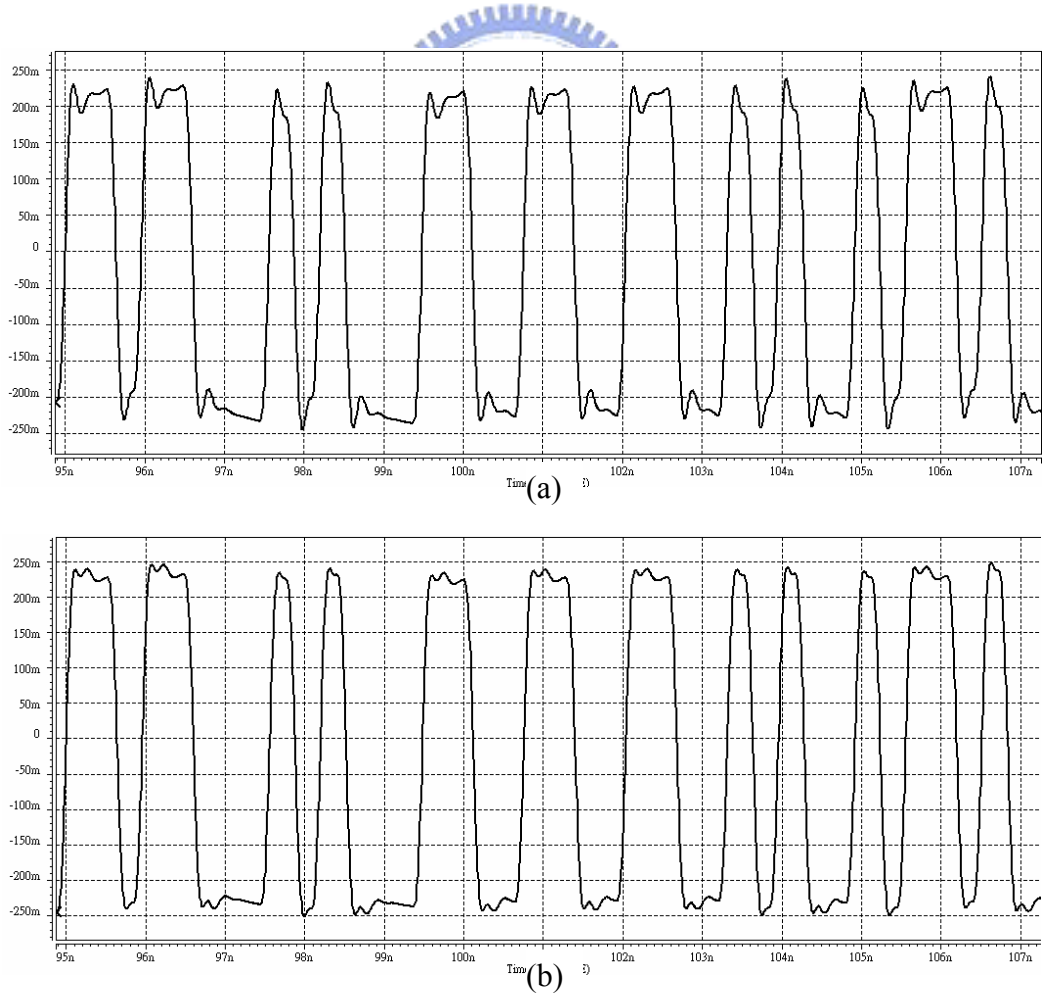


Figure 3.10 The simulation result in receiver end (a) only tap1 (b) tap1 and tap2

The calibration driver provides current in initial state to compensation the output amplitude according to FSM that we will discuss later.

3.2.3 Transition Detector

The transition detector detects data transition. When data has a transition, it sends a pulse to the pre-emphasis driver to make the pre-emphasis increases current to compensate attenuation as shown in Figure 3.11.

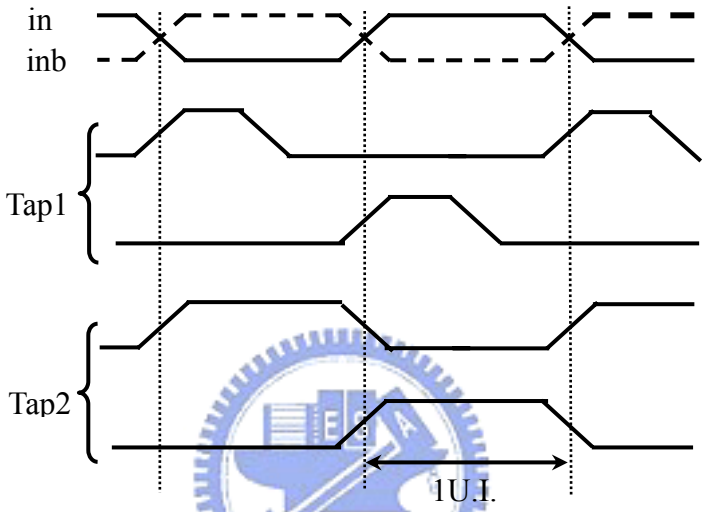


Figure 3.11 Transition detector function

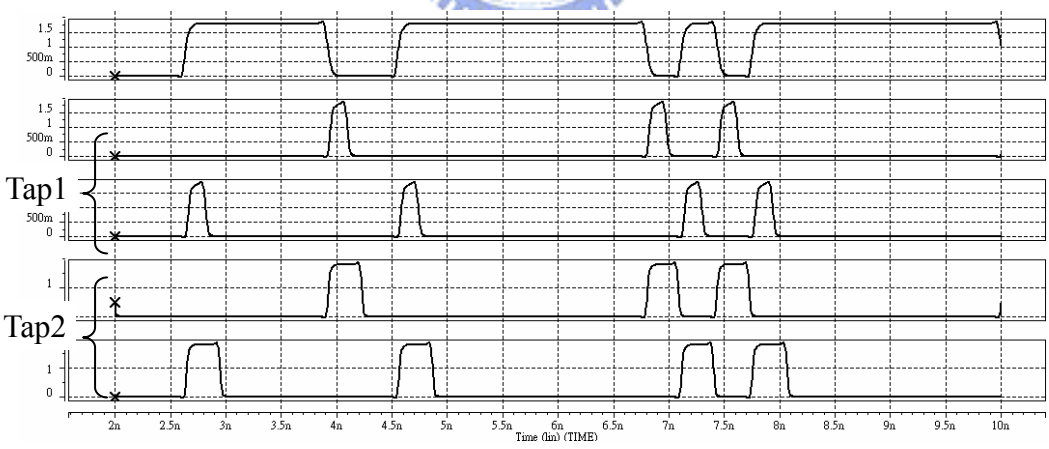


Figure 3.12 Simulation result of the transition detector

When data is from high to low or low to high, the transition detector produces two types of pulses for pre-emphasis and calibration as shown in Figure 3.12.

3.2.4 Swing Calibration Controller

In out system, the driver is like a voltage divider with resistors as shown in Figure 3.13.

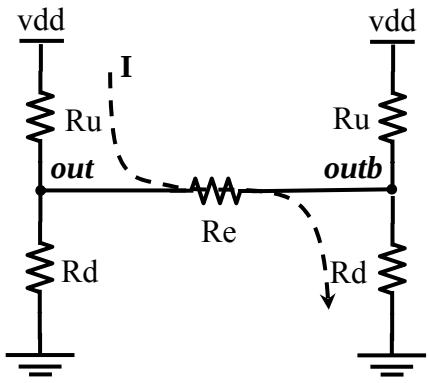


Figure 3.13 The driver equivalent model

In (3.2), the current (I) is equal to

$$I = \frac{vdd}{R_u + R_d + R_e}, \tag{3.3}$$

and (3.2) can be rewritten to

$$\Delta V = \frac{R_e}{R_u + R_d + R_e} \cdot vdd \tag{3.4}$$

We can write V_{out} and V_{outb}

$$V_{out} = \frac{R_d + R_e}{R_u + R_d + R_e} \cdot vdd$$
$$V_{outb} = \frac{R_d}{R_u + R_d + R_e} \cdot vdd \tag{3.5}$$

So when we change R_u and R_d, V_{out} and V_{outb} are both influenced at the same time. If the process variation happens, we can control and change R_u and R_d by parallel resistors. The FSM is needed here. This FSM can control how many resistors are parallel connected to guarantee the output swing. The state diagram of

FSM is shown in Figure 3.14.

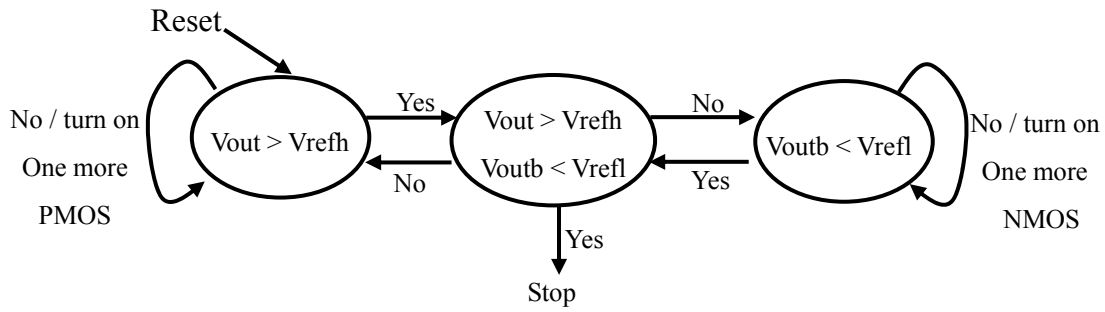


Figure 3.14 State diagram

In Figure 3.14, V_{refh} and V_{refl} are the reference voltages. V_{refh} is lower than V_{out}, and V_{refl} is higher than V_{outb}. So we can control the output amplitude by changing V_{refh} and V_{refl}. According to state diagram, we can plot our calibration curve as shown in Figure 3.15.

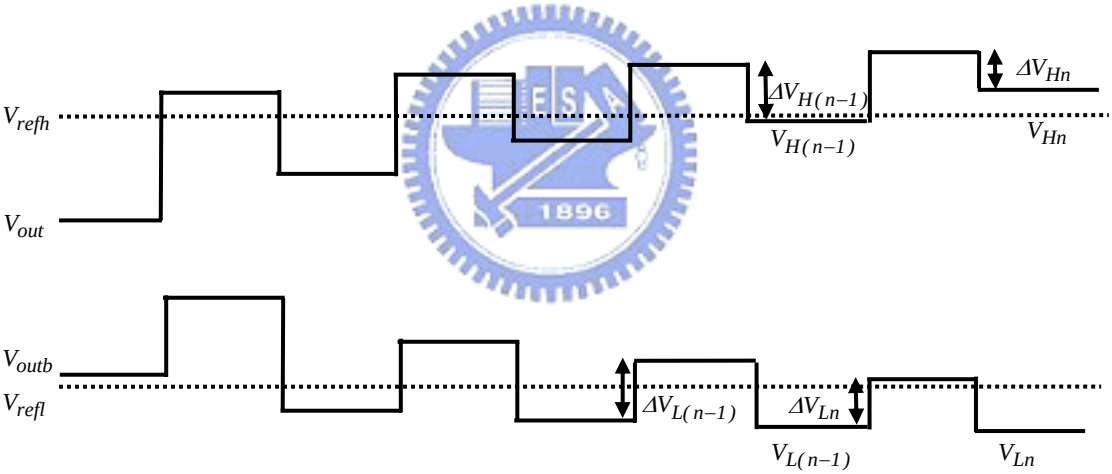


Figure 3.15 Calibration curve according to state diagram

How can we guarantee the algorithm to be convergent and calibrates the output voltages to the wanted levels by control the parallel resistors? If we can prove following equations (3.6), (3.7), and (3.8), we can say this algorithm is convergent because V_{out} and V_{outb} are monotonic increasing and monotonic decreasing.

$$\lim_{n\to\infty} V_{Hn} = V_{DD};\ \lim_{n\to\infty} V_{Ln} = 0 \tag{3.6}$$

$$V_{Hn} > V_{H(n-1)};\ V_{Ln} < V_{L(n-1)} \tag{3.7}$$

$$\Delta V_{Hn} < \Delta V_{H(n-1)}; \Delta V_{Ln} < \Delta V_{L(n-1)} \tag{3.8}$$

Where V_{Hn} is the nth voltage level of V_{out}, and V_{Ln} is the nth voltage level of V_{outb}. V_{Hn} and V_{Ln} are the voltages that are parallel connection with n resistors (R_{Hn} and R_{Ln}). R_{Hn} and R_{Ln} are

$$\begin{aligned} R_{Hn} &= \frac{R_a \cdot R_u}{n \cdot R_H + R_a}; \\ R_{Lm} &= \frac{R_b \cdot R_d}{m \cdot R_L + R_b} \end{aligned} \tag{3.9}$$

where R_a and R_b are the parallel resistors and n is the number of the parallel resistors. We can easily prove Equation (3.6) is correct.

$$\begin{aligned} \lim_{n\to\infty} V_{Hn} &= \lim_{\substack{n\to\infty \\ m\to\infty}} \frac{R_{Lm} + R_e}{R_{Hn} + R_{Lm} + R_e} \cdot V_{DD} = V_{DD} \\ \lim_{n\to\infty} V_{Ln} &= \lim_{\substack{n\to\infty \\ m\to\infty}} \frac{R_{Lm}}{R_{Hn} + R_{Lm} + R_e} \cdot V_{DD} = 0 \end{aligned} \tag{3.10}$$

Afterward we will show that Equation (3.7) is correct. In Figure 3.15, V_{Ln} and $V_{L(n-1)}$ are given by

$$\begin{aligned} V_{Ln} &= \frac{R_{Ln}}{R_{Hn} + R_{Ln} + R_e} \cdot V_{DD} \\ V_{L(n-1)} &= \frac{R_{L(n-1)}}{R_{H(n-1)} + R_{L(n-1)} + R_e} \cdot V_{DD} \end{aligned} \tag{3.11}$$

We can suppose that R_u is equal to R_d and R_a is equal to R_b and n is equal to m, so R_{Hn} is equal to R_{Lm}. This supposition makes calculation easily. We can get the Equation (3.12) after reduction

$$V_{L(n-1)} - V_{Ln} = \frac{(R_{H(n-1)} - R_H) \cdot R_e}{(R_{H(n-1)} + R_{L(n-1)} + R_e) \cdot (R_{Hn} + R_{Ln} + R_e)} \cdot V_{DD} > 0 \tag{3.12}$$

And in the same way, we also show that $V_{H(n-1)}$ is greater than V_{Hn}. So we prove Equation (3.7) is correct.

Then we will discuss Equation (3.8). ΔV_{Hn} and $\Delta V_{H(n-1)}$ in Figure 3.15 are the differences between high level and low level of V_{out}. They are given by

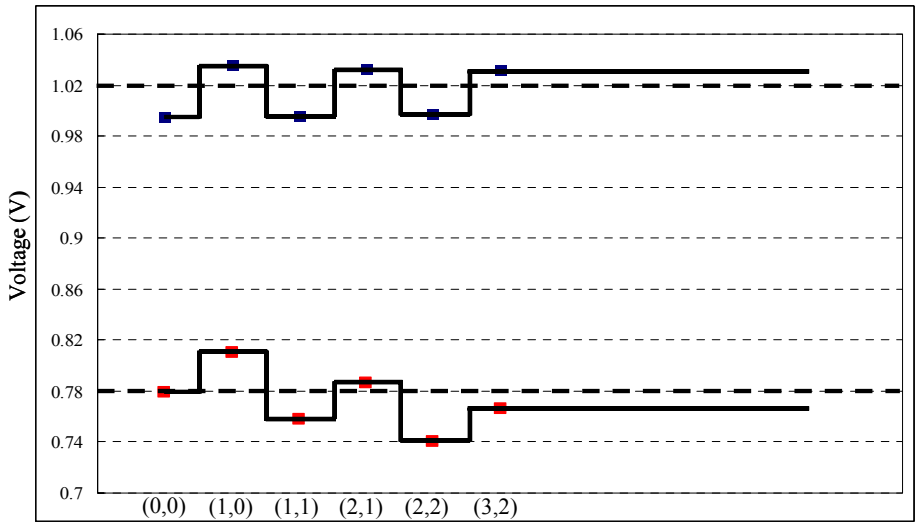
$$\Delta V_{Hn} = \frac{(R_{L(n-1)} - R_{Ln}) \cdot R_{Hn}}{(R_{Hn} + R_{L(n-1)} + R_e) \cdot (R_{Hn} + R_{Ln} + R_e)} \cdot V_{DD}$$
$$\Delta V_{H(n-1)} = \frac{(R_{L(n-2)} - R_{L(n-1)}) \cdot R_{H(n-1)}}{(R_{H(n-1)} + R_{L(n-1)} + R_e) \cdot (R_{H(n-1)} + R_{L(n-2)} + R_e)} \cdot V_{DD} \quad (3.13)$$

If $\Delta V_{H(n-1)} - \Delta V_{Hn} > 0$, then $\Delta V_{H(n-1)} > \Delta V_{Hn}$. So we can get the below equation.

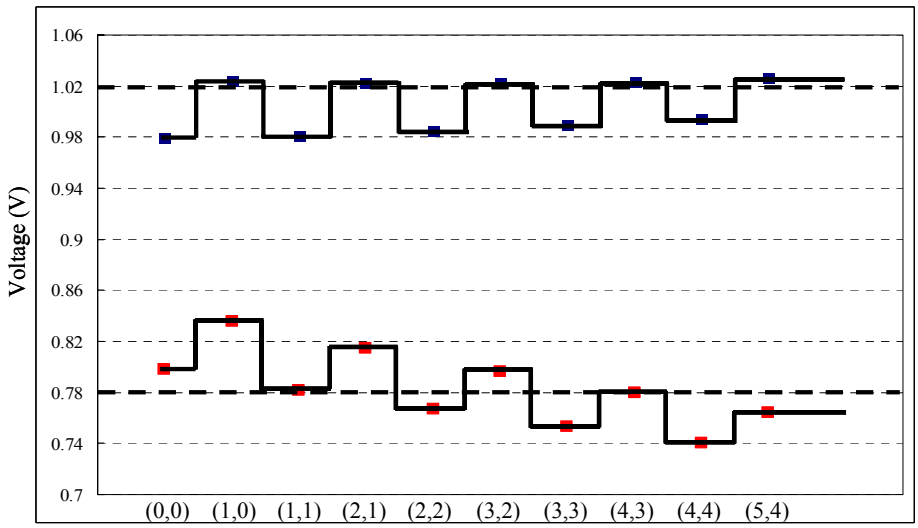
$$\Delta V_{H(n-1)} - \Delta V_{Hn} = \left(\frac{(R_{L(n-2)} - R_{L(n-1)}) \cdot R_{H(n-1)}}{(R_{H(n-1)} + R_{L(n-1)} + R_e) \cdot (R_{H(n-1)} + R_{L(n-2)} + R_e)} - \frac{(R_{L(n-1)} - R_{Ln}) \cdot R_{Hn}}{(R_{Hn} + R_{L(n-1)} + R_e) \cdot (R_{Hn} + R_{Ln} + R_e)}\right) \cdot V_{DD} \quad (3.14)$$

We can also suppose that R_u is equal to R_d and R_a is equal to R_b, so R_{Hn} is equal to R_{Ln} and n is equal to m. In this way, we can calculate easily. Because it is long and complex calculation, the reader can try to calculate and we do not show the process here. After reduction, we know that Equation (3.14) is greater than zero so $\Delta V_{H(n-1)}$ is greater than ΔV_{Hn}. And in the same way, we can show that $\Delta V_{L(n-1)}$ is greater than ΔV_{Ln}. Above the demonstration, we know that Equation (3.6), (3.7), and (3.8) are all correctly. So this algorithm is stable and convergent and V_{out} and V_{outb} are monotonic increasing and monotonic decreasing.

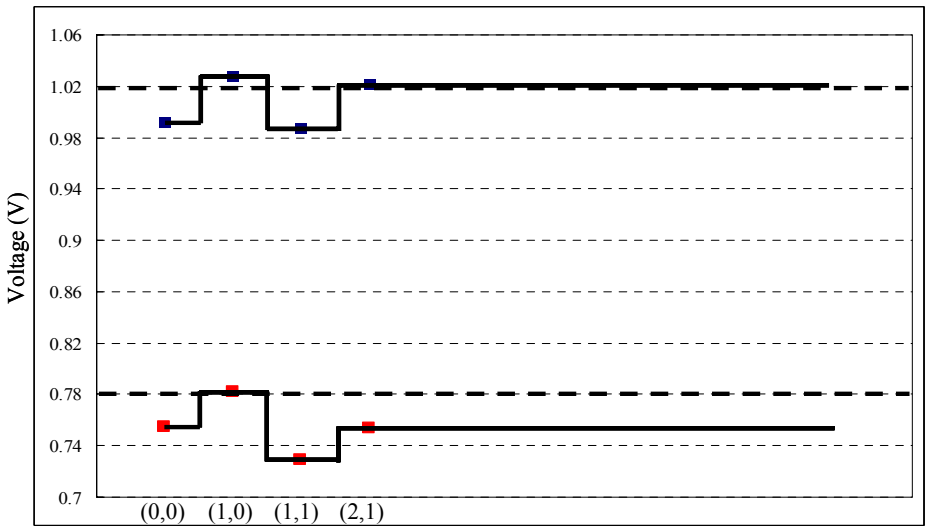
There are calculations by hand to demonstrate that this algorithm feasible. We get the values of R_u, R_d, R_a and R_b in spice simulation under all corner cases and plot calibration curves after calculation as shown in Figure 3.16. The reader may find FF case is mission. Because it matches the output voltage in initial state, the FSM will not operate calibration function.


1.06
1.02
0.98
0.94
0.9
0.86
0.82
0.78
0.74
0.7
Voltage (V)
(0,0) (1,0) (1,1) (2,1) (2,2) (3,2)
Number of parallel resistor (Ra,Rb)

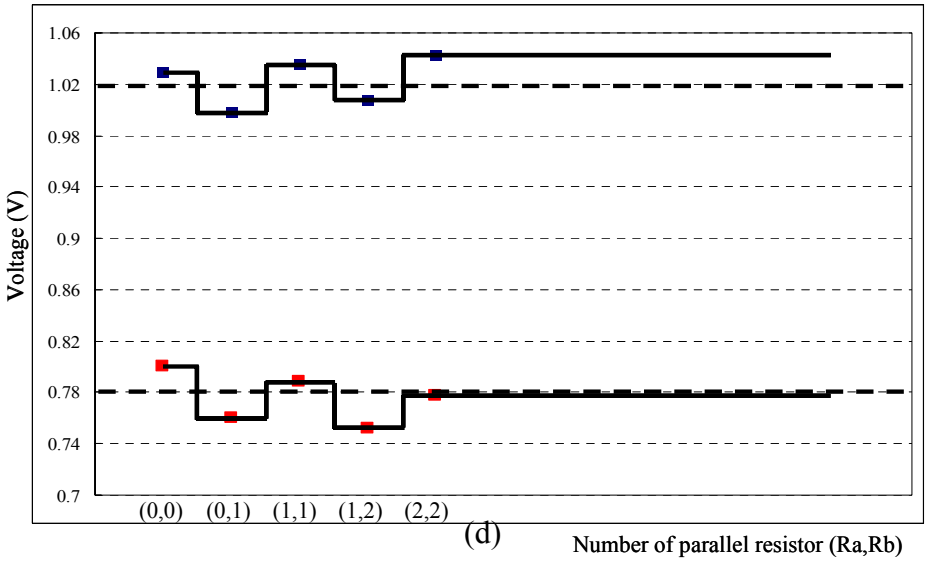
(a)


1.06
1.02
0.98
0.94
0.9
0.86
0.82
0.78
0.74
0.7
Voltage (V)
(0,0) (1,0) (1,1) (2,1) (2,2) (3,2) (3,3) (4,3) (4,4) (5,4)
Number of parallel resistor (Ra,Rb)

(b)


1.06
1.02
0.98
0.94
0.9
0.86
0.82
0.78
0.74
0.7
Voltage (V)
(0,0) (1,0) (1,1) (2,1)
Number of parallel resistor (Ra,Rb)

(c)



(d)

Figure 3.16 The calibration curve (a) TT case (b) SS case (c) FS case (d) SF case

We will discuss some cases that can not be calibrated perfectly by this algorithm. Our driver is like a resistor system as shown in Figure 3.13. If R_u or R_d is less than R_{stable} (the resistor value for the desired level) in the initial state, what is happen in this status. Figure 3.17 shows the results of the above the problem. If R_u or R_d is less than R_{stable} in the initial state, then only one voltage of output will be calibrated and the other one will not be calibrated as shown in Figure 3.17 (a) (b)

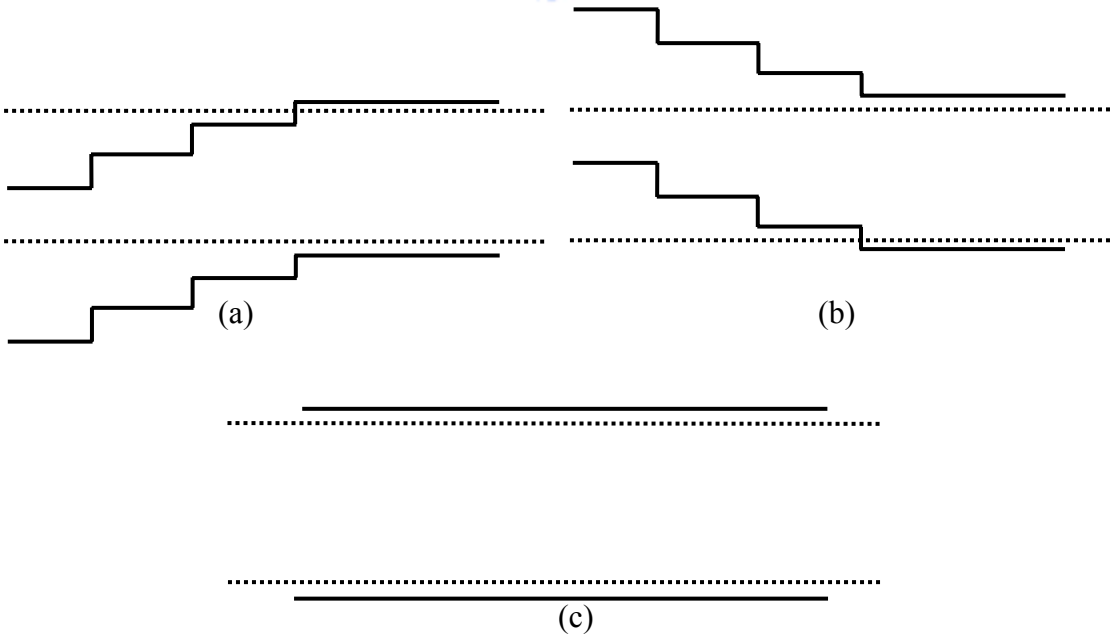


Figure 3.17 Cases that can not be calibrated (a) $R_d < R_{stable}$ (b) $R_u < R_{stable}$ (c) $R_u < R_{stable}$ and $R_d < R_{stable}$

The same status happens, when R_u and R_d are less than R_{stable} in the initial state. The calibration function does not work and the voltage levels of the output are determined by initial resistors as shown in Figure 3.17(c). When R_u and R_d are greater than R_{stable}, the FSM will calibrate both voltage levels of the output. This is an initial condition for this algorithm. Note that parallel resistor only increases and not decrease.

3.3 Summary

In this chapter, the architecture of the proposed transmitter is described. The pre-emphasis concept is introduced. In the next chapter, we will describe the detail circuit. The algorithm of calibration is proposed and proven that it is convergent. We will realize this algorithm by circuit in the next chapter.

Chapter 4

Transmitter Circuit Design

4.1 Introduction

This chapter will describe the detail circuit of the proposed architecture. The circuit includes the pre-emphasis transition detector, the output swing calibration controller, and the driver circuit. At the end of this chapter, the simulation results are given. We use the channel in SPICE to test and verify the proposed architecture. The frequency response of channel is shown in Figure 2.2.

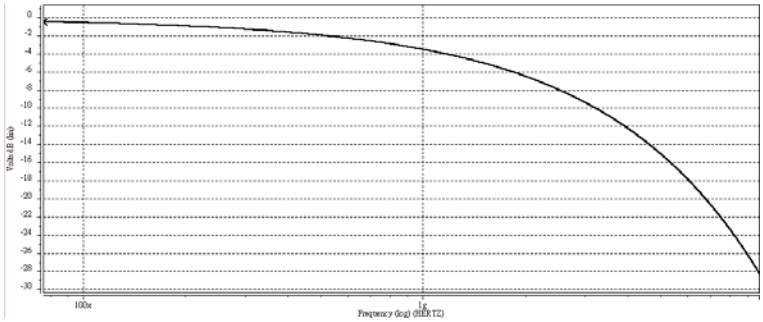


Figure 4.1 Frequency response of using HSPICE channel model

Figure 4.1 shows the frequency response using the HSPICE model. The characteristic impedance of the channel is $50\,\Omega$.

4.2 Circuit Design

4.2.1 Transition Detector

Chapter3 has described the function of the 2 taps pre-emphasis. Tap1 operates when there are data transitions. The tap1 detection block is as shown in Figure 4.2. We use latch to produce a data delay of half symbol space. Then this circuit provides opposite pulses by using NAND gate and NOR gate. $Pout_{1\text{-}0}$ and $Poutb_{1\text{-}0}$ send pulses when data transit from high to low and $Pout_{0\text{-}1}$ and $Poutb_{0\text{-}1}$ send pulses when data from low to high.

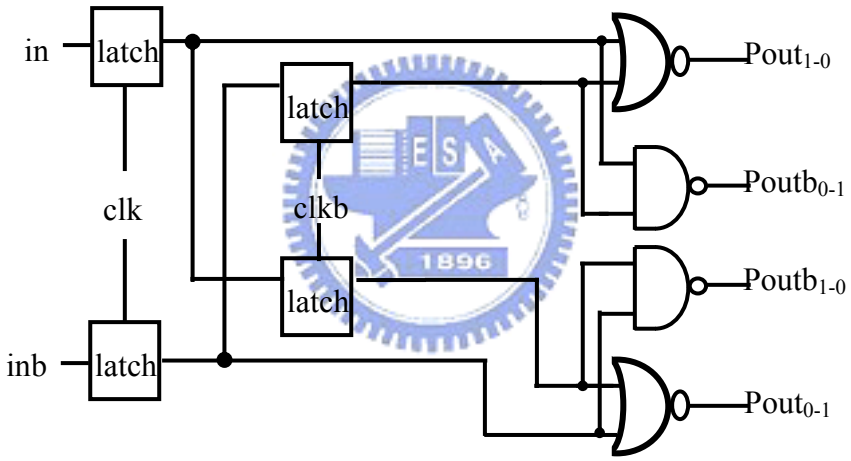


Figure 4.2 Tap1 detection circuit

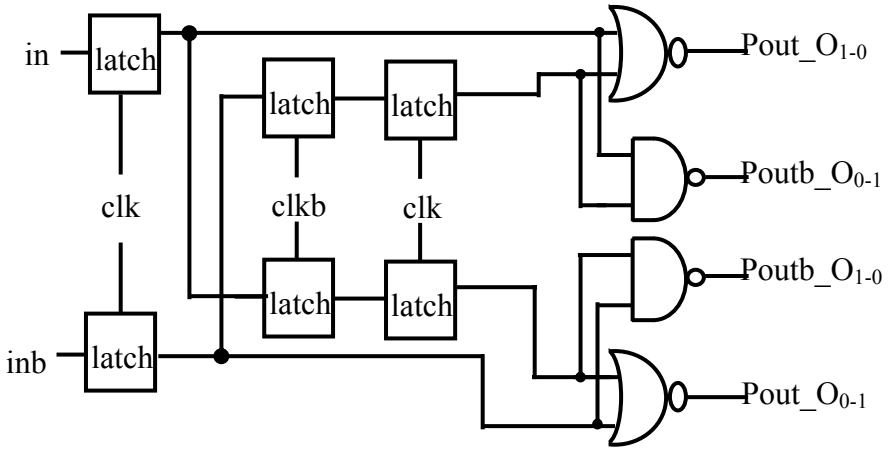


Figure 4.3 Tap2 detection circuit

The tap2 detection block is shown in Figure 4.3. Tap2 operates when there are data transitions and it maintains the voltage level of the output after tap1 is over. We also use latch to make delay and use logic gate to generate pulses. Pout_$O_{1\text{-}0}$ and Poutb_$O_{1\text{-}0}$ send pulses when data is from high to low and Pout_$O_{0\text{-}1}$ and Poutb_$O_{0\text{-}1}$ send pulses when data is from low to high. Note that the clock rate of the transition detector is the same as the data rate. For example, data rate is 3Gbps and the clock rate is 3GHz.

4.2.2 Swing Calibration Controller

Swing calibration controller is used to compensate voltage of the output due to process variation. This block includes FSM, a shift register, and comparators as shown in Figure 4.4.

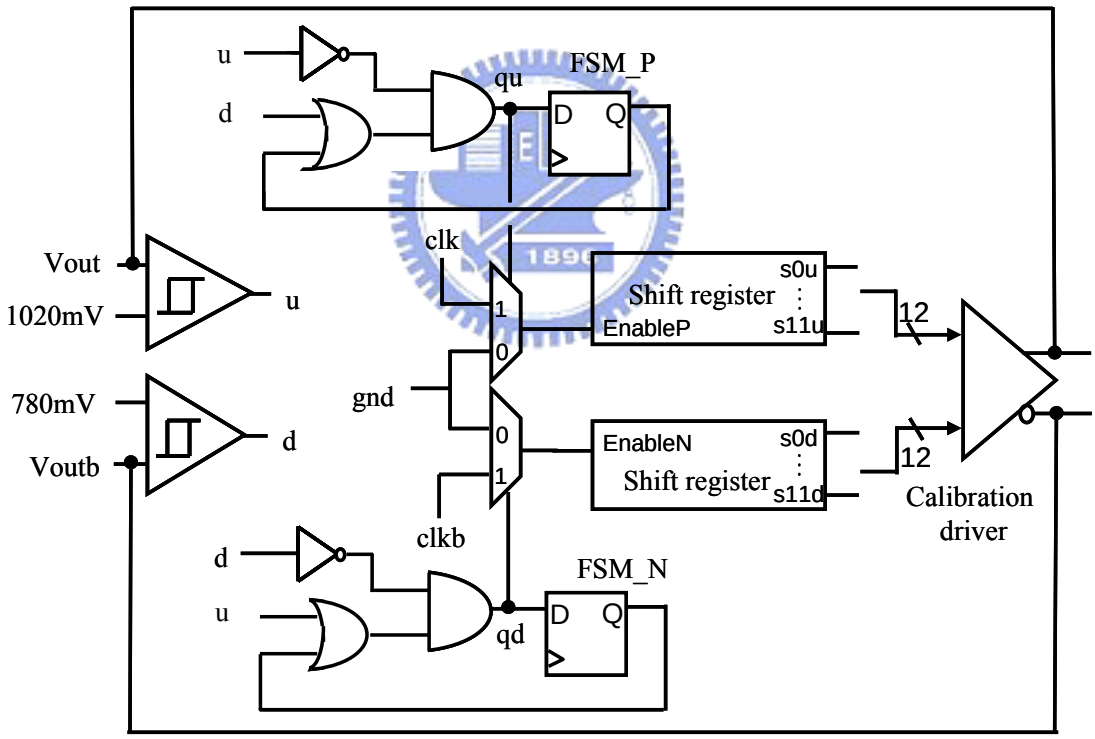


Figure 4.4 The architecture of the swing calibration controller

The source information of FSM is from the comparators. We use a simple two-stage operational amplifier to compare the output voltage and reference voltages as shown in Figure 4.5. Inverters are added to obtain digital outputs.

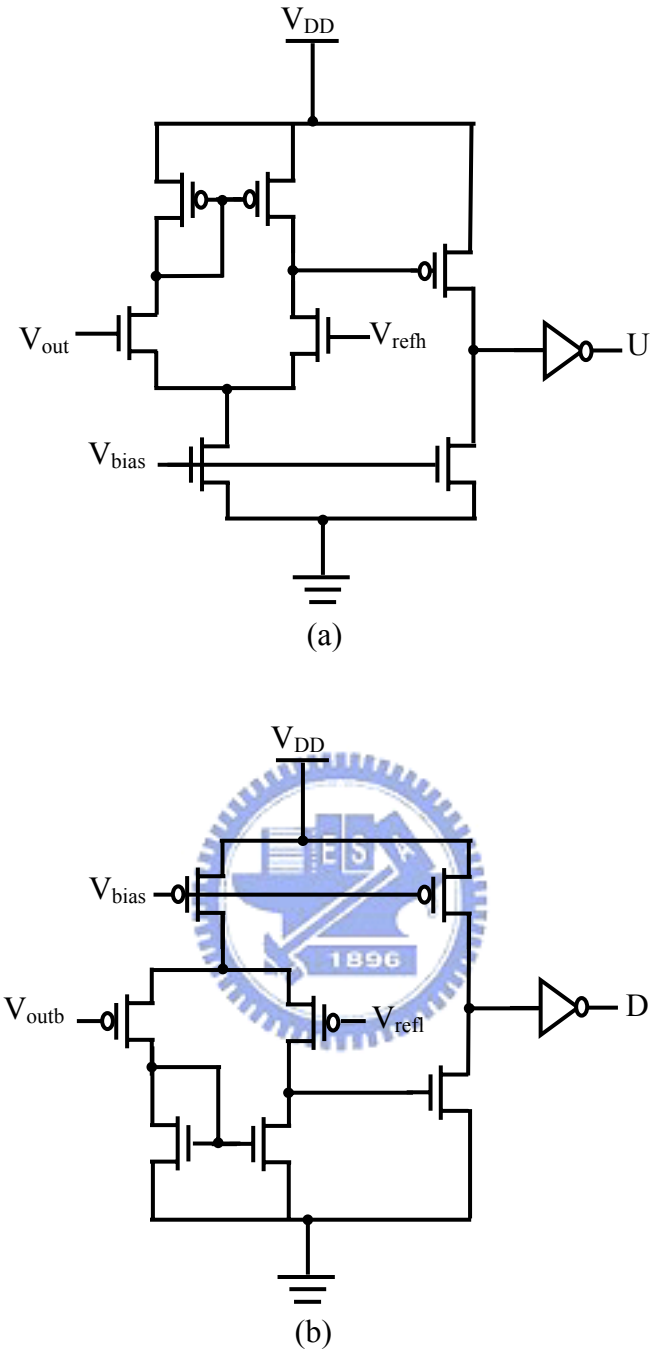


Figure 4.5 The comparator circuit (a) for higher output voltage (b) for lower output voltage

After the comparison with output voltage level and reference voltage, we have two digital outputs (U and D). When V_{out} is higher than V_{refh}, U is 1, otherwise U is 0. When V_{outb} is lower than V_{refl}, D is 1, otherwise D is 0. According to results of the comparators and Figure 3.14, we can find the truth table and equations of FSM as shown in Table 4-1.

Table 4-1 Truth table of FSM

u d q	qu	qd	Pmos	Nmos
0 0 0	0	0		setup
0 0 1	1	1	setup	
0 1 0	1	0		
0 1 1	1	0		
1 0 0	0	1		
1 0 1	0	1		
1 1 0	0	0	stable	stable
1 1 1	0	0	stable	stable

$$qu = \bar{u} \cdot (d + q)$$
$$qd = \bar{d} \cdot (u + q) \quad (4\text{-}1)$$

This calibration begins when there is a reset signal. V_{out} that is a higher DC voltage level is calibrated first, when calibration function operates. V_{out} is calibrated until u is one. It means V_{out} is higher than V_{refh}. When FSM calibrates V_{out}, we use qu to control the multiplexer to transmit clock to shift register. It makes shift register work. When qu is one, it means V_{out} is less than V_{refh} and we need to increase resistors to raise V_{out}. Increasing one resistor means the shift register shifts one to next. When qu is zero, it means V_{out} has been greater than V_{refh} and the shift register stops working and holds the value in the shifter register. When V_{out} is calibrates over, FSM begins to calibrate V_{outb} and it is the same process we describe the above-mentioned. But we use clkb to achieve. This way can reduce calibration cycle time. Two calibration functions will operate in rotation until qu and qd are all zero and calibration is over. It means V_{out} is greater than V_{refh} and V_{outb} is less than V_{refl}. Figure 4.6 shows the show the shift register. We can see that the shift registers always shift right. So the shift registers increase the number of one and do not reduce. The flip-flop of shift registers is the static type. We can not use the dynamic flip-flop, because after the self-calibration the output value of the D flip-flop must hold on itself forever.

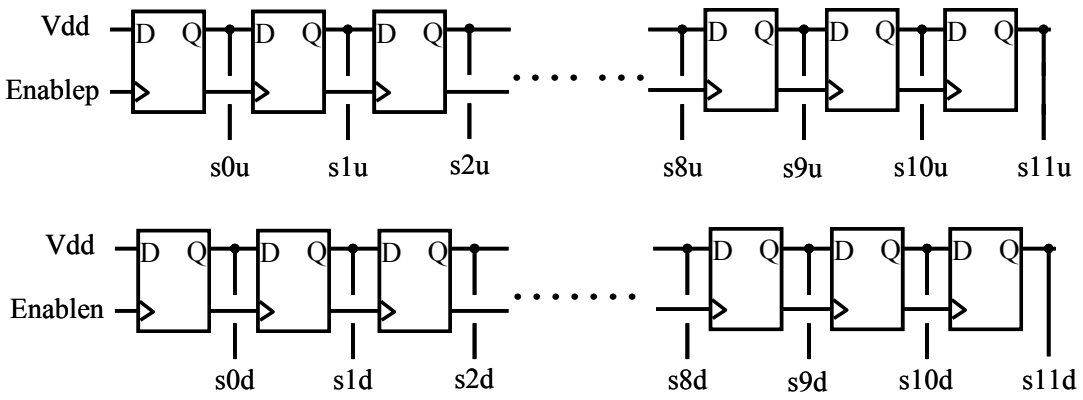


Figure 4.6 The shift registers

When calibration function operates, the reflection will happen. The reflection makes calibration function error and unlock as shown in Figure 4.7.

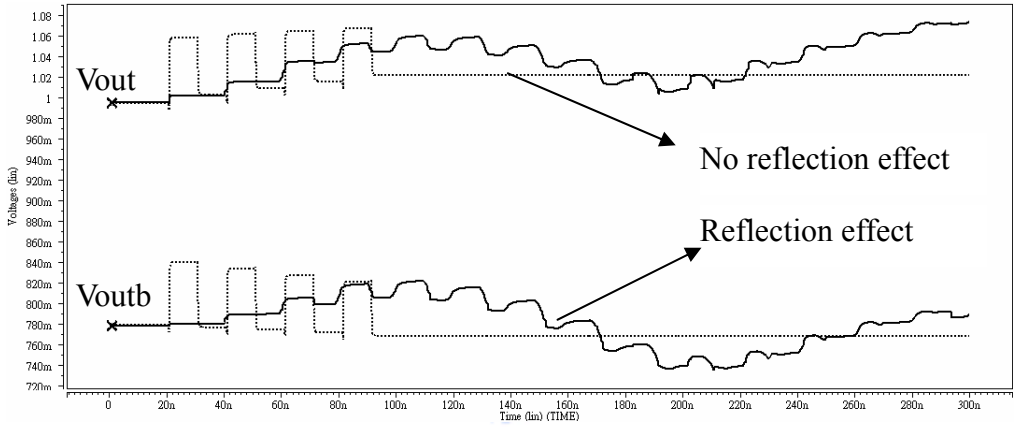


Figure 4.7 Reflection effect when calibration function operates

In order to solve this problem, we reduce the clock rate to wait for the reflection effect to disappear and sample the stable output as shown in Figure 4.8.

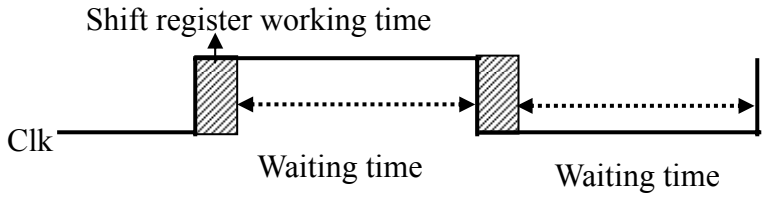


Figure 4.8 Solution of reflection effect

This solution has successfully solved the reflection effect. The simulation results as shown in Figure 4.9. When output voltage is stable, we send a pulse to EnableP (EnableN).

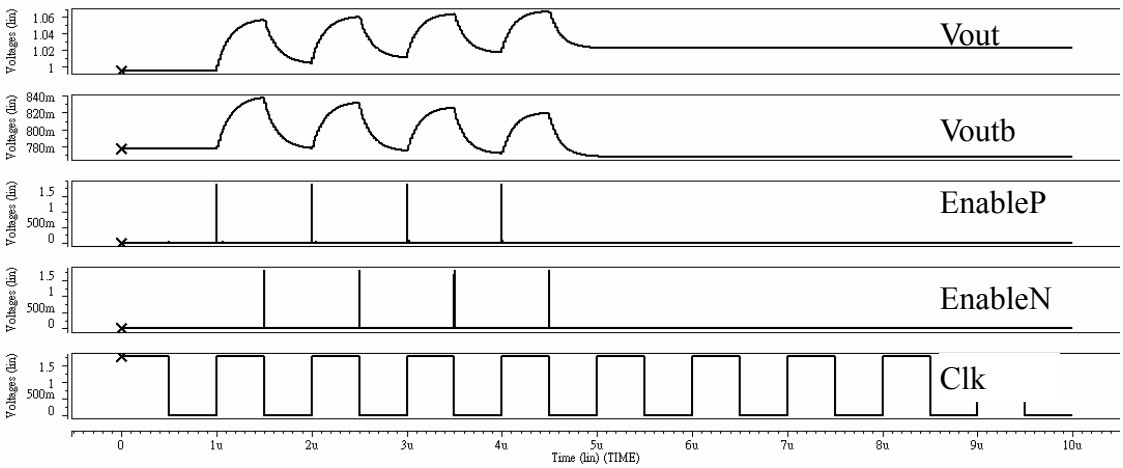


Figure 4.9 Simulation result of calibration which overcomes reflection effect

4.2.3 Counter

The counter is a simple block. The counter operates at low as kHz. So we choose the simple architecture shown in Figure 4.10. There are six D Flip-Flops and a NOR gate. D and Qb are connected to together so that D Flip-Flops become T-Flip-Flops. When the clock trigger, S1~S6 are triggered in sequence. After 16 clocks, Tx goes high, the calibration process ended and the driver starts sending data.

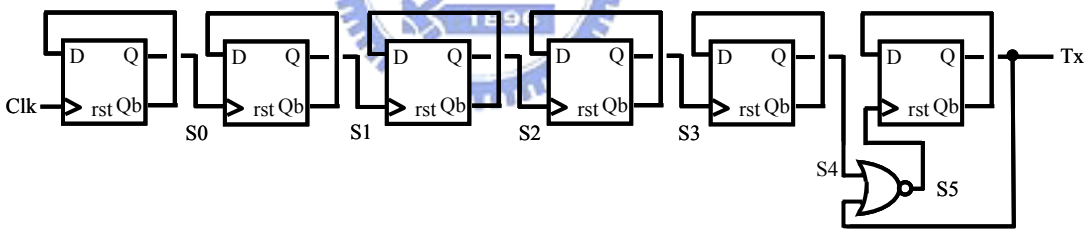


Figure 4.10 The architecture of the counter

Figure 4.11 shows the function verification of the counter above. After the reset, S0~S4 begin to count until S5 changes. Tx signal rise from LOW to HIGH and hold on until the next reset. We use this counter to decide when the transmitter to transmit or do self-calibration. Tx signal presents the operation mode of our transmitter.

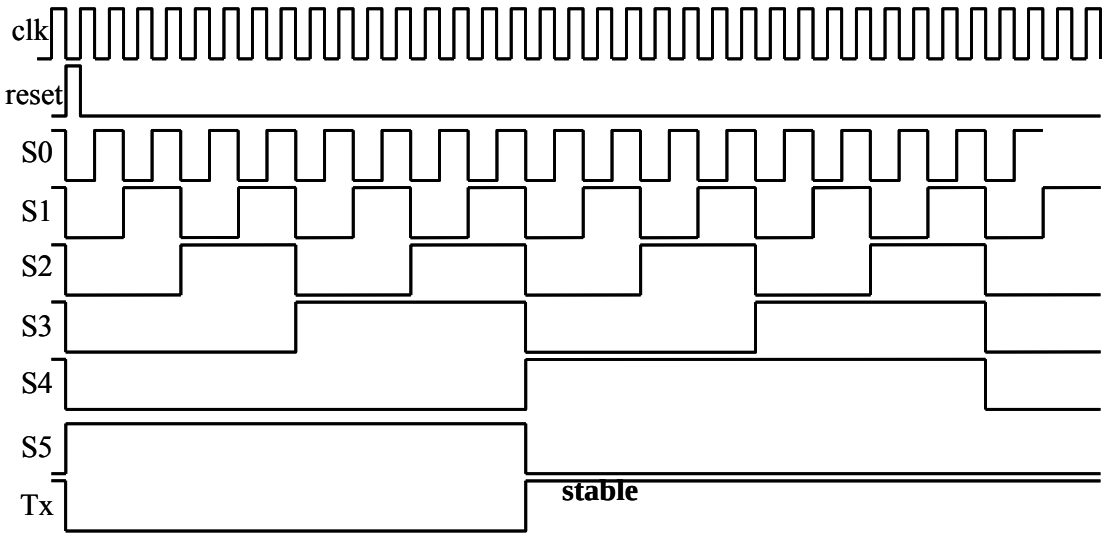


Figure 4.11 The function verification of the counter

4.2.4 Driver

The driver is studied in this section. The power supply and ground of an IC is not ideal. It is combined with the equivalent inductance and capacitance of power distribution networks as shown in Figure 4.12. The load capacitor will be charged and discharged when signal transient. The switching noise increases as the frequency increases.

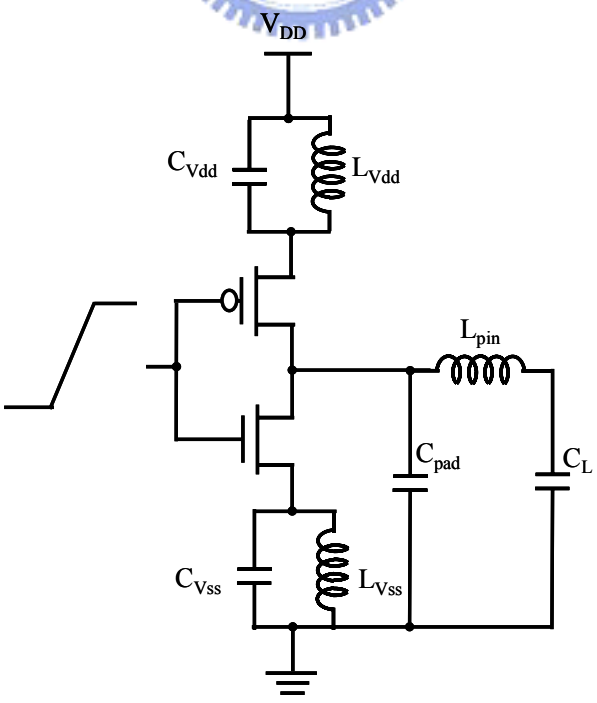


Figure 4.12 Simplified electrical model of chip-package interface

Conventionally, two current sources are connecting to power and ground respectively to minimize the current change hence reduce noise as shown in Figure 4.13 (a). Unfortunately, these two current sources will create a large voltage drop and limit the output voltage swing. In order to meet LVDS standard, the size of the four switching transistors need to be increased. So, the sizes of the pre-drivers must also be increased. This will increase the area and power of the pre-driver. It is a trade-off between the performance and the cost. Due to the device size scaled-down, the power supply voltage decreases. This problem becomes a challenge for designers. So, we proposed the following architecture. It has no current source in power supply and ground as shown in Figure 4.13 (b).

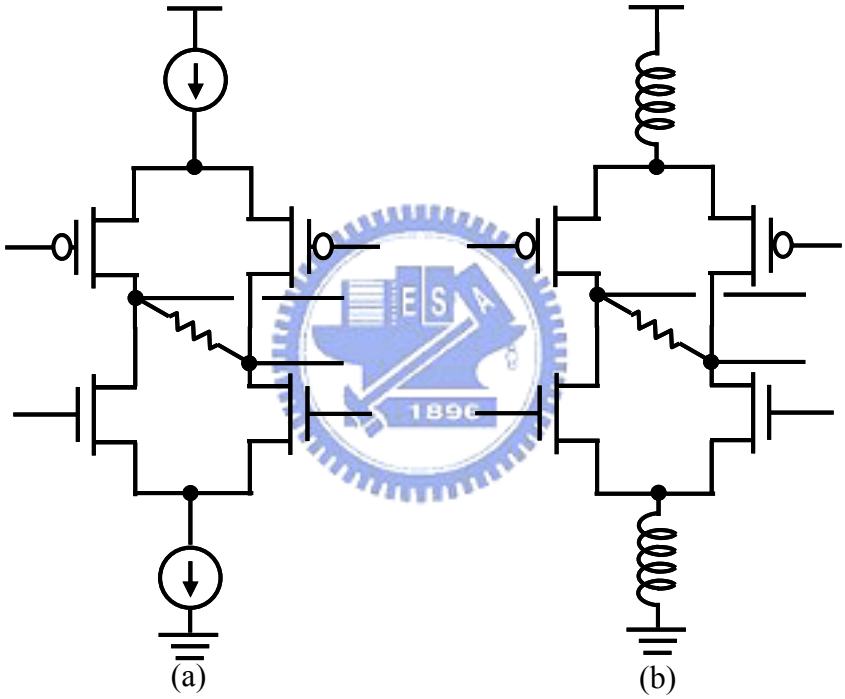


Figure 4.13 LVDS driver (a) traditional (b) proposed driver

This methodology has some advantages. First, the driver needs no current source so output signal swing is enlarged. It also reduces the sizes of switch transistor greatly. Hence, the sizes of the pre-driver are reduce as well. It reduces the overall chip area substantially. Furthermore, the whole driver architecture looks like the two inverter connected back to back, it makes the control and layout easier. Notice that, the common-mode voltage is lowered from 1.25V to 0.9V to be used in a 1.8V supply environment. According to the proposed driver, we add logic gates to the driver. The completive version for the design is shown in Figure 4.14.

Figure 4.14 (a) shows the circuit of the main driver and the calibration driver.

For the main driver, A and B pins are connected to Vdd. For calibration driver, then we can control A and B pins according to the swing calibration controller. In total, there are twelve calibration drivers. Figure 4.14 (b) shows the circuit of the pre-emphasis driver. We can control A and B pins respectively to connect HIGH or LOW to determent how many PMOS and NMOS being turned on according to the channel loss. The transition detector controls $Pout_{0\text{-}1}$, $Poutb_{0\text{-}1}$, $Pout_{1\text{-}0}$ and $Poutb_{1\text{-}0}$. When data has transitions, the transition detector generates pulses to control these pins to shape output signal. Note that Tap1 and Tap2 are the same and the only difference is that the transition detector sends different widths of pulses to the drivers.

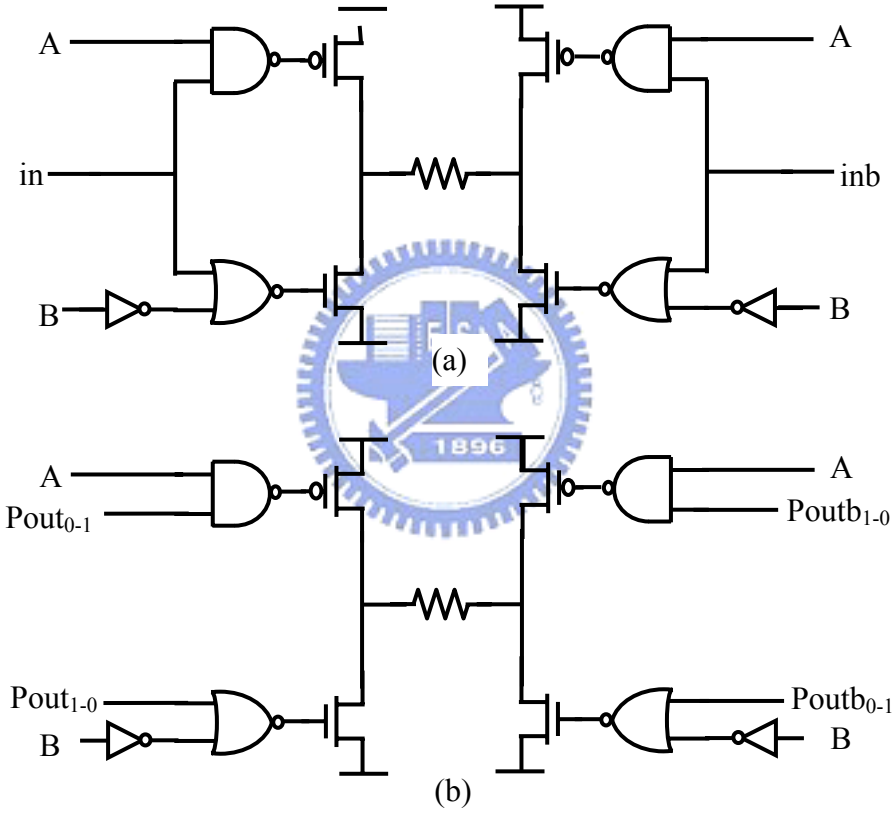


Figure 4.14 Complete version of our driver (a) main and calibration driver (b) pre-emphasis driver

In chapter3, we stated that our driver is like a voltage divider with resistors. These resistors are PMOSs and NMOSs as shown in Figure 4.14. And we will discuss the reflection problem. When the driver is operating in the pre-emphasis state, we can not guarantee that equivalent resistor is 50Ω. But we hope it is 50Ω to cancel the reflection effect in steady statue at least. We can determent the termination resistor value of near end and the equivalent resistors of four switches to make these resistors

be equal to 50Ω when the reflection happens as shown in Figure 4.15. When we determent termination resistor value of near end, we just control the output voltage at desired level, then the resistor will be equal to the needed 50Ω. If the output voltage is wrong, the swing calibration controller will calibrate it.

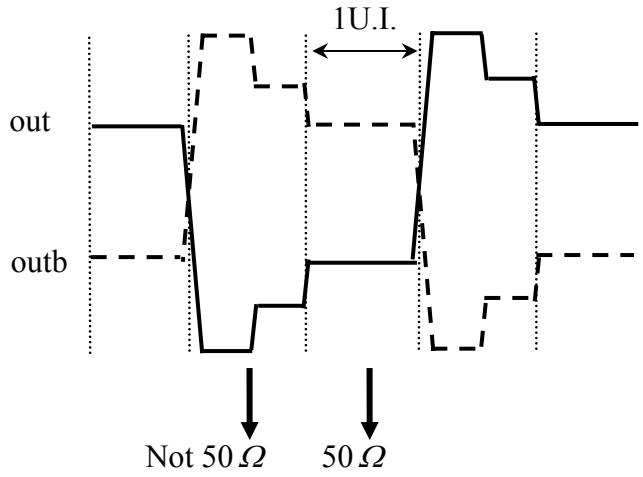


Figure 4.15 Equivalent resistors change

According to simulation results, we can get relationship between the turn-on MOSs and the output voltage in Figure 4.16. We can change tune-on MOS to change the output voltage to reach desired level. At the same method, the SF and FS cases also are considered in our driver design.

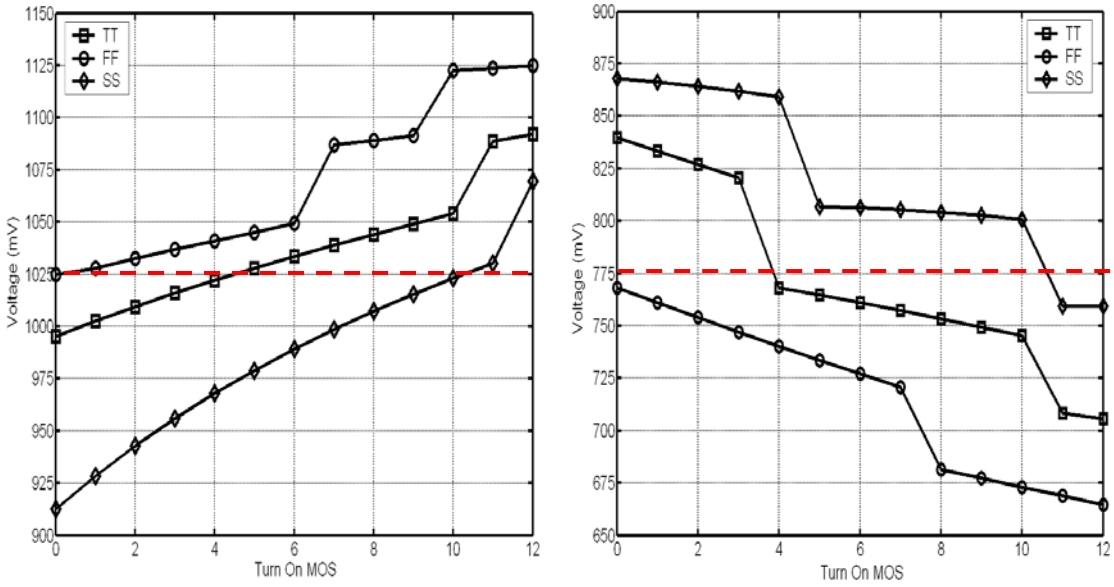


Figure 4.16 The output voltage of the TT, SS and FF cases

4.2.5 Delay Buffer

The delay buffer is the simple circuit. In order to obtain the same delay for the main driver, the calibration driver, and the pre-emphasis driver, we use inverter chains to obtain the same delay as shown in Figure 4.17.

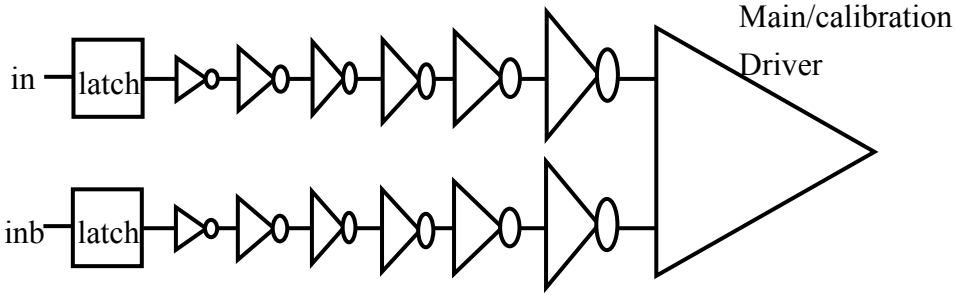
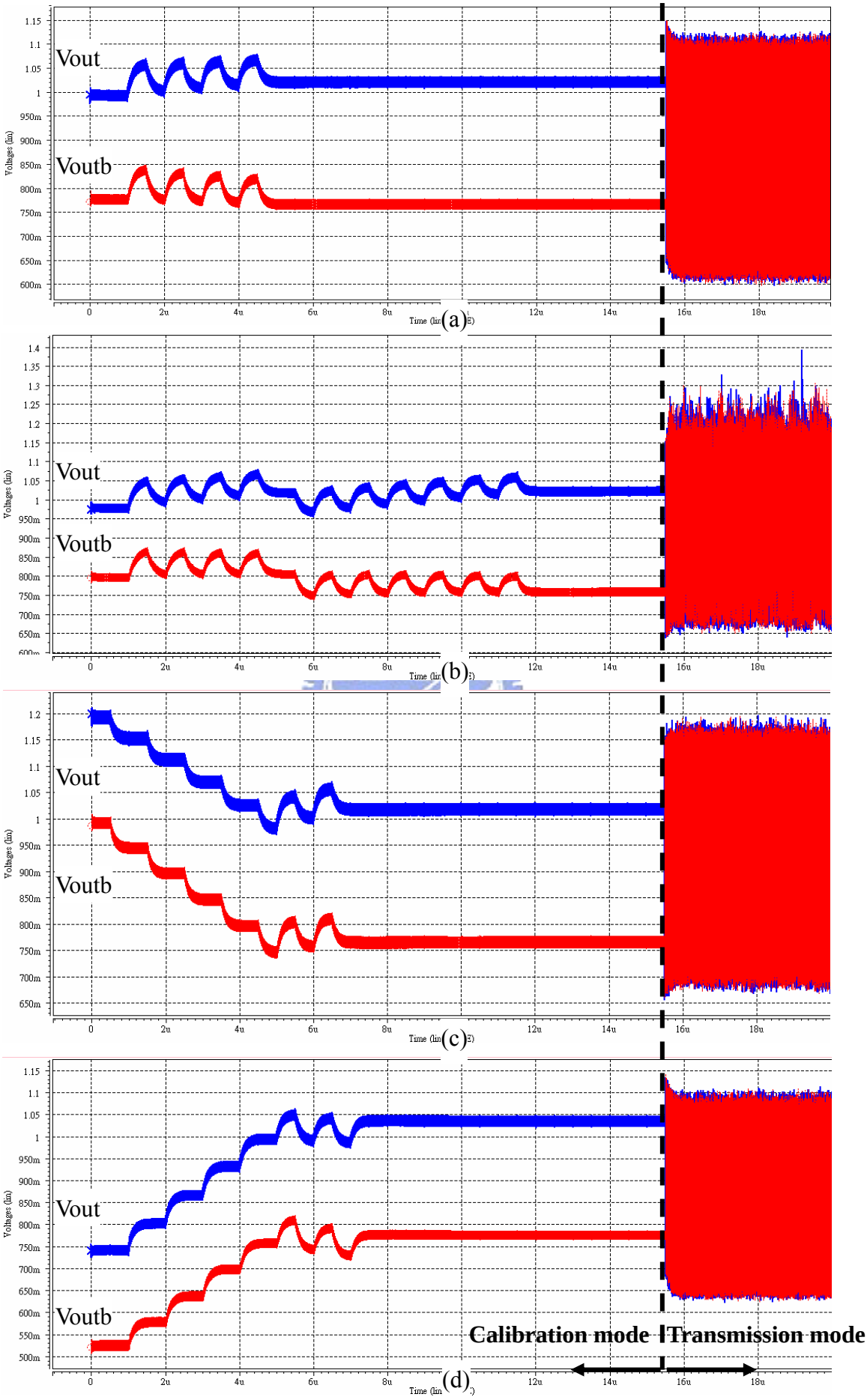


Figure 4.17 Delay buffer circuit

4.3 Simulation Result

4.3.1 Output Swing Calibration Simulation

To verify the design of the swing calibration controller circuit, the post-simulation results of the transmitter circuit are shown in this section. Figure 4.18 and Table 4-2 show the simulation results of the calibration function. We set the reference voltages to 1020mV (V_{refh}) and 780mV (V_{refl}) for a swing of 250mV and a common mode of 900mV. V_{high} is 1025mV and V_{low} is 775mV. The calibration needs at most twelve clock cycles to complete, our counter will count sixteen clock cycles and switch to transmission mode. We can see the mode change in Figure 4.18. The calibration function of FF case does not operate because R_u and R_d are less than R_{stable} initially. R_{ru} and R_{rd} can be calculated according to the simulation data and their values are about 50Ω in steady state. This can reduce the reflection effect.


Vout
Voutb
Voltages (lin)
Time (lin
(a)
(b)
(c)
(d)
Calibration mode
Transmission mode

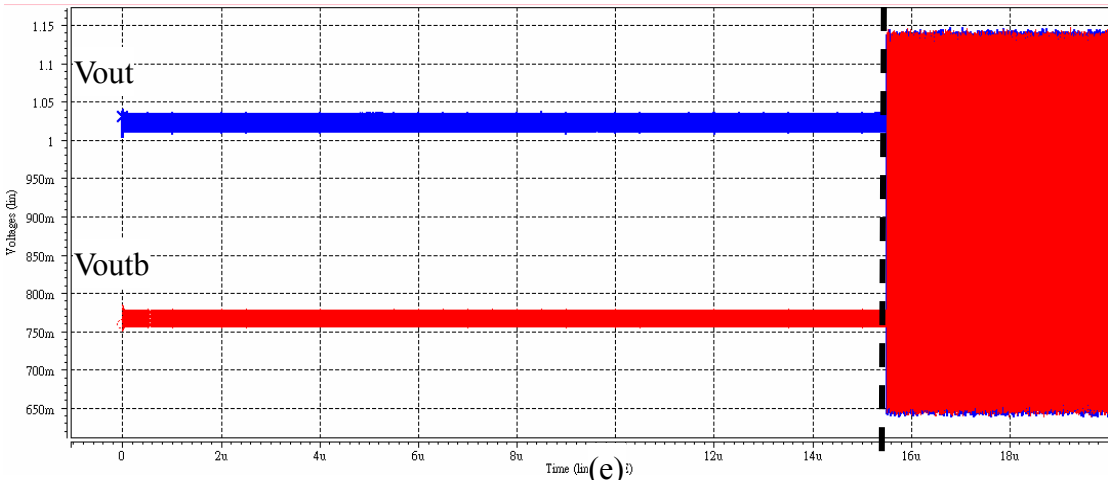


Figure 4.18 Post-Simulation results of calibration functions (a) TT case (b) SS case (c) SF case (d) FS case (e) FF case.

Table 4-2 Parameter summary after calibration

Corner case	V_{high}	V_{low}	After Calibration R_u	After Calibration R_d	Reflection resistor R_{ru}	Reflection resistor R_{rd}
TT	1.022V	0.768V	178.2 Ω	176.01 Ω	49.7 Ω	49.9 Ω
FF	1.025V	0.768V	175.8 Ω	174.3 Ω	49.5 Ω	49.7 Ω
SS	1.023V	0.760V	171.5 Ω	167.7 Ω	49.0 Ω	49.3 Ω
FS	1.036V	0.777V	171.2 Ω	173.3 Ω	49.6 Ω	49.2 Ω
SF	1.034V	0.773V	170.6 Ω	172.2 Ω	49.4 Ω	49.3 Ω

4.3.2 Output Eye Diagram Simulation

After checking the calibration functions, we simulate the output eye diagram of our driver in this section. We use C language to generate 3.125Gbps random data. In Figure 4.19, the driver without the pre-emphasis has a jitter of 26ps in post-layout simulation. The height of the eye diagram is about ±250mV. Receiver eye diagram is not good due to channel loss. So we add pre-emphasis function to the driver and the output jitter is about 36ps as shown in Figure 4.20. Although the transmitter output jitter is increased, the eye diagram of the receiver is a better than in Figure 4.19. The height of the eye diagram of the receiver is about ±200mV.

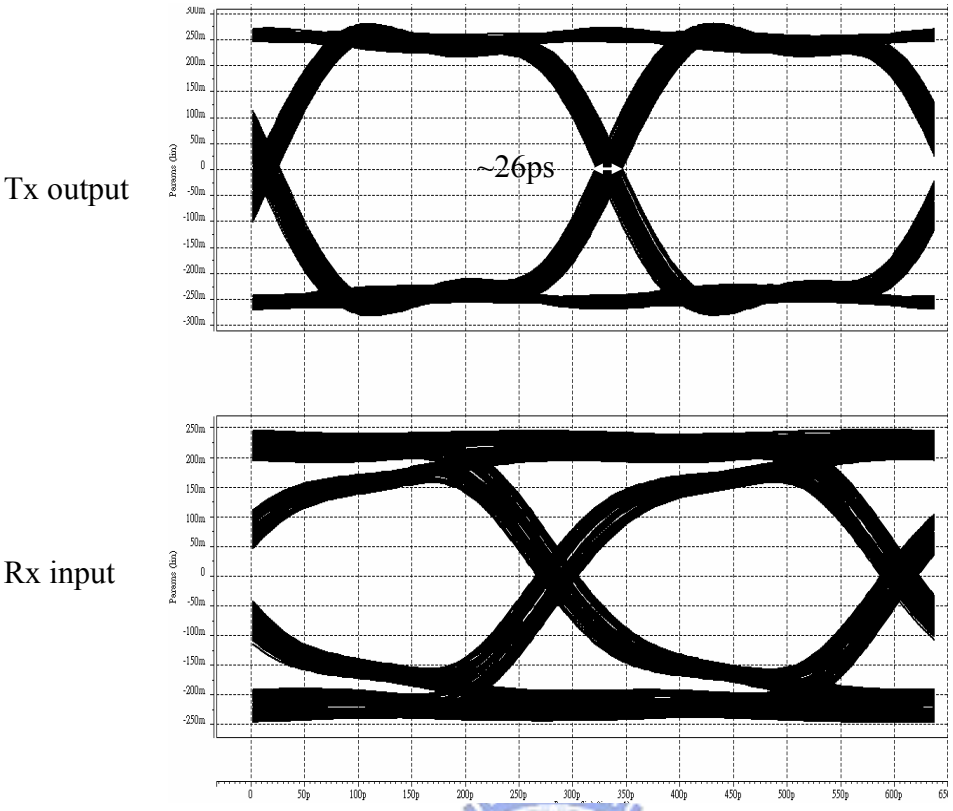


Figure 4.19 Eye diagram of propose transmitter without pre-emphasis

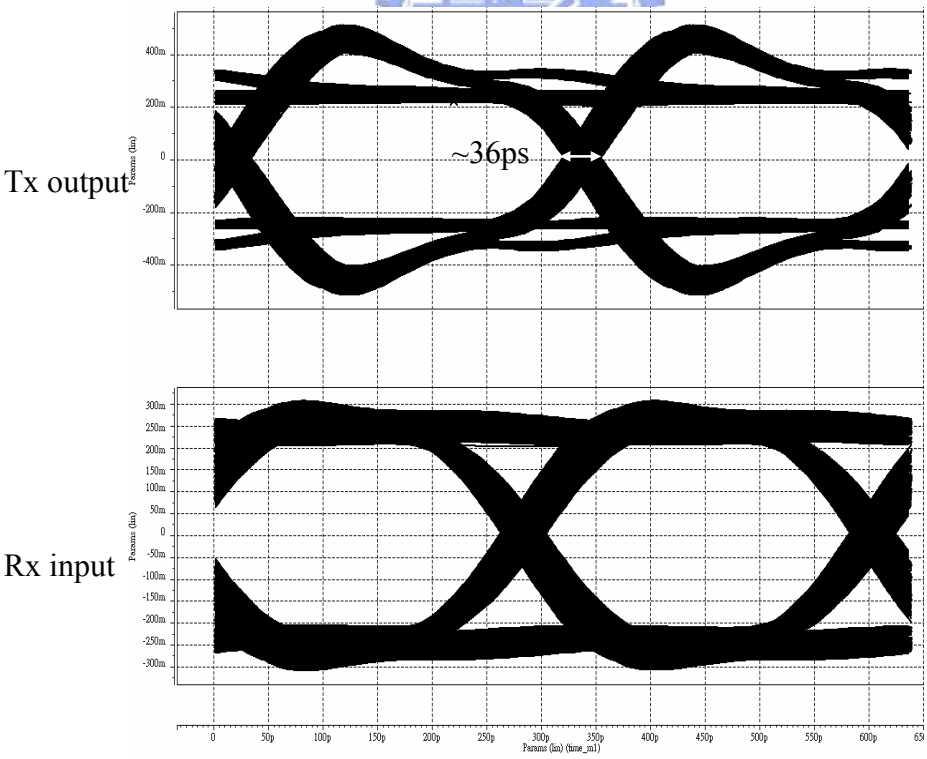


Figure 4.20 Eye diagram of propose transmitter with pre-emphasis

Figure 4.21 is the overlap of the eye diagrams with and without pre-emphasis. We can see clearly that pre-emphasis compensates the channel loss effectively.

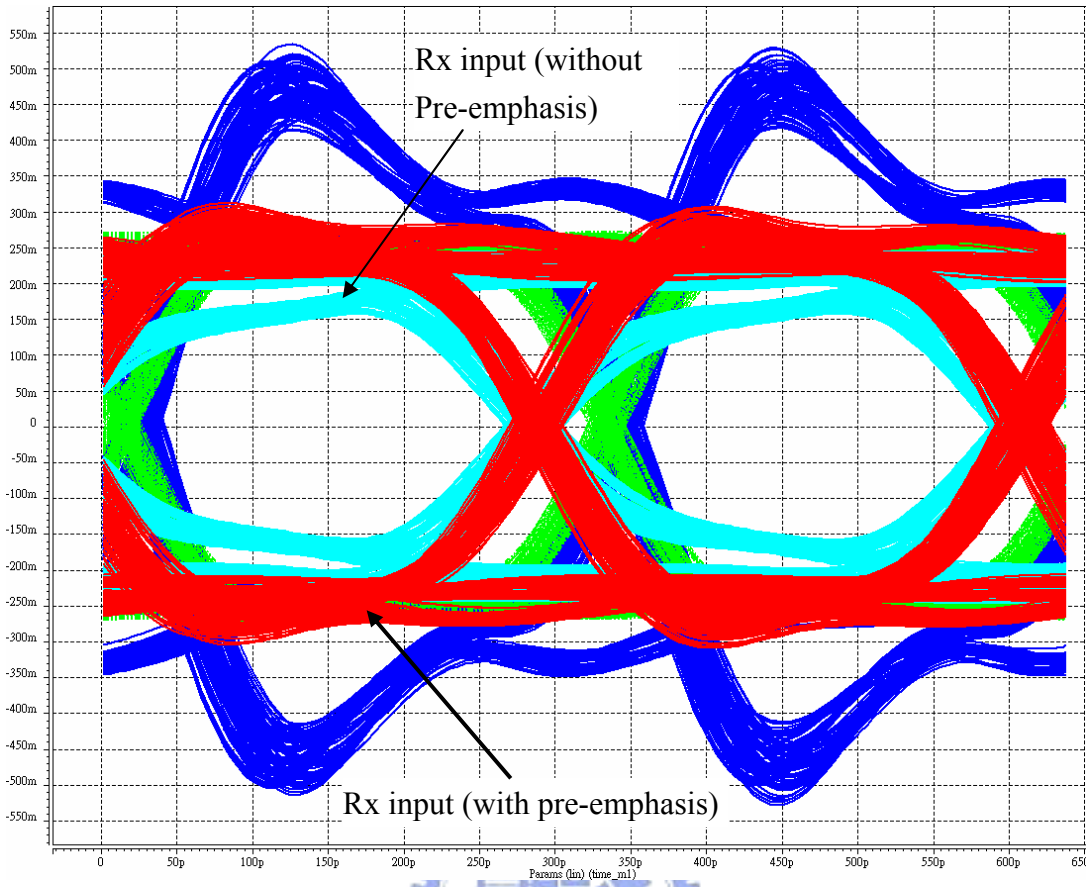


Figure 4.21 Overlap eye diagrams to comparison

4.4 Implementations

The proposed transmitter is implemented using TSMC 1P6M 0.18um. The total chip area is 0.95mm*0.84mm and the core area is 0.47mm*0.44mm as shown in Figure 4.22. The driver is in the middle of the chip and the transition detector (TD) and the swing calibration controller (SCC) are on both sides. We use pre-emphasis control pins to control pre-emphasis according to the channel response. Some pins are reserved for debugging. The summaries of post-layout simulation are shown in Table 4-3.

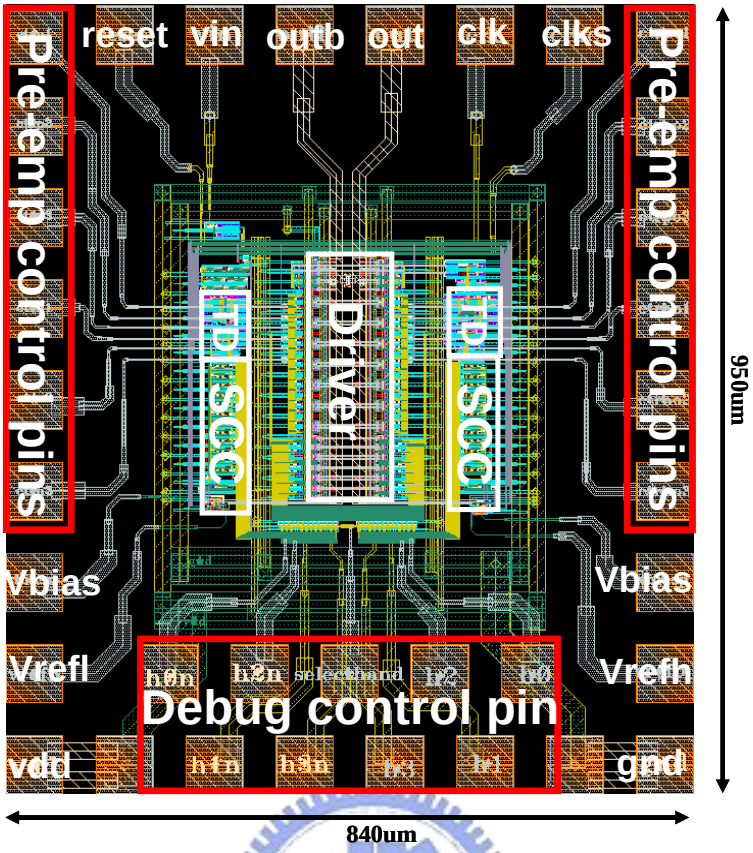


Figure 4.22 Layout of proposed transmitter

Table 4-3 Chip summary of the transmitter

Function	Tx with pre-emphasis
Technology	0.18um 1P6M CMOS
Power Supply	1.8V
Chip area	940*850 (um^2)
Core area	470*440 (um^2)
Transistor/Gate Count	4221/1360
Power Dissipation	38.7 mW (without pre-emp) 50.6 mW (with pre-emp)
Jitter (pk-pk)	26p @3.125Gbps(no pre-emp) 36p @3.125Gbps(with pre-emp)

4.5 Summary

In this chapter, we have described the proposed transmitter circuit. The driver has an additional circuit that can calibrate the output voltage by itself. The chip can detect the output level and start the calibration by reset. After 16 clocks, the calibration ends and the driver start sending data. The pre-emphasis is also added to this driver to compensate channel loss. According to the channel response, we can adjust pre-emphasis. We can control the rising/falling time and no over compensation in steady state. The overall simulation results of transmitter and receiver eyes diagrams and calibration are shown in this section.

Chapter 5

Conclusion

5.1 Conclusion

High-speed link becomes more and more important. In this thesis, we proposed a 3.125 Gbps transmitter architecture that uses novel scheme with self-calibration and pre-emphasis. We have described Tap1 and Tap2 of the pre-emphasis. It improves the signal quality at far end. The self-calibration that compensates the process variation is also proposed and its algorithm is proved. We have described overall transmitter circuit and simulation. According to post-layout simulation, we know that the self-calibration and pre-emphasis are working correctly. Our pre-emphasis is better than others, because we can control the rising (falling) time and no overshot in steady state. The proposed transmitter is composed of the digital logic gates, so a self-calibration, all-digital 3Gbps driver with pre-emphasis is implemented in this thesis. The proposed driver can be used in SATA Ⅱ [8]. This transmitter is implemented in TSMC 1P6M 0.18um CMOS technology.

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