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Thermal analysis on the degradation of poly-silicon TFTs under AC stress

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ABSTRACT

In this work, the degradation mechanism of N-channel poly-silicon thin-film transistor (poly-Si TFT) has been investigated under dynamic voltage stress at room temperature. The ON-current of TFT is degraded to as low as 0.3 times of the initial value after 1000 s stress. On the other hand, both the sub-threshold swing and threshold voltage kept well during the AC stress. The current crowding effect was rapidly increased with increasing of stress duration. However, comparing the initial and degraded characteristics at rising temperature, namely, 150 °C, the ON-current of TFT only decrease to 75% of the initial value after 1000 s AC stress. It depicts that creation of effective trap density in tail-states of poly-Si film is responsible for the electrical degradation of poly-Si TFT. At high temperature, electron has enough energy to pass the energy barrier created by ac stress and the degradation is less obvious.

1. Introduction

Low-temperature processed polycrystalline-silicon (poly-Si) has been widely investigated as a material for mobile applications such as digital cameras [1] and note book computers, because the electron mobility of low-temperature poly-Si thin-film transistors (TFTs) is about 100 times larger than that of the conventional amorphous silicon TFTs. Since the maximum process temperature is lower than 600 °C, poly-Si TFTs can be fabricated on a wide variety of cheap glasses. The major advantage of the poly-Si TFT is a higher field effective mobility than that of the a-Si-based TFT. Moreover, the poly-Si TFT can be produced as complementary transistors, N-channel and P-channel ones. Taking advantage of these features, poly-Si TFTs are applied for pixel TFTs and the driver circuits (ex. scan driver). If the mobility of poly-Si TFTs is further increased, this poly-Si technology will realize the system on panel (SOP) which will integrate memory, CPU, and display [2]. However, the traps of grain structures play an important role for the electrical properties and stabilities of poly-Si TFTs. TFT devices in functional circuits serve as the switches and suffer the high frequency voltage pulses. Previous research reports have shown a relationship between the creation of states and hot-carriers effect by performing DC stress [3,4]. The degradation mechanism of N-channel TFT under dynamic voltage stress, however, has not been clarified yet [5,6]. The degraded TFT will seriously influence the operation of the circuits. In this study, the degradation mechanism under dynamic operation for poly-Si N-channel TFT will be investigated by electrical analysis in detail.

2. Experimental

N-channel poly-Si TFTs with top-gate structure were fabricated on a glass substrate without lightly doped drain (LDD). First, a 50 nm-thick amorphous silicon (a-Si) film was deposited by plasma enhanced chemical vapor deposition (PECVD), and subsequently, the films were dehydrogenated by furnace annealing. After dehydrogenation, the a-Si films were crystallized by XeCl excimer-laser. The power of the line-shaped beam was 350 mJ cm^{-2}. Following the laser process, 100 nm-thick gate oxide was deposited by PECVD. Then the implantation was adopted to define the source/drain (S/D) region. Then an annealing process was performed to activate the dopant impurities. MoW was sputtered as a gate metal. The length and width of TFTs in this work were 10 μm and 30 μm, respectively. The overlap of gate metal and S/D junction was 1 μm. The stress pulses were performed on the gate electrode as the dynamic stress and S/D were grounded, as shown in the inset of Fig. 1. As for the stress condition, we used the rectangular pulse with amplifier of ±15 V and frequency of 500 kHz. Both the rising time (T_r) and falling time (T_f) were 100 ns. The TFTs were stressed at room temperature. *I–V* and *C–V* characteristics were measured before and after AC stress at 30 °C, 60 °C, 90 °C, 120 °C and 150 °C.

3. Results and discussions

Fig. 2(a) shows the I_D–V_G relationships of N-channel poly-Si TFT with different dynamic stress times. The *I–V* curves were measured

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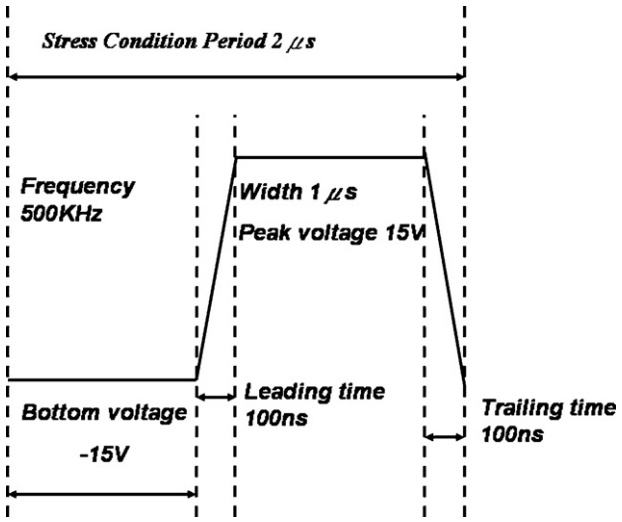

Fig. 1. The stress pulses were performed on the gate electrode as the dynamic stress and source/drain were grounded.

in linear region with $V_D = 0.1$ V at 30 °C. The distinct decrease in ON-current was found with the increasing stress duration. After stressing 1000 s, the degradation of the TFT ON-current is 26.4%. Both the sub-threshold swing (0.13 V dec.$^{-1}$) and threshold voltage (1.5 V) kept well during the stressing. Threshold voltage was defined as the gate voltage that I_D was equal to ln$A$. In general, the ON-current degradation is induced by oxide trapping or states creation. Since the threshold voltage did not shift, the degradation

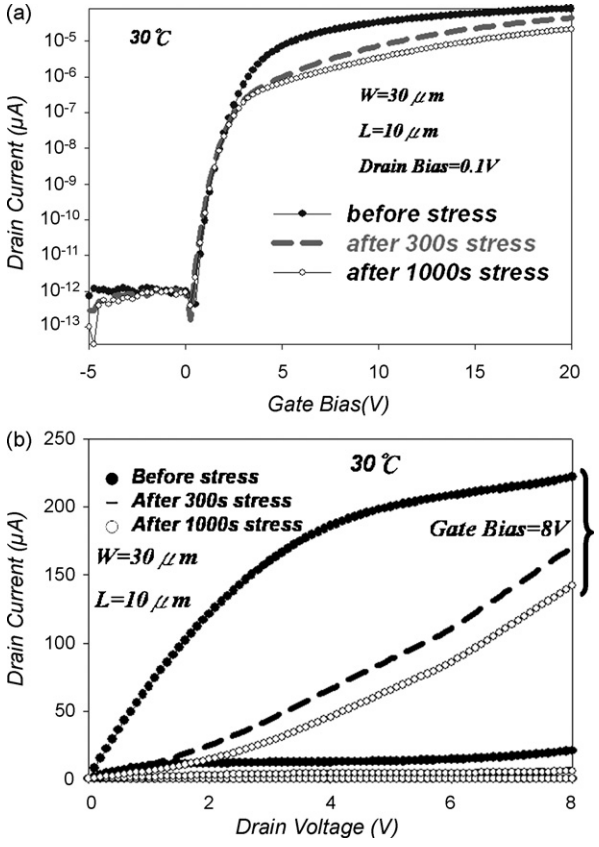

Fig. 2. (a) the I_D–V_G relationships of N-channel poly-Si TFT with different dynamic stress times. The distinct decrease in ON-current was found with the increasing stress duration. (b) The I_D–V_D characteristics of TFT at 30 °C with the dynamic stress times. Current crowding effect was observed after dynamic stress.

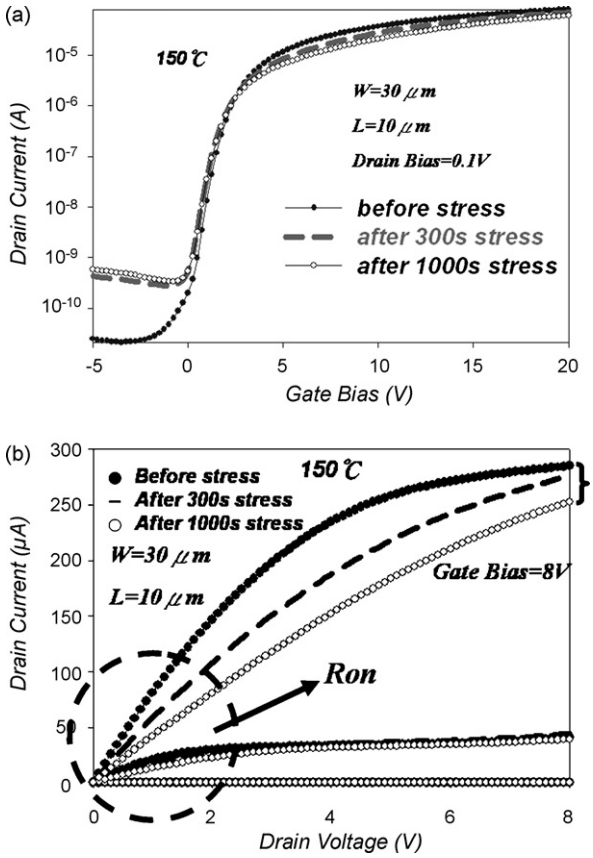

Fig. 3. (a) The I_D–V_G relationships of stressed poly-Si TFT at 150 °C. (b)The I_D–V_D relationships of stressed poly-Si TFT at 150 °C. The degradation at 150 °C is significantly lower.

induced by oxide trapping was thus excluded. The states creation was justified to be the main reason for degradation of ON-current. From the evolution of the transfer characteristics at the linear operation region with stress time, it is apparent that the impact of the applied stress leads to an obvious decrease of the ON-current operated at the above threshold region of the I_D–V_G characteristics. For poly-Si TFTs, the degradation under DC stress is usually characterized by a decrease of the sub-threshold slope mainly due to the generation of traps at deep states in poly-Si grains and a threshold voltage shift caused by charge trapping in the gate oxide and at the deep states [7]. However, the experimental data show that both sub-threshold slope and threshold voltage remain unchanged in all stressed devices in comparison with the non-stressed device. This indicates that the degradation of the N-channel poly-Si TFTs is neither occurred by charge trapping in the gate oxide nor by the creation of traps at the deep states. We can infer that the tail-states are responsible for the electrical degradation of TFT [7]. The I_D–V_D characteristics of TFT at 30 °C with the dynamic stress times are illustrated in Fig. 2(b). It is observed that the current crowding effect on TFT is significantly enlarged with the increase of stress time, which indicates parasitic resistance contributes to the degradation on electrical properties of TFT. The parasitic resistance is dependent on the following several factors, such as the trap states near the S/D junctions, sheet resistance of N^+ poly-Si layer, and S/D contact quality [8,9]. According to our previous report [10], the trap states near the S/D junctions was though as the main reason. The large parasitic resistance would result in the current crowding effect, as shown in Fig. 2(b). Fig. 3(a) shows the I_D–V_G curves of stressed poly-Si TFT at 150 °C. Compared with Fig 2(a), the degradation behavior observed at 150 °C is significantly lower. The ON-current of TFT is 75% of the initial value after 1000 s AC stress at 150 °C. Both the sub-threshold

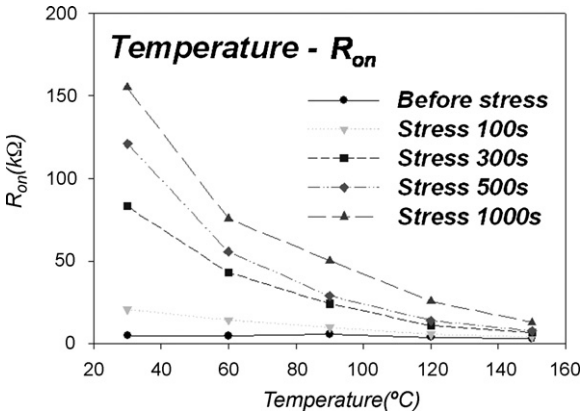

Fig. 4. R_{on}-temperature relationships versus stress time. The current crowding effect was increasing with dynamic stress duration increase and obviously reduced with temperature increasing.

swing and threshold voltage still kept exhibit no difference at high temperature. It is apparent that the ON-current degradation is less obvious as measurement temperature rises. The I_D–V_D relationships at 150 °C can be seen in Fig. 3(b). Current crowding effect was also less obviously at high measuring temperature. As mention above, the large parasitic resistance induced by the trap states near the S/D junctions would result in the current crowding effect and ON-current degradation. There is surely a close relation between turn-on resistance and ON-current degradation. The turn on resistance R_{on} was extracted form the linear region of I_D–V_D curve under the operation of small drain voltages V_D and high gate voltages V_G. Specifically, R_{on} is the reciprocal of slope of I_D–V_D curve. Fig. 4 shows R_{on} versus measurement temperature for device stressed with different times. The R_{on} is more dependent on the temperature as dynamic stress duration increasing. The range of R_{on} of unstressed TFT was between 5 kΩ and 3 kΩ. It was not sensitive to temperature. The R_{on} at 30 °C was significantly degraded from 5 kΩ to 155 kΩ with the stress time increasing. The R_{on} of stressed TFT becomes smaller as temperature increasing. In the case of TFT after 1000 s stressing, R_{on} at 150 °C is only about 8% of the value at 30 °C. As experimental data of the above, the current crowding effect is more obvious for longer dynamic stress duration but less observed at higher temperatures. The phenomena hinted us that the degradation was because of trap states. The possible mechanism is the generations of trap states near drain and source junctions. It has been reported that a potential barrier was induced by trap states, and that this potential barrier disturbed the carrier flow, which reduces the conductance and drain current [11]. As a result of a potential barrier induced by trap states, the current crowding was increasing. When carriers had enough energy to cross the potential barrier into the channel, the current crowding effect was reduced. It was reasonable to explain the degradation of TFT was reduced with temperature increasing. Fig. 5(a) shows *C*–*V* curves measured at 1 MHz under the operation of Gate voltage varied with grounding source and drain. *C*–*V* curves were significantly stretched out and shifted in the positive direction. In case of MIS structure (Metal Insulator Semiconductor structure) result, the *C*–*V* curve was significantly stretched out because the trap states did not appear to be affected by the higher frequency [12]. In the case of TFT, the minor carriers were not generated from energy band bending of semiconductor but came from source and drain junctions. As the mention of above, the potential barrier induced by trap states disturbed the minor carriers into the channel. It was possible reason that the *C*–*V* curves were stretched out at higher frequency. The mechanisms of degradation of *I*–*V* and *C*–*V* curves were the same. Therefore, the degradation of *C*–*V* curves should be reduced with temperature

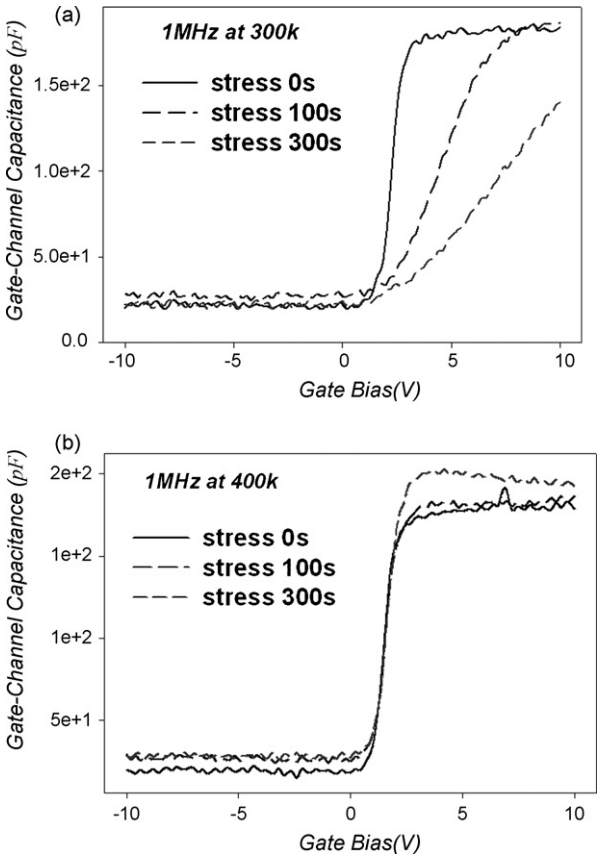

Fig. 5. (a) *C*–*V* curves were measured at 1 MHz under the operation of gate voltage varied with grounding source and drain. *C*–*V* curves were significantly stretched out and shifted in the positive direction. (b) The *C*–*V* curves were measured at 400 K. The *C*–*V* curves were not stretched out, and the degradation of *C*–*V* curves of stressed TFT was reduced at 400 K.

rising. The *C*–*V* characteristics of stressed TFTs at higher temperature were studied in order to prove that. The *C*–*V* curves at 400 K were indicated in Fig. 5(b). The *C*–*V* curves were not stretched out at 400 K. The degradation of *C*–*V* curves of stressed TFT was reduced at 400 K. The phenomenon of *C*–*V* curves was the same as *I*–*V* datum of above. It was proved that all degradations were result from a potential barrier induced by trap states. The electrical properties of poly-Si TFT are strongly influenced by the traps in the poly-Si film. The trap states were created during dynamic stress time. The position of trap states was near the surfaces of source and drain junctions. The potential barrier induced by trap states was main reason for degradation of stressed TFT. The degradation was obviously reduced by temperature rising.

4. Conclusion

In this study the distinct decrease in ON-current of N-channel poly-Si TFT was found during the dynamic voltage stress. In spite of electrical degradation appearing at the ON-current of the poly-Si TFT and the *C*–*V* characteristics of the poly-Si TFT, the sub-threshold swing and threshold voltage kept in a good condition. This can be inferred that the tail-states were produced in ploy-Si film due to the ac stress. The potential barrier induced by trap states was near source and drain. It disturbed the carriers into the channel. The phenomenon resulted in the current crowding and stretching the *C*–*V* curves out. At 400 K, the carriers were enough energy to cross potential barrier. Therefore, the degradation of the poly-Si TFT was decreasing with temperature increasing.

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References

[1] M. Furuta, S. Maegawa, H. Sano, T. Yoshioka, Y. Uraoka, H. Tsutsu, I. Kobayashi, T. Kawamura, Y. Miyata, Euro Display Tech. Dig. 96 (16th Int. Display Res. Conf.), Birmingham, England, 1996, p. 547.
[2] Y. Nakajima, Y. Kida, M. Murase, Y. Toyoshima, Y. Maki, SID Tech. Dig. (2004) 864–867.
[3] I.W. Wu, W.B. Jackson, T.Y. Huang, A.G. Lewis, A. Chiang, IEEE Electron Device Lett. 11 (1990) 167.
[4] N. Kato, T. Yamada, S. Yamada, T. Nakamura, T. Hamano, IEDM Tech. Dig. (1992) 677–680.
[5] Y. Uraoka, Y. Morita, H. Yano, T. Hatayama, T. Fuyuku, Jpn. J. Appl. Phys. 41 (2002) 5894.
[6] Y. Toyota, T. Shiba, IEEE Trans. Elec. Devices 51 (2004) 927.
[7] M. Hack, A.G. Lewis, I.W. Wu, IEEE Trans. Elec. Devices 40 (1993) 890.
[8] M. Stewart, R.S. Howell, L. Pires, M.K. Hatalis, IEEE Trans. Elec. Devices 48 (2001) 845.
[9] H.W. Zan, T.C. Chang, P.S. Shih, D.Z. Peng, P.Y. Kuo, T.Y. Huang, C.Y. Chang, P.T. Liu, IEEE Electron Device Lett. 24 (2003) 509.
[10] C.W. Chen, T.C. Chang, P.T. Liu, H.Y. Lu, T.M. Tsai, C.F. Weng, C.W. Hu, T.Y. Tseng, Electrochem. Solid-State Lett. 8 (9) (2005) H69–H71.
[11] G. Fortunato, A. Pecora, G. Tallarida, L. Mariucci, C. Reita, P. Migliorato, IEEE Trans. Elec. Devices 41 (3) (1994) 340–346.
[12] J.S. Choi, G.W. Neudeck, IEEE Trans. Elec. Devices 39 (11) (1992) 2515–2522.