國 立 交 通 大 學

電 機 與 控 制 工 程 學 系 研 究 所

碩 士 論 文

適用於 Serial-ATA 之展頻時脈產生器

A Spread Spectrum Clock Generator for Serial-ATA

研 究 生：陳緯達

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中華民國　九十四年　七月

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摘要

隨著對高速傳輸速率需求的不斷提升，*Serial AT Attachment* (Serial-ATA)成為一種普遍的外部儲存規格。隨著電路運作速度的增快，高速時脈信號所造成的電磁干擾(*Electro-Magnetic Interference*, EMI)成為不可忽視的問題。因此 Serial-ATA 系統要求時脈頻率具有 5000 ppm 展頻量、30~33 kHz 調變率。

在本論文中，我們提出一個適用於 Serial-ATA 之展頻時脈產生器(*Spread Spectrum Clock Generator*, SSCG)。展頻技術是利用對時脈信號頻率做調變以有效降低電磁干擾。我們使用一個具備三階三角積分器的除小數鎖相迴路來實現展頻時脈產生器。除小數鎖相迴路可合成出比參考頻率小的頻率，使用數位式三角積分調變技術可將量化雜訊調變到高頻以減少 spur 現象。

論文中我們實現了一個 1.5 GHz，具有 5000 ppm、33 KHz 三角波調變的展頻時脈產生器。此展頻時脈產生器使用台積電 0.18 um CMOS 製程製造。在非展頻情況所量測到時脈 jitter 為 80 ps。展頻模式下，頻譜上的時脈峰高能量降低了 23.44 dB。

A Spread Spectrum Clock Generator for Serial-ATA

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ABSTRACT

As the increasing demand for high data transmitting rate, *Serial AT Attachment* (Serial-ATA) is one of the popular external storage specifications. As operating at high frequencies, currents and voltages present in the circuits and the signal traces lead to great *Electro-Magnetic Interference* (EMI). Hence, Serial-ATA systems require a wide spreading of 5000 ppm and a 30~33 kHz modulation rate.

In this thesis, we proposed a *Spread Spectrum Clock Generator* (SSCG) for Serial-ATA. SSCG is a special technique of frequency modulation to reduce EMI effectively. We use a fractional-N PLL with a digital 3rd order MASH 1-1-1 delta-sigma modulator to accomplish the spread spectrum function. Fractional-N PLL can achieve high resolution with high operation frequency. The use of digital delta-sigma modulation technique in the fractional-N PLL can eliminate spurs.

The SSCG generates clocks at 1.5 GHz, a 5000 ppm down spread with a triangular waveform frequency modulation of 33 KHz. The circuit is fabricated with 0.18 um CMOS technology. The non spread spectrum clocking has a measured jitter of 80 ps and the peak amplitude reduction is 23.44 dB in spread spectrum mode.

致　謝

時光匆匆，兩年的研究所生涯結束了。回想這段日子，總覺得自己很幸運，除了研究之外，也體驗許多美妙的事。

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感謝科管所同學們這一年來的包容，我會永遠記得與大家一起辦活動，熬夜趕報告以及灑著汗水在球場上奔馳。

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最後感謝養育我的父母，願他們能以我為榮。

陳緯達　于　故鄉　風城

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Chapter 1

Introduction

1.1 Motivation

As the increasing demand for higher data transmitting rate, *Serial AT Attachment* (SATA) is one of the popular external storage specifications. High speed serial link technology is applied in optical communication, PCI Express and USB recently. Using serial link technology has many advantages including low cost, high speed and pin reduction. SATA is used with high transmission rate up to 3 Gb/s and extends to 6 Gb/s in next generation and the system needs a high speed clock generator.

As operating at high frequencies, currents and voltages present in the circuits and the signal traces lead to great *Electro-Magnetic Interference* (EMI). EMI is caused by the radiated emission of unwanted radio frequency signals that pollute managed radio spectrum. In the United States, the *Federal Communications Commission* (FCC) regulates the amount of EMI an electronic device may emit to ensure that electronic devices do not interfere with each other.

Many EMI reduction techniques can be classified into two. One is to enclose the EMI from emitting and another is to reduce the EMI at the source. The reduction methods include *Printed Circuit Broad* (PCB) layout techniques, metal shielding, and passive components. Another popular technique, *Spread Spectrum Clocking* (SSC), belongs to the latter which can reduce the amplitude at each clock harmonic to meet EMI restriction [1]. Ideally, the EMI reduction is done on chip without using heavy shielding materials in order to be low cost and portable. SATA systems adopt the SSC technique to reduce EMI problem. The *Spread Spectrum Clock Generator* (SSCG) is a special technique of frequency modulation to reduce EMI effectively.

Figure 1.1 shows the SATA requirement [2]. The frequency varies with time, a down spreading of 5000 ppm and a 30~33 kHz triangular modulation rate. The frequency deviation is 7.5 MHz so the lowest frequency is 1.4925 GHz. Down spread frequency modulation ensures the highest frequency is below the original frequency, 1.5 GHz. Typical modulation frequencies should be above the 30 KHz audio band but low enough to avoid system timing problems. SATA specification define 30~33 KHz triangular modulation.

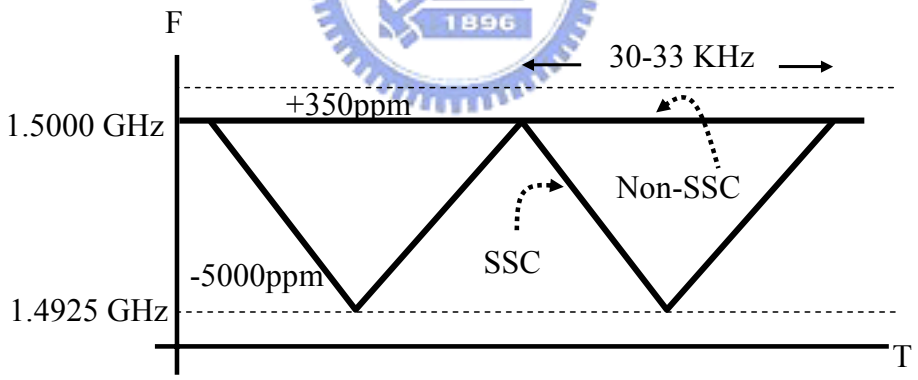


Figure 1.1: Spread spectrum requirement for Serail-ATA

1.2 Basic of Serial Link

Figure 1.2 shows general purpose serial link transceiver architecture. The low speed, parallel, digital signal is to be transferred to far-end. The PLL, based on a low frequency reference clock, generates appropriate clock and apply these clock to the MUX. The MUX transfers these parallel input data to a high speed serial output data.

The driving capability of the MUX output is small, so it is enlarged stage by stage by the driver. When signal is through the cable, which frequency and phase drift due to external noise, the amplitude will decay as well. The receiver front end enlarges the signal amplitude, and then CDR (*Clock and Data Recovery*) finds the optimal sampling phase and retime the signal. The De-MUX transfers the serial signals to the parallel ones.

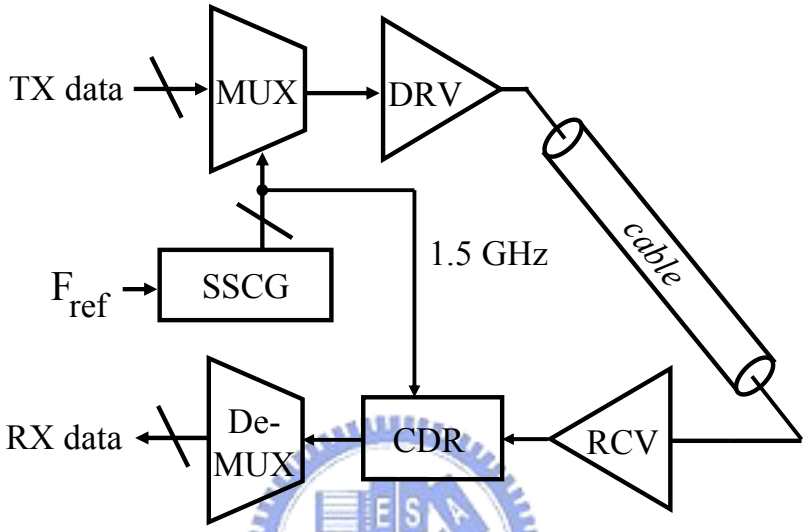


Figure 1.2: Serial link transceiver architecture

1.3 Thesis Organization

This thesis is on the design of a spread spectrum clock generator using fractional-N PLL with delta-sigma modulator for *Serial-ATA* (SATA) specification. In Chapter 2, we introduce spread spectrum theory and how it can reduce EMI problem. Then we will introduce different types of spread spectrum clock generators.

Chapter 3 begins with the introduction of the frequency synthesizer including theory of PLL and the fractional-N concept. The most important part is to describe the digital delta-sigma modulator.

In Chapter 4, we present a spread spectrum clock generator using fractional-N PLL with a delta-sigma modulator. A conventional PLL consists of a phase frequency detector, a charge pump, a loop filter, a voltage controlled oscillator and a multi-modulus divider. Then we will introduce address generator that generates triangular waveform and a third-order MASH 1-1-1 delta-sigma modulator.

In Chapter 5, we will show the simulation and measurement results of the SSCG. The chip is implemented in TSMC 0.18 um 1P6M CMOS technology. In Chapter 6, a jitter generator using spread spectrum clock generator is proposed for clock jitter BIST usage. The idea is to change the amplitude and period of the modulation frequency to generate the wanted jitter. Chapter 7 gives the conclusions.

Chapter 2

Basic of Spread Spectrum

Spread spectrum clocking is a popular technique to reduce EMI for *Serial-ATA* (SATA) requirement. In this chapter, we discuss the *Spread Spectrum Clocking* (SSC) fundamental theory including the basic properties and the effects on the original timing.

2.1 Spread Spectrum Clocking Fundamental Theory

Spread spectrum clocking is a special technique of frequency modulation to reduce EMI effectively. As shown Figure 2.1 [3], by spreading the clock frequency slightly, the energy is spread out as well. This reduces the maximum peak energy under the same total amount of energy. Only a small amount of variation in frequency is needed to obtain several decibels of energy reduction. Otherwise, it would take a lot of expensive shielding to achieve the similar results. As a result, spread spectrum clocking is an effective and low cost technique to meet EMI restriction.

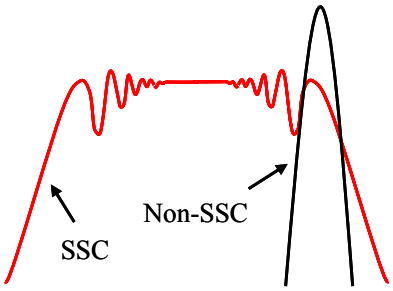


Figure 2.1: Spread fundamental frequency comparison

To obtain the details of spread spectrum, we analyze that how frequency modulation to lead to spread spectrum. Figure 2.2 shows the effect of frequency modulation on the frequency spectrum, where f_c is the carrier frequency, f_m is the modulating frequency, and Δf is the amplitude of frequency change. As can be seen frequency domain of the frequency-modulated sinusoidal waveform, sideband harmonics are generated, and the magnitude at center frequency is reduced compared to un-modulated signal. The frequency difference between each two adjacent sideband harmonics is f_m.

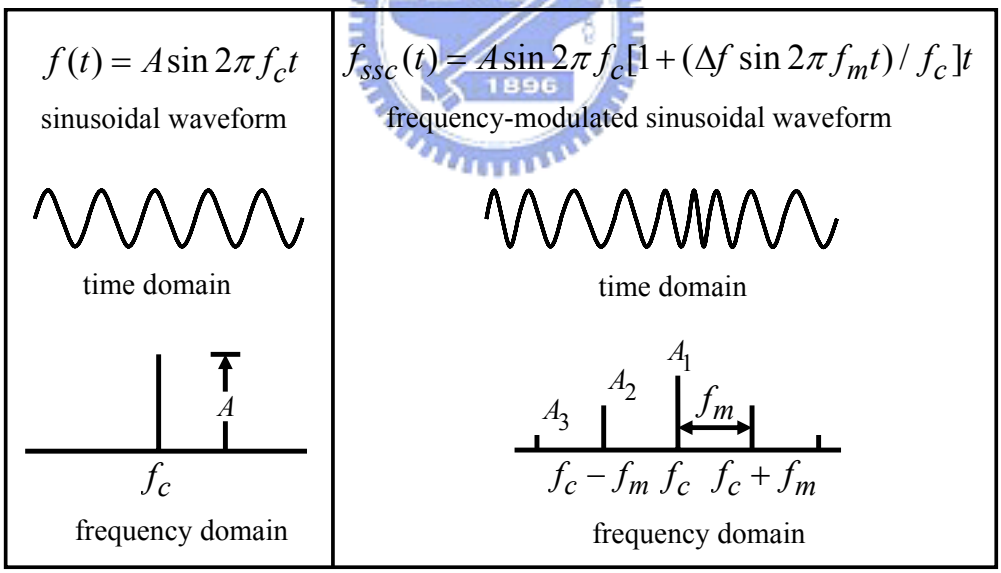


Figure 2.2: The effect of frequency modulation on the frequency spectrum

The extent of shattering and the magnitude of the resultant spectrum depend on the modulation index $\beta \equiv \Delta f / f_m$ [4]. Figure 2.3 shows the actual spectra for several β values. The larger the β values, the more evenly distributed are the spectrum.

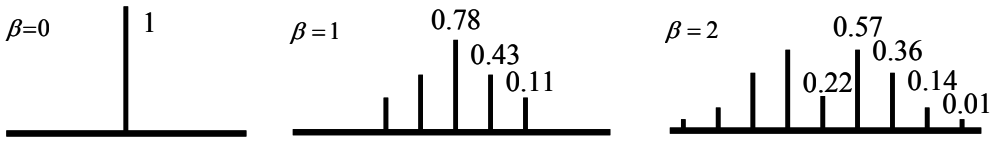


Figure 2.3: Spectra of frequency-modulated sine wave

According to Carson's Rule, Total power of a signal is unaffected by the frequency modulation. The total power of a signal is equal to the summation of the square of each harmonic amplitude. Referring to Figure 2.3, this means

$$A^2 = A_1^2 + 2(A_2^2 + A_3^2 + ...). \tag{2-1}$$

98% of the total power of a frequency modulated signal is contained inside the bandwidth β_T, where $B_T = 2(\beta + 1)f_m$. If $\beta \gg 1$, the $B_T = 2\Delta f$.

As shown in Figure 2.4, if the un-modulated waveform is a pulse train, then it itself contains harmonics. Frequency modulation of pulse train waveform shatters each of the switching harmonic components into sideband harmonic.

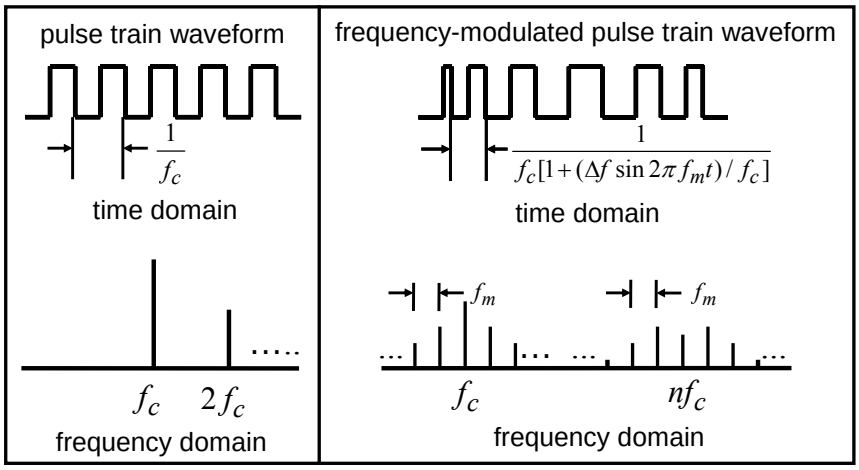


Figure 2.4: Spectra of pulse train waveform

An ideal square wave is composed of infinite sinusoidal components. For a frequency-modulated pulse train, the modulation index of each harmonic β_n is

different, where n is the number of switching harmonics of the un-modulated pulse train. Then $\beta_n = n\beta$. Carson's Rule applies to each harmonic, i.e., $B_{nT} = 2(n\beta + 1)f_m$. If $\beta \gg 1$, then $B_{nT} = nB_T$. The higher harmonic number, the more even is the spread-out power.

2.2 Implementation of SSCG

There are many types of *Spread Spectrum Clock Generator* (SSCG) in the literature [5], [6], [7]. Figure 2.5 shows the different approaches. The first type modulates the VCO directly. Using another charge pump to generate the triangular wave in to the low pass filter and modulating the VCO output clock. Due to the process variation, this analog approach may need calibration to sure 5000 ppm spread amounts. The second type combines the multiphase circuits to achieve the spread-spectrum function. This approach needs multiphase and has large load, so the power consumption is very large. The third type modulates the divider in a PLL. Our design is also based on this architecture. The PLL track and lock at divider by N1, after a period of modulation frequency, the divider jump to N2. Then the divider back to N1 after a period of modulation frequency again. And go on and go on and go on. In this way, it will generator at triangle modulation profile on low pass filter to achieve our goal.

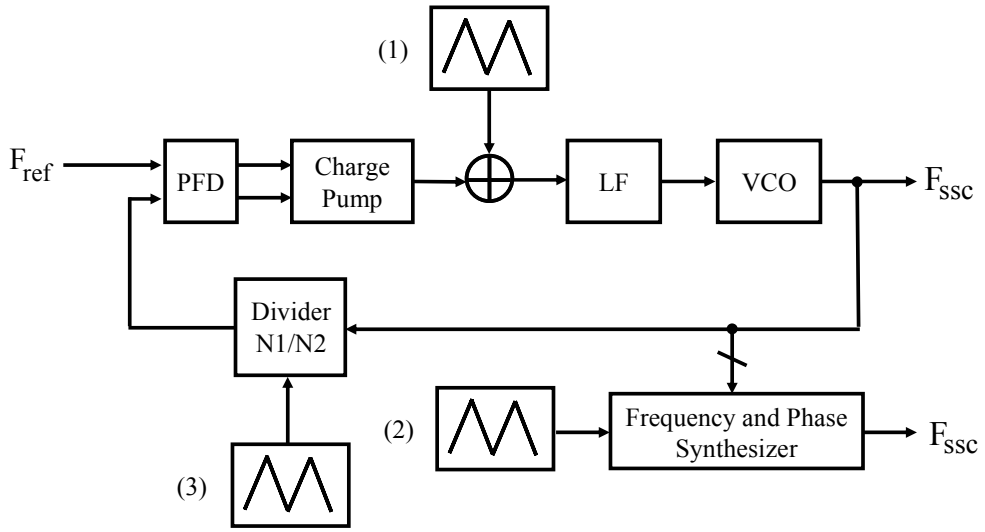
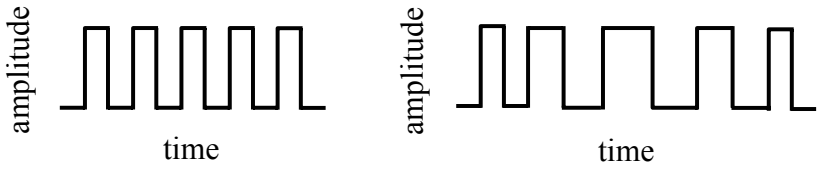


Figure 2.5: Types of SSCG architecture

Due to the 5000 ppm clock deviation of SATA requirement, it is impossible to use many dividers which division ratio is very big to implement the SSCG. Fractional-N PLL can achieve high resolution with high operation frequency. But, one major disadvantage is the generation of high tones at multiples of the channel spacing. The use of digital delta-sigma modulation technique in the fractional-N PLL can eliminate spurs and we will introduce that afterward.

2.5 Time Domain Impacts of SSC

Spread spectrum clock is a technique of frequency modulation. In frequency domain, the clock frequency is spread; the energy is spread out as well. In time domain, the frequency varies periodically with time, so dose the period of clock. As shown in Figure 2.6, the period of modulated signal varies with time and its change depends on modulation profile. Due to the variation of modulated signal period, the impacts on timing are important [8].



(a) un-modulated signal (b) modulated signal

Figure 2.6: Time domain behavior

Long term jitter is defined that maximum change in a clock's output transition from its ideal position. Figure 2.7 shows the graphical representation of long term jitter.

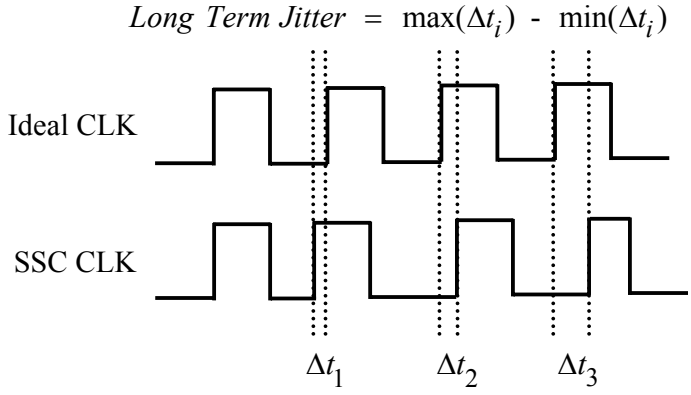


Figure 2.7: Graphical representation of long term jitter

Because the SATA specification define 30~33 KHz 5000 ppm down spread frequency modulation, there are many clock cycles pass by the reference period. The long term jitter of the spread spectrum modulated signal is tremendous.

Cycle to cycle jitter is the change in a clock's output transition from its corresponding position in the previous cycle. Figure 2.8 shows a graphical representation of the cycle to cycle jitter.

$$Cycle\ to\ Cycle\ Jitter = max(\Delta t_{c(i+1)} - \Delta t_{ci}) - min(\Delta t_{c(i+1)} - \Delta t_{ci})$$

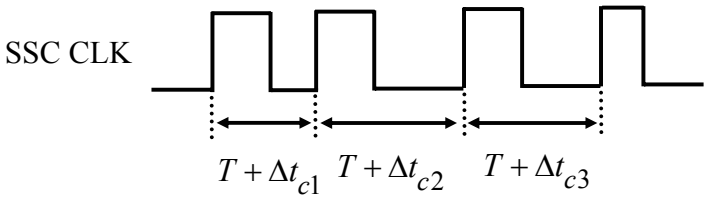


Figure 2.8: Graphical representation of short term jitter

The period between the maximum and minimum frequencies in a spread spectrum clocking system is

$$\Delta T_{total} = \frac{1}{(1-\delta) f_{nom}} - \frac{1}{f_{nom}} \approx \frac{\delta}{f_{nom}}, \qquad (2\text{-}2)$$

where f_{nom} is non-spread frequency, δ specifies the total amount of spreading as

a relative percentage of f_{nom}.

The number of clock cycles that exist in the time interval that the modulated clock migrates from f_{nom} to $(1-\delta)f_{nom}$ can be found as

$$N = f_{avg} \cdot \frac{1}{f_m} \cdot \frac{1}{2} = \frac{f_{avg}}{2f_m}, \tag{2-3}$$

where f_{avg} is the average frequency of the spread spectrum clock, f_m is the modulation frequency. Because the modulation profile is symmetric, we can only consider f_{avg} in the half of the modulation period.

$$f_{avg} = (1 - 0.5\delta) \cdot f_{nom}. \tag{2-4}$$

Calculate above equation and we can find the cycle to cycle jitter of spread spectrum clock is

$$\Delta T_{c\text{-}c} = \frac{\Delta T_{total}}{N} = \frac{2\delta}{1 - 0.5\delta} \cdot \frac{f_m}{{f_{nom}}^2}. \tag{2-5}$$

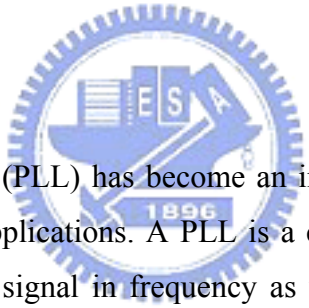
In our design, spread spectrum clock with 5000 ppm triangular modulation and 33 KHz modulation frequency, the increase cycle to cycle jitter is

$$\Delta T_{c\text{-}c} = \frac{2 \cdot 0.5\%}{1 - 0.5 \cdot 0.5\%} \cdot \frac{33 \cdot 10^3}{(1.5 \cdot 10^6)^2} = 1.47034 \cdot 10^{-17}\ sec. \tag{2-6}$$

The results shows that cycle to cycle jitter of spread spectrum clock can be ignored.

Chapter 3

Fractional-N PLL with Delta-Sigma Modulator



The *Phase-Locked Loop* (PLL) has become an important technique to generate signals in radio and timing applications. A PLL is a circuit synchronizing an output signal with a reference input signal in frequency as well as in phase. PLL play an important role in the serial link transceiver. Whether parallel-to-serial data conversion in the transmitter or serial-to-parallel data conversion in the receiver, the generating phases of PLL are needed. Because the need of frequency deviation is small, we can use fractional-N PLL to meet this SATA requirement. Traditionally, fractional-N uses analog compensation mechanisms to suppress spurious signals. In our design, we use the all digital delta-sigma modulator to implementation. Delta-sigma modulator can leave the average input unchanged and modulate the quantization noise to higher frequency. All digital design can be easily integrated into single chip and is insensitive to process variation.

3.1 Phase-Locked Loop Fundamental

A *Phase-Locked Loop* (PLL) is able to lock the output phase of frequency to an

input reference by means of negative-feedback loop. Figure 3.1 shows a block diagram of a typical PLL. A conventional PLL consists of a *Phase Frequency Detector* (PFD), a *Charge Pump* (CP), a *Loop Filter* (LF), a *Voltage Controlled Oscillator* (VCO) and a divider.

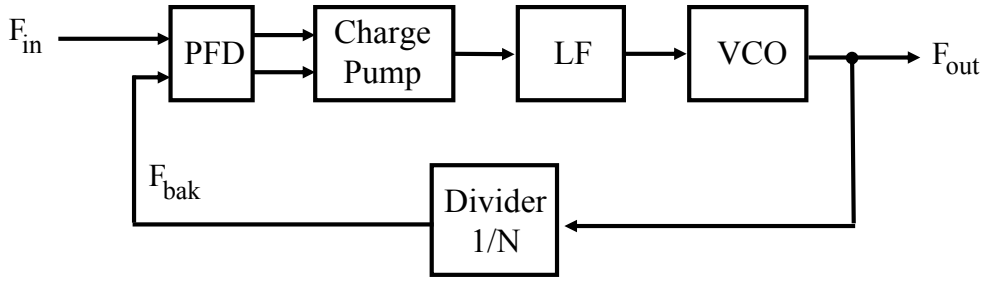


Figure 3.1: A block diagram of a typical PLL

The internal feedback signal "F_{bak}" from the divider is compared to external reference signal "F_{in}" by PFD, which generates lead or lag message to charge pump. The charge pump will charge or discharge loop filter to vary VCO output frequency according to the phase difference detected by PFD. Then VCO oscillates at a frequency equal to the N times input frequency with a phase difference. Finally, the frequency of the "F_{bak}" can be adjusted according to synchronous the input signal and "F_{out}" will become "$N \times F_{in}$" in stable state.

3.2 Phase-Locked Loop Linear Model

We can use small signal linear model to determine the design parameter of PLL [9]. Figure 3.2 shows linear model of PLL. K_{PFD} is gain of charge pump current divided by 2π. The loop filter can be repented with s domain transfer function $Z_{LF}(S)$. K_{VCO} is gain of VCO with unit of $\frac{\text{rad/s}}{\text{V}}$. Since integration is a linear operation on VCO's output frequency, frequency divider is also divider the output phase by a factor of N.

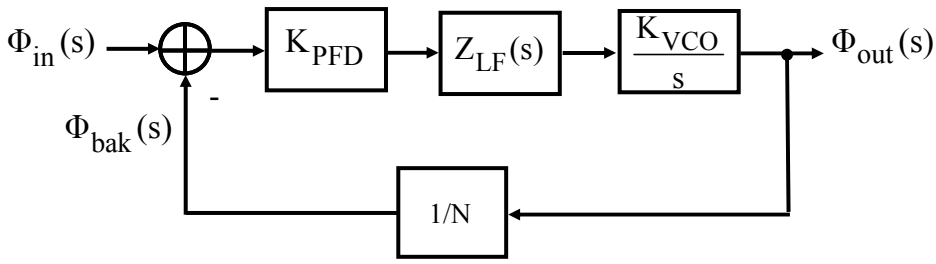


Figure 3.2: Linear model of PLL

The forward gain of the PLL is therefore derived as

$$G(s) = \frac{K_{PFD} Z_{LF}(s) K_{VCO}}{s}, \tag{3-1}$$

and the reverse loop gain is

$$H(s) = \frac{1}{N}, \tag{3-2}$$

then close loop transfer function of the model can be expressed as

$$H(s) = \frac{\Phi_{out}}{\Phi_{in}} = \frac{G(s)}{1 + G(s)H(s)} = \frac{\frac{K_{PFD} Z_{LF}(s) K_{VCO}}{s}}{1 + \frac{K_{PFD} Z_{LF}(s) K_{VCO}}{s \cdot N}}. \tag{3-3}$$

The order of PLL transfer function is determined by loop filter transfer. We consider a linear model charge-pump PLL and the loop filter transfer function is

$$Z_{LF}(s) = R + \frac{1}{sC}, \tag{3-4}$$

then we rewrite the close loop transfer function as

$$\begin{aligned} H(s) = \frac{\Phi_{out}}{\Phi_{in}} &= \frac{\frac{K_{PFD} K_{VCO}}{C}(sRC + 1)}{s^2 + s\frac{K_{PFD} K_{VCO}}{NC} RC + \frac{K_{PFD} K_{VCO}}{NC}} \\ &= \frac{\frac{K_{PFD} K_{VCO}}{C}(sRC + 1)}{s^2 + 2\delta\omega_n s + \omega_n{}^2} \end{aligned}. \tag{3-5}$$

Now by using the concept of control theory, the natural frequency ω_n and damping factor δ of the system can be derived as

$$\omega_n = \sqrt{\frac{K_{PFD} K_{VCO}}{N \cdot C}}, \quad \delta = \frac{RC}{2}\omega_n. \tag{3-6}$$

3.3 Types of noise sources in PLL

Using above linear model, we discuss the noise of PLL. The model with noise is shown in Figure 3.3. There are three noise sources in this model, $V_{n1}(s)$ is associated with PFD and charge pump and also known as the reference noise. $V_{n2}(s)$ is introduced by loop filter's component and $V_{n3}(s)$ is phase noise generated by VCO.

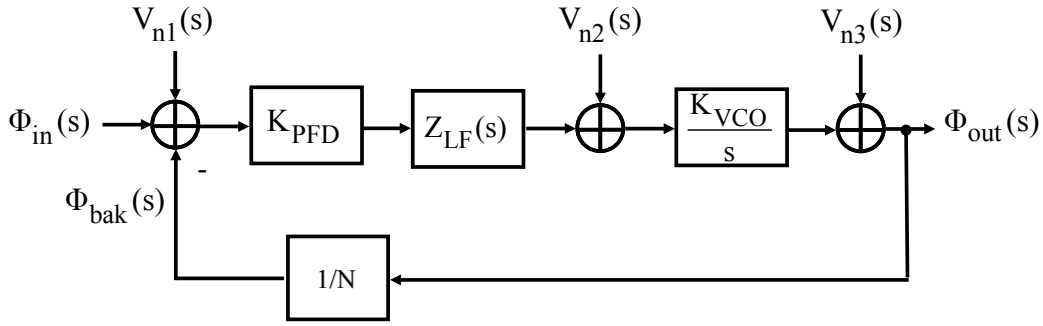


Figure 3.3: Noise sources in a PLL

The noise transfer function of reference noise is low pass while that of VCO phase noise is high pass. If reference noise varies rapidly, then output phase does not fully track the variations. In other words, slow jitter at the input propagates to the output unattenuated but fast jitter does not. On the other hands, slow jitter components generated by the VCO are suppressed but fast jitter components are not. Figure 3.4 conceptually summarizes the response of PLL to input jitter and VCO jitter. Depending on the application and the environment, one or both sources may be significant, requiring on optimum choice of the loop bandwidth [10].

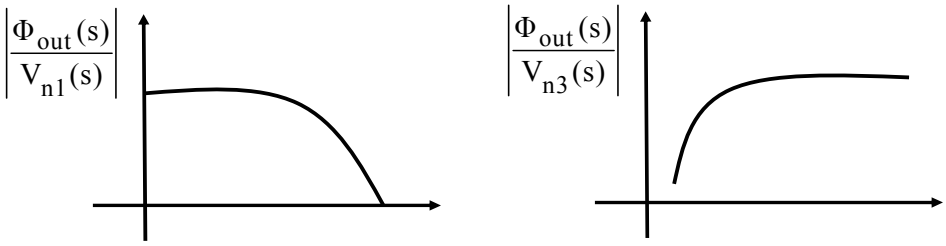


Figure 3.4: Transfer function of noise sources

3.4 Fractional-N Frequency Synthesis

Due to the limitation of EMI, we need generate SSC function for SATA specification. We modulate divider to achieve the goal in this design. The 5000 ppm deviation of SSC specification is too small and it is impossible to use several dividers with large division ratio to realize it. The use fractional-N frequency synthesis has the advantage of synthesize non-integer multiple output frequency with a fixed reference signal. As sown in Figure 3.5, we can use a dual modulus prescaler to divide VCO's output frequency by either N or N+1. Together, two synchronous counters are combined to construct a variable frequency divider [11].

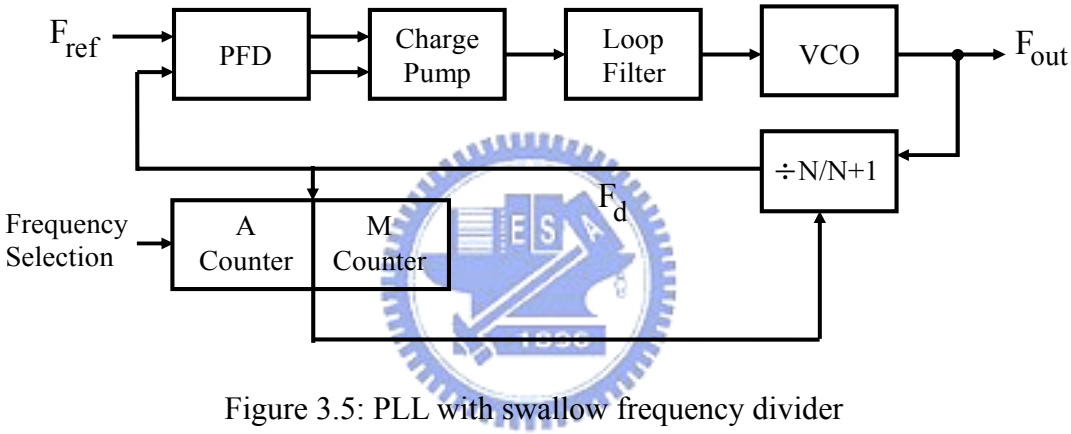


Figure 3.5: PLL with swallow frequency divider

Initially, both /A counter and /M counter start in the same time. The PLL track and lock at divider by N+1 during the cycle of /A counter and /A counter will be disabled. Then the divider jump to N until /M counter is overflow. Then both /A counter and /M counter start again and the divider back to N+1. And go on and go on and on, with $(N+1)\cdot A + N\cdot(M-A) = M\cdot N + A$ cycles of input signal, the divider division ratio is average to $N+\frac{A}{M}$. Frequency divider division ratio includes an integer number plus a fractional number, and fractional-N PLL can easily achieve fine resolution with high operation frequency.

However, this structure has a serious problem that will result in saw tooth phase error in PFD. This periodic phase error will be the frequency modulated by the VCO and generate fractional spurs in the output spectrum. As shown in Figure 3.6, the periodical switch signal of divider ratio will result in sawtooth phase error in PFD output. The phase error can be calculated as

$$
\begin{aligned}
e_q(Clk) &= Modulus(Clk) - N - \frac{A}{M} \\
Modulus(Clk) &= \begin{cases} N+1 & 0 < ((Clk))_M \le A \\ N & A < ((Clk))_M \le M \end{cases}, \\
\varphi_e(Clk) &= 2\pi \times \sum_{i=0}^{Clk} e_q(i)
\end{aligned}
\tag{3-8}
$$

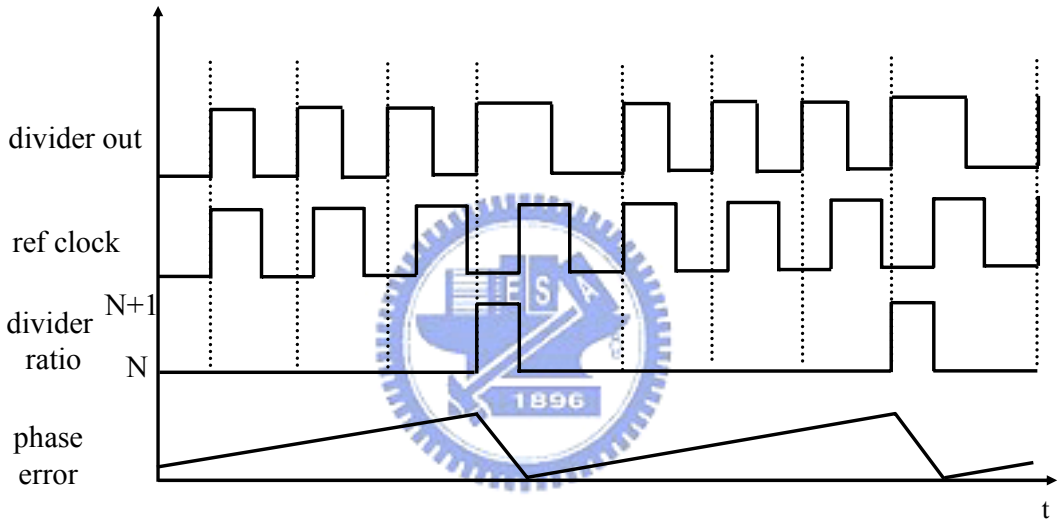


Figure 3.6: Sawtooth phase error

This periodic phase error will be frequency modulated by the VCO and generate fractional spurs in the output spectrum. As shown in Figure 3.7, the resulting fractional spurs is typically only 20 or 30 dB below center frequency and will serious degrade the purity of output spectrum [12].

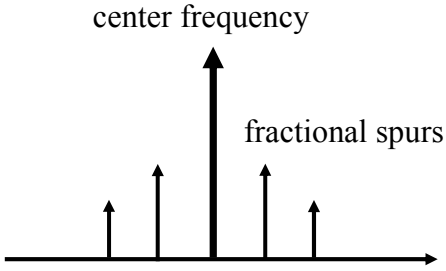


Figure 3.7: Spurious noise in VCO output spectrum

3.5 Delta-Sigma Modulator

Delta-sigma modulator is widely used for ADC and DAC application which can push the quantization noise to higher frequency [13]. As shown in Figure 3.8, the idea of delta-sigma modulator is add an integrator in the input and a differentiator behind the quantizer then push the quantization noise to higher frequency. In conventional delta-sigma Digital-to-Analog converters, the output of the modulator is followed by an analog low pass filter in order to remove quantization noise. Due to low pass characteristic of PLL, the out band quantization noise can be suppressed by higher order poles.

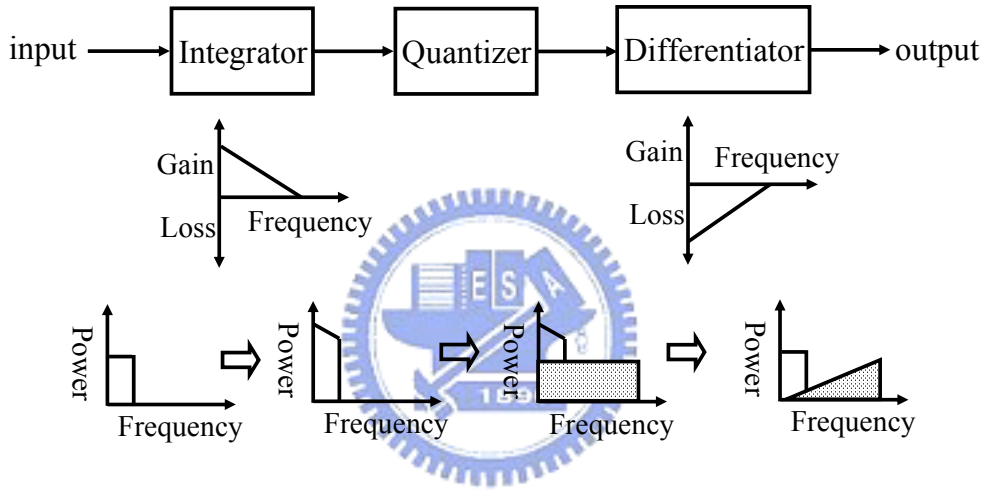


Figure 3.8: Theory of delta-sigma modulator

A first order delta-sigma modulator including an integrator, a quantizer and a differentiator is shown in Figure 3.9. Both integrator and differentiator are first order and quantizer is usually two-level. The original architecture of first order delta-sigma modulator encounters overflow problem. In order to solve this problem, we can put subtraction of differentiator to the input as a negative feedback system and the transfer function does not change. Figure 3.10 shows the improved first order delta-sigma modulator.

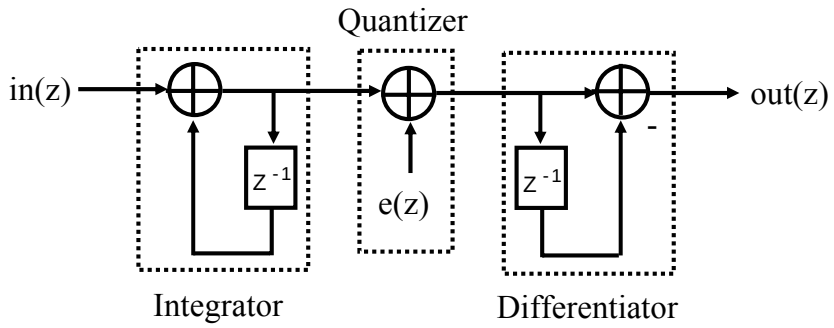


Figure 3.9: Original architecture of first order delta-sigma modulator

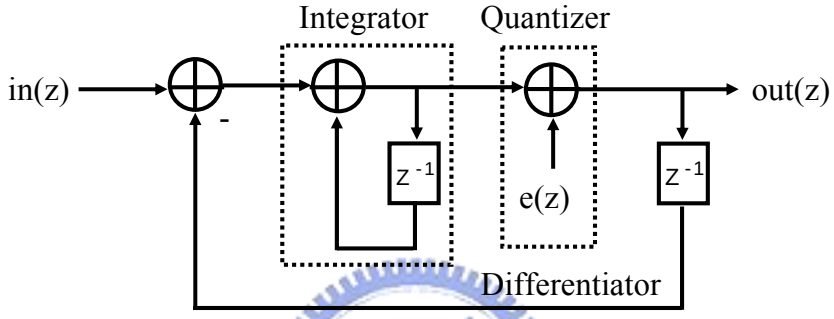


Figure 3.10: Modified architecture of first order delta-sigma modulator

In z domain, the transfer function of first order delta-sigma modulator can be written as

$$out(z) = in(z) + (1 - z^{-1}) \cdot e(z), \tag{3-9}$$

where *in(z)* and *out(z)* are modulator input and out, *e(z)* is the quantization, respectively. In above equation, $1 - z^{-1}$ term is referred to as NTF (Noise Transfer Function). It is known that an additional zero in the origin will make transfer function slope sharper by 20 dB/dec. Using more zeros at the origin can push the quantization noise to higher frequency. The NTF of higher order delta-sigma modulator can be written as $(1 - z^{-1})^m$, where m is the order of modulator.

With the NTF of modulator, the modulated power spectrum density can be calculated. The detail mathematical calculation is refer to [14], and the power spectrum density of NTF can be written as

$$L(f) = \frac{(2\pi)^2}{12 f_S} \cdot \left[2\sin(\pi \frac{f}{f_S}) \right]^{2(m-1)}, \qquad (3\text{-}10)$$

where f_S is oversampling rate and m is order of delta-sigma modulator. The phase noise generated by quantization noise of delta-sigma modulator is plotted with second order, third order and fourth order structures as in Figure 3.11.

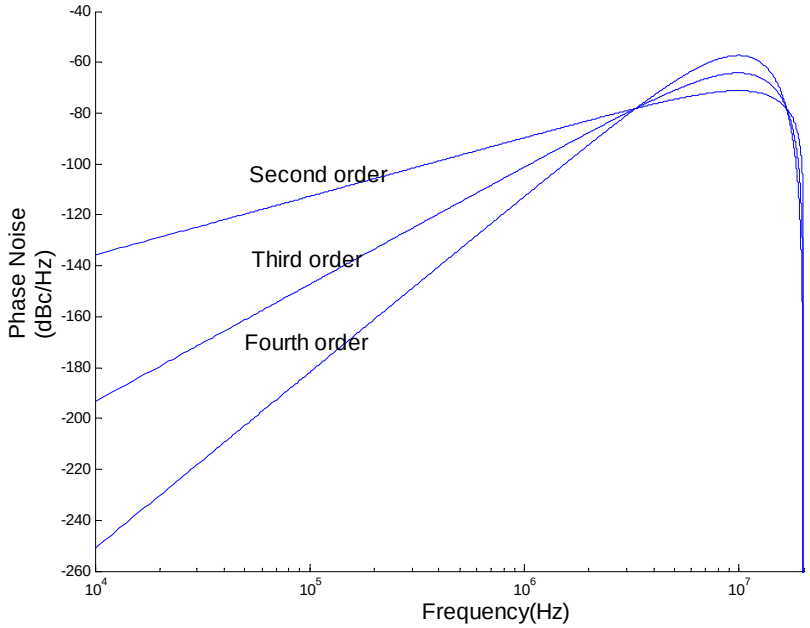


Figure 3.11: Quantization noise of first to third delta-sigma modulator

With the quantization set to two-level, an all digital delta-sigma modulator called DPA (*Digital Phase Accumulator*) can be converted to the form given by Figure 3.12. The adder in DPA can be represented as an accumulator with overflow. Residue that is the difference between overflow and sum of accumulator delays a cycle and connect to the input of adder.

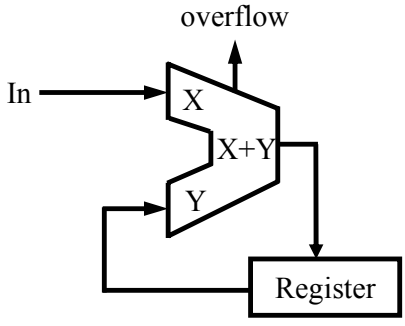


Figure 3.12: Digital phase accumulator

3.6 MASH 1-1-1 Delta-Sigma Modulator

Higher order delta-sigma modulator can suppress quantization noise effectively, but they tend to become "unstable". The single-loop architecture offers a higher flexibility in terms of noise shaping; however, it has instability problem and is more complex.

Multi-Stage-Noise-Shaping (MASH) can solve instability problem and design is easily. As shown in Figure 3.13, a third order MASH 1-1-1 is formed by cascading three first order delta-sigma modulator [15]. The quantization error of the first modulator is fed to the second modulator and the second modulator's quantization error is fed to the third.

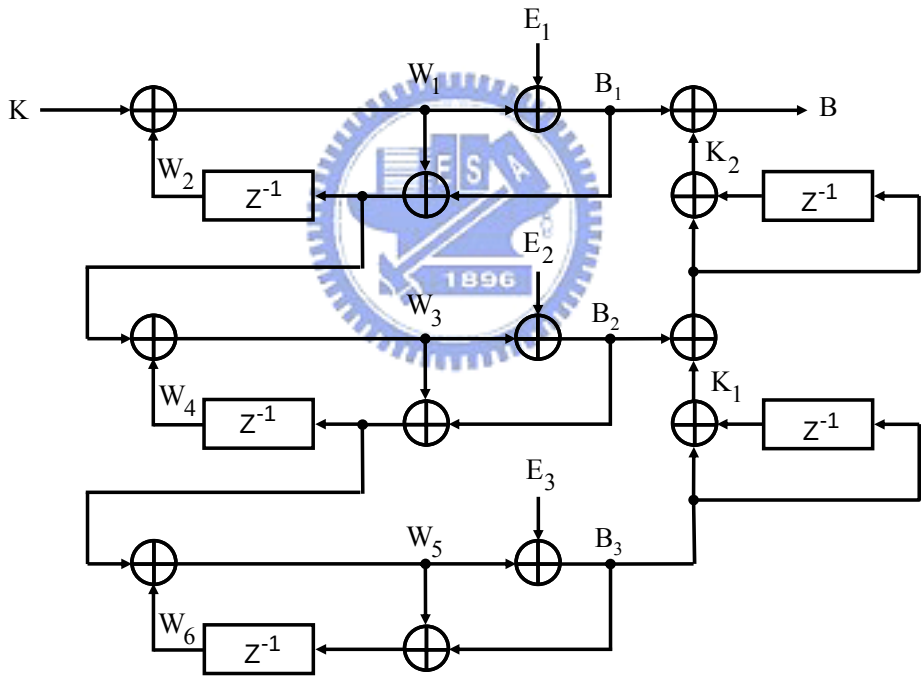


Figure 3.13: Third order MASH 1-1-1 delta-sigma modulator

The equations of the individual modulators can be written as

$$\begin{aligned} B_1(z) &= K(z) + E_1(z)\cdot(1 - z^{-1}) \\ B_2(z) &= -E_1(z) + E_2(z)\cdot(1 - z^{-1}) \\ B_3(z) &= -E_2(z) + E_3(z)\cdot(1 - z^{-1}) \end{aligned}, \qquad (3\text{-}11)$$

where $E_1(z)$, $E_2(z)$ and $E_3(z)$ each represents the quantization noise of the three

modulators. Combination of above equations, the transfer function of MASH 1-1-1 delta-sigma modulator is

$$B(z) = K(z) + E_3(z) \cdot (1 - z^{-1})^3 . \tag{3-12}$$

The quantization error of third modulator is noise shaped by placing three zeros at the origin. Using DPA to realize MASH 1-1-1 architecture is shown in Figure 3.14. The advantages of MASH structure are the immunity of instability and all digital implementation avoiding process variation.

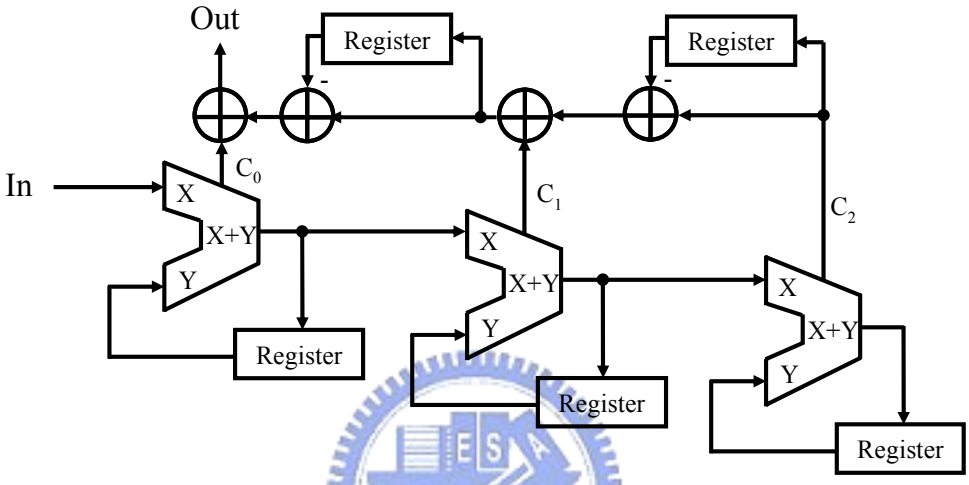


Figure 3.14: Digital realization of MASH 1-1-1

3.7 Mechanism of Fractional-N PLL with DSM

A fractional-N PLL with delta-sigma modulator is shown in Figure 3.15. The delta-sigma modulator is MASH 1-1-1 architecture. Set the wanted word of length to the input of MASH which output control the divider ratio. When overflow occurs, the divider ratio changes to N+1 from N. On average, by a fractional value between N and N+1, we can get the wanted division ratio as

$$N_{div} = N + \frac{L_{div}}{L_{acc}}, \tag{3-13}$$

where L_{acc} is the length of accumulator. The fractional-N PLL can have a high resolution by using wider accumulator length.

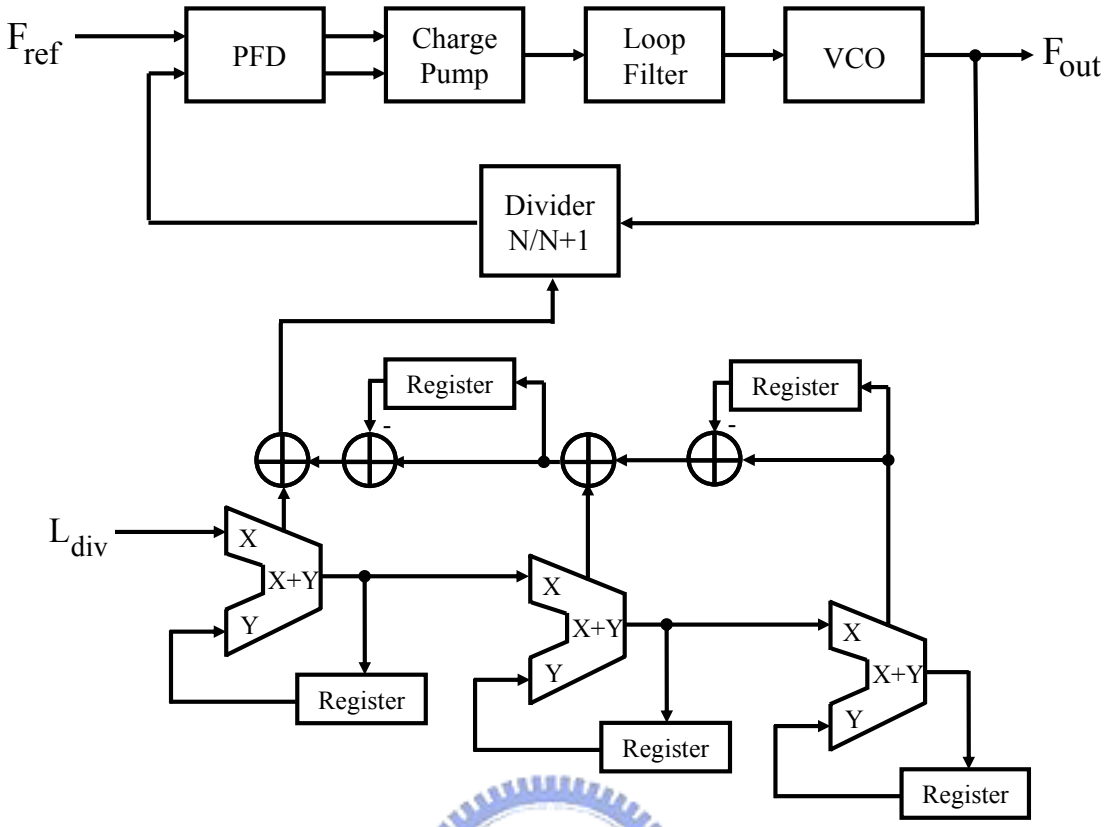


Figure 3.15: A fractional-N PLL with delta-sigma modulator

Chapter 4

Spread Spectrum Clock Generator

4.1 Spread Spectrum Clock Generator Architecture

A building block of the proposed *Spread Spectrum Clock Generator* (SSCG) is shown in Figure 4.1. The SSCG is based on a fractional-N PLL using delta-sigma modulation technique to modulate the divider. The fractional-N frequency synthesizer consists of a conventional PLL, an address generator, and a delta-sigma modulator. The divider output clock of the PLL uses the address generator to produce a triangular waveform of 30~33 kHz, 5000 ppm frequency deviation as the control signal of the delta-sigma modulator. Using a delta-sigma modulator, the multi-bit word coming from the address generator is converted into a random bit stream which can toggle the multi-modulus divider between 2 dividers. Therefore the high frequency resolution with the same reference clock can easily be achieved with reasonable control signal. Modulation signals are generated by periodically switching the multi-modulus divider between two different numbers in the feedback path and the specified spread amounts can be achieved to produce *Spread Spectrum Clocking* (SSC).

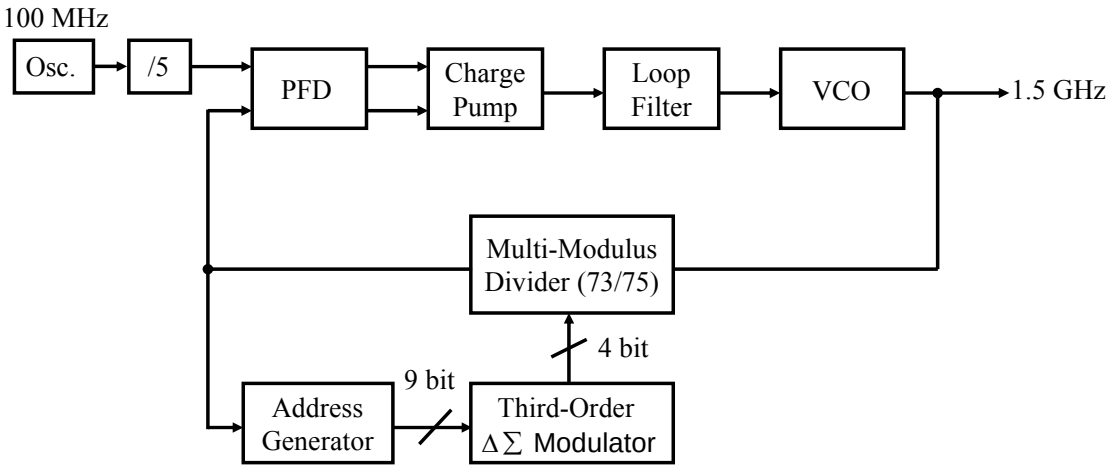
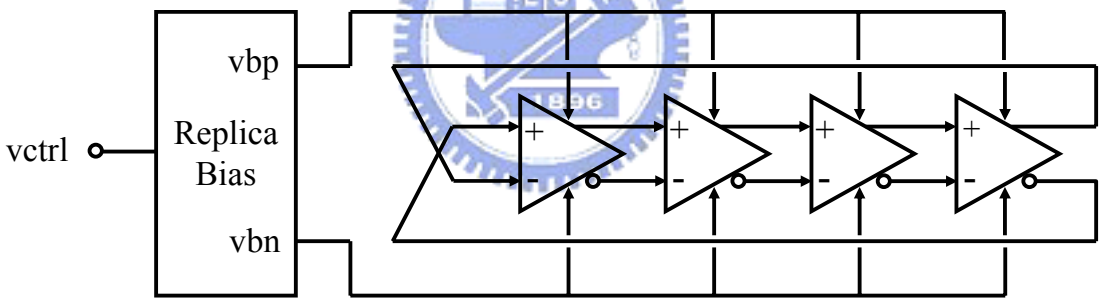


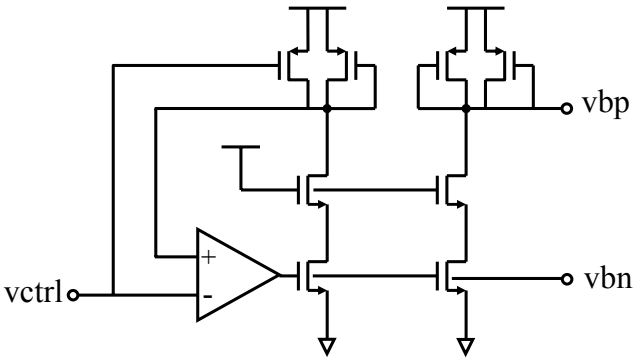
Figure 4.1: Spread spectrum clock generator

■ Voltage Controlled Oscillator

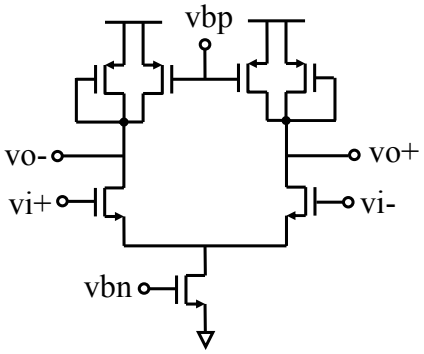
Figure 4.2 shows the circuit schematic of the VCO, which includes a 4-stage ring oscillator and a bias voltage generator for frequency tuning [16]. The delay cell of ring oscillator is a differential pair with symmetric active loads.



(a) VCO



(c) Bias voltage generator



(b) Symmetric active loads

Figure 4.2: Circuit schematic of VCO

As shown in Figure 4.3, the I-V curve of symmetric loads is like a resistance. This characteristic is a merit for better linearity of VCO gain and wider oscillation swing. In order to keep the I-V curve characteristic of symmetric loads for the variation of P.V.T., the bias generator can adjust bias current of delay cell dynamically.

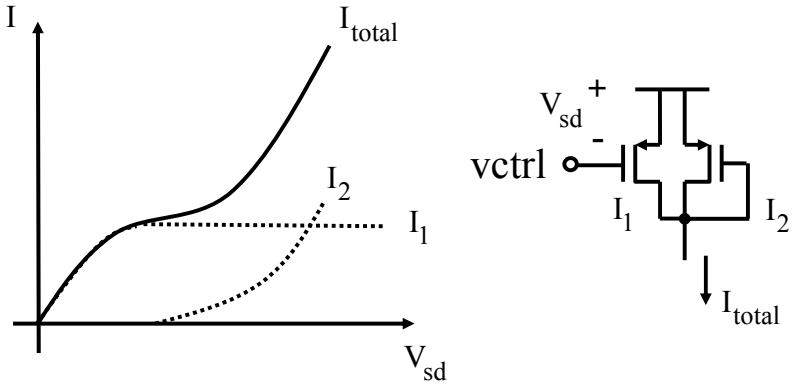


Figure 4.3: I-V characteristic of symmetric loads

■ Phase Frequency Detector

The *Phase Frequency Detector* (PFD) is composed of two D-flip flops and a NOR gates, as shown in Figure 4.4 [17]. It has an advantage of zero dead zone. The *True Single Phase Clock* (TSPC) type D-Latch is for the high speed operation. The conventional PFD generates phase jitter since it does not have sufficient turn on time to change the control voltage when phase difference is within the dead zone. Adding an appropriate delay to ensure PFD working accurately even there is little phase difference between reference clock and feedback signal. The timing block, as shown in Figure 4.5, shows how PFD works when input is in phase or out of difference.

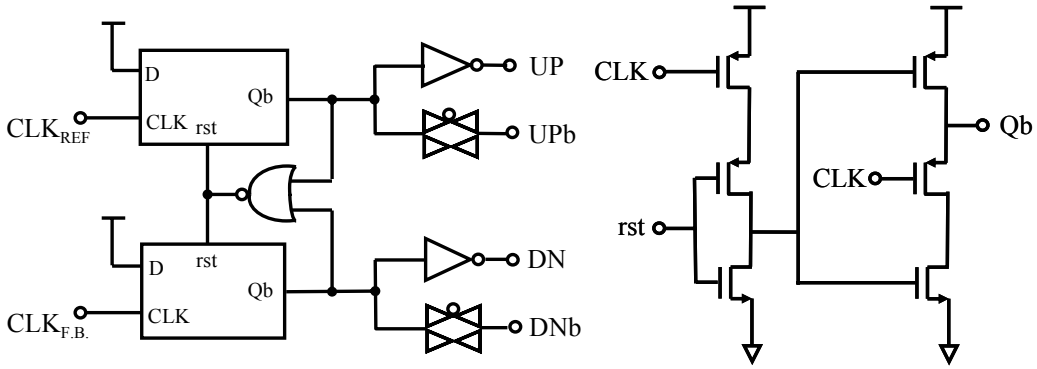


Figure 4.4: Phase frequency detector

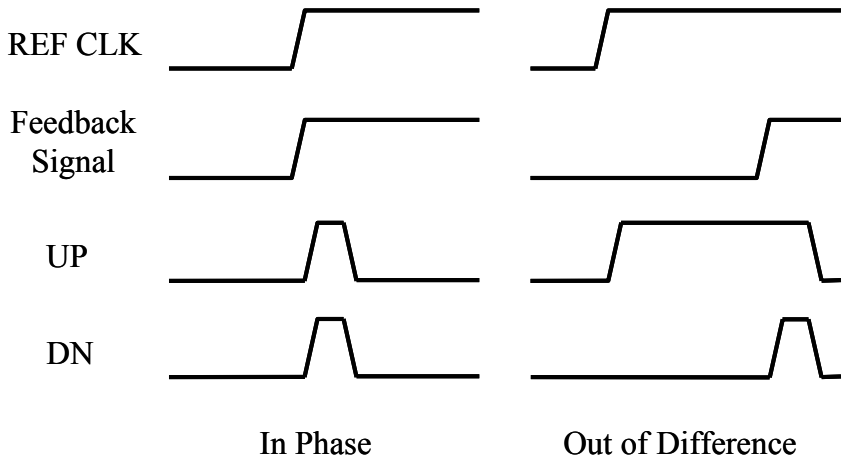


Figure 4.5: The output waveforms of PFD

■ Charge Pump

The purpose of charge pump is charge or discharge the loop filter to vary the frequency of VCO by changing the control voltage. The charge pump loop is shown in Figure 4.6 [18], it consists of two current source, four current switches and an OP. A unity-gain buffer is used to clamp the terminal voltages of current sources during the zero-current pumping period. In this way, voltage glitches on the loop filter due to charge sharing can be eliminated.

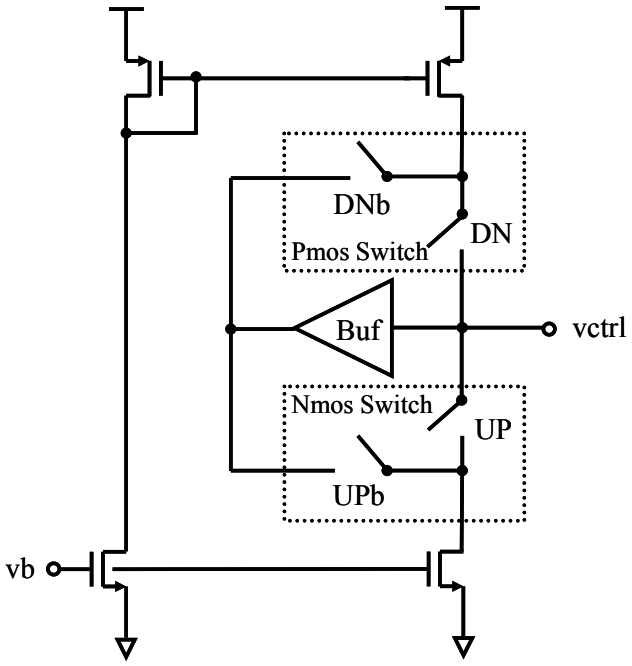


Figure 4.6: Charge pump

■ 3rd order MASH Delta-Sigma Modulator

Due to that using fractional-N PLL can easily achieve fine resolution with high operation frequency, we can use a dual modulus prescaler to divide VCO's output frequency by either N or N+1. Together, two synchronous counters are combined to construct a variable frequency divider. This structure, however, have a serious problem that will result in saw tooth phase error in PFD. This periodic phase error will be the frequency modulated by the VCO and generate fractional spurs in the output spectrum. A delta-sigma modulator can leave the average input unchanged and modulate the quantization noise to higher frequency. In conventional delta-sigma Digital-to-Analog converters, the output of the modulator is followed by an analog low pass filter in order to remove quantization noise. In this system, the out-band quantization noise can be filtered by the low-pass characteristic of the PLL. Higher order delta-sigma modulator can suppress quantization noise effectively but single-loop architecture has instability and is more complex. MASH (*multi-stage-noise-shaping*) can solve instability problem and can be implemented using all digital architectures. Thus, it can be easily integrated into single chip and is insensitive to process variation.

A 3rd order MASH 1-1-1 delta-sigma modulator, which is formed by cascading three first order sigma-delta modulator is illustrated in Figure 4.7. By performing linear analysis on this model, the input/output relationship of this modulator can be found as follow

$$B(z) = K(z) + E_3(1 - z^{-1})^3, \tag{4-1}$$

where $K(z)$, $B(z)$, and $E_3(z)$ are the Z-transform of the input, output and quantization noise from three stages respectively. It is shown that the quantization error is shaped and pushed to high frequency by placing three zeros at the origin and then the closed loop behavior of PLL will filter it out. The digital realization of MASH 1-1-1 delta-sigma modulator is shown in Figure 4.8.

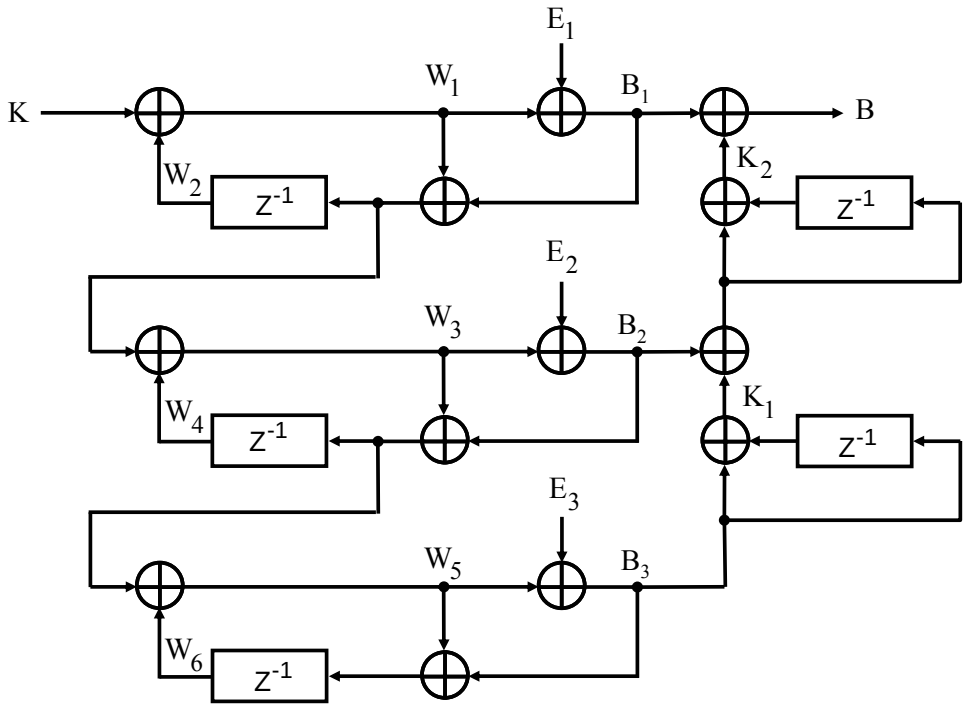


Figure 4.7: 3rd order MASH 1-1-1 delta-sigma modulator

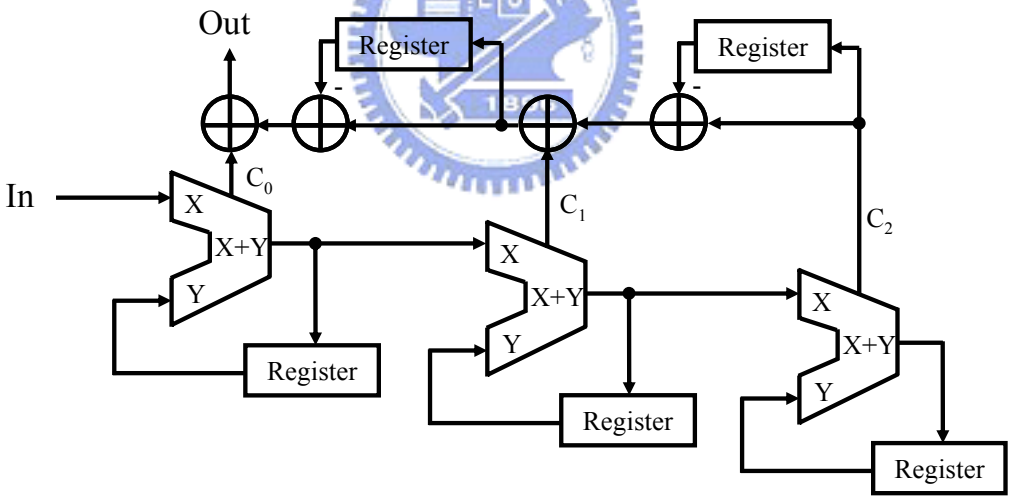


Figure 4.8: Digital realization of MASH 1-1-1

■ Multi-Modulus Divider

The MASH modulator is unavoidably spreading the possible output sequence into multi-bit states. In order to produce a fractional division of N that equals n + fraction, the output of third order MASH 1-1-1 delta-sigma modulator is spread to n-3, n-2, n-1, n, n+1, n+2, n+3 and n+4. As shown in Figure 4.9 [19], the multi-modulus

divider is composed of six cascaded 2/3 dividers and some simple logic and is capable of dividing by these divisions. The division ratio is

$$N = 64 + 2^5 \cdot 0 + 2^4 \cdot con3 + 2^3 \cdot \mathrm{con}^2 + 2^2 \cdot con1 + 2^1 \cdot \mathrm{con}^0 + 2^0, \quad (4\text{-}2)$$

where, *con*3, *con2*, *con*1 and *con*0 are the weights for the determination of the division modulus.

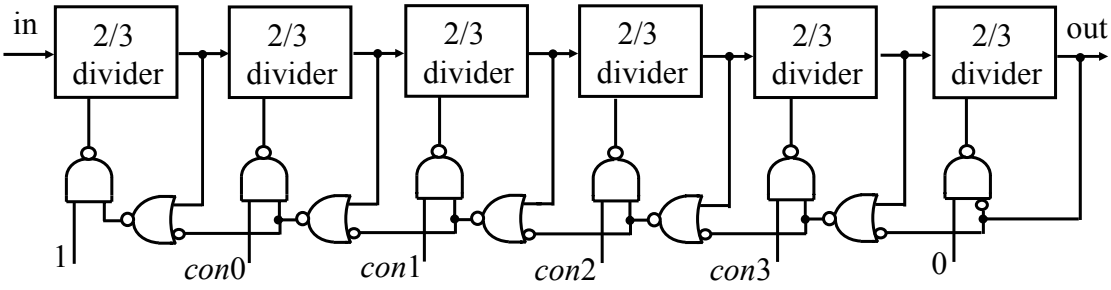


Figure 4.9: Multi-modulus divider

■ Address Generator

The *Serial-ATA* (SATA) systems require spread spectrum clock with 30~33 kHz, 5000 ppm frequency modulation. One can use address generator to determine the above required parameter. As shown in Figure 4.10, the address generator consists of a divider, up/down counter, control logics and a SR latch. The divider determines the modulation rate and control logics control the frequency deviation of the SSCG. The output of up/down counter oversampled by the delta-sigma modulator can produce a triangular waveform. The more bit number of up/down counter is used, the more accurate shape of triangular waveform will be.

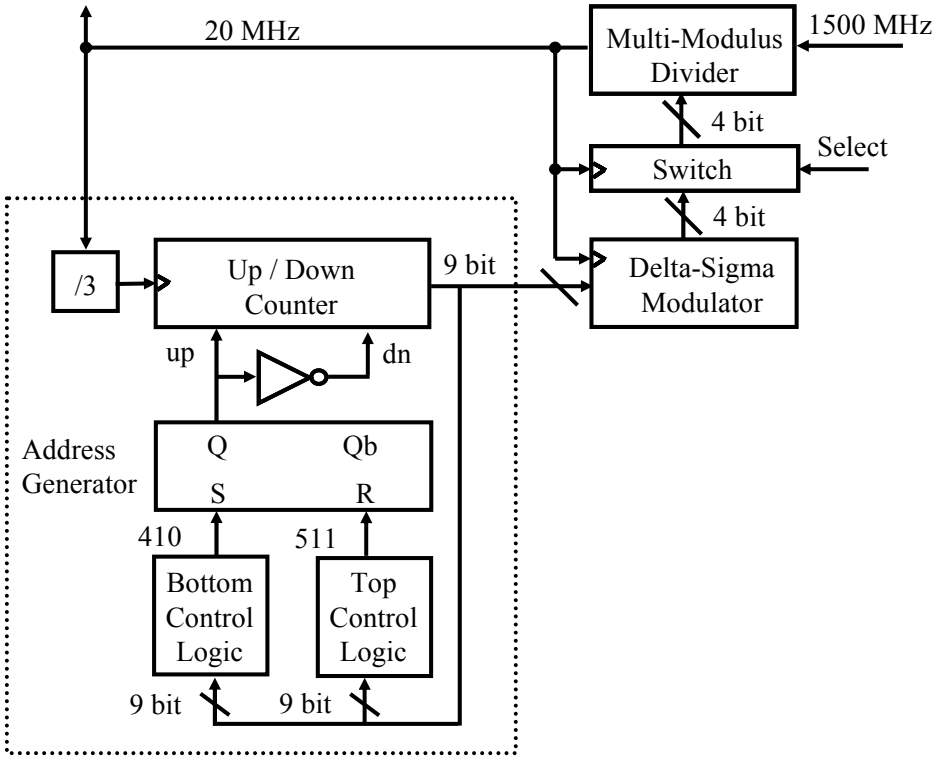


Figure 4.10: Address Generator

■ Loop Filter

The loop filter determines most of the PLL specifications. Generally, we can design filter using open loop gain bandwidth and phase margin to determine the passive component values. As shown in Figure 4.11, we consider 2nd loop filter to design type-II charge pump PLL system. Locating the point of minimum phase shift at the unity gain frequency of the open loop response ensures loop stability.

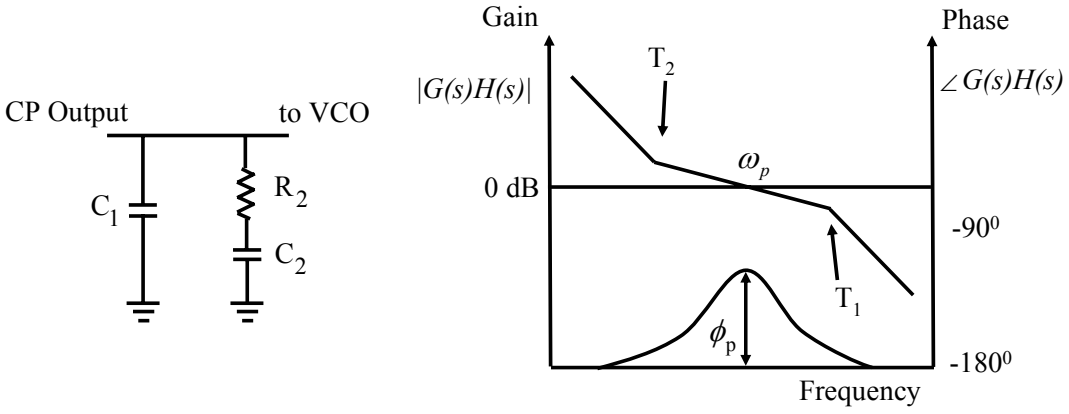


Figure 4.11: Schematic and bode plot of second order filter

The impedance of 2nd filter in Figure 4.11 is

$$Z(s)=\left[\left(R_2+\frac{1}{sC_2}\right)//\frac{1}{sC_1}\right]=\frac{1}{s(C_1+C_2)}\frac{sR_2C_2+1}{sR_2(C_1//C_2)+1}. \quad (4\text{-}3)$$

Define the time constants which determine the pole and zero frequencies of the filter

$$T_1=R_2(C_1//C_2), \quad (4\text{-}4)$$

$$T_2=R_2C_2. \quad (4\text{-}5)$$

According [20], we can calculate some equations to get passive component values as

$$C_1=\frac{T_1}{T_2}\frac{K_{PFD}K_{VCO}}{\omega_p{}^2N}\sqrt{\frac{1+(\omega_p\cdot T_2)^2}{1+(\omega_p\cdot T_1)^2}}, \quad (4\text{-}6)$$

$$C_2=C_1\left(\frac{T_2}{T_1}-1\right), \quad (4\text{-}7)$$

$$R_2=\frac{T_2}{C_2}, \quad (4\text{-}8)$$

where ω_p, K_{PFD}, K_{VCO}, N are loop bandwidth, gain of phase frequency detector, gain of VCO and divider ration. We need design this component values carefully to ensure system stability. A common rule of thumb is to begin design with a 45^0 phase margin.

The out-band quantization noise from delta-sigma modulator will be suppressed by the low-pass characteristic of the PLL. But delta-sigma modulator will introduce current switching noise in the divider and charge pump at the reference rate. This may cause unwanted FM sidebands at RF output. As shown in Figure 4.12, an additional pole of 3rd order loop filter can be added to suppress the reference spur. The added attenuation from the low-pass filter is

$$ATTEN = 20 \log [(2 F_{ref} R_3 C_3)^2 +1]. \quad (4\text{-}9)$$

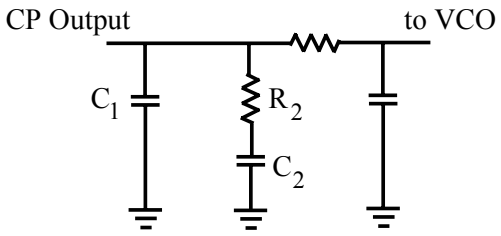


Figure 4.12: 3rd order loop filter

The PLL becomes a high order loop and stability is an important issue. So, one must be careful in determining the loop bandwidth of the system. A PLL needs a sufficiently large loop bandwidth to track the modulation frequency of SSCG. But, we need to choose a small loop bandwidth to suppress the reference spur and RMS phase error. In general, the loop bandwidth need to meet the RMS phase error to reduce jitter and it is sufficient to track the modulation frequency.

According to [21], the dynamic range of the Lth-order delta-sigma modulator should meet the following condition.

$$\frac{3}{2}\cdot\frac{2L+1}{\pi^{2L}}\cdot(OSR_{eff})^{2L+1} > \left(\frac{f_{PFD}}{\Delta f_n}\right)^2, \tag{4-10}$$

where OSR_{eff}, f_{PFD}, Δf_n are the oversampling ratio and the bandwidth of the phase frequency detector and in-band noise respectively. So the approximate upper bound of the loop bandwidth is obtained as

$$f_c < \left[\left(\frac{\theta_{rms}}{\sqrt{2}}\right)^2\cdot\frac{L+0.5}{(2\pi)^{2L}}\right]^{(1/2L-1)}\cdot f_{PFD}, \tag{4-11}$$

where θ_{rms} [rms rad] is the in-band phase error. In this design, when the frequency of PFD is 20 MHz, the upper bound of the bandwidth of a 3rd order delta-sigma modulator to have less than 1^0 RMS phase error is about 120 KHz.

Chapter 5

Simulation and Measurement Results

The spread spectrum clock generator using fraction-N PLL with delta-sigma modulator has many system design issues. We need consider some problem including stability problem, loop bandwidth, digital and analog parts in the same system and spread spectrum clocking function. Since the IC design flow from system design, simulation, chip layout, foundry fabrication and measurement takes several months, system simulation is very important. Circuit level simulation such as SPICE is complicated and time consuming, especially taking the PLL with digital MASH structure into consideration. In this chapter, we verify the spread spectrum clocking function from behavior simulation to SPICE simulation. Finally, we show the measurement results of our spread spectrum clock generator design.

5.1 Simulation of Delta-Sigma Modulator

`The Bode plot of ideal NTF (*Noise Transfer Function*) and frequency response of behavior model simulation using MATLAB for MAH 1-1-1 delta-sigma modulator is shown in Figure 5.1. It achieves good approximation of -60dB decay of the noise power.

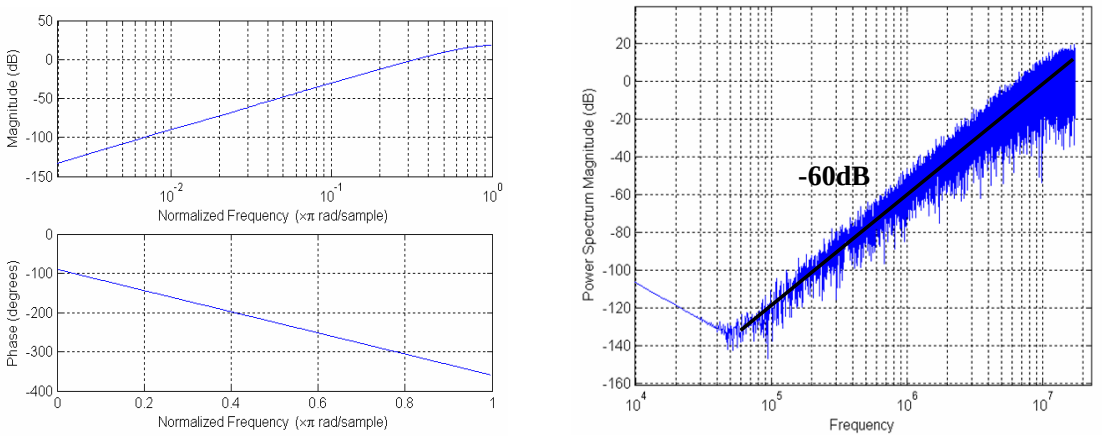


Figure 5.1: Bode plot of NTF and frequency response of behavior model

5.2 SSCG Behavior Simulation

The close loop simulation with SPICE takes a lot of time, we can use SIMULINK to analyze the loop stability and verify the SSC function. As shown in Figure 5.2, the charge pump is modeled by a voltage gain and VCO is modeled a voltage to frequency component. The transfer function of loop filter determines stability and order of the PLL system.

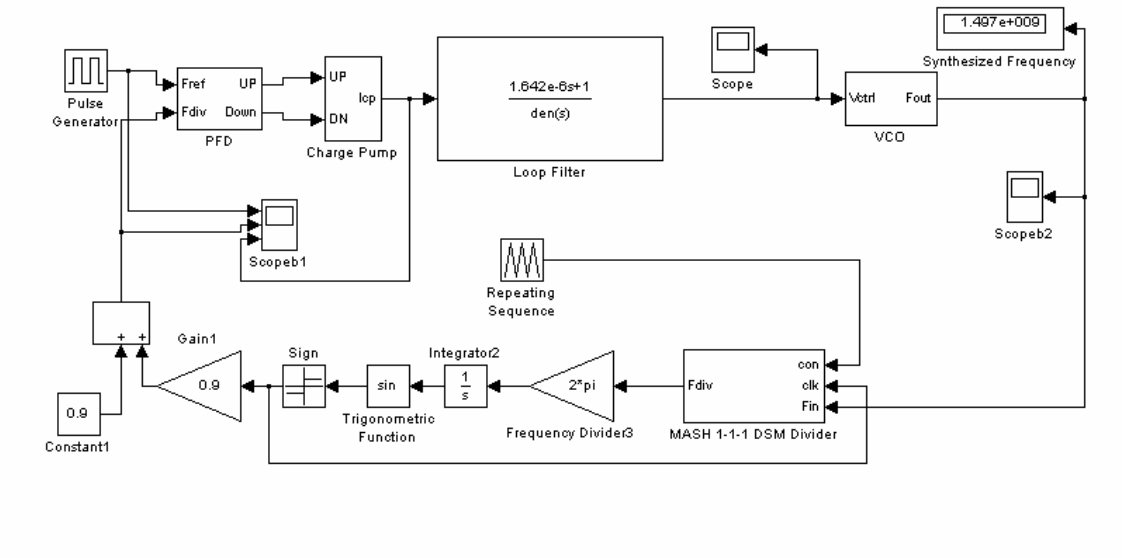


Figure 5.2: Behavior simulation of SSCG using SIMULINK

Figure 5.3 shows the Bode plot of SSCG system and the SSCG behavior simulation. We can see the 33 KHz, 5000 ppm frequency modulation with triangular waveform obviously.

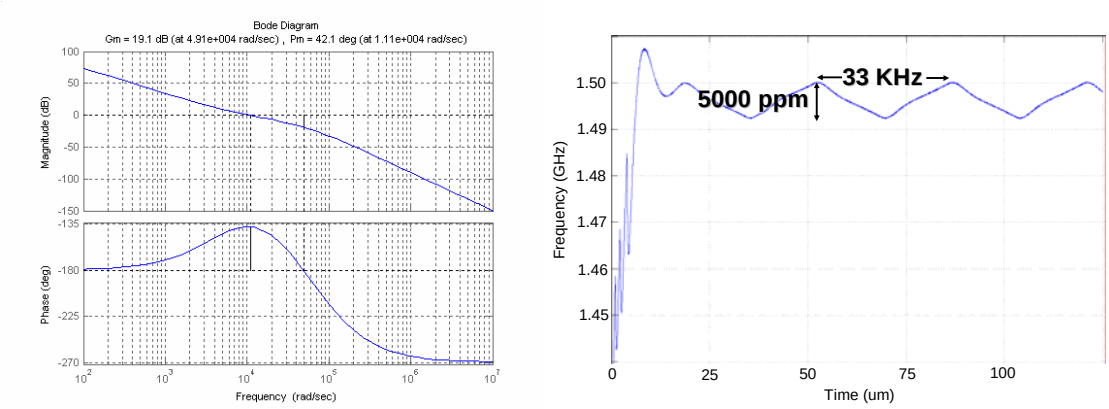


Figure 5.3: Bode plot of SSCG system and the SSCG behavior simulation

5.3 SSCG Circuit Level Simulation

The circuit level simulation analyzes voltage and current in every transistor node. The simulation using SPICE takes a significant amount of time but the results are more precise. Figure 5.4 shows the post-layout simulated eye diagram from a 1.5 GHz non-SSC fractional-N PLL output. The peak to peak jitter is 8 ps. Figure 5.5 shows the control voltage of VCO from a 1.5 GHz SSC PLL. We can see a frequency modulation by triangular waveform obviously.

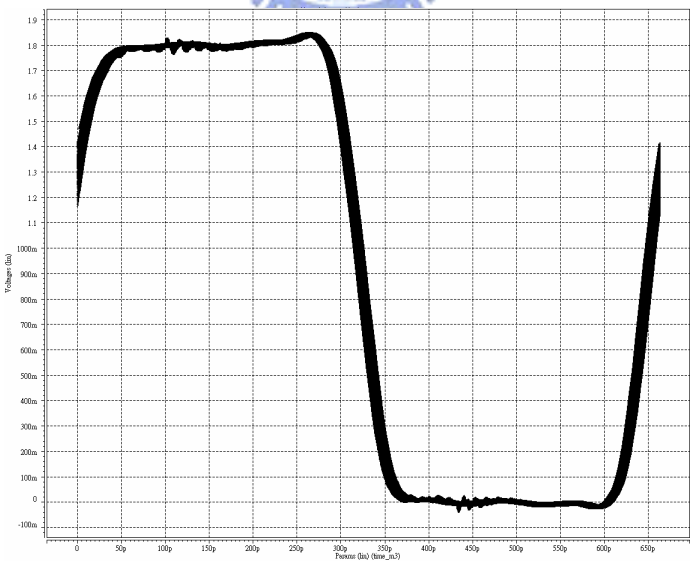


Figure 5.4: Eye diagram of non-SSC output

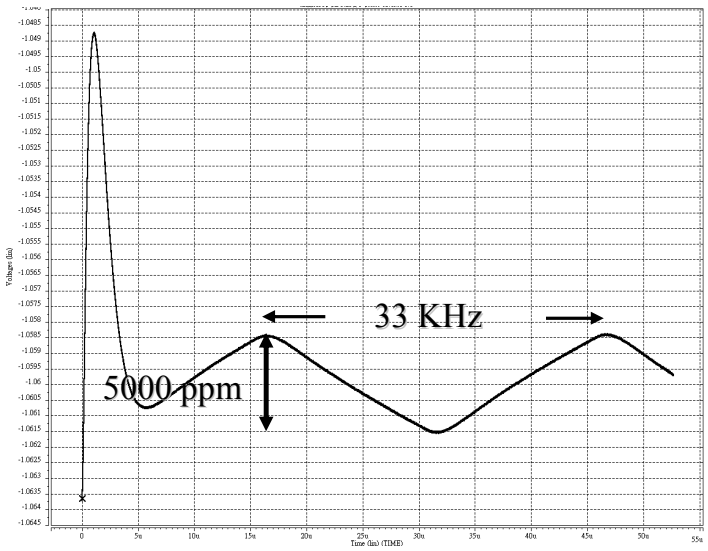


Figure 5.5: Control voltage of VCO

5.4 Testing Setup

Considering the speed and noise issues, the IC is un-packaged to reduce parasitic loading of the packages. Figure 5.6 is the SSCG die photo and die area is 1000um by 1000um. The chip is implemented in TSMC 0.18 um CMOS 1P6M technology.

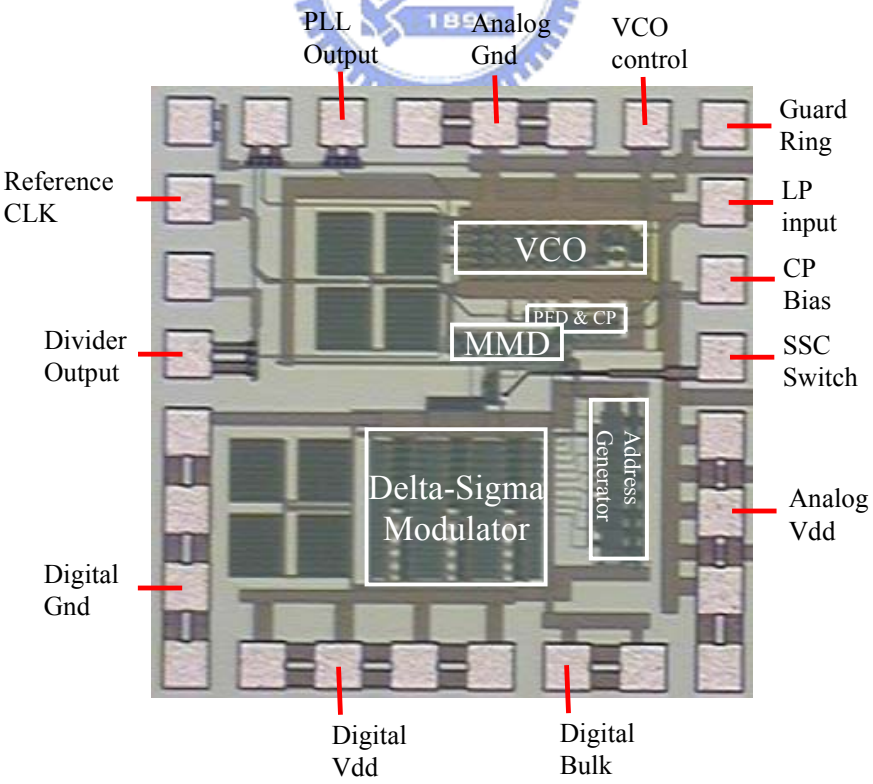


Figure 5.6: Microphotograph of die

Figure 5.7 is the photograph of testing board. External charge pump bias resistance is used to adjust the charge pump current. A SSC switch is used to select non-SSC or SSC mode. Use external third order filter to determine the parameter of PLL system.

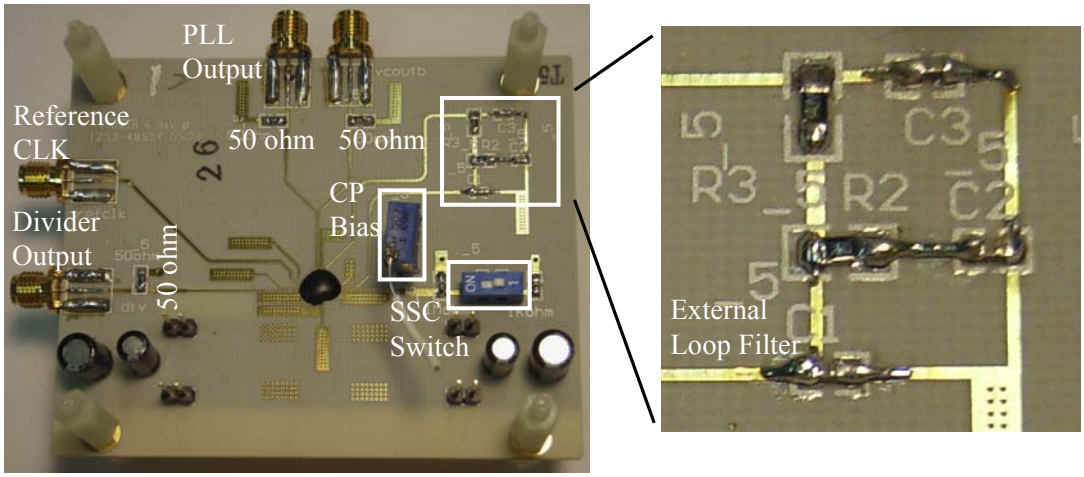


Figure 5.7: Photograph of testing board

The measurement setup is shown in Figure 5.8. Pulse data generator is used to send a 100 Mega Hz reference clock to PLL. Wide-Bandwidth Oscillator is used to show the divider and VCO output waveform of PLL. Spectrum Analyzer is used to show the spectrum of SSCG output.

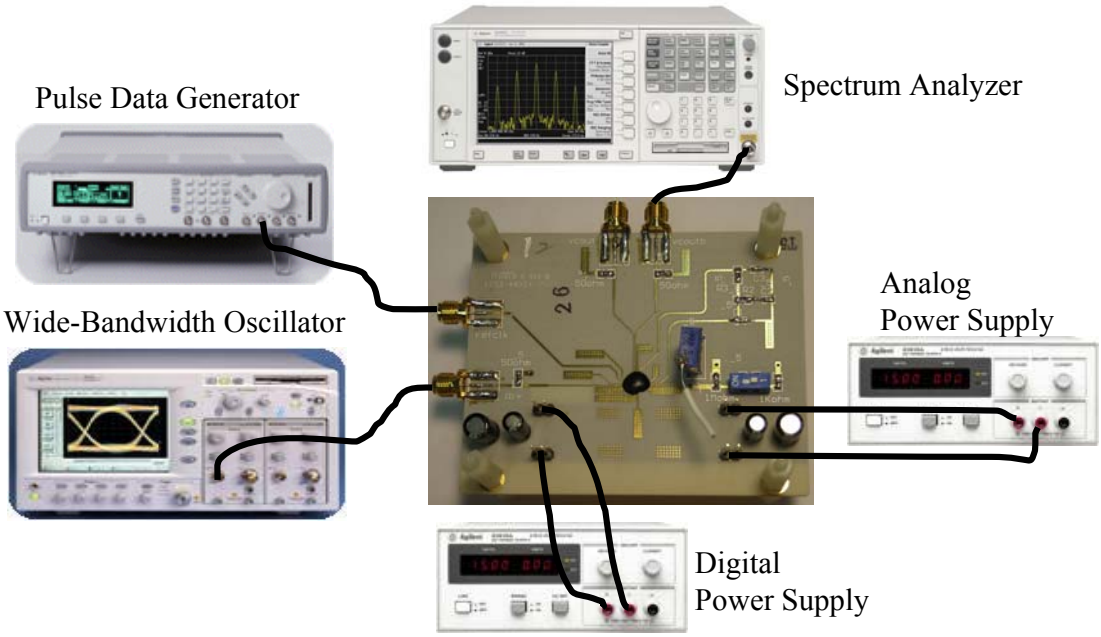


Figure 5.8: Measurement setup

5.5 Measurement Results

Figure 5.9 shows the eye diagram from a 1.5 GHz non-SSC PLL output. The peak to peak jitter is 80 ps.

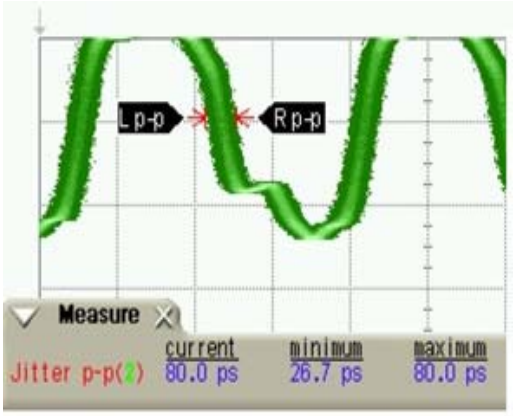
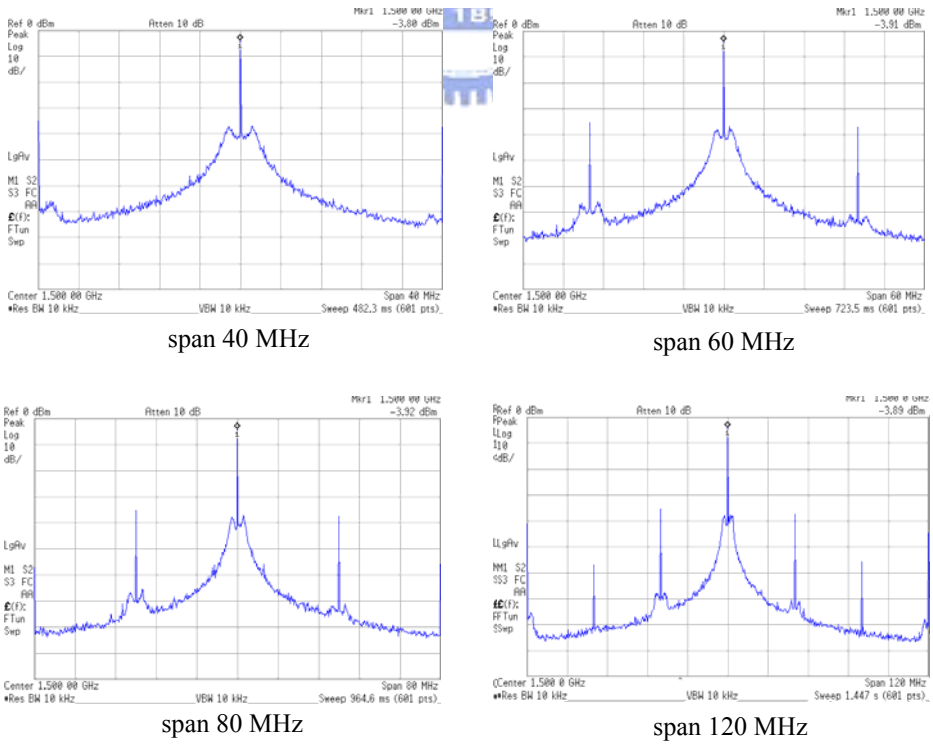


Figure 5.9: Measured jitter of SSCG output

igure 5.10 shows the measured spectrum of non-SSC VCO output at 1.5 GHz under the different scale span.



span 40 MHz

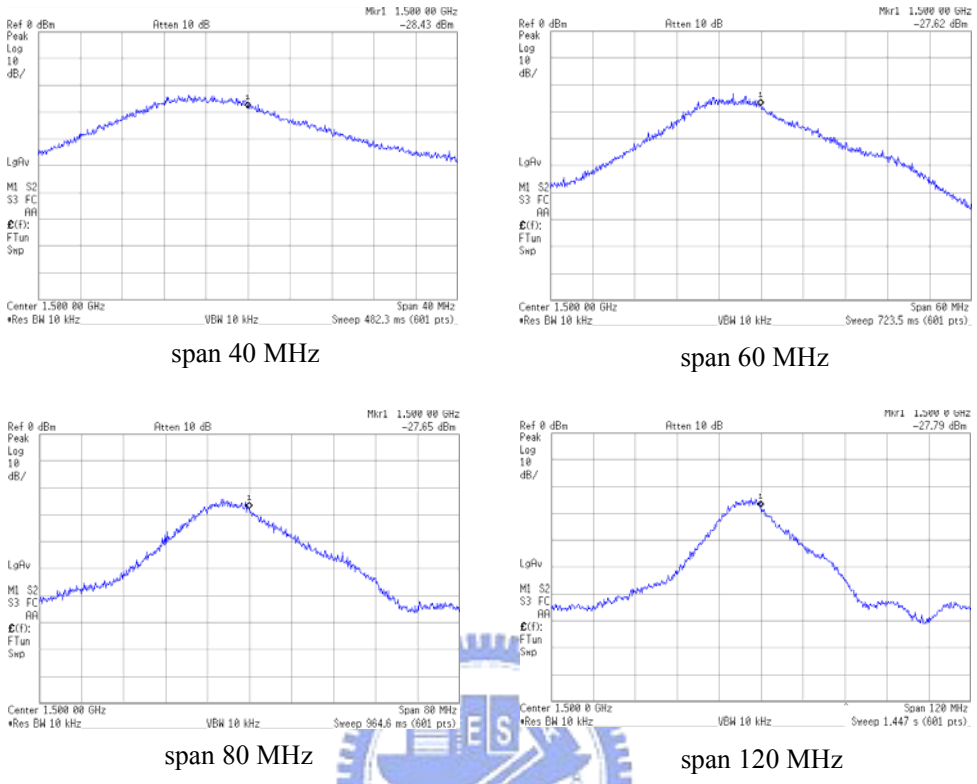
span 60 MHz

span 80 MHz

span 120 MHz

Figure 5.10: Spectrum of non-SSC output at 1.5 GHz

Figure 5.10 shows the measured spectrum of SSC VCO output at 1.5 GHz under the different scale span. The peak energy is reduce



span 40 MHz　　span 60 MHz

span 80 MHz　　span 120 MHz

Figure 5.11: Spectrum of SSC output at 1.5 GHz

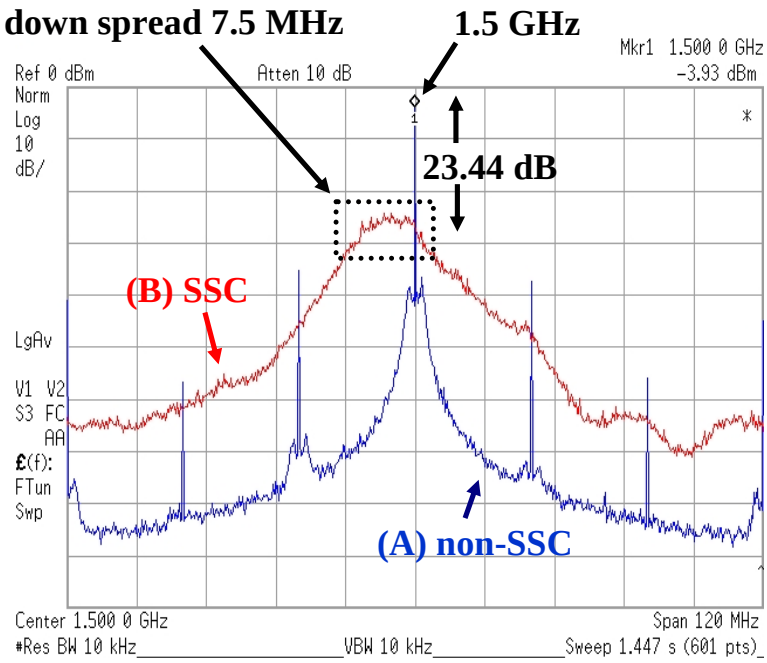


Figure 5.12: Spectrum of SSCG output at 1.5 GHz

Figure 5.12 shows the comparison of SSC and non-SSC VCO output at fundamental frequency. The line A is the spectrum of non-SSC VCO output; the center frequency is 1.5 GHz. The line B is the spectrum of SSC VCO output, every scale is 10 MHz, and we can see the frequency down spread 7.5 MHz. The peak amplitude reduction is 23.44 dB.

Figure 5.13 shows the peak attenuation of every harmonic term. The range is from 22 to 29 dB. Figure 5.14 shows the VCO voltage-frequency characteristics. The VCO tuning range is from 0.3 to 1.2 voltage and VCO gain is about 2.22 GHz/V. Table 1 gives the performance summary of the SSCG.

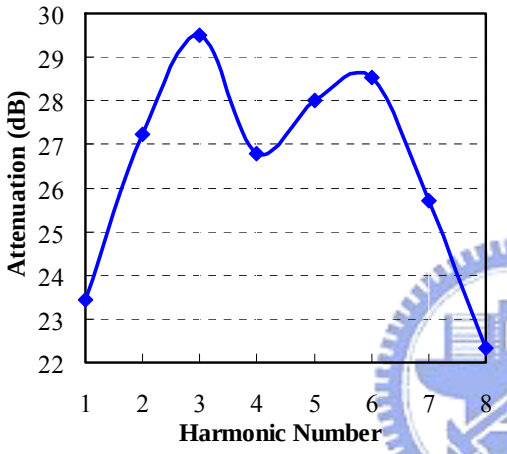


Figure 5.13: Attenuation of every harmonic

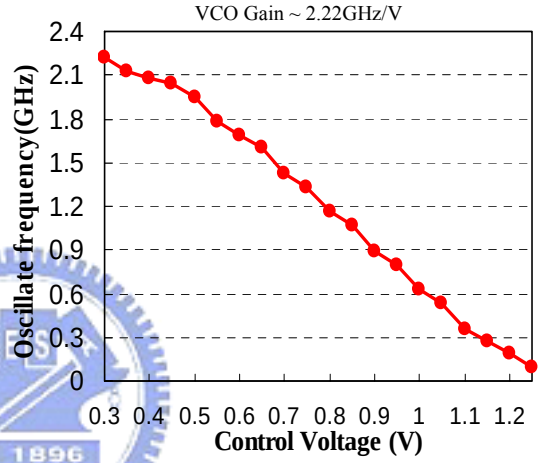


Figure 5.14: VCO V-F characteristic

Table 5.1: Performance summary of the SSCG

SSCG frequency	1.5 GHz
Technology	TSMC 0.18um CMOS
Modulation Method	Modulation on divider
Modulation Profile	33 KHz Triangular
Frequency Deviation	5000 ppm
Loop Bandwidth	120 KHz
Supply Voltage	1.8V
Power Dissipation	55 mW
Jitter (non-SSC)	80 ps
Peak Energy Reduction	23.44 dB
SSCG chip area	860um•860um

Chapter 6

Jitter Generator

6.1 Introduction

While the speed of the clock reaches GHz in recent years, it becomes more and more expensive to measure the clock jitter by using external high speed test equipment. The Built-In-Self-Test method becomes an alternative way to measure the clock jitter at a lower cost. In order to convert for the BIST usage; we can generate wanted jitter and measure it. If the measured result is close to generated jitter, the accuracy of measurement mechanism is higher. In this chapter, we propose a jitter generator using spread spectrum clock generator.

It will not generate jitter when the clock frequency fixes with time, on the other hand, jitter will occur when clock frequency varies with time. As shown in Figure 6.1, a triangular waveform is modulated into a carrier clock frequency. The modulation frequency deviation is Δf and period is $2t$, so the long term jitter (UI) can be defined as

$$\text{long term jitter (UI)} = \Delta f \cdot t \cdot \frac{1}{2}. \qquad (6\text{-}1)$$

According the equation, we can change the amplitude and period of modulation frequency to obtain wanted jitter.

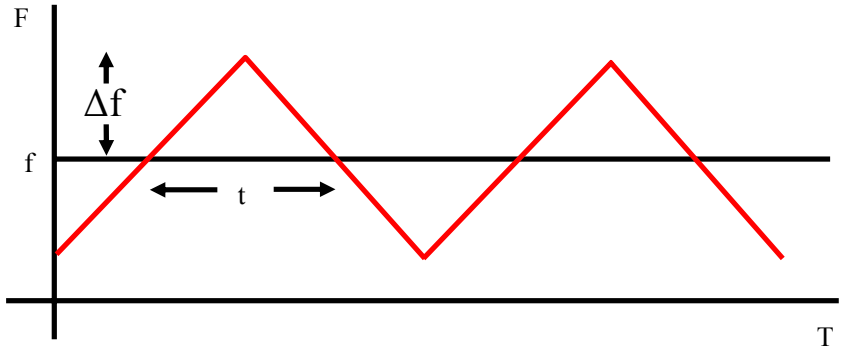


Figure 6.1: Jitter generated by frequency modulation

6.2 Jitter Generator Using SSCG

In previous chapters, we design a spread spectrum clock generator for SATA. SATA system requires clock frequency spread spectrum 30~33 KHz, 5000 ppm. We can design a programmable SSCG to change the deviation and period of the frequency modulation and generate wanted jitter.

Figure 6.2 shows the address generator. In order to achieve the goal easily, we only change the number of bottom control logic. Either deviation or period changed by controlling the number of bottom control logic, we can determine the wanted jitter.

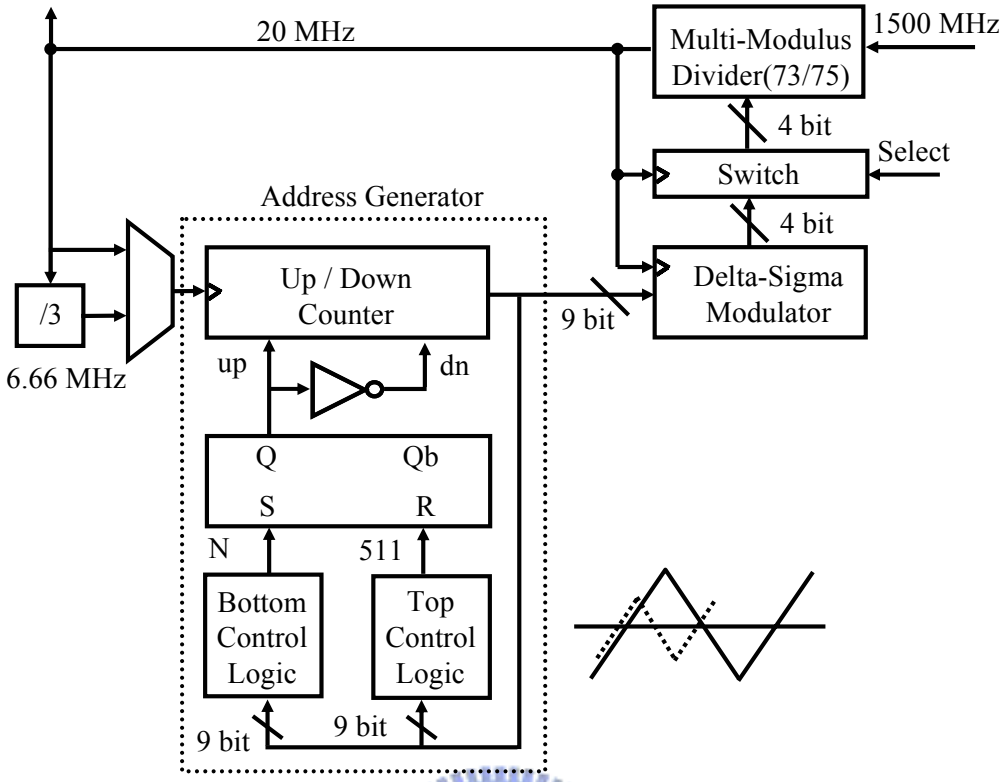


Figure 6.2: Address generator

As shown in Figure 6.3, this jitter generator design with the previous SSCG has the long term jitter as

$$\text{jitter (UI)} = \frac{1}{2}\cdot\left[40\cdot 10^{6}\cdot\frac{511-N}{511}\right]\cdot\frac{(511-N)\cdot 2}{20\cdot 10^{6}}\cdot\frac{1}{4} = \frac{1}{2}\frac{(511-N)^{2}}{511}, \quad \text{(6-2)}$$

where N is number of bottom control logic. Table 6.1 shows the control number N and its corresponding jitter.

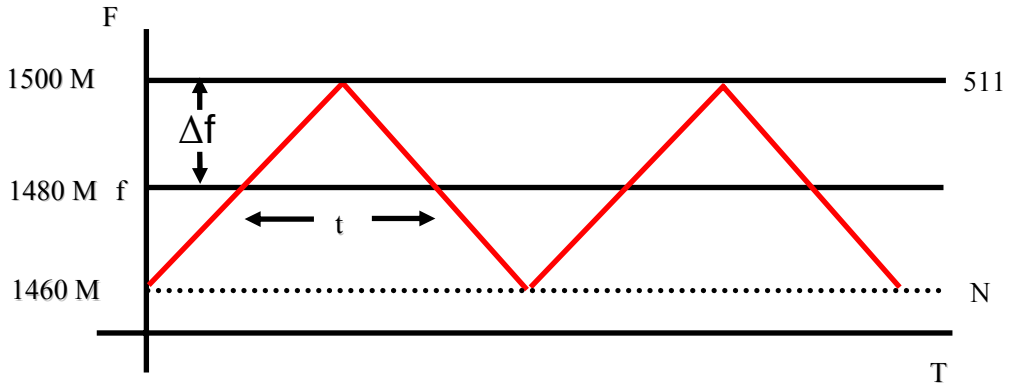


Figure 6.3: Jitter generator design

Table 6.1 Control number N and its corresponding jitter

N	jitter (UI)
487	0.563600783
488	0.517612524
489	0.473581213
490	0.431506849
491	0.391389432
492	0.353228963
493	0.31702544
494	0.282778865
495	0.250489237
496	0.220156556
497	0.191780822

It is difficult to verify the idea using the SPICE simulation because it takes very long time. As shown in Figure 6.4, we use SIMULINK to analyze the system and capture the VCO output to show the eye diagram.

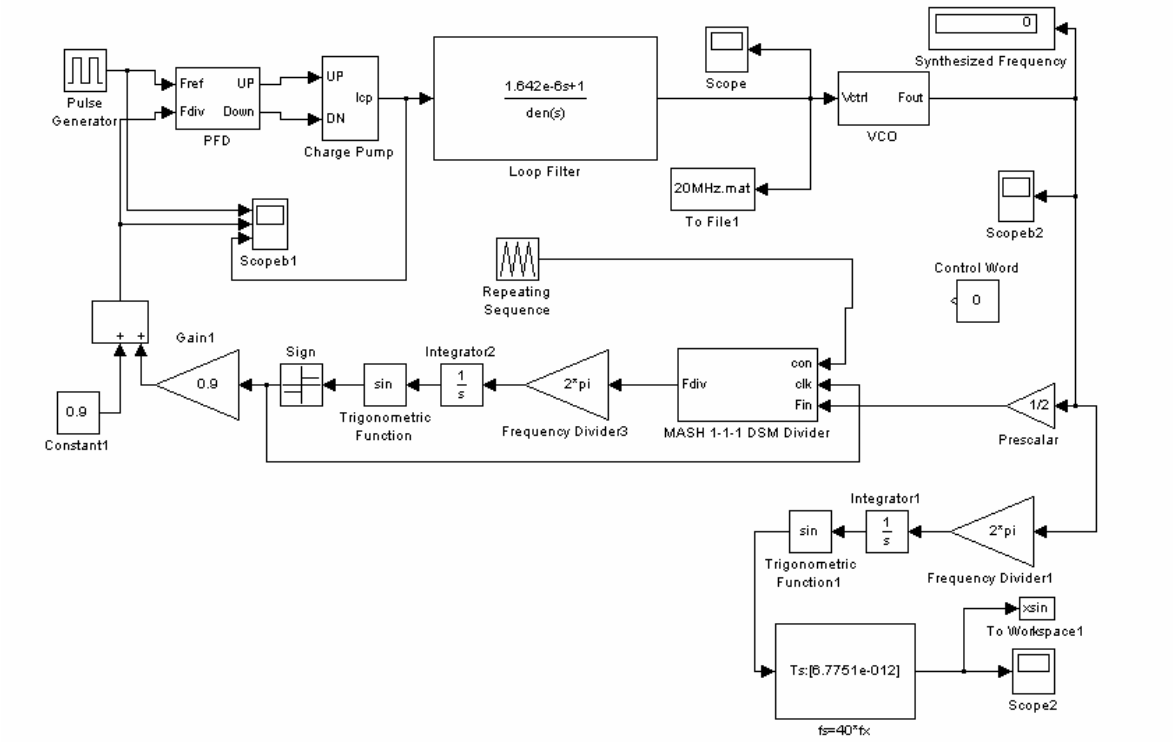
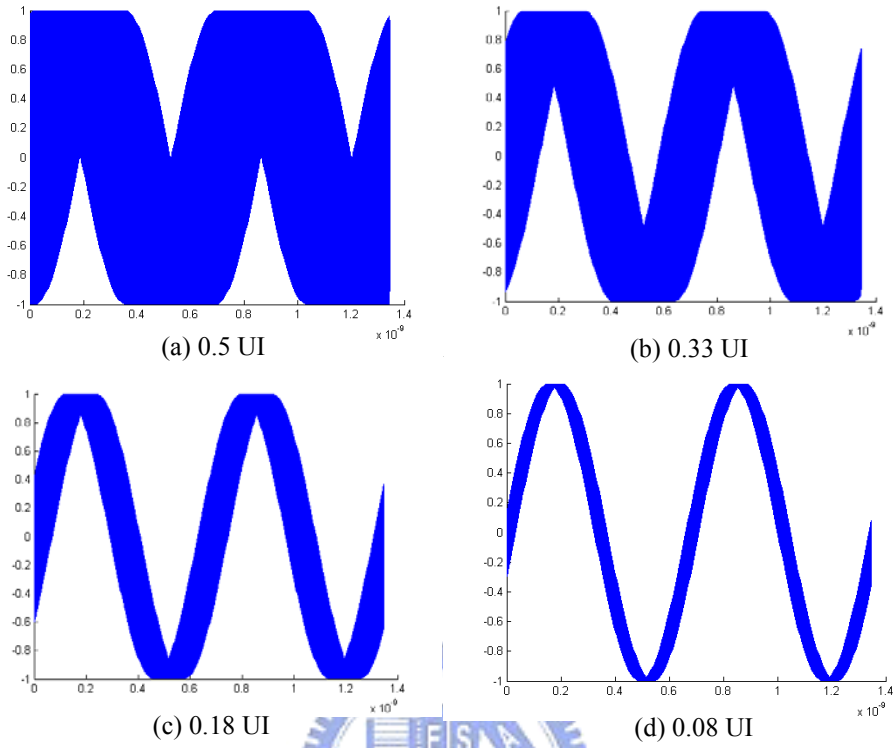


Figure 6.4: Behavior simulation of jitter generator using SIMULINK

Figure 6.5 shows the eye diagrams with different control number N and its corresponding jitter.



(a) 0.5 UI (b) 0.33 UI

(c) 0.18 UI (d) 0.08 UI

Figure 6.5: Eye diagrams with different control number N

Chapter 7

Conclusions

In this thesis, we have designed a spread spectrum clock generator for the SATA system. The SSCG uses a fractional-N frequency synthesizer to achieve spread spectrum function with triangular waveform modulation. The SSCG consists of a conventional PLL, an address generator, and a delta-sigma modulator. Fractional-N PLL can achieve high resolution with high operation frequency. But, one major disadvantage is the generation of high tones at multiples of the channel spacing. The use of digital delta-sigma modulation technique in the fractional-N PLL can eliminate spurs.

The SSCG circuit has been implemented in TSMC 0.18 um 1P6M CMOS technology. The measurement results show that the non spreading clock has a jitter of 80 ps and the peak amplitude reduction is 23.44 dB in the spread spectrum mode.

In order to convert for clock jitter BIST usage, we have proposes a jitter generator using spread spectrum clock generator in this thesis. The simulation results show that we can generate the wanted jitter by changing the deviation and period of the modulation frequency.

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