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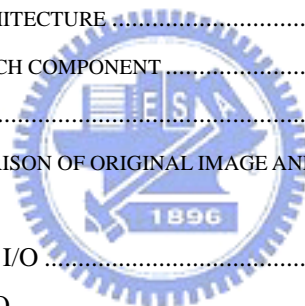
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# Award

1. 本論文曾參加第六屆 TIC100 冬令營競賽獲第二名



2. 本論文動態估測內容已提出國內專利申請:發明專利案號 93120023 “動態影像估測的裝置與方法”，透過交大智財中心於民國 93 年 8 月 13 日送出
3. 本論文曾入圍 2005 SIP 競賽決賽