Chapter 4 Implementation Result

4.1 Verification Procedure

The hardware verification mainly includes three parts:

1. Functional simulation:

This MPEG-4 encoder IP is implemented by using synthesizable HDL code and stimulated by test bench to run cycle accurate simulation. The functional simulation and verify procedure is shown in Fig. 4-1. The “xvid” is used as MPEG-4 encoder C model, and then replace the motion estimation, texture coding and variable length coding modules as ours. This C model is our reference model, and it will dump out the test pattern and the encoded bit stream. The dumped test pattern will be input into the MPEG-4 synthesizable RTL code. The simulator also will dump out the simulation bit stream as text file, and this bit stream text file are compared with software encoded bit stream by edit software such as Ultra Edit to achieve automatic comparison.

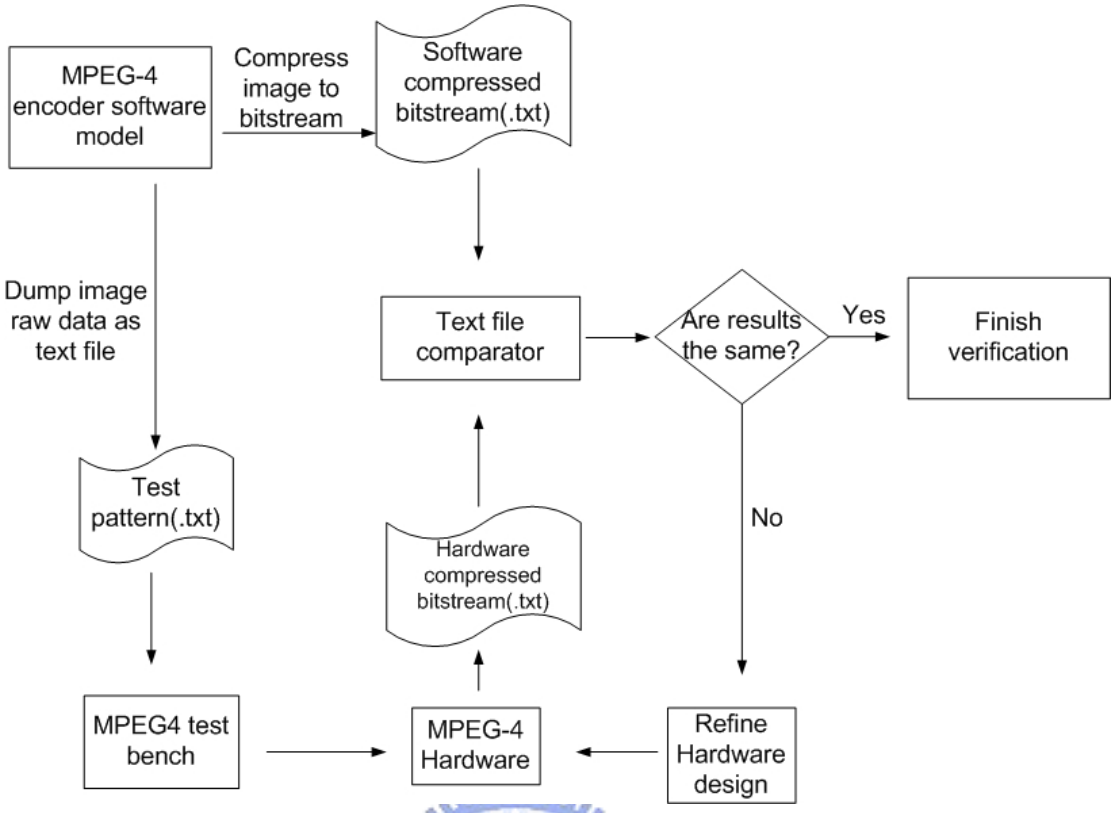

Figure 4-1 Functional simulation and verification procedure

2. FPGA prototyping:

HDL simulation is very time-consuming. In order to verify large amount of test pattern rapidly, FPGA is used. We use the ARM Integrator as our prototyping platform which introduced in the chapter 1 and the chapter 3. After the MPEG-4 encoder finish encoding, the ARM would write out the bit stream as text file and compared with the software model result. And the bit stream could be decoded on the PC by the xvid decoder and the PSNR performance can be evaluated instantly. Fig. 4-2 shows that we debug in the ARM Developer Suite (ADS), and Fig. 4-3 shows the decoded frame by xvid decoder.

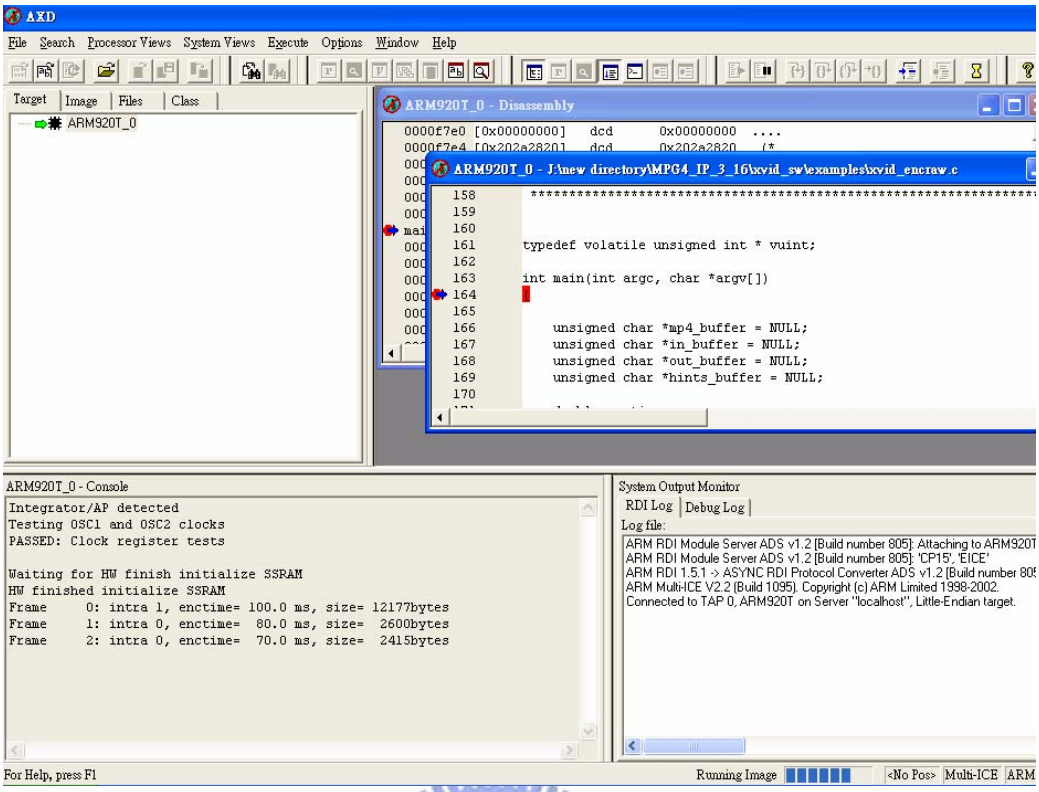

Figure 4-2 The hardware driver running on the ARM ADS

Figure 4-3 MPEG-4 bit stream is decoded by xvid decoder

3. Gate-level simulation:

This MPEG-4 encoder is synthesized using the UMC 0.18um process library. The gate level netlist is simulated using the same testbench which used in the functional simulation. And the comparison procedure is the same as functional simulation. The gate-level simulation result is the same as the functional simulation.

4.2 Design for Testability (DFT)

Considering the ASIC testing, the scan chain and build-in self-test (BIST) design are inserted. The test architecture is shown in Fig. 4-4. In order to reduce the length of scan chain, each module has its own scan chain. Which module will be tested can be selected via setting the Test_Sel input port, the Test_si1 is the scan in signal of module testing and the Test_si2 is the scan in signal of the MPEG4_IP top level. And the test pattern of each module is generated by the ATPG tool.

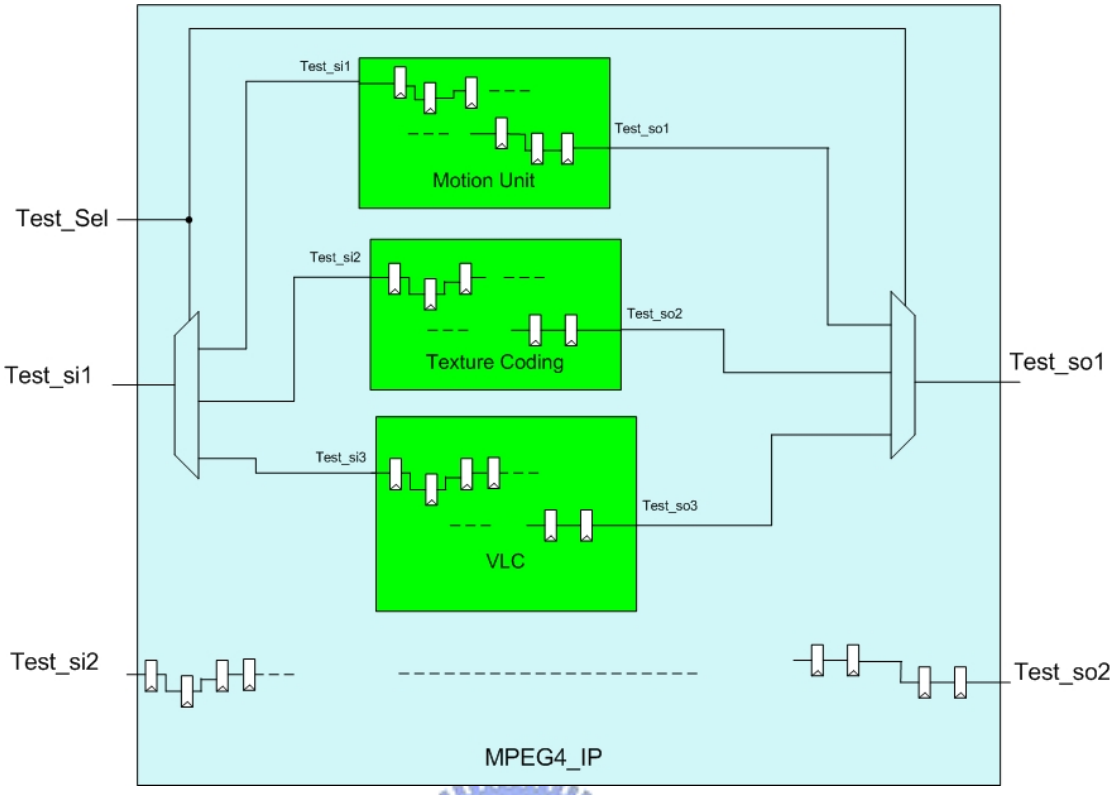

Figure 4-4 DFT architecture

The BIST method is used for on-chip memory testing, and the BIST architecture is shown in Fig. 4-5. There are four BIST groups in the MPEG4_IP. In order to reduce the I/O pin number, the user could select which ram module would be tested and only one ram module test result will be output to the output pin.

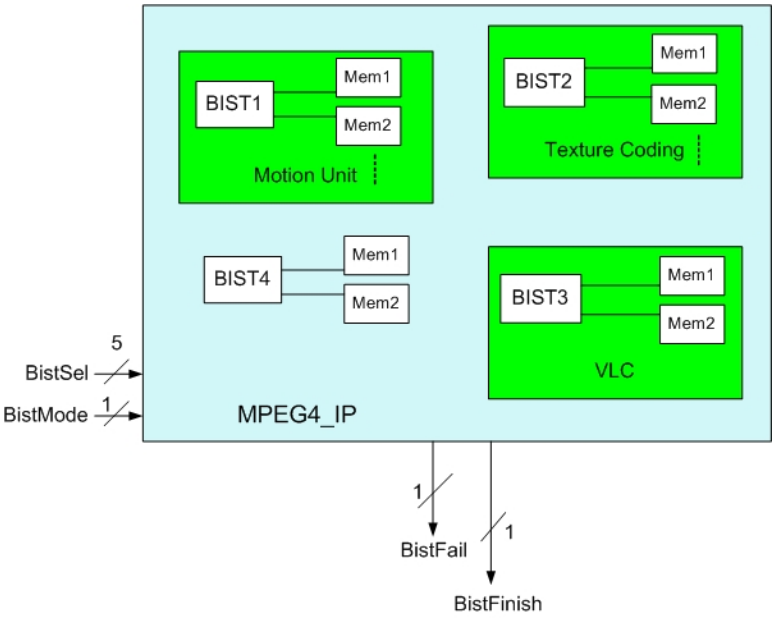

Figure 4-5 Build-in self-test architecture

4.3 Achievement

4.3.1 PSNR comparison

We compare our MPEG-4 C model with the xvid official version software encoder. The PSNR result is shown in Table 4-1. The PSNR dropping of the hardware design mainly is caused by two reasons. One reason is that the data precision in the hardware design is less precise than the xvid official version software. The other reason is that the search algorithm in the hardware is not as flexible as the xvid official version software.

Table 4-1 Encoder PSNR comparison at bitrate = 384 kbps

Video sequence	xvid official version software encoder	Our hardware design
Akiyo	42.38	41.45
Foreman	30.81	29.92
Table tennis	31.51	29.66
Mobile	21.31	20.93
Flower garden	22.25	21.88

4.3.2 Hardware implementation result

This MPEG-4 encoder IP has been synthesized using the UMC 0.18um process and the Artisan standard cell library. The total gate count of the MPEG-4 encoder IP is 204K gates, and the area percentage of each component is shown in Fig. 4-6. The motion unit includes the downsampling, the motion estimation and the motion compensation. The texture coding includes the DCT/IDCT, the quantization, the inverse quantization and the AC/DC prediction. The VLC includes the zig-zag scan and the variable length coding.

The synchronous SRAM usage is listed in Table 4-2. This MPEG-4 encoder IP totally uses 51696 bits (6462 bytes) on-chip memory and 445600 bytes off-chip memory.

The chip layout and specification are listed in Fig. 4-7 and Table 4-3. Fig. 4-8 shows the image quality comparison of original image source and the compressed image.

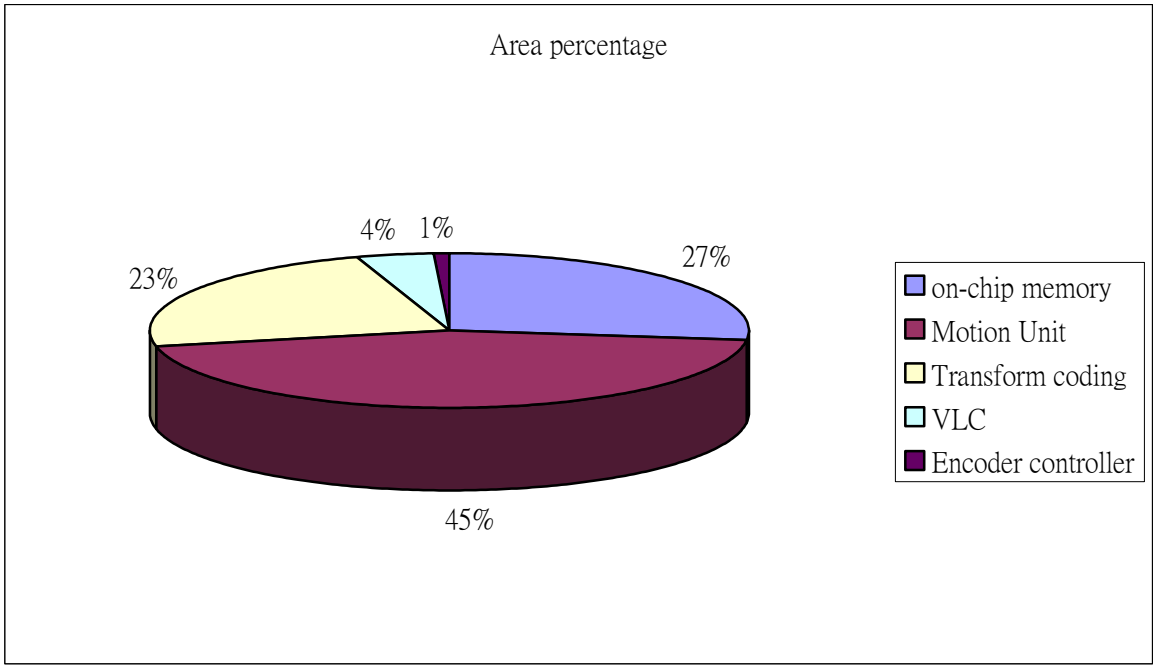

Figure 4-6 Area percentage of each component

Table 4-2 Memory usage in MPEG4 encoder IP

On-chip memory	Function	Characteristic	Depth x Width	Number	Bits	Area
	Current MB for ME	Single port SRAM	32 x 32	2	2048	79549.218 x 2 (um^2)
	Search area for ME	Single port SRAM	24 x 32	5	3840	53748.453 x 5 (um^2)
	Current MB buffer for MC	Single port SRAM	96 x 32	1	3072	153744.457 (um^2)
	Previous MB buffer for MC	Single port SRAM	96 x 32	2	6144	153744.457 x 2 (um^2)
	L1 buffer for downsampling	Single port SRAM	88 x 18	1	1584	49355.589 (um^2)
		Single port SRAM	48 x 32	2	3072	83069.718 x 2 (um^2)
	L2 buffer for downsampling	Single port SRAM	48 x 18	1	864	52338.288 (um^2)
		Single port SRAM	24 x 32	1	768	53748.453 (um^2)
	AC/DC Prediction memory	Single port SRAM	232 x 12	1	2784	62605.613 (um^2)
		Single port SRAM	256 x 12	2	6144	79945.837 x 2 (um^2)

	DCT/IDCT transpose memory	Dual port SRAM	64 x 16	1	1024	170675.692 (um^2)
	DCT/IDCT input buffer	Single port SRAM	96 x 36	2	6912	171413.142 x 2 (um^2)
	VLC input buffer	Single port SRAM	432 x 12	2	10368	83031.222 x 2 (um^2)
	Encoder output buffer	Dual port SRAM	48 x 32	2	3072	177044.735 x 2 (um^2)
Total on-chip memory bits/area					51696 bits	2.466807 (mm^2)

External memory	Function	Characteristic	Bytes
	Image buffer	Single port SRAM	444016 bytes
	Memory for ME data	Single port SRAM	1584 bytes
Total external memory size(Not include bitstream memory area)			445600 bytes

1

[1] The on-chip memory is generated by Artisan memory compiler using UMC 0.18um process

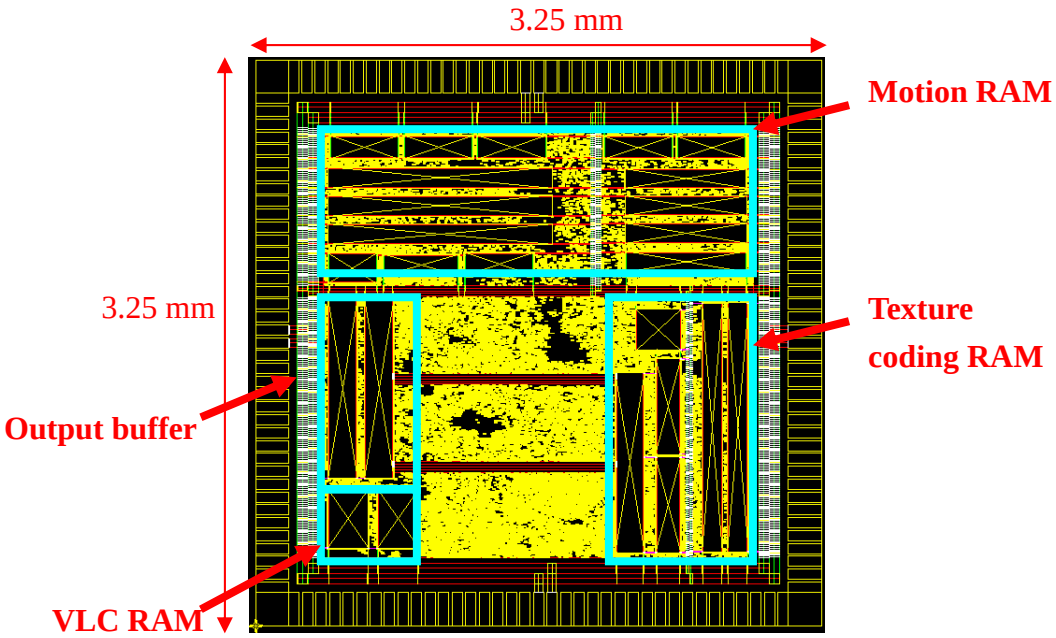

Figure 4-7 Chip layout

Table 4-3 Specification of MPEG-4 encoder IP

Profile	Simple Profile Level 3
Supported image format	YUV 4:2:0
Supported VOP type	I frame & P frame
Supported image size	CIF (352 x 288)
Encoding frame rate	30 CIF/sec
Maximum operation frequency	43 MHz
Gate count	204K gates
Interface	AMBA AHB
On-chip memory	6462 bytes
Off-chip memory	445600 bytes

Original image　　Compressed image

Original image　　Compressed image

Figure 4-8 Image property comparison of original image and compressed image

4.3.3 Comparison with other MPEG-4 encoder chip

Table 4-4 shows the comparison of our design with other MPEG-4 encoder chips. From the compression speed point of view, our design only needs 21 mega clock cycles to achieve 30 CIF image compression. In order to consider the compression speed and the chip area at the same time, a comparison metric called normalized processing capability per gate (NPCPG) is used [14].

$$NPCPG_{xxx} = \frac{\left[(required\ clock\ cycle\ for\ CIF\ 30\ fps)\times(gate\ count)\right]_{our\ design}}{\left[(required\ clock\ cycle\ for\ CIF\ 30\ fps)\times(gate\ count)\right]_{xxx}}.$$

From the NPCPG comparison, we can see that our design is a low cost and high performance MPEG-4 video encoder.

Table 4-4 MPEG-4 encoder chip comparison

Designer	Function	Visual profile	Encoding complexity	Needed cycles per 30 CIF images
AMPHION CS6701 [12]	Video encoder	SP@L3	30 CIF frames/second	36 Mega clock cycles
FUJITSU [13]	Video codec	SP@L3	15 CIF frames/second	54 Mega clock cycles
Our design	Video encoder	SP@L3	30 CIF frames/second	21 Mega clock cycles

Designer	Logic gate count	Process	Chip area	NPCPG
AMPHION CS6701 [12]	170K	0.18 um	N/A	0.7
FUJITSU [13]	700K	0.18 um	5.296mm x 5.296mm	0.1125
Our design	204K	0.18 um	3.25mm x 3.25mm	1