Chapter 5 Conclusion

5.1 Contribution of this thesis

1. This thesis proposes an novel hierarchical motion estimation hardware architecture, HMEA. This architecture could improve the data reuse capability and reduce the internal memory to 1393 bytes. The HMEA is also efficient enough to achieve real-time encoding. It only takes 495 cycles to find one best motion vector, and it demonstrates its PSNR performance is close to conventional full search block matching algorithm. The HMEA architecture is also a regular and simple search scheme, so it is suitable for LSI implementation.
2. In the bit stream unit, the bit stream encoding complexity is analyzed and the hardware/software encoding work partition is applied. A variable length coding hardware architecture is proposed to achieve MPEG-4 simple profile level 3 bit stream encoding and the encoding throughput could arrive at one symbol per cycle.
3. A three-stage pipeline scheduling of the MPEG-4 encoder system is implemented. The motion estimation, texture coding, and variable length coding work parallel with each other, and the MPEG-4 encoder only needs 21 mega clock cycles to accomplish 30 CIF images encoding. It implies that this encoder could achieve real-time encoding.
4. An AMBA system has been built on the ARM Integrator for verifying the MPEG-4 encoder with ARM processor. This AMBA system includes a direct memory access controller (DMAC) design which could ease the software computational loading.

5.2 Improvement in the future

1. The ARM Integrator is a good platform for hardware design verification, because it contains ARM CPU and is ready to be used AMBA bus which connected to FPGA development board. Unfortunately, there is a FIFO whose depth is sixteen between the Core Module [3] and AP [2], so that the DMAC could only read one word from the SDRAM per sixteen clock cycles. If we want to develop a real-time FPGA application, we need a platform which allows our hardware design directly access to SDRAM or image capture device.
2. The hierarchical search algorithm is suitable for processing large size image, the search range and processing image size have better to be extendable and configurable.
3. Currently, the GOP size is constant and set by the software. If the frame mode decision could be decided adaptively by the image distortion criteria such as the SAD, our MPEG-4 encoder will encode the scene changed or high motion cases better.