Design of 24-GHz 0.8-V 1.51-mW Coupling Current-Mode Injection-Locked Frequency Divider With Wide Locking Range

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***Abstract*—A 0.8-V CMOS coupling current-mode injection-locked frequency divider (CCMILFD) with 19.5% locking range and a current-injection current-mode logic (CICML) frequency divider have been designed and fabricated using 0.13-μm 1p8m CMOS technology. In the proposed CCMILFD, the current-mode technique to minimize the loss of input signals and the coupling circuit to enlarge the phase response have been designed to increase the locking range. The locking range of the fabricated CCMILFD is 4.1 GHz with a power consumption of 1.51 mW from a power supply of 0.8 V. In the proposed CICML frequency divider, the current-injection interface is applied to the current inputs to make the circuit operated at a higher frequency with low power consumption under a low voltage supply. The operation frequency of the fabricated CICML frequency divider can divide the frequency range from CCMILFD and consume 1.89 mW from a 0.8-V voltage supply. The chip core areas of the CCMILFD and CICML frequency divider without pads are 0.23 and 0.015 mm^2, respectively. The proposed circuits can be operated in a low supply voltage with the advantages of a wider locking range, a higher operation frequency, and lower power consumption.**

***Index Terms*—Coupling current-mode injection-locked frequency divider (CCMILFD), current-injection current-mode logic (CICML) frequency divider, current-mode injection-locked frequency divider (CMILFD), current-mode logic (CML), injection-locked frequency divider (ILFD).**

I. Introduction

In RF frequency synthesizers, the high-speed frequency divider plays a critical role in various broadband and wireless applications. Recently, voltage-mode injection-locked frequency dividers (ILFDs) and direct injection-locked frequency dividers (DILFDs) have been proposed in some of the research [1]–[4]. They have the advantages of low power consumption and high-frequency capability. However, both conventional ILFDs and DILFDs have the same problem of a narrow locking range. In order to solve this problem, enlarging the size of input transistors to generate a larger transconductance g_m or decreasing the quality factor of the resonant network in [1]–[7] are the most common solutions. With a larger g_m, the injected voltage signal can be converted to a higher ac current to reach a larger locking range. However, an increase in the size of the tail transistor also increases the undesired parasitic capacitance, which becomes a leakage path for a high-frequency injection signal. It seriously degrades the ratio η of the injection current $(I_{\rm inj})$ to a dc current $(I_{\rm DC})$. This issue has been raised in previous research [5] and the technique of shunt-peaking locking range enhancement has been proposed. Though there is some improvement in the locking range, the cost of chip area due to the extra inductors in the circuit is high.

Another method to extend the locking range is decreasing the effective quality factor of the resonant network. With the lower quality factor, the bandwidth is broadened and the signals with different frequencies are allowed to be evident at outputs. The CML-type ILFD with resistive loads proposed in [6] can have a lower quality factor and higher locking range when compared to a high-Q narrowband *LC*-tank ILFD. However, it needs more power for the circuit to guarantee the oscillation and maintain the output amplitude.

Recently, new techniques of utilizing coupling circuits between dividers [7] and common-node injection [8] have been proposed to extend the locking range with low power consumption. However, the circuits presented in [7] are not suitable for low-voltage applications due to the cascode structure. In addition, because the incident signals are voltage mode and injected from the tail transistors of the circuit, η cannot be improved to further improve the locking range.

In the lower frequency band, the CML-type frequency divider is a good option because of its optimization of power, speed, and area consumption. However, the conventional CML divider is not suitable in a low-voltage operation when working at a high frequency. It suppresses the voltage headroom of the current source and makes evaluation pairs more difficult to change its logic states. As shown in [9], the operating frequency is proportional to the supply voltage. When the voltage supply is down below 1 V, the divider cannot accommodate a signal with a frequency over 10 GHz.

In order to solve the problems above, this paper proposes a current-mode divided-by-4 circuit, which is composed of two divider stages. The first stage is the coupling current-mode injection-locked frequency divider (CCMILFD) for higher frequency signals, and the second stage is the current-injection current-mode logic (CICML) frequency divider for lower frequency signals. The CCMILFD is composed of two current-

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mode injection-locked frequency dividers (CMILFDs) and one coupling circuit. A new method of injecting the current signal directly into the divider instead of the voltage signal is adopted in the proposed CMILFD. This reduces the required voltage headroom and solves the problem of poor efficiency associated with voltage-to-current translation in the input stage. The coupling circuit is used to generate an extra phase to compensate for the loop phase shift. As a departure from previous work [7], the incident signals are injected into both the CMILFD stage and the coupling circuit stages. As a result, the locking range can be enhanced with low power consumption.

In the second divider, in order to solve the problems of the conventional CML divider, a CICML structure is introduced. The switching mechanism is determined by the current and not the voltage signal. The voltage headroom requirement and the switching response time for the devices can be reduced. It can make the entire circuit feasible to be operated in a high-frequency band and under a low supply voltage condition.

The proposed frequency current-mode divider has been designed and fabricated using 0.13-μm CMOS technology. The fabricated chip has been measured to verify precisely its performance. The measurement results show that the CCMILFD has a locking range of 19.5% with a power consumption of 1.51 mW. The fabricated CICML divider can cover the full range of the first stage at a 0.8-V supply with a power consumption of 1.89-mW.

In Section II, the design concept and model of the proposed CCMILFD are presented. In Section III, the circuit design is described. The experimental results are presented in Section IV. Finally, a conclusion is given in Section V.

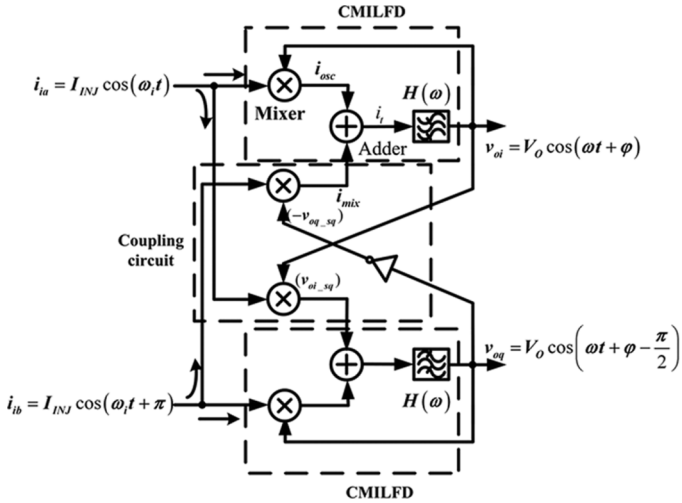

Fig. 1. Proposed model for CCMILFD.

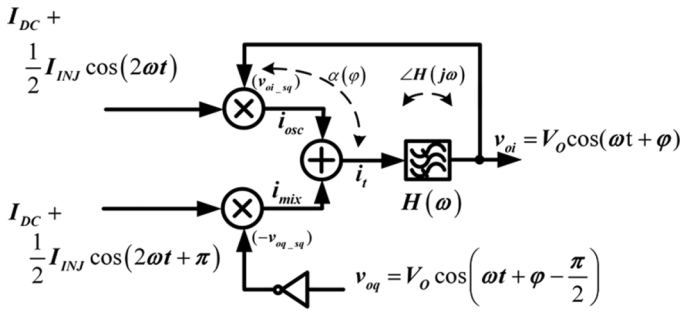

Fig. 2. Half model of CCMILFD.

II. Theoretical Model Analysis

A. Locking Range of CCMILFD

Based on the concept of an *LC* ILFD [1], [10], [11], a new model for a CCMILFD is proposed, which is composed of two CMILFDs and one coupling circuit. The injection current signal is injected not only into the CMILFD itself, but also into the coupling circuit. The coupling circuit behaves as a mixer and is used to provide an extra phase to compensate for the phase shift caused by the input signal. The block diagram for the proposed CCMILFD model is shown in Fig. 1, where the phase differences between v_{oi} and i_{ia} and between v_{oq} and i_{ib} are φ, the signals i_{ia} and i_{ib} are differential input signals, v_{oi} and v_{oq} are quadrature output voltages, $i_{\rm osc}$ is generated through the mixer by mixing i_{ia} and v_{oi}, $i_{\rm mix}$ is the output current of the coupling circuit by mixing i_{ib} and v_{oq}, and i_t is the tank current in the *LC* tank.

When the double frequency current signals are injected into the divider, the input current is given by both the dc current $I_{\rm DC}$ of the mixer and the double frequency current. Since the injection current flows into both the CMILFD and coupling circuit, each of them can be assumed to receive half of the injection current. As shown in Fig. 2, both $i_{\rm osc}$ and $i_{\rm mix}$ are generated through the mixers by modulating the injection current signals and dc currents with quadrature output voltages. After the *LC* tank, only the fundamental component of the output signal can be filtered out at the output nodes. Moreover, since the output amplitude of CCMILFD is large and able to switch on and off the transistors abruptly, the v_{oi} and v_{oq} can be viewed as square waves for the mixer to simplify the analysis. The fundamental component of currents $i_{\rm osc}$ and $i_{\rm mix}$ can be derived as

$$\begin{aligned} i_{\rm osc} &= \left[I_{\rm DC} + \frac{1}{2}i_{ia}\right] v_{oi\_\rm sq} \\ &\simeq \frac{4}{\pi}I_{\rm DC}\cos(\omega t + \varphi) + \frac{1}{\pi}I_{\rm INJ}\cos(\omega t - \varphi) \\ &\quad - \frac{1}{3\pi}I_{\rm INJ}\cos(\omega t + 3\varphi) + \text{high-order harmonics} \end{aligned} \tag{1}$$

$$\begin{aligned} i_{\rm mix} &= \left[I_{\rm DC} + \frac{1}{2}i_{ib}\right](-v_{oq\_\rm sq}) \\ &\simeq -\frac{4}{\pi}I_{\rm DC}\cos\left(\omega t + \varphi - \frac{\pi}{2}\right) \\ &\quad - \frac{1}{\pi}I_{\rm INJ}\cos\left(\omega t - \varphi + \frac{3\pi}{2}\right) \\ &\quad + \frac{1}{3\pi}I_{\rm INJ}\cos\left(\omega t + 3\varphi - \frac{\pi}{2}\right) + \text{high-order harmonics} \end{aligned} \tag{2}$$

where the input frequency ω_i is twice the output frequency ω, $I_{\rm INJ}$ is the amplitude of i_{ia} and i_{ib}, and $v_{oi\_\rm sq}$ and $v_{oq\_\rm sq}$ are the Fourier series of the square waves produced by v_{oi} and v_{oq}. The derivations are given in Appendix A.

In the proposed CCMILFD, $i_{\rm mix}$ is further added to $i_{\rm osc}$ in order to generate an extra phase shift for the tank current

i_t. To derive an analytical expression of the locking range for CCMILFD, i_t can be derived as

$$i_t = i_{\rm osc} + i_{\rm mix} = I_T \cos\left(\omega t + \gamma(\varphi)\right) \tag{3}$$

where

$$I_T = \frac{4\sqrt{2}}{\pi}\left|\frac{1}{\eta} + \frac{1}{6}\cos 2\varphi - j\left(\frac{1}{3}\sin 2\varphi\right)\right| I_{\rm INJ} \tag{4}$$

$$\gamma(\varphi) = \varphi + \frac{\pi}{4} - \arctan\left(\frac{\frac{1}{3}\eta\sin 2\varphi}{1+\frac{1}{6}\eta\cos 2\varphi}\right). \tag{5}$$

In (4) and (5), η is the injection current ratio and equal to $I_{\rm INJ}/I_{\rm DC}$. The derivations are given in Appendix B.

From (5), the phase response $\alpha(\varphi)$ between v_{oi} and i_t can be calculated as

$$\alpha(\varphi) = \gamma(\varphi) - \varphi = \frac{\pi}{4} - \arctan\left(\frac{\frac{1}{3}\eta\sin 2\varphi}{1+\frac{1}{6}\eta\cos 2\varphi}\right). \tag{6}$$

With the assumption of sufficient close loop gain, the locking range is only determined by the close loop phase condition of the Barkhausen criteria. As derived in Appendix B, the single-sided locking range $|\Delta\omega|$ can be expressed as

$$\Delta\omega \equiv |\omega - \omega_o| = \left(\frac{\omega_o}{2Q}\right)\cdot\left(\frac{1+\frac{1}{6}\eta\cos 2\varphi - \frac{1}{3}\eta\sin 2\varphi}{1+\frac{1}{6}\eta\cos 2\varphi + \frac{1}{3}\eta\sin 2\varphi}\right). \tag{7}$$

As may be seen from (7), the locking range depends on the injection current ratio η, tank quality factor Q, and the phase difference φ between injection currents $i_{ia,b}$ and output voltage $v_{oi,q}$, respectively. In particular, the locking range can be increased by increasing η and reducing Q at the expense of power consumption for a given output amplitude.

From (7), it also shows that the optimal phase response for the locking range occurs when the phase φ is equal to $3\pi/4$. Under this condition, the locking range is a function of η and Q and the final result is given by

$$\Delta\omega \le \left(\frac{\omega_o}{2Q}\right)\cdot\left(\frac{1+\frac{1}{3}\eta}{1-\frac{1}{3}\eta}\right). \tag{8}$$

In the conventional ILFD, the phase response $\alpha(\varphi)$ and locking range $|\Delta\omega|$ are [1]

$$\alpha(\varphi) = -\arctan\left(\frac{\frac{2}{3}\eta\sin 2\varphi}{1+\frac{1}{3}\eta\cos 2\varphi}\right) = \arctan\left(2Q\frac{\omega-\omega_o}{\omega_o}\right) \tag{9}$$

$$\Delta\omega \le \left(\frac{2\omega_o}{3Q}\eta\right). \tag{10}$$

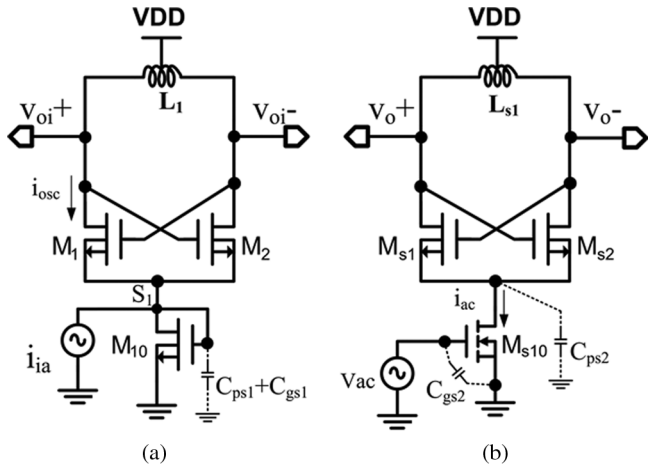

Fig. 3. Circuit diagrams of: (a) CMILFD and (b) conventional ILFD.

When comparing (6) with (9), it can be seen that because of $i_{\rm mix}$, the CCMILFD creates an extra phase shift of $\pi/4$. In a conventional ILFD, the phase response is determined by η. When η is very small, the phase response becomes very small and the locking range is limited by the Barkhausen criteria in phase. However, in the proposed CCMILFD, it can provide an extra phase shift to prevent the circuit from the failure of the phase criteria, especially when η is small. Furthermore, when comparing (8) with (10), the locking range of the proposed circuit is much larger than that of a conventional ILFD.

In addition to the extra phase shift resulting from the proposed circuit, the output amplitude can also be improved to increase the loop gain. The tank current amplitude I_T is enhanced by a factor of $\sqrt{2}$, as shown in (4). Due to an increase in the amplitude of i_t, both the output level of $v_{oi,q}$ can be higher and the loop gain of the entire loop can be increased. This can guarantee that the initial assumption of sufficient loop gain is sustained and the possibility of losing lock in the loop due to insufficient loop gain can be reduced.

III. Circuit Realization and Simulation Results

The divide-by-4 circuit consists of a divide-by-2 CCMILFD and a divide-by-2 CICML frequency divider. The circuit realization and simulation results of the CMILFD, CCMILFD, and CICML divider are discussed in Sections III-A–D.

A. CMILFD

The circuit diagrams of the CMILFD and the conventional ILFD are shown in Fig. 3(a) and (b), respectively. In Fig. 3(a), the cross-coupled pair (M_1, M_2) in the CMILFD can be viewed as a mixer to generate the output current $i_{\rm osc}$ by mixing v_{oi} and i_{ia}. To reduce the power loss on the input parasitic capacitance, a new incident interface for i_{ia} is proposed. As shown in Fig. 3(a), i_{ia} is directly injected into the common source connection S_1 instead of through the gate of input transistor M_{s10} in Fig. 3(b). In Fig. 3(b), $i_{\rm ac}$ is generated by converting the voltage signal $v_{\rm ac}$ through the transconductance g_m of M_{s10}. In order to have a larger $i_{\rm ac}$, a higher g_m is required. A higher g_m is realized by increasing the dc current and transistor size of M_{s10}. However,

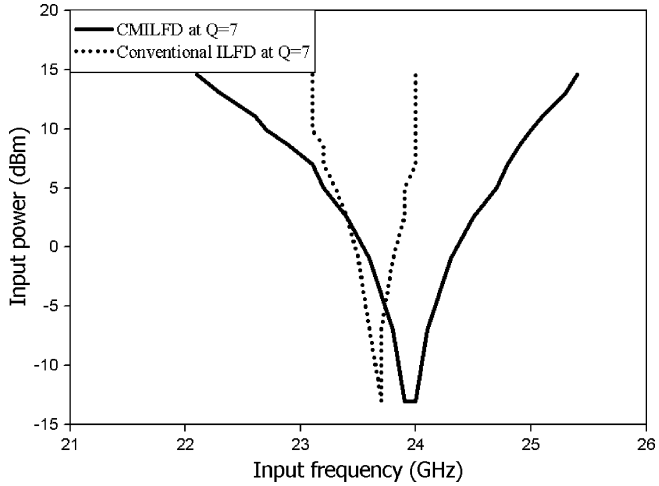

Fig. 4. Simulated comparison of the locking ranges between CMILFD and ILFD at $Q = 7$.

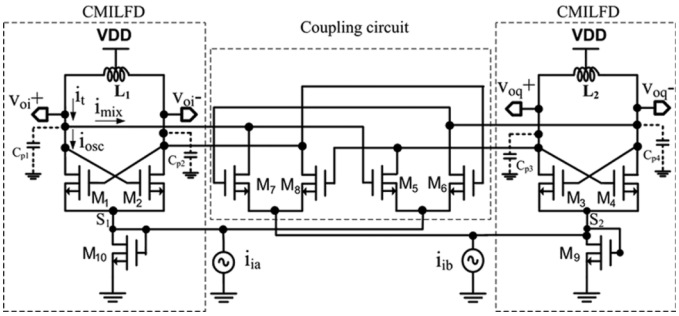

Fig. 5. Circuit diagram of CCMILFD.

it results in higher power consumption and larger signal loss through its parasitic capacitors $C_{\rm gs2}$ and $C_{\rm ps2}$.

In the CMILFD, since the injection current is injected directly to S_1, it is not related to the transconductance of M_{10}. Therefore, the diode-connected transistor M_{10} that behaves as a resistive load is used to provide the dc current and this allows for a reduction in the transistor size. When the size of M_{10} becomes smaller, the parasitic capacitance $C_{\rm ps1}$ and $C_{\rm gs1}$ of node S_1 can be decreased to reduce the current signal loss. Since the signal loss is minimized, most input current can be injected into to the circuit and the injection current ratio η can be improved. As a result, the locking range of the CMILFD can be increased.

In Fig. 4, the sensitivity curves of the CMILFD and the conventional ILFD are simulated by using Spectre RF with the same *LC* tank and power supply voltage. From Fig. 4, it can be seen that, at the same level of input power, the locking range of the CMILFD is much larger than that of the conventional ILFD. Therefore, the locking range can be improved using the proposed approach involving a current–mode interface.

B. CCMILFD

The circuit diagram of the CCMILFD is shown in Fig. 5, which has two CMILFDs and one coupling circuit. The coupling circuit is composed of (M_5, M_6) and (M_7, M_8), as shown in Fig. 5. The resonant frequency of the circuit is determined by the two center-tapped inductors L_1 and L_2 and the parasitic capacitances C_{p1}, C_{p2}, C_{p3}, and C_{p4} at the output modes.

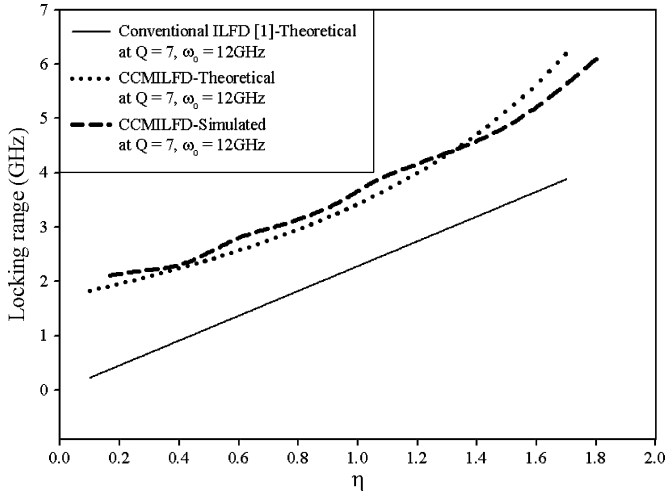

Fig. 6. Simulated locking range versus η.

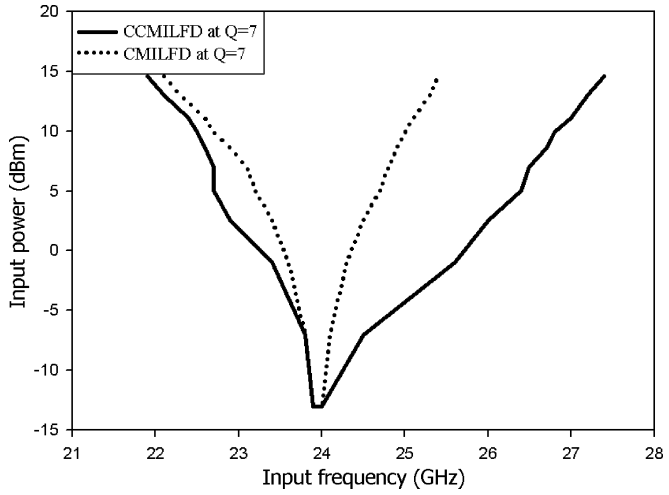

Fig. 7. Simulated comparison of the locking range between CCMILFD and CMILFD.

(M_5, M_6) and (M_7, M_8) behave as two hard-limiting mixers to mix the quadrature output voltages and input current signals. The output current $i_{\rm mix}$ of the coupling circuit is combined with $i_{\rm osc}$ from the CMILFD to generate the tank current i_t. The injection currents i_{ia} and i_{ib} are differential and each of them is fed into the CMILFD and the coupling circuit.

The simulation results of the locking range versus η is simulated by using Spectre RF and is shown in Fig. 6. From Fig. 6, under the conditions of quality factor $Q = 7$ and $\omega_o = 12\times10^9$, the simulated locking range of the CCMILFD is around 4.6 GHz at $\eta = 1.4$. The theoretical single-sided locking range is calculated using (8) and then the double-sided locking range is multiplied by a factor of 2. The simulation result correlates well with the theoretical locking range of the CCMILFD and is much larger than that of the conventional ILFD. As also seen from Fig. 6, the higher η has a larger locking range. Fig. 7 shows the simulation results of input power plotted against input frequency in order to compare the sensitivities between the CCMILFD and the single CMILFD without the coupling circuit. It can be seen in Fig. 7 that with the same input power, the locking range of

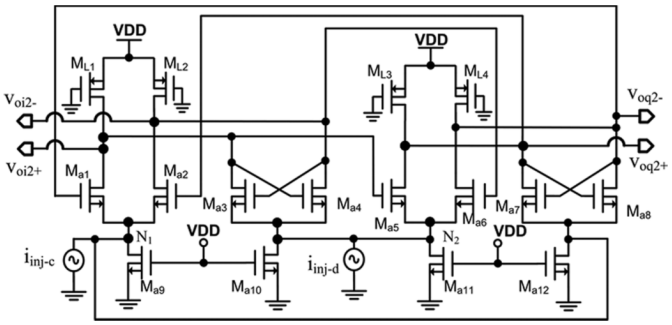

Fig. 8. Circuit diagram of CICML divider.

the CCMILFD is much larger than that of the single CMILFD due to the existence of the coupling circuit.

Through the *LC* tank in the circuit, the signal of fundamental frequency can be taken from the output node, and its relative harmonics are suppressed by the *LC* filter. The simulated second and third harmonics can be suppressed to approximately 24 and 40 dB below the fundamental signal, respectively.

C. CICML Divider

The circuit diagram of the proposed CICML frequency divider is depicted in Fig. 8. M_{L1}, M_{L2}, M_{L3}, and M_{L4} are the PMOS loads for the divider. (M_{a1}, M_{a2}) and (M_{a5}, M_{a6}) form the evaluation pairs, which can switch the logic state. (M_{a3}, M_{a4}) and (M_{a7}, M_{a8}) are the latch pairs to latch the logic. M_{a9}, M_{a10}, M_{a11}, and M_{a12} are the current sources.

When the conventional CML frequency divider [9] is operated in a low voltage supply, the voltage swing in the internal nodes of the circuit is suppressed and makes the circuit difficult to change the logic states of the evaluation pair and latch pair. The low gate voltage swing also makes the current source transistors difficult to be switched on and off. Therefore, the operation frequency is limited due to the low voltage supply.

The concept of a current-mode injection interface is applied to this circuit to solve the above problem. The input current signals $i_{\text{inj-}c}$ and $i_{\text{inj-}d}$ are injected into the nodes N_1 and N_2, respectively. The current signals instead of voltage signals are provided to switch on and off the evaluation pairs and latch pairs. When the current flows to the evaluation pair, it starts to determine the logic value. The result is transmitted to the latch pair and it is latched when the current flows to the latch pair. Since the logic is decided by the current switching mechanism, the limitation on speed due to the response time of the current source transistors in the conventional CML divider [9] is reduced and the operating frequency can be much higher than that for a conventional CML frequency divider when in low-voltage operation. A comparison of high-frequency capability between a conventional CML and the proposed CICML divider in simulation with a low voltage supply is shown in Fig. 9. The frequency of the CICML can be up to 14 GHz at a low supply voltage of 0.8 V, whereas that of CML divider is approximately 10 GHz. In this study, the self-oscillation frequency of the CICML is designed at around 5.5 GHz. The sensitivity curve covers the desired frequency band, as shown in Fig. 10. From Fig. 10, the locking range at the input power of 10 dBm is around 7 GHz.

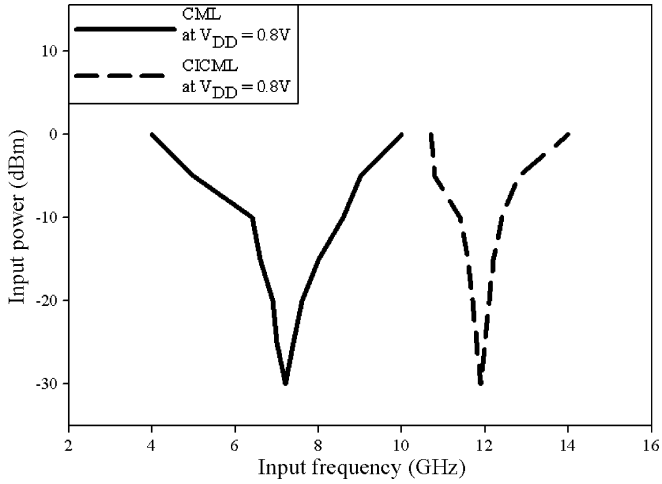

Fig. 9. Simulated comparison between classical CML and CICML dividers at $V_{DD} = 0.8$ V.

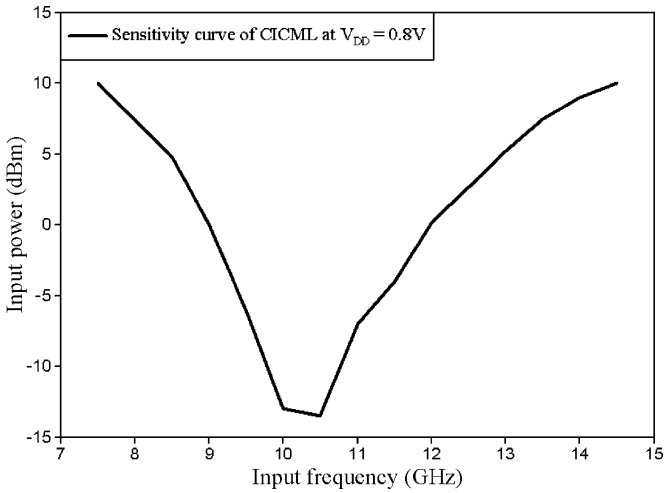

Fig. 10. Simulated sensitivity curve of CICML divider.

D. Divide-by-4 Circuit

The overall circuit diagram of the divide-by-4 divider is depicted in Fig. 11. It consists of a CCMILFD divider, a CICML divider, and four open-drain output buffers for measurement.

Four current buffers for the inter stages are used to propagate the current signals in Fig. 11. The circuit diagram and its small-signal model of the current buffer are shown in Fig. 12(a) and (b), respectively. In Fig. 12(a), C_b is a large blocking capacitor and can be viewed as a short circuit at high frequency. The gain of the current buffer can be derived from the small-signal model in Fig. 12(b) and simplified as

$$\frac{i_o}{i_i} = \frac{1}{1 + s\dfrac{C_{\text{gd1}} + C_{\text{db1}}}{g_{m2} + s(C_{\text{gs2}} + C_{\text{db2}})}} \tag{11}$$

where C_{gd1} and C_{db1} are the gate–drain and drain–bulk capacitance of M_{c1}, C_{gs2} and C_{db2} are the gate–source and drain–bulk capacitance of M_{c2}, and g_{m2} is the transconductance of M_{c2}. The first pole of the circuit is at

$$|P_1| = \frac{g_{m2}}{C_{\text{gd1}} + C_{\text{db1}} + C_{\text{gs2}} + C_{\text{db2}}}. \tag{12}$$

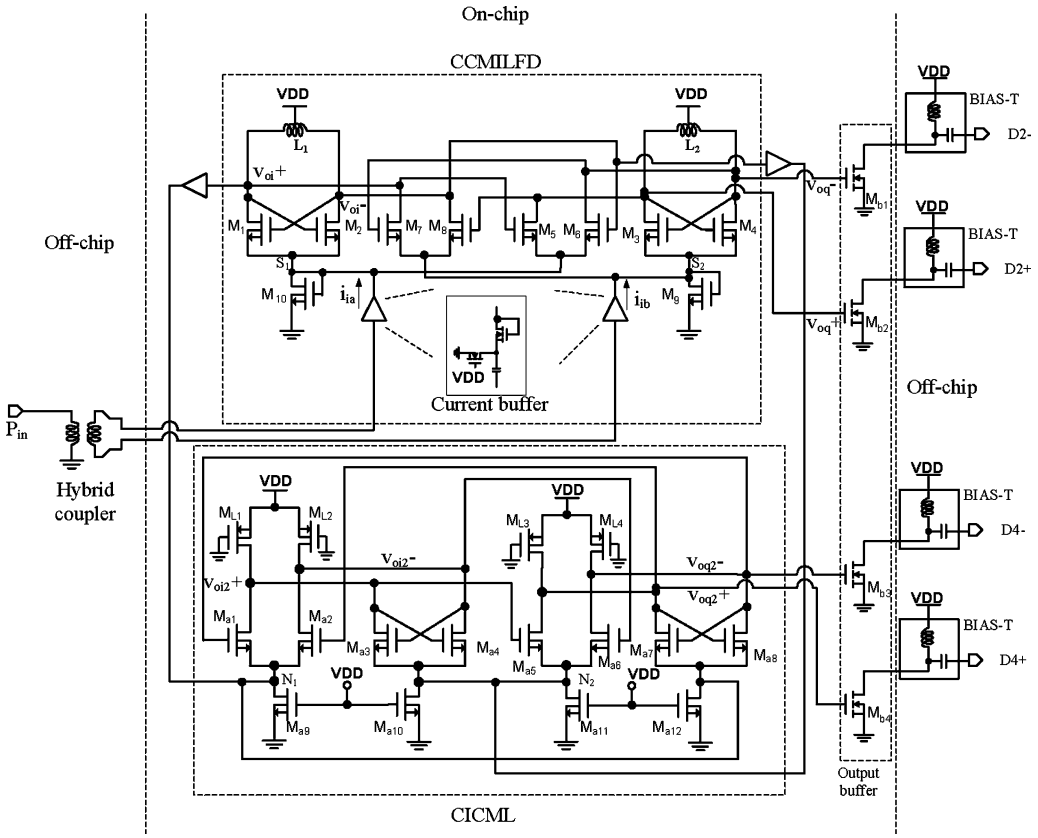

Fig. 11. Circuit diagram of divide-by-4 divider.

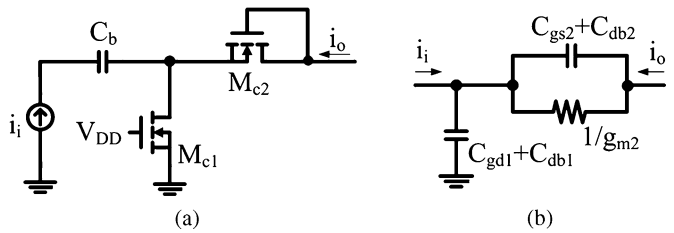

Fig. 12. Current buffer. (a) Circuit diagram. (b) Small-signal model.

From the above equations, it can be seen that when both $C_{\rm gd1}$ and $C_{\rm db1}$ are very small, the gain of the current buffer is close to 1 and the location of the first pole approaches to the unity gain frequency f_T of M_{C2}. Therefore, it is a wideband-unity-gain current buffer and is very suitable to propagate the current signals in the current-mode applications.

For measurement purposes, an external signal source and a hybrid coupler were used to generate accurate differential input signals to measure the detailed locking range of the CCMILFD. In Fig. 11, the output signals $D2+$ and $D2-$ are the outputs of $v_{oq}+$ and $v_{oq}-$ after passing through open-drain buffers with off-chip bias-tee components, respectively. $D4+$ and $D4-$ are the outputs of $v_{oq2}+$ and $v_{oq2}-$, respectively, in the divided-by-4 after the buffers.

IV. Experimental Results

The designed 24-GHz current-mode divide-by-4 circuit was fabricated using 0.13-μm 1p8m CMOS technology. The chip micrograph of the designed dividers is shown in Fig. 13. The chip includes a CCMILFD, CICML frequency divider, output buffers, and testing pads. On-wafer probing measurement was adopted to verify the performance of the dividers. There are three ground–signal–ground–signal–ground (GSGSG) RF probes with a pitch of 100 μm and one six-pin dc probe with a pitch of 150 μm used to probe the chip. A hybrid coupler and an external signal source are applied to the generation of accurate differential input signals for the CCMILFD when measuring

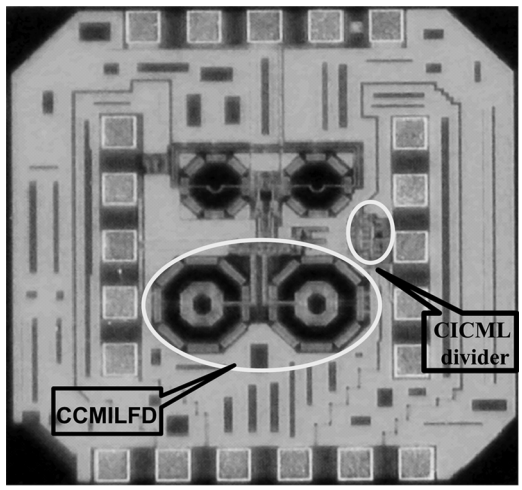

Fig. 13. Micrograph of chip.

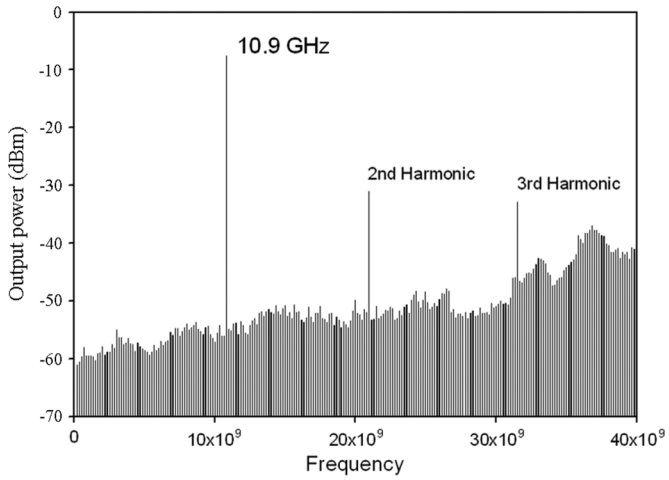

Fig. 14. Measured spectrum of CCMILFD.

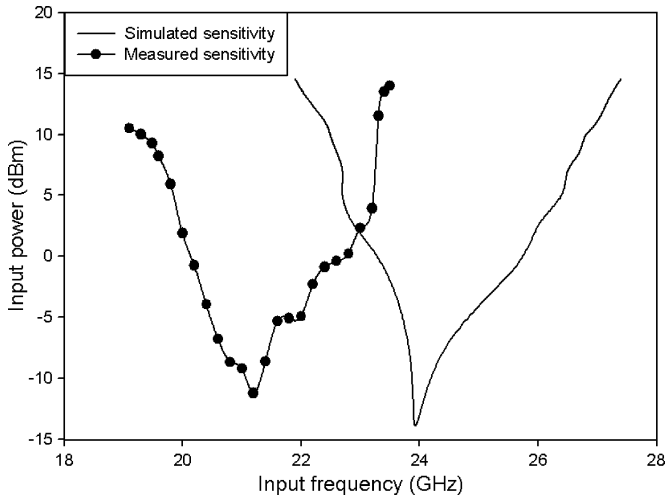

Fig. 15. Measured and simulated sensitivity curve of CCMILFD at $Vdd = 0.8$ V.

its locking range. The losses from cables, probes, and adaptors were calibrated and compensated in the measurement results.

Owing to the layout parasitic and process variation of the fabricated chip, the measured frequency of circuits is slightly shifted down, as shown in Figs. 14 and 15. In Fig. 14, the measured spectrum of the output signals of the fabricated CCMILFD is shown. The output frequency is exactly divided by two from an input frequency of 21.8 GHz. In Fig. 15, the measured sensitivity curve of the CCMILFD is presented. The locking range at an input power of 10 dBm is from 19.3 to 23.4 GHz. The phase noise of CCMILFD is -123 dBc/Hz at 1-MHz frequency offset and the measurement result is depicted in Fig. 16. The core chip area of the CCMILFD is 0.36×0.64 mm^2. The power consumption of the CCMILFD is 1.51 mW with a 0.8-V power supply.

For the measurement of the second stage of the divider, because there are no external sources designed to measure the CICML frequency divider, the precise sensitivity curve cannot be presented in this paper. However, the CICML can divide the signals from the CCMILFD completely to achieve our goal of dividing the input frequency by 4. The measured spectrum is

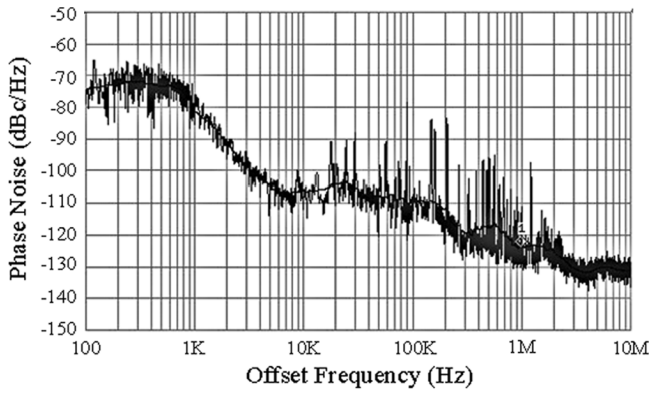

Fig. 16. Measured phase noise of CCMILFD.

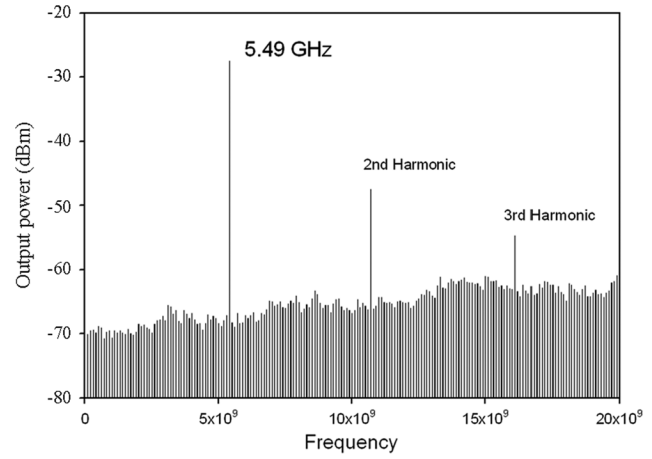

Fig. 17. Measured spectrum of CICML divider.

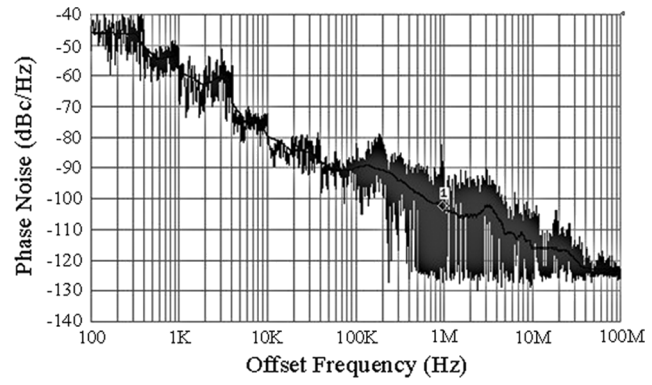

Fig. 18. Measured phase noise of CICML divider.

shown in Fig. 17. The input frequency is 10.98 GHz from the CCMILFD and its output is located at 5.49 GHz. The power consumption is 1.89 mW with a 0.8-V power supply voltage. The phase noise of the CICML divider is -104 dBc/Hz at 1-MHz frequency offset and the measurement result is shown in Fig. 18.

The measurement results are summarized in Table I for both the CCMILFD and CICML frequency divider. The performance comparisons among different CMOS ILFDs are given in Table II. As compared to other CMOS ILFDs, the proposed CCMILFD and CICML divider have the advantages of a lower

TABLE I
SUMMARY OF MEASUREMENT RESULTS FOR CCMILFD AND CICML

	CCMILFD	CICML
Technology	0.13-um CMOS	0.13-um CMOS
Topology	Current-mode LC divider	Current-Injection CML
VDD (V)	0.8	0.8
Self-oscillation (GHz)	11.13	5.5
Division	2	2
Power (mW) (w/o buffer)	1.51	1.89
Locking range (GHz)	19.3~23.4 *2 22.4~27 (post-sim)	*1 9.65~11.7 *2 7.5~14.5 (post-sim)
Phase noise @1-MHz	-123	-104.33
Core chip area (mm^2)	0.36 × 0.64	0.1×0.15

*1 It was measured to cover all frequency ranges from the first stage divider. No external sources were designed to measure its exact performance.
*2 The post-layout simulation results are simulated at the input power of 10 dBm.

voltage operation, significantly lower power consumption, and a wide locking range of 19.5% of the center frequency.

V. CONCLUSION

In this study, both a CCMILFD and CICML frequency divider are proposed and applied to the design of a CMOS divide-by-4 divider. In the proposed CCMILFD, a new coupling circuit to improve the phase response and a current-mode technique to minimize the loss of input signals are proposed to increase the locking range and to minimize power consumption. The theoretical model analysis of the CCMILFD has been developed. In the proposed CICML frequency divider, a current-injection interface has also been proposed to increase the operation frequency under a low voltage supply. The divide-by-4 divider has been fabricated by using 0.13-μm 1p8m CMOS technology. The measured locking range of the fabricated CCMILFD is about 19.5% of the center frequency and the entire output range of CCMILFD is covered by the CICML frequency divider. The power consumptions of the CCMILFD and CICML frequency divider are 1.51 and 1.89 mW with core chip areas of 0.23 and 0.015 mm^2, respectively. The measurement results have verified that the proposed circuits can be operated on a low supply voltage of 0.8 V and provide the advantages of a wider locking range, a higher operation frequency, and a lower power consumption. Thus, the current-mode technique has great potential in applications of low-voltage RF systems in nanometer CMOS technologies.

APPENDIX A

In the design of CCMILFD, the quadrature outputs of CCMILFD are large signals. When the output amplitude is large compared with the switching voltage of the mixer, the mixer can be switched abruptly. In such case, v_{oi} and v_{oq} can be assumed as square waves for the mixer to simplify the analysis of locking range. The Fourier series of the square waves can be expressed by the fundamental term and harmonics as [1]

$$v_{oi\_sq} = \frac{4}{\pi}\left[\cos(\omega t+\varphi) - \frac{1}{3}\cos(3\omega t+3\varphi) + \frac{1}{5}\cos(5\omega t+5\varphi) - \cdots\right] \tag{A.1}$$

$$v_{oq\_sq} = \frac{4}{\pi}\left[\cos\left(\omega t+\varphi-\frac{\pi}{2}\right) - \frac{1}{3}\cos\left(3\omega t+3\varphi-\frac{3\pi}{2}\right) + \frac{1}{5}\cos\left(5\omega t+5\varphi-\frac{5\pi}{2}\right) - \cdots\right] \tag{A.2}$$

where φ is the phase difference between $i_{ia,b}$ and $v_{oi,q}$, respectively. The injection currents i_{ia} and i_{ib} are differential and can be expressed as

$$i_{ia} = I_{\rm INJ}\cos(\omega_i t) \tag{A.3}$$

$$i_{ib} = I_{\rm INJ}\cos(\omega_i t+\pi) \tag{A.4}$$

where ω_i is the input frequency and $I_{\rm INJ}$ is the amplitude of i_{ia} and i_{ib}.

$i_{\rm osc}$ and $i_{\rm mix}$ are generated by mixing the injection current signals in (A.3) and (A.4) and dc currents with the quadrature output voltages in (A.1) and (A.2). The results are given by

$$\begin{aligned} i_{\rm osc} &= \left[I_{\rm DC}+\frac{1}{2}i_{ia}\right]v_{oi\_sq} \\ &\simeq \frac{4}{\pi}I_{\rm DC}\cos(\omega t+\varphi)+\frac{1}{\pi}I_{\rm INJ}\cos(\omega t-\varphi) \\ &\quad -\frac{1}{3\pi}I_{\rm INJ}\cos(\omega t+3\varphi)+\text{high-order harmonics} \end{aligned} \tag{A.5}$$

$$\begin{aligned} i_{\rm mix} &= \left[I_{\rm DC}+\frac{1}{2}i_{ib}\right](-v_{oq\_sq}) \\ &\simeq -\frac{4}{\pi}I_{\rm DC}\cos\left(\omega t+\varphi-\frac{\pi}{2}\right) \\ &\quad -\frac{1}{\pi}I_{\rm INJ}\cos\left(\omega t-\varphi+\frac{3\pi}{2}\right) \\ &\quad +\frac{1}{3\pi}I_{\rm INJ}\cos\left(\omega t+3\varphi-\frac{\pi}{2}\right)+\text{high-order harmonics} \end{aligned} \tag{A.6}$$

where $I_{\rm DC}$ is the dc current of CMILFD and the coupling circuit, input frequency ω_i is equal to two times of output frequency ω.

APPENDIX B

The tank current i_t is generated by adding the two currents $i_{\rm osc}$ and $i_{\rm mix}$. From (A.5) and (A.6), we have

$$\begin{aligned} i_t &= i_{\rm osc}+i_{\rm mix} \\ &= \frac{4}{\pi}I_{\rm DC}\left[\cos(\omega t+\varphi)-\cos\left(\omega t+\varphi-\frac{\pi}{2}\right)\right] \\ &\quad +\frac{1}{\pi}I_{\rm INJ}\left[\cos(\omega t-\varphi)-\cos\left(\omega t-\varphi+\frac{3\pi}{2}\right)\right] \\ &\quad -\frac{1}{3\pi}I_{\rm INJ}\left[\cos(\omega t+3\varphi)-\cos\left(\omega t+3\varphi-\frac{\pi}{2}\right)\right] \\ &\quad +\text{high-order harmonics.} \end{aligned} \tag{B.1}$$

The high-order harmonics in (B.1) can be rejected by the *LC* tank in the circuit. Therefore, only fundamental terms are considered.

TABLE II
PERFORMANCE COMPARISONS AMONG DIFFERENT CMOS ILFDS

Ref.	Technology	Topology	Division number	VDD (V)	Input Freq (GHz)	Power (mW)	Locking range (GHz)	(%)	Chip size (mm2)
[5]	0.35μm CMOS	Voltage-mode LC divider	2	1.2	19	0.5	1.36	7	0.3
[6]	0.13μm CMOS	Voltage-mode CML divider	2	1.8	37	12	3.5	9	_
[7]	90nm CMOS	Voltage-mode Miller divider	2	1.2	20	6.4	5	25	0.0264
[7]	90nm CMOS	Voltage-mode LC divider	2	1.2	20	6.4	~3.6	18	0.0264
[8]	0.18μm CMOS	Voltage-mode LC divider	2	1.4	58	2.8	4.9	8	0.37
CCMILFD CICML	0.13μm CMOS	Current-mode LC divider	4	0.8	21	1.51 1.89	4.1	19.5	0.23 0.015

To obtain the phase of it, the fundamental terms of (B.1) can be rewritten in complex notation as

$$\begin{aligned}
i_t &= \frac{4\sqrt{2}}{\pi} I_{\mathrm{DC}} \cos\left(\omega t + \varphi + \frac{\pi}{4}\right) \\
&\quad - \frac{\sqrt{2}}{\pi} I_{\mathrm{INJ}} \cos\left(\omega t - \varphi + \frac{5\pi}{4}\right) \\
&\quad - \frac{\sqrt{2}}{3\pi} I_{\mathrm{INJ}} \cos\left(\omega t + 3\varphi + \frac{\pi}{4}\right) \\
&= \mathrm{Re}\left\{ \frac{4\sqrt{2}}{\pi} I_{\mathrm{DC}} \cdot e^{j\omega t} \cdot e^{j\varphi} \cdot e^{j\frac{\pi}{4}} \right. \\
&\qquad - \frac{\sqrt{2}}{\pi} I_{\mathrm{INJ}} \cdot e^{j\omega t} \cdot e^{-j\varphi} \cdot e^{j\frac{5\pi}{4}} \\
&\qquad \left. - \frac{\sqrt{2}}{3\pi} I_{\mathrm{INJ}} \cdot e^{j\omega t} \cdot e^{j3\varphi} \cdot e^{j\frac{\pi}{4}} \right\} \\
&= \mathrm{Re}\left\{ \frac{4\sqrt{2}}{\pi} I_{\mathrm{INJ}} \cdot e^{j\omega t} \cdot e^{j\varphi} \right. \\
&\qquad \left. \cdot e^{j\frac{\pi}{4}} \left[\frac{I_{\mathrm{DC}}}{I_{\mathrm{INJ}}} + \frac{1}{4} \cdot e^{-j2\varphi} - \frac{1}{12} e^{j2\varphi} \right] \right\} \\
&= \mathrm{Re}\left\{ \frac{4\sqrt{2}}{\pi} I_{\mathrm{INJ}} \cdot e^{j\omega t} \cdot e^{j\varphi} \right. \\
&\qquad \left. \cdot e^{j\frac{\pi}{4}} \left[\frac{I_{\mathrm{DC}}}{I_{\mathrm{INJ}}} + \frac{1}{6} \cos 2\varphi - j\left(\frac{1}{3}\sin 2\varphi\right) \right] \right\} \\
&= \mathrm{Re}\left\{ \frac{4\sqrt{2}}{\pi} I_{\mathrm{INJ}} \cdot e^{j\omega t} \cdot e^{j\varphi} \cdot e^{j\frac{\pi}{4}} \right. \\
&\qquad \cdot \left[\left| \frac{1}{\eta} + \frac{1}{6}\cos 2\varphi - j\left(\frac{1}{3}\sin 2\varphi\right) \right| \right. \\
&\qquad \left. \left. \cdot e^{-j\arctan\left(\frac{(\eta/3)\sin(2\varphi)}{1+(\eta/6)\cos(2\varphi)}\right)} \right] \right\} \\
&= \mathrm{Re}\left\{ \frac{4\sqrt{2}}{\pi} \left| \frac{1}{\eta} + \frac{1}{6}\cos 2\varphi - j\left(\frac{1}{3}\sin 2\varphi\right) \right| I_{\mathrm{INJ}} \right. \\
&\qquad \left. \cdot \left[e^{j\omega t} \cdot e^{j\varphi} \cdot e^{j\frac{\pi}{4}} \cdot e^{-j\arctan\left(\frac{(\eta/3)\sin(2\varphi)}{1+(\eta/6)\cos(2\varphi)}\right)} \right] \right\} \\
&= \mathrm{Re}\left\{ \frac{4\sqrt{2}}{\pi} \left| \frac{1}{\eta} + \frac{1}{6}\cos 2\varphi - j\left(\frac{1}{3}\sin 2\varphi\right) \right| I_{\mathrm{INJ}} \right. \\
&\qquad \left. \cdot \left[e^{j\omega t} \cdot e^{j\left(\varphi + \frac{\pi}{4} - \arctan\left(\frac{(\eta/3)\sin(2\varphi)}{1+(\eta/6)\cos(2\varphi)}\right)\right)} \right] \right\} \\
&= \left[\frac{4\sqrt{2}}{\pi} \left| \frac{1}{\eta} + \frac{1}{6}\cos 2\varphi - j\left(\frac{1}{3}\sin 2\varphi\right) \right| I_{\mathrm{INJ}} \right] \\
&\quad \cdot \cos\left(\omega t + \varphi + \frac{\pi}{4} - \arctan\frac{\frac{1}{3}\eta\sin 2\varphi}{1+\frac{1}{6}\eta\cos 2\varphi}\right) \\
&= I_T \cos\left(\omega t + \gamma(\varphi)\right) \qquad \text{(B.2)}
\end{aligned}$$

where η is the injection current ratio and equal to $I_{\mathrm{INJ}}/I_{\mathrm{DC}}$. From (B.2), I_T and $\gamma(\varphi)$ can be found as

$$I_T = \frac{4\sqrt{2}}{\pi} \left| \frac{1}{\eta} + \frac{1}{6}\cos 2\varphi - j\left(\frac{1}{3}\sin 2\varphi\right) \right| I_{\mathrm{INJ}} \qquad \text{(B.3)}$$

$$\gamma(\varphi) = \varphi + \frac{\pi}{4} - \arctan\left(\frac{\frac{1}{3}\eta\sin 2\varphi}{1+\frac{1}{6}\eta\cos 2\varphi}\right). \qquad \text{(B.4)}$$

Therefore, the phase response can be expressed as

$$\alpha(\varphi) = \gamma(\varphi) - \varphi = \frac{\pi}{4} - \arctan\left(\frac{\frac{1}{3}\eta\sin 2\varphi}{1+\frac{1}{6}\eta\cos 2\varphi}\right). \qquad \text{(B.5)}$$

It is known that, the impedance of an *LC* tank can be described as

$$H(\omega) = \frac{H_o}{1 + j2Q\dfrac{\omega - \omega_o}{\omega_o}} = |H(\omega)|\, e^{j\angle H(\omega)} \tag{B.6}$$

where Q is the quality factor of the *LC* network. From (B.6), the phase of $H(\omega)$ is

$$\angle H(j\omega) = -\arctan\left(2Q\frac{\omega - \omega_o}{\omega_o}\right). \tag{B.7}$$

To derive an analytical expression for the locking range, let us suppose that there is a sufficient loop gain for the close loop. In such a case, the locking range is only limited by the phase condition of the Barkhausen criteria. Using (B.5) and (B.7), the loop phase under the Barkhausen criteria can be shown as

$$\alpha(\varphi) + \angle H(j\omega) = 0. \tag{B.8}$$

Substituting (B.5) and (B.7) into (B.8), we have

$$-\arctan\left(\frac{\frac{1}{3}\eta\sin 2\varphi}{1 + \frac{1}{6}\eta\cos 2\varphi}\right) = \arctan\left(2Q\frac{\omega - \omega_o}{\omega_o}\right) - \frac{\pi}{4}. \tag{B.9}$$

The right-hand side can be rewritten as

$$-\arctan\left(\frac{\frac{1}{3}\eta\sin 2\varphi}{1 + \frac{1}{6}\eta\cos 2\varphi}\right) = \arctan\left(\frac{2Q\dfrac{\omega - \omega_o}{\omega_o} - 1}{2Q\dfrac{\omega - \omega_o}{\omega_o} + 1}\right). \tag{B.10}$$

By solving (B.10), the single-sided locking range can be expressed as

$$\Delta\omega \equiv |\omega - \omega_o| = \left(\frac{\omega_o}{2Q}\right)\cdot\left(\frac{1 + \frac{1}{6}\eta\cos 2\varphi - \frac{1}{3}\eta\sin 2\varphi}{1 + \frac{1}{6}\eta\cos 2\varphi + \frac{1}{3}\eta\sin 2\varphi}\right). \tag{B.11}$$

When the phase φ is equal to $3\pi/4$, the circuit becomes a quadrature output system and the maximum locking range can be derived as

$$\Delta\omega = \left(\frac{\omega_o}{2Q}\right)\cdot\left(\frac{1 + \frac{1}{3}\eta}{1 - \frac{1}{3}\eta}\right). \tag{B.12}$$

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