Design of an All-Digital LVDS Driver

Hungwen Lu, Hsin-Wen Wang, Chauchin Su, *Member, IEEE*, and Chien-Nan Jimmy Liu, *Member, IEEE*

***Abstract*—This paper presents an all-digital low-voltage-differential-signaling (LVDS) driver design for Serial Advanced Technology Attachment II. A simultaneous-switching-noise reduction technique and an autocalibration mechanism are implemented to suppress switching noise and to handle process and environmental variations. The circuit is implemented in a 0.18-μm 1P6M CMOS process with a core area of 0.072 mm^2. At 3 Gbps, it consumes 9 mW of power under a 1.8-V power supply or 3 pJ/bit.**

***Index Terms*—Low-voltage-differential-signaling (LVDS) driver, simultaneous switching noise (SSN).**

I. Introduction

LOW-VOLTAGE differential signaling (LVDS) [1]–[11] is a technique to increase data rates and also decrease power consumption for point-to-point transmission. Fig. 1 shows three LVDS designs discussed in previous papers. As shown in Fig. 1(a), Vogel *et al.* [2] use complementary current sources and MOS switches to reduce *simultaneous switching noise* (SSN) and increase noise immunity. In order to reduce input loading, [3]–[6], as shown in Fig. 1(b), replace PMOS switches by NMOS switches. Thus, the power and hardware overhead of predrivers are significantly reduced. However, when the technology is scaled down and the supply voltage is reduced, the cascode topology drivers face challenges of limited overdrive voltage and reduced noise margins. Therefore, as shown in Fig. 1(c), [7] and [8] apply a single current source to alleviate overdrive voltage and noise margin issues. However, this cascode of the three transistors from $V_{\rm dd}$ to $V_{\rm ss}$ still has limitations.

To further reduce the number of cascoding transistors, this paper employs digital inverters as LVDS drivers, as shown in Fig. 2(a). With only two transistors, the overdrive voltages and noise margins can be extended. As a result, the device sizes and the power consumption can be reduced. However, without constant current sources for the differential operation, the SSN and the *process, supply voltage, and temperature* (PVT) variations become two major concerns. Therefore, we propose an SSN reduction technique and an autocalibration mechanism to solve these two problems.

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H. Lu and C.-N. J. Liu are with the Department of Electrical Engineering, National Central University, Jung-Li City 320, Taiwan (e-mail: s9521011@cc.ncu.edu.tw).

C. Su is with the Department of Electrical and Control Engineering, National Chiao Tung University, Hsinchu 300, Taiwan.

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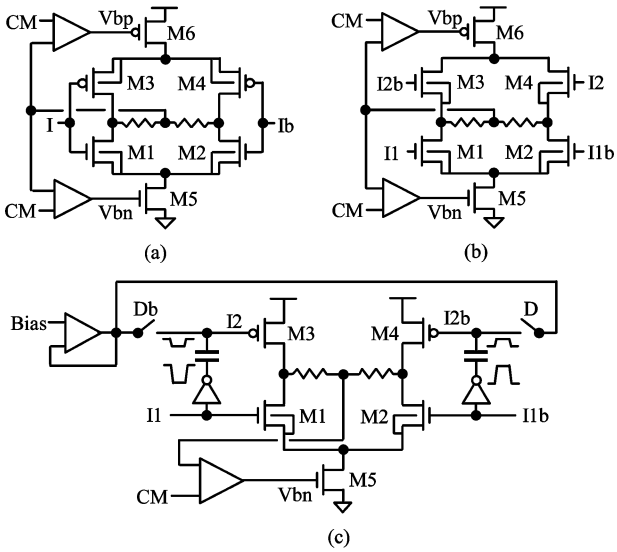


Fig. 1. Reported LVDS driver (a) Cascode topology Version 1 [2] (b) Cascode topology Version 2 [4]. (c) Folded topology [7].

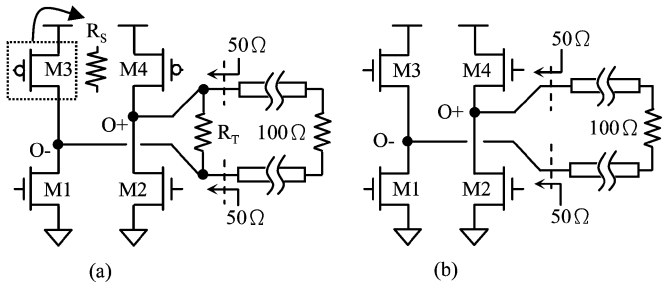


Fig. 2. Proposed LVDS drivers: (a) Version 1 for general case and (b) version 2 for low-power case.

This paper is organized as follows. Section II introduces the digitalized LVDS drivers and the output-level calibration circuits. Section III describes the proposed SSN reduction technique used in the predriver. The implementation and the measurement of the test chip are discussed in Section IV, which is followed by concluding remarks in Section V.

II. Digital LVDS Driver

A. Driver Architecture

Fig. 2 shows the proposed LVDS drivers. These drivers remove current sources and use full-swing input signals. Because of a higher overdrive voltage, the size and parasitic capacitances of data switches become lower. Moreover, the successive predriver stage can be easily designed. Finally, the area of the overall driver system can be significantly reduced.

In general, the transmission channel is designed to have a characteristic impedance of 50 Ω. Hence, a termination resis-

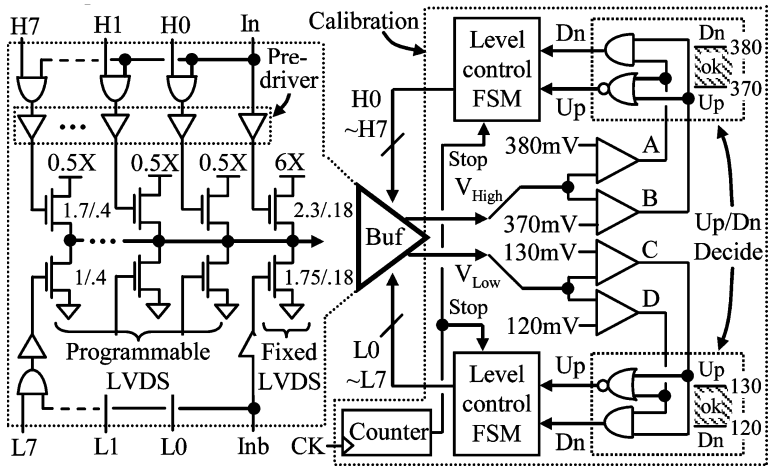


Fig. 3. Size set of LVDS2 and output-level calibration architecture.

tance of 50 Ω is required to minimize the reflection and maintain the signal integrity. In this paper, the near-end matching is achieved by a turn-on resistance of data switches (R_S) and an on-chip polyresistor (R_T), as shown in Fig. 2(a). The output swing is calculated as follows:

$$V_{O+}-V_{O-} = V_{\mathrm{DD}} \cdot \frac{(100//R_T)}{(100//R_T)+2R_S}. \tag{1}$$

Therefore, the ratio of the static current between the reported LVDS driver $(I_{S,\mathrm{Con}})$ and the proposed one $(I_{S,\mathrm{Pro}})$ is as follows:

$$\frac{I_{S,\mathrm{Pro}}}{I_{S,\mathrm{Con}}} = \frac{\frac{(V_{O+}-V_{O-})}{(100//R_T)}}{\frac{(V_{O+}-V_{O-})}{50}} = 0.5 + \frac{50}{R_T}. \tag{2}$$

Equations (1) and (2) indicate that the proposed driver can reduce the static current by up to 50% and raise the output swing by up to $V_{\mathrm{DD}}/2$. Fig. 2(b) is the lowest power case that removes the on-chip polyresistor $(R_T = \infty)$ and makes the turn-on resistance of the data switch 50Ω $(R_S = 50)$. All the data switches are implemented by NMOS transistors to minimize the parasitic capacitance. The digital driver is designed regarding the Serial Advanced Technology Attachment specification [12].[1] Since the differential output swing is 0.5 V with a common-mode voltage of 0.25 V, the proposed driver utilizes two supply voltages, 1.8 V for the predriver and 0.5 V for the output driver.

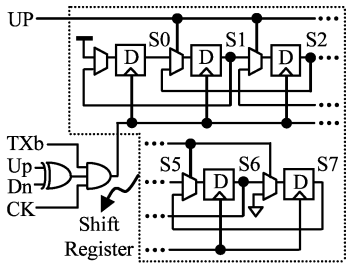
B. PVT Variation Consideration

Under PVT variation, the driver is unlikely to provide a 50-Ω matching and maintain a 250-mV common-mode voltage. Therefore, an autocalibration mechanism is implemented. The block diagram shown in Fig. 3 is composed of programmable drivers, comparators, and level control *finite-state machines* (FSMs). The differential outputs are compared with 375 ± 10 mV and 125 ± 10 mV or other target levels. The compared results of the differential outputs are fed to two FSMs in order to determine how many numbers of drivers should to be turned on. The pull-up and -down drivers are controlled independently. Additionally, a calibration counter is applied to stop the FSM after the calibration is finished.

[1]Available online at: http://www.serialata.org/

	S0	S1	S2	S3	S4	S5	S6	S7
UP	0	0	0	0	0	0	0	0
=0	1	0	0	0	0	0	0	0
	1	1	0	0	0	0	0	0
	1	1	1	0	0	0	0	0
	1	1	1	1	0	0	0	0
	1	1	1	1	1	0	0	0
	1	1	1	1	1	1	0	0
UP	1	1	1	1	1	1	1	0
=1	1	1	1	1	1	1	1	1

(a)



(b)

Fig. 4. Level control FSM: (a) Control code. (b) Schematic.

Fig. 4 shows the schematic and control codes of the FSM which is similar to a bidirectional shifter. $S0-S7$ connect to the gates of the drivers in order to either turn on or off the transistors. $S0-S7$ will shift left or right depending on whether the "Up" signal is HIGH or LOW. The calibration process will be completed when the output level enters the desired range or the calibration counter overflows.

Fig. 5 shows the relationship between the output levels and the number of turned-on transistors at the SS, TT, and FF corners, which is simulated at 27 °C. As one can see, regardless of the process corner, there exists at least one combination that can produce the desired output levels.

To sum up, the calibration solves several problems in a single approach. First, the offset is controlled at 250 mV, and the differential swing is controlled at 500 mV. Next, the reflection is minimized due to the equivalent 50- Ω termination at the near end. Finally, the power consumption is halved because no passive resistance exists in the near-end termination.

III. SSN-Reduced Predriver

The proposed SSN-reduced predriver is composed of a distributed-and-weighted buffer and a duty-cycle-adjustment buffer. Their functions and designs are described in the following sections.

A. Distributed-and-Weighted Predriver

The reported SSN-reduction techniques reduce the supply current fluctuation during the data transition. As shown in Fig. 6(a), Cabara *et al.* [13], Garcia *et al.* [14], and Shin *et*

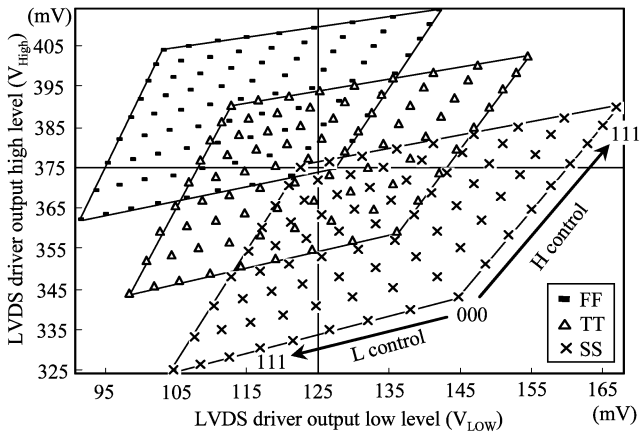


Fig. 5. Output levels of LVDS2 at different corners and controls.

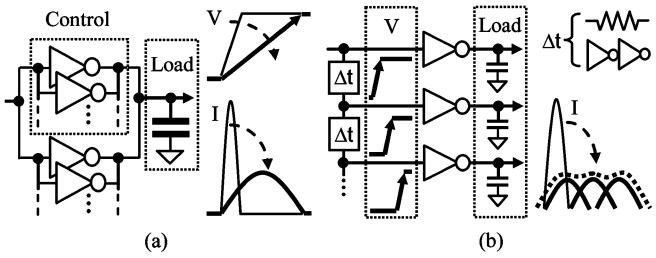


Fig. 6. (a) Slew-rate-control buffer and (b) distributed-and-weighted buffer.

al. [15] adjust the output loading capacitance or charged/discharged current to change output slew rates. Since the slew rate is highly related to the noise immunity, it results in a tradeoff between the SSN and the noise immunity. Senthinathan and Prince [16] and Deutschmann and Ostermann [17] propose a distributed-and-weighted buffer that divides a large driver into several small subdrivers and triggers subdrivers in order in a short timing interval, as shown in Fig. 6(b). This approach has a higher noise immunity because the slew rates of the divided driving signals are not lowered.

In order to estimate the noise immunity to the power supply of both SSN-reduction buffers, the distributed-and-weighted and slew-rate-control buffers are modeled as a single-pole system, as shown in Fig. 7. N is the number of taps in the distributed-and-weighted buffer. When we set up a step input, the timing of output data crossing through 0.5 is denoted as T_1. T_1 is equal to $\ln 2 \cdot R_O C_O$. R_O and C_O are the parasitic resistance and capacitance at the output, respectively. The jitter caused by the supply noise is as follows:

$$T_j = \Delta T_1 = \ln 2 \cdot \Delta V_{\mathrm{DD}} \frac{\mathrm{d}R_O}{\mathrm{d}V_{\mathrm{DD}}} C_O. \tag{3}$$

According to (3), the jitters of the slew-rate-control buffer $T_{j,\mathrm{SRC}}$ and the distributed-and-weighted buffer $T_{j,\mathrm{DW}}$ affected by the supply noise are represented, respectively, as

$$T_{j,\mathrm{SRC}} = \ln 2 \cdot \Delta V_{\mathrm{DD}} \frac{\mathrm{d}R_{O,\mathrm{SRC}}}{\mathrm{d}V_{\mathrm{DD}}} (C_{O,\mathrm{SRC}} + C_L) \tag{4}$$

$$T_{j,\mathrm{DW}} = \ln 2 \cdot \Delta V_{\mathrm{DD}} \frac{\mathrm{d}R_{O,\mathrm{DW}}}{\mathrm{d}V_{\mathrm{DD}}} \left(C_{O,\mathrm{DW}} + \frac{C_L}{N} \right). \tag{5}$$

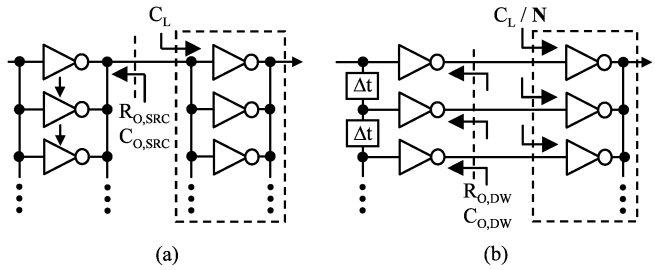


Fig. 7. Parasitic effects of the (a) slew-rate-control and (b) distributed-and-weighted buffers.

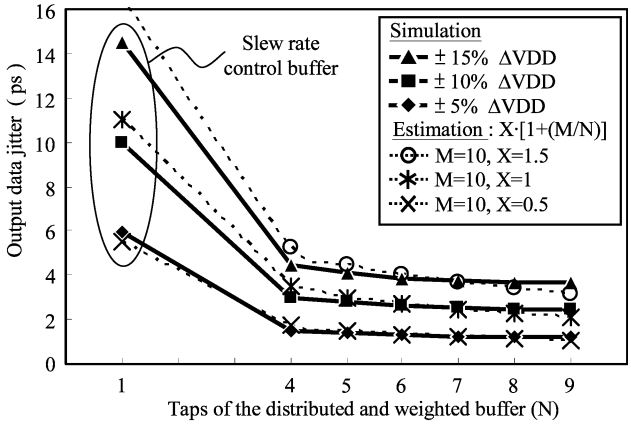


Fig. 8. Jitter to noise sensitivity calculation and simulation.

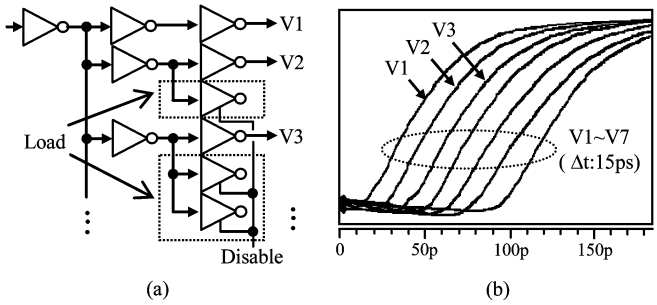


Fig. 9. Proposed distributed-and-weighted buffer. (a) Circuit. (b) Simulation.

Two assumptions are made for comparison

$$\frac{\mathrm{d}R_{O,\mathrm{SRC}}}{\mathrm{d}V_{\mathrm{DD}}} \approx \frac{\mathrm{d}R_{O,\mathrm{DW}}}{\mathrm{d}V_{\mathrm{DD}}}, C_{O,\mathrm{SRC}} \approx C_{O,\mathrm{DW}} = C_L/M. \tag{6}$$

First, the variation of parasitic resistance caused by the supply noise remain the same in both architectures. Second, the parasitic capacitances $(C_{O,\mathrm{SRC}}, C_{O,\mathrm{DW}})$ are identical, and they are equal to $1/M$ times the input capacitance (C_L) of driver. Therefore, the ratio of (4) to (5) becomes

$$T_{j,\mathrm{SRC}} : T_{j,\mathrm{DW}} \approx (l + M) : \left(1 + \frac{M}{N}\right). \tag{7}$$

According to a random supply noise at a percentage of 5%–15%, Fig. 8 shows the simulated and the estimated jitters at different numbers of taps (N). $N = 1$ refers to slew-rate-control buffer. $N \geq 4$ indicates a distributed-and-weighted buffer.

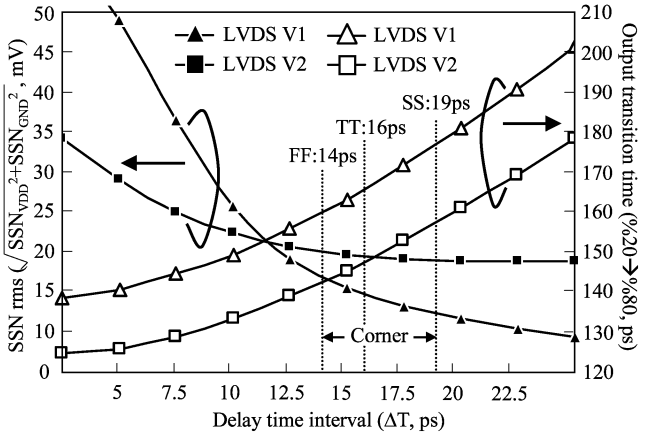


Fig. 10. Distributed-and-weighted buffer simulation.

For the estimated jitter, X denotes a weighting factor which is adjusted manually to match the simulation results. We note that a high timing interval Δt between the driving signals will result in a ladderlike output and cause more jitters.

In previously reported designs, the distributed-and-weighted buffer delays signals through the application of inverters and resistors. However, these designs cannot achieve a high resolution. Therefore, we propose a new distributed-and-weighted buffer (see Fig. 9) to reach a higher resolution. In our design, the driving signal goes through several paths with different loadings after the data have passed the first two inverters. Additionally, signals V1 and V2 rise at different times due to the differences in the loading. Finally, some inverters are added at V1, V2, and V3 to make every delayed driving signal have the same transition time. Based on this framework, the driving signal is divided into seven subsets. The first six signals are used to drive the fixed drivers, and the last one is for the programmable drivers, as shown in Fig. 3.

In order to determine an optimum resolution, we have the SSN and the output transition time as a function of the delay spread, as shown in Fig. 10. The timing interval (Δt) and the number of subdrivers (N) should be maximized in order to minimize the SSN. However, this maximization will limit the output signal slew rate. In addition, Fig. 10 shows that the SSN has an apparent crossover during the time resolution between 20 and 15 ps. Therefore, the timing interval of each signal should be designed to 15 ps in order to reach its optimum. In a 0.18-μm technology, 15 ps is about one-forth the gate delay.

B. Duty-Cycle Adjustment

In addition to the distributed-and-weighted predriver, the duty-cycle adjustment is also used to reduce the SSN. For a perfectly matched 50% duty-cycle driving signal and LVDS1, as shown in Fig. 11(a), V and V_b signals have a crossing point at $V_{\rm DD}/2$. With a nonzero threshold voltage $(V_{\rm TH})$, the transistor controlled by V is turned off before the one controlled by V_b is turned on. Thus, this phenomenon creates a total current discontinuity and makes the SSN increase. In order to avoid the current discontinuity, the duty cycle for V should be extended, as shown in Fig. 11(b), to have the transistor turned on before it

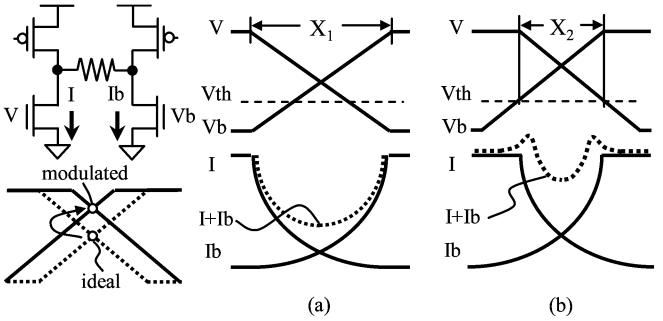


Fig. 11. Current variation curve of LVDS1: (a) Crossing point at central region and (b) crossing point at upper region.

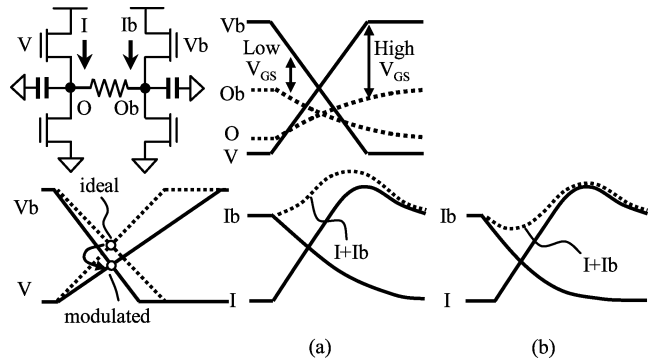


Fig. 12. Current variation curve of LVDS2: (a) Crossing point at central region and (b) crossing point at lower region.

is turned off. As a result, the total current fluctuation is reduced. The ideal crossing point is at $(V_{\rm DD} - V_{\rm TH})/2$.

Unlike LVDS1, the current of LVDS2 is not in linear transition because the overdrive voltage of the upper switches is in relation to LVDS2's output levels. Fig. 12 shows the current transfer curve of LVDS2 at different input duty cycles. For the upper switches, the overdrive voltage at the rising edge is higher than that at the falling edge, which causes an unbalance between the charge and discharge currents. Thus, in Fig. 12(a), a positive current pulse is induced with a 50% duty cycle. In order to reduce a pulse, the duty cycle is adjusted to above 50%, and the falling edge needs to be sharper than the rising edge.

Fig. 13 is the simulation setup used to analyze the relationship between the current variation, the duty cycle, and the SSN. T_{D1}, T_{D2}, T_{D3}, and T_{D4} are the duty cycle adjustments at different inputs. C_L is the loading capacitance. Two inductances of 2 nH at power supplies are the bonding wires. Fig. 14 shows the current variations of LVDS1 and LVDS2. First, the dotted lines represent individual currents (upper) and the total current (lower) without duty-cycle adjustments. The solid lines refer to currents with a duty-cycle adjustment of 20 ps in LVDS1 and that of -15 ps in LVDS2. Therefore, the total current fluctuation becomes much smaller in terms of this adjustment.

Fig. 15 shows the relationship between the duty cycle and the SSN, in which C_L is 2 pF. The SSN of LVDS1 has a high variation from 6 to 40 mV when T_{D1} and T_{D2} are altered from -40 to 40 ps. The SSN at ground is only affected by T_{D1}, and the SSN at power is only affected by T_{D2}. The optimum T_{D1} and T_{D2} are 13 and -13 ps, respectively. Compared with that of LVDS1, the

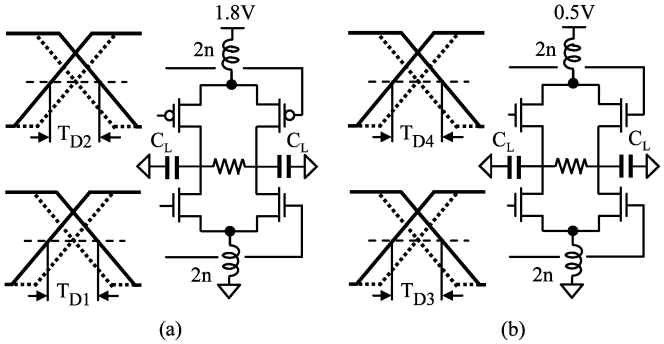


Fig. 13. Duty-cycle simulation setting: (a) LVDS1. (b) LVDS2.

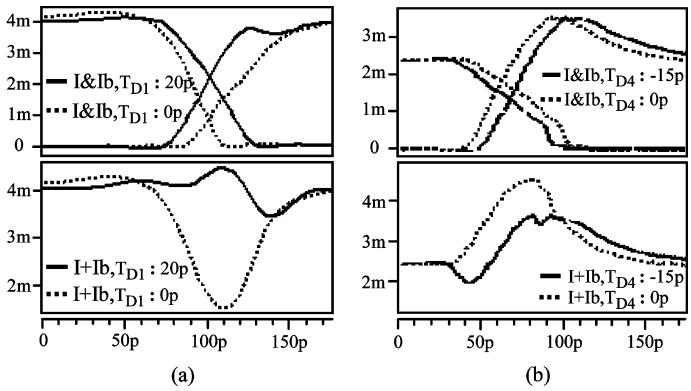


Fig. 14. Simulated current variation: (a) LVDS1 and T_{D1} are 0 or 20 ps. (b) LVDS2 and T_{D4} are 0 and -15 ps.

SSN of LVDS2 is less sensitive to the duty cycle, which varies from 14 to 25 mV. The SSN at ground is affected by T_{D3} and T_{D4}, in which T_{D4} has a higher weighting. Similarly, the SSN at ground is mainly affected by T_{D3}. The optimum T_{D3} and T_{D4} are -5 and -15 ps, respectively.

Because the current of LVDS2 is related to output levels, its optimum duty cycle also varies regarding loading capacitances. Fig. 16 shows the optimum duty cycles at different loading capacitances. For LVDS2, the current mismatch is inversely proportional to the loading capacitance. A lower loading capacitance results in a higher mismatch; therefore, the crossing point needs to be changed to a lower region. For LVDS1, its charge and discharge currents are only controlled by inputs. Hence, its optimum duty cycle is independent of the output capacitances. This design operates at 3 Gbps, and its output capacitance should be defined above 3 pF in order to avoid the *inter-symbol interference* (ISI) effect. Thus, the optimum duty cycle is defined by a 2-pF loading capacitance.

In Fig. 17, the duty cycle is adjusted by using two stages of inverters with a specific size ratio. Thus, four optimum duty cycles can be obtained. On the other hand, the inverter can achieve a very low cost, but its performance would be various regarding processes, supplies, and environmental effects. Hence, an automatic control system is required to compensate process variations.

C. Process Variation and Driver Comparison

Fig. 18 shows that, by using H-SPICE, the Monte Carlo simulations represent different corner cases. In each case, we take

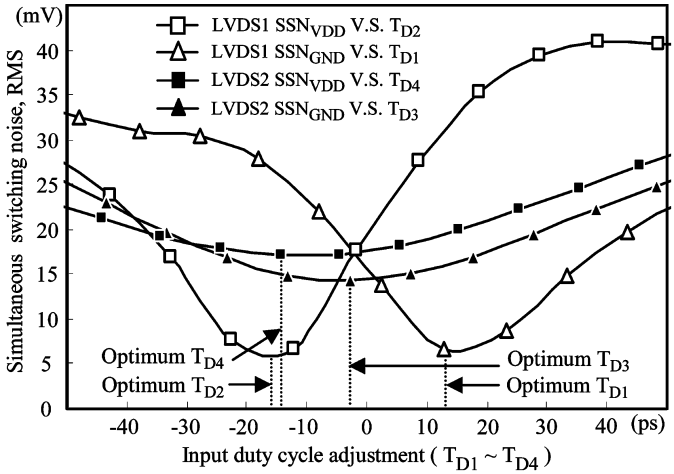


Fig. 15. SSN versus input duty-cycle adjustment.

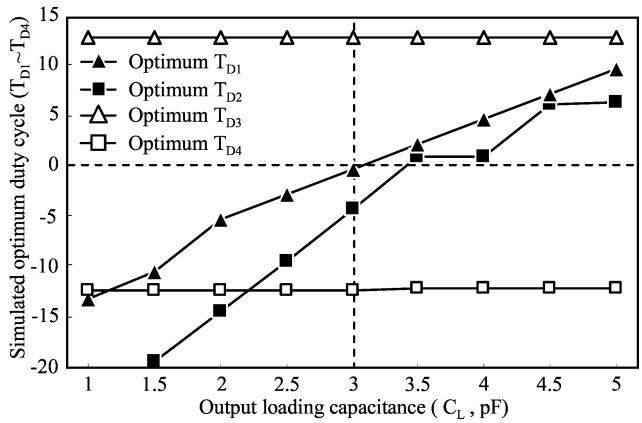
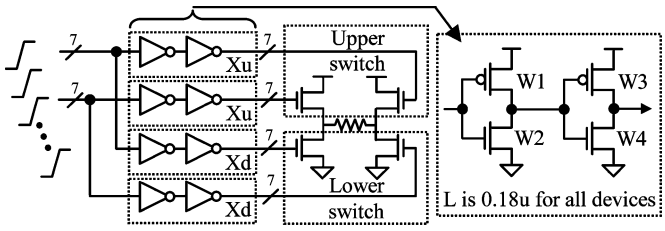


Fig. 16. Optimum duty cycle versus output loading capacitance.



Size set for LVDS1

	W1	W2	W3	W4
Xd	2.08u	0.69u	2.25u	0.52u
Xu	2.27u	0.5u	2.06	0.71u

Size set for LVDS2

	W1	W2	W3	W4
Xd	2.28u	0.49u	2.05u	0.72u
Xu	2.35u	0.42u	1.95u	0.82u

Fig. 17. Schematic and size set of duty-cycle-adjustment buffer.

50 samples and attain their average values. Moreover, the SSN of LVDS1 is more sensitive to process variation than that of LVDS2, but LVDS1's value at an optimum duty cycle is much lower than LVDS2's. For LVDS1, the SSN is dominated by the duty cycle. However, the delay time has only a minor impact on LVDS1. In addition, because the duty cycle variations are skewed at FS and SF cases, these variations cause more SSN

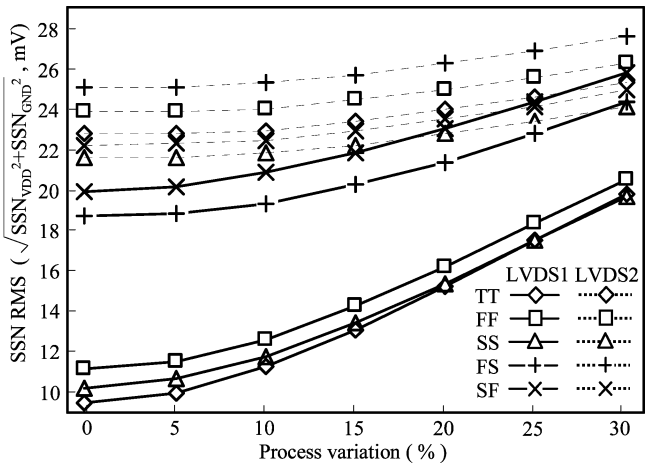


Fig. 18. SSN at different corner cases and process variation.

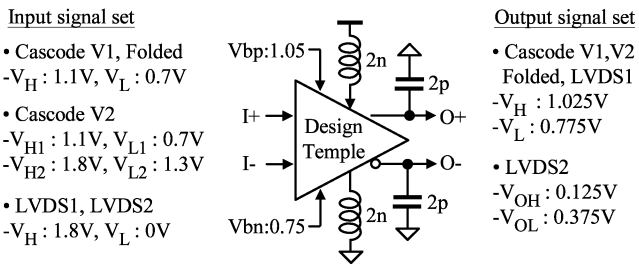


Fig. 19. Simulation set for LVDS driver comparison.

TABLE I
SIMULATED LVDS DRIVER COMPARISON

LVDS (Fig.1)		Cascode V1	Cascode V2	Folded
Size List (W)	M1,M2	5.9um, M=10	6.35um, M=10	7.05um, M=10
	M3,M4	21.8um, M=10	6.6um, M=10	6.85um, M=10
	M5	8.2um, M=10	8.9um, M=10	9.85um, M=10
	M6	32.8um, M=10	36um, M=10	
	Σ(W×L)	123.66 um^2	104 um^2	42.75 um^2
Input capacitance		736f	177f (I1)&192f (I2)	405f
Average current		5.12mA	5.46mA	6.06mA
SSN (rms) VDD / GND		23.4mV / 9.9mV	75.4mV / 10.6mV	4.8mV / 11.4mV
SSN (rms) $\sqrt{VDD^2+GND^2}$		25.4 mV	76.1mV	12.4mV

LVDS (Fig.2)		LVDS1		LVDS2	
Size List (W)	M1,M2	0.73um, M=10		1.24um, M=10	
	M3,M4	2.15um, M=10		1.54um ,M=10	
	Σ(W×L)	5.1 um^2		5 um^2	
Input capacitance		85f		89f	
Average current		4.21mA		2.55mA	
SSN (rms) VDD / GND		Original	52.1mV / 38.5mV	Original	61.7mV / 20.4mV
		Improved	7.2mV / 6.1mV	Improved	18.9mV / 16.1mV
SSN (rms) $\sqrt{VDD^2+GND^2}$		Original	64.8mV	Original	65mV
		Improved	9.4mV	Improved	24.8mV

* Channel length is 0.18um in all MOS, W: Width, M: Parallel connection number

than the other corners. For LVDS2, although the duty cycle variation causes more SSN than the delay-time variation, both variations have similar weighting. Hence, in LVDS2, the SF and FS corners cause more noise than SS and FF corners.

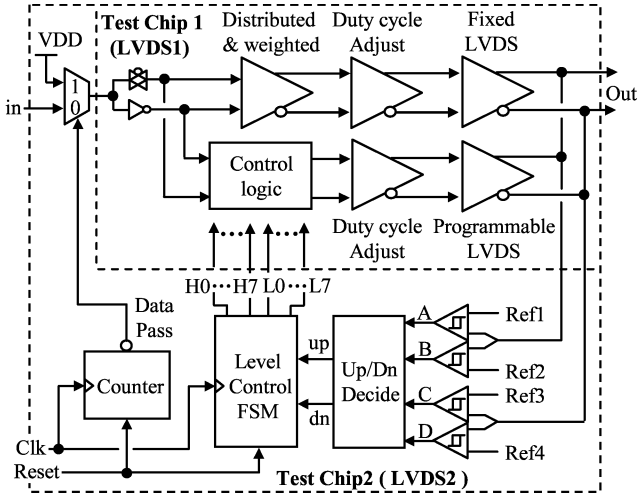
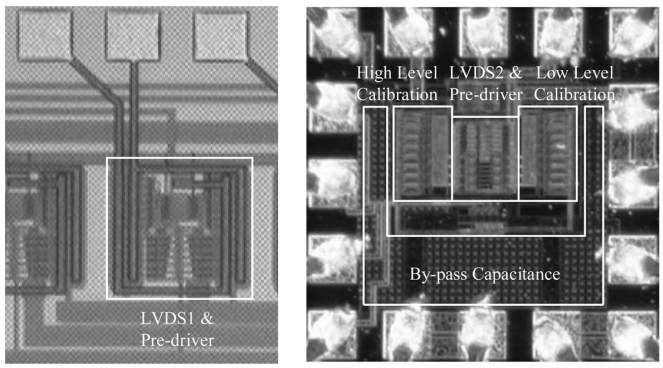


Fig. 20. Test chip architecture.



(a) (b)

Fig. 21. Chip photo: (a) LVDS1. (b) LVDS2.

In addition to the previous factors, the total driver current (I1 + I2, Fig. 14) variation can changes the SSN a lot. However, this factor can be ignored after the output level is calibrated with a feedback circuit.

In order to compare LVDS1 and LVDS2 to the previously reported LVDS drivers, a simulation is made by using the setup shown in Fig. 19. Vbn and Vbp are used for cascode and folded topology LVDS drivers. According to a 2-nH parasitic inductance at the power, a 2-pF loading capacitance, and an output swing of 500 mV, Table I shows the simulated hardware overhead. The proposed digital drivers are better than reported analog drivers in terms of input loading capacitance, area, and static power consumption. However, the proposed digital drivers have higher SSNs. The SSN of LVDS1 with the proposed predriver is reduced from 64.8 to 9.4 mV, and it is better than both the cascode and folded topology drivers. For LVDS2, the SSN is reduced from 65 to 24.8 mV, and it is also better than the cascode V1 and V2. However, it is worse than the folded.

IV. TEST CHIP MEASUREMENT

The proposed digital LVDS driver with SSN reduction and autocalibration is shown in Fig. 20. Two test chips were implemented to verify the proposed designs, as shown in Fig. 21. They are implemented in a 0.18- μm CMOS process. LVDS1,

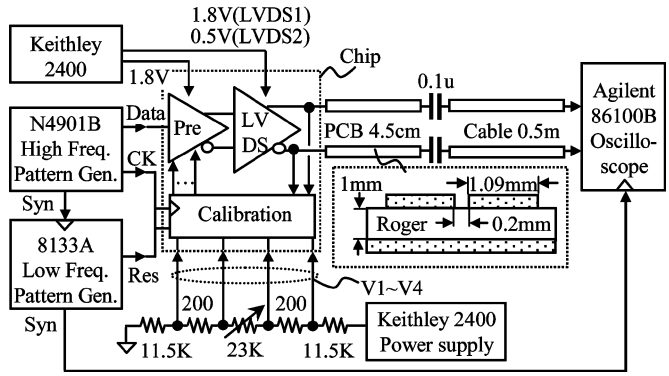


Fig. 22. Test environment setup.

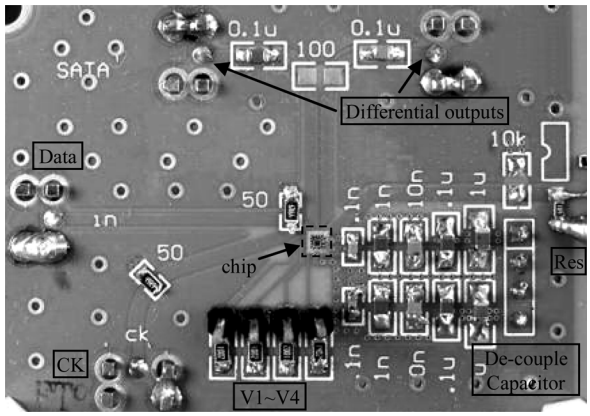


Fig. 23. Test PCB photo.

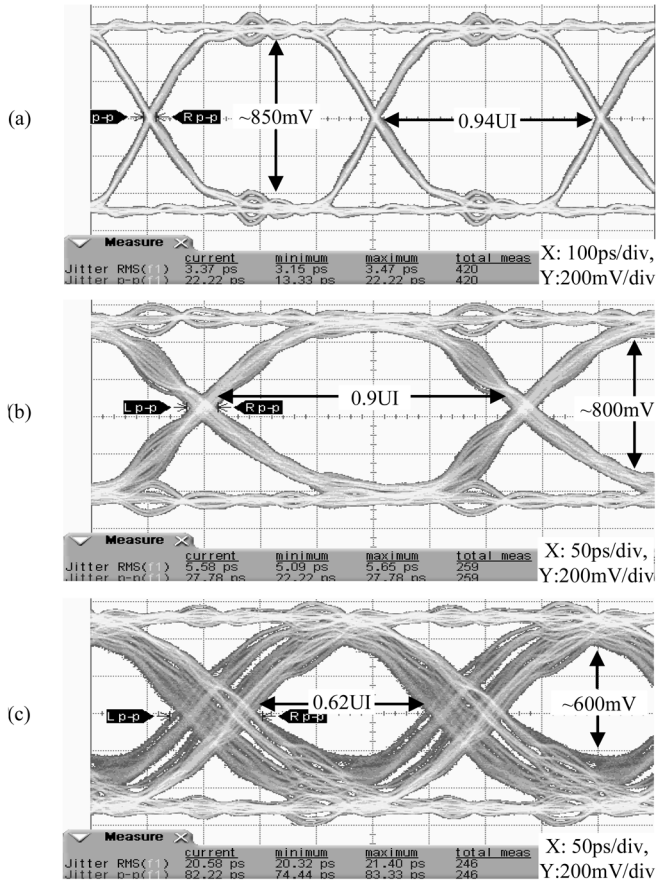


Fig. 24. LVDS1 output eye diagrams: (a) 2.5, (b) 3.5, and (c) 4.5 Gbps.

LVDS2, and the calibration circuit occupy 0.044, 0.024, and 0.048 mm^2 of area, respectively. The test setup is shown in Fig. 22. The test printed circuit board (PCB) in Roger material is shown in Fig. 23. Agilent N4901B generates a full-swing random data input, and Agilent 11801C measures the output eye diagram. Keithley 2400 generates two supply voltages: 0.5 V for the LVDS2 driver and 1.8 V for the LVDS2 predriver and LVDS1. The first test focuses on verifying the output timing jitter and the current consumption under different data rates. Thus, the input data rate was swept from 1.25 to 5 Gbps. The other test examines the function of output-level calibration in LVDS2. N4901B generates a 1.25-GHz clock as the reference clock, and Agilent 8133A generates a periodic 39.06-MHz pulse input as the reset. An adjustable resistor ladder divides the 0.5 V of supply voltage into four reference voltages, 375 ± 10 mV and 125 ± 10 mV.

A. Eye Diagram Measurement

Figs. 24 and 25 show the output eye diagrams of LVDS1 and LVDS2 at different data rates. LVDS1 has a differential swing of 900 mV at steady state. The peak-to-peak jitters are 22.2 ps at 2.5 Gbps and 83.3 ps at 4.5 Gbps. LVDS2 has a differential swing of 488 mV at steady state. The peak-to-peak jitters are 25.67 ps at 2.5 Gbps and 65.56 ps at 5 Gbps. Because of the SSN of the predriver, we can see a periodic spur noise occurring in the eye diagram. Furthermore, the ladderlike rising waveform indicates that the termination is slightly mismatched. It should be noted that the random data generated by N4901B have an intrinsic timing jitter around 5 ps. The peak-to-peak noise in the power supply is around tens of millivolts.

When the data rate is above 3.5 Gbps (4.25 Gbps) in LVDS1 (LVDS2), the data period is less than the effective transition time of the driving signals. Hence, the output jitter is significantly raised due to the ISI effect. With a distributed-and-weighted architecture, Figs. 24(c) and 25(c) show that the transition edge is spread to many specific edges. The measured eye diagrams match the simulated results.

Fig. 26 shows the relationship of the output jitter and the data rate. The dotted lines indicate jitter limitations in *unit-time interval* (UI). The total output jitter limitation for the overall system should be less than 0.25 UI, which is defined by Serial ATA. Therefore, the limitation for drivers should be around 0.1 UI. LVDS1 can achieve 3.5 Gbps, and LVDS2 can achieve 3 Gbps based on the limitation of 0.1 UI.

In order to characterize power efficiency, Fig. 27 shows current consumption as a function of the data rate. For the static power consumption, LVDS1 consumes a total of 7.6 mA under 1.8 V. For LVDS2, the driver consumes 2.5 mA under 0.5 V, and the predriver consumes 0.82 mA under 1.8 V. For the dynamic part, LVDS1 is 1.37 mA/Gbps, and LVDS2 is 0.06 mA/Gbps for the driver and 1.4 mA/Gbps for the predriver.

Through dividing the measured power consumption by the data rate (F), the power efficiencies of LVDS ($E1$) and LVDS2 ($E2$) are calculated as follows:

$$E1 = \frac{1.8(7.6 + 1.37 \times F)}{F} = 2.47 + \frac{13.79}{F} \tag{8}$$

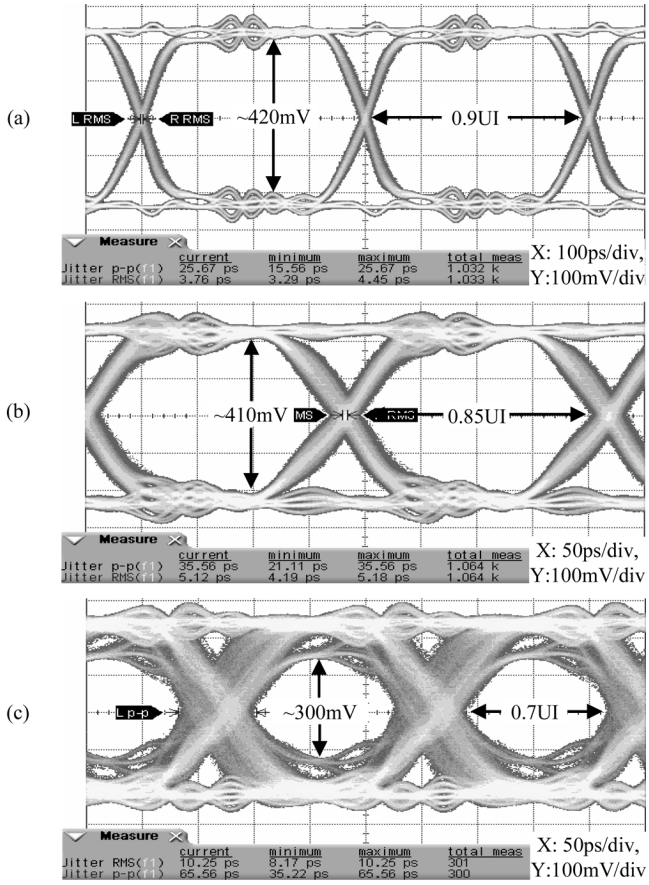


Fig. 25. LVDS2 output eye diagrams: (a) 2.5, (b) 4.25, and (c) 5 Gbps.

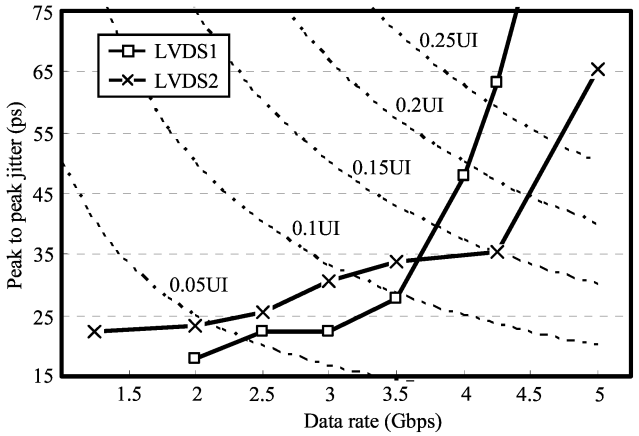


Fig. 26. Relation of output jitter and data rate.

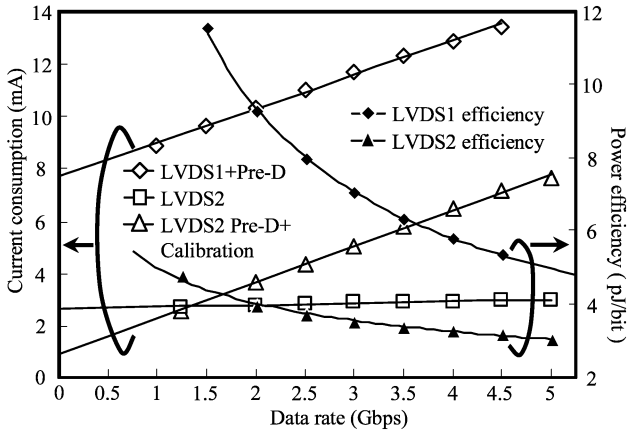


Fig. 27. Relation of current consumption, power efficiency, and data rate.

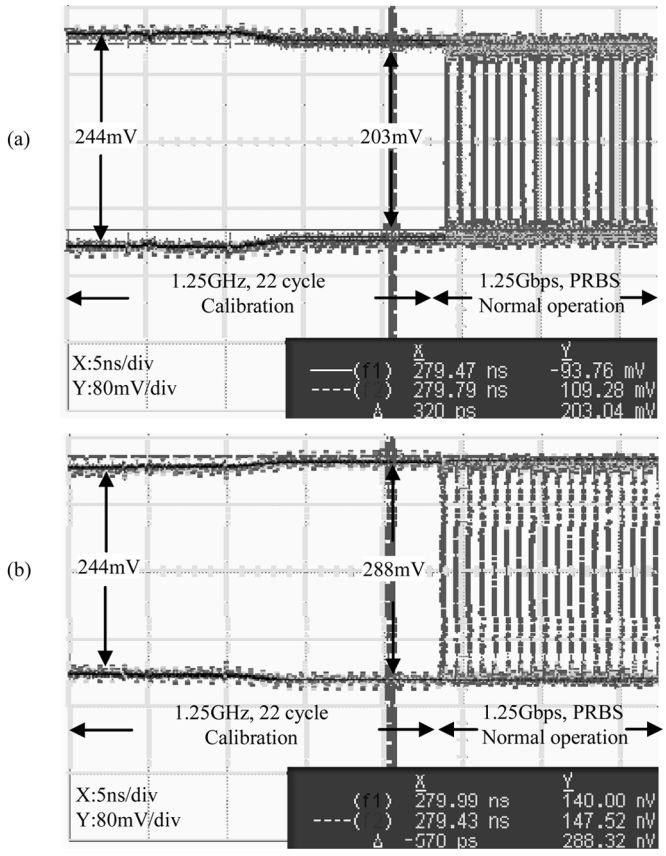


Fig. 28. Autocalibration function verification: (a) Calibrated minimum output swing and (b) calibrated maximum swing.

$$E2 = \frac{0.5\,(2.5 + 0.06 \times F) + 1.8(1.4 \times F)}{F} = 2.55 + \frac{1.25}{F}. \tag{9}$$

According to (8) and (9), the power efficiencies of LVDS1 and LVDS2 at 3 Gbps are 7.06 and 2.97 pJ/ bit.

B. Calibration Function Testing

In LVDS2, the measured eye diagram has a differential mode swing of 488 mV and a common-mode level of 0.25 V; therefore, the calibration does not adjust the output level with the predefined reference voltage. Hence, we set the four reference voltages to 0.25 V, thereby achieving a minimum calibrated output swing, as shown in Fig. 28(a). The reset signal is a 39.06-MHz periodic pulse input to let the output levels be calibrated repeatedly. The calibration takes a total period of 22 clock cycles, and the output level is calibrated to an output swing of 203/406 mV (single/differential). Again, we set the high-level reference voltages to V_{DD} and low-level reference voltages to ground, thereby achieving a maximum calibrated output swing of 288/576 mV, as shown in Fig. 28(b). This shows that the calibration has sufficient ranges to handle the PVT variation.

TABLE II
CHIP SUMMARY

Function	LVDS1	LVDS2 with calibration
Technology	TSMC 0.18um CMOS	TSMC 0.18um CMOS
Supply voltage	1.8V	1.8V, 0.5V
Core size	210um×210um	300um×80um (LVDS) 300um×160um(Calibration)
Power	19.8mW @ 2.5Gbps 22.1mW @ 3.5Gbps 24.1mW @ 4.5Gbps	4.4mW @ 1.25Gbps 9mW @ 3Gbps 12.7mW @4.25Gbps 1.48mW @ Calibration
Output data jitter (Peak-Peak)	22.2ps @ 2. 5Gbps 27.8ps @ 3.5Gbps 83.3ps @ 4.5Gbps	22.2ps @ 1.25Gbps 30.6ps @ 3Gbps 35.6ps @ 4.25Gbps
Output data jitter (RMS)	4.3ps @ 2.5Gbps 5.7ps @ 3.5Gbps 21.4ps @ 4.5Gbps	4.3ps @ 1.25Gbps 5.1ps @ 3Gbps 5.2ps @ 4.25Gbps
Output Swing (single-end)	450mV	203-288mV

TABLE III
LVDS DRIVERS AND LOW-POWER I/O BUFFER COMPARISON

LVDS driver	Reference	JSSC 01 [4]	JSSC 05 [7]	TCAS 06 [18]	ESSCIRC 00 [2]
	Technology	0.35 um	0.35 um	0.35 um BiCMOS	0.18 um
	Supply voltage	3.3 V	1.8 V	1.8 V	1.8V
	Output swing	412 mV	340 mV	300 mV	325mV
	Data rate	1.2 Gbps	1.2 Gbps	2 Gbps	1.25Gbps
	Static power	43 mW	12.8 mW	<10.8 mW	-
	Core size	0.17 mm^2	0.14 mm^2	-	-
LVDS driver	Reference	MWSCAS 01 [21]	ASSCC 05 [22]	This work LVDS1	This work LVDS2
	Technology	0.18 um	0.08 um	0.18 um	0.18 um
	Supply voltage	1.8V	1.2V	1.8 V	0.5 V
	Output swing	-	161mV	450 mV	250 mV
	Data rate	625Mbps	6Gbps	3.5 Gbps	3 Gbps
	Static power	23mW	6.2mW	13.68 mW	1.25 mW
	Core size	0.022 mm^2	-	0.044 mm^2	0.024 mm^2
Low power I/O buffer	Reference	JSSC05 [19]	JSSC06 [20]	This work LVDS1	This work LVDS2
	Technology	0.1 um	0.18 um	0.18 um	0.18 um
	Supply voltage	1.8 V	1.8 V	1.8 V	1.8 V, 0.5 V
	Output swing	100 mV	-	450 mV	250 mV
	Data rate	1 Gbps	3 Gbps	3.5 Gbps	3 Gbps
	Total power	5.6 mW	15 mW	21.01 mW	9 mW
	Power efficiency	5.6 pJ/bit	5 pJ/bit	6pJ/bit	3 pJ/bit
	Core size	0.028 mm^2	0.0014 mm^2	0.044 mm^2	0.024 mm^2

Table II summarizes the results of these two chips. Moreover, in Table III, we compare LVDS1 and LVDS2 to previous LVDS drivers [2], [4], [7], [18], [21], [22]. It should be noted that LVDS2 has the lowest power consumption and a small area overhead. Comparing with low-power I/O designs [19], [20], plus-mode I/Os [19], [20] have the smallest area with good power efficiency. LVDS2 has the highest power efficiency.

V. CONCLUSION

In this paper, we have presented two digital LVDS drivers with novel schemes for SSN reduction and autocalibration. The proposed orderly turned-on and duty-cycle-adjustment methods are effective for SSN reduction. We apply the programmable drivers to solve a process variation problem and to obtain an expected offset and swing. Furthermore, by merging the 100-Ω differential termination resistance into the driver, the power consumption is reduced by half.

Two chips have been implemented in a 0.18- μm CMOS process with a core size of 0.044 mm^2 for LVDS1 and 0.024 mm^2 for LVDS2. For LVDS2, the power consumption is 9 mW at 3 Gbps with a power efficiency of 3 pJ/bit. The jitter performance is 0.092 UI at 3 Gbps and 0.15 UI at 4.25 Gbps. In addition, the results also show that the offset and swing can be calibrated to expected levels.

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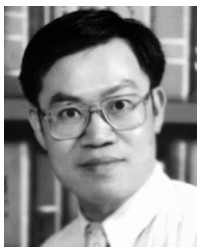
Hungwen Lu received the B.S. degree in electronic engineering from the National Central University, Jung-Li City, Taiwan, in 2001, where he is currently working toward the Ph.D. degree in the Department of Electrical Engineering.

His research interests include high-speed interconnect design and mixed-signal circuit design.

Hsinwen Wang received the M.S. degree in electrical and control engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 2004.

His research interests include high-speed interconnect design and mixed-signal circuit design.



Chauchin Su received the B.S. and M.S. degrees in electrical engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 1979 and 1981, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Wisconsin, Madison, in 1990.

Since graduation, he has been with the Department of Electrical and Control Engineering, National Chiao Tung University. His research interests are in the areas of mixed-analog and digital-system testing and design for testability. He is also involved in projects on baseband and circuit design for wireless communication.

Chien-Nan Jimmy Liu received the B.S. and Ph.D. degrees, both in electronics engineering, from the National Chiao Tung University, Hsinchu, Taiwan.

He is an Associate Professor with the Department of Electrical Engineering, National Central University, Jung-Li City, Taiwan. His research interests include behavioral modeling for analog/mixed-signal designs, high-level power and noise modeling, and functional verification for hardware description language (HDL) designs.

Dr. Liu is a member of Phi Tau Phi.