Enhanced Hole Gate Direct Tunneling Current in Process-Induced Uniaxial Compressive Stress p-MOSFETs

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***Abstract*—On a nominally 1.27-nm-thick gate oxide p-MOSFET with shallow trench isolation (STI) longitudinal compressive mechanical stress, hole gate direct tunneling current in inversion is measured across the wafer. The resulting average gate current exhibits an increasing trend with STI compressive stress. However, this is exactly contrary to the currently recognized trend: hole gate direct tunneling current decreases with externally applied compressive stress, which is due to the strain-altered valence-band splitting. To determine the mechanisms responsible, a quantum strain simulator is established, and its validity is confirmed. The simulator then systematically leads us to the finding of the origin: a reduction in the physical gate oxide thickness, with the accuracy identified down to 0.001 nm, occurs under the influence of the STI compressive stress. The strain-retarded oxide growth rate can significantly enhance hole direct tunneling and thereby reverse the conventional trend due to the strain-altered valence-band splitting.**

***Index Terms*—Layout, mechanical stress, MOSFET, piezoresistance, shallow trench isolation (STI), tunneling.**

I. Introduction

HOLE direct tunneling current across the gate oxide of p-MOSFETs has been extensively studied in the presence of an *external* mechanical stress applied during the measurement of this current [1]–[3]. The corresponding gate oxide thickness change due to the effect of Poisson's ratio has been shown to be negligible in magnitude; for example, in [1], around 0.03% change in the gate oxide thickness has been estimated for an external stress of 300 MPa. Therefore, the physical gate oxide thickness essentially remains unchanged, regardless of the externally applied stress. Under the circumstances, the induced gate current variation can be properly attributed, through the change in both the carrier repopulation and the effective SiO_2/Si barrier height, to the strain-induced valence-band splitting. It has therefore been argued that the hole gate direct tunneling current decreases with the external compressive stress [1], [2]. On the other hand, for the case of p-MOSFETs undergoing a *process*-induced (*internally* applied) mobility-boosting mechanical stress during the manufacturing of the device, hole gate direct tunneling current may encounter complicated situations (gate oxide thickness change due to strain dependence of the oxidation rate, for example), rather than simply the strain-altered valence-band splitting. So far, it has been unclear whether the decreasing trend of the hole direct tunneling with the compressive stress, as claimed in the literature [1], [2], could hold for the internal case. Thus, the ability to distinguish the external stress effect from the internal one and/or find the similarities between the two is crucial.

In this paper, we will elaborate on the above subject. First, we will present the experimental hole gate direct tunneling current of p-MOSFETs under shallow trench isolation (STI)-induced longitudinal compressive stress, which does not appear to follow the trend [1], [2] caused by the strain-altered valence-band splitting alone. A quantum strain simulator will be developed to resolve this contradictory issue. The validity of the simulator will be examined in detail. Then, the quantum simulator will be combined, in a systematic manner, with the experimental data in order to determine the underlying physical origin.

II. Experimental

P-channel MOSFETs, as schematically shown in Fig. 1, were fabricated using a state-of-the-art manufacturing process. In this process, the STI-induced compressive stress was applied prior to the growth of the gate oxide and the source/drain implantation. The nominal process parameters were obtained by the capacitance–voltage fitting: p^+ polysilicon doping concentration $N_{\rm poly} = 1 \times 10^{20}$ cm^{-3}; physical gate oxide thickness $t_{\rm ox} = 1.27$ nm; and n-type substrate doping concentration $N_{\rm sub} = 6 \times 10^{17}$ cm^{-3}. The gate width-to-length ratio was fixed at $W/L = 10\ \mu$m$/1\ \mu$m. The devices were formed on the (001) wafer with the channel length direction along $\langle 110 \rangle$. The use of the wide structures ensures that the transverse channel stress can be reasonably ignored. To control the longitudinal channel stress, the gate to STI spacing, labeled as a in Fig. 1, was drawn with three values of 10.0, 0.495, and 0.21 μm. The corresponding stress magnitude can be determined via the piezoresistance coefficients. First, the peak hole mobility at $V_D = -0.025$ V was measured across the wafer. The relative change of the average peak hole mobility was then obtained with respect to that of $a = 10\ \mu$m, as plotted in Fig. 2 versus

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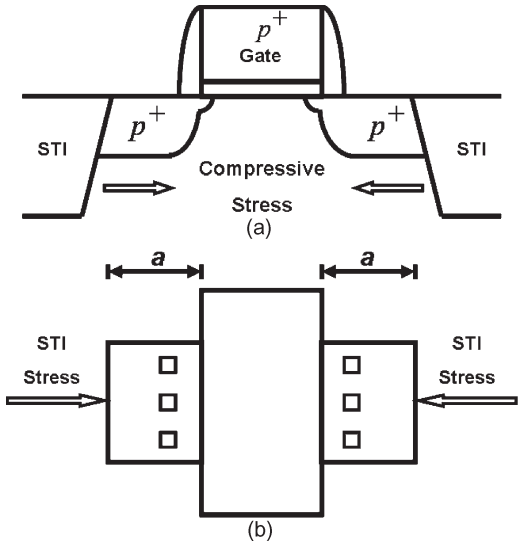

Fig. 1. Schematic demonstration of (a) the cross-sectional and (b) topside view of the test device. The gate edge to STI edge spacing labeled as a is highlighted. The compressive stress is due to the lower thermal expansion rate of STI oxide compared to silicon.

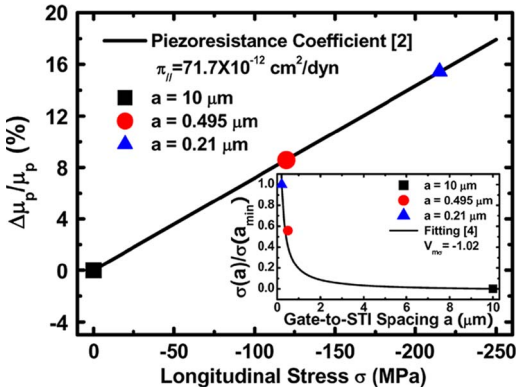

Fig. 2. Measured (symbols) and calculated (line) hole mobility change versus STI stress. The straight line is from the piezoresistance coefficient [2]. The inset shows the extracted stress divided by that of the minimum a as a function of a, along with a fitting curve as cited in [4].

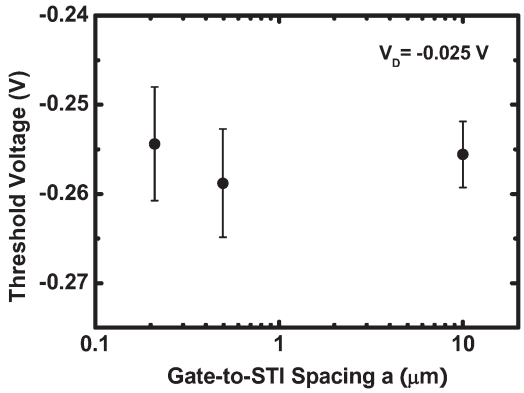

Fig. 3. Measured threshold voltage versus gate-to-STI spacing at $V_D = -0.025$ V. The error bar represents the standard deviation of the distribution and the data point (symbol) represents the average of the distribution.

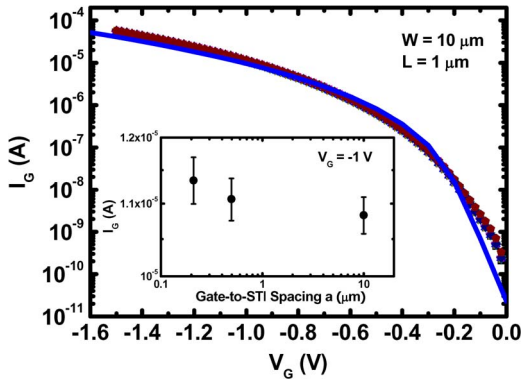

Fig. 4. Comparison of simulated (line) gate current versus gate voltage with those (symbols) measured from eight samples. The different symbols stand for the different device positions on wafer and the different gate-to-STI spacing values. The line represents the no-stress simulation result with the nominal process parameters. The source, drain, and substrate are all tied to the ground. The inset shows the distribution of the measured gate current at $V_G = -1$ V versus gate-to-STI spacing. The error bar represents the standard deviation of the distribution and the data point represents the average of the distribution.

stress. Here, the state-of-the-art inversion-layer piezoresistance coefficient for holes, as quoted elsewhere [2], was employed as demonstrated by a straight line in the figure. The corresponding longitudinal channel stress σ is therefore determined to be around -120 and -215 MPa for $a = 0.495$ and 0.21 μm, respectively. To testify to the validity of the extracted stresses, one empirical formula, which connects the layout parameters to the stress quantities, was also cited elsewhere [4]: $\sigma(a) = \sigma(a_{\min})\ (1 + V_{m\sigma}(a - a_{\min})/a)$, where $a_{\min}$ is the minimum gate-to-STI spacing, and $V_{m\sigma}$ is the maximum variation for $a \to \infty$ with respect to $\sigma(a_{\min})$. Excellent fitting was achieved with $V_{m\sigma} = -1.02$, as shown in the inset of Fig. 2.

To examine the poly stress, the threshold voltage was also measured across the wafer with the results in Fig. 3 in terms of the average and standard deviation of the distribution. The threshold voltage variation appears to be a weak function of the gate-to-STI spacing, and its trend looks irregular, prohibiting the poly stress from being determined. However, in our previous work [9], the electron direct tunneling data confirm the existence of a lateral STI-induced stress in the polysilicon, and since the gate oxide is rather thin, the lateral stress near the polysilicon surface is reasonably close to that of the underlying silicon. The same wafer was used in this study, and thereby, the poly stress was made equal to the channel stress. Extra evidence will be given later.

The hole gate direct tunneling current was measured in inversion with the source, drain, and substrate tied to the ground. Strikingly, the gate current versus gate voltage characteristics measured across the whole wafer do not appear to deviate from each other. This situation is displayed in Fig. 4 for several samples with different a values and different device positions. Obviously, it is difficult to distinguish the measured I–V characteristics in a wide current range. This argument remains valid, regardless of the device position on wafer or the value of a used. To produce a clear difference, the average and standard deviation of the gate current distribution at a specific gate voltage $V_G = -1$ V was adopted, as inserted into Fig. 4. The inset of the figure clearly reveals an increasing trend of the average hole gate direct tunneling current with the compressive stress (decreasing a), which is exactly contrary to that published in the

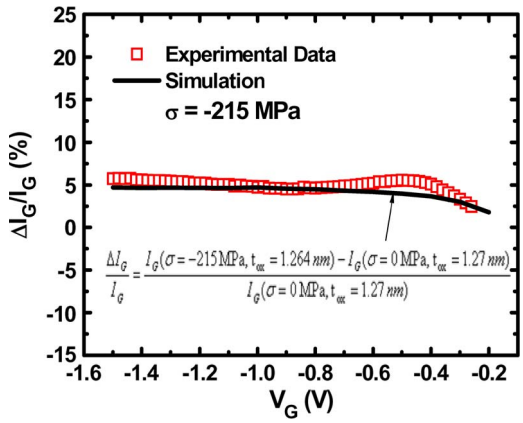

Fig. 5. Experimental and simulated gate current change versus gate voltage under −215 MPa longitudinal stress. The formulas used are inserted.

literature [1], [2]. The role played by the standard deviation of the gate current will be described later. Additionally, the relative change of the average gate current with respect to that of $a = 10\ \mu$m was found to be a weak function of the gate voltage, as shown in Fig. 5 for $\sigma = -215$ MPa. This specific characteristic over the gate voltage can serve as the corroborating evidence while determining the underlying physical mechanisms, as will be explained later.

III. Quantum Strain Simulation

To resolve the contradicting issue mentioned above, a quantum strain simulator was developed around the hole direct tunneling process, as schematically described in Fig. 6 in terms of the energy band diagram. First, with the combination of the six-band $k \bullet p$ Hamiltonian and a triangular-well approximation, as detailed elsewhere [5], the strain-induced valence-band edge shift can be calculated under a certain surface electric field as follows:

$$E(j,i) = \left(\frac{\hbar^2}{2m_{zhi}}\right)^{1/3} \left(\frac{3\pi q F_s \left(j - \frac{1}{4}\right)}{2}\right)^{2/3} + q(E_{V1} - E_{Vi}) \tag{1}$$

where $E(j,i)$ represents the energy of the jth subband in the ith valence band, $i = 1$, 2, and 3 correspond to the first, second, and third valence band, respectively, m_{zhi} is the hole out-of-plane effective mass associated with the ith valence band, F_s is the silicon surface electric field strength, E_{Vi} is the energy of the ith valence band, and q is the elemental charge. The calculated energy levels at $V_G = -1$ V for the top (first), second, and split-off (third) hole subbands are shown in Fig. 7 versus stress. Here, it can be seen that the top subband is insensitive to the stress while for the remaining subbands, the energy levels rise up, thereby reducing the corresponding SiO_2/Si barrier height seen by the holes while tunneling across the oxide. The involved hole out-of-plane effective masses in the inversion layer were found to be fairly constant, i.e., $m_{zh1} = 0.27\ m_0$, $m_{zh2} = 0.22\ m_0$, and $m_{zh3} = 0.23\ m_0$, which are the same values as those of the citation [1].

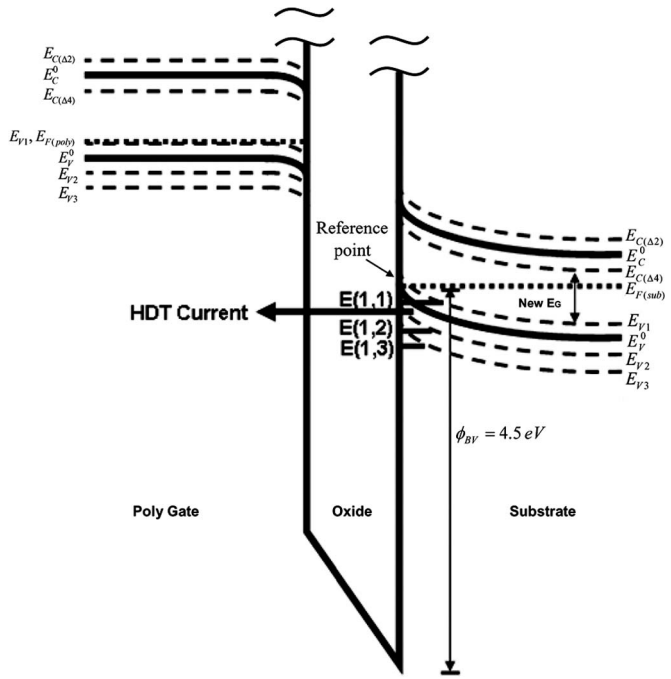

Fig. 6. Schematic energy band diagram of a p^+ polysilicon/SiO_2/n-Si system biased in the inversion condition and stressed with uniaxial compressive conditions. The solid lines indicate the conduction and valence band edge without external stress. The dotted lines indicate the stress induced band edge shift of the conduction and valence band. The figure also shows the energy quantization effect in the inversion layer and the hole direct tunneling process from the inversion layer to the polysilicon gate.

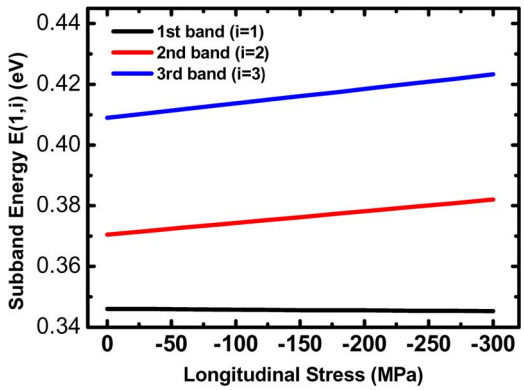

Fig. 7. Calculated energy levels versus stress for the top (first), second, and split-off (third) hole subbands.

Then, the carrier repopulation under stress can be calculated as follows:

$$N(j,i) = \left(\frac{m_{dhi} k_B T}{\pi \hbar^2}\right) \ln\left(1 + \exp\left(\frac{E_F - E(j,i)}{k_B T}\right)\right) \tag{2}$$

where $N(j,i)$ represents the hole density per unit area of the jth subband in the ith valence band, m_{dhi} is the 2-D density of states effective mass of the ith valence band, E_F is the hole Fermi level, k_B is Boltzmann's constant, and T is the absolute temperature. Finally, the triangular-potential-based hole direct

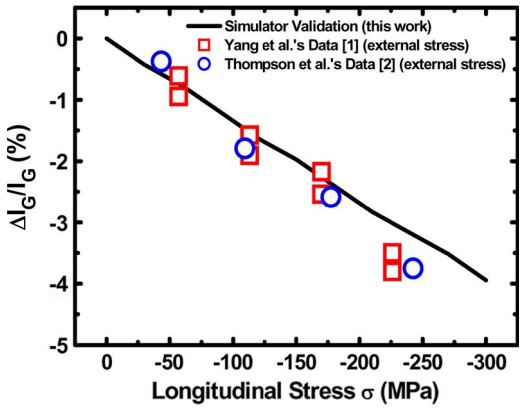

Fig. 8. External-stress-dependent hole gate current data [1], [2] (symbols) used to examine the validity of the quantum strain simulator. The line represents the simulation result due to the strain altered valence-band splitting only.

tunneling model in our previous work [6] can be applied, in which the hole direct tunneling current per unit area reads as

$$J_h = \sum_i \sum_j q f(j,i) N(j,i) P_t\left(E(j,i)\right) \tag{3}$$

where $f(j,i)$ is the hole impact frequency on the Si/SiO_2 interface and equals $(qF_s/2)(2m_{zhi}E(j,i))^{-1/2}$, where ε_{si} is the silicon permittivity, and $P_t(E(j,i))$ is the hole transmission probability across the SiO_2 film. The hole effective mass in oxide m^*_{ox} can play a critical role in determining the transmission probability $P_t(E(j,i))$.

Therefore, by incorporating both the conduction-band deformation potential (see [7] for the complete formulas, which were also cited in our previous work dedicated to the electron direct tunneling [8], [9]) and the valence-band $k \bullet p$ calculation results into the triangular-potential-based hole direct tunneling simulator [6], the strain-altered hole gate current is able to be readily quantified. The validity of the presented quantum strain simulator can be examined using three different aspects. First, a fairly good agreement with the measured gate current versus gate voltage characteristics was created in a wide range of four decades, as demonstrated in Fig. 4 for $\sigma = 0$. This means that the simulator is reliable for the gate voltage more negative than -0.2 V. The same argument holds for the nonzero stress. Second, the hole effective mass in the oxide m^*_{ox} is exactly equal to the literature value (0.32 m_o) [10]. This also is the case for the hole out-of-plane effective masses in the inversion layer as mentioned above. Finally, with the fixed gate oxide thickness, the simulated hole gate direct tunneling current change at $V_G = -1$ V due to the strain-altered valence-band splitting was found to be close to those measured under the *externally* applied compressive stress [1], [2], as depicted in Fig. 8. Therefore, the validity of the quantum strain simulator is confirmed.

IV. Physical Origin and Discussion

To find out the plausible physical mechanisms that account for the hole gate current enhancement, we employed the quantum strain simulator verified above through the changes in the process parameters. First, with polysilicon doping concentration N_{poly} and substrate doping concentration N_{sub} both fixed at their nominal values, the simulated gate current change percentage is given in Fig. 9(a) versus gate voltage with the gate oxide thickness t_{ox} as a parameter. The corresponding fractional gate current change remains constant in a wide range of the gate voltage, regardless of t_{ox}. This means that the same flat characteristics as those experimentally encountered over the gate voltage can be reached as long as the appropriate gate oxide thickness has been determined. Second, to reflect the stress effect on impurity diffusion [9], [11]–[13], additional simulations were conducted for varying N_{poly} or N_{sub}. The

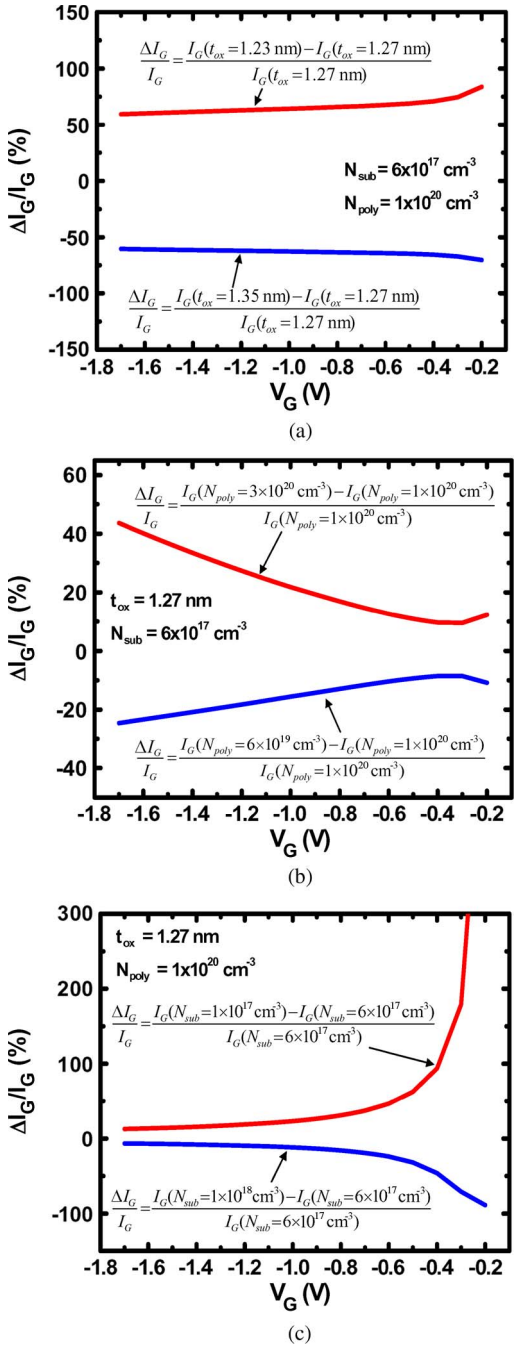

Fig. 9. Simulated gate current change versus gate voltage for (a) different gate oxide thicknesses, (b) different poly gate doping concentrations, and (c) different substrate doping concentrations. The formulas used are inserted.

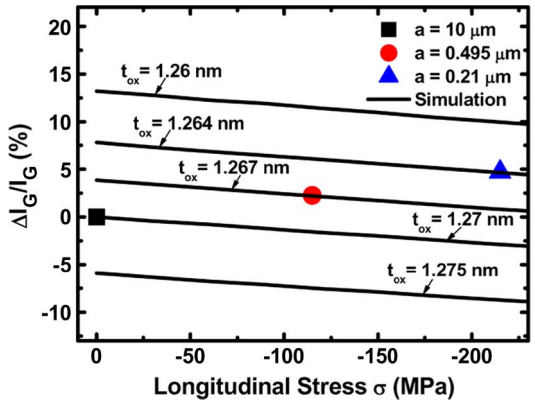

Fig. 10. Simulated gate current change versus stress for several oxide thickness with respect to the gate current of $\sigma = 0$ case (i.e., $t_{\rm ox} = 1.27$ nm). Both the polysilicon doping concentration and substrate doping concentration are kept at the nominal values. Also shown for comparison are the experimental data (symbols) corresponding to the inset of Fig. 4.

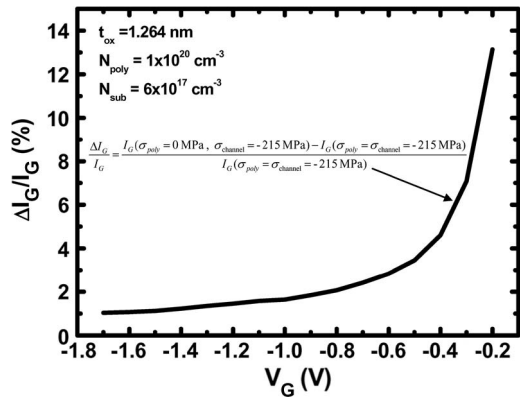

Fig. 11. Simulated gate current change of zero poly stress with respect to a poly stress of -215 MPa as a function of gate voltage for a channel stress of -215 MPa. The formulas used are inserted.

results are given in Fig. 9(b) and (c). The gate current change presented in Fig. 9(b) corresponds to two different values of $N_{\rm poly}$ under fixed $t_{\rm ox}$ and $N_{\rm sub}$, clearly revealing a profoundly significant deviation for more negatively biased gate voltages. Such a huge deviation also appears in Fig. 9(c) for two different values of $N_{\rm sub}$ under fixed $t_{\rm ox}$ and $N_{\rm poly}$, which occurs instead in the direction of less negative gate voltage. Therefore, the stress-induced dopant redistribution is unlikely to serve as the responsible mechanism. Furthermore, the remaining possible factors were considerably ruled out: 1) the channel area change due to source/drain extension diffusion retardation [9], [13] is insignificant $(\sim 10^{-3})$ and 2) the trap-assisted tunneling as the dominant mechanism is impossible because of less correlation with the mobility data in Fig. 2; specifically, the mobility change at -215 MPa stress is about three times the gate current change.

The analyses above suggest the reduction in the physical gate oxide thickness over the whole gate area as the principal factor in producing the gate current enhancement. Thus, the quantum strain simulation was further carried out for different gate oxide thicknesses with other process parameters kept unchanged. The results are plotted in Fig. 10 versus stress along with the data for comparison. The underlying gate oxide thickness can be straightforwardly obtained with an accuracy of 0.001 nm: $t_{\rm ox} = 1.267$ and 1.264 nm for -120 and -215 MPa stress, respectively. The extracted gate oxide thickness reduction is around 0.003 and 0.006 nm for -120 and -215 MPa stress, respectively. Again, the gate current change for $t_{\rm ox} = 1.264$ nm and $\sigma = -215$ MPa was simulated with respect to the nominal case ($t_{\rm ox} = 1.27$ nm and $\sigma = 0$ MPa). The results are given in Fig. 5. Here, it can be seen that good agreements with the data are created for a wide range of gate voltage down to -0.2 V, achieved without adjusting any parameters.

At this point, it is interesting to make a comparison with the existing thermal oxidation experiment on a bending silicon wafer [14], [15]. In one of the citations [14], an externally applied mechanical stress of -100 MPa was shown to have no noticeable effect on the thickness of the formed oxide (800 °C dry O_2 100% oxidation), particularly in a certain range down to 2 nm thick, which is comparable with the gate oxide thickness used in this work. In [15], the effect of the external compressive mechanical stress was also shown to be insignificant as well, valid with an accuracy of 0.5 nm. However, with the combination of both the quantum strain simulator and the hole direct tunneling data as done in this work, we reached the gate oxide thickness with the greatly improved precision down to 0.001 nm. Indeed, it is difficult for current capacitance measurements to deliver such a precision of 0.001 nm or 0.08% in gate oxide thickness variation. As widely recognized, however, in the direct tunneling regime the gate current is highly sensitive to the change in the gate oxide thickness. This means that the gate direct tunneling current may serve as an ultra-precision detector of the oxide thickness. However, care must be taken in this direction. This explains the importance of a quantum simulator, as demonstrated in this paper.

Additionally, the inset of Fig. 4 clearly points out that the standard deviation of the gate current is comparable between different gate-to-STI spacing values. This dictates that the spatial fluctuation in the gate oxide thickness is caused by the random process during the thermal oxidation, regardless of the stress. Only the average of the gate current steadily increases with the stress. This means that applying a compressive stress may retard the oxidation rate and, thus, give rise to a reduction in the physical gate oxide thickness. On the other hand, the presented change of up to 0.47% in the gate oxide thickness is larger than that caused by the Poisson's ratio (0.03%) [1]. This means that the strain-retarded gate oxidation rate may dominate over the strain-altered valence-band splitting counterpart. As a result, the currently recognized trend [1], [2] that the hole gate direct tunneling current decreases with the compressive stress is significantly reversed, as clearly demonstrated in this paper.

Finally, the simulator was, again, carried out to examine the effect of the poly stress. The resulting gate current change of zero poly stress with respect to poly stress of -215 MPa is plotted in Fig. 11 as a function of gate voltage for channel stress of -215 MPa. It can be seen in the figure that significant discrepancies occur, particularly for less negative gate voltage. Thus, this new deviation, as well as its striking trend, can provide the extra evidence to support the aforementioned hypothesis that the poly stress is close to the channel stress. On the other hand, modeling the gate current through a

metal-gate/high-k/interfacial SiO_2/p-type inversion layer/n-type silicon system remains to be a challenging issue. It can be expected for the presented simulator to find applications in this metal-gate high-k gate stack case. To achieve the goal, some suggestions are given. First, the subband energy calculation by the triangular potential approximation in the presence of the stress can be directly applied to the p-type inversion layer. The corresponding energy band diagram as shown in Fig. 6 can be retained, but with the poly side removed. The remaining energy band part corresponding to the metal-gate and high-k dielectrics may be roughly constructed from the electrostatics aspects in terms of the capacitance, the inversion charge density, and the threshold voltage. Refining of the overall band diagram may be achieved through the fitting of the gate current. At this point, the tunneling model used in this work must be modified substantially. Specifically, the tunneling involved with the traps might dominate the overall gate current in metal-gate/high-k devices due to the thicker insulator and the higher trap density within the insulator of the metal-gate/high-k devices. Multilayer tunneling and/or hopping mechanisms may be significant as well.

V. Conclusion

The measured hole gate direct tunneling current on a nominal 1.27-nm gate oxide p-MOSFET has exhibited an increasing trend with STI compressive stress, which is exactly contrary to that of the externally applied compressive stress. To resolve this contradicting issue, a quantum strain simulator has been established. The validity of the simulator has been examined in detail. The combination of the verified simulator and the experimental data has systematically led to the finding of the origin: a reduction in the apparent physical gate oxide thickness over the whole gate area, with an accuracy of 0.001 nm, occurs under the influence of the STI compressive stress. A linkage to the mechanical-stress-dependent thermal oxidation experiment in the open literature has been constructed. The extracted gate oxide reduction in this work has been shown to be able to significantly enhance the hole direct tunneling current and, consequently, reverse the conventional trend with the stress. Some suggestions have also been given concerning the application of the simulator in the metal-gate/high-k devices.

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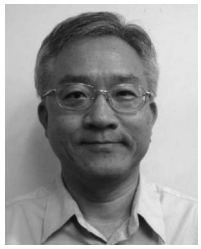

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