Statistical Metrology of Metal Nanocrystal Memories With 3-D Finite-Element Analysis

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***Abstract*—We study the parametrical yield of memory windows for the metal nanocrystal (NC) Flash memories with consideration of the 3-D electrostatics and channel percolation effects. Monte Carlo parametrical variation that accounts for the number and size fluctuations in NCs as well as channel length is used to determine the threshold voltage distribution and bit error rate for gate length scaling to 20 nm. Devices with nanowire-based channels are compared with planar devices having the same gate stack structure. Scalability prediction by 1-D analysis is found to be very different from 3-D modeling due to underestimation of effective NC coverage and failure to consider the 3-D nature of the channel percolation effect.**

***Index Terms*—Nanocrystal (NC), nonvolatile memories, programming window distribution, 3-D electrostatics.**

I. Introduction

DUE to the scaling limit of gate length and tunneling oxide thickness, it is difficult for conventional floating gate memories to achieve required retention and interference characteristics while maintaining low-voltage program/erase (P/E) operations [1]. To overcome this inherent design limitation, nanocrystal (NC) [2] memory is considered as one of the promising candidates that enable reduced intercell floating gate coupling, tolerance to local dielectric defect, low P/E voltage, fast P/E speed, and compatibility with current CMOS technology [3]–[7]. In particular, metal NC memories can potentially push further scaling due to large density of states, inherent field enhancement, selectable work function, and tunneling asymmetry between P/E and retention [5], [7]. Furthermore, Coulomb blockade energy can be reduced by replacing the insulating layer in the gate stack by a high-κ dielectric, which also leads to an increase in channel–NC coupling due to the field enhancement effect [6], [8].

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Fluctuation in memory window due to NC size/density/registry variations and gate length is one of the main concerns for scalability [9], [10]. The goal of this paper is to illustrate the importance of the 3-D electrostatics and channel percolation effects that are not considered in previous Monte Carlo (MC) statistical metrology of NC memories [9]–[15]. The new model can be used for more accurate scaling prediction. We perform the MC parametrical analysis, with inner loops by the finite-element (FE) solver in COMSOL to predict the threshold voltage ($V_{\rm th}$) variations and corresponding bit error rate (BER). Furthermore, nanowire (NW)-based memories with sub-10-nm Si-channel widths have been proposed to obtain large $V_{\rm th}$ shifts and longer charge retention times by the bottleneck and quantum confinement effects [16]. Metal NC memory with NW [17] channel is studied in comparison with the planar device for $\Delta V_{\rm th}$ variation analysis. Simulation results indicate that the high percentage of erratic bits will still be one of the main concerns for NW devices with sub-30-nm gate lengths due to NC number density variation. Previously, it has been shown that preferential self-alignment (SA) of NC to the carbon nanotube (CNT) can be achieved [18]. Preferential growth of NC near the channel can offer an effective solution to NC density variation.

II. Device Modeling and Assumptions

Schematics and a sample mesh of the simulated planar and NW devices [17] are shown in Figs. 1 and 2, respectively. Our model assumes a p-type silicon substrate with 10^{17} cm^{-3} doping. For planar devices, a halo-doping profile is added to control short-channel effects (SCEs), and the channel width is fixed at 20 nm. Spherical NCs are embedded in a gate stack with 18 nm HfO_2 control oxide and a heterogeneous tunnel dielectric of 2 nm HfO_2 and 1 nm SiO_2 [8]. The NC diameter is 6.1 $\pm$ 1.2 nm, and the average number density is 5.0×10^{11} cm^{-2} with percentage fluctuations of 51% and 34% for 20 and 30 nm channel lengths, respectively, following the experimental distribution from unconstrained self assembly in a gate-first process [19]. Gaussian variations of NC size and channel length, Poisson variations of NC number density, and uniform variation on NC registry have been included in the MC simulation, with statistics extracted from the experiments [17]–[20]. The NW device is 3 nm in diameter [17] and has the same gate stack structure, doping level (but without halo), and source/drain structures as the planar device for direct comparison. All simulation cases assume an electrostatic environment, where the NCs either remain charged with five electrons or uncharged,

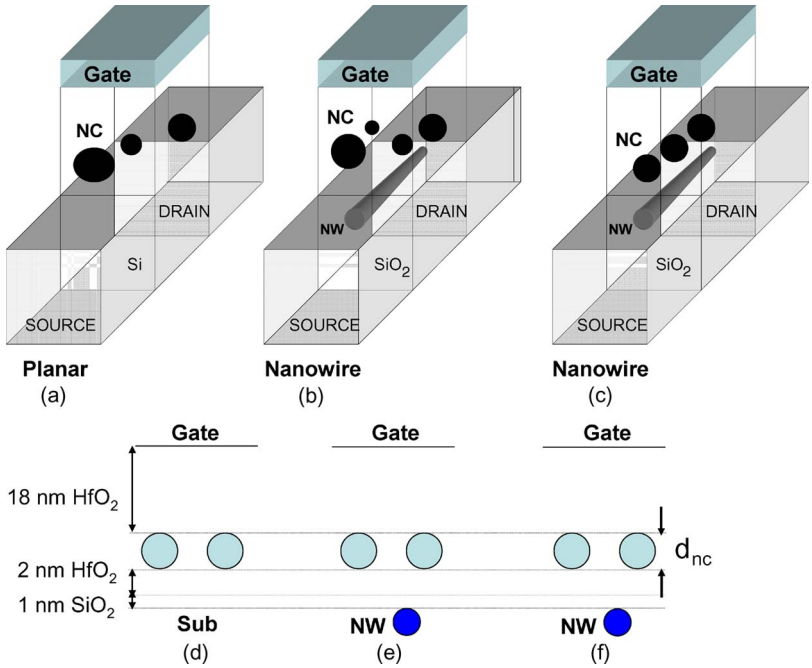

Fig. 1. Schematic of metal NC Flash memory with (a) a planar channel, (b) an NW channel, and (c) an NW channel with self-aligned NCs. For the SA case, each NC is centered at locations on top of the channel region. The corresponding cross-sectional views are shown in (d), (e), and (f), respectively. Simulation parameters of the structure: NC diameter $d_{\rm nc}$: 6.1 nm; NW diameter: 3 nm; average NC density: 5.0×10^{11} cm^{-2}; tunneling oxide: 2 nm HfO_2 on top of 1 nm SiO_2; and control oxide: 18 nm HfO_2.

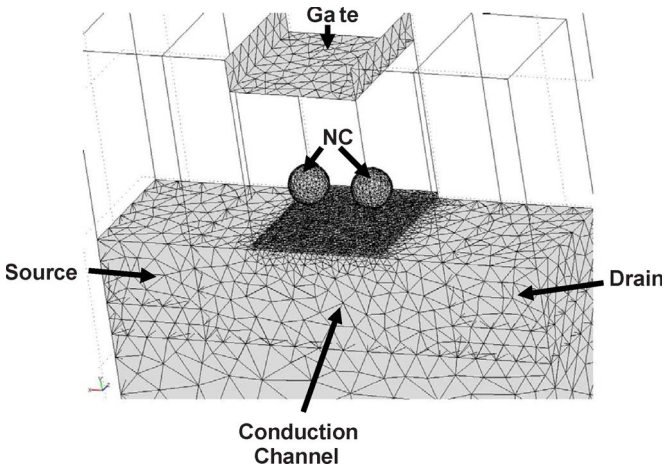

Fig. 2. Sample mesh of the planar device with 20 nm gate length in the COMSOL FE solver.

for calculating the control gate characteristics, unless stated otherwise. Our FE model consists of 3-D Poisson and modified drift-diffusion formalisms, implemented by COMSOL [21]. It does not include detailed quantum transport effects that can enhance the accuracy for sub-90-nm above-$V_{\rm th}$ currents [22]. We also ignore quantum confinement and band-splitting effects, which may be important in NW devices [23], [24]. The classical transport is used to maintain acceptable computational efficiency in the statistical metrology of 3-D geometrical design, where total computation can be accomplished in several weeks on a 64-bit central processing unit 8-GB memory platform. For $\Delta V_{\rm th}$ fluctuation prediction, our simulation model should be acceptable since 3-D electrostatics and channel percolation below $V_{\rm th}$ are self-consistently considered. We define BER as the probability of a programmed bit with an offset in $V_{\rm th}$ that falls below the nominal "0" state plus a fixed voltage $V_{\rm tol}$, which is determined by the sense amplifier tolerance. Table I shows the simulated Gaussian fitted mean threshold voltage shift $\mu(\Delta V_{\rm th})$ and standard deviation $\sigma(\Delta V_{\rm th})$ for various device structures.

III. Results and Discussion

A. Fringing Field Effect and Comparison With 1-D Analytical Model

To have a qualitative understanding on $V_{\rm th}$ fluctuation to account for 3-D electrostatics, we can describe the nominal memory window $\Delta V_{\rm th}$ in a semiempirical model as [9], [20]

$$\Delta V_{\rm th} = R \cdot \frac{e \cdot N}{C} \tag{1}$$

where e is the elemental charge, R is a constant representing the relative strength of channel–NC coupling, C is the 3-D NC-to-control-gate coupling capacitance, and N is the number of electrons stored in each NC. The nominal memory window $\Delta V_{\rm th}$ as well as $V_{\rm th}$ fluctuations increases with increasing R through effective NC coverage over the channel. Clearly, the charge in an NC perturbs the channel potential on a larger coverage area than the NC cross-sectional area due to the fringing effect [20]. As shown in Fig. 3, $\Delta V_{\rm th}$ estimated by the 3-D MC FE solver is significantly greater than the cases where the coverage area is assumed to be the NC cross-sectional area in semi-1-D models. Good agreement can be obtained between the 3-D model [20] and the MC FE solver for $\Delta V_{\rm th}$ versus the number charges stored in each NC. Due to the discrete nature

TABLE I
GAUSSIAN-FITTED MEAN THRESHOLD VOLTAGE SHIFT $\mu(\Delta V_{\rm th})$, STANDARD DEVIATION $\sigma(\Delta V_{\rm th})$, AND BER WITH $V_{\rm tol} = 0.1$ V. FC CASES REFER TO THE CASES WHERE ALL NCs HAVE FIVE ELECTRONS STORED. PC CASES REFER TO THE CASES WHERE ONLY NCs CENTERED ON TOP OF THE CHANNEL REGION ARE CHARGED. SA CASES REFER TO THE CASES WHERE THE NCs ARE SELF-ALIGNED ON THE CNT BY SURFACE ENERGY PREFERENCE

Device	Channel Type	Gate Length (nm)	Diameter/ Width (nm)	$\mu(\Delta Vth)$ (V)	$\sigma(\Delta Vth)$ (V)	BER V_{tol} = 0.1 V
A	Planar	20	20	0.50	0.27	3.85×10^{-2}
B	Planar	30	20	0.47	0.19	1.92×10^{-2}
C	Nanowire, FC	20	3	0.53	0.28	3.41×10^{-2}
D	Nanowire, FC	20	7	0.41	0.26	6.65×10^{-2}
E	Nanowire, FC	30	3	0.65	0.21	3.4×10^{-3}
F	Nanowire, FC	30	7	0.53	0.23	3.15×10^{-2}
G	Nanowire, PC	20	3	0.16	0.29	1.87×10^{-1}
H	Nanowire, PC	20	7	0.17	0.33	1.64×10^{-1}
I	Nanowire, PC	30	3	0.24	0.26	1.42×10^{-1}
J	Nanowire, PC	30	7	0.34	0.21	7.54×10^{-2}
K	Nanowire, SA	20	3	0.32	0.11	2.27×10^{-2}
L	Nanowire, SA	30	3	0.53	0.10	1.52×10^{-6}

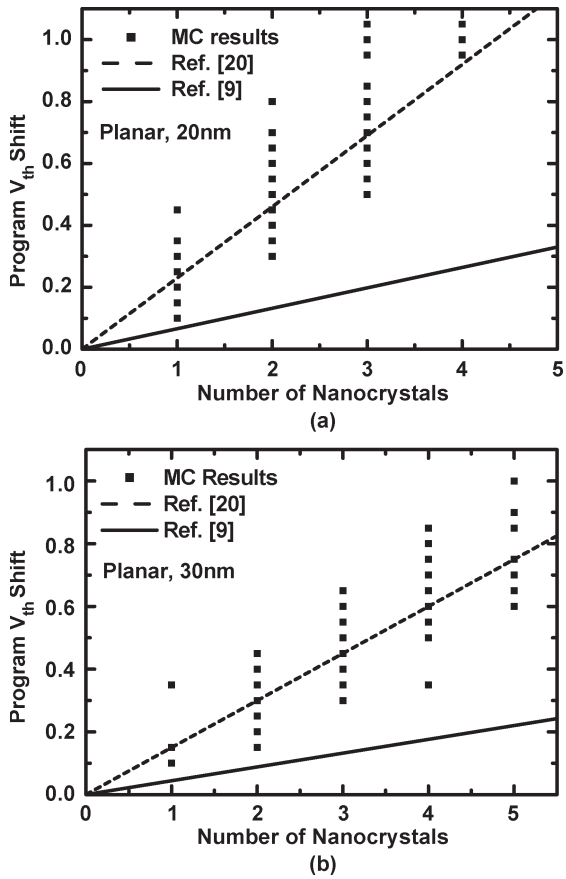

Fig. 3. Threshold voltage shift after programming versus the number of NCs within each planar device with (a) 20 nm and (b) 30 nm gate lengths. Five electrons are stored in each NC. Semi-1-D analytical model assumes that the coverage area is equal to the NC's cross-sectional area, whereas 3-D model incorporates the fringing field enhancement effect on channel–NC coupling. One hundred cases were simulated for each scenario.

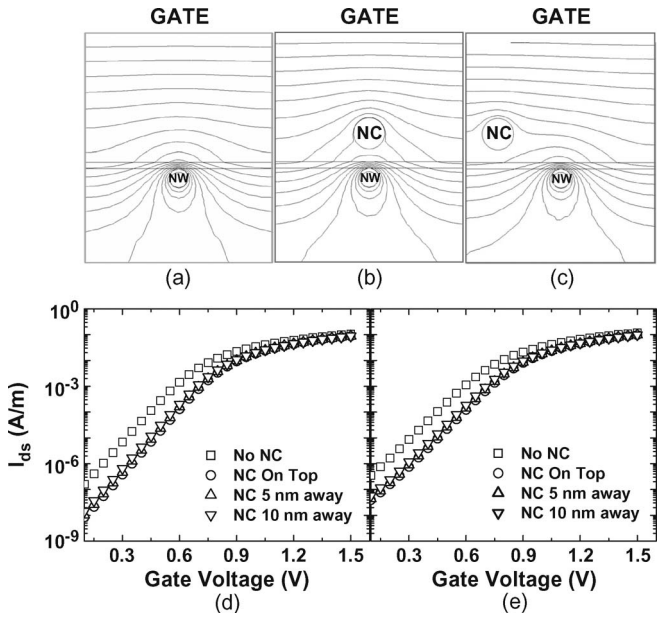

Fig. 4. Cross-sectional view of the 3-D electrostatic potential contours of the NW devices with (a) no NC, (b) one NC centered on top of the NW, and (c) one NC centered 10 nm away from the NW. Five electrons are stored in each NC. $V_G = 2$ V, and the contour spacing is 90 mV. Also shown are the corresponding I–V curves of (d) 3-nm-diameter and (e) 7-nm-diameter NW devices with no NC, one NC centered directly on top of the NW, and one NC centered either 5 or 10 nm away from the NW.

of NC array and the spherical shape of NC, $\Delta V_{\rm th}$ and $V_{\rm th}$ fluctuation prediction must be calculated rigorously considering the entire 3-D potential profile in the channel.

Fig. 4 shows the potential contours of an NW device with NC located directly on top and away from the channel, where the channel potentials are affected by the NC fringing fields and the corresponding I–V curves for NW devices with diameters of 3 and 7 nm. We have found minute fluctuation in $\Delta V_{\rm th}$ from NC registry variation in planar or NW devices, which suggests an enhanced channel–NC coupling dominated by the fringing field effect. However, the NC registry can affect the charging state during the P/E operations in the NW device since the tunneling length, and hence, the program current can be very different. We consider two asymptotic scenarios: 1) full coverage (FC),

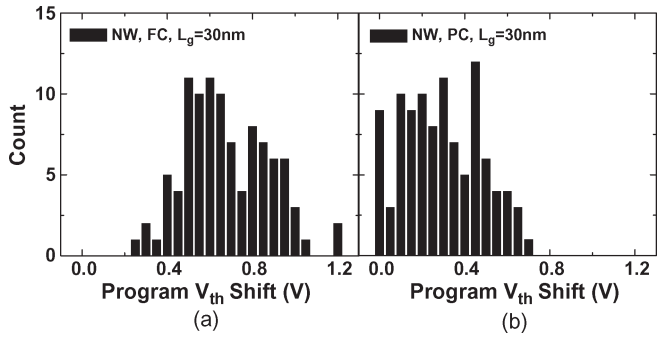

Fig. 5. MC simulation results showing the $\Delta V_{\rm th}$ distribution of the scenarios where (a) all the NCs within the gate area are charged (FC) or (b) only the NCs that overlap with the channel region are charged (PC). The NW is 3 nm in diameter and 30 nm in gate length. Five electrons are stored in each NC. One hundred cases were simulated for each scenario.

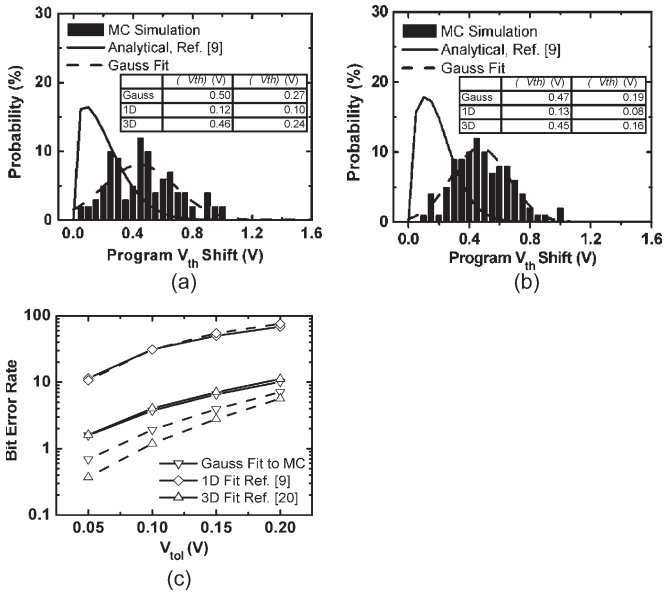

Fig. 6. $\Delta V_{\rm th}$ distribution probability density curves for planar devices with (a) 20 nm and (b) 30 nm gate lengths. Gaussian-fitted and semi-1-D analytical models are also shown. The inset is a table comparing $\mu(\Delta V_{\rm th})$ and $\sigma(\Delta V_{\rm th})$ estimated by semi-1-D, full 3-D electrostatic, and Gaussian-fitted models. Plot (c) compares the corresponding BERs calculated from the three models versus $V_{\rm tol}$. The solid lines represent the 20-nm device, and the dashed lines represent the 30-nm device.

where every NC in the gate stack is uniformly charged, and 2) partial coverage (PC), where only NCs overlapping the NW channel are charged. Fig. 5 compares $\Delta V_{\rm th}$ distribution plots for the PC and FC configurations. The design combination of planar and NW devices is summarized in Table I. Due to the fringing fields coming from NCs that do not overlap with the NW, devices A and D show larger $\Delta V_{\rm th}$ and slightly tighter distribution than devices G and I.

In either the 1-D [9] or 3-D [20] analytical models, the mean threshold voltage shift $\mu(\Delta V_{\rm th})$ and the standard deviation $\sigma(\Delta V_{\rm th})$ can be approximated by

$$\mu(\Delta V_{\rm th}) = R \cdot \frac{e \cdot N}{C} \cdot \overline{N_{\rm td}} \tag{2}$$

$$\sigma(\Delta V_{\rm th}) = \mu \Delta {\rm V_{th}} \cdot \sqrt{\frac{\sigma^2 N_{\rm td}}{\overline{N_{\rm td}}^2} + \frac{1}{\overline{N_{\rm td}}} \cdot \frac{(\sigma(R))^2}{\overline{R^2}^2}} \tag{3}$$

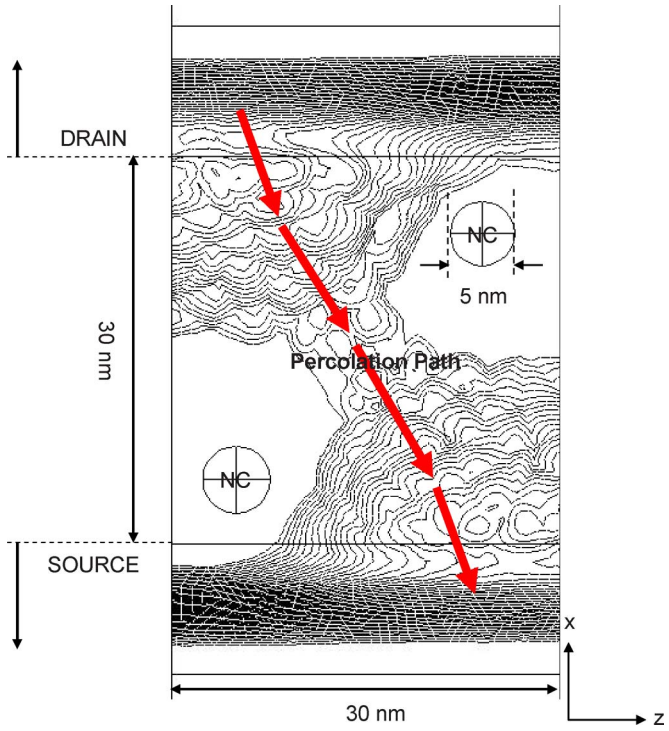

Fig. 7. Contour plot of electron density for a 30 × 30 nm planar device. Each NC is charged with one electron. Electrons in the channel are screened by the NC, and the dominant percolation path of the channel leakage current is highlighted.

where $\overline{N_{\rm td}}$ is the average number of NCs, and $\sigma(R)$ is the standard deviation of substrate–NC coupling factor. Fig. 6 compares $\mu(\Delta V_{\rm th})$, $\mu(\Delta {\rm V_{th}})$, and BER as a function of gate length for the analytical models by (2) and (3) [9], [20] and Gaussian-fitted MC simulation. It has been shown that R is a relative weak function of NC diameter when the channel coupling is adequate [20]. Since Gaussian-fitted parameters agree well with the 3-D analytical model, the variation in $\Delta V_{\rm th}$ is mainly determined by density fluctuation according to (3). However, previous semi-1-D models [9]–[15] excluding 3-D fringing and channel percolation underestimated NC coverage, resulting in severe parametric distribution distortion.

B. Impact of Gate Length and NW Diameter

The channel percolation effect of the planar structure is illustrated in Fig. 7. Typically, the percolation effect is enhanced with increasing channel W/L ratio, resulting in more severe $\Delta V_{\rm th}$ fluctuations [11]. Fig. 8 shows the percentage increase in BER for various device structures by scaling down the effective gate length from 30 to 20 nm. For gate length scaling with a fixed channel width, the number of percolation paths available increases, and a higher BER is observed. As the diameter of NCs becomes larger than the diameter of NW devices, channel–NC coupling is enhanced, and the number of percolation path vanishes in comparison with planar devices. Devices with a larger NW diameter (B and E) have a BER larger than those of the smaller ones (A and D) in FC charging as shown in Table I, dominated by the fringing field effect. In

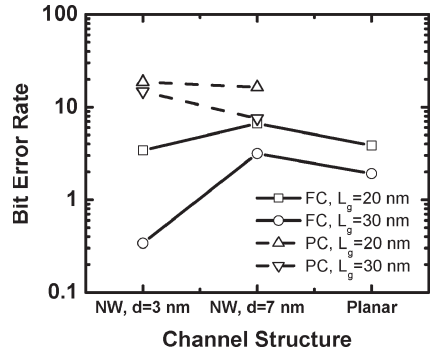

Fig. 8. BER comparison between planar and NW channels with 20 and 30 nm gate lengths. BER calculated with the following two additional constraints are also shown for illustration: 1) all NCs within the gate region (FC) or 2) only NCs that are centered within the channel area (PC) have five electrons stored.

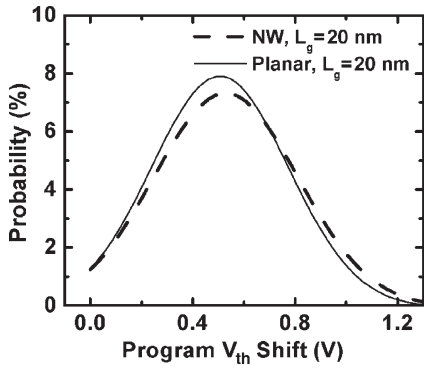

Fig. 10. Gaussian-fitted curves to the $\Delta V_{\rm th}$ distribution estimated by the MC method for the (solid lines) planar and (dash lines) 3-nm NW devices. Gate length is 20 nm, and all NCs within the gate area have five electrons stored.

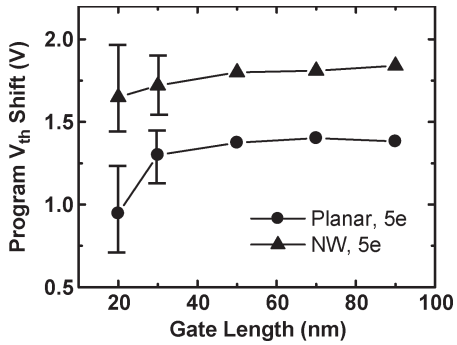

Fig. 9. $V_{\rm th}$ roll-off behavior with statistical error bars for the 3-nm-diameter NW and planar devices. Each NC is charged with five electrons. NCs are orthogonally aligned with a fixed inter-NC distance of 10 nm and an NC diameter of 5 nm.

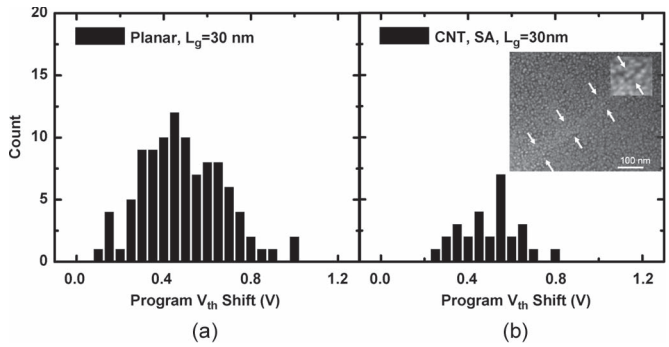

Fig. 11. MC simulation results of (a) planar (100 cases) and (b) 3-nm-diameter self-aligned NW devices (25 cases). Gate length is set at 30 nm. Inset shows an SEM image of self-aligned NC to carbon nanotubes, where NCs are concentrated near the channel area.

contrast, devices I and J with PC charging show a decreasing BER with increasing NW diameter due to $\Delta V_{\rm th}$ sensitivity to NC density variation when NCs away from the channel are not charged and do not exert additional fringing fields.

C. Templated Assembly of NC

NC placement can be regulated by polymer [25] or protein [26] lattice, and hence, the NC size and position variation becomes negligible. However, the number density and vertical alignment with NW devices will still contribute to $\Delta V_{\rm th}$ variations. Fig. 9 shows the $V_{\rm th}$ roll-off behavior and statistical error bars for an array of NCs orthogonally aligned with a fixed inter-NC distance of 10 nm and an NC diameter of 5 nm. NW devices have superior control on the SCE, even in sub-30-nm devices and larger $\Delta V_{\rm th}$ for the same number of electrons stored in each NC, but we observe NW devices having similar $\Delta V_{\rm th}$ fluctuations as the planar devices. Originally, the bottleneck effect [16] with decreasing channel width in the NW device is expected to eliminate the percolation leakage effect and increase mean memory window as well as standard deviation. However, if we consider 3-D fringing, $\Delta V_{\rm th}$ fluctuation should be less severe in the NW device in comparison with previous semi-1-D models [9], [16]. As illustrated in Fig. 10, planar and 3-nm NW devices can have similar $\Delta V_{\rm th}$ fluctuation. Although planar devices are less sensitive to NC number density variation, it lacks the channel–NC coupling enhancement effect in the NW devices.

D. SA of NC to NW or Nanotube Channels

Previous work has demonstrated that CNT devices can achieve SA of NC to the CNT [18] by surface energy preference. Fig. 11 compares planar to self-aligned NW devices with an average number density of 10^{12} cm^{-2} near the channel area. With the NC diameter larger than that of the NW, NC–channel coupling is dominant due to the fringing field enhancement. Number density variation on $\Delta V_{\rm th}$ becomes less severe with increased density near the channel surface area. Thus, we observe higher $\mu(\Delta V_{\rm th})$ and smaller $\sigma(\Delta V_{\rm th})$, which suggests that self-aligned NW devices can be the device candidate to achieve a small BER.

IV. Conclusion

We have demonstrated the importance of including 3-D electrostatics and channel percolation in metal NC memory statistical metrology and examined BER in various channel structures for scaling prediction. Contrary to previous semi-1-D models, $\Delta V_{\rm th}$ fluctuation is mainly due to number density variation and is less sensitive to NC diameter variation within the range of 6.1 $\pm$ 1.2 nm. In addition, the field enhancement

effect from NCs away from the channel has noticeable effects on devices with small width/length ratios. NW devices benefit from the field enhancement and the bottleneck effect to achieve a higher threshold voltage shift, but with diminishing return as the gate area is scaled down even with templated NC placement. SA of NC to NW shows strong promise in both increasing memory windows and controlling $\Delta V_{\rm th}$ fluctuation.

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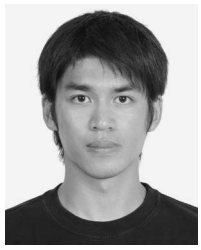

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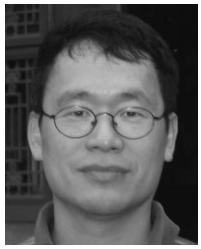

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