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Trend transformation of drain-current degradation under drain-avalanche hot-carrier stress for CLC n-TFTs

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ABSTRACT

Continuous-wave green laser-crystallized (CLC) single-grain-like polycrystalline silicon n-channel thin-film transistors (poly-Si n-TFTs) demonstrate the higher electron mobility and turn-on current than excimer laser annealing (ELA) poly-Si n-TFTs. Furthermore, high drain voltage accelerates the flowing electrons in n-type channel, and hence the hot-carriers possibly cause a serious damage near the drain region and deteriorate the source/drain (S/D) current. In this study, at high drain stress voltage, it appears that CLC TFT was degraded in the initial stress time (before 50 s), but the drain current was enhanced after 50 s. After 50 s stress time, the amount of grain boundary trap states near the drain side was getting large and the reflowing holes damaged the source region or injected into gate oxide near source side as well.

1. Introduction

One of the cardinal constraints for scaling down TFT's dimensions is the device reliability. Degradation of TFTs can be caused by bias temperature stressing (BTS) [1], Fowler–Nordheim tunneling injection [2] and the hot-carrier stressing [3]. The hot-carrier stressing and Fowler–Nordheim tunneling can cause degradation both near the SiO_2/Si interface [4] and the grain boundary [5] and in the bulk of gate oxide [6]. In the recent stage, a mature and low-cost fabrication technology in liquid–crystal-display (LCD) panel is that the gate channel of TFT device is formed with amorphous silicon (a-Si) type. Comparing the driving current between a-Si TFT and low-temperature-poly-silicon (LTPS) TFT [7,8], the later exhibits higher electron-and-hole mobility characteristics. Moreover, LTPS TFT can be fabricated with self-alignment process and is similar to the process of metal–oxide-semiconductor field-effect transistor (MOSFET) [9,10]. Hence, the implemented integration of TFT drivers and TFT devices on glass substrate is possible to fabricate in one set of processes. Additionally, laser crystallization providing the local heating and avoiding the melting glass around 600 °C will be a key technology to improve the driving performance of TFT panel, due to the good annealing quality of TFT channel. In the meantime, a large size of LTPS TFT LCD is a trend in global market need. Thus, a higher driving speed of TFT device is strongly expected. Although an excimer laser system [11] possibly produces 100–500 nm grain size in gate channel, the interfaces of grain boundaries [12] are too dense, causing the carrier mobility decreases and the channel leakage increases. To solve these disadvantages, the continuous-wave laser crystallization technology [13–15] demonstrates excellent single-grain-like polycrystalline silicon thin film because of the low crystallization rate. Furthermore, CLC system is more efficient than excimer laser system in cost, and produces high reliability and high-performance characteristics of TFTs for the application of active matrix LCDs and system-on-panel (SOP) on optical glass or quartz substrate.

In this study, this CLC poly-Si TFT [16] demonstrates that excellent electron mobility, up to 530 $cm^2/V\,s^{-1}$, is greater than that with low-temperature poly-silicon fabrication technology. Although the gate dielectric with TEOS–SiO_2 [17] was deposited with 100 nm thickness by plasma-enhanced chemical vapor deposition (PECVD), the current-driving capability of CLC poly-Si n-TFT was sufficiently obtained instead of high-*k* gate dielectric [18]. Hence, the thick gate dielectric provides the good immunity against gate leakage current. Undoubtedly, while poly-Si n-TFT was stressed with drain-avalanche hot-carrier (DAHC) stress, interface states and defects near drain region, and electrons injecting into gate dielectric were obviously observed.

2. Experimental procedure

After substrate clean, the fabrication of devices started by depositing a buffer silicon-nitride layer and a thin buffer oxide

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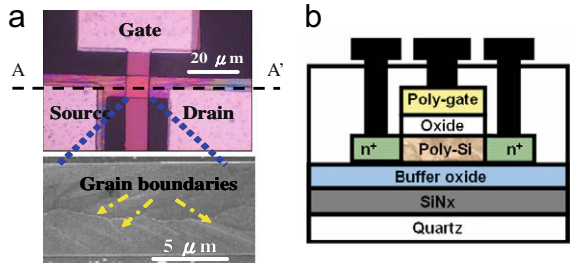

Fig. 1. Schematic profiles of (a) test-key pattern [16,19] and (b) A–A′ cross-sectional view of CLC poly-Si n-TFT structure with the bottom-floating configuration.

layer to capture the mobile ions and release the stack stress, respectively. Then, a 200 nm undoped amorphous Si layer at 550 °C in a low-pressure chemical-vapor-deposition (LPCVD) system on quartz substrate capped with a 100-nm thick TEOS oxide layer with plasma-enhanced chemical-vapor-deposition technology at 300 °C was deposited. The CLC poly-Si n-TFT device was then fabricated by a green laser annealing system, defining as continuous-wave laser crystallization, to produce a grain-like silicon channel. Finally, the active region of a TFT transistor was fabricated on the CLC poly-Si. The test-key pattern of CLC grain-like poly-Si n-TFT [16,19] is shown in Fig. 1a and b describes the A–A′ cross-section profile in Fig. 1a.

The steeper subthreshold swing (SS) presents the less traps in the grain [18]. After green laser crystallization, furnace annealing or green laser annealing can be accessed to activate the single-grain-like polycrystalline silicon thin film and dopant atoms. In some lecture [19], the process of green laser annealing to activate the impurity after implantation exhibited excellent electron mobility. Adopting a typical hot-carrier stress called drain-avalanche hot-carrier (DAHC) stress on CLC n-TFTs is a good metrology to verify the confident reliability of CLC TFTs. In this research, the thermal furnace activation in source/drain, and poly-gate implantation was accessed to firstly discuss the CLC poly-Si TFTs under DAHC stress. Before stress, Fig. 2 displays the great electrical characteristics of CLC poly-Si n-TFTs. The turn-on current (I_{ON}) is around 870 μA/μm at $V_{DS} = V_{GS} = 16$ V. The field-effect mobility (μ_{FE}) [20] is about 406 $cm^2/V\,s^{-1}$ at maximum trans-conductance for a width/length (W/L) = 25/15 (μm/μm) n-TFT device.

Table 1
The stress conditions of DAHC tests.

	DAHC-1	DAHC-2
Gate voltage (V)	7	9
Drain voltage (V)	14	18
Temperature (°C)	25 and 50	
Stress time (s)	0–3000	

3. Test results and discussion

The selected device was 25 μm at width and 15 μm at length, and the threshold voltage was about 1.75 V which was defined by maximum trans-conductance method (max Gm method) at $V_{DS} = 0.1$ V. For the DAHC stress conditions on CLC n-TFTs, the forced drain and gate voltages, and temperatures were shown in Table 1. In the meantime, the source terminal was grounded.

With regard to DAHC stress on conventional nMOSFETs, the stress condition is usually defined at the specified gate and drain voltages while the maximum substrate current appears. For a long channel-length device, the maximum substrate current will appear as the applied gate voltage is located at the half or one-third of forced drain voltage. In this study, the selected TFT device was a long channel-length device as 15 μm, so that the worst degradation of DAHC stress can be approximately employed when the forced gate voltage is equal to the half of the forced drain voltage. The characteristic curves of drain current and gate current with and without electrical stress involving room temperature and high temperature are presented in Fig. 3. The CLC poly-Si n-TFTs were dealt by DAHC-1 test and DAHC-2 test labeled in the Table 1.

For DAHC-1 and DAHC-2 stresses, the degradation in drain current is obviously observed, especially at high temperature, and a deterioration of gate current is found, too. In the meantime, the subthreshold swing (SS) is also degraded. The drain current at the saturation region is usually defined as [21,22]

$$I_{DS,sat.} = \frac{W}{2L}\mu_n C_{ox}(V_{GS} - V_{TH})^2 \quad (1)$$

where μ_n is the electron mobility, C_{ox} the gate dielectric capacitance, and V_{TH} is the threshold voltage.

Therefore, the degradation of drain current may be attributed to the degradation in electron mobility, gate dielectric capacitance, or threshold voltage (V_{TH}). In the worst case, all these three factors contribute the degradation for S/D current together. Before, at first, while temperature increases from 25 °C to 50 °C, the electron

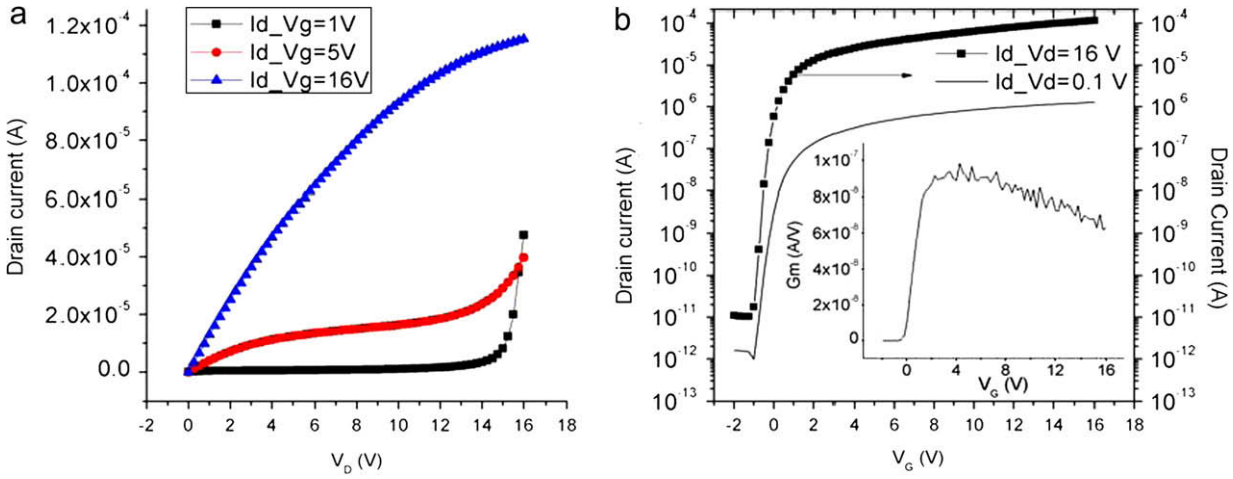

Fig. 2. Initial electrical characteristics of I_{DS} vs. V_{DS} and I_{DS} vs. V_{GS} for CLC poly-Si n-TFT.

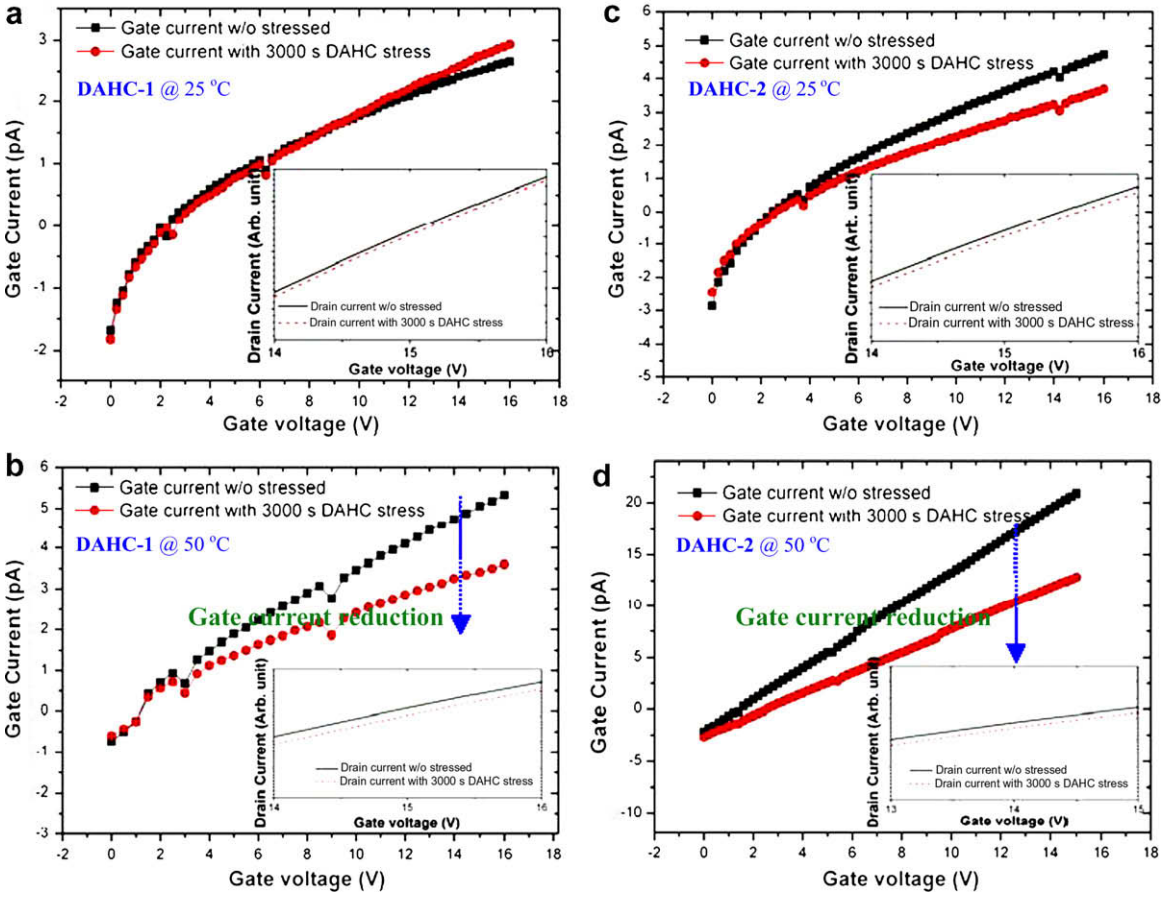

Fig. 3. Drain current and gate current with and without (w/o) DAHC stresses under temperature effect. The CLC poly-Si n-TFTs were processed with (a) DAHC-1 at 25 °C, (b) DAHC-1 at 50 °C, (c) DAHC-2 at 25 °C, and (d) DAHC-2 at 50 °C.

mobility reduces due to the lattice vibration, and hence the degradation of drain current is more obvious at high temperature than at room temperature, as shown in Fig. 3a–d. After DAHC stress, the oxide-trap charges, grain boundary traps, bulk grain traps and interface traps influenced the degradation of device performance. The electrons occupied the oxide trap forming negative trapped charges in the oxide layer. The negative trapped charges repelled the continuous jumping electrons that reduced the gate leakage current [23], presented in Fig. 3a–d. One model with connected equivalent resistance, as shown in Fig. 4, is suitable to interpret the reduction of gate leakage. The trapped charges, occupying the oxide trap and repelling the continuous jumping electrons, reduce the gate leakage current [23]. However, the gate capacitance integrity with PECVD TEOS-SiO_2 exhibited lower performance than that with thermal oxidation SiO_2. The resistance phenomenon was obviously observed. Therefore, the resistance model was considerably adopted and adequate to explain the gate current decrease after stress.

Additionally, the relationship between gate leakage and gate voltage with room temperature can be expressed as

$$I_{G,Total\_25\ ^\circ C} = A\ \ln(V_{GS}) - B \tag{2}$$

where A and B are constant and A extracted by linear regression is 1×10^{-12} for DAHC-1 at 25 °C, and 2×10^{-12} for DAHC-2 at 25 °C. Again, the value of B extracted by the same calculated method is 3×10^{-12} for DAHC-1 at 25 °C, and 4×10^{-12} for DAHC-2 at 25 °C. There are several physical mechanisms composing for gate current [20]. Referring Ref. [20], the gate current was theoretically attributed to $exp(E_i)$. However, in this work,

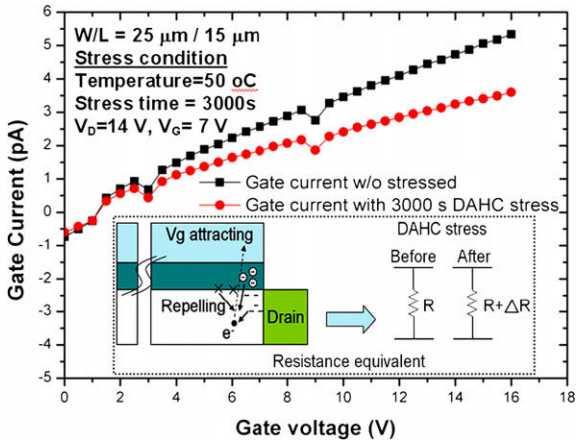

Fig. 4. Dependence of gate leakage of CLC poly-Si n-TFT w and w/o DAHC-1 stress. The inset plot demonstrates the reduction of gate current with an equivalent resistance model.

the proposed equation of gate current was related to $ln(V_{GS})$ due to the LPCVD TEOS oxide which contained a lot of oxide trapped states and easily provided the tunneling path. Thus, the gate current rapidly increased at the initial time, but gradually saturated at a long-term operation. At high temperature, the total gate current can be considered as liner dependence and represented as

$$I_{G,Total\_50\ ^\circ C} = CV_{GS} - D \tag{3}$$

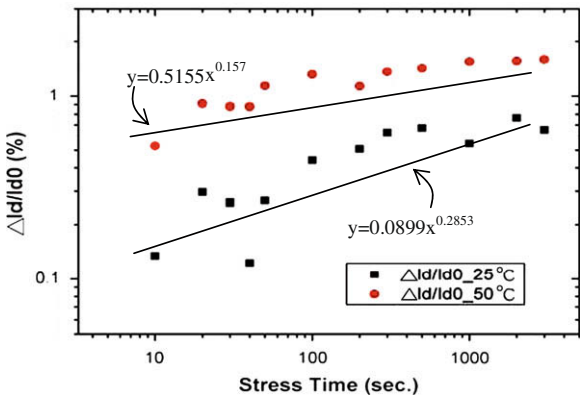

Fig. 5. Time history of $\triangle Id/Id_0$ degradation under DAHC-1 stress. An increased trend of drain-current degradation with either 25 °C or 50 °C was observed.

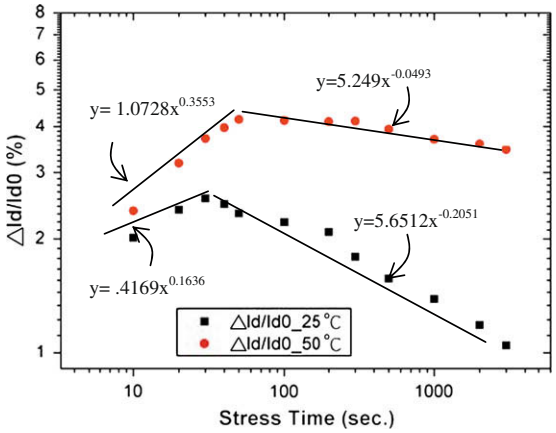

Fig. 7. Degradation of drain current $\triangle Id/Id_0$ vs. stress time under DAHC-2 high-field stress. A turning point is observed with either 25 °C or 50 °C before and after 50 s of stress time.

where the values of C and D for DAHC-1 and DAHC-2 stresses at 50 °C extracted by linear regression are 2×10^{-13} and 3×10^{-13} with DAHC-1, and 3×10^{-13} and 2×10^{-12} with DAHC-2, respectively.

From Eqs. (2) and (3), we find while temperature has been involved, the total gate leakage current exhibits a non-linear distribution, especially in low vertical electrical field (low V_{GS}). Furthermore, the degradation of drain current after DAHC-1 or DAHC-2 stress can be simply correlated to $I_{G,Total}$ with different temperatures by

$$I_{D,\,degradation} \propto -I_{G,Total\_Temperature} \tag{4}$$

When the difference of total gate current increases, based on Eq. (4), a serious degradation of drain current can be measured. The degradation of drain current under DAHC-1 with the increase in stress time is attributed to the generation in grain boundary trap states and interface trap states, as shown in Fig. 5. The power law numbers at room temperature and high temperature are 0.157 and 0.285, respectively. While the TFT device was stressed with DAHC-2 condition, the forced gate and drain voltages were increased so that some holes injecting into gate oxide and the other reflowing to source terminal were occurred. The schematic diagram of hole-injection and oxide damage with hole flow is displayed in Fig. 6. The threshold voltage shift in this work, because of the poly-Si channel, is not chiefly evident to realize the hole-injection at the source side. Using gate-to-source capacitance vs. gate voltage (C_{GS}–V_{GS} curve) could be better to illustrate the hole-injection mechanism, shown in Fig. 7.

In addition to the TFT device stressed by DAHC-1, the device under DAHC-2 stress appears the amount of interface trap states and grain boundary trap states was larger than that with DAHC-1 stress. The grain boundary trap states were possibly generated from the broken bonds of Si–H. However, there are a large number of grain boundaries in the channel [24], and hence the contribution

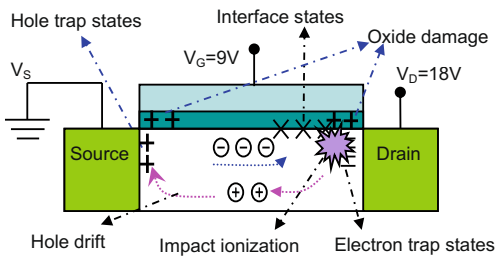

Fig. 6. Schematic cross-section of drain-current degradation under DAHC-2 stress. Two possible flow paths of hole carriers are pointed out.

of interface states in degradation of electrical characteristics was acceptably ignored. Furthermore, the hole carriers injecting into gate oxide caused an increase in inversion charges at the channel. At this meantime, the electrical field near the drain region was so high that the dangling bonds formed by Si–H bond hardly capture the flowing electrons. Thus, the generated holes not only inject into the gate oxide, but reflow from the drain side to source terminal as well. Finally, at low stress time, the interface trap states and grain boundary trap states near the drain side were dominated. After 50 s stress time, the amount of grain boundary trap states near the drain side was getting large and the reflowing holes damaged the source region or injected into gate oxide near source side as well.

4. Conclusions

A comprehensive investigation of the DAHC reliability mechanism of high-performance CLC n-TFT is reported for the first time. Various stress conditions, including electrical fields and temperature impact, are performed to differentiate the degradation mechanisms. For the low-field stress (DAHC-1) plus temperature effect, it is found that degradation of drain current showing the increase trend is due to impact ionization at the drain site. Higher temperature provides more sufficient thermal energy to energize the moving electrons to gain more kinetic energy to impact the drain site, inducing the worse degradation. For the high-field stress (DAHC-2) with temperature contribution, the degradation of drain current after a short-term stress dramatically depicts a turning point and gets healing because of the attraction of high drain field. The captured electrons in boundary traps and interface states were released.

The study of DAHC effect on CLC poly-Si n-TFT device with temperature effect is necessary to be revealed that it impacts on TFT devices from different performance required not only in LCD monitor, but in system-on-panel consideration. Through this experiment, the degradation of electrical characteristics of CLC poly-Si n-TFT under DAHC stress is similar to the logic nMOSFET device and the worst reliability case may be occurred in high temperature, not low temperature.

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