Chapter 3 Fabrication

The fabrication process is covered in more depth in this chapter. SOI wafers and processing technology are selected due to the large device thickness, and therefore large capacitance that can be achieved. Additionally, deep RIE etching processes are used to fabricate devices with high aspect ratios. This also improves the maximum capacitance. A further benefit of the thick device layer and high aspect ratio is that the resulting devices have a very high out-of-plane stiffness compared to the in-plane stiffness. This is important for the attachment of a significant amount of mass to the device after the processing is completed.

3.1 Process flow

The basic process flow is shown in Fig 3.1. The SOI wafers have a device layer of 200 μm, oxide layer of 2 μm, handle layer (substrate) of 500 μm. The device layer silicon resistivity is less than 0.02 Ω-cm.

First, a thick photoresist of 7 μm is spin coated on the wafer and patterned via photolithography. Next the wafer is etched by Deep RIE down to the oxide layer. The third step is to remove the photoresist and to release the movable part by immersing the device in an HF solution with etching rate of about 1 μm/min. The release time should be controlled carefully so that the oxide under movable parts is removed completely but the anchor remains still. The fourth step is to apply aluminum by the thermal coater to form the pad and interconnection. The thickness is not more than 5000Å.

Finally, an external mass is attached to the movable plate. Since the mass is large, high density material like tungsten or steel is chosen to reduce the total size. The mass needs to be placed precisely on the center of the device; otherwise the out-of-axis motion will be easily induced. Therefore, the movable plate has a big hole in the center for a spherical mass, which can automatically fit into the position. Steel balls with various diameter (and thus mass) are available. The resonant frequency can be adjusted by applying different balls to fit the vibration source. The steel ball is bond to the center plate by a double stick tape.

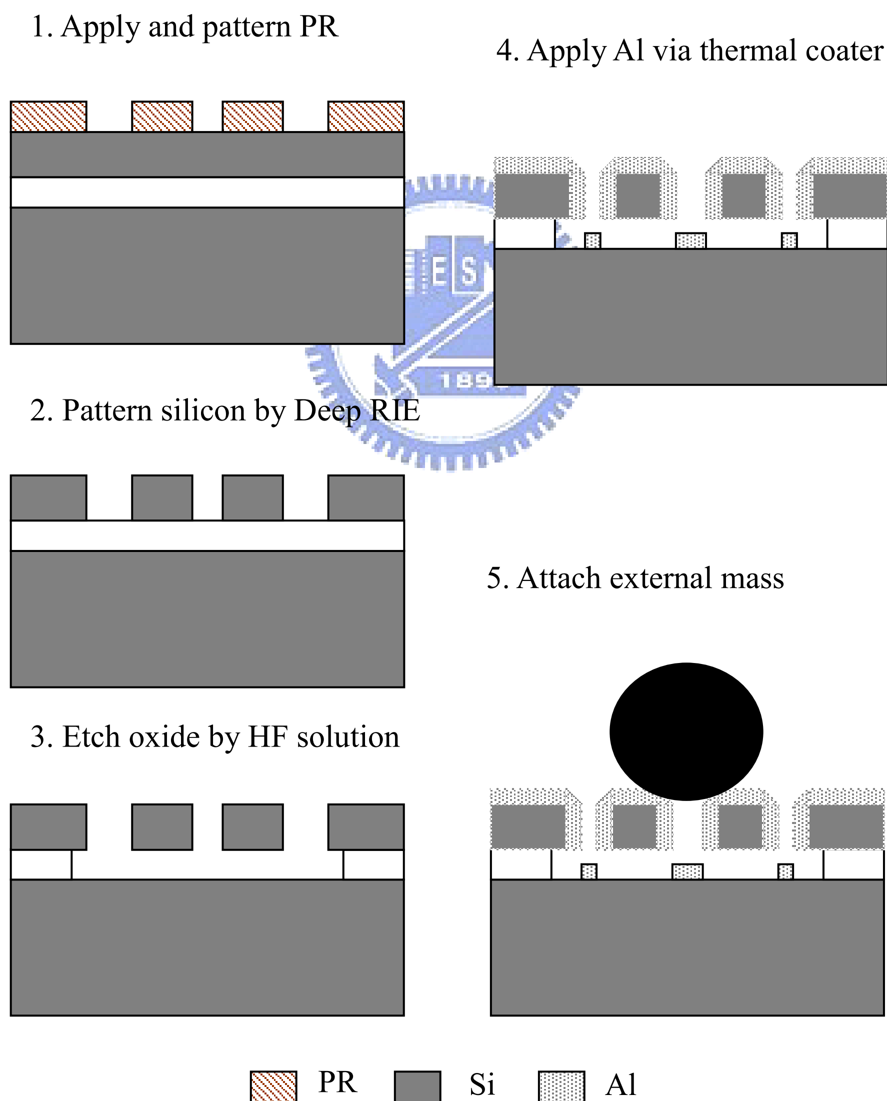


Figure 3.1 Process flow

3.2 Processing issues

Issues related to processing and tolerances are noted. First, it is essential to minimize parasitic capacitance. A main contribution to parasitic capacitance is the capacitance between the movable plate and the substrate beneath. The direct solution is to remove the substrate under the center plate by backside etching. Furthermore, though the backside etching does increase the processing complexity, the stiction issue in the releasing step can be prevented all at once. However, since the area of the etched substrate is very large, the robustness of the die or wafer can be a problem. The remained substrate will be fragile in supporting the device and the attached mass. As a result, the backside etching is not performed in the first prototype. The top plate and the substrate are connected with wire bonding to reduce the parasitic capacitance instead.

Parasitic resistance should also be noticed. Since the device is quite large, the device layer should be highly conductive to reduce resistive losses. Thus the device layer silicon resistivity is chosen to be less than 0.02 Ω-cm.

Next, as shown in Figure 3.2, the cross section of patterned thick photoresist, such as AZ4620 is not ideal. With the layout size of 10 μm and photoresist thickness of 8.5 μm, the actual width on the top and bottom are 7.8 μm and 9.3 μm, respectively. This is due to the photolithography inaccuracy, e.g. over exposure, over development, or the characteristic of the photoresist itself. Since the photoresist serves as the hard mask for deep RIE, this deviation will influence the device feature size. Improvement of the photolithography step can eliminate this problem to certain degree. Another solution is to pre-enlarge the layout size in the layout design.

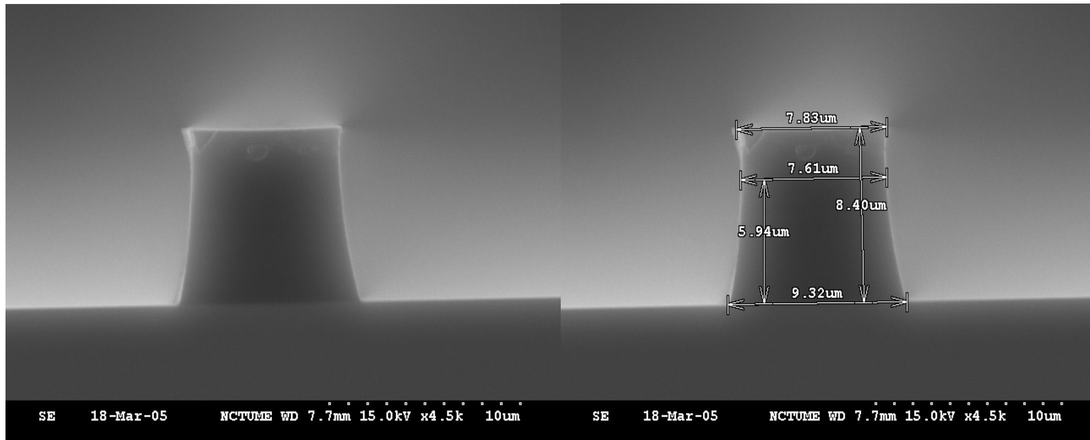


Figure 3.2 Cross-section view of thick PR patterning

Third, the deep RIE process has some unwanted characteristics [26]. First is the initial undercut issue as shown in Figure 3.3. The undercut is generally about 0.5 μm. This effect can be eliminated somewhat by process tuning. Moreover, the deep RIE process is a series of etching and passivation process (Bosch process [27]). This results in a wavy sidewall as shown in the Figure 3.3. In Chapter 2, the capacitance is calculated based on the assumption of two planar plates. Thus the wavy sidewall will cause unpredictable capacitance change compare to design value. Process parameters such as the etching and passivation duty cycle will influence the level of this effect. The peak to peak roughness is less than 100nm in the current process.

Since SOI wafers are used, dimples for stiction prevention can not be included in the design. Therefore, the release process needs to be treated carefully. In addition to releasing the movable plates by an HF solution, HF vapor release is also tried. After the oxide is etched away, the device is dried by the standard process using IPA and hotplate baking or CO_2 super critical approach.

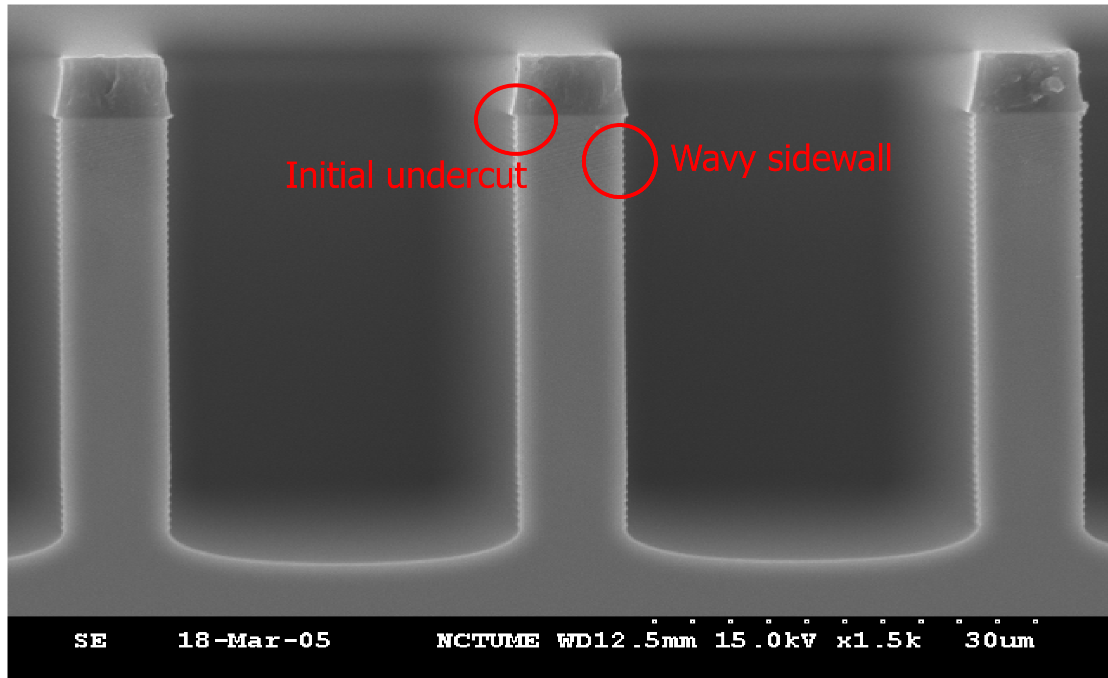


Figure 3.3 Initial undercut and wavy sidewall of deep RIE

The first wafer suffered a serious problem in the wafer dicing process. The wafer was diced before the device was released. Unexpectedly, the cooling wafer destroyed the comb fingers in almost every die on the wafer. The second wafer utilized photoresist as a protection layer to protect the fingers during the dicing process. The photoresist was spin coated all over the wafer after the deep RIE process and baked for 30 minutes at 90℃. After dicing, very few fingers were damaged. However, the fingers were bended by the photoresist in the gap as shown in Figure 3.4. After the protection photoresist was removed, most of the fingers returned back to the original position, as shown in Figure 3.5. In Figure 3.5, a probe was used to push the deformed fingers back to the center as shown in Figure 3.6. Most of the fingers could be pushed back to the center; only a few could not and would be removed by the probe to prevent shortage during the vibration.

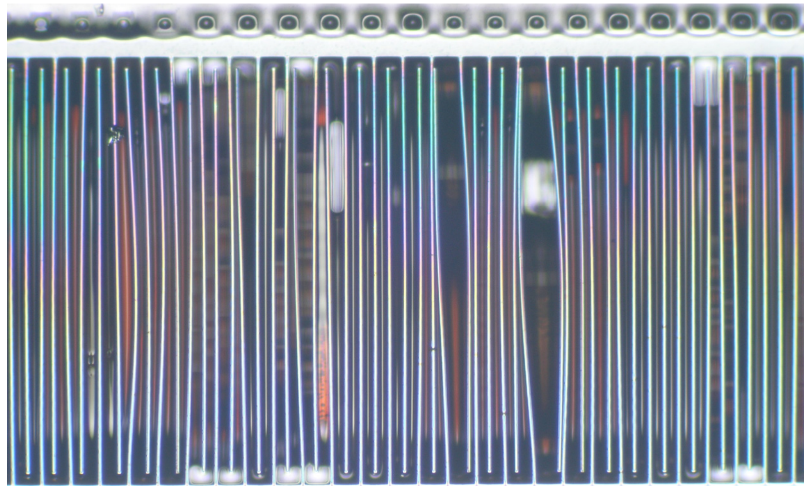


Figure 3.4 Bended fingers due to protection photoresist before release

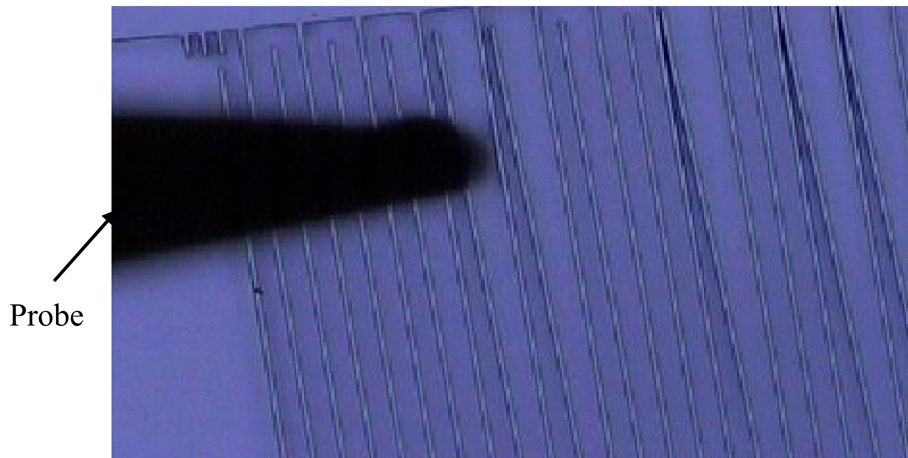


Figure 3.5 Bended fingers due to protection photoresist after PR removed

Figure 3.6 Bended fingers pushed back using probes

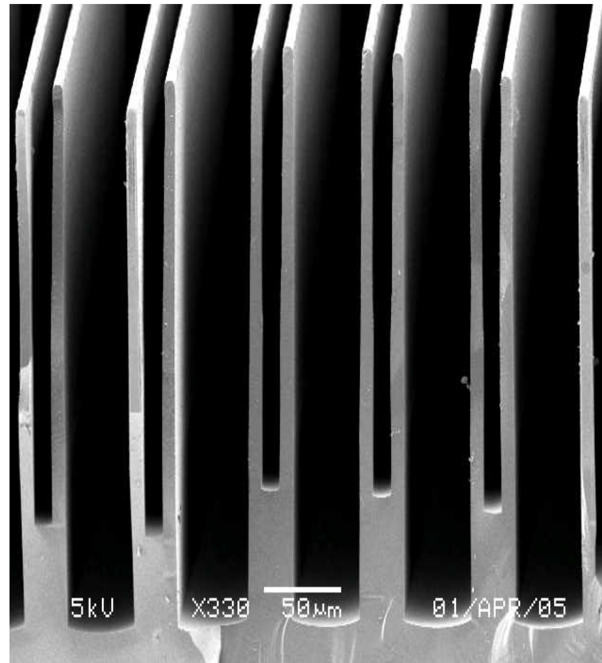


Figure 3.7 RIE leg effect

Unbalanced comb fingers as the driving electrodes were designed for measuring the spring constants and resonant frequency. However, the device failed due to RIE leg in the deep RIE process, as shown in Figure 3.7. The silicon between the closer fingers was not completely etched away. Thus the fingers stick together after released.

3.2 Fabricated device

Figure 3.8 shows the SEM photograph of the fabricated device, including the spring, mechanical stops, release holes, and a test pattern for the Deep RIE process in the lower right corner. Figure 3.9(a) shows the three short displacement indicator fingers below the movable finger in the lower right corner. The indicator fingers is 2 μm in the layout but were etched away in the deep RIE process, as shown in Figures 3-9 (b) and (c). The fabricated fingers are 1200 μm long and about 6.8 μm wide, as shown in Figure 3.10, compared to the layout width of 10 μm. The initial gap between

fingers is 29.4 μm, compared to the layout size of 25 μm. The cross section view of the fingers is shown in Figure 3.11. The etching depth is 200μm and the perpendicularity is about 90°. It can be seen that the fingers are thinner near the depth of about 50 μm. This may be attributed to the process control of the deep RIE process.

The reason of the shrunk feature size are the non-ideal photolithography and the under cut of the deep RIE process as mentioned above. Besides the process tuning and pre-enlarge the feature size, another solution is to apply additional oxide layer. The PECVD oxide can be coated on the wafer before the photolithography process. The oxide is patterned by the same photolithography mask with thinner photoresist, which the effect of PR non-ideality is reduced. Oxide layer with the remaining PR than serve as the hard mask in the Deep RIE process which provide higher selectivity and can thus reduce the shrunk feature size.

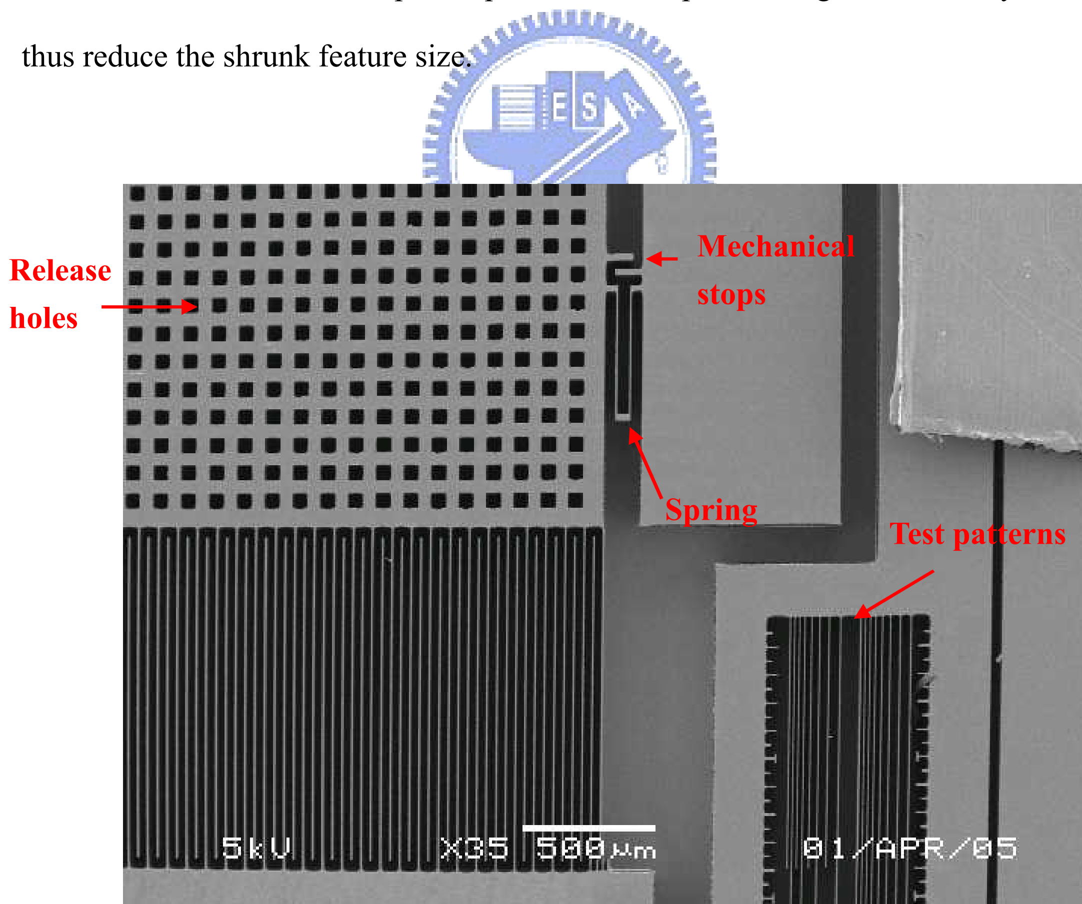
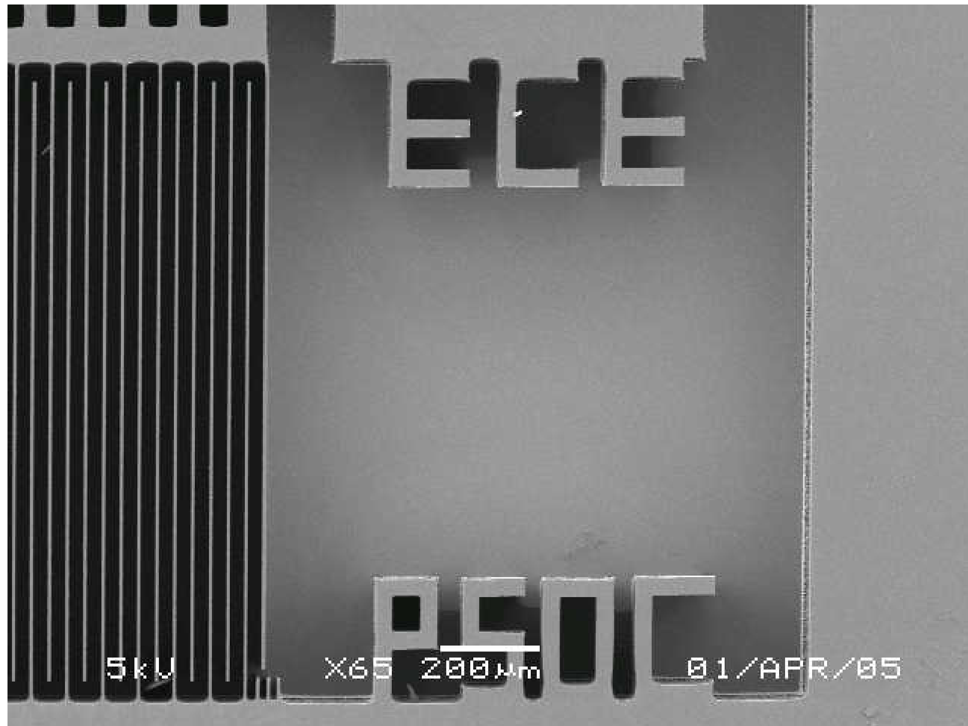
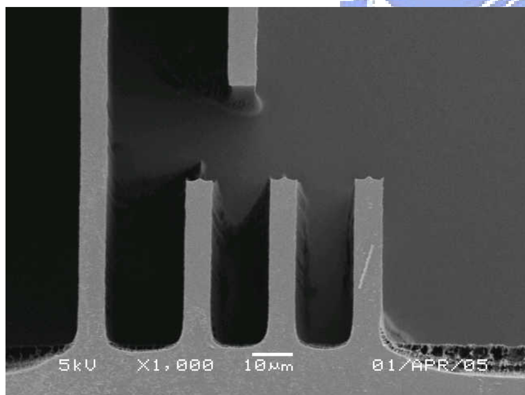
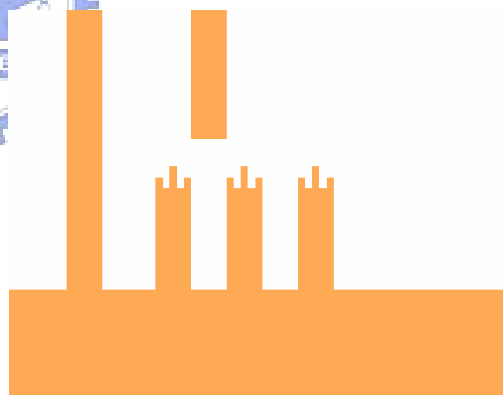


Figure 3.8 SEM top view of the corner of device



(a)





(b) (c)

Figure 3.9 Displacement indicator (a) top view (b) close up view (c) layout

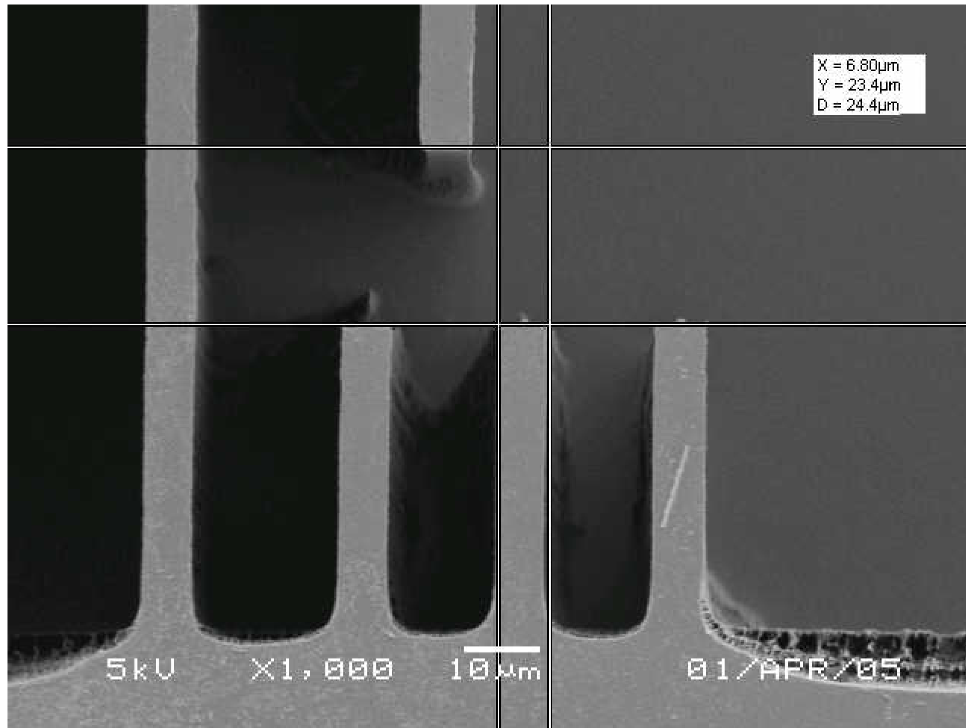


Figure 3.10 Shrunk finger width

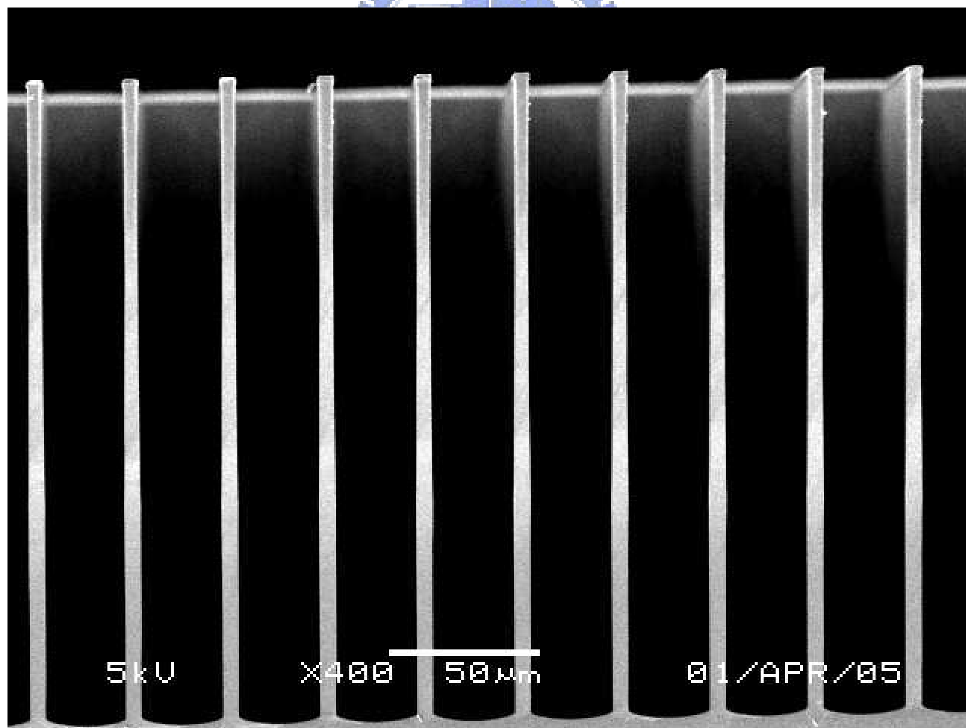


Figure 3.11 Cross section view of fingers