

藉由非理想特性與功率分析達到三角積分類比數位轉換器之最佳化設計

研究生：鍾卓翰

指導教授：陳福川 教授

國立交通大學

電機與控制工程研究所

摘要

由於傳統的積分三角類比數位轉換器設計過程需花費大量的時間和需要經過許多的錯誤嘗試。因此，在本篇論文中，我們提出一個針對積分三角類比數位轉換器的最佳化設計演算法。首先我們必須透過了解電路上的不完美特性，來建立積分三角電路的非理想特性模型，而為了估測其功率消耗，我們亦嘗試建立功率消耗模型。我們發現在積分三角調變器的電路中，各項設計參數如超取樣比、量化位元數...等的變化均有可能造成雜訊功率的改變，甚至造成整體功率消耗的變化。而不同設計參數的組合，亦可能會造成在系統效能上相當大的差異，所以我們在設計積分三角調變器時，需要一組最佳化的設計參數。我們所提出的最佳化演算法可以找出在特定系統規格下，能達到最大權重函數的一組設計參數，通常這便是所需的最佳化參數。這套演算法是由 Mathematica 這套數值軟體建構而成。最後我們將針對兩篇已發表的設計結果來做驗證的工作。

Optimization Designs of Sigma-Delta ADCs via Nonideality and Power Analyses

Student : Cho-Han Chung

Advisor : Dr. Fu-Chuang Chen

Institute of Electrical and Control Engineering

Nation Chiao Tung University

ABSTRACT

An optimization algorithm for the design of $\Sigma\Delta$ ADCs is proposed. Conventional $\Sigma\Delta$ ADCs design approach is a time consuming process and needs much trial and error. Through a systematic study of circuits' imperfections, circuit nonideality models are derived in output noise power forms. Power model is also presented in order to estimate the relative power consumption. Through analyzing the models, it is clear that variation of a design parameter can potentially affect several noises and errors in different ways, and may change system power rate. This complexity is qualitatively summarized into a table. The completeness of models allows us to propose an optimization algorithm to search globally for a combination of design parameters which meet the design specifications while minimizing power consumption. Our optimization algorithm is tested against two published design results. Some design discrepancies are observed, and they are analyzed and discussed. Parameter sensitivity issues are also visited.

誌謝 Acknowledgment

在這裡向我的指導教授陳福川教授致上最大的謝意，感謝老師兩年來的指導與關懷，由於老師不斷的督促，讓我在專業領域中獲得更多的知識，也使我徹底了解做研究的方法與精神，使得論文能順利的完成。此外也感謝口試委員林清安教授、董蘭榮博士與洪浩喬博士對本篇論文所給予的建議與指導。

還要感謝實驗室的兩位學長—林旻致學長跟陳威志學長。打從進實驗室的第一天起，你們就帶領著我來熟悉環境。一切學業上與研究生生活上不懂的地方都會請教兩位學長。感謝威志學長在類比電路設計上給我的指導，讓我從以前的完全不懂到現在的程度，真的很感謝你。感謝旻致學長教導我如何當一個稱職的研究生，也在無聊的周末陪我一起出去玩，或是大家一起去吃大餐，這種滋味真的很難忘。另外，也感謝湯鎮帆學長在研究上對我的支持，幫我解答了許多的疑點與迷惑，使我的論文可以順利完成。另外感謝我的同袍詠文，因為有你，許多數位電路上的設計工作變的簡單，也感謝你指導我許多程式方面的問題，祝你以後前程似錦，發展順利。接著還要謝謝實驗室的學弟—英瑋，由於你的加入使得實驗室更加活潑與熱鬧，並且在論文的研究過程中也因為有與你的討論與切磋，才能彌補我不足的地方。由於有各位同學，學長跟學弟的支持與參予，使的六 0 八實驗室能蓬勃的發展，也充滿欣欣向榮的氣息。謝謝所有在清華大學與交通大學幫助過我的老師、朋友跟同學，因為有你們，使我在新竹留下了一輩子難以忘記的美好回憶。

最後要感謝我的父母，讓我在求學的過程中可以無後顧之憂，沒有你們的支持，永遠也不會有今天的我；同時也謝謝我的女友書敏，每當心情鬱卒時，有妳的安慰能使我快速的振作起來，也感謝妳在這兩年全心的支持與鼓勵。

List of Symbols

Symbols

| | |
|-----------------|---|
| V_{LSB} | Quantizer step size |
| OSR | OverSampling Ratio |
| n | Order of the sigma delta modulator |
| B | Number of bits in the quantizer |
| f_s | Sampling Frequency |
| f_B | Signal Bandwidth |
| V_{ref} | Reference Voltage of the quantizer |
| A | Gain of OTA |
| f_{in} | Frequency of the input signal |
| ϕ_i | i th phase of a nonoverlap clock |
| A_i | Amplitude of input signal |
| $\sigma_{jit.}$ | standard deviation of clock jitter |
| C_s | Sampling capacitor |
| C_I | Integrating capacitor |
| C_L | Load capacitor of OTA |
| V_s | Input signal plus feedback DAC signal |
| τ_1 | Time constant of input branch |
| σ_{v_s} | Standard deviation of V_s |
| τ_2 | Time constant of integrator output settling |
| a_i | gain coefficient of i th integrator |
| η | percentage of the bottom plate parasitic |
| T | Absolute temperature |
| R | Switch ON resistance |
| N | quantizer levels |
| gm1 | Amplifier transconductance |
| Pr() | Probability of some condition |
| $\sigma_{cap.}$ | Mismatch of unit capacitance |
| k | Boltzmann's constant (1.38×10^{-23}) J/K |
| α | OTA noise factor |
| $Erf[]$ | Error Function |

Lists of Tables

| | | |
|-----------|--|----|
| Table 4.1 | Std. deviation of V_s with different quantizer level | 40 |
| Table 4.2 | Tolerant comparator offset for different OSR and topologies | 51 |
| Table 4.3 | Tolerant comparator hysteresis for different OSR and topologies | 51 |
| Table 5.1 | Summary of noise-power and power-rating when design parameters increase | 81 |
| Table 6.1 | Comparisons of our design results and those in [Gag 03] with different K | 85 |
| Table 6.2 | The corresponding noise powers for the design parameters listed in Table 6.1 | 87 |
| Table 6.3 | Comparisons of our design results when $K = 0.8$ with those in [Gee 00] | 89 |

Lists of Figures

| | |
|--|----|
| Fig. 1.1 Conventional design methodology of $\Sigma\Delta$ modulator | 2 |
| Fig. 2.1 (a) Original signal spectrum | |
| (b) Sample function when $f_s > 2f_B$ | |
| (c) Signal spectrum that is sampled by (b) | |
| (d) Sample function when $f_s < 2f_B$ | |
| (e) Signal spectrum that is sampled by (d)..... | 6 |
| Fig. 2.2 Quantization process | 7 |
| Fig. 2.3 Quantization error caused by A/D converter | 7 |
| Fig. 2.4 Quantization error range | 8 |
| Fig. 2.5 P.D.F of quantization error | 8 |
| Fig. 2.6 Sampling system | 10 |
| Fig. 2.7 Noise distribution after sampling | 10 |
| Fig. 2.8 (a) General sigma delta modulator | |
| (b) Linear model with quantization noise | 11 |
| Fig. 2.9 Noise shaping | 12 |
| Fig. 3.1 Block diagram of sigma delta A/D converter. | 14 |
| Fig. 3.2 First order sigma delta modulator | 15 |
| Fig. 3.3 Single-loop second order $\Sigma\Delta$ modulator | 17 |
| Fig. 3.4 Comparison of noise shaping techniques | 18 |
| Fig. 3.5 Single loop high order sigma delta modulator | 19 |
| Fig. 3.6 Four-order interpolative architecture | 19 |
| Fig. 3.7 2-1 architecture MASH sigma delta modulator | 21 |
| Fig. 3.8 SNR v.s. OSR with different quantizer bit number | 23 |

| | |
|--|----|
| Fig. 3.9 Multibit architecture | 24 |
| Fig. 3.10 A B-bit DAC with DEM technique | 25 |
| Fig. 3.11 Operation principle of the DWA algorithm | 26 |
| Fig. 3.12 Output spectrum with three kinds of DAC | 26 |
| Fig. 3.13 Comparison of sigma delta modulator architectures | 27 |
| Fig. 3.14 Performance characteristic of a sigma delta converter | 30 |
| Fig. 4.1 Schematic of a generalized $\Sigma\Delta$ modulator | 31 |
| Fig. 4.2 Schematic of a switched capacitor integrator | 32 |
| Fig. 4.3 Illustration of $\Sigma\Delta$ output Spectrum with finite OTA gain | 34 |
| Fig. 4.4 Influence of finite OTA gain on single loop second order 3 bit system | 34 |
| Fig. 4.5 General model of n order single-loop $\Sigma\Delta$ modulator | 36 |
| Fig. 4.6 INTF of a second order $\Sigma\Delta$ modulator with 1% mismatch | 36 |
| Fig. 4.7 SNR versus mismatch of a second order three-bit $\Sigma\Delta$ modulator | 37 |
| Fig. 4.8 SC integrator model with switch resistance R | |
| (a) Sampling phase | |
| (b) Integration phase | 38 |
| Fig. 4.9 Input voltage histogram of first integrator | |
| (a) 10-level quantizer | |
| (b) 13-level quantizer | 39 |
| Fig. 4.10 Integrator output voltage vs. time | 41 |
| Fig. 4.11 A Gaussian distribution V_s | 44 |
| Fig. 4.12 Single loop 2 nd order sigma delta ADC with SIMULINK | 45 |
| Fig.4.13 Output settling noise floor vs. OSR | 46 |
| Fig. 4.14 Output noise spectrum of a 2 nd order sigma delta modulator OSR =500 | 47 |
| Fig. 4.15 The charge distribution when the MOS switch turns off | 48 |
| Fig.4.16 Clock feedthrough effect | 49 |

| | |
|---|----|
| Fig. 4.17 Transfer curve of a comparator with offset and hysteresis | 50 |
| Fig. 4.18 Implementation of the 4-bit DAC | 52 |
| Fig. 4.19 A nth-order multi-bit sigma delta converter with the nonideal DAC | 53 |
| Fig. 4.20 P.d.f of DAC noise with 3 bit quantizer | 54 |
| Fig. 4.21 A nth order sigma delta converter with DWA calibration | 56 |
| Fig. 4.22 Corresponding output spectrum of Fig. 4.21 | 56 |
| Fig. 4.23 Illustration of Clock Jitter | 57 |
| Fig. 4.24 Output spectrum of a jittered system with different input frequency | 59 |
| Fig. 4.25 Resistor thermal noise model and its PSD | 60 |
| Fig. 4.26 (a)S/H circuit (b) NMOS switch (c) PMOS switch (d)CMOS switch | 61 |
| Fig. 4.27 Finite resistance model of a switch | 61 |
| Fig. 4.28 A sampling circuit with noise source | 62 |
| Fig. 4.29 Multi-branches sampling circuit | 63 |
| Fig. 4.30 Schematic of integrator during sampling phase | 64 |
| Fig. 4.31 Scheme of integrator during sampling phase with thermal noise sources ... | 65 |
| Fig. 4.32 Scheme of integrator during integration phase with thermal noise sources | 66 |
| Fig. 4.33 Noise voltage source of MOSFET | 67 |
| Fig. 4.34 Equivalent circuits of sampling and integration phase | 68 |
| Fig. 4.35 Integrator output noise spectrum in sampling phase | 68 |
| Fig. 4.36 gm1 versus OTA thermal noise | 70 |
| Fig. 4.37 Bandgap voltage reference circuits | 71 |
| Fig. 4.38 Equivalent circuit while considering reference noise | 71 |
| Fig. 4.39 Main nonidealities sources in the sigma delta modulator | 72 |
| Fig. 5.1 OTA noise versus a1 with OSR=64 | 77 |
| Fig. 5.2 (a) SNR versus R with 100 kHz signal bandwidth | |
| (b) SNR versus R with 1 MHz signal bandwidth | 78 |

Fig. 5.3 Proposed optimization algorithm for the sigma delta modulator design 81

Fig. 6.1 3D plot of $P\delta^2$ v.s. GBW and SR 88

Fig. 6.2 3D plot of variation of SNR with respect to R and C 91



Contents

| | |
|---|-----|
| 中文摘要 | I |
| English Abstract | II |
| 誌謝..... | III |
| List of Symbols | IV |
| Lists of Tables | V |
| Lists of Figures | VI |
| Contents | X |
| Chapter 1 Introduction | 1 |
| 1.1 Current Status and Background | 1 |
| 1.2 Motivation and Aims | 1 |
| 1.3 Organization | 4 |
| Chapter 2 Fundamental Theorems of Sigma-Delta Modulator | 5 |
| 2.1 Nyquist Sampling Theorem | 5 |
| 2.3 Quantization Noise and Peak SNR | 7 |
| 2.2 Techniques of Sigma-Delta Modulator | 9 |
| 2.3.1 Oversampling | 9 |
| 2.3.2 Noise shaping | 11 |
| Chapter 3 Architectures of Sigma Delta Modulator | 14 |
| 3.1 First Order Sigma delta Modulator | 15 |
| 3.2 Second Order Sigma delta Modulator | 17 |
| 3.3 Single Loop High Order Sigma Delta Modulator | 18 |
| 3.4 Interpolative Sigma Delta Modulator | 19 |
| 3.5 MASH Architecture | 20 |
| 3.6 Multi-bit Quantization Sigma Delta Modulator | 22 |

| | |
|---|----|
| 3.7 Multi-bit Sigma Delta Modulator use DEM Technique | 24 |
| 3.7.1 Randomization Technique | 25 |
| 3.7.2 Data Weighted Averaging (DWA) | 25 |
| 3.8 Decimator | 27 |
| 3.9 Performance Metrics for a $\Sigma\Delta$ Modulator | 28 |
| Chapter 4 Models of Sigma Delta Modulator Nonidealities and Power | 31 |
| 4.1 Models of Integrator Nonidealities | 32 |
| 4.1.1 Finite OTA Gain | 33 |
| 4.1.2 Capacitor Mismatch in Coefficient | 35 |
| 4.1.3 Settling Problem | 37 |
| 4.1.4 Clock Feedthrough and Charge Injection | 48 |
| 4.2 Quantizer Nonidealities | 49 |
| 4.3 Models of DAC Nonidealities | 51 |
| 4.4 Models of other Intrinsic Noises | 56 |
| 4.4.1 Clock Jitter Noise | 57 |
| 4.4.2 Thermal Noise of Switches, OTAs and Reference Voltage | 59 |
| 4.5 Models of Relative Power | 72 |
| Chapter 5 Optimization Algorithm of Sigma-Delta ADCs Design | 75 |
| 5.1 Modified SNR Equation | 75 |
| 5.2 Discussions of Circuit Parameters | 76 |
| 5.3 Trade-Off between SNR and Power | 80 |
| 5.4 Optimization Algorithm | 81 |
| Chapter 6 Experimental Results | 84 |
| 6.1 Sigma Delta ADC for ADSL-CO Application | 84 |
| 6.2 Sigma Delta ADC for Broadband Application | 89 |
| 6.3 A Discussion on Sensitivity of parameters | 90 |

Chapter 7 Conclusions and Future Works 92
References 94

