1
Introduction

1.1 Current Status and Background

Sigma-Delta modulators are widely used for high resolution analog-to-digital conversion applications, achieving resolution up to 12~20 bits. The earlier focus is on low to medium speed applications, such as audio [Bos 88][Nor 89][Fog 00], voice codec and DSP chip. In recent years, sigma delta ADCs are applied to signals with higher bandwidth and low power. For example, in ×DSL [Gag 03][Rio 04] applications, people need to handle signals up to 2.2MHz. Since it is difficult to significantly increase the sampling rate (80 MHz is the current limit), people either seek to increase order or cascade stages [Oli 02][Vle 01][Jia 04], or to employ multi-bit quantization [Gri 02][Mil 03], or both, in order to achieve the required dynamic range. Due to advances in process technologies, the matching properties of component have been much improved, so the multi-bit architecture is becoming popular. New technologies also help to reduce power consumption [Yao 04]. The design of sigma delta modulators is a complex and time consuming process, because there are many coupled design parameters to be determined. Since the design specifications are getting more demanding as is described above, it is very challenging to come up with an acceptable design. In this work, we proposed an optimization approach to increase the automation and reduce complexity in the sigma delta ADCs design.

1.2 Motivation and Aims

Typically, when signal bandwidth is specified, people use the following three steps

to design a ΣΔ ADC to achieve a desired effective output resolution. First step is called system level design, people need to decide on a system architecture. One can choose among single-loop or MASH architecture. Each has different pros and cons. Then, ideal peak SNR equations are frequently employed to help determine such system parameters as oversampling ratio (OSR), quantizer bit number B, orders of ΣΔ modulator *n*, and gain coefficients. The ideal peak SNR is deliberately made larger here, because it will inevitably be reduced by circuit noise and other errors. Different selections of these parameters may cause large variation in performance [Mar 98b]. Second step is called circuit level design, the nonidealities in the ΣΔ modulator must be considered. Every effort is made to select circuit parameters to reduce the effects of the nonidealities. This is a complex and difficult task, since the circuit parameters and the nonidealities are highly coupled. For example, a larger sampling capacitor can suppress thermal noise, but it can also increase the integrator loading and the analog power consumption. Much trade off exists in this step, and extensive experiences are required. Yet, there is no guarantee of optimal choice of parameters. Finally, the overall design goes through simulations and, if acceptable, may be implemented. This flow is shown in Fig. 1.1.

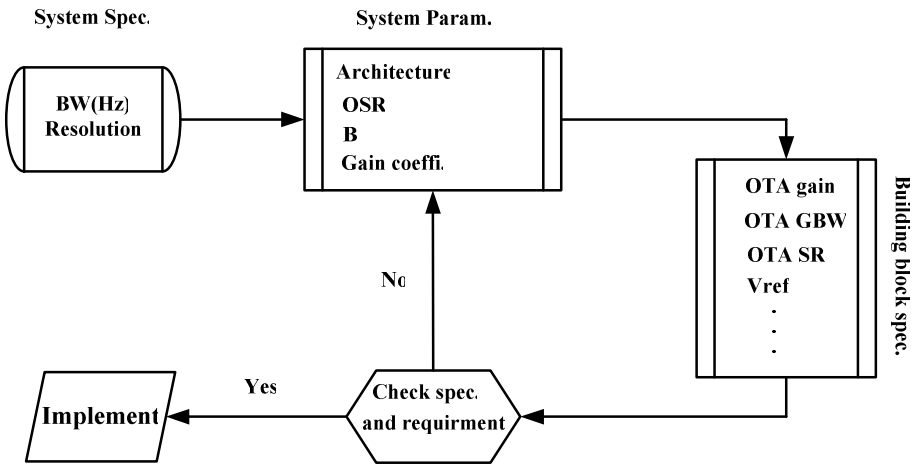


Fig. 1.1 Conventional design methodology of sigma delta modulator

We will focus on single-loop architecture in this work, in order to propose an optimization algorithm; we need to have models of the nonidealities and the model of power consumption. Issues about $\Sigma\Delta$ modulator noise and error modeling appeared in [Bos 88] [Nor 89] [Mal 03] [Wu 01] [Kas 03] [Dia 92] [Med 99] [Mar 00] [Ter 03] [Bri 97] [Sch 97]. In [Fra 00] and [Sch 97] some system simulation tools were proposed. The simulator in [Fra 00] is time consuming because it uses behavioral models of nonidealities. Also, it lacks models of the multi-bit DAC noise and the reference thermal noise. The simulator in [Sch 97] is a tool box can be used in Matlab, although it is a convenient simulator but it lacks models of the major nonidealities in sigma delta ADC and only those can be mapped to the transfer function could be included by the user manually. The results in [Mal 03], [Wu 01], [Kas 03] model some nonidealities by simple behavioral functions, but these models are not shown in noise power forms, so people cannot easily observe the relations between circuit parameters and noise powers. The applications of these models depend heavily on the experience of the designers, and much trial and error is needed. Reference [Dia 92] modeled the settling noise and the thermal noise, but some assumptions about the settling error are not accurate. The OTA models in [Med 99] are relatively complete, but it lacks the DAC noise modeling. Results in [Mar 00] [Ter 03] focus on the device noises such as thermal noise and flicker noise. Flicker noise is not considered in this work because there are several techniques to reduce its effect, such as using large size transistor in OTA or using Correlated Double Sampling. In chapter 4, we will elaborate on settling noise, DAC noise, OTA thermal noise and reference voltage thermal noise. We also categorize all the major nonidealities into 4 parts, and present their models in noise power forms in a multi-bit setup. The power consumption models for the analog part [Mar 98a] and the digital part of $\Sigma\Delta$ modulators will be given too.

Differing from the conventional design in Fig. 1.1, another design approach is proposed. We combine the system and circuit level designs, and optimize all design parameters ay the same time. The main nonideailties are taken into account for optimization, and then the optimal SNR point can be obtained quickly. Power consumption is also considered in the optimization. The relation between circuit parameters and power consumption is derived. The proposed optimization design of single-loop $\Sigma\Delta$ ADCs considers both on power and performance at the same time. It is convenient for an inexperienced designer. Because there exists some trade off between system and circuit parameters. By establishing theses trade-offs equations, we can easily estimate optimal SNR. It is helpful in the starting of design. This noise model also helps people to sweep circuit parameter versus the impact of nonidealities on the modulator's performance.

1.3 Organization

This work is organized as follows. In Chapter 2 and Chapter 3, systematic studies of fundamental theory and various architectures of $\Sigma\Delta$ modulator are presented first. In Chapter 4, analyses of several errors which may degrade system performance are proposed, the power consumption model uses the same parameters as error models is derived. In Chapter 5, the optimization algorithm of sigma delta modulator design is proposed, and the circuit parameters that involve with SNR and power consumption are discussed, it will propose a guideline for the sigma delta converter design. In Chapter 6, experimental results of published papers for different applications like ADSL and broadband communication are listed and the conclusion and future works are presented in Chapter 7.

2
Fundamental Theorems of Sigma-Delta Modulator

Before we establish the error model and optimization of sigma-delta, there are several important theorems and concepts must be known, such as Nyquist sampling theorem and quantization error, and the two most critical techniques in sigma-delta modulator: oversampling and noise shaping. All topology of sigma-delta modulator are based on these two techniques. There also have some parameters we must to understand, just like OSR, SNR…etc. The section in bellow will start from fundamental theorem, and introduce several topologies of sigma delta modulator.

We will illustrate quantization error and analyze quantization noise with ideal A/D converter, furthermore derives the peak signal-to-noise ratio. The resolution of whole A/D converter is determined by signal-to-noise ratio. This is a very important parameter in the system, also.

2.1 Nyquist Sampling Theorem

In the analog-to-digital converter, the continuous analog signal comes from external environment must convert to discrete time signal by sampling, however the sampling rate (fs) and signal frequency (f_B) must follow Nyquist sampling theorem in (2.1):

$$f_S \geqq 2f_B \qquad (2.1)$$

the sampling rate must higher or equal to two times of signal bandwidth in order to prevent the occurrence of aliasing. We will illustrate the phenomenon of aliasing by Fig. 2.1. Fig. 2.1(a) and (b) is the spectrum of signal and sample function respectively; from fig. 2.1(c), when sampling rate is two times higher than signal bandwidth, the

signal after sampling has no aliasing, such signal can be perfectly reconstructed by using low pass filter. However, in Fig.2.1(d), when the sampling rate is lower than two times of signal bandwidth, aliasing will appear in the signal after sampling. The signal has aliasing is difficult to reconstruct to original signal[Mach 96], like Fig.2.1(e).

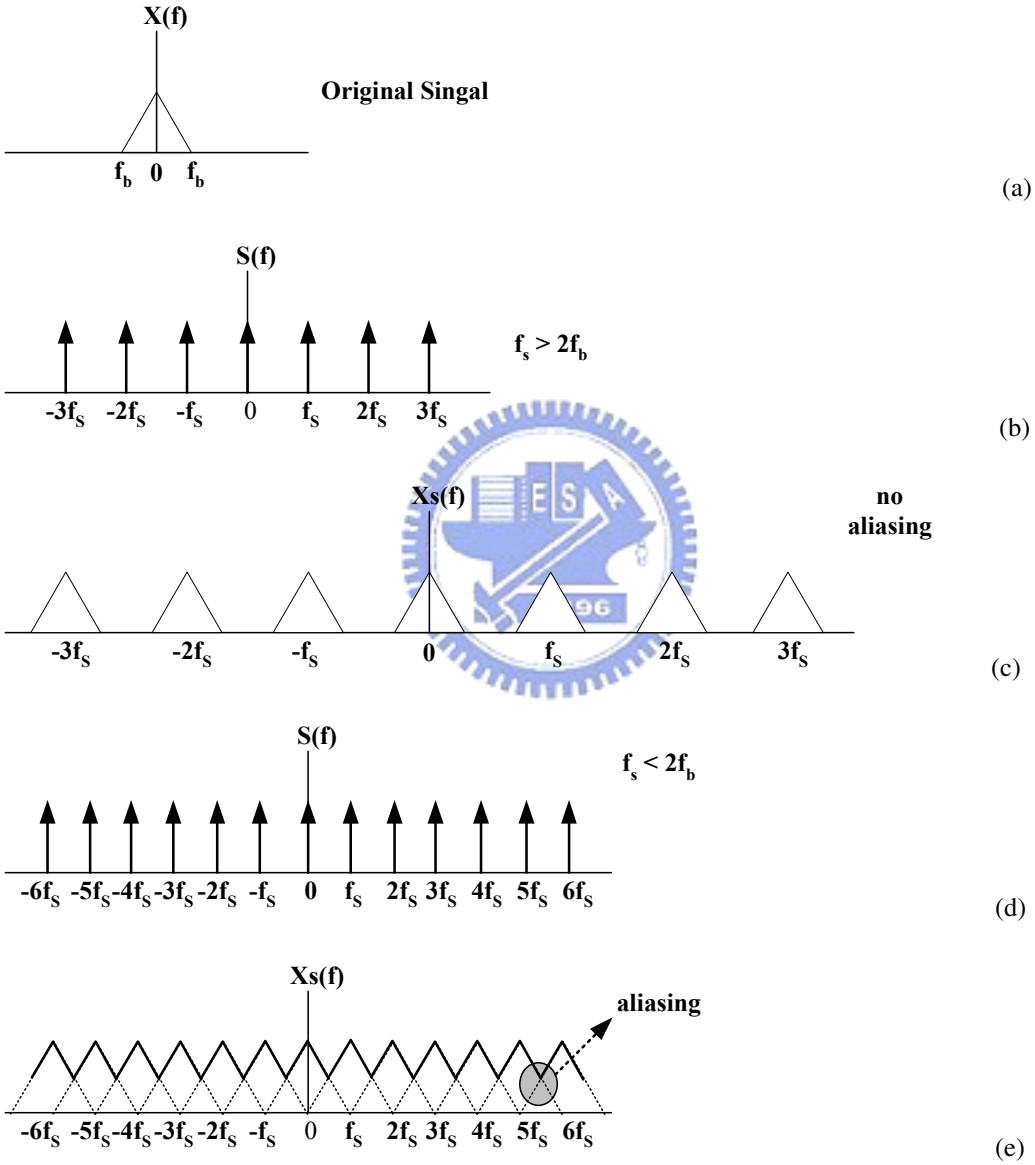


Fig. 2.1（a）Original signal spectrum（b）Sample function when fs > 2fB（c）Signal spectrum that' sampled by (b)（d）Sample function when fs < 2fB（e）Signal spectrum that sampled by (d)

2.2 Quantization noise and Peak SNR

We can get a discrete-time signal by sampling continuous time signal, this signal can be converted to digital signal. Quantization will appear in this process, the basic concept of quantization is to classify the original signal to different level, and according to its level to determine the bit number of this signal, as Fig. 2.2 shows.

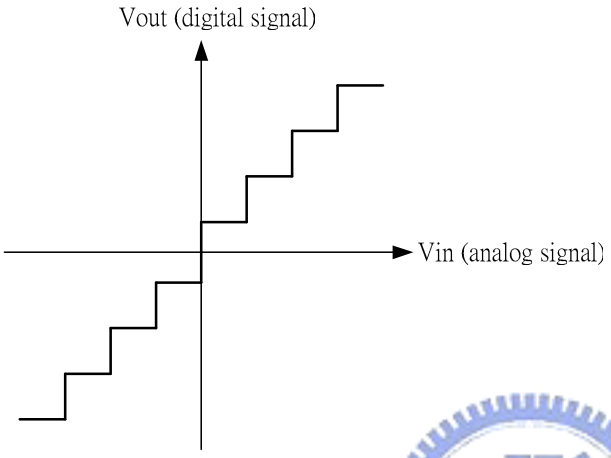
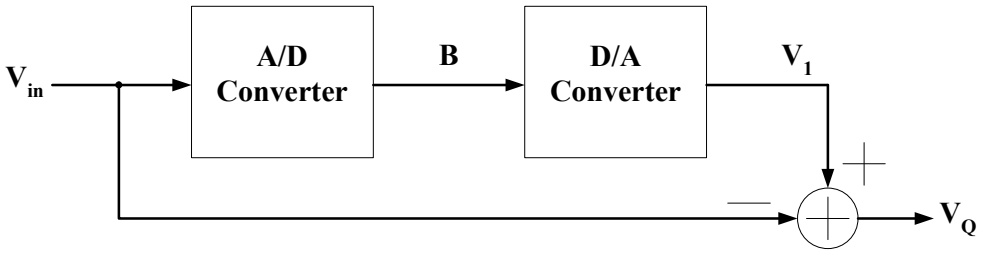


Fig. 2.2 Quantization process

Even in the ideal analog-to-digital converter will have quantization error. As in Fig .2.3, we convert the digital signal B to analog signal V_1 by a D/A converter, and be subtracted by input signal Vin, the result is the quantization error V_Q, as equation (2.2)[Joh 97].

$$V_Q = V_{in} - V_1 \qquad (2.2)$$



Quantization noise $V_Q = V_{in} - V_1$

Fig. 2.3 Quantization error caused by A/D converter

Range of quantization error is limited in $\pm V_{LSB}/2$ (as Fig. 2.4), and we assume the probability density function of quantization error is uniform distribution between $\pm V_{LSB}/2$, its mean is zero, like Fig. 2.5. From this assumption, we can easily get quantization noise power $V_{Q(rms)}^2$ is as equation (2.3).

$$V_{Q(rms)}^2 = \int_{-\infty}^{\infty} x^2 \cdot f_Q(x) \cdot dx = \frac{1}{V_{LSB}} \int_{-VLSB/2}^{VLSB/2} x^2 \cdot dx = \frac{V_{LSB}^2}{12} \qquad (2.3)$$

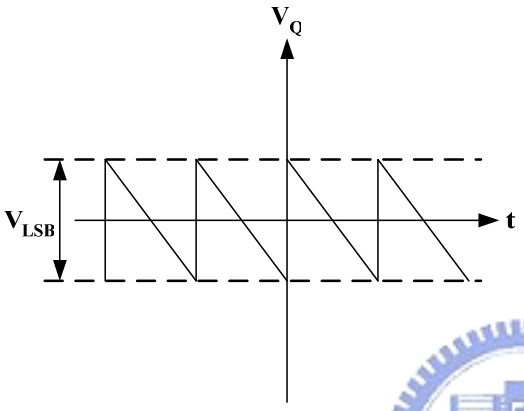


Fig. 2.4 Quantization error range

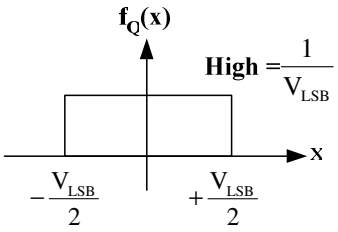


Fig. 2.5 P.D.F of quantization error

From (2.3) we can know the quantization noise power is proportional to square of V_{LSB}, and V_{LSB} can represent as equation(2.4), so we can say that the quatization noise will be reduce by increasing quantization bit number.

$$V_{LSB} = \frac{FS}{2^B} \qquad (2.4)$$

FS=Full scale = $V_{ref+} - V_{ref-}$　　B：Quantization bit number

Assume that input signal is sinusoidal, expressed as $V_{in}(t) = A \sin\omega t$，so the input signal power $V_{in(rms)}^2$ is as（2.5）, in this equation we define the amplitude of input signal is the full scale of reference voltage, and from (2.3), (2.4) and (2.5), the peak SNR(Peak Signal-to-Noise Ratio) can be derived as equation (2.6).

$$V_{in(rms)}^2 = \frac{1}{T} \int_{-T/2}^{T/2} (A \cdot \sin \omega t)^2 \cdot dt = \frac{A^2}{2} = \frac{(2A)^2}{8} = \frac{FS^2}{8} \qquad (2.5)$$

$$PSNR = 10 \log \left(\frac{V_{in(rms)}^2}{V_{Q(rms)}^2} \right) = 6.02B + 1.76 \text{ dB} \qquad (2.6)$$

Equation (2.6) is the result obtained by Nyquist sampling rate, can know that each additional bit number in quantizer increase 6dB in SNR. In Nyquist A/D converters, increases the resolution of quantizer (decrease V_{LSB}) to reduce quantization noise is a general method, to reach higher SNR, but this method is sensitive to analog device mismatches, so the general Nyquist A/D converter is not easily to implement with high resolution.

2.3 Techniques of Sigma-Delta Modulator

In order to reach high resolution, sigma delta A/D converter is based on oversampling and noise shaping. Oversampling means the sampling rate is much faster than Nyquist rate, about 8~512 times in general applications, the mean goal of oversampling is to expand quantization noise to wider range, it can reduce the quantization noise in signal bandwidth and increase the DR(Dynamic range) of input signal. Noise shaping is a technique that moves noise to high frequency, it is done by using discrete time filter and feedback technique, after noise shaping, the noise in high frequency can be filtered by a digital filter[Nor 97].

2.3.1 Oversampling Technique

First, the assumption that quantization noise is a uniform distribution in sampling spectrum must be true, its mean is zero and called white noise [Raz 01]. The system in Fig. 2.6 just has oversampling function and don't have noise shaping effect. If a A/D converter is sampled by Nyquist rate, then the quantization noise is uniform distribute between $\pm f_B$; if it is sampled by oversampling technique, then quantization noise is uniform distribute between$\pm$ $f_{S2}/2_s$, it is much larger than $f_{B;}$ As in Fig. 2.7, if the bandwidth we need is between $\pm f_{B,}$ quantization noise in this bandwidth will be reduced by using oversampling technique, it will raise PSNR significantly.

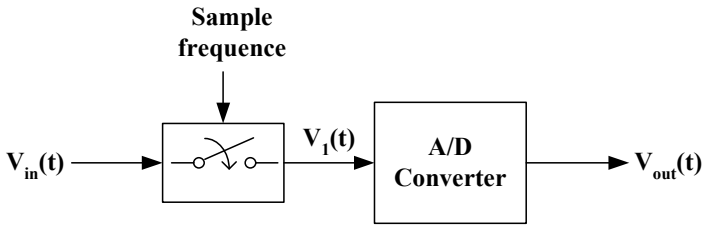


Fig. 2.6 Sampling system

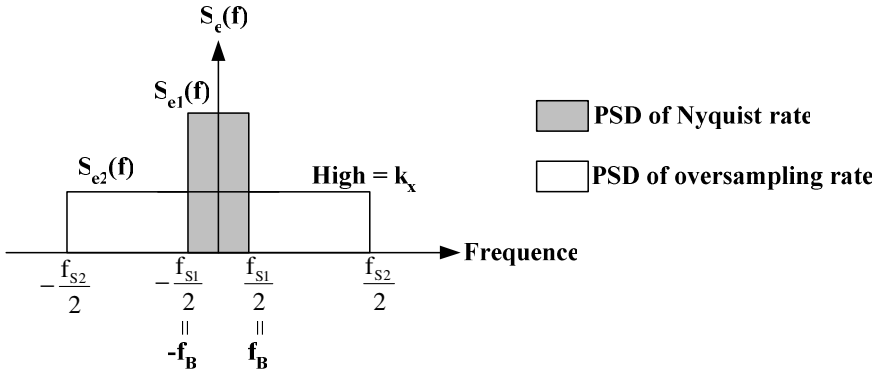


Fig. 2.7 Noise distribution after sampling

In the condition of oversampling, the PSD(Power Spectrum Density) of quantization noise is as $S_{e2}(f)$ in Fig. 2.7 and can be represent as:

$$k_x^2 = \frac{V_{LSB}^2}{12 \cdot f_s} = S_{e2}^2(f) \qquad (2.7)$$

From equation (2.7) we can estimate the quantization noise in $2f_B$ after oversampling is

$$P_Q = \int_{-f_B}^{f_B} k_x^2 \cdot df = \frac{2f_B}{f_s} \cdot \frac{V_{LSB}^2}{12} = \frac{FS^2}{12 \cdot 2^{2B} \cdot OSR} \qquad (2.8)$$

In this equation, we define a parameter OSR(Oversampling Ratio) as

$$OSR = \frac{f_s}{2f_B} \qquad (2.9)$$

Finally, we can get PSNR from (2.5) and (2.8)

$$PSNR = 10 \log \left(\frac{P_{signal}}{P_Q} \right) = 6.02B + 1.76 + 10 \log (OSR) \qquad (2.10)$$

We can find that doubling OSR will increase 3dB in PSNR, it is about 0.5 bit increase

in resolution. Although oversampling can reduce quantization noise, but it is difficult to reach high SNR when use low bit quantizer. For example, if we need a 16bit A/D converter, then SNR must equal to 98dB, if the signal bandwidth is 20KHz, then the sampling rate must equal to $2 \times 10^9 \times 20\text{KHz}$, it is impossible to implement. Because at such high frequency, quantization noise is no longer a white noise, it is correlated with input signal. So there is not only oversampling technique, we must add noise shaping technique also, if we want to achieve high resolution.

2.3.2 Noise Shaping

We can model a general ΣΔ modulator and its linear model like in Fig. 2.8.

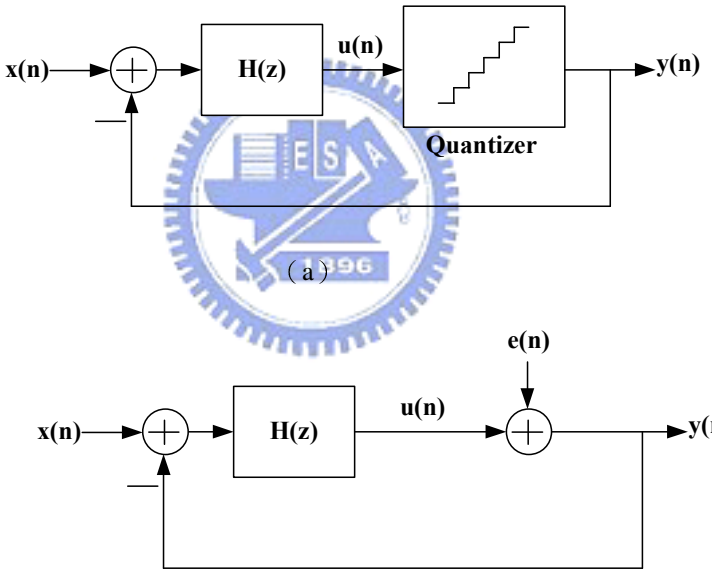


Fig. 2.8 (a)General sigma delta modulator (b) Linear model with quantization noise

From Fig. 2.8(a), we can derive output Y(z) as (2.11)

$$Y(z) = \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} E(z) \qquad (2.11)$$

and define Signal Transfer Function S_{TF} and Noise transfer function N_{TF} as

$$S_{TF}(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \qquad (2.12)$$

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \quad (2.13)$$

Where H(z) is the transfer function of a discrete time filter. There have two important meanings of (2.12), (2.13), if we want to obtain highest SNR, then S_{TF} must equal to 1, that means the input signal can transfer to output without decay; and N_{TF} (z) must equal to 0, because that the quantization noise will not affect output SNR.

In order to make N_{TF} (z) be a high pass filter, so at DC(z = 1), N_{TF} must be 0, and z = 1 is a pole of H(z), so the transfer function H(z) of the discrete filter is as

$$H(z) = \frac{1}{Z-1} = \frac{Z^{-1}}{1-Z^{-1}} \quad (2.14)$$

Substitute (2.14) into (2.12) and (2.13), we can get

$$S_{TF}(z) = \frac{1}{z} \quad (2.15)$$

$$N_{TF}(z) = 1 - \frac{1}{z} \quad (2.16)$$

And we substitute z with $e^{j\frac{2\pi f}{fs}}$, then we can plot $|S_{TF}(f)|^2$ and $|N_{TF}(f)|^2$ in frequency domain, as Fig. 2.9. We can find $|N_{TF}(f)|^2$ also increases with frequency, and $|S_{TF}(f)|^2$ is always equal to 1, if we choose signal bandwidth in low frequency, then we can get highest signal power and lowest noise power, from this figure we see that quantization noise is moved to higher frequency significantly, this is the noise shaping effect.

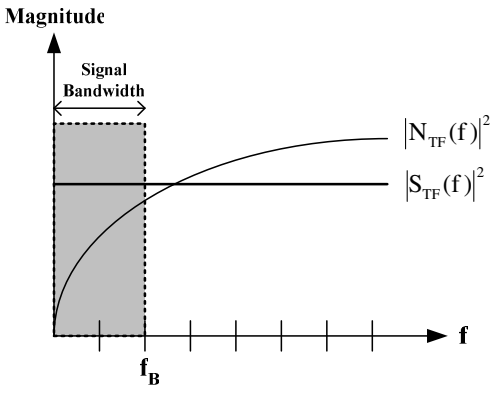


Fig. 2.9 Noise shaping

After noise shaping, we can filter out the noise in high frequency by using digital filter, we will illustrate its architecture more detail on next chapter.

3
Architectures of Sigma-Delta Modulator

Before we introduce various architectures of ΣΔ modulators, we must to realize the basic architecture of a general ΣΔ A/D converter; Fig. 3.1 is a complete block diagram of ΣΔ A/D converter[Joh 97], we can separate it into two different parts, first part is the sigma delta modulator, the main function of this part is doing oversampling and noise shaping to the input analog signal; second part is the decimation filter, main function of this part is to remove noise in high frequency and down sampling the sampling frequency to base band frequency.

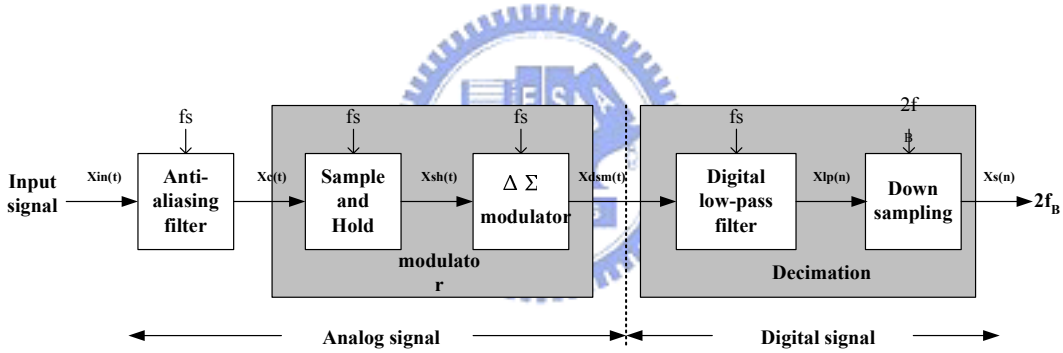


Fig. 3.1 Block diagram of sigma delta A/D converter

First, the input signal Xin(t) pass an Anti-aliasing filter, the 3dB frequency of this filter is about few times of Nyquist frequency, so signal and noise out of Nyquist frequency is filtered roughly, and this signal goes into the sigma delta modulator after goes through a S/H circuit. However, in the circuits implement situation, the sample and hold function is included in the circuits of sigma delta modulator, so the signal Xc(t) will pass this modulator and produces a high speed data code Xdsm(n), because of noise shaping, the quantization noise will appear in high frequency. Finally, we must filter the noise in high frequency and reduce the sampling frequency to Nyquist frequency by a decimator, and passes the digital signal to the output[Joh 97].

In this chapter, we will focus on the architectures of sigma delta modulator, because that the noise model and optimal method is focus on this part, we must understand the theorem, benefits and drawbacks of each kinds of sigma delta modulators. In addition, the implement of decimator is very typical[Ner 02][Mok 94]. In today's technology, DSP processors is also used to replace decimators, so we will introduce this part roughly.

3.1 First-Order Sigma Delta Modulator

We recall that H(z) in equation (2.14) is $\frac{Z^{-1}}{1-Z^{-1}}$, substitute it into Fig. 2.8, then we can get a first-order sigma delta modulator; Analyze transfer function H(z) from time-domain, it indicates that output signal m(t) is obtained by adding the delayed input signal n(t-1) and the delayed output signal m(t-1), so we can express a complete first-order sigma delta modulator as Fig. 3.2.

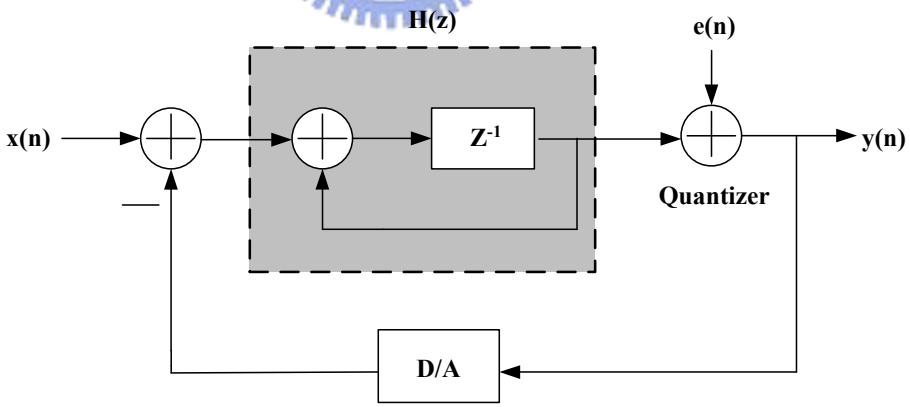


Fig. 3.2 First order sigma delta modulator

H(z) in Fig. 3.2 is indicated the effects of delay and accumulation, this is equivalent with an integrator in circuit design, so the three circuits components of sigma delta modulator are integrator, quantizer and DAC in the feedback path.

A first order ΣΔ modulator's output can represent as

$$Y(z) = z^{-1}X(z) + (1-z^{-1})E(z) \qquad (3.1)$$

From (3.1) we can find the signal transfer function is as a delay function, and noise transfer function is as a high pass filter, moves the noise to high frequency. In order to derive PSNR of first order sigma delta modulator, we must get the magnitude of $N_{TF}(z)$ and $S_{TF}(z)$ in the frequency domain, so we substitute z with $e^{j2\pi \cdot f/f_s}$, and get $|S_{TF}(f)|$ and $|N_{TF}(f)|$ respectively as:

$$|S_{TF}(f)| = |z^{-1}| = |e^{-j2\pi \cdot f/f_s}| = 1 \qquad (3.2)$$

$$N_{TF}(f) = 1 - e^{-j2\pi \cdot f/f_s} = \sin(\frac{\pi f}{f_s}) \times 2j \times e^{-j\pi \cdot f/f_s}$$

$$\Rightarrow \quad |N_{TF}(f)| = 2 \cdot \sin(\frac{\pi f}{f_s}) \qquad (3.3)$$

So the quantization noise in base band $\pm f_B$ can obtain by equation(2.7) and (3.3)

$$P_Q = \int_{-f_B}^{f_B} S_e^{\,2}(f) \cdot |N_{TF}(f)|^2 df = \int_{-f_B}^{f_B} \frac{V_{LSB}^{\,2}}{12 \cdot f_s} \cdot \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 \cdot df \qquad (3.4)$$

Because that f_B is much lower than f_s, so $\sin(\pi f/f_s)$ is approximate equal to $(\pi f/f_s)$, and P_Q is as

$$P_Q = \frac{V_{LSB}^{\,2}\pi^2}{36} \cdot (\frac{1}{OSR})^3 = \frac{FS^2 \cdot \pi^2}{36 \cdot 2^{2B} \cdot OSR^3} \qquad (3.5)$$

From (2.5) and (3.5), if we have the max. signal power, then PSNR is as (3.6)

$$PSNR = 10\log(\frac{P_{signal}}{P_Q}) = 10\log(\frac{3}{2}2^{2B}) + 10\log[\frac{3}{\pi^2}(OSR)^3]$$

$$= 6.02B + 1.76 - 5.17 + 30\log(OSR) \qquad (3.6)$$

From equation (3.6), we find that each octave of OSR, PSNR will increase 9dB, increase 1.5 bit in resolution. Compare (3.6) with equation (2.10) that only has oversampling effect; we can find that 1st order noise shaping increases the performance of sigma delta modulator.

3.2 Single Loop Second-Order Sigma Delta Modulator

When the discrete time filter in Fig. 2.8 is replaced by two cascade integrator, then it is a second order sigma delta modulator, output of the first integrator is only connecting with the input of the second integrator, it is shown in Fig. 3.3

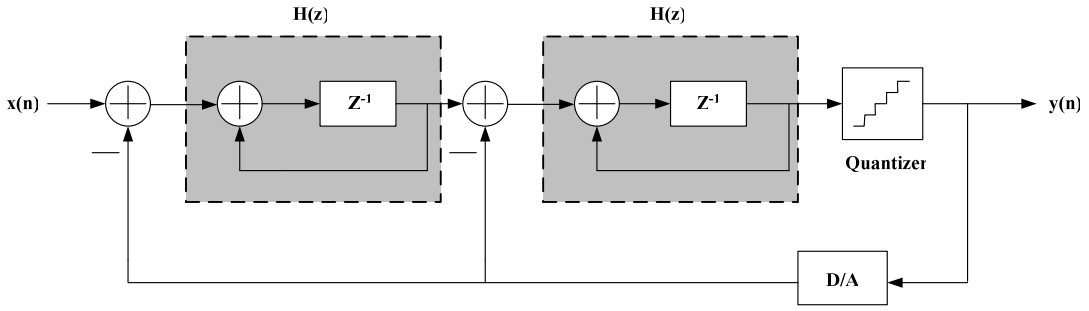


Fig. 3.3 Single loop second order ΣΔ modulator

Then the output of it can easily be derived as

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2E(z) \quad (3.7)$$

where S_{TF} and N_{TF} is as

$$S_{TF}(z) = z^{-2} \quad (3.8)$$

$$N_{TF}(z) = (1- z^{-1})^2 \quad (3.9)$$

Using the same method in (3.3) (3.4), we can obtain

$$\left|S_{TF}(f)\right| = 1 \quad (3.10)$$

$$\left|N_{TF}(f)\right| = \left[2 \cdot \sin\left(\frac{\pi f}{f_s}\right)\right]^2 \quad (3.11)$$

$$P_Q = \frac{V_{LSB}{}^2 \cdot \pi^4}{60 \cdot OSR^5} = \frac{FS^2 \cdot \pi^4}{2^{2B} \cdot 60 \cdot OSR^5} \quad (3.12)$$

So finally, PSNR of the second order sigma delta modulator is as

$$PSNR = 10\log\left(\frac{P_{signal}}{P_Q}\right) = 10\log\left(\frac{3}{2}2^{2B}\right) + 10\log\left[\frac{5}{\pi^4}(OSR)^5\right]$$

$$= 6.02B + 1.76 - 12.9 + 50\log(OSR) \quad (3.13)$$

In the single loop second order architecture, each octave of OSR can increase PSNR by 15 dB, it is equivalent to 2.5 bit in resolution. If we compare equation (3.13), (3.11) with $|NTF(f)|=1$ that without noise shaping, as Fig. 3.4, we can find that in our needed signal bandwidth, the quantization noise is highest when $|NTF(f)|=1$, and that with second order noise shaping is smallest among this figure [Joh 97].

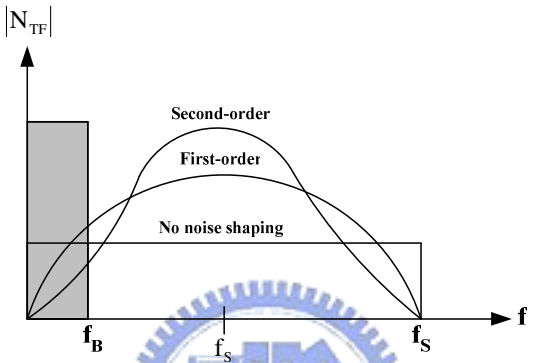


Fig. 3.4 Comparison of noise shaping techniques

3.3 Single-Loop High Order Sigma Delta Modulator

Fig. 3.5 is a single loop high order sigma delta modulator, frome the derivation in section 3.1 and section 3.2, we can get the quantization noise P_Q in signal bandwidth is as

$$P_Q = \frac{V_{LSB}^{\ 2}}{12} \cdot \frac{\pi^{2L}}{2L+1} \cdot \left(\frac{1}{OSR}\right)^{2L+1} \quad , L: \text{order} \qquad (3.14)$$

and its PSNR is

$$PSNR = 6.02B + 1.76 - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L+10)\log(OSR) \qquad (3.15)$$

In the application of high order sigma delta modulator,, (6L+3)dB increases in SNR when OSR is octave, so PSNR can be raised by increasing the order of the system, especially at large oversampling ratio. But sometimes in high order architecture, the performance will be worsen than result predicted by (3.13), because of the stability problem, it will make less effective noise shaping function, so the quantization noise will not be suppressed completely.

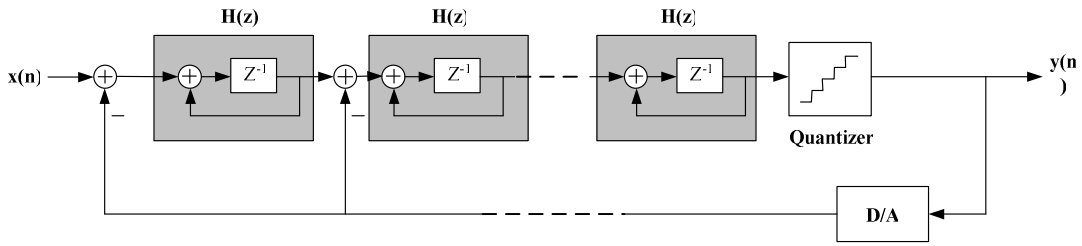


Fig 3.5 Single loop high order sigma delta modulator

3.4 Interpolative Sigma Delta Modulator

Interpolative is a kind of high order sigma delta modulator, it changes connection of some stages, adds some feedforward paths and feedback paths in order to suppose more aggressive noise shaping effect, Fig. 3.6 is a four-order interpolative architecture $\Sigma\Delta$ modulator [Cha 90].

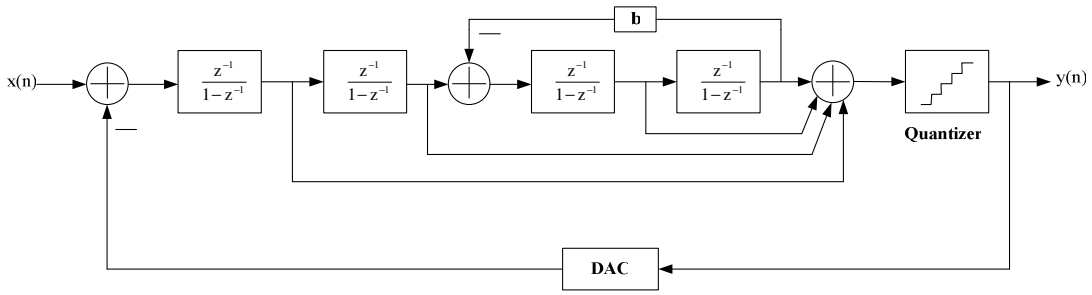


Fig. 3.6 Four-order interpolative architecture

This architecture also has stability problem, when the order L increases, each

integrator produces one pole, and when the order is higher, poles of this system will also increase, and it will cause unstable situation, so the range of integrator gain will be limited; if the range of integrator gain is small, oscillation will appear in the circuits. Another is the considerations of clock control, when we use SC (switched-capacitor) to implement the integrator, each integrator needs two clocks to control its operation, and we will need more clock to control the integrator when the order of system increases, it will produce more problems.

3.5 MASH Architecture

MASH(Multi-stAge noise SHaping) architecture is also called Cascade architecture, it is a method that cascades several low order loops modulator in order to get high order noise shaping effect. The fundamental ideal of MASH is delivering quantization noise of front stage to input of next stage, and combining the digital outputs of all the stages with proper transfer function in digital domain, only the quantization noise of last stage will appear at the output, and the orders of N_{TF} is the same with total orders in the cascade ΣΔ modulator. Fig 3.7 is a three-orders cascade ΣΔ modulator, its is the combination of a second-order and first-order ΣΔ modulator, so also called 2-1 cascade architecture[Wil 94].

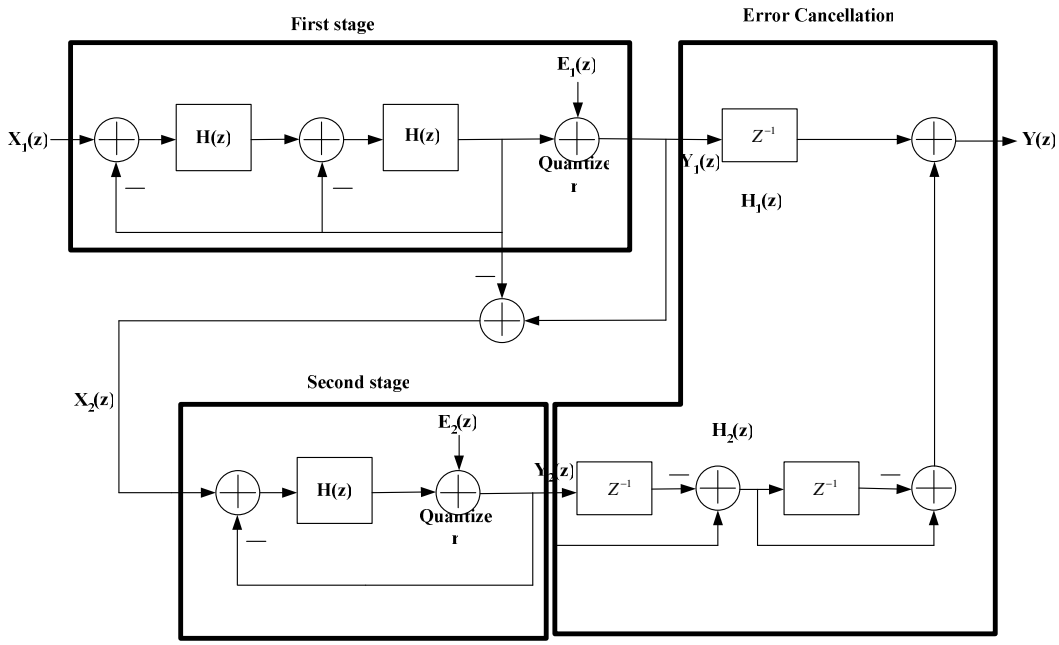


Fig. 3.7 2-1 architecture MASH sigma delta modulator

From Fig. 3.7, we can derive the first stage output $Y_1(z)$ can be represented as

$$Y_1(z) = z^{-2}X_1(z) + (1-z^{-1})^2E_1(z) \quad (3.16)$$

Output of second stage $Y_2(z)$ is as

$$Y_2(z) = z^{-1}X_2(z) + (1-z^{-1})E_2(z) \quad (3.17)$$

and overall output of MASH Y(z) is as

$$Y(z) = H_1(z)Y_1(z) + H_2(z)Y_2(z) \quad (3.18)$$

and we can say that second stage input $X_2(z)$ is almost the same with $E_1(z)$, in order to eliminate first stage quantization noise $E_1(z)$, from equation (3.16) ~ (3.18), we can define the error cancellation functions $H_1(z)$ and $H_2(z)$ as

$$H_1(z) = z^{-1} \quad (3.19)$$

$$H_2(z) = (1-z^{-1})^2 \quad (3.20)$$

From equation (3.16)~(3.20), $E_1(z)$ can be eliminated, and second stage quantization noise $E_2(z)$ is shaped by third-order noise shaping function, and the MASH output Y(z) is as

$$Y(z) = z^{-3}X_1(z) + (1-z^{-1})^3E_2(z) \quad (3.21)$$

The most significant advantage of this architecture is that stability is not an issue, because it is composed by several low-order systems, and the quantization noise will not be amplified stage by stage, so its stability is good. Most important, the noise shaping function is equivalent as high order sigma delta modulator, so it is popular in recent publications[Rio 04][Vle 01]. However, there also have some drawbacks of this topology; it is sensitive to the circuits' imperfections, such as finite DC gain of OTA, variance of integrator gain due to capacitor mismatch and non-zero switch resistance. These are all practical considerations when we design a MASH architecture sigma delta modulator[Gag 03].

3.6 Multi-bit Quantizer Sigma Delta Modulator

The demands of high resolution and high bandwidth ADC are more and more in recent years. In a high signal bandwidth, OSR of sigma delta ADC can't be too high, and the peak SNR of a sigma delta modulator with such limited OSR can't satisfy of high resolution applications, if we use higher order architecture, then the performance will degrade due to instability. So the most general method to increase performance is to use multibit quantizer. The most obvious advantage of using multibit quantizer is that the distance between quantizer level V_{LSB} in (2.4) is much smaller due to increasing of B, and according to (2.3), the power of quantization noise is attenuated. Fig. 3.8 is the results of theoretical peak SNR of sigma delta modulator versus oversampling ratio, with different order and quantizer bits, it is noted that peak SNR of the same OSR is increase 6 dB with each additional bit number in quantizer, and at low OSR, low order higher bit number architecture has equivalent performance as high order architecture. This result is usable for high bandwidth applications, and the power consumption of digital circuit in sigma delta modulator is reduced due to lower

sampling rate[Pel 99].

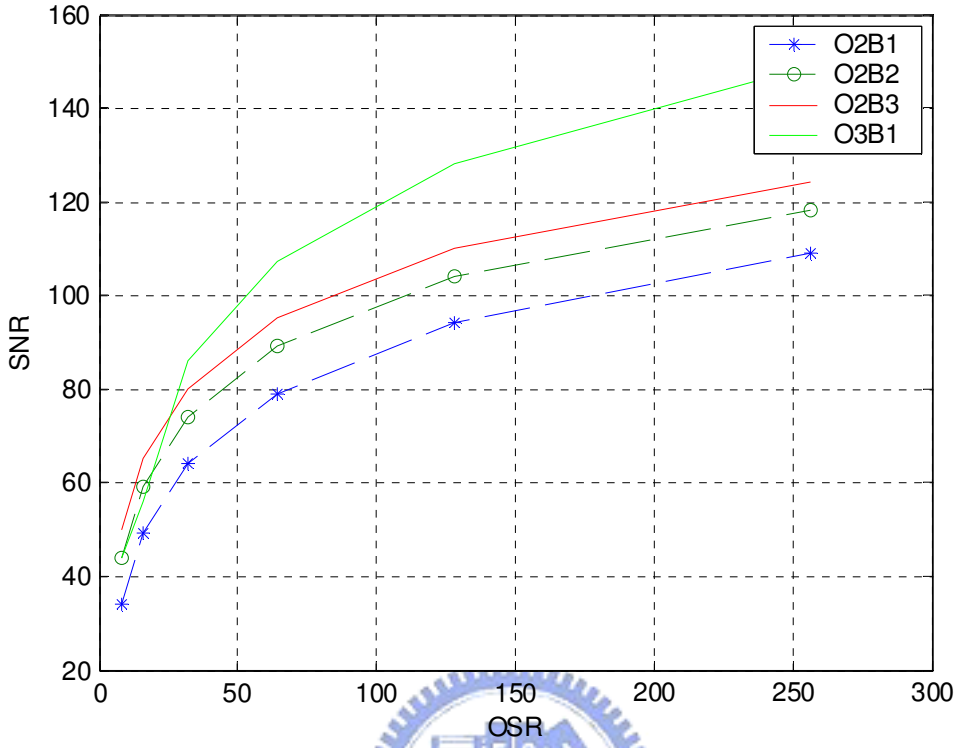


Fig. 3.8 SNR v.s. OSR with different quantizer bit number

Because of using multibit quantizer, so we also need to use multibit DAC(Digital-to Analog Converter) to transfer the digital output to analog signal, and feed it back to integrator. The most significant disadvantage is the non-linearities introduced by multibit DAC can degrade the performance of sigma delta converter, like Fig. 3.9. It is a linear model of multibit sigma delta modulator, where E(Q) and E(D) represent the quantization noise and feedback DAC noise respectively. The values of these capacitor elements in DAC will not equal to ideal values that we need, it is due to process variation, typical value of mismatch in modern CMOS technology is about 0.05% ~ 0.5%. In recent years, so many researches are make efforts on reduce DAC noise due to mismatch, such as trimming[Nor 97], Dynamic element matching(DEM)[Mil 03][Reb 90], although trimming is effective, but it has a expensive production step. So, DEM becomes more and more popular because of its

efficiency and cheaper cost.

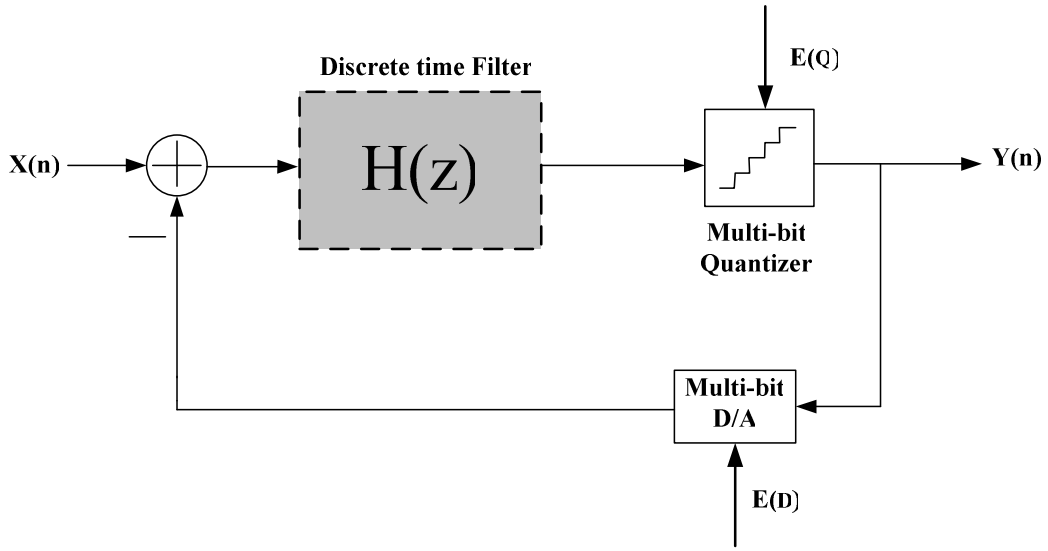


Fig. 3.9 Multibit architecture

3.7 Multibit Sigma Delta Modulator use DEM Technique

Dynamic element matching is a different approach to decrease the DAC noise, it is used to improve the linearity of pure DACs[Pla 79], but now it is most used in inner DAC of multibit sigma delta modulator. A DAC with DEM technique is illustrated in Fig. 3.10, 2^B bits thermometer code is put into the element selection logic block, and the function of element selection logic is try to select DAC elements in such way let the errors introduced by DAC average to zero for several operation periods. Because the DEM block is located in feedback loop, so its delay must be very small prevent to degrade the performance of sigma delta converter, therefore the algorithm used in the DEM block must be simple. There are several techniques of DEM, such as Randomization [Car 89], Clocked Averaging (CLA) [Pla 79], Individual Level Averaging (ILA) [Che 95], Data Weighted Averaging (DWA)[Bai 95], Randomization is the first approach to use DEM technique in sigma delta ADC, and DWA offers a good performance to reduce DAC error, in this section, an overview

introduction of these two algorithms will be presented, and the operation principle of them will be explained.

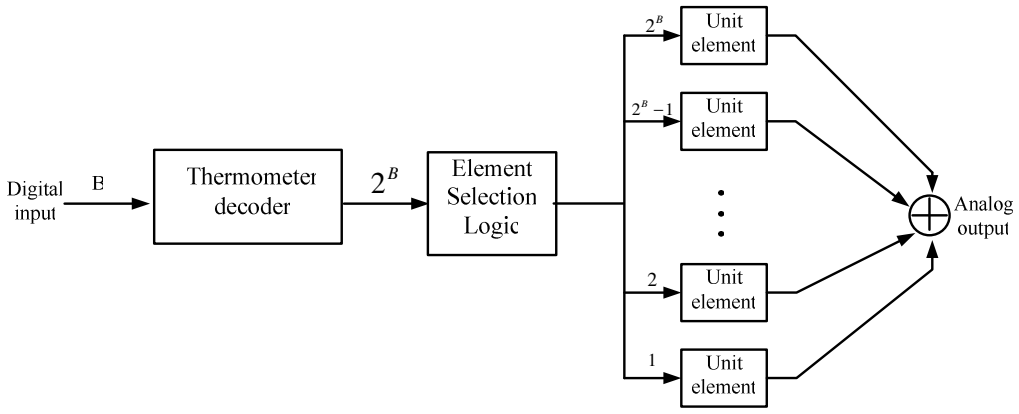


Fig. 3.10 A B-bit DAC with DEM technique

3.7.1 Randomization Technique

The main operation principle of randomization is that the element selection logic performs as a randomizer. In each clock period, the randomizer selects DAC elements randomly to generate the output of DAC. If the randomizer is ideal, then the DAC noise will become uncorrelated with each other. Simulation results show that randomization DEM technique reduce the noise floor from DAC error by several dB, but it still be a white noise in low frequency. Fig. 3.11 is the output spectrum of a second-order sigma delta modulator with a 0.1% capacitor mismatch, it is notable that the noise floor of randomization DEM is lower than that without any calibration technique in the feedback DAC.

3.7.2 Data Weighted Averaging (DWA)

DWA is a efficiently method to reduce DAC mismatch noise, it uses one register to remember the capacitor last time used, and always points to the first unused unit capacitor in this clock, so DWA rotates through all the unit capacitors such that all capacitors are used at the maximum possible rate. From this algorithm, each elements is used the same number of times in long interval, this ensures that the errors caused

by the DAC average to zero quickly. In Fig. 3.11, it is a 4-bit DAC and the shaded boxes is the number of 1's in the thermometer code. Assumes that the input codes sequence is 8, 8, 10, 9, 10, 10, 11, 11, 12, 11, 14, 11, 14, 13, 12, 15... Fig. 3.12 is the simulation results of a third order sigma delta modulator, we can see that without DEM has highest noise floor and DWA works as a first order noise shaping function of DAC noise, ideal DAC only with quantization noise has third-order noise shaping.

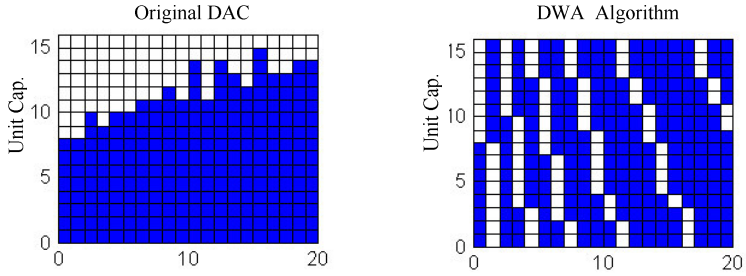


Fig. 3.11 Operation principle of the DWA algorithm

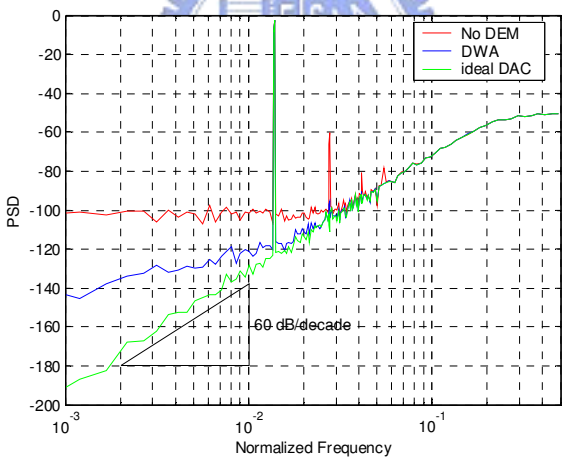


Fig. 3.12 Output spectrum with three kinds of DAC

Another consideration is the sub-ADC(quantizer) of the sigma delta modulator, we usually use Flash A/D as the multi-bit quantizer because of its high speed, but Flash A/D has a significant disadvantage is that the number of comparators of it is proportional to 2^B. That means a 6 bit quantizer needs 64 comparators, the occupied area of comparator may not much, but in modern SOC applications, the problems of

power and area are important, so it becomes one limitation of multi-bit quantization.

Sigma Delta A/D converter is attractive for high resolution application, for higher signal bandwidth, we increase system oreder to raise SNR, but it still have stability problem. So people develop MASH and multi-bit architecture to improve its performance. Finally, we classify they into low order, high order, MASH and multi-bit four kinds of architecture, and compare their advantage and disadvantage as Fig. 3.13 [Med 99]

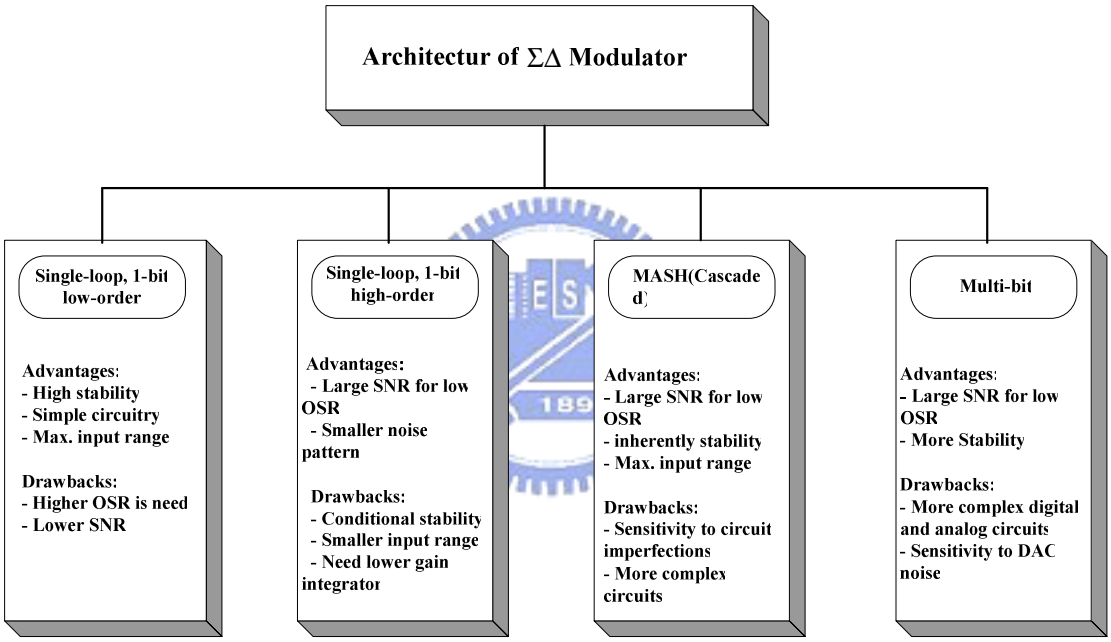


Fig. 3.13 Comparison of sigma delta modulator architectures

3.8 Decimator

In sigma delta A/D converter, digital decimator is used to process digital signal of the quantizer output, the high speed data word after oversampling modulation can't be used directly. Because there have original signal and quantization noise among it, so the main function of decimator is to convert the oversampled B-bit output words of the quantizer at a sampling rate of fs to N-bit words at Nyquist rate of input, and

removes the noise out of signal band. In order to prevent the noise introduced by other frequency, the decimator filter must have very flat signal pass-band, and sharp transition region and enough signal attenuation in stop band. Two stage decimator is used in a general situation, because that single stage decimator is difficult to convert sampling rate to Nyquist rate in 1 time and without degrading SNR. In the first stage, we can down-sample the sample frequency to 2~4 times of Nyquist frequency, and in the second stage, we can use IIR or FIR filter that have high linearity [Nor 97]. For a large OSR, multi-stage decimator is used.

3.9 Performance Metrics for a ΣΔ Modulator

In order to understand the performance merits used to specify the behavior of sigma delta modulator, several specifications concerning the performance are discussed [Gee 02].

- **Signal to Noise Ratio :** The SNR of a data converter is the ratio of the signal power to the noise power, measured at the output of the converter for a certain input amplitude. The maximum SNR that a convertercan achieve is called the peak SNR.
- **Signal to Noise and Distortion Ratio :** The SNDR of a converter is the ratio of the signal power to the power of the noise and the distortion components, measured at the output of the converter for a certain input amplitude. The maximum SNDR that a converter can achieve is called the peak SNDR.
- **Dynamic Range at the input :** The DRi is the ratio between the power of the largest input signal that can be applied without significantly degrading the performance of the converter, and the power of the smallest detectable input signal. The level of significantly degrading the performance is defined as the point where the SNDR is 6 dB bellow the peak SNDR. The smallest detectable input signal is

determined by the noise floor of the converter.

- **Dynamic Range at the output :** The dynamic range can also be considered at the output of the converter. The ratio between maximum and minimum output power is the dynamic range at the output DR_o, which is exactly equal to peak SNR.
- **Effective Number of Bits:** ENOB gives an indication of how many bits would be required in an ideal quantizer to get the same performance as the converter. This numbers also includes the distortion components and can be calculated from (2.6) as

$$\text{ENOB} = \frac{SNR - 1.76}{6.02} \tag{3.22}$$

- **Overload Level :** OL is defined as the relative input amplitude where the SNDR is decreased by 6dB compared to peak SNDR

Typically, these specifications are reported using plots like Fig. 3.14. This figure shows the SNR and SNDR of the ΣΔ converter versus the amplitude of the sinusoidal wave applied to the input of the converter. For small input levels, the distortion components are submerged in the noise floor of the converter. Consequently, the SNDR and SNR curves coincide for small input levels. When the input level increases, the distortion components start to degrade the modulator performance. Therefore, the SNDR will be smaller than the SNR for large input signals. Note that these specification are dependent on the frequency of the input signal and the clock frequency of the converter. Fig. 3.14 also shows that SNDR curves drop very fast once the overload point is achieved. This is due to the overloading effect of the quantizer which results in instabilities.

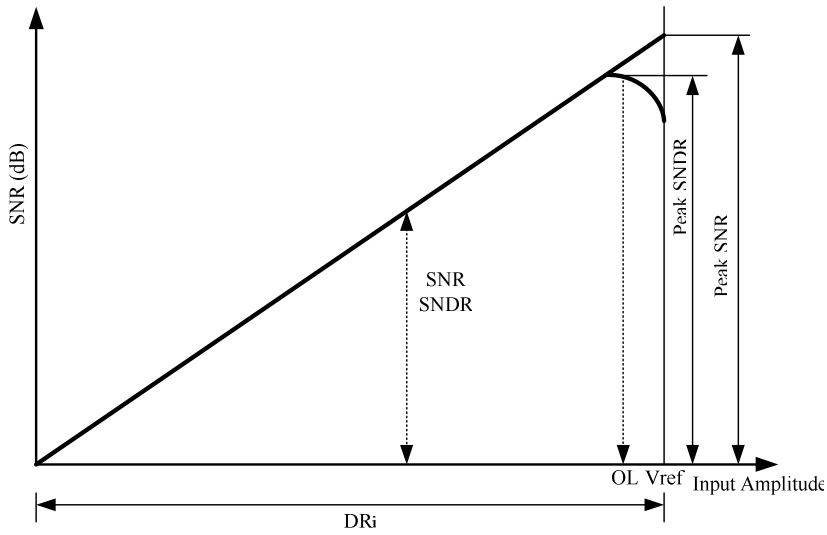


Fig. 3.14 Performance characteristic of a sigma delta converter

4

Models of Sigma-Delta Modulator Nonidealities and Power

Through fundamental analysis in previous chapter, we had come to know that the quantization noise is lowered by 6dB for each additional bit in the quantizer, and it is also lowered by $(2n+1)\cdot 3\,\mathrm{dB}$ when the OSR increases per octave, where n is the order of $\Sigma\Delta$ modulator. This situation is not available in real circuits because of several nonisealities are among sigma delta modulators, the main circuits' errors are described in this section, such as clock jitter, thermal noise and settling problem… These errors analysis in following can use in every switched-capacitor integrator of sigma delta modulator. Stability problems are out of scope in this work. Through these analyses, we can understand which circuit specification depends on which circuit non-ideality. Because of convenience, we categorize these nonidealities in four groups corresponding to the major blocks in a sigma delta modulator (see Fig. 4.1). They are: integrator nonidealities, quantizer nonidealities, DAC nonidealities, and other noise. These errors are modeled as following.

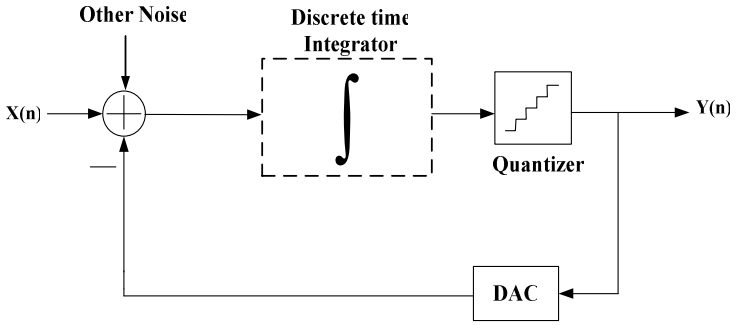


Fig. 4.1 Schematic of a generalized $\Sigma\Delta$ modulator

4.1 Models of Integrator Nonidealities

The schematic of a switched capacitor (SC) integrator is shown in Fig. 4.2, it has several components as OTA (Operational Transconductance Amplifier), MOS switches, sampling capacitor (Cs), integrating capacitor (CI), and out parasitic capacitor (CL), where $\phi 1$ and $\phi 2$ are two non-overlap clock, $\phi 1d$ and $\phi 2d$ are the delayed version of them respectively. The goal of delayed clock signal is to overcome the influence of charge injection problem [Hai 83]. The operation of a SC integrator is: when $\phi 1$ and $\phi 1d$ are ON, the sampling capacitor is charged as $\mathrm{Cs} \cdot \mathrm{Vin}$, and during another clock period, when $\phi 2$ and $\phi 2d$ are ON, the two terminal of Cs are connect with ground, so the charges are transferred to CI and redistribute on it. Hence the additional voltage of the integrator output during each clock cycle is $\frac{\mathrm{Cs}}{\mathrm{C_I}} \cdot Vin$, the evolution of the output node during the n th integration period is given by :

$$Vo(t) = Vo(nTs - Ts) + \frac{Cs}{C_I} \cdot Vin(nTs - Ts) \qquad (4.1)$$

where Ts is the period of the sampling clock, and we take z transform on both side of (4.1), then we can get the ideal transfer function of an integrator is as:

$$I_I(z) = \frac{Vo(z)}{Vin(z)} = \frac{a \cdot z^{-1}}{1 - z^{-1}} \qquad a = \frac{Cs}{C_I} \qquad (4.2)$$

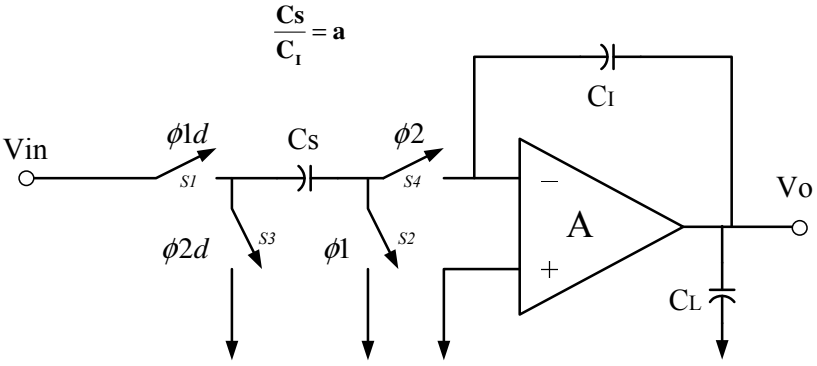


Fig. 4.2 Schematic of a switched capacitor integrator

We usually implement the integrator in the sigma delta modulator as fully

differential architecture, this helpful for increasing the input signal power, and eliminates the effects of charge injection and clock feedthrough due to MOS switch. However, it will increase the chip area and introduce more thermal noise in the system. The model of integrator nonidealities is based on single ended structure for convenience, and it is easily to extend to fully differential structure.

4.1.1 Finite OTA Gain

Finite gain of the OTA is the first nonideality we will model, the schematic of an integrator with finite gain OTA is shown in Fig. 4.2, the gain of OTA is represented as A. In this figure, we don't consider the parasitic capacitor in the OTA input, because it's value is difficult to estimate in system level, and it is vary with different process technology. By using charge conservation theory and Kirchoff's current and voltage laws, the transfer function of an integrator with finite gain is given by

$$I(z)_A = \frac{a \cdot z^{-1}}{1 - \frac{1}{A} - \frac{a}{A} - (1 - \frac{1}{A})z^{-1}} \cong \frac{a \cdot z^{-1}}{1 - (1 - \frac{1}{A})z^{-1}} \qquad (4.3)$$

From (4.3) we find that the integrator output of last period is not perfectly add to input of this period, so it will introduce some leakage in the process of integration. Then we substitute (4.3) into all single-loop architecture in chapter 3, the nth order noise transfer function of quantization noise is become

$$N_{TF}(z, A) \cong (1 - \frac{1}{A})(1 - z^{-1})^n + \frac{1}{A} z^{-(2n-1)} \qquad (4.4)$$

Then we can calculate the modified quantization noise by substitute (4.4) into equation like (3.3) and (3.4), the result is represented as [Med 99]

$$P_Q(A) \cong \frac{V_{LSB}^2}{12} \left[\frac{\pi^{2n}}{(2n+1)\mathrm{OSR}^{2n+1}} + \left(\frac{a}{A}\right)^2 \frac{\pi^{2n-2} \cdot n}{(2n-1)\mathrm{OSR}^{2n-1}} \right] = P_Q + P_{AV} \qquad (4.5)$$

The first term in (4.5) is the ideal quantization noise power, and the second term is the

additional quantization noise due to finite OTA gain. It is easily to find that the second term will disappear with infinite OTA gain, and the result is identified with ideal condition. Fig. 4.3 is the illustration of sigma delta converter output spectrum, it can be found that finite OTA gain effect will increase the noise floor in low frequency and increase the total quantization noise furthermore.

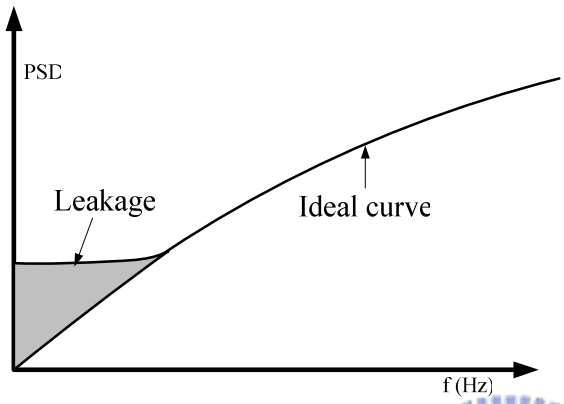


Fig. 4.3 Illustration of $\Sigma\Delta$ output Spectrum with finite OTA gain

The noise model derived in (4.4) can be used to determine the minimum OTA gain that without degrading system performance. Fig. 4.4 shows the simulation results of a single loop second order three-bit sigma delta converter for different oversampling ratio and various OTA gains. This shows that the gain of 50 dB is sufficient in order to avoid performance degradations. The required gain is increase with the oversampling ratio slightly.

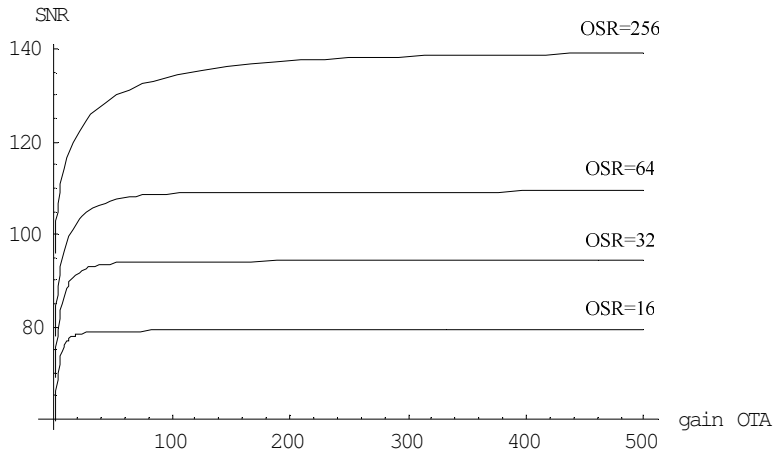


Fig. 4.4 Influence of finite OTA gain on single loop second order 3 bit system

This situation is quit different in the cascade architectures, because of its noise

cancellation logic need exact gain coefficients, so the leakage noise due to finite OTA gain will effects system severely. The detail can be seen in [Med 99]. The typical value of necessary OTA gain in MASH architecture is about 70 dB above.

4.1.2 Capacitor Mismatch in Coefficient

In a practical implementation, the gain coefficient of integrator is determined by the ratio of sampling capacitor and integrating capacitor $\frac{Cs}{C_I}$. Although it has high accuracy in modern CMOS technology, but due to process variation and error in layout process, there will have some deviation of this ratio. Then the sigma delta modulator will operate with slightly different gain coefficient with original design. We will demonstrate the influence of this nonideality. Now consider a single loop topology sigma delta modulator in Fig. 4.5, a1~an is the corresponding gain coefficient of each integrator. If we consider a 2nd order system, the capacitor ratio a1, a2 with mismatch are represented as

$$\begin{aligned} a_1' &= a_1 \cdot (1-\varepsilon_1) \\ a_2' &= a_2 \cdot (1-\varepsilon_2) \end{aligned} \tag{4.6}$$

where ε_n means the deviation from nominal coefficient gain. For convenient calculation, we assume that a1 = 0.5 and a2 = 2, and we substitute them into Fig. 4.7 to calculate noise transfer function, then it becomes

$$N_{TF}(mis.) = \frac{(1-z^{-1})^2}{z^{-2} \cdot \left(1+(1-\varepsilon_1)(1-\varepsilon_2)-2(1-\varepsilon_2)\right)-2\varepsilon_2 z^{-1}+1} \tag{4.7}$$

Let $\frac{fs}{2 \cdot f} >> 1$, and eliminate some small term, then we can obtain the magnitude of (4.7) as

$$|N_{TF}(mis.)| \cong \frac{16 f^4 \pi^4}{fs^4 [\varepsilon_2^{\,2} + (\varepsilon_1 - 1)^2 + \varepsilon_2 (4\varepsilon_1 - 2)]} \tag{4.8}$$

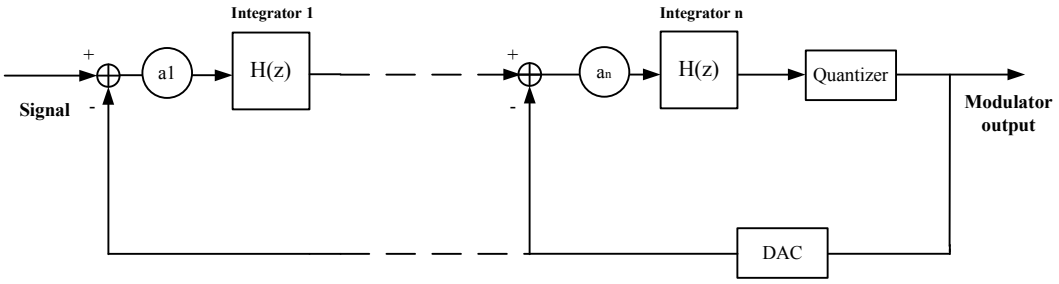


Fig. 4.5 General model of n order single-loop $\Sigma\Delta$ modulator

It can be found that the noise transfer function with capacitor mismatch is be modified, then we integrate (4.8) from –fB to fB, the modified quantization noise in the signal band becomes

$$P_Q(mis.) = \int_{-f_B}^{f_B} \frac{V_{LSB}^2}{12fs} \cdot |N_{TF}(mis.)|\, df$$

$$\cong \frac{V_{LSB}^2}{120} \cdot \frac{\pi^4}{OSR^5} \left(\frac{1}{(1-2\varepsilon_1^2)(1-2\varepsilon_2^2)} \right) \qquad (4.9)$$

Equation (4.9) will be true while OSR is large enough (>12). We can find that even with 10% mismatch in capacitor, the in band quantization noise is just 1.04 times higher than ideal case. So gain coefficient due to capacitor mismatch in single loop sigma delta modulator is not an important issue. Fig. 4.6 is the magnitude of noise transfer function versus frequency with 1% mismatch; it is a little higher than ideal case. Fig. 4.7 is the diagram of peak SNR versus mismatch, it is obtain by (4.9), it is notable that capacitor mismatch affect system performance slightly..

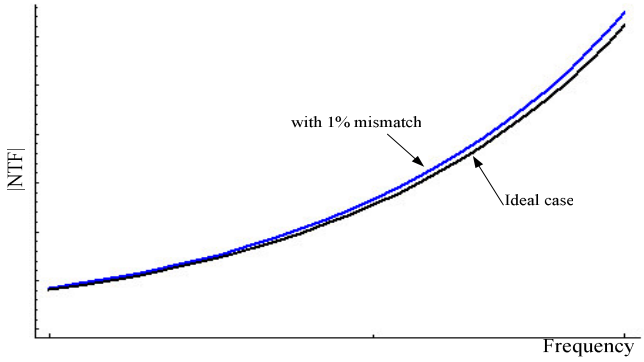


Fig. 4.6 |NTF| of a second order $\Sigma\Delta$ modulator with 1% mismatch.

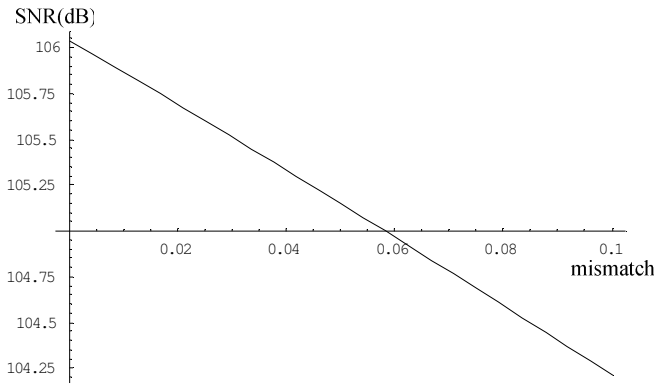


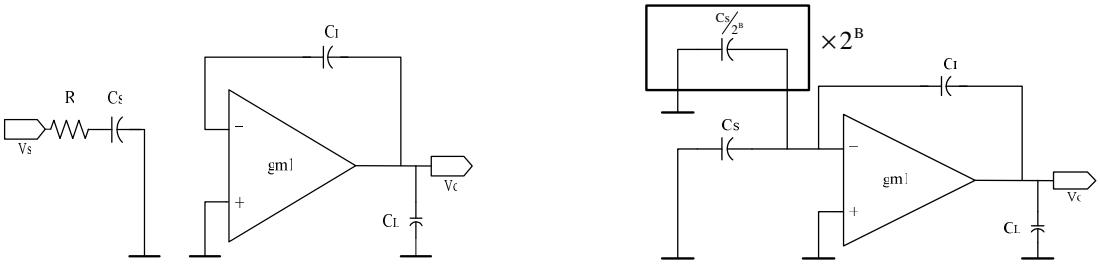
Fig. 4.7 SNR versus mismatch of a second order three-bit $\Sigma\Delta$ modulator

But when in cascade (MASH) architecture sigma delta modulator, the situation is quit different. Because the coefficients in error cancellation logic is matched with the analog coefficients that determined by capacitor ratio, small deviations in capacitor ratio results in incomplete cancellation of quantization from the first or second stage in MASH architecture. Hence the performance (SNR) of it will degrade. In [Gee 99a], the authors show that in a cascade 2-1-1 sigma delta modulator, 0.5% is the limitation of capacitor mismatch avoids degrade SNR.

4.1.3 Settling Problem

As the sampling frequency of Sigma-Delta modulators increase higher for high resolution and high speed applications, the dynamic setting problem of switched capacitor integrator in sigma delta converter becomes a more dominant factor than before. In this section, building an integrator model include switch “ON” resistance and loading capacitor in order to know how OTA finite slew rate (SR) and gain bandwidth (GBW) degrading the performance of sigma-delta modulator both on sampling phase and integrating phase. Settling problem depends on the dynamic performance of the OTA, the two most important dynamic parameters of OTA are SR and GBW, GBW is defined as the frequency at differential gain of OTA is 0 dB, and it

represents the signal change ability at small signal situation. The slew rate is defined as the signal change rate in the OTA output at large signal condition.



(a) Sampling phase (b) Integration phase

Fig. 4.8 SC integrator model with switch resistance R

In order to analyze the settling behavior both in sampling and integration phase, we consider the equivalent circuit schemes in these two phases in Fig. 4.8. In Fig. 4.8(a), assumes that switch on-resistance is R, gm1 is the transconductance of OTA input stage, output parasitic load capacitance is C_L, the voltage Vs represents the signal that difference of sinusoid input and feedback from DAC. In this phase, it is sampled at Cs, so Cs is charged to voltage like (4.10) in half clock period $\frac{T}{2}$:

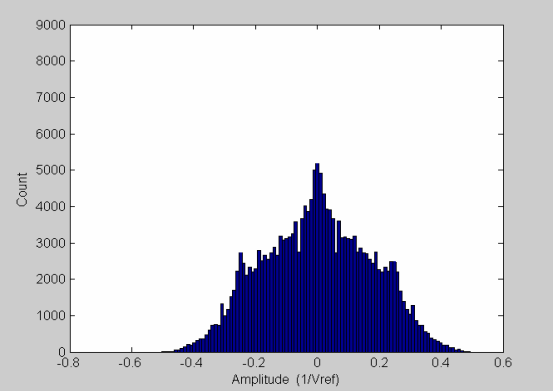
$$Vcs = Vs \cdot [1 - \exp(-\frac{T}{2 \cdot \tau 1})] \qquad (4.10)$$

where $\tau 1 = R \times Cs$ is the RC time constant in input branch. Due to this reason, the setting condition during sampling phase is depends on $\tau 1$, and we can get settling error by (4.11):

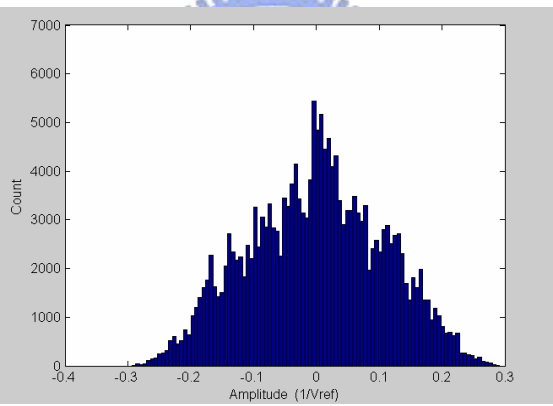
$$\delta_1 = Vs - Vcs = Vs \cdot \exp(-\frac{T}{2 \cdot \tau 1}) \qquad (4.11)$$

From (4.11), we want to obtain the average power of this noise, and then we must to know the distribution of Vs and estimate its standard deviation and variance. In order to realize its distribution, we simulate a single loop second-order $\Sigma\Delta$ modulator with $a_1 = 0.5$ and $a_2 = 2$, reference voltage $V_{ref} = \pm 1$ through SIMULINK, the voltage distribution of the first integrator input is shown in Fig. 4.9,

it is looked like Gaussian distribution, Fig. 4.9 (a) is the result with 10-level quantizer, and Fig. 4.9(b) is with 13-level quantizer, it can find that the distribution of higher quantizer levels is more concentrated on mean value, the amplitude of input signal is equal to V_{ref} . This situation is also verified in [Str 03].



(a) 10-level quantizer



(b) 13-level quantizer

Fig. 4.9 Input voltage histogram of first integrator

The standard deviation σ_{VS} of Vs with different quantizer levels are listed in Table 4.1. From this table, we observe that σ_{VS} decreases with quantizer level, this is because output voltage of the quantizer is more close to the value of input voltage, so their difference becomes smaller. In order to model the relation of B and σ_{VS}, we conclude the results in Table 4.1 and it can be approximated by

$$\sigma_{VS} \cdot 2^{B} \cong 1.4 \cdot \left| V_{ref} \right| \qquad (4.12)$$

Std. deviation (σ)	Variance	Quantizer level (N)	Bit (B)
0.706	0.498	2	1
0.476	0.227	3	1.585
0.282	0.08	5	2.322
0.198	0.04	7	2.808
0.152	0.023	9	3.17
0.124	0.016	11	3.46
0.047	0.002	31	4.95

Table 4.1

Equation (4.12) also indicates that large input amplitude, will increase the variance of Vs. From (4.11) and (4.12), the noise power spectrum of settling noise during sampling phase due to $\tau 1$ is a white noise and distributed in the range of $(-fs/2, fs/2)$, it can be expressed as:

$$S_{\delta 1} = \frac{1}{fs} \cdot \left(\frac{1.4 \cdot Vref}{2^B} \right)^2 \cdot \exp(\frac{-T}{\tau_1}) \tag{4.13}$$

and due to oversampling, the noise power can be obtained by integrating (4.13) in the baseband $(-f_B, f_B)$, the answer is:

$$P_{\delta 1} = \frac{1}{OSR} \cdot \left(\frac{1.4 \cdot Vref}{2^B} \right)^2 \cdot \exp(\frac{-T}{\tau_1}) \tag{4.14}$$

Equation (4.14) represents the settling noise in sampling phase, it is independent with the performance of OTA and is depends on the time constant obtained by switch on resistance and sampling capacitor. Too large R will affect the settling performance; it is need to notice in the switch designs.

During the integration phase of a switched-capacitor integrator, the charge store in sampling capacitor will transfer into the integrating capacitor, this charge current is supplied by OTA, so when the slew rate and gain bandwidth are not large enough, then the settling noise will be produced. Fig. 4.10 shows the evolution of the integrator output node voltage during integrating phase, its configuration is like Fig.

4.8 (b). The output voltage Vo(t) approaches to its final value Vo. For an integrator, we can represent its output node voltage during *i*th integration period as

$$Vo(t) = Vo(iT - T) + \frac{Cs}{C_I} Vs(1 - e^{\frac{-t}{\tau_2}}), 0 < t < \frac{T}{2} \tag{4.15}$$

where $\tau_2 = 1/2\pi GBW$ is the time constant of the integrator and GBW is the equivalent gain bandwidth during integration phase. The equivalent capacitor loading of an OTA during integration phase is heavier than it in sampling phase, see Fig. 4.8(b). It can easily be derived as [Gee 99a]:

$$C_{L2} = 2Cs + C_L \times \frac{C_I + (2Cs)}{C_I} \tag{4.16}$$

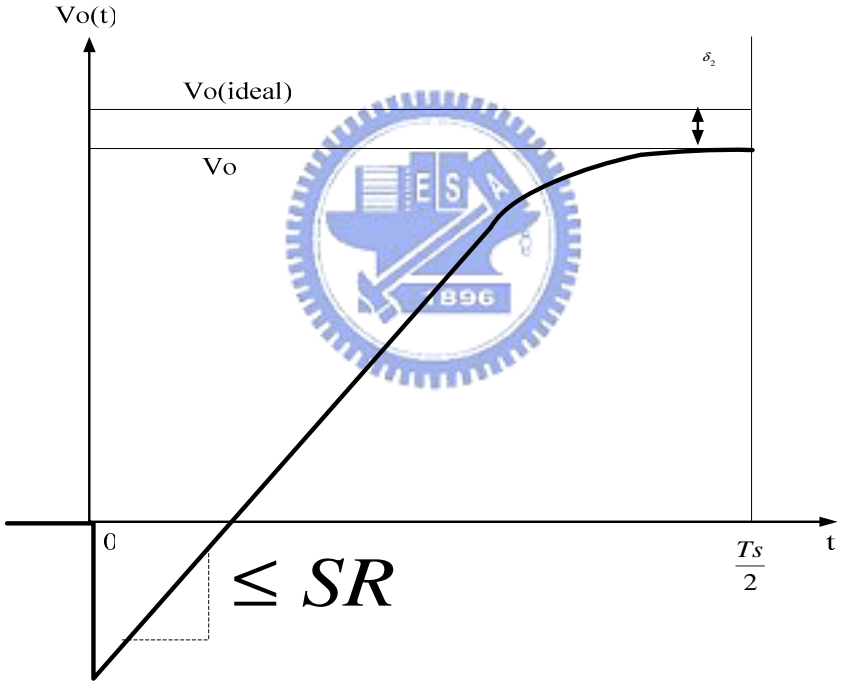


Fig. 4.10 Integrator output voltage vs. time

In order to know whether the integrator output change rate is larger than slew rate, so we must derive the slope of Vo(t) at t = 0, the result is

$$\left.\frac{\partial Vo(t)}{\partial t}\right|_{t=0} = \frac{Cs}{C_I}\frac{Vs}{\tau_2} = a\frac{Vs}{\tau_2} \tag{4.17}$$

According to (4.17), depending on the absolute value of Vs, there are three cases of settling conditions will happen in the integrator output during this phase, we assume

first integrator coefficient is a_1, the corresponding settling conditions and voltage errors are:

1. The slope in (4.17) is lower than OTA SR (slew rate), so no slew rate limitation in this case, only linear settling error is induced. The settling error δ_2 is expressed as

$$\delta_2 = a_1 Vs - a_1 Vs(1 - e^{\frac{-T}{2\tau_2}}) = a_1 |Vs| \cdot e^{\frac{-T}{2\tau_2}} \tag{4.18}$$

This condition is happened when $0 < Vs < {SR\tau_2}/{a_1}$. The distribution of Vs is verified to be a Gaussian distribution in above, so we will suppose that such error in (4.18) also presents as Gaussian distribution in the range $(-\delta_{2\max}, \delta_{2\max})$, where $\delta_{2\max}$ is the maximum value of (4.18), and it can be obtained by substituting $Vs = \frac{SR\tau_2}{a_1}$ into (4.18). Thus, the power spectrum density is a constant in the sampling frequency band, if we assume the std. deviation of (4.18) is about ${\delta_{2\max}}/{3}$, it can be calculated as

$$S_{\delta 2} \cong \frac{{\delta_{2\max}}^2}{9\,fs} = \frac{1}{9\,fs}\left(SR\tau_2 \cdot e^{\frac{-T}{2\tau_2}}\right)^2 \tag{4.19}$$

Integrating (4.19) in the signal band $(-f_B, f_B)$ results in the error power due to incomplete linear settling:

$$P_{\delta 2}(lin.) \cong \frac{1}{9OSR}\left(SR\tau_2 \cdot e^{\frac{-T}{2\tau_2}}\right)^2 \tag{4.20}$$

2. The initial change rate of Vs is larger than SR, so the OTA is slew rate limit. But it will become linear settling gradually, because the Vs change rate is bellow SR after t_0, t_0 is the time instance that Vs change rate is bellow SR. It can be obtained by the analysis in [Mal 03], the value is

$$t_0 = \frac{a_1 Vs}{SR} - \tau_2 \tag{4.21}$$

If $t_0 \leq T/2$, then the evolution of integrator output voltage is as

$$Vo(t) = SRt_0 + (a_1 Vs - SR \cdot t_0)(1 - e^{-\frac{t-t_0}{\tau_2}}) \quad t > t_0 \tag{4.22}$$

It is called partial slewing condition, and the settling error in this case can be obtained by substituting (4.21) into (4.22), and subtract it with (4.15), so the results is as

$$\delta_2 = SR \cdot \tau_2 \cdot \exp(\frac{a_1 |Vs|}{SR \cdot \tau_2} - \frac{T}{2\tau_2} - 1) \tag{4.23}$$

Equation (4.23) is happened when $SR\tau_2/a_1 < |Vs| < (T/2 + \tau_2)\frac{SR}{a_1}$, it can be obtained by (4.18) and (4.21). In order to estimate settling noise power caused by (4.23), the distribution of δ_2 in (4.23) must be obtained. Because Vs is a Gaussian distribution variable, so the distribution of (4.23) can be obtained as following analysis:

Fig. 4.11 is the Gaussian distribution of Vs, and we divided the value of Vs into three regions that corresponding to the three different settling cases. They are linear settling, partial slewing and fully slewing, the former two cases are explained above, the third case will introduced later. The occurrence probabilities of these three conditions are

$$\Pr_{lin} \cong \int_0^{\frac{SR \cdot \tau_2}{a_1}} \frac{2}{\sqrt{2\pi} \cdot \sigma_{VS}} \exp(\frac{-Vs^2}{2 \cdot \sigma_{VS}^2})\, dVs = Erf[\frac{SR\tau_2}{\sqrt{2}a_1\sigma_{VS}}] \tag{4.24}$$

$$\Pr_{par} \cong \int_{\frac{SR \cdot \tau_2}{a_1}}^{(\tau_2 + \frac{T}{2}) \cdot \frac{SR}{a_1}} \frac{2}{\sqrt{2\pi} \cdot \sigma_{VS}} \exp(\frac{-Vs^2}{2 \cdot \sigma_{VS}^2})\, dVs$$

$$= Erf[\frac{SR(T + 2\tau_2)}{2\sqrt{2}a_1\sigma_{VS}}] - Erf[\frac{SR\tau_2}{\sqrt{2}a_1\sigma_{VS}}] \quad \frac{SR\tau_2}{a_1} < 2Vref \tag{4.25}$$

$$\Pr_{ful} \cong \int_{(\tau_2 + \frac{T}{2}) \cdot \frac{SR}{a_1}}^{2 \cdot Vref} \frac{2}{\sqrt{2\pi} \cdot \sigma_{VS}} \exp(\frac{-Vs^2}{2 \cdot \sigma_{VS}^2})\, dVs$$

$$= Erf[\frac{2V_{ref}}{\sigma_{VS}}] - Erf[\frac{SR(T+2\tau_2)}{2\sqrt{2}a_1\sigma_{VS}}] \qquad (\tau_2 + \frac{T}{2})\frac{SR}{a_1} > 2Vref \qquad (4.26)$$

where $Erf[x]$ is the error function of x. From (4.25), the probability density function (p.d.f) of Vs during $SR\tau_2/a_1 < |Vs| < (T/2 + \tau_2)\frac{SR}{a_1}$ is as

$$f_{par}(vs) = \frac{1}{\Pr_{par}} \cdot \frac{2}{\sqrt{2\pi}\cdot\sigma_{VS}} \exp(\frac{-Vs^2}{2\cdot\sigma_{VS}^2}) \qquad (4.27)$$

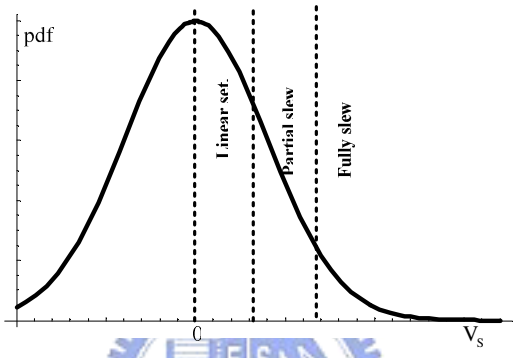


Fig. 4.11 Three types of settling conditions in integration phase

If we have the p.d.f of Vs, then the p.d.f of (4.23) is represented as [Gar 94]

$$f_{par}(\delta_2) = f_{par}(vs)\cdot\frac{dVs}{d\delta_2} \qquad (4.28)$$

where $\frac{dVs}{d\delta_2}$ can be obtained by solving (4.23), and its value is $\frac{SR\tau_2}{a_1\delta_2}$, then the average noise power of partial slewing is the autocorrelation of (4.28), and we integrating it from $\delta_2|Vs = SR\tau_2/a_1$ to $\delta_2|Vs = (\tau_2 + \frac{T}{2})\frac{SR}{a_1}$, the result is

$$P_{par}(\delta 2) = \int_{\delta_2|Vs=SR\tau_2/a_1}^{\delta_2|Vs=(\tau_2+T/2)\cdot SR/a_1} f_{par}(\delta_2)\cdot\delta_2^2 d\delta_2 \qquad (4.29)$$

3. The initial change rate of Vs is larger than SR, and $t_0 > T/2$, so the OTA is slewing during whole integration phase, the evolution of integrator output is as

$$Vo(t) = Vo(nT - T) + SR\cdot\frac{T}{2} \qquad (4.30)$$

It is called fully slewing condition, and the settling error in this case can be obtained by substituting subtract $a_1 Vs$ with (4.30), the results is as

$$\delta_2 = a_1 |Vs| - SR \cdot \frac{T}{2} \tag{4.31}$$

Equation (4.31) is happened when $|Vs| > (\tau_2 + \frac{T}{2}) \frac{SR}{a_1}$, if we want to estimate the noise power, we must do the same analysis as in last case. The p.d.f of Vs during $Vs > (\tau_2 + \frac{T}{2}) \frac{SR}{a_1}$ is

$$f_{ful}(vs) = \frac{1}{\Pr_{ful}} \cdot \frac{2}{\sqrt{2\pi} \cdot \sigma_{VS}} \exp(\frac{-Vs^2}{2 \cdot \sigma_{VS}{}^2}) \tag{4.32}$$

where $\Pr_{ful}$ is represented in (4.26). If we have the p.d.f of Vs, then the p.d.f of (4.31) is represented as

$$f_{ful}(\delta_2) = f_{ful}(vs) \cdot \frac{dVs}{d\delta_2} \tag{4.33}$$

where $\frac{dVs}{d\delta_2}$ can be obtained by solving (4.31). Then the average noise power of fully slewing is the autocorrelation of (4.33), and we integrating it from $\delta_2 |Vs = (\tau_2 + \frac{T}{2}) \frac{SR}{a_1}$ to $\delta_2 |Vs = 2V_{ref}$, the result is as

$$P_{ful}(\delta_2) = \int_{\delta_2 |Vs = (\tau_2 + T/2) \cdot SR/a_1}^{\delta_2 |Vs = 2Vref} f_{ful}(\delta_2) \cdot \delta_2{}^2 d\delta_2 \tag{4.34}$$

From (4.20), (4.29) and (4.34), the total average power of settling noise in integration phase is expressed as

$$P_{\delta 2} = \frac{1}{OSR} \cdot [P_{lin.}(\delta_2) \cdot \Pr_{lin.} + P_{par.}(\delta_2) \cdot \Pr_{par.} + P_{ful.}(\delta_2) \cdot \Pr_{ful.}] \tag{4.35}$$

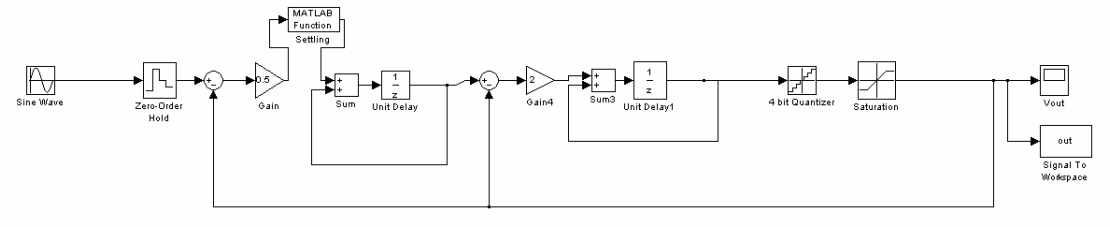


Fig. 4.12 Single loop 2nd order sigma delta ADC with SIMULINK

In order to simulate the settling noise, and compare the result in (4.35), we using SIMULINK to build a second-order $\Sigma\Delta$ modulator with 4 bit quantizer, the settling function block in [Mal 03] is used, the simulation environment is shown in Fig. 4.12. We assume that $a_1 = 0.5$, $GBW = 50MHz$, $f_B = 30kHz$ and $SR = 50 V/\mu S$. After performing FFT (Fast Fourier Transform) in the output data of sigma delta modulator, we can get the total noise power of quantization noise and settling noise, Fig. 4.13 is the noise floor of Fig. 4.12 with different oversampling ratio, the dash line is the results obtain by (4.35) and theoretical quantization noise, we find that these two lines are very close, although there have some little difference between these two lines, it is due to the distribution of Vs is not a perfectly Gaussian. This figure confirms our settling error model is reasonably precise.

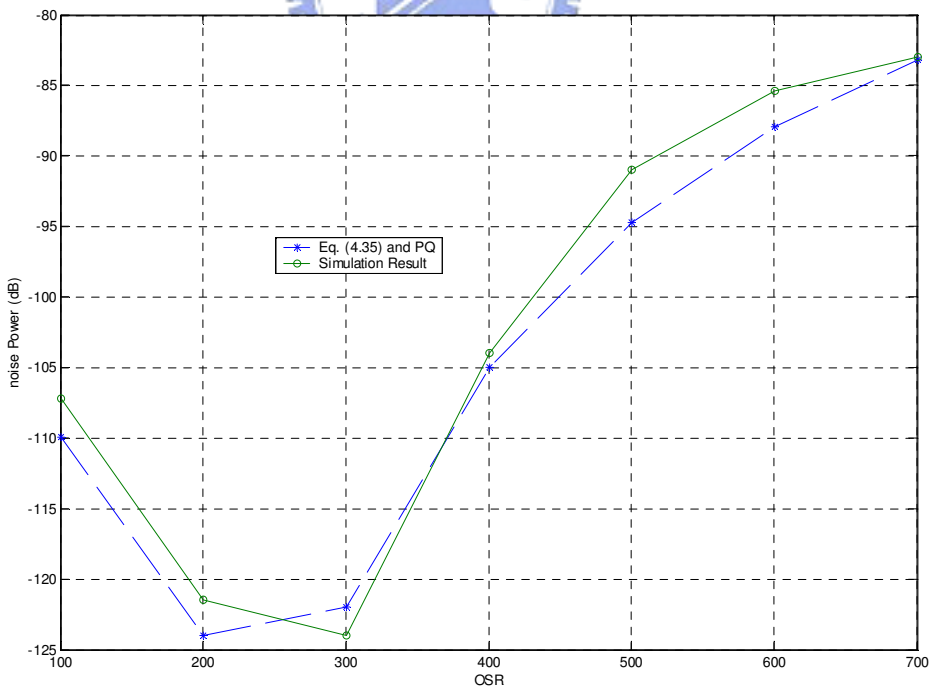


Fig. 4.13 Output settling noise floor vs. OSR

In this figure, noise floor increases when OSR is larger than 250, that means

settling error becomes dominant noise source while OSR>250, so the noise floor increase with OSR. Fig. 4.14 is the output noise spectrum while OSR = 500, it is as a white noise at low frequency, and the noise spectrum is coincide with quantization noise at middle and high frequency. Increases the values of SR and GBW will reduce this noise and increase SNR, but also increase the analog power consumption and the OTA design challenges.

Two more discussions about settling error can be found. First, because the specification of first integrator is most critical, so we only consider its effect. The gain coefficient of first integrator can be chosen smaller to lower the slew rate specification. Small gain coefficient decreases the signal amplitude when integration. Second, multi-bit quantizer also decrease the slew rate specification, because multi-bit structure make the output feedback signal is more close to input signal, so the difference voltage of input and feedback signal *Vs* will become smaller, that relaxes the slew rate specification of OTA.

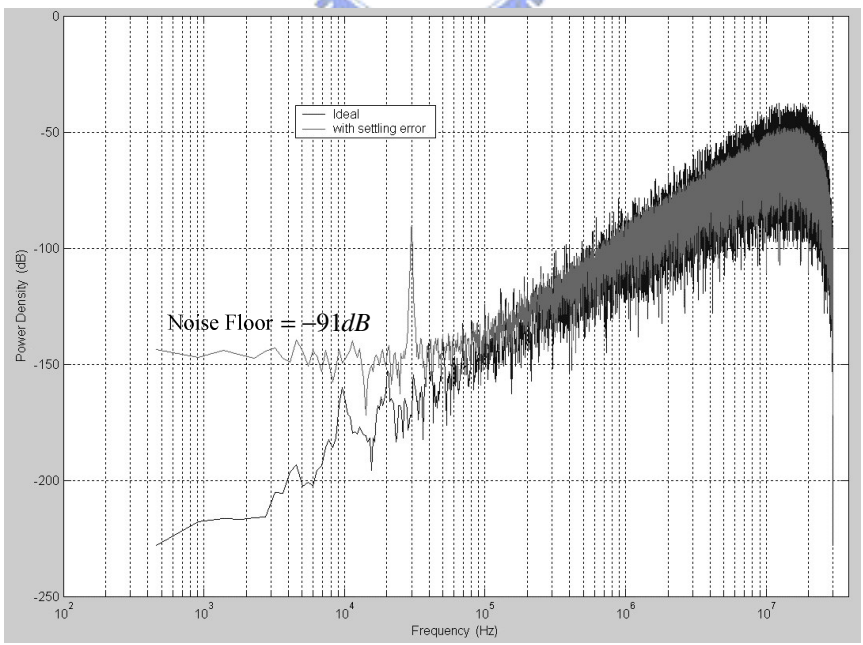


Fig. 4.14 Output noise spectrum of a 2nd order sigma delta modulator with OSR =500

4.1.4 Clock Feedthrough and Charge Injection

MOSFET switch is an important component when we implement a circuit of sigma delta modulator. Besides the OTA GBW and slew rate, the MOS switches also introduce two errors to degrade the settling performance of the integrator. They are charge injection and clock feedthrough respectively. When a switch turns off, the channel charge equals to

$$Q_{ch} = WLC_{ox}\ (V_{GS}-V_t) \qquad (4.36)$$

flows out of the channel to the source and drain, like Fig. 4.15. If these charge flowing to the input node, then that won't influence the voltage of the output node, but such assumption is not real, so the charge will flow to the output node and produces little voltage change ΔV, influences the precision of the output node, it is a severe influence for a high resolution sigma delta converter. Although using a CMOS transmission gate would have no charge injection problem since the negative charge from the NMOS cancel the positive charge from PMOS, but this is not true in practice. The reason is that the NMOS and PMOS transistors are not perfectly matched. The fraction of the charge flowing to the source and drain depends on many factors such as the impedances seen at these nodes and other reasons [Weg 87].

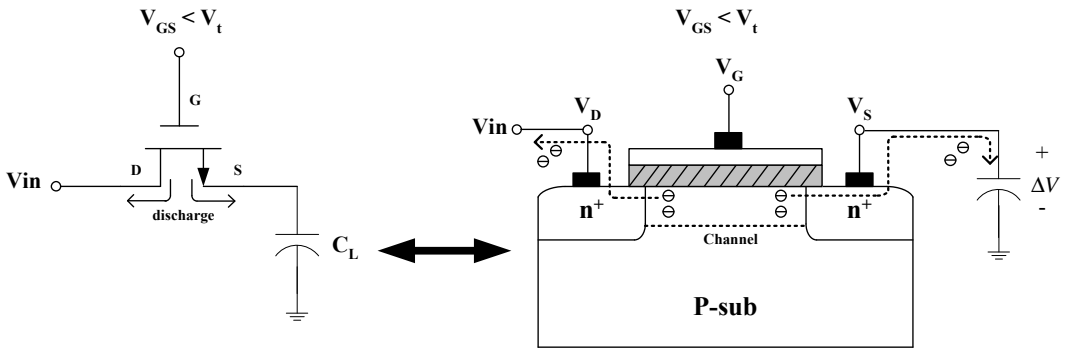


Fig. 4.15 The charge distribution when the MOS switch turns off

Another error source is clock feedthrough. Due to the overlap capacitance between the gate and source or drain regions C_{gs} and C_{gd}, when the clock signal adds to the

gate of MOS switch, the voltage in gate will coupling to the load capacitance C_L through the overlap capacitance, this effect will also produce an error at output node like Fig. 4.16. We assume that overlap capacitance C_{ov} is a constant value, then this voltage step can be expressed as

$$\Delta V = V_{CK}\frac{C_{ov}}{C_{ov}+C_L} \qquad (4.37)$$

where C_{ov} is the overlap capacitance and V_{ck} is the amplitude of the clock signal. The value of C_{ov} is proportional to the gate area, if we choose large size MOSFET, (4.37) will become severely. So the size of the sampling switches also result in the trade off between speed and precision. These two error sources can be eliminate by using fully differential implement, since that charge injection only results in a small dc-offset voltage. Another method is turning off switches S1 and S3 in Fig. 4.2 a bit after S2 and S4 have been turned off. Since this disconnects the top terminal of C_L when the charge injection takes place, the injected charge cannot be stored on C_L and therefore introduces no error.

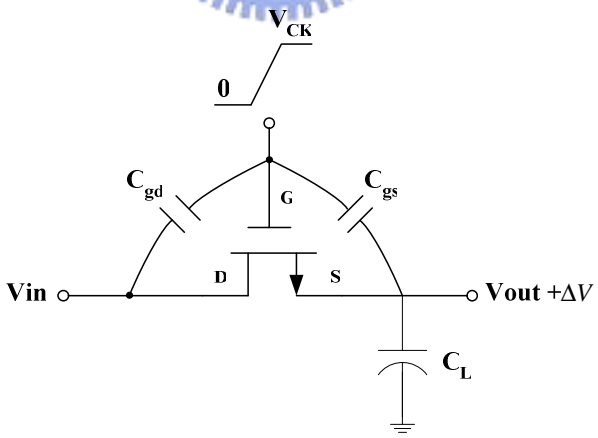


Fig. 4.16 Clock feedthrough effect

4.2 Quantizer Nonidealities

The nonidealities in the quantizer are less important than the other nonidealities of other components due to the location in the sigma delta converter. The nonidealities of

the quantizer are suppressed by the gain of the preceding integrators. In fact, they are subject to the same noise shaping action as the quantization noise. However, it will be shown to that they become a performance limiting factor in high resolution sigma delta modulators.

Since we need a high speed quantizer that without any latency, so it is implemented as a flash A/D converter that consisting of several parallels comparators and a reference ladder. The main nonidealities of quantizer consist of offset and hysteresis. Each of the parallel comparators is subjected to offset and hysteresis errors. The source of offset is from matching issue, and the hysteresis effect is due to an incomplete reset and clock feedthrough [Yin 92]. The two errors for one comparator are shown in Fig. 4.17..

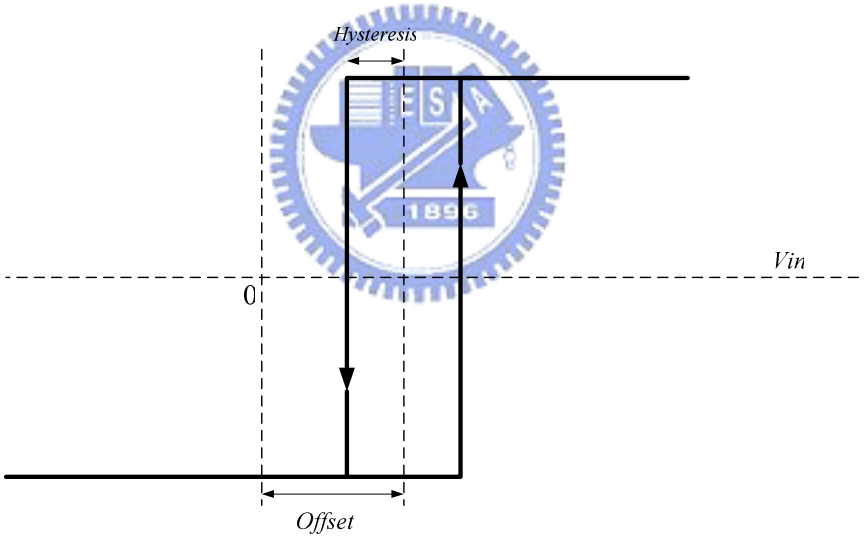


Fig. 4.17 Transfer curve of a comparator with offset and hysteresis

If we consider these two errors into behavioral simulation, the offset and hysteresis are considered as random variables, with different topologies and OSR, the SNR degradation of the sigma delta modulator can be obtained. Table 4.2 and 4.3 [Gee 99b] are the specifications with different OSR and topologies sigma delta modulator, the specification means the tolerant offset and hysteresis that only degrade SNR by 1dB. From these tables we find single bit sigma delta converters are insensitive to the

nonidealities in the quantizer. But in MASH and multibit topologies, the situation is quit different. In these architecture sigma delta modulators, the designer must design the quantizer more carefully. The offset error can be reduced by using large size input transistor of the comparator, but it will also result in large input capacitance. Multi-bit quantizer has several parallel comparators which increases input capacitance even further. So the settling performance of last integrator will degrade.

OSR	8	16	32	64	128
O2B1	*> 500*	*> 500*	*> 500*	*> 500*	*> 500*
O2B2	*40*	*10*	*10*	*4*	*6*
O2B3	*10*	*7*	*7*	*5*	*4*
O2B4	*7*	*3*	*4*	*2*	*0.5*

Table 4.2：Tolerant comparator offset(mV) for different OSR and topologies

OSR	8	16	32	64	128
O2B1	*40*	*40*	*70*	*70*	*90*
O2B2	*30*	*20*	*40*	*50*	*40*
O2B3	*50*	*20*	*20*	*30*	*40*
O2B4	*20*	*20*	*8*	*8*	*6*

Table 4.3：Tolerant comparator Hysteresis(mV) for different OSR and topologies

4.3 Models of DAC Nonidealities

The DAC in the feedback loop of the sigma delta converter also introduced nonidealities. Fig. 4.18 shows the implementation of the multi-bit DAC in the switched capacitor integrator. The nonidealities sources are from the unit capacitors. The main important problem of the unit capacitors are the variation of their values. The position of the DAC is located in the feedback loop of the converter, so the matching deviations degrade the performance easily.

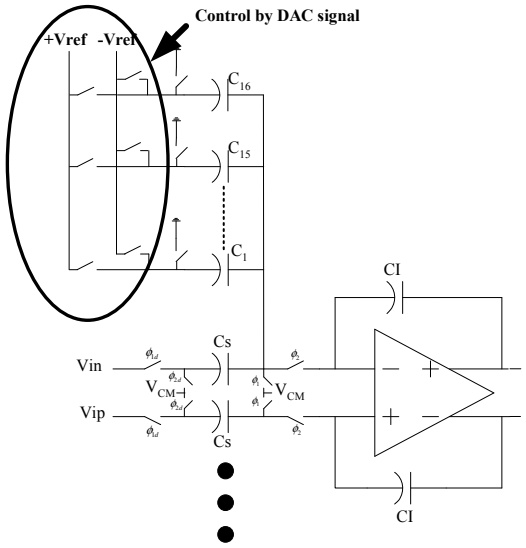


Fig. 4.18 Implementation of the 4-bit DAC

In general, a B-bit DAC inside a sigma delta converter is composed of 2^B unit capacitors. Each of these capacitors is used to generate a positive or negative feedback signal, so the contributions of all capacitors are summed to construct the feedback signal for the converter. Due to process variations, the values of these capacitors will not be equal to the wanted value and the DAC will introduce errors. If we assume the distribution of these capacitor weights is Gaussian, the normalized capacitance be

$$c_k = \frac{C_k}{\sum_{i=1}^{2^B} C_i} \quad , \qquad 1 \le k \le 2^B \tag{4.38}$$

where C_k is the capacitance of each unit capacitor. Define the deviation of c_k as $e_k = c_k - c_m$, where

$$c_m = \frac{\sum_{k=1}^{2^B} c_k}{2^B} \tag{4.39}$$

The selection of the unit capacitor in the DAC is determined by a thermometer code. We let $x(n)$ be the number of capacitors that need to contribute positively, so total $x(n)$ capacitors are summed and the other capacitors are subtracted to generate the DAC output value [Gee 02].

$$V_{dac}(n) = V_{ref}\left(\sum_{k=1}^{x(n)} c_k - \sum_{k=x(n)+1}^{2^B} c_k\right) \tag{4.40}$$

so the voltage error caused by the unit capacitor mismatches is given by

$$V_{dac,id}(n) - V_{dac}(n) = V_{ref}\left(\sum_{k=1}^{x(n)} c_m - \sum_{k=x(n)+1}^{2^B} c_m\right) - V_{ref}\left(\sum_{k=1}^{x(n)} c_k - \sum_{k=x(n)+1}^{2^B} c_k\right)$$

$$= V_{ref}\left(\sum_{k=1}^{x(n)} e_k - \sum_{k=x(n)+1}^{2^B} e_k\right) = e_{dac}(n) \tag{4.41}$$

A general model of a multi-bit sigma delta converter with a nonideal DAC in the feedback loop can be modeled as an ideal DAC, followed by an additive error source, it is shown in Fig. 4.19. The error e_{dac} is given by (4.41) and equals to the difference between the output of nonideal DAC and ideal DAC. We can find that the first DAC's nonidealities will appear directly at the output, without shaped by the loop, so the first DAC is the most important DAC in the feedback loop.

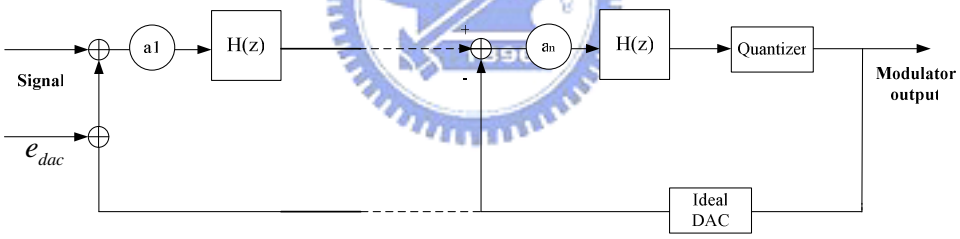


Fig. 4.19 A nth-order multi-bit sigma delta converter with the nonideal DAC

We want to estimate the average DAC noise caused by e_{dac}, suppose that the variance of e_k is given by $\sigma_{cap.}^{\ 2}$, the value of $\sigma_{cap.}^{\ 2}$ depends on the process of capacitance. The variance of equation (4.41) must calculated as

$$\sigma_{dac}^{\ 2} = V_{ref}^{\ 2} \cdot \left(x(n) \cdot \sigma_{cap.}^{\ 2} + (2^B - x(n)) \cdot \sigma_{cap.}^{\ 2}\right) = V_{ref}^{\ 2} \cdot 2^B \cdot \sigma_{cap.}^{\ 2} \tag{4.42}$$

This noise power is direct added to the output of the sigma delta converter, suppose that the input values of the DAC from 1 to 2^B have the same probability equal $1/2^B$, so the DAC noise power without noise shaping is as

$$P_{dac} = \frac{1}{OSR} \cdot V_{ref}{}^{2} \cdot 2^{B} \cdot \sigma_{cap.}{}^{2} \tag{4.43}$$

From (4.43), we can know that DAC noise power is like a white noise at low frequency and also proportional to quantizer bit B and variance of unit element matching, but it can be suppressed by using high oversampling ratio. So when B is increase, this noise will be raised. The distribution of e_{dac} versus each input thermometer code with 3 bit (8 levels) quantizer is shown in Fig. 4.20, e_{dac} is the same at every input code. Note that in a one bit sigma delta converter, this noise is not an issue since a one-bit DAC only contains two different levels and it is intrinsically linear.

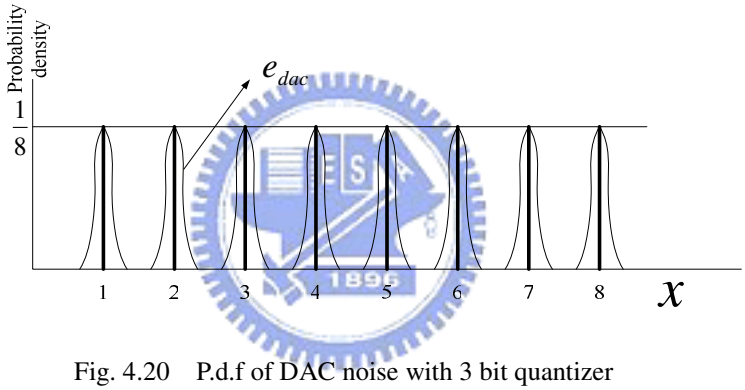


Fig. 4.20 P.d.f of DAC noise with 3 bit quantizer

To reduce the matching requirements of the unit capacitors, different techniques are introduced. Dynamic element matching (DEM) is a common used technique, there have several algorithms for DEM, such as randomize [Car 89], ILA [Che 95], CLA and DWA. In contrast to the other technique, DWA algorithm selects all the DAC elements cyclically and is the most efficient algorithm, detail operation of DWA is shown in chapter 3. The analysis shown bellow in order to show the DWA algorithm result in a first order noise shaping effect and we can use that result to estimate the DAC noise power in the SNR equation when the DWA algorithm is used.

We let ptr(t) be the pointer position which addresses the selected unit capacitor at clock time (t). According to the operation principle of DWA, we can say that at each

clock cycle, this pointer is incremented modulo quantizer level N by the input code [Nys 96]:

$$\text{ptr(t)=ptr(t-1)} + \ x(n) \qquad \text{mod} \quad \text{N} \tag{4.44}$$

where $x(n)$ is the number of 1's of input thermometer code, the mismatch error at time t can also be expressed as

$$e_{dac}(t) = \sum_{k=ptr(t-1)}^{ptr(t)} c_k - x(n) \cdot c_m \tag{4.45}$$

In order to illustrate that this mismatch is suffered from first order noise shaping, we define a function of the accumulated mismatch error as

$$\text{IM(ptr(t))} = \sum_{k=1}^{ptr(t)} (c_k - c_m) \tag{4.46}$$

From (4.46), the equation (4.45) can also be rewritten as

$$e_{dac}(t) = \text{IM(ptr(t))} - \text{IM(ptr(t-1))} \tag{4.47}$$

We find that $e_{dac}(t)$ can be represented as first order differentiation of a function of IM(ptr(t)), and (4.47) can be written in Z-domain into the form

$$E_{dac}(Z) = (1 - Z^{-1}) \cdot IM(ptr(Z)) \tag{4.48}$$

In (4.48), it shows that the mismatch error will be suppressed by DWA with a first order noise shaping. The value of $IM(ptr(Z))$ is the autocorrelation function of mismatch error and it is equal to equation (4.42), so the total mismatch noise power at the sigma delta converter output while using DWA algorithm is as

$$P_{dac}(DWA) = \int_{-f_B}^{f_B} \frac{P_{dac}}{fs} \cdot \left|(1 - Z^{-1})\right|^2 df$$

$$\cong \int_{-f_B}^{f_B} \frac{P_{dac}}{fs} \cdot \left|\frac{j2\pi \cdot f}{fs}\right|^2 df = {V_{ref}}^2 \cdot 2^B \cdot {\sigma_{cap.}}^2 \cdot \frac{\pi^2}{3 \cdot OSR^3} \tag{4.49}$$

Equation (4.49) will be used to estimate the DAC noise power in the optimization process. Noise shaping technique such as DWA significantly reduces the mismatch noise of the DAC, while the complexity of the digital hardware will increase. But it

shows that DEM techniques are suitable for high speed and high resolution sigma delta converter. The block diagram of a nth order sigma delta converter with DEM is shown in Fig. 4.21, and the corresponding output spectrum is illustrated in Fig. 4.22, quantization noise is suffered from nth order noise shaping, and the DAC noise is suffered from first order noise shaping.

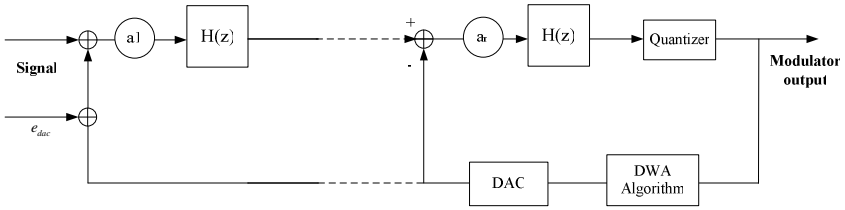


Fig. 4.21 A *n*th order sigma delta converter with DWA calibration

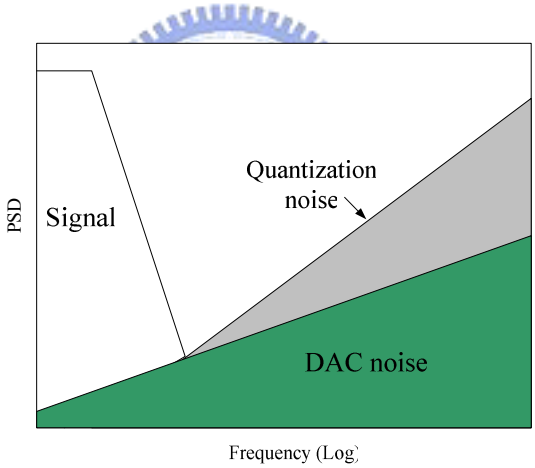


Fig. 4.22 Corresponding output spectrum of Fig. 4.21

4.4 Models of other Noises

The quantization noise is not the only noise source that can limit the maximum SNR of the sigma delta converter. In a practical circuit implementation, several noise sources will appear such as jitter noise and thermal noise. These noises are caused by the clock generator, MOS switches, the OTAs and the reference voltage circuit. The contribution of these noises is analyzed in this section.

It is easily to show that the noise of the first integrator is suppressed by $\frac{1}{OSR}$, so the input referred noise of the first integrator cannot distinguish from input signal, and it is severest. The contribution of the second integrator noise is suppressed by $\frac{\pi^2}{3OSR^3}$, for a 64× OSR, this corresponding to a 49dB noise reduction relative to the first integrator. So the noise from the first integrator is the dominant circuit noise source in the sigma delta converter.

4.4.1 Clock Jitter Noise

Signal bandwidth and resolution of $\Sigma\Delta$ converter are climbed up today, so clock jitter becomes a difficult challenge and becomes an important issue when we discuss the models of nonidealities. Jitter is usually defined as a random variation in clock signal period around the ideal value, see Fig. 4.23, and we suppose that the value of jitter is as a Gaussian random variable with zero mean and standard deviation $\sigma_{jit.}$. Even if the on-chip sampling circuitry is ideal, the jitter will be introduce by the external clock source, mainly due to the device thermal noise and the Power/Ground substrate noise of PLLs (Phase Locked Loops) and CMOS oscillators, the detailed formulation reason of jitter cause by these circuits are shown in [Her 99] [Hey 04].

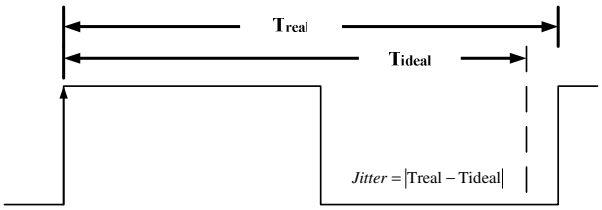


Fig. 4.23 Illustration of Clock Jitter

Now we want to show the impact of clock jitter on $\Sigma\Delta$ modulator, see Fig. 4.2. If an input analog signal is be sampled by clock ϕ_1, if there has some variation in clock high time, the input signal will be sampled at wrong instant and get a voltage error

consequently. Let a sinusoidal input signal with maximum amplitude A_i and frequency f_{in}, it is sampled by a clock which has jitter variation, then the voltage error is as:

$$\Delta V \cong 2\pi \cdot f_{in} \cdot A_i \cos(2\pi \cdot f_{in} \cdot t)\Delta T \qquad (4.50)$$

where ΔT is the variation of clock period [Bos 88]. Furthermore, we can derive jitter noise power now; because sampling voltage error is a white noise spectrum spread over $(\pm fs/2)$ and also suffer from oversampling effect. So the jitter noise power becomes:

$$P_{jitter} = \frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} (\Delta V)^2 dt = \frac{(2\pi \cdot f_{in} \cdot A_i)^2}{2} \cdot \frac{\sigma_{jit.}^{\ 2}}{OSR} \qquad (4.51)$$

$$= \frac{(2\pi \cdot f_B \cdot V_{ref})^2}{2} \cdot \frac{\sigma_{jit.}^{\ 2}}{OSR} \qquad \text{(worst case)} \qquad (4.52)$$

The worst case in (4.52) is that f_{in} is equivalent to signal bandwidth f_B, and the input signal amplitude is equal to the reference voltage, from (4.52) it is notable that the jitter noise becomes severer when we use high input frequency and large input amplitude. The tolerant jitters of a second order system with 100× OSR that avoid to degrade SNR by 3dB, are 15pS and 30pS for f_{in} = 300 kHz and 150 kHz respectively. If f_{in} is fixed, then according to (4.52), this noise is proportional to reciprocal of OSR.

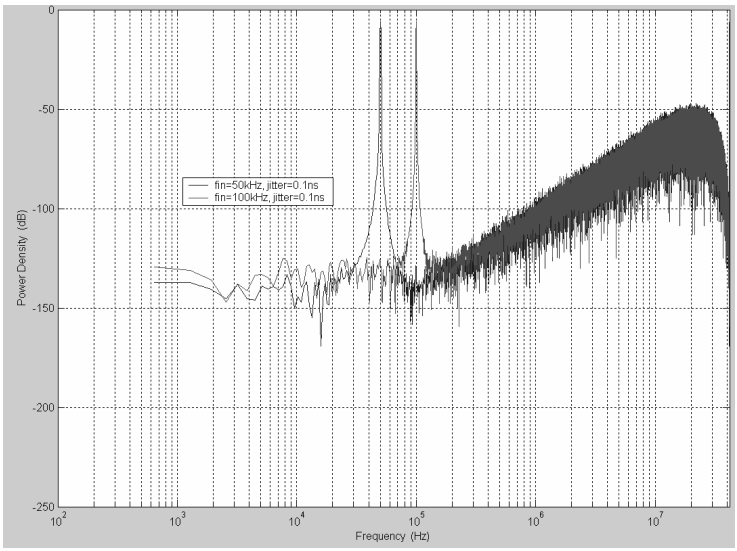


Fig. 4.24 Output spectrum of a jittered system with different input frequency

Fig. 4.24 shows the output spectrum for a jitter sigma delta converter with two different input frequency and $\sigma_{jit.} = 0.1ns$, it is notable that the noise floor in low frequency region of 100kHz input is higher than it of 50kHz input signal.

4.4.2 Thermal Noise of Switches, OTAs and Refence Voltage

Thermal noise will appear in the devices such as resistors and MOSFETs, but they have the same fundamental theory. Thermal noise in resistor is due to that the random motion of electronics in a conductor introduces fluctuations in the voltage measured across the conductor even if the average current is zero. The phenomenon is called thermal noise. Thus, the spectrum of thermal noise is proportional to the absolute temperature [Raz 01]. Fig. 4.25 shows the thermal noise of a resistor R can be modeled as a voltage source, and its one-sided spectrum density is as

$$S_R(f) = 4KTR, \qquad f \geqq 0 \qquad (4.53)$$

Where K = 1.38 × 10-23 J/K is the Boltzmann constant and T is the absolute temperature.

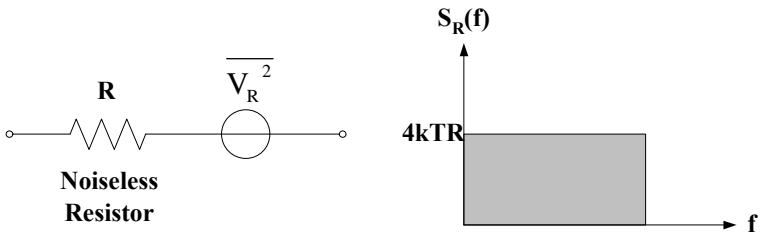


Fig. 4.25 Resistor thermal noise model and its PSD

$S_R(f)$ is expressed in V^2/Hz, thus we can also write

$$\overline{V_R^2} = 4kTR \qquad (4.54)$$

It is helpful for analyzing noises in the circuits if we assume it as a voltage source. Fig. 4.26 is a simple S/H circuit; and we often use NMOS, PMOS or CMOS to implement the switches. Because the MOSFET is a voltage control device, so we can control its ON and OFF by the voltage of gate. So when the switch is ON, we can model it as a finite resistor R, as Fig. 4.27. In general, CMOS switches are common used, because its on resistance is equal to the parallel resistance value of PMOS and NMOS, so the resistor value of CMOS can be minimize and more linear.

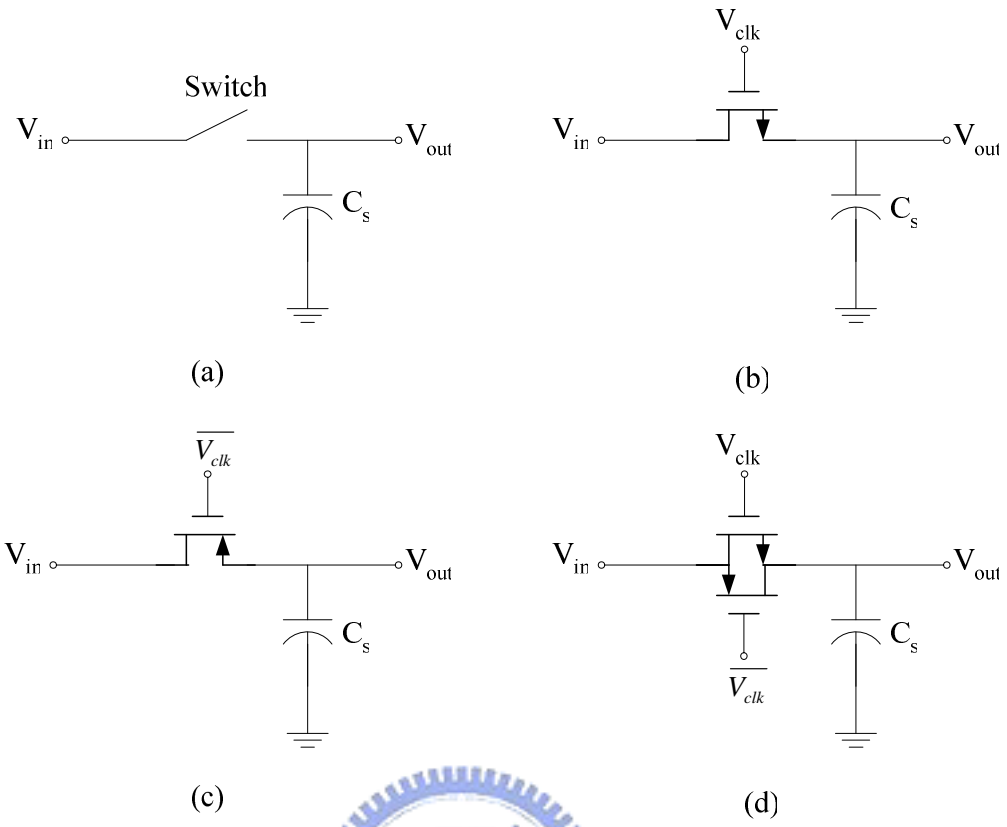


Fig. 4.26 (a)S/H circuit (b) NMOS switch (c) PMOS switch (d) CMOS switch

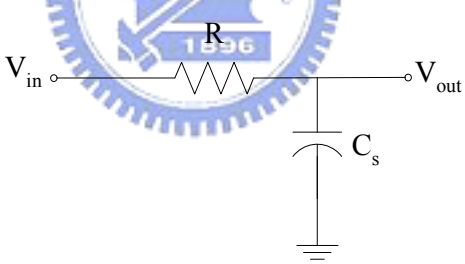


Fig. 4.27 Finite resistance model of a switch

We use equation (4.54) to Fig. 4.27, and then we can get a sampling circuit with a noise voltage source series with the resistor. In order to get the noise power across the sampling capacitor in Fig. 4.27, we suppose that Vin is connected to ground and ignore its effect as Fig. 4.28 shows.

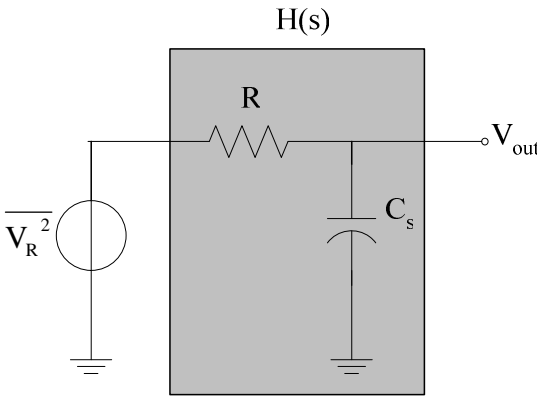


Fig. 4.28 A sampling circuit with noise source

The transfer function of H(s) in Fig. 4.28 is given by

$$H(s) = \frac{V_{out}}{V_R}(s) = \frac{1}{1 + sRC_s} \qquad (4.55)$$

The output spectrum density $S_{out}(f)$ is obtained by input spectrum density $S_R(f)$ pass H(s), it is given by

$$\begin{aligned} S_{out}(f) &= S_R(f)\left|H(j2\pi f)\right|^2 \\ &= 4kTR\frac{1}{1 + 4\pi^2 R^2 C_s^{\ 2} f^2} \end{aligned} \qquad (4.56)$$

From (4.56), we can know that the output spectrum $S_{out}(f)$ is the results of the input white spectrum $S_R(f)$ pass through a lowpass filter, and the output noise power P_{out} is as

$$\begin{aligned} P_{out} &= \int_0^{\infty} \frac{4kTR}{4\pi^2 R^2 C_s^{\ 2} f^2} df \,, \quad \text{Let } u = 2\pi RC_s f \\ &= \frac{2kT}{\pi C_s} \tan^{-1} u \,|_{u=0}^{u=\infty} \\ &= \frac{kT}{C_s} \end{aligned} \qquad (4.57)$$

We only consider one sampling circuit condition in the above analysis, but there have many switches in a sigma delta modulator, each switch can modeled as Fig. 4.28. We must consider the output noise in a multi sampling circuits. Fig. 4.29 is a two branches sampling circuits.

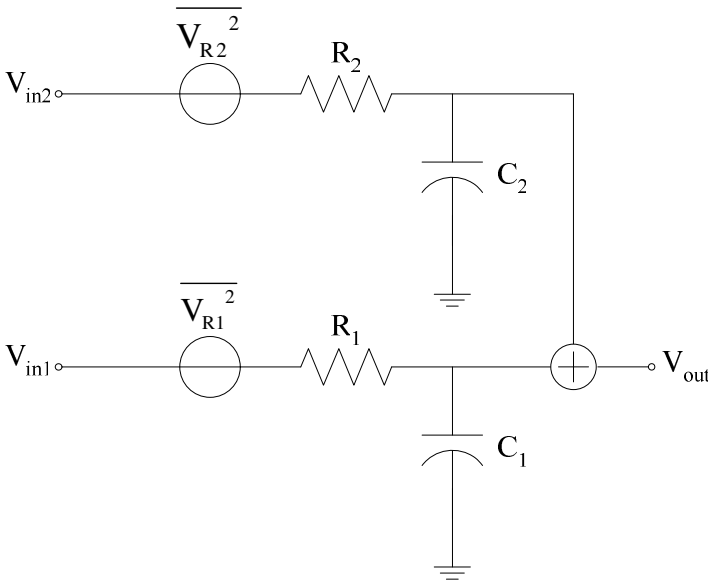


Fig. 4.29 Multi-branches sampling circuit

According to the results in (4.57), the output noise power P_{out1} and P_{out2} is given by

$$P_{out1} = \frac{kT}{C_1} \qquad (4.58)$$

$$P_{out2} = \frac{kT}{C_2} \qquad (4.59)$$

Because (4.58) and (4.59) are uncorrelated noise, so the total output noise power can be represented as

$$P_{out} = P_{out1} + P_{out2}$$

$$= kT\left(\frac{1}{C_1} + \frac{1}{C_2}\right) \qquad (4.60)$$

According to (4.60), we can prove that if there has M branches RC sampling circuits, and the total output noise power can be represented as

$$P_{node} = \sum_{i=1}^{M} \frac{kT}{C_i} \qquad (4.61)$$

The result in (4.61) is helpful to estimate the input sampling noise power in a multi-bit sigma delta converter.

Fig. 4.30 is the equivalent circuit schematic of a integrator in the sigma delta modulator during sampling phase, we replace the switches by finite resistances R, and assume the number of quantizer is B, so the number of unit capacitors is 2^B, and

capacitor value is $\frac{Cs}{2^B}$. If we add the switch thermal noise in Fig. 4.30, then the circuit will become as Fig. 4.31. So the switch thermal noise power during sampling phase in the input branch can be calculated by the above method and its value is

$$P_{sw1}(Cs) = \frac{\mathrm{kT}}{\mathrm{Cs}} \tag{4.62}$$

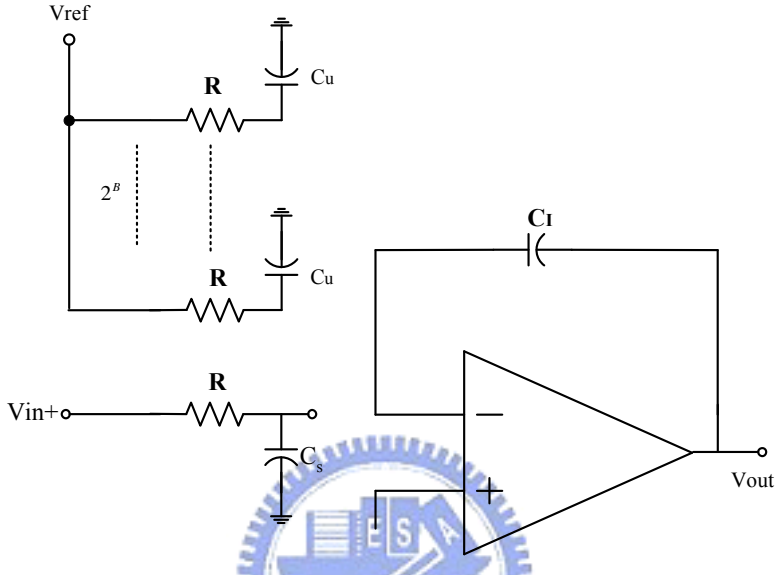


Fig. 4.30 Schematic of integrator during sampling phase

The thermal noise power of DAC branches is a little different with input branch, assumes that Vn is the equivalent noise voltage across the unit capacitor Cu, it is a zero mean random variable and the variance of Vn can be calculated as (4.57), the value is $\frac{kT}{C_u}$. Using the charge conservation theorem, the total noise charge on the DAC braches are added together, and redistributed in the integration capacitor CI in the integration phase, thus we can refer them as an equivalent noise voltage source Vn(in) to the input branch (Cs), it is given by

$$Vn(in) = \frac{\sum_{i=1}^{2^B} C_{ui} \cdot Vn}{Cs} \tag{4.63}$$

Then the noise power of the DAC branches can be obtained by calculating the variance of (4.63), it is given by

$$P_{sw1}(C_u) = \frac{2^B \cdot C_u^{\,2} \cdot \frac{kT}{C_u}}{Cs^2} = \frac{kT}{Cs} \qquad (4.64)$$

The noise power in (4.64) is the same with (4.62). If we use fully differential architecture, then the total switch noise power during sampling phase is expressed as

$$P_{sw1} = 2 \cdot \left(P_{sw1}(C_S) + P_{sw1}(C_u)\right) = \frac{4kT}{Cs} \qquad (4.65)$$

From (4.65) we can find that the switch thermal noise during sampling phase won't vary with the quantizer bit number B if we set the unit capacitor value Cu = $\frac{Cs}{2^B}$, it important for the designer while they want to increase B and don't want to increase the thermal noise effect.

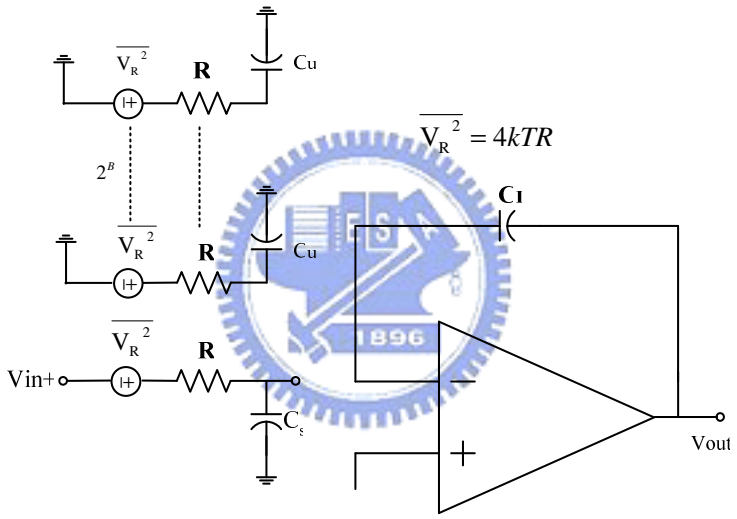


Fig. 4.31 Schematic of integrator during sampling phase with thermal noise sources

Additional switch thermal noise is introduced during integration phase. The schematic in this phase is shown in Fig. 4.32, it is looked like an inverting amplifier architecture, the transfer functions of $\overline{V_R^2}$ to Vout of input branch is given by

$$H_1(s) = \frac{Cs}{C_I} \cdot \frac{1}{1 + sC_SR} \qquad (4.66)$$

And the transfer functions of $\overline{V_R^2}$ to Vout of DAC branch is given by

$$H_2(s) = \frac{Cs}{C_I} \cdot \frac{1}{2^B + sC_SR} \qquad (4.67)$$

Then the switch thermal noise power during integration phase can be calculated as

the method of (4.57), and we must refer it to the input branch, the result are

$$P_{sw2}(C_S) = \left(\frac{C_I}{C_S}\right)^2 \cdot \int_0^\infty 4kTR \cdot |H_1(f)|^2 df$$

$$= \frac{kT}{C_S} \tag{4.68}$$

$$P_{sw2}(C_u) = 2^B \cdot \left(\frac{C_I}{C_S}\right)^2 \cdot \int_0^\infty 4kTR \cdot |H_2(f)|^2 df$$

$$= 2^B \cdot \left(\frac{C_I}{C_S}\right)^2 \cdot \left(\frac{C_S}{C_I}\right)^2 \frac{kT}{C_S \cdot 2^B} \tag{4.69}$$

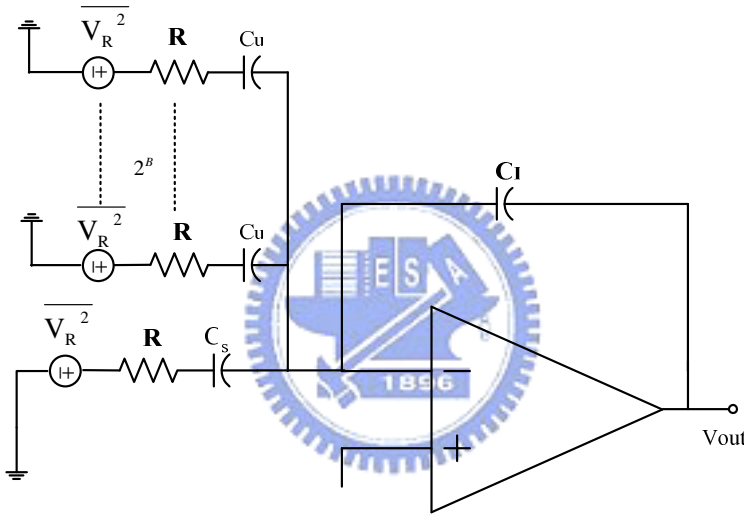


Fig. 4.32 Schematic of integrator during integration phase with thermal noise sources

If we use fully differential architecture, then the total switch noise power during integration phase is expressed as

$$P_{sw2} = 2 \cdot \left(P_{sw2}(C_S) + P_{sw2}(C_u)\right) = \frac{4\mathrm{kT}}{\mathrm{Cs}} \tag{4.70}$$

From (4.65) and (4.70), the switch thermal noise are the same in these two phases. Since the thermal noise voltages introduced during these two phases are uncorrelated, so we can add (4.65) and (4.70). Therefore, the total switches thermal noise at the sigma delta modulator output is as

$$P_{sw} = \frac{1}{OSR} \cdot \left(P_{sw1} + P_{sw2}\right) = \frac{1}{OSR} \cdot \left(\frac{8kT}{Cs}\right) \tag{4.71}$$

Because MOSFETs will produce thermal noise, so the amplifier in the sigma delta modulator will has an equivalent input referred noise source. Fig. 4.33 is thermal noise source in the gate of a MOS transistor, we can write it as

$$\overline{V_{mos}^{\ 2}} = \text{MOSFET\_Thermal\_Noise}$$

$$= 4kT\frac{\gamma}{gm} \qquad (4.72)$$

Where γ is a process variable, in a long channel process it is as 2/3, but in a deep submicron process, we must use a larger γ, and it is as 2.5 [Raz 01]

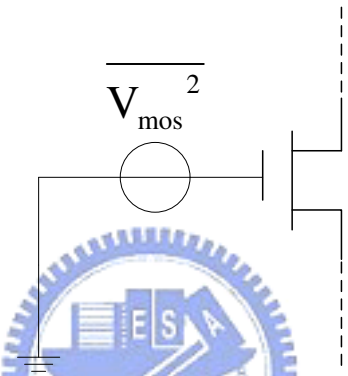


Fig. 4.33 Noise voltage source of MOSFET

The noise in the input of MOSFET will cause some impact on the peak SNR of sigma delta modulator. In [Gag 03], we can find that OTA input thermal noise is just a little bellow switch thermal noise. In this work, we will analyze this noise both on sampling and integration phase. The parameters of OTA like gm and C_L will be considered here. See left side of Fig. 4.34, it is the equivalent circuit schematic during sampling phase, where Vno is the input referred thermal noise spectrum of the OTA. In deep submicron process [Gra 01]

$$\text{Vno} \cong \frac{\alpha \cdot 10kT}{\text{gm1}} \qquad (4.73)$$

It is represented in $\frac{V^2}{Hz}$, where gm1 is the transconductance of the OTA input transistor and α is a noise factor depend on OTA topology, in two stage OTA $\alpha \approx 2$, and in folded cascade OTA, it will be higher.

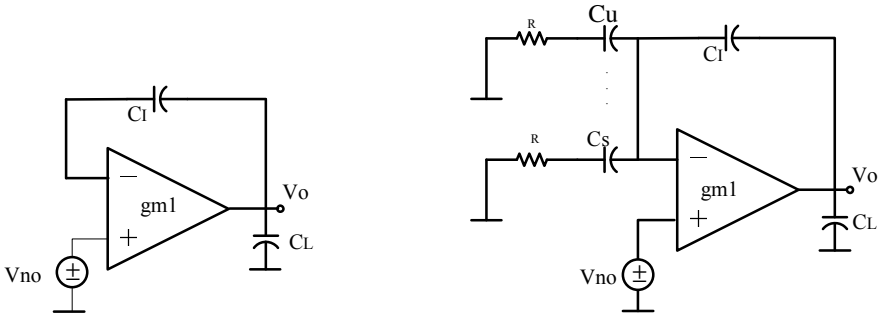


Fig. 4.34 Equivalent circuits of sampling and integration phase

During sampling phase, the circuit is looked like a voltage follower, so the voltage transfer function can be derived as $\frac{\text{Vo}}{\text{Vno}} = 1$, but it will lead to an infinite thermal noise power in the integrator output, this is impossible in the practical situation. So, due to OTA finite gain bandwidth, noise at Vo has an equivalent bandwidth, as Fig. 4.35 shown. So the thermal noise power at integrator output in sampling phase is expressed as

$$P_{OTA}(samp.) \cong \text{Vno} \cdot \frac{\text{GBW}_{\text{samp.}}}{A \cdot 2\pi} \cdot \frac{\pi}{2}$$

$$= \frac{\alpha \cdot 10kT}{\text{gm1}} \cdot \frac{\text{gm1}}{C_L \cdot A \cdot 2\pi} \cdot \frac{\pi}{2} = \frac{10\alpha kT}{4AC_L} \qquad (4.74)$$

where $GBW_{samp.}$ is the gain bandwidth of OTA in sampling phase is represented in rad/S, it is much higher than that during integrating phase, and A is the finite OTA gain.

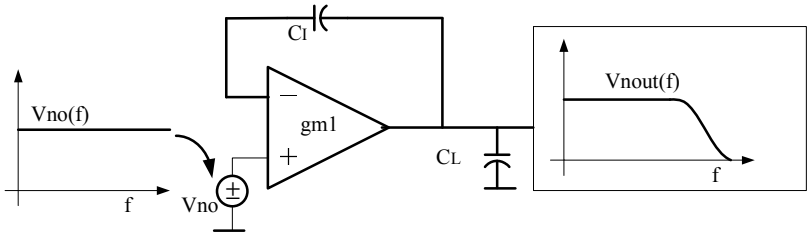


Fig. 4.35 Integrator output noise spectrum in sampling phase

The equivalent circuit schematic during integration phase is in the right side of Fig. 4.34, it looks like a non-inverting amplifier, suppose that the OTA has finite gain and finite gain bandwidth, and we can easily derive the transfer function as

$$\frac{Vo}{Vno}(s) \cong \left(\frac{2a+1+2sC_SR}{1+2sC_SR}\right) \Big/ \left(1+\frac{s}{GBW\cdot 2\pi/A}\right) \qquad (4.75)$$

where GBW is the equivalent gain bandwidth of OTA during integration phase, so $GBW\cdot 2\pi/A$ in equation (4.75) is the 3dB frequency of the non-inverting amplifier in Fig. 4.34. Finally the OTA thermal noise power in the integrator output can estimate as the switch thermal noise as

$$P_{OTA}(\text{int.}) \cong \int_0^\infty Vno \cdot \left|\frac{\text{Vo}}{\text{Vno}}(f)\right|^2 df \qquad (4.76)$$

Finally, the total OTA thermal noise during these two phases must be referred to the input of modulator, so they must to multiply by $1/a^2$. Then this noise will appear in the output of $\Sigma\Delta$ modulator as input signal without any attenuation, it is given by

$$P_{OTA} = \frac{1}{OSR}\cdot\left(\frac{1}{a}\right)^2 \cdot (P_{OTA}(samp.) + P_{OTA}(\text{int.}))$$

$$= \frac{1}{OSR\cdot a^2}\cdot\left(\frac{10\alpha kT}{4AC_L} + \int_0^\infty Vno\cdot\left|\frac{\text{Vo}}{\text{Vno}}(f)\right|^2 df\right) \qquad (4.77)$$

From above analyzes, gm1 seems play an important role in the equation of Vno. Large gm1 can reduce Vno significantly, but how (4.77) changes when gm1 increase..? So we simulate it in Fig. 4.36, it shows calculated OTA thermal noise versus gm1 use equation (4.77), with $A = 60dB$, $a = 0.5$, $R = 500\Omega$ and $Cs = 2pF$, it shows that this noise does not vary significant with gm1. The reason is that the equivalent noise bandwidth will also increase while gm1 increases, although Vno becomes lower, so the total noise is almost the same. So the value of gm1 is independent with OTA

thermal noise, higher gm1 is helpful to get high GBW, but it will consume more analog power.

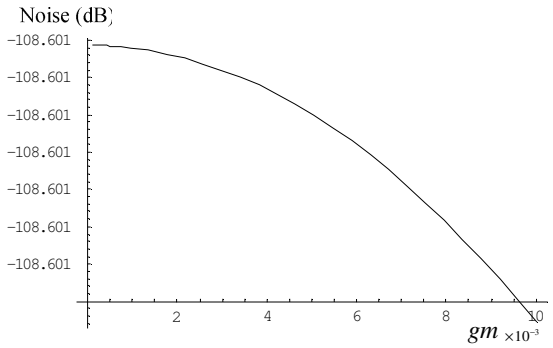


Fig. 4.36 gm1 versus OTA thermal noise

Because reference voltage circuit is implemented by transistors, so the device thermal noise will appear in the output of reference circuit. Noise from voltage reference circuit is also a critical impact in $\Sigma\Delta$ modulator. If an unbuffered reference circuit is used to generate the feedback voltage from a DAC, then the noise from reference circuit output will influence system directly without any suppression. Consider a CMOS bandgap reference circuit in Fig. 4.37, noise at the reference output is almost equivalent to the input referred noise of OTA in Fig. 4.37 [Raz 01], so we can write it as

$$\overline{V_{ref}^{\,2}} \approx Vno = \frac{10kT \cdot \alpha}{gm1} \tag{4.78}$$

Fig. 4.38 is the scheme of integrator with reference noises, because this noise is introduced only in sampling phase, and the reference noise power can be derived as

$$P_{ref} = \frac{1}{OSR} \cdot \int_0^{\infty} \frac{\overline{V_{ref}^{\,2}}}{1+4\pi^2 R^2 C_S^2 f^2}\, df = \frac{\overline{V_{ref}^{\,2}}}{OSR \cdot 4RC_S} \tag{4.79}$$

From above analyses, it is notable that if we divided sampling capacitor into smaller capacitors in parallel feedback branches, the number of branches are proportional to 2^B, then thermal noise in sigma delta modulator won't increase with

quantizer bit number B.

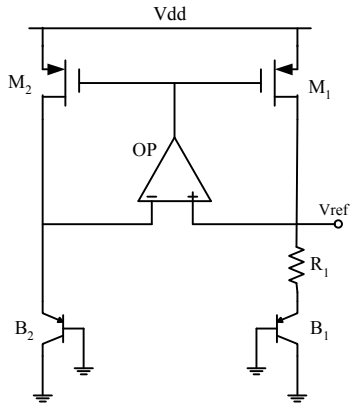


Fig. 4.37 Bandgap voltage reference circuits

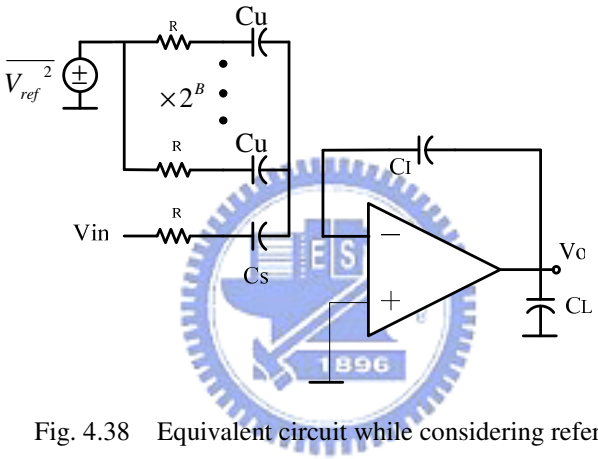


Fig. 4.38 Equivalent circuit while considering reference noise

We must realize the source of each nonideailities in the sigma delta ADC thus we can know how to model their effect. As the analysis shown above, the leakage noise due to finite OTA gain can be considered as an additional quantization noise, so the total quantization noise will higher than theoretical quantization noise, and it can be modeled at D2 in Fig. 4.39, the location is the same with quantization noise. The other nonidealities can be all modeled at D1 in Fig. 4.39, because we have modeled them as input-referred noise in the input of switched-capacitor integrator, and we only consider the nonidealities in the first integrator, so they are all modeled in the input of the sigma delta modulator as D1.

According to the analyses shown above, we can find that if we increase quantizer

bit number B, the quantization noise will be suppressed and dynamic requirements of OTA will be reduced, but on the other hand the switch and DAC branch are also increase, then DAC noise effects are severer, this is one example that needs the designer to make a choice and need to be optimized.

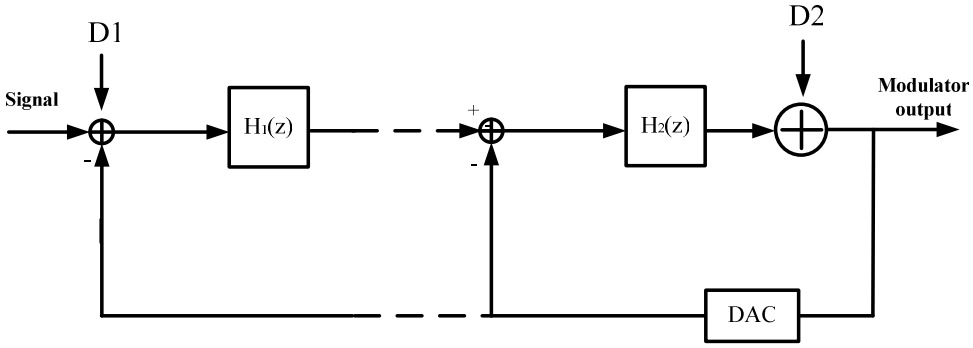


Fig. 4.39 Main nonidealities sources in the sigma delta modulator

4.5 Models of Relative Power

In order to understand how the power consumption of ΣΔ modulators is related to different circuit parameters, we must derive the equation of power dissipation. Some derivations of this part are based on the results presented in [Gee 02, Mar 98a]. It is difficult to estimate the real power consumption in system level, so our goal is not to estimate the absolute value of the power, but is to find how the power changes with the circuit parameters; it is called the relative power consumption. Typically, the power consumption of ΣΔ ADC is categorized to analog part and digital part. We analyze analog part first. The analog part of power dissipation in a ΣΔ modulator is mainly from OTA, and it is proportional to the product of several parameters:

$$POW_{OTA} \sim k_{OTA} \cdot V_{DD} \cdot \pi \cdot C_{L2} \cdot GBW \tag{4.80}$$

where k_{OTA} is the number of current branches of OTA and V_{DD} is the power supply. The k_{OTA} depends on the topology of OTA. There exists a unknown constant $k_{\Sigma\Delta}$ such that the analog power consumption equals $k_{\Sigma\Delta} \cdot POW_{OTA}$, where $k_{\Sigma\Delta}$ is

proportional to the order n of the ΣΔ modulator. The scaling technique of successive integrators is also considered, and we assumed that the scaling factor is as 0.5. Then from (4.80), total power consumption of analog part is as:

$$POW_{ana\log} \cong k_{\Sigma\Delta} \cdot POW_{OTA}$$

$$\sim \left(\sum_{i=0}^{n-1} (0.5)^i \right) \cdot k_{OTA} \cdot V_{DD} \cdot \pi \cdot C_{L2} \cdot GBW \qquad (4.81)$$

So the analog power consumption is related to n, V_{DD}, C_{L2} and GBW, which are important circuit parameters to be determined in the design flow.

Next, we discuss the digital power consumption. The digital part of power consumption is mainly from the operation of MOS switches, and it is proportional to the product of another set of parameters:

$$POW_{SW} \sim n \cdot 2^B \cdot C_{Switch} \cdot V_{DD}{}^2 \cdot 2 \cdot f_B \cdot OSR \qquad (4.82)$$

where $2 \cdot f_B \cdot OSR$ is equal to the sampling frequency, and C_{Switch} is the total gate capacitance of switches. The value of C_{Switch} is inversely proportional to the switch-on resistance R [Wes 94], so we define the relative digital power as

$$POW_{digital} \sim n \cdot 2^B \cdot \frac{1}{R} \cdot V_{DD}{}^2 \cdot f_S \qquad (4.83)$$

When the quantizer bit number B increases, the DEM technique may be used. In our optimization algorithm, the power consumption of DEM hardware is taken into account when B is larger than 3. In general, the DEM which has better noise shaping consumes more power. Considering practical situations, in our algorithm the DEM power rating is assumed to be 60% of the ΣΔ modulator total power rating. Then the total relative power is defined as

$$\text{Power} = \mathrm{K}_1 \cdot POW_{ana\log} + \mathrm{K}_2 \cdot POW_{digital} \qquad (4.84)$$

where K_1 and K_2 are adjusted to make Power (in Watt) to be comparable in

magnitude with real power dissipations. After comparing with power measurements reported in [Gag 03, Mil 03], we set $K_1 = 0.434$ and $K_2 = 0.59 \times 10^{-10}$. Both [Gag 03] and [Mil 03] are based on 0.18-μm CMOS technology. For other CMOS technologies, the K_1 and K_2 may be set to other appropriate values.

5
Optimization Algorithm of Sigma-Delta ADCs Design

As the chapter 1 says, another design approach is proposed to design a sigma delta ADC. Optimizations of all parameters that need to be selected in the design of sigma delta modulator are needed in the process. The main nonideailties are taken into account for optimization, and then the optimal SNR point can be obtained fast. Power consumption are also be considered, the relation between circuit parameters and power is derived, so the optimal design based on power and performance considerations are proposed. In this chapter, the discussions of all circuits parameters both affect SNR and power dissipation are presented. Through the discussions, the trade-off of SNR and power is clearly shown. We can also realize which parameter should be optimized or be set at some reasonable range; it is helpful for optimization work. After that, a complete optimization algorithm is proposed; it can find the combinations of circuit parameters which can achieve certain design specifications and lead to minimum power consumption. They are always called optimal solutions of sigma delta ADC design.

5.1 Modified SNR Equation

With the models of power and nonidealities derived in chapter 4, we will employ them to systematically discuss how each design parameter affects the SNR and the power consumption. After identifying critical parameters, we will use them to propose an optimization algorithm, in order to search for optimal combinations of these

parameters. Before the discussions, we formally define the peak SNR at ΣΔ ADC output as

$$SNR = \frac{\frac{(2V_{ref})^2}{2}}{P_Q + P_{AV} + P_{\delta 1} + P_{\delta 2} + P_{dac} + P_{jitter} + P_{sw} + P_{OTA} + P_{ref.}} \quad (5.1)$$

where $\frac{(2V_{ref})^2}{2}$ is the signal power of a sinusoidal input signal, and capacitor mismatch noise of integrator coefficient is not included due to it is not an important issue in single-loop architecture. Equation (5.1) is used to estimate the peak SNR during the optimization process.

5.2 Discussions of Circuit Parameters

Based on models in chapter 4, the influences of each design parameter to the SNR in (5.1) and the Power in (4.84) are discussed in the following:

1. **OSR** can influence the behavioral of all nonidealities, and can affect power consumption. Higher OSR is helpful to suppress all noises and errors except the settling error. Furthermore, OSR is proportional to the digital power consumption according to (4.82).
2. **B** is an important system parameter. Higher bit number results in smaller quantizer step, and relaxes the dynamic requirement of OTA, so the quantization noise and settling noise can be reduced. However, both the DAC noise power (4.43) and the digital power consumption (4.83) increase exponentially with respect to B.
3. ***n*** is the order of a ΣΔ modulator. Increasing *n* can suppress quantization noise, but can provide little help to other noises and errors. The drawbacks of increasing *n* are the reduced stability and higher digital and analog power consumption.

4. ***A*** is the open loop gain of OTA. Equation (4.5) shows the finite *A* will cause leakage quantization noise. Fortunately, it is not serious in single-loop architecture. A minimum required *A* can be estimated by (4.5) for single-loop architecture, which is about 50 dB.

5. **a_1** is the gain coefficient of first integrator, it usually varies from 0.1 to 1. The a_1 appears in several noise models in last section. Fig. 5.1 is the diagram of OTA input referred noise versus a_1, assuming that OSR = 64. It can be found that OTA noise increases by only 2 decibels when a_1 changes from 0.1 to 1. Using a smaller a_1 is helpful for complete settling, because smaller voltage step is added at integrator output in each clock period, so the required slew rate and gain bandwidth of the first OTA is reduced. Due to stability consideration, the upper limit of a_1 is set to be 1. If higher-order modulator is used, this upper limit is reduced further. However, smaller a_1 needs to be compensated by larger a_i, $i \geq 2$.

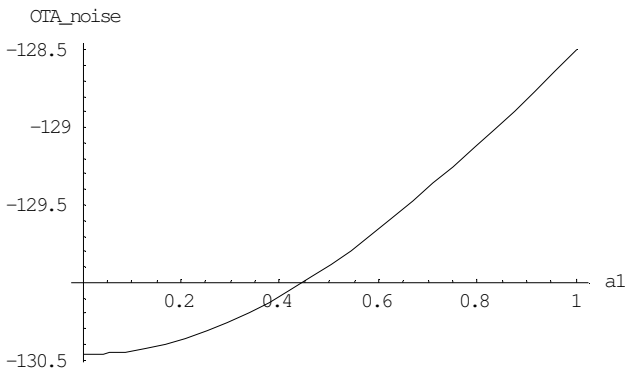


Fig. 5.1 OTA noise versus a1 with OSR=64

6. **R** is the on-resistance of switches. Higher value of R will increase settling error during sampling phase, but it can reduce thermal noise from reference circuit. Fig. 5.2(a) and (b) are the diagrams of peak SNR versus R, for signal bandwidth

100 kHz and 1 MHz respectively, both being under the conditions OSR = 16, B = 4 and n = 3. It is notable that the influence of R to SNR is mainly determined by the sampling rate. The value of R is inversely proportional to the parasitic gate capacitance of transistor. Therefore, higher R reduces the digital power consumption.

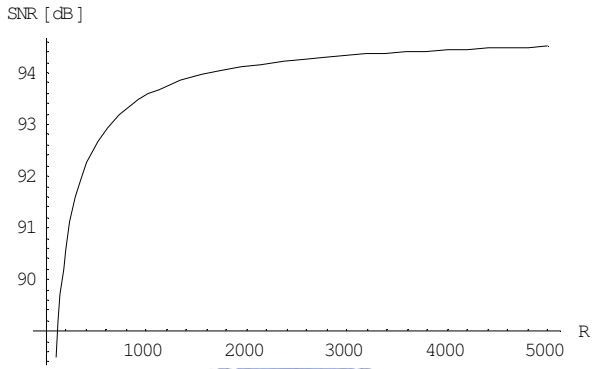


Fig. 5.2 (a) SNR versus R with 100 kHz signal bandwidth

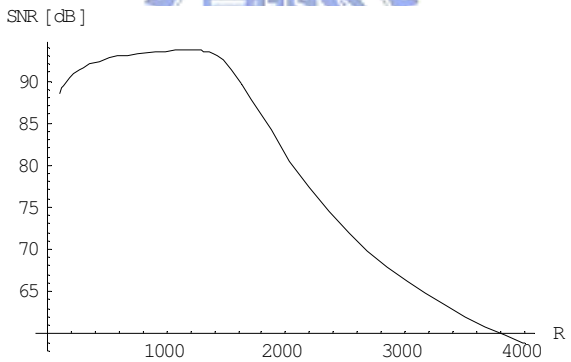


Fig. 5.2 (b) SNR versus R with 1MHz signal bandwidth

7. **GBW** means the effective gain bandwidth of OTA during integration phase. A larger GBW can reduce integration phase settling. It seems that higher GBW will cause higher OTA noise, because the effective noise bandwidth is higher. However, in practice, the input transconductance gm1 of OTA also increases when GBW increase, so the input referred noise spectrum of OTA will decrease. Overall, the total OTA thermal noise won't change significantly with respect to GBW. But higher GBW results in higher gm1, and also higher the bias current

at OTA input stage, leading to higher analog power consumption.

8. **C_S** is the value of sampling capacitor. Choosing C_S value can be a complex work. A larger C_S can reduce thermal noise, but can increase settling noise at integrator input. A large C_S also increases the effective loading of integrator, and leads to the degradation of GBW and slew rate. Thus settling noise floor of integrator output will increase. Heavy output loading of integrator will increase the power consumption of operation amplifiers.

9. **SR** is the slew rate of OTA and it plays an important role in the settling performance of integrator output. Typical value of slew rate in modern design is 80 V/μs ~ 500 V/μs. If the sampling frequency is lower, or if B is larger, then the specification of slew rate can reduce. Large slew rate needs large output current to charge the loading capacitance, so the OTA power consumption also increases. A simple estimation of the minimum required SR is

$$\text{SR(min.)} = V_{ref} \cdot 2 \cdot 2 \cdot f_B OSR \qquad (5.2)$$

It means the integrator output voltage should change Vref during half clock period.

10. **V_{ref}** is the reference voltage, which is usually proportional to supply voltage V_{DD}. Larger V_{ref} can increases signal power and leads to larger SNR. Generally, the maximum reference voltage is limited by the signal swing of an OTA output and it is estimated in [Gag 03] as

$$V_{ref} \cong \frac{0.95 \cdot V_{DD} - 2 \cdot V_{DS}}{1.2} \qquad (5.3)$$

where V_{DS} is the overdrive voltage of the output stage transistor. The V_{DD} is a factor of process technology. It is usually set at 1.8V in 0.18-μm CMOS technology.

11. **σ_{jit}** is the standard deviation of clock jitter. From equation (4.51), jitter plays an

important role in high frequency and large magnitude applications. It is difficult to specify σ_{jit} in the early stage of design. We expect the in band jitter noise not to be higher than the ideal quantization noise. Since the ideal quantization noise is determined by OSR, B and n, which are to be determined by the optimization process, we specify the maximum tolerable value of σ_{jit} after the optimization process.

12. **σ_{cap}** is the standard deviation of the unit capacitor. Its value depends on process technology. Recently, double poly and metal-insulator-metal (MIM) capacitor are the two main methods to implement capacitances in analog integrated circuits. These two types of capacitors have high linearity and good matching accuracy, and the σ_{cap} of them are all below 0.05% [All 02]. The main influences of σ_{cap} on ΣΔ modulator are about the deviation of integrator coefficient and the multi-bit DAC linearity. Although 0.05% accuracy is sufficient for a_i, this accuracy is not enough when B is large, so the DEM calibration techniques may be needed for compensating the DAC noise.

5.3 Trade-Off between SNR and Power

The Table 5.1 is used to summarize the discussions above. Basically we identify B, OSR, *n*, R, GBW, C_S and SR as the design parameters used in the optimization process. Table II shows qualitatively how the noises and the power are affected when a particular design parameter increases. It can be perceived from Table 5.1 that the ΣΔ ADC design task is a very complex one. A designer can hardly decide the circuit parameters quickly by conventional design approaches, reviewed in section I.

	B ↑	OSR ↑	n ↑	R ↑	GBW ↑	Cs ↑	SR ↑
P_Q	↓	↓	↓	—	—	—	—
P_{AV}	↓	↓	↓	—	—	—	—
$P_{\delta 1}$	↓	↑	—	↑	—	↑	—
$P_{\delta 2}$	↓	↑	—	—	↓	↑	↓
P_{dac}	↑	↓	—	—	—	—	—
P_{jitter}	—	↓	—	—	—	—	—
P_{sw}	—	↓	—	—	—	↓	—
P_{OTA}	—	↓	—	—	↑	—	—
P_{ref}	—	↓	—	↓	↓	↓	—
Power	↑	↑	↑	↓	↑	↑	↑

Table 5.1 Summary of noise-power and power-rating when design parameters increase

5.4 Optimization Algorithm

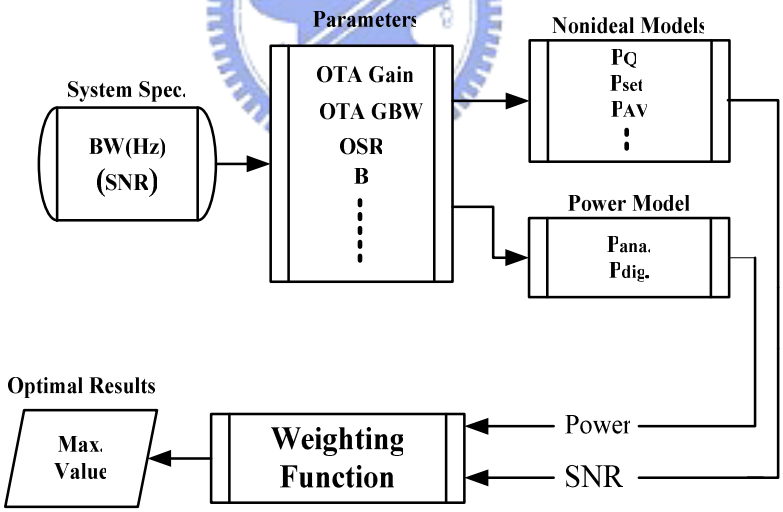


Fig. 5.3 Proposed optimization algorithm for the sigma delta modulator design

In the following we propose an optimization algorithm to help designers to reach an optimal design quickly. It is based on the error and power models described in section II. The complete flow of the optimal methodology is shown in Fig. 5.3. The input signal bandwidth (Hz) and the output signal SNR (dB) are treated as the design

specifications. We modify the figure-of-merit (FOM) [Sch 05] function by multiplying a variable K to the SNR term of FOM, to become our weighting function.

$$\text{Weighting Function} = \text{K} \cdot \text{SNR}_{\text{dB}} + 10\log\left(\frac{f_B}{\text{Power}}\right) \tag{5.4}$$

Basically the optimization algorithm is to search through the entire parameter space to find the set of design parameters which maximize the Weighting Function. The variable K would certainly affect the optimization result. This is discussed later. The parameter searching space is specified to be

- OSR : 8 ~ $\dfrac{80\ \text{MHz}}{2 \cdot f_B}$
- B : 1 ~ 6 (if > 3, DEM is required)
- n : 1 ~ 3
- R : 100 Ω ~ 1000 Ω
- GBW : 50 MHz ~ 500 MHz
- SR : 50 V/μs ~ 500 V/μs
- C_S : 1 pF ~ 10 pF

The parameters σ_{cap} and V_{ref} depend on the technology, so they are set before the optimization. After the optimization process, the tolerable value of jitter standard deviation σ_{jit} can be specified. During the optimization process, the gain coefficients a_i are specified according to the rules provided in [Mar 98b]. The optimization algorithm systematically searches the entire parameter space listed above. In each iteration, the SNR and the Power are computed, and the Weighting Function is evaluated. The value of K can significantly modify the Weighting Function and affect the optimization result. Typically, if we prefer high resolution designs, we set K higher and SNR plays a more important role than Power; on the other hand, if we prefer low power designs, we can set K lower. After the optimization process, the set of design parameters which results in the largest Weighting Function value is the

outcome of the process. This outcome is evaluated. If not acceptable, the K is adjusted and the optimization process is return.

6
Experimental Results

This optimal algorithm described above is implemented by Mathematica®. In order to demonstrate the accuracy and practicability of our method, we apply it to two published design cases from two different application fields. The first case is a multi-bit ΣΔ modulator in 0.18-μm CMOS technology for ADSL-CO application [Gag 03], which has a reference voltage at 0.9 V. Its peak SNR can reach 85 dB over 276 kHz signal bandwidth. The second case is also a multi-bit ΣΔ ADC for broadband applications [Gee 00], which is fabricated by 0.65-μm CMOS technology with 1 V reference. The signal bandwidth is 1.25MHz. The circuit can reach 95 dB peak SNR. At the end of this section, we will also discuss issues related to sensitivity.

6.1 Sigma Delta ADC for ADSL-CO Application

To compare with the design of [Gag 03], the optimization algorithm uses the same specifications as those in [Gag 03]. They are:

- SNR : 85 dB
- Signal bandwidth : 276 kHz

The OTA gain A is set at 60 dB and the V_{ref} is set at 0.9 V for a 1.8 V power supply in 0.18-μm CMOS technology. The matching of capacitor σ_{cap} is set at 0.05% for the MIM capacitance. The variable ranges of the parameters are also specified as follow. For the signal bandwidth of 276 kHz, the range of OSR is set between 8 ~ 128, and the quantizer bit B is between 1 ~ 5. The order n is between 1 ~ 3, since using a n higher than 3 may cause instability. The range of R is between 100 Ω ~ 1 kΩ, which is a reasonable range for switch on-resistance. C_S is between 1

pF and 10 pF. The minimum size of C_S is usually determined by process technology. Finally, GBW and SR are between 50 MHz ~ 500 MHz and 50 V/μs ~ 500 V/μs respectively. The results published in [Gag 03] and those obtained from our optimization methodology are all listed in Table 6.1, which includes three optimization results corresponding to $K = 0.5$, $K = 0.8$, and $K = 1$.

circuit parameters	**[Gag 03]**	**K =0.5**	**K =0.8**	**K =1**	**Unit**
OSR	96	45	95	95	-
B	3	2	3	4	-
n	2	2	2	2	-
R	300	1k	1k	950	Ω
C_S	1.7	1	1.6	1.25	pF
GBW	**400**	50	**130**	130	MHz
SR	**500**	50	**150**	150	V/μs
σ_{jit}	-		15		Ps
SNR	87.6	84.4	87	96.5	dB
Power	30	1.9	2.9	19.6	mW

TABLE 6.1 Comparisons of our design results and those in [Gag 03] with different K

From Table 6.1, we find that when $K = 0.5$, the SNR is 84.4 dB, which does not meet the specification. To increase SNR, we need to increase K. When $K = 0.8$, the result of SNR = 87 dB satisfies the specification, although the Power = 2.9 mW is higher than Power = 1.9 mW when $K = 0.5$. Although $K = 0.8$ is satisfactory, the results from higher K are also reported. When $K = 1$, parameters achieving high SNR are preferred, resulting in OSR being 95 and B being 4. Since B is larger than 3, the DEM technique is used. The power consumption is dramatically larger at 19.6 mW, and this is due to the facts that the DEM is employed and that B is larger. Notice that the optimization algorithm selects 2 for n, instead of 3. Our analysis reveals that increasing n from 2 to 3 only raises SNR by 0.1 dB. Since there exist noises that are

larger than quantization noise as are shown in Table 6.2, an additional order does not have significant effect. On the other hand, increasing n can raise power consumption considerably, so it seems that $n = 3$ is decisively rejected by the algorithm. We conclude that we accept the design that is achieve when $K = 0.8$. Due to sensitivity problems discussed later, we normally prefer the designed SNR reasonably higher than the specified value.

Next, we want to compare our design (for $K = 0.8$) with that reported in [Gag 03]. Table 6.1 shows that some of our parameters are very close to the those in [Gag 03], such as OSR, B and n. There are some differences in the values of R and C_S, resulting in different RC time constants, 1.6k Ω-pF v.s. 510 Ω-pF. Therefore, the $P_{\delta 1}$ for our design is at -88.6 dB, and that in [Gag 03] is much smaller at -196 dB, as is shown in Table 6.2. The very small $P_{\delta 1}$ in [Gag 03] is not helpful in improving SNR, but only to increase power consumption. Since larger R can save much power consumption, it is selected by our algorithm. Significant differences also appear in GBW and SR. Our solution shows GBW = 130 MHz and SR = 150 V/μs are the optimal choices to implement this modulator, in contrast to GBW = 400 MHz and SR = 500 V/μs proposed in [Gag 03]. Consequently, settling error $P_{\delta 2} = -110.8\,\text{dB}$ in our design, while $P_{\delta 2} = -248\,\text{dB}$ in [Gag 03]. It is clear from Table 6.2 that, in both designs, the dominating noise power is P_{dac} which is -86.7 dB. Therefore, although large GBW and SR in [Gag 03] result in very small $P_{\delta 2}$, this renders no improvement in SNR, but can significantly increase power consumption. Table 6.1 shows Power = 30 mW for [Gag 03] and Power = 2.9 mW for our design. The big difference in power consumption is the direct result of different GBW, SR and R values used in the two designs. Notice that the SNR of [Gag 03] listed in Table 6.1 is computed by our model using the parameters provided in [Gag 03]. The measured SNR in [Gag 03] is 85 dB.

Noise	in [Gag 03]	K =0.5	K =0.8	K =1
P_Q	- 109.8 dB	- 87.5 dB	- 109.7 dB	- 115.8 dB
P_{AV}	-146.4dB	- 128.2 dB	- 143.9 dB	- 149.9 dB
$P_{\delta 1}$	- 196.5 dB	- 201.4 dB	- 88.6 dB	- 111.6 dB
$P_{\delta 2}$	- 248 dB	- 115.6 dB	- 110.8 dB	- 113.6 dB
P_{sw}	- 96.9 dB	- 91.3 dB	- 96.6 dB	- 95.5 dB
P_{ref}	- 104.5dB	- 92.8 dB	- 104.3 dB	- 101.9 dB
P_{OTA}	- 123 dB	- 117.4 dB	- 122.7 dB	- 121.6 dB
P_{dac}	- 86.7 dB	-86.4 dB	- 86.7 dB	- 117.5 dB
P_{total}	- 85.6 dB	- 82.4 dB	-85 dB	-94.5 dB

TABLE 6.2 The corresponding noise powers for the design parameters listed in Table 6.1

Some more discussions will be given based on the noise powers listed in Table 6.2, where P_{total} is the sum of in band noise powers. When $K = 0.5$, quantization noise and DAC noise are dominant due to low OSR. This suggests that device noises can be neglected under low resolution applications. For both the cases in [Gag 03] and in $K = 0.8$, the quantization noise is no longer the major noise source, but the DAC noise becomes the major sources to degrade the performance with switch thermal noise tracking behind about 9 dB lower. In our model, DEM is not used when B is less than 4 bits, and this is the reason P_{dac} dominates, since B = 3 both for [Gag 03] and $K = 0.8$. For $K = 0.8$, high switch on-resistance is also a reason for performance degradation although not a major one. When $K = 1$, the optimization algorithm set B to be 4, so the DEM technique is employed, and DAC noise is suppressed to -117.5 dB. Accordingly the P_{sw} at -95.5 dB and P_{ref} at -101.9dB become the dominating noise powers. Finally, we want to report a case not listed in Tables 6.1 and 6.2. That is, suppose we change our rule to enable DEM when B is

equal to or larger than 3. Then, for the case $K = 0.8$, the algorithm again sets B to be 3, but P_{dac} is reduced to -120 dB (from -86.7 dB), and SNR is raised to 90 dB (from 87 dB). But the penalty of additional digital power consumption will appear. This tradeoff must be considered by the designers.

Our settling noise models are also useful in conventional design approach. As mentioned in chapter 1, people select OSR, B and n in the system level. In [Gag 03], they set OSR = 96, B = 3 and n = 2. The discussions above suggest that the circuit level design of [Gag 03] results in $P_{\delta 1}$ and $P_{\delta 2}$ smaller than needed. Our models can be applied to circuit level designs. From our $P_{\delta 1}$ model in (4.14), if we set $R \cdot C_S < 1.1k\,\Omega \cdot pF$, then this can make $P_{\delta 1}$ below the quantization noise power. Furthermore, larger R and lower C_S can reduce total power consumption. People may use these two criteria to choose adequate values of R and C. Next, Our $P_{\delta 2}$ model in (4.35) can be used to compute the variation of $P_{\delta 2}$ v.s. GBW and SR, as is shown is Fig. 6.1. It can be observed that $GBW \geq 130$ MHz and $SR \geq 150$ V/μs are sufficient to suppress $P_{\delta 2}$ to be below quantization noise power. It is also notable from Fig. 6.1 that increasing GBW is more efficient than increasing SR for reducing the value of $P_{\delta 2}$.

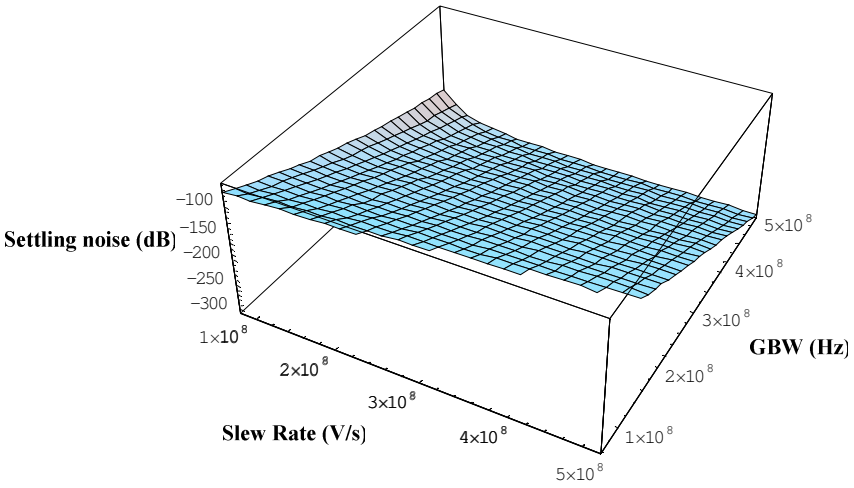


Fig. 6.1. 3D plot of $P_{\delta 2}$ v.s. GBW and SR

6.2 Sigma Delta ADC for Broadband Application

The following specifications for broadband applications are listed as the input of optimization process:

- SNR : 95dB
- Signal bandwidth : 1.25 MHz

These specifications are similar to the ones used in reference [Gee 00], where a single-loop third order sigma delta modulator is used to achieve the specifications. The oversampling ratio used in [Gee 00] is 24, and a four bit quantizer and the DEM are used in their design. For this design problem, the algorithm is setup in the following before the optimization process starts. The value of finite OTA gain A is set at 70 dB for high bandwidth applications. V_{ref} is set at 1V. The matching of capacitor σ_{cap} is set at 0.05% for this process. The ranges of OSR is set to be 8 ~ 32. The ranges of other parameters are almost the same as in the previous case. Table 6.3 shows the design results of those published in [Gee 00], and those generated from our optimization methodology, with $K = 0.8$.

circuit parameters	[Gee 00]	proposed	unit
OSR	24	24	-
B	4	4	-
n	3	3	-
R	220	250	Ω
C_S	3.2	3	pF
GBW	220	190	MHz
SR	145	140	V/μs
σ_{jit}	-	6	ps
SNR	97.7	97.5	dB
Power	295	250	mW

TABLE 6.3. Comparisons of our design results when $K = 0.8$ with those in [Gee 00]

Obviously, the results of our design are very close to those in [Gee 00]. This means that the design parameters in [Gee 00] are almost the optimal solution. Lower power consumption is achieved in our design due to a larger R, a lower GBW and a smaller C_S. The system order n is chosen as 3 both in the [Gee 00] and in our design, although n = 3 may reduce stability in single-loop architecture. However, through careful design of integrator coefficient, instability condition can be avoided. Lower order architecture may require larger OSR to achieve high SNR, but it is difficult to raise OSR under wide signal bandwidth. Finally, higher order architecture, lower OSR and large B with DEM are selected by our algorithm. We find that the performance of a high resolution and high speed $\Sigma\Delta$ modulator is quantization noise and thermal noise (kT/C) limited. The switch thermal noise power P_{sw} is at -96 dB in this design. If we reduce n = 3 to n = 2, the quantization noise will become -84 dB (from -104 dB). Then the overall system will become quantization noise limited and can not achieve the required specification of SNR.

6.3 A Discussion on Sensitivity of parameters

A set of parameters satisfying design requirement can be sensitive if a small perturbation to some of the parameters would result in significant reduction in SNR. Our SNR model (5.1) can be used to check the sensitivity of parameters with sufficient confidence. For example, for a 300 kHz signal bandwidth, the design B = 3, OSR = 120, n = 2, SR = 150 V/μs, GBW = 220 MHz, R = 450 Ω and C = 3 pF can achieve a 85.4 dB SNR, but 10% deviation of R and C can degrade SNR by 10 dB. Such a design can not lead to a robust result, so it must be rejected. Fig. 6.2 shows the variation of SNR with respect to R and C, with other parameters fixed. The R and C at (450 Ω, 3 pF) labeled as point A is apparently situated at a disadvantaged location. If

R and C is moved to point B at (200 Ω, 2 pF) with SNR = 90.12 dB, the worse SNR reduction is 0.13 dB with even a 20% variation in R and C. Thus, we can say the design corresponding to point B is a relatively robust one. Parameter drifting is something that can not be avoided, at least for two reasons: First it may be due to model inaccuracies, and second, it may be caused by the fabrication processes. Therefore, we suggest that people use our SNR model (5.1) to check about the sensitivity of their design.

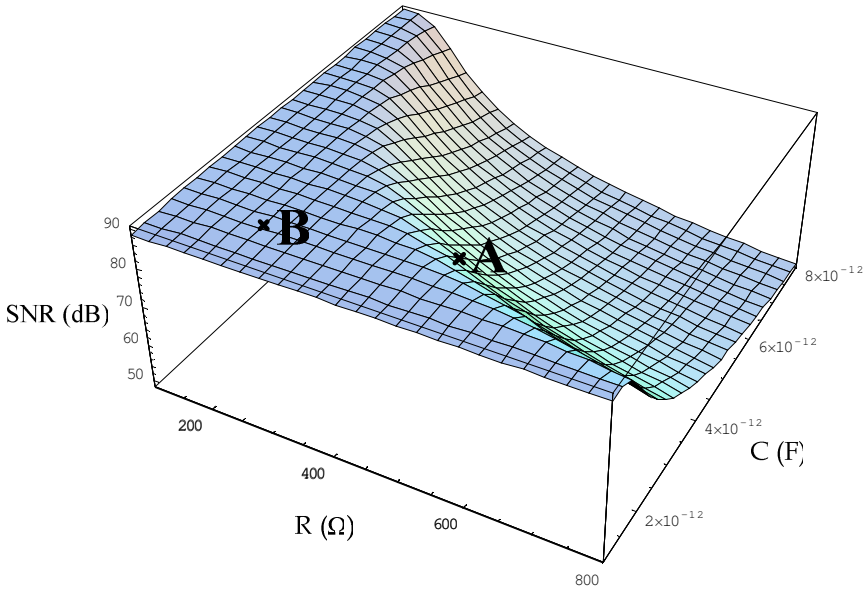


Fig. 6.2. 3D plot of variation of SNR with respect to R and C

7
Conclusions and Future Works

The main contributions of this work are described in the following. First, we construct a settling error model of the switched capacitor integrators in ΣΔ modulators using statistical analysis. This model considers both settling errors in the sampling and the integration phases, and is represented in noise-power form. We also derive the DAC noise-power model. In addition, we make modifications to existing noise-power models of other noises, particularly to thermal noise models. The noise-power models of all major noises and errors are established in chapter 4, and the SNR is defined in (5.1) accordingly. This provides a powerful analytical tool to ΣΔ modulator designers. For example, in chapter 6, the SNR is used to check parameters sensitivities, and the settling model is applied to determine GBW and SR values. Second, based on the nonidealities models and the relative power model, we propose an optimization algorithm in section chapter 5. In contrast to the complexity and the difficulty encountered in the conventional ΣΔ modulator design approach which is also qualitatively discussed in chapter 5, this algorithm can completely and efficiently search the entire design parameters space to find the set of parameters which satisfies the specifications, while achieving the lowest power consumption. It is shown in chapter 6 that our algorithm can achieve better results compared with existing designs. However, the more important issue in chapter 6 is that the complete models allow people to analytically evaluate design results; no matter they are generated from our algorithm or designed elsewhere. Many cases on the regard are discussed in chapter 6.

Although this work is convenient for inexperience sigma delta designers, but there still have some limitations of this algorithm. It is more suitable for single-loop

architecture, because some models of nonidealities in MASH architecture are quit different with that in single-loop topology. It needs some new derivations of these models and takes them into this algorithm, and then the optimization topology in this algorithm can extend to MASH topology. In the future works, the nonlinear problems of switch resistance, capacitors and OTA gain in sigma delta modulator are needed to be considered. Stability problems are also needed to be analyzed. There also have some other imperfections in sigma delta modulators, so the models of these imperfections can help people to get a more accurate SNR equation and power model. The optimization algorithm for a more complete optimization design of sigma delta modulators will be established.

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