A Charge-Recycling Buck-Store and Boost-Restore (BSBR) Technique With Dual Outputs for RGB LED Backlight and Flashlight Module

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***Abstract*—A boost converter with buck-store and boost-restore (BSBR) technique fabricated by 0.25 μm CMOS BCD process can provide different supply voltages to drive series red, green, and blue LEDs in sequence for reducing the power consumption on the constant current generator. The proposed technique not only stores and restores extra energy during the transient time of the reference tracking response to improve the efficiency but also enhances the reference tracking response to greatly reduce load transition time. Experimental results show that the period of reference tracking response can be improved. When the load current is 100 mA, the periods of reference down-tracking and up-tracking are smaller than 10 and 20 μs, respectively. Furthermore, this technique can also provide a regulated voltage to drive the subblock implemented in the liquid crystal display system. The maximum efficiency of charge recycling is up to 94%, and the maximum efficiency of this boost converter is 94.5%. Experimental results demonstrate fast and efficient reference tracking performance is achieved by the proposed BSBR technique.**

***Index Terms*—Charge recycling, dc–dc converter, field color sequential (FCS), reference tracking.**

I. Introduction

THE SELECTION of the backlight module becomes more and more important in order to get high-quality display in liquid crystal display (LCD) panels. Today's most popular and power-efficient backlight module is the white-LED backlight in LCD panels since the power dissipation can be reduced about 40% compared to the cold-cathode fluorescent lamps (CCFLs) backlight module. In addition, the white-LED backlight generates 70%–80% National Television System Committee (NTSC) color gamut, which is better than that of a CCFL backlight. Furthermore, the color filter, which determines the color of the images in LCD panels, masks much of the light emitted, and thus, increases power consumption in the backlight system. This reduced efficiency becomes the major disadvantage of the current backlight systems.

Based on the field color sequential (FCS) technique [1], [2], the color filter-less LCD panels with red, green, and blue (RGB) LED backlight can provide 110% NTSC color gamut in order to have better color gamut and low power consumption. The operation of the FCS technique [3] shown in Fig. 1 can effectively reduce color breakup and motion blur effects [1]. Owing to sequential colors of RGB, the RGB LEDs are not always turned on, and thus, the power consumption can be reduced. Persistence of vision can make the color image appear in human's eyes without sacrificing the color gamut compared to the conventional CCFL backlight. As a result, this innovation becomes a trend in today's LCD display market owing to high color gamut and low power consumption. For portable devices like notebook computers, the largest power consumption comes from the backlight module. Therefore, it is important to decrease the power consumption in backlight module of the notebooks without sacrificing any image quality. As a matter of course, the color filter-less LCD panel with the FCS technique proves to be the best choice to reduce the power consumption of the display panels in the design of notebooks. However, color filter-less LCD panels using the FCS technique need an efficient RGB LED backlight driver to improve power efficiency and image quality. Consequently, the RGB LED backlight driver module for the FCS technique becomes more and more popular owing to the characteristics of low power consumption and high image quality.

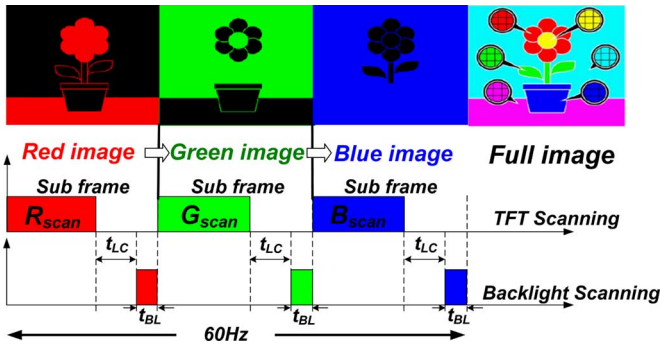

Fig. 1. Timing diagram of field color sequential technique.

The frame per second (fps) for the FCS technique is 60 Hz. According to the FCS technique, one frame of data needs to be divided into three different color subframes, which are $R_{\rm scan}$, $G_{\rm scan}$, and $B_{\rm scan}$, as shown in Fig. 1. Thus, the full color of one image can be constituted by the three subframes. As a result, the subframe rate of the three subframes is 180 Hz. The operation of one subframe contains three basic steps. The first step is the operation of thin-film transistor (TFT) scanning in order to get the image color data. Second, according to the image color data, liquid crystal is rotated to the correct position within

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liquid crystal time t_{LC}. Finally, after liquid crystal is turned to the correct position, the LED backlight module emits correct light through the LCD panels to display the image colors at the rest of time t_{BL}, which indicates the lighting time to determine the brightness of backlight module. Consequently, the RGB LED backlight driver needs to provide enough driving voltage and current for different color LEDs according to the subframe rate of 180 Hz. Generally speaking, since the material characteristic of blue and green LEDs is indium gallium nitride (InGaN) and the material characteristic of red LEDs is aluminum gallium indium phosphate (AlGaInP) [4], the forward voltages of red LEDs are different from that of green and blue LEDs, i.e., the forward voltage of green and blue LEDs is approximately 2.8–3.3 V, and the forward voltage of red LEDs is close to 2.2–2.8 V. Moreover, LED drivers use constant current generator to provide the regular current for constant lumen. In general, the constant current generator occupied minimum of about 0.4 V to keep the characteristic of regular current, and when the current is regulated to 25 mA, the forward voltages of an R-LED and a G-LED (or B-LED) are close to 2.2 and 3 V, respectively. Therefore, the driving voltage for four-series R-LEDs and G-LEDs (or B-LEDs) are approximated to 9.3 and 12.4 V, respectively, i.e., the driving voltage of the RGB LED backlight driver needs to efficiently switch between two driving voltages 9.3 and 12.4 V in order to meet the requirement of the FCS technique.

In this paper, a new charge recycling buck-store and boost-restore (BSBR) technique is proposed to reduce the power dissipation on the LED driver circuit and is applied on the boost converter to control the voltage: 9.3 V for four-series R-LEDs and 12.4 V for G- or B-LEDs in the LED backlight module. The analysis of power consumption and the overall efficiency in the design of RGB LED backlight driver are presented in Section II. In Section III, the architecture of the proposed BSBR control, the BSBR tracking algorithm, and the energy transforming efficiency are discussed in detail. Section IV describes the circuit implementation composed of the proposed BSBR controller and the pulsewidth-modulated (PWM) generator of the boost controller. The chip was fabricated in TSMC 0.25 μm BCD 40 V technology and the experimental results are shown in Section V. Finally, a conclusion is made in Section VI.

II. Analysis of Power Consumption and the Overall Efficiency in the Design of RGB LED Backlight Driver

The light illumination of LED is related to the amount of driving current and the forward voltage [4]–[6]. The forward voltage developed across an LED depends primarily on the semiconductor design and manufacturing tolerance. It is not economic and inefficient to use the voltage control to determine the brightness for achieving uniform luminance of the backlight. In order to get uniform and sufficient luminance, the LED backlight module needs to use constant current to drive series-connected LEDs. Using a constant current driving technique, the variation of the LED forward voltage can be solved by simply boosting the driving voltage to a sufficient high-voltage level. As a result, the architecture of conventional LCD panel with LED backlight module [7] is shown in Fig. 2. The function of the dc–dc converter can provide a sufficient high voltage to overcome the total forward voltage $V_{\rm LED}$ of series-connected LEDs. The constant current generator is designed to regulate the driving current of the series-connected LEDs to get uniform luminance. Besides, the driving current I_{CC} is independent of the sufficient high voltage $V_{\rm out}$ generated by the dc–dc converter. The power dissipation $P_{\rm module}$ in LED backlight module for the FCS technique is composed of three parts, which is expressed as

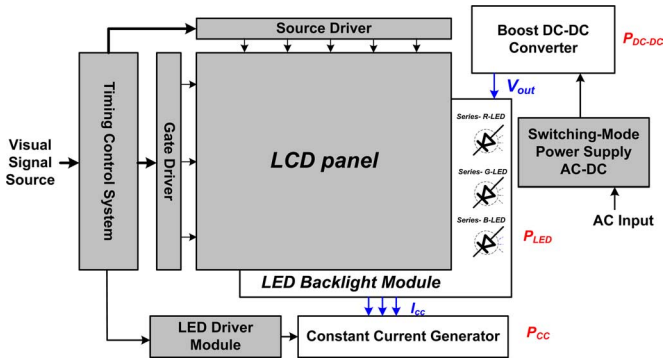


Fig. 2. Function block of the conventional LCD panel with LED backlight module.

$$P_{\rm module} = P_{\rm LED} + P_{CC} + P_{\rm dc-dc}. \tag{1}$$

$P_{\rm LED}$ is the power consumption on the series-connected LEDs when the constant driving current flows through and forces the LEDs to emit light to the LCD panel. The constant driving current generated by the constant current generator consumes power dissipation P_{CC}, assuming the voltage across the constant current generator is V_{CC}. Besides, the power dissipation of the boost dc–dc converter is $P_{\rm dc-dc}$.

In the efficiency consideration of the backlight module, the power conversion efficiency of the switching dc–dc converter is higher than 90%, i.e., the reduction of power loss $P_{\rm dc-dc}$ in the dc–dc converter is much smaller than those of other power dissipations and cannot be decreased remarkably. Thus, in order to reduce the overall power consumption of the LED backlight module, the primary consideration of reducing power consumption is focused on $P_{\rm LED}$ and P_{CC}.

The comparison of power consumption between conventional TFT LCDs with white-LED backlight and FCS TFT LCDs with RGB-LED backlight is illustrated in Fig. 3 under the same light illumination condition. Interestingly, the FCS technique can save 40% power compared to the conventional LCD display since there is no color filter that reduces the brightness of the LCD panel. Hence, the power consumption of the backlight module can be drastically minimized. Furthermore, this technique can be extended to accompany the local blanking/dimming technique according to the locally averaged image data, i.e., a higher power saving result can be achieved, and thus, the power reduction can be more than 60%. Actually, the minimum power consumption of the LCD display can be reduced to 20% of the conventional design when the backlight system is turned off. However, the image only contains gray levels at

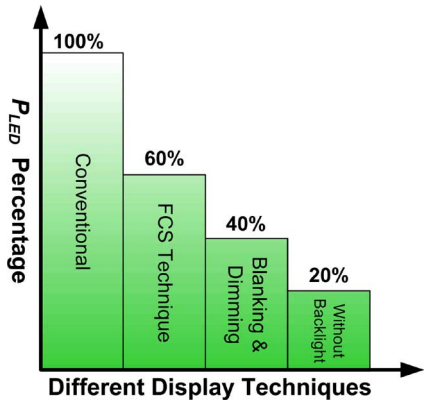


Fig. 3. Comparison of power consumption between different display techniques.

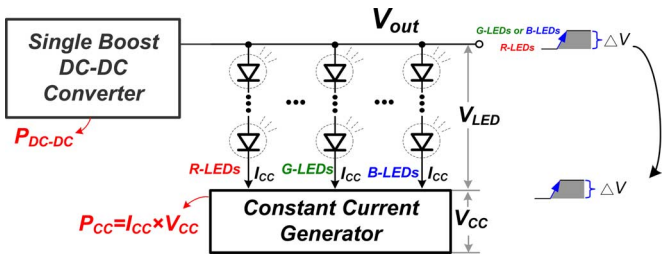


Fig. 4. Power dissipation on the constant current generator when using only one boost dc–dc converter.

this moment. Therefore, this paper utilizes the FCS technique to reduce the power consumption $P_{\rm LED}$.

The power dissipation on the constant current generator is proportional to the current I_{CC} and the headroom voltage V_{CC}, as shown in Fig. 4. According to the aforementioned statement, I_{CC} is designed to define the brightness of LCD panel, which should not be reduced arbitrarily. Therefore, the LED backlight module is designed to minimize the voltage V_{CC} for reducing the power consumption [8]–[10]. However, the forward voltage of R-LEDs is different from that of G- or B-LEDs because of the different material characteristics. It is not suitable to continuously supply the higher output voltage for FCS technique since the higher output voltage for turning on the R-LEDs consumes larger power dissipation on the constant current generator than that of the G-LEDs or B-LEDs. If the RGB LED backlight system needs to reduce the cost, only one dc–dc converter is utilized to supply a sufficient voltage to the different color LEDs [11]. Therefore, the conventional LED backlight module utilizes many converters [12] with different output driving voltages to reduce power consumption at the sacrifice of design cost. The design of RGB LED driver needs to consider high efficiency and low cost in order to improve the advantage of the FCS technique in the color filter-less LCD panels.

The proposed BSBR technique can store extra charge and recycle it back to the output node when the backlight module switches between the R-LEDs and G-LEDs (or B-LEDs). The efficiency of charge recycling can be up to about 94%, which is the common power efficiency in dc–dc converters. Moreover, the BSBR stage not only can operate the BSBR operations in order to achieve fast reference tracking performance but can also supply the regulated voltage $V_{\rm BSBR}$ by the pulse frequency modulation (PFM) control when the stored charge needs to supply other subblocks of the system. The fast reference tracking performance can ensure the voltage across the constant current generator is minimized to achieve high efficiency. As a result, the equation of luminance efficiency, which indicates the power transformation from the electric power to light luminance, can be written as

$$\eta = \frac{K \times P_{\rm LED}}{P_{\rm LED} + P_{CC} + P_{\rm dc-dc}} \tag{2}$$

where K indicates the converting coefficient from electric power $P_{\rm LED}$ to luminance of light. This value of K depends on different display techniques and backlight characteristics. This paper uses the FCS technique to enhance the value of K so that the backlight module can achieve better light luminance by means of smaller power dissipation $P_{\rm LED}$. Furthermore, the dc–dc converter with the BSBR technique can efficiently store and recycle extra charge, thereby reducing the value P_{CC} to improve the overall efficiency $\eta_{\rm module}$.

III. Buck-Store and Boost-Restore Technique

The output voltage for driving the series-connected R-LEDs is smaller than that for driving G-LEDs and B-LEDs. Thus, the output voltage of the boost dc–dc converter needs to switch between two output voltages, which are 9.3 and 12.4 V. In order to switch the output voltage between the two values, the reference voltage integrated in the chip needs to switch between 0.92 and 1.22 V. The proposed BSBR technique is applied to the boost dc–dc converter for achieving fast and efficient reference tracking performance. The function blocks and waveforms are illustrated in Fig. 5(a). The BSBR technique delivers extra charge and stores it on the capacitor $C_{\rm BSBR}$ once the output voltage $V_{\rm out}$ expresses much voltage stress on the constant current generator. As a result, the reference down-tracking is sped up and more charge is saved to achieve high efficiency compared to the conventional structure [13]. In other words, the LED backlight module can get higher efficiency due to low voltage headroom of the constant current generator. Furthermore, the BSBR technique recycles the stored charge back to the capacitor $C_{\rm Load}$ when the FCS technique changes the color of LED from red to green or blue. Therefore, the BSBR technique can efficiently recycle extra charge [14] and enhance the transient response of reference tracking. When the BSBR technique is enabled to store or restore extra charge, the boost converter is disabled to prevent the two power stages from being influenced by each other, i.e., the boost converter is shut down when the BSBR technique efficiently transfers the charge between the two capacitors $C_{\rm Load}$ and $C_{\rm BSBR}$. The architecture of the BSBR technique contains one BSBR power stage and one BSBR controller. The input node of the BSBR power stage is connected to the output node of the boost dc–dc converter. The output node of the BSBR power stage is named as $V_{\rm BSBR}$. There is a large capacitor $C_{\rm BSBR}$ connected at the node $V_{\rm BSBR}$ in order to store extra charge from the output node of the boost dc–dc converter. The stored charge can be utilized to pull the voltage

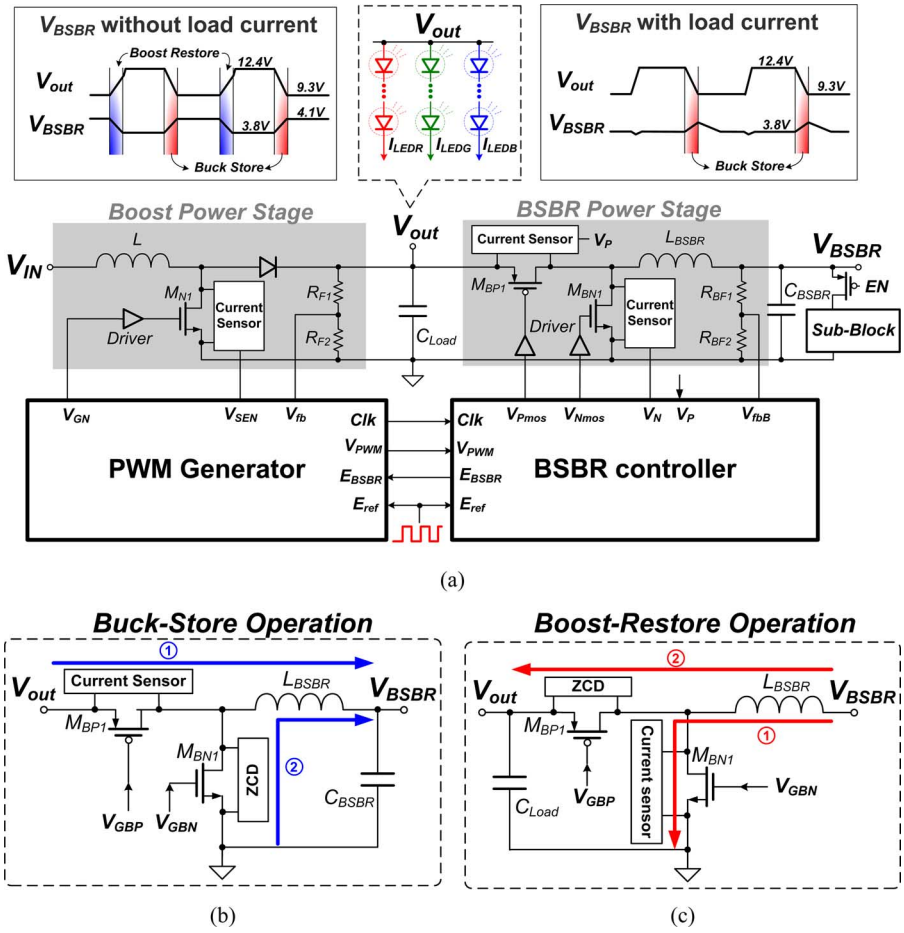


Fig. 5. (a) Proposed boost converter with BSBR technique and the timing diagram of the voltage $V_{\rm BSBR}$ with/without load current requested from another subblock in the LCD driving system. The BSBR power stage can be simplified as (b) buck-store operation and (c) boost-restore operation.

$V_{\rm out}$ back to a higher level or to drive another subblock in the LCD system. Furthermore, the BSBR power stage can regulate the steady output voltage for the subblock of LCD system when the digital signal EN is triggered from high to low level.

The signal $E_{\rm ref}$ generated by the LCD timing control system can indicate the display color, i.e., the high or low level of this signal represents the output voltage of the boost converter as high or low supplying voltage, respectively. The transition of the signal $E_{\rm ref}$ from low to high indicates that the output voltage $V_{\rm out}$ needs to be raised to high supplying voltage level. The stored charge should be restored back to the output voltage $V_{\rm out}$. On other hand, the transition of the signal $E_{\rm ref}$ from high to low indicates that the output voltage $V_{\rm out}$ needs to be reduced to the low supplying voltage level. As a result, extra charge should be stored in the BSBR capacitor $C_{\rm BSBR}$. The signal $E_{\rm ref}$ can be used to determine whether it is the buck-store or boost-restore operation. The signal $E_{\rm BSBR}$ is a signal to coordinate the two power stages, which are the boost converter and the BSBR power stage, in order to correctly control the two closed loops. The digital signal $V_{\rm PWM}$ indicates the current comparator output of the PWM generator, and it reflects the output voltage information. The signal $V_{\rm sen}$ is the sensing information of the inductor L current. The signals V_P and V_N indicate the sensing information of the inductor $L_{\rm BSBR}$ current.

A. Architecture of the BSBR Power Stage and Controller

The BSBR technique is composed of the BSBR operations. Extra charge is transferred from the output capacitor $C_{\rm Load}$ to the capacitor $C_{\rm BSBR}$ by the buck-store operation and restored from $C_{\rm BSBR}$ back to $C_{\rm Load}$ by the boost operation. The reference down-tracking utilizes the buck-store operation to rapidly reduce the output voltage of the boost converter from the high to low supplying voltage level. The BSBR controller is enabled to turn on the p-type power transistor M_{BP1} first to increase the inductor current. The duty cycle is determined by the closed loop of the BSBR controller. After turning off the M_{BP1}, the BSBR controller turns on the n-type power transistor M_{BN1} to decrease the inductor current. In addition, the current-sensing circuit of p-type power transistor M_{BP1} is utilized to set the maximum delivering current, and the current-sensing circuit of n-type power transistor M_{BN1} is used as the zero-current-detector (ZCD) mechanism for avoiding the reversal inductor current releasing to ground. The procedure that the output voltage $V_{\rm out}$ delivers charge to the capacitor $C_{\rm BSBR}$ for storing extra charge is similar to the operation of a buck converter [15] that steps down the output voltage $V_{\rm out}$ to the voltage $V_{\rm BSBR}$, and the BSBR power stage can be simplified as the buck-store operation illustrated in Fig. 5(b). For the reference up-tracking operation,

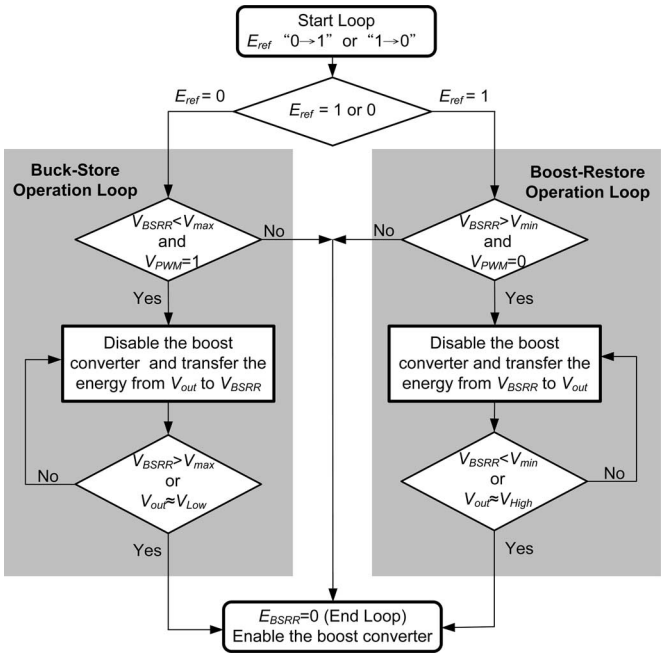


Fig. 6. Flowchart of the BSBR tracking algorithm.

the system turns on the n-type power MOSFET M_{BN1} to increase the inductor current at first, and then, turns on the p-type power transistor M_{BP1} to decrease the inductor current after the power MOSFET M_{BN1} is turned off. The charge stored on the capacitor $C_{\rm BSBR}$ can be restored back to the capacitor $C_{\rm Load}$. Similarly, the current-sensing circuits of p-type and n-type power transistors are operated for ZCD and current-limiting mechanism, respectively. Thus, $V_{\rm BSBR}$ steps up the output voltage $V_{\rm out}$ through the operation of the boost converter, as shown in Fig. 5(c). Therefore, the BSBR technique can rapidly pull down the output voltage $V_{\rm out}$ from 12.4 to 9.3 V and raise $V_{\rm out}$ back to 12.4 V from 9.3 V when driving the G-LEDs and B-LEDs. Furthermore, the BSBR power stage is also designed as a switching converter to regulate a steady voltage at node $V_{\rm BSBR}$ by the simple PFM control when the BSBR technique is disabled.

B. Tracking Algorithm of the BSBR Technique

The BSBR power stage is controlled by the three operation loops (buck-store operation, boost-restore operation, and PFM) to pull down/up the output voltage or regulate the BSBR voltage $V_{\rm BSBR}$. Therefore, the tracking algorithm of the BSBR technique is necessary to choose the appropriate operation loops for avoiding incorrect switching sequences. The algorithm is described by the flowchart in Fig. 6 starting from the transition of the signal $E_{\rm ref}$ from high to low or low to high. For the buck-store operation, this algorithm estimates the values of the voltage $V_{\rm BSBR}$ and the PWM signal $V_{\rm PWM}$ to decide whether the charge needs to store in the BSBR capacitor $C_{\rm BSBR}$ or not. When all of the controller signals are in the correct state, the BSBR power stage increases the inductor current by means of energy delivering from the output voltage $V_{\rm out}$. Hence, the charge is transferred to the capacitor $C_{\rm BSBR}$ every switching cycle. The boost converter is disabled in the meantime in order not to disturb the closed loop of the BSBR power stage.

When the output voltage $V_{\rm out}$ approaches to the low supplying voltage ($V_{\rm Low}$) or the voltage $V_{\rm BSBR}$ exceeds the predefined voltage $V_{\rm max}$, the algorithm ends the buck-store operation loop and the BSBR power stage is controlled by the PFM operation. In succession, the boost converter is enabled to regulate the output voltage $V_{\rm out}$. Consequently, the voltage $V_{\rm BSBR}$ is increased due to extra charge stored on the BSBR capacitor $C_{\rm BSBR}$.

For reference up-tracking response, the algorithm will enable the boost-restore operation loop if the signals $V_{\rm BSBR}$ and $V_{\rm PWM}$ are set by the correct values. The stored charge is transferred from the BSBR capacitor $C_{\rm BSBR}$ to the output load capacitor $C_{\rm Load}$, and thereby steps up the output voltage. Until the voltage $V_{\rm BSBR}$ is lower than the predefined minimum voltage $V_{\rm min}$ or the output voltage $V_{\rm out}$ approaches to the high supplying voltage $V_{\rm High}$, the boost-store operation loop is ended, and then, the output voltage will be regulated by the boost converter. Furthermore, the algorithm also determines the function of current-sensing circuit in the different power transistors M_{BN1} and M_{BP1} as ZCD or current-limiting mechanism.

When the BSBR technique is disabled by the tracking algorithm, the voltage $V_{\rm BSBR}$ is also designed to supply a regulated voltage by PFM operation for another subblock in the LCD system. Therefore, this voltage should be kept constant to prevent the subblock in this system from being affected by the voltage variation [8], [9]. Therefore, $C_{\rm BSBR}$ (10 μF) is designed larger than $C_{\rm Load}$ (1 μF), and the voltage $V_{\rm BSBR}$ only rises one-tenth of the output voltage due to the law of the charge conservation ($Q \equiv C \times V$). In this design, $V_{\rm BSBR}$ is used to turn on white LEDs. Furthermore, the maximum current supplied by the PFM operation of BSBR controller is about 100 mA in this design.

C. Efficiency of Charge Transition

The BSBR technique is utilized to transfer extra charge between the capacitors $C_{\rm Load}$ and $C_{\rm BSBR}$. The extra charge energy can be expressed as

$$W_{\rm cap} = \frac{1}{2} C_{\rm Load} \Delta V^2 \tag{3}$$

where ΔV is the different voltage between high and low supplying voltage. During the transforming procedure, part of the energy is consumed by the equivalent ON-resistance of power transistors (M_{BN1} and M_{BP1}). The energy stored on the capacitor is also wasted on the feedback resistors (R_{BF1} and R_{BF2}) during the transition period depending on the FCS frequency. Therefore, the transforming efficiency can be approximated by

$$\eta_{\rm tran} = \frac{W_{\rm cap} - W_{R\_\rm ON} - W_{V_{\rm BSBR}}}{W_{\rm cap}} \tag{4}$$

where $W_{R\_\rm ON}$ and $W_{V_{\rm BSBR}}$ represent the energy consumption on the power transistor and feedback resistor, which are shown as

$$\begin{aligned} W_{R\_\rm ON} &= I_{\rm avg}^2 R_{ds\_\rm ON}(T_{\rm up} + T_{\rm down}) \\ &= 2 I_{\rm avg} R_{ds\_\rm ON} C_{\rm Load} \Delta V \end{aligned} \tag{5}$$

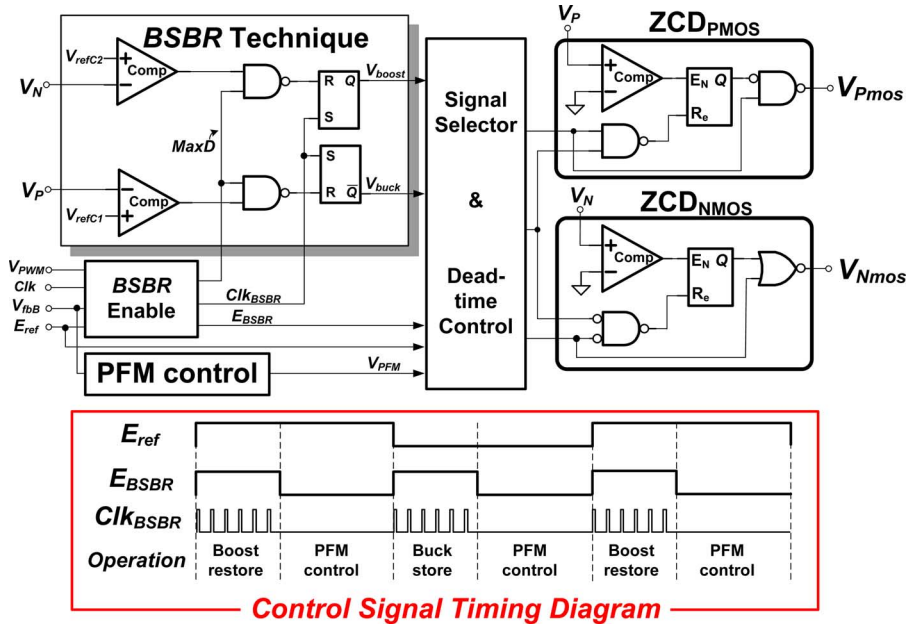


Fig. 7. Implementation of the proposed BSBR controller and the control signal timing diagram.

$$W_{V_{\rm BSBR}} = \frac{V_{\rm BSBR}^2}{R_{BF1}+R_{BF2}} T_{\rm FCS} = \frac{V_{\rm BSBR}^2}{(R_{BF1}+R_{BF2}) f_{\rm FCS}} \tag{6}$$

where R_{ds_ON} is the equivalent ON-resistance of power transistors, $I_{\rm avg}$ is the average transforming current during up- or down-reference tracking, $C_{\rm Load}$ is the output capacitance, $T_{\rm FCS}$ is the period of the FCS technique, and $T_{\rm up}$ and $T_{\rm down}$ are the transient time of up- and down-reference tracking, respectively. According to (5), small R_{ds_ON} and $I_{\rm avg}$ can reduce the energy consumption of W_{R_ON}. However, small R_{ds_ON} leads to larger chip area due to large power transistors, and thus, the value of R_{ds_ON} can be decreased depending on the chip area limitation. On the other hand, small average current $I_{\rm avg}$ results in longer transient time. Thus, in this proposed design, the maximum transforming current is designed to about 0.5 A, which is smaller than the conventional current-limiting mechanism. In addition, according to (6), large feedback resistors (R_{BF1} and R_{BF2}) and small $T_{\rm FCS}$ can reduce the value of energy $W_{V_{\rm BSBR}}$. However, the period of $T_{\rm FCS}$ depends on the speed of liquid crystal rotation. As a result, a large resistor is chosen to improve the transforming efficiency.

IV. Implementation of the BSBR Technique

A. Implementation of the Proposed BSBR Controller

The proposed BSBR controller and its control signal timing diagram are shown in Fig. 7. Basically, the operation mode of BSBR power stage can be divided into two parts, which are the PFM operation and the BSBR technique. The BSBR enable circuit is designed to implement the BSBR tracking algorithm, as shown in Fig. 8. This algorithm utilizes the signals V_{fbB} and $V_{\rm PWM}$ to appraise whether the system is suitable for transforming extra charge or not. Therefore, when these two conditions are suitable to enable the BSBR technique, this circuit will generate the signal $E_{\rm BSBR}$ to enable or disable the boost converter and the PFM operation of the BSBR controller. Moreover, the signals *Clk* and $E_{\rm BSBR}$ produce the signal $Clk_{\rm BSBR}$ to increase the inductor current of the BSBR power stage for transferring the energy at a fixed frequency. Furthermore, the signal selector utilizes these two signals $E_{\rm BSBR}$ and $E_{\rm ref}$ to determine the operation mode and disable either the $\rm ZCD_{PMOS}$ or $\rm ZCD_{NMOS}$ mechanism for avoiding incorrect switching. Therefore, this proposed BSBR technique uses these digital signals to determine the function of the BSBR power stage as buck-store (down-reference tracking) or boost-restore (up-reference tracking) operation. Moreover, V_N and V_P are sensing signals of power transistor current (M_{BN1} and M_{BP1}). The BSBR technique uses these two signals V_N and V_P to decide the maximum delivering current. In normal condition, the voltage $V_{\rm BSBR}$ is regulated by the PFM controller. When the signal $V_{\rm BSBR}$ is lower than 3.8 V, the PFM controller turns on the power transistor M_{BP1} at a fixed duty to provide energy for regulating the voltage $V_{\rm BSBR}$. As a result, the PFM operation can regulate the voltage $V_{\rm BSBR}$ according to the load current condition. On the other hand, the BSBR technique is utilized to transfer the charge between the two capacitors $C_{\rm Load}$ and $C_{\rm BSBR}$. The signal $E_{\rm ref}$ generated by the timing control system defines output voltage level of the boost converter, as described in Section III. Additionally, when the BSBR power stage is controlled by the BSBR technique, the PFM operation will be disabled until the BSBR tracking algorithm ends the loop.

For the buck-store (down-reference tracking) case, the current-sensing circuits of power transistors M_{BP1} and M_{BN1} illustrated in Fig. 5(a) are utilized to act as current limiting and ZCD mechanism, respectively. The transistor M_{BP1} is turned on, and then, the inductor current is increased to ramp up. The transistor M_{BP1} is turned off when the inductor current exceeds

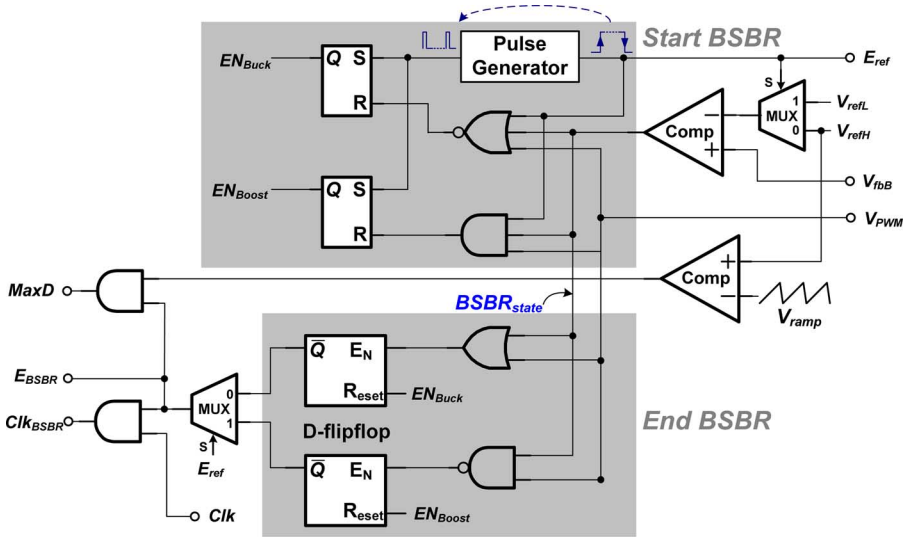


Fig. 8. Function block of the proposed BSBR enable circuit.

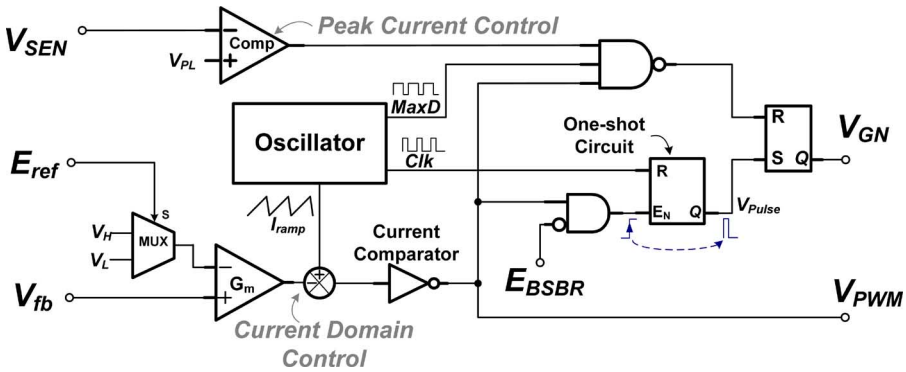


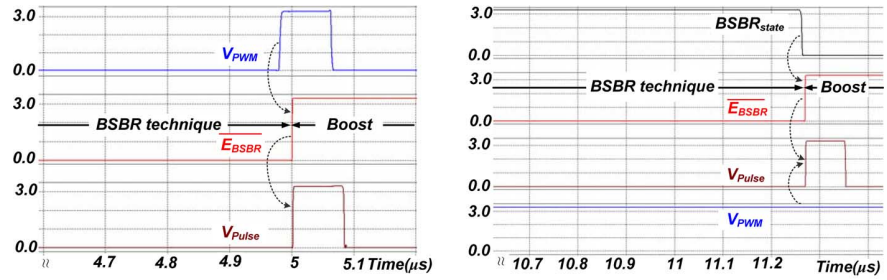
Fig. 9. Schematic of the PWM generator with characteristic of fast response and stability.

the predefined maximum current. After the deadtime period, the transistor M_{BN1} is turned on to decrease the inductor current. In succession, the BSBR power stage undergoes the switching activities, turning on and off the transistors M_{BP1} and M_{NB1} alternately. Hence, extra charge can be safely and quickly transferred to the BSBR capacitor $C_{\rm BSBR}$. When the signal $V_{\rm PWM}$ transits from low to high or $V_{\rm BSBR}$ is higher than $V_{\max}$, the buck-store algorithm loop is ended. The signal $Clk_{\rm BSBR}$ is disabled and the inductor current will not be increased to ramp up anymore. The remaining inductor current is decreased through the power transistor M_{BN1} to the capacitor. When the reversal of the inductor current happens, the $\rm ZCD_{NMOS}$ is used to turn off the transistor M_{BN1} for alleviating the problem of the reverse inductor current flowing to the ground. On the contrary, the function of the $\rm ZCD_{PMOS}$ is disabled to avoid the error digital control signal. For the reference up-tracking case, the boost-restore operation is selected by the BSBR enable circuit according to the BSBR algorithm. At first, the BSBR turns on the power transistor M_{BN1} to increase the inductor current, and then, transfers extra charge to the capacitor $C_{\rm Load}$. Hence, the boost-restore technique senses the n-type power transistor M_{BN1} to decide the discharging time and uses the $\rm ZCD_{PMOS}$ to alleviate the boost converter to provide the unnecessary energy to the capacitor $C_{\rm BSBR}$. When the signal $V_{\rm PWM}$ is triggered to low or $V_{\rm BSBR}$ is lower than the voltage $V_{\min}$, the boost-restore operation is completed.

B. PWM Generator of the Boost Converter

The PWM generator is the main circuit of the boost converter, as shown in Fig. 9. The LED backlight driver uses the boost converter to provide enough voltage and current to overcome the forward voltage of series LEDs. This PWM generator translates all signals to current domain [16] in order to compensate the system without any large external compensation capacitors [17], [18]. The G_m amplifier [11] with high-bandwidth characteristic is used to convert the voltage difference between V_{fb} and $V_{\rm ref}$ to a correct current signal according to the output voltage condition. Therefore, the response of this converter can result in fast load/line transient [19] and reference tracking.

Since the LED driver turns on the series LEDs after the liquid crystal being rotated to the correct position according to the image data as discussed in Section I, the PWM generator need not increase the inductor current every switching period. Hence, when the timing control system turns on the LED driver and leads to V_{fb} drop below the reference voltage V_H



(a) (b)

Fig. 10. Enable sequence of boost converter resulted from the end of BSBR tracking algorithm. (a) Buck-store operation is ended by the signal $V_{\rm PWM}$ and the boost converter can immediately be enabled by the pulse signal $V_{\rm pulse}$ to regulate the output voltage. (b) Boost-restore operation is ended by the signal $\rm BSBR_{state}$ and the PWM generator can immediately control the boost converter.

or V_L, the signal $V_{\rm PWM}$ instead of the clock signal enables the pulse control circuit to turn on the power transistor M_{N1}, as described in Fig. 5(a).

The reset signal of the PWM signal is determined by three loops. In the normal condition, the current-domain control forms the linear loop composed of G_m amplifier and current comparator to determine the duty ratio. The peak current control uses the current information of M_{N1} to turn off the M_{N1} preventing the chip from being damaged by large current. Besides, the PWM system applies the maximum duty loop to ensure that the inductor current is transferred to the output during a period. In this proposal, the maximum duty is set as high as 80%. Hence, these three control loops can effectively regulate the boost converter. During the BSBR technique operation, the digital signal $E_{\rm BSBR}$ transits to high and prevents the boost converter from being enabled by the pulse signal of the pulse control. There are two conditions that decide the end of the buck-store algorithm loop.

One condition occurs when $V_{\rm BSBR}$ is higher than the predefined maximum voltage, i.e., no extra charge on $C_{\rm Load}$ needs to be transferred to the capacitor $C_{\rm BSBR}$. The signal $V_{\rm PWM}$ indicates that the output voltage information is still in the low level to keep the power transistor M_{N1} OFF. Once the output voltage drops below the reference voltage V_L, the boost converter starts switching activities to regulate the output voltage. This condition is designed to prevent the chip from being damaged by excess voltage $V_{\rm BSBR}$. In general, the buck-store algorithm is ended when the signal $V_{\rm PWM}$ transits from low to high to end the buck-store algorithm. Accordingly, $E_{\rm BSBR}$ instantly transits from high to low level to generate the pulse signal $V_{\rm pulse}$, as depicted in Fig. 9, and the sequence is shown in Fig. 10(a).

Therefore, the boost converter can be immediately controlled by the PWM generator. Similarly, the BSBR technique ends the boost-restore algorithm loop when the output voltage exceeds the high supplying voltage or $V_{\rm BSBR}$ is lower than the predefined minimum voltage $V_{\rm min}$. Nevertheless, some power loss occurs in the procedure of transforming energy. Thus, the boost-restore algorithm loop is usually ended once the $V_{\rm BSBR}$ is lower than $V_{\rm min}$. In the meanwhile, the signal $\rm BSBR_{state}$ described in Fig. 8 transits from high to low level, and $V_{\rm PWM}$ is still in the high level. Therefore, the pulse signal from one shot circuit is immediately generated to turn on the transistor M_{N1} for increasing the inductor current and stepping up the output voltage and the signal sequence is shown in Fig. 10(b). As the BSBR technique ends, the PWM generator can be activated without any delay to avoid the voltage drop and use the peak current control loop to rapidly pull up the output voltage. Therefore, this converter with BSBR technique can quickly track the output voltage that the series LEDs need.

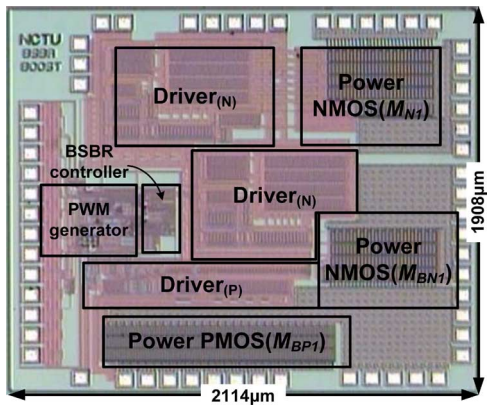


Fig. 11. Chip micrograph.

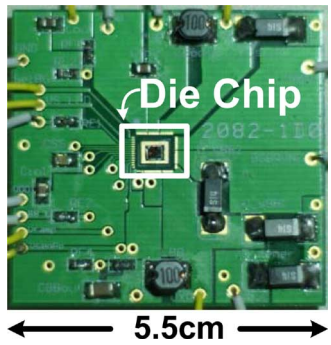


Fig. 12. Prototype for testing the RGB LED driver with the BSBR technique.

V. Measured Results

The chip containing the boost converter and BSBR technique was fabricated by a 0.25-μm BCD process, and Fig. 11 shows a die micrograph of the implement with the die area being $4.03\,\rm mm^2$, out of which the BSBR controller only occupies $0.072\,\rm mm^2$. The maximum allowable voltages for drain–source voltage and gate–source voltage are 40 and 12 V, respectively. The developed prototype is shown in Fig. 12. Table I summarizes the design parameters and the measurement results.

TABLE I
CHIP FEATURES

Fabrication Process	0.25μm BCD 40V 1P5M (Maximum V_{DS} = 40 and V_{GS} = 12V)
Chip Area	4.03mm^2(1908μm×2114μm)
Supply Voltage (V_{in})	3.3-6V
Output Voltage (V_{out})	9-15V
Control Voltage (V_{DD})	3.3V
Switching Frequency	1MHz
Maximum Load Current	300mA
Inductor	L=10μH, L_{BSBR}=10μH
Capacitor	C_{Load}=1μF, C_{BSBR}=10μF
Maximum Efficiency of Charge Recycling	94%
Maximum Efficiency of Boost Converter	94.5%
Reference Tracking Speed	10μs for 9.3V→12.4V with I_{Load}=100mA 20μs for 12.4V→9.3V with I_{Load}=100mA

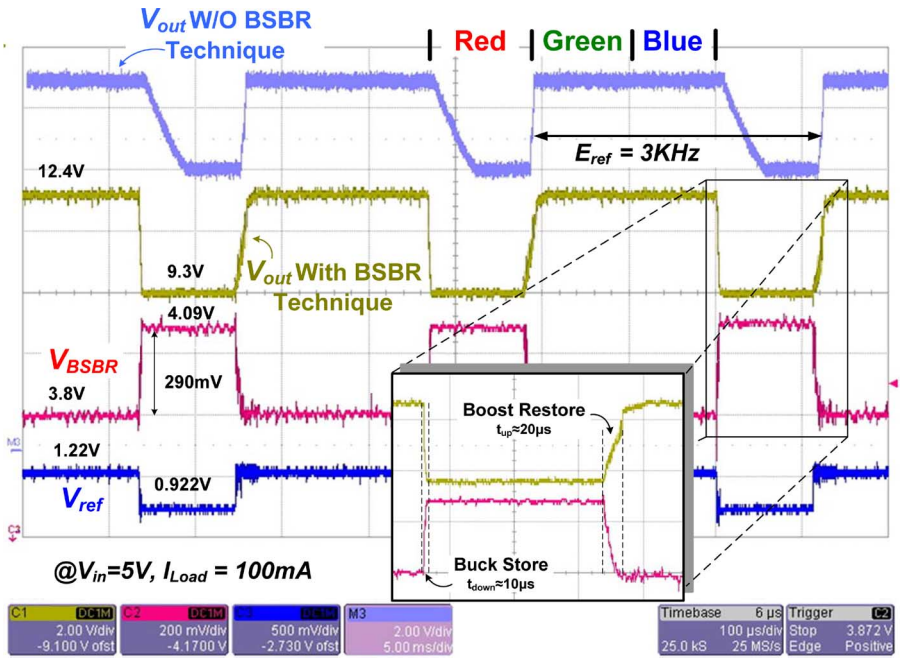


Fig. 13. Measured waveforms for reference tracking response with/without BSBR technique.

The prototype working with input voltage ranging from 3.3 to 6 V is applied to the RGB LED backlight module with FCS technique, and thus, the boost converter steps up the output voltage to 9.3 V for four-series R-LEDs and 12.4 V for four-series G- or B-LEDs. The values of the inductors L and $L_{\rm BSBR}$ are both chosen as 10 μH. The values of the capacitors $C_{\rm Load}$ and $C_{\rm BSBR}$ are chosen as 1 and 10 μF in this proposal. Besides, the voltage $V_{\rm BSBR}$ is regulated around 3.8 V to turn on white LED implemented on the flashlight of the portable device. However, the capacitor $C_{\rm BSBR}$ can be chosen to be any types of capacitors according to different applications. The frequency of the FCS technique usually utilizes the 60 Hz switching frequency to switch different color LEDs. Nevertheless, in order to ensure the functionality and reliability of the developed prototype, a higher switching frequency (3 kHz) is utilized to test the performance and observe the response of the reference tracking procedure, as shown in Fig. 13. The output voltage is dynamically stepped up to 9.3 and 12.4 V according to the digital signal $E_{\rm ref}$ from the FCS technique when the load current is 100 mA. For reference down-tracking response, the output voltage without BSBR technique drops slowly and causes large power consumption on the constant current generator. However, the output voltage with BSBR technique can transfer extra charge to the capacitor $C_{\rm BSBR}$ so that the period of reference down-tracking is smaller than 10 μs and five times faster than that of the traditional converter when load current is 100 mA. Furthermore, extra charge stored on the capacitor $C_{\rm BSBR}$ is more efficient than prior art [13], [20], [21]. Therefore, the voltage $V_{\rm BSBR}$ is raised from 3.8 to 4.09 V under no-load situation when the boost converter changes the output voltage level to turn on the R-LEDs. On the contrary, when the output voltage is raised from 9.3 to 12.4 V, the boost-restore technique is

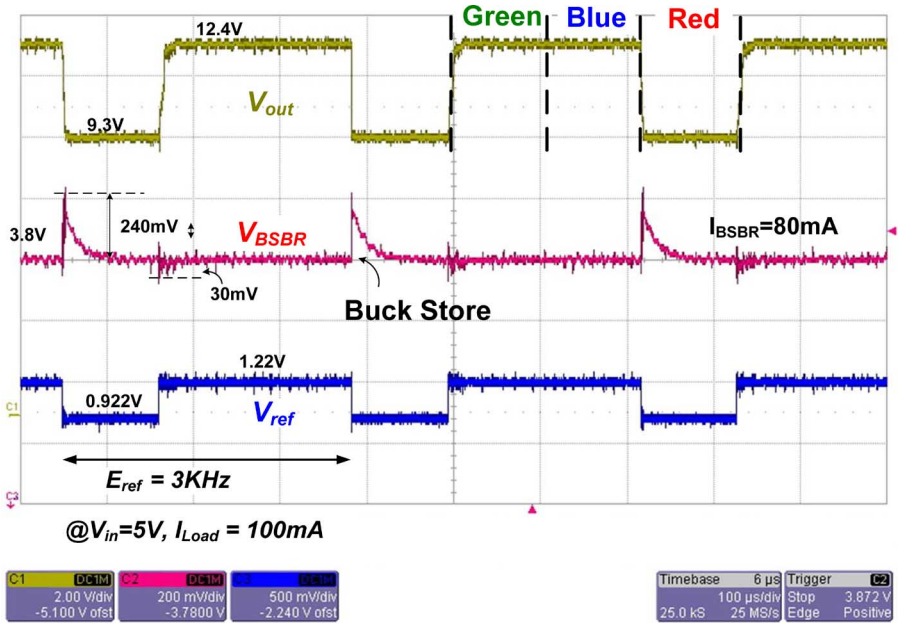


Fig. 14. Measured waveforms showing the BSBR power stage with 80 mA load current (I_{BSBR}) for forwarding white-LED. The PFM control and BSBR techniques are used to maintain the voltage V_{BSBR} above 3.8 V.

enabled to transfer the stored charge back to the capacitor C_{Load}. Until the voltage V_{BSBR} is smaller than 3.8 V, the boost-restore technique is disabled. In succession, the boost converter continues to step up the output voltage to the desired voltage 12.4 V. As shown in Fig. 13, the output voltage has two different rising slopes when the output voltage is stepping up from 9.3 to 12.4 V. The first slope is controlled by the BSBR technique and the second one is by the boost converter. Since the BSBR technique uses the smaller transforming current for reducing the power consumption, the first slope is smaller than the second one. However, the up-tracking response is smaller than 20 μs and fast enough for the FCS technique. Furthermore, the maximum efficiency of the extra charge recycling can be up to 94%.

Fig. 14 shows the measured waveforms of the BSBR power stage with 80 mA load current. Because the forwarding voltage of white LED is close to 3.5 V, the voltage V_{BSBR} must be set above 3.7 V. Therefore, the PFM control and BSBR techniques are used to regulate V_{BSBR} to be 3.8 V in this application. When the output voltage drops from 12.4 to 9.3 V, the BSBR technique is enabled to transfer the extra charge, and thus, the voltage V_{BSBR} is instantly increased owing to buck-store technique. When the buck-store technique is disabled, the PFM control technique continues to regulate the voltage V_{BSBR}. However, when the output voltage rises from 9.3 to 12.4 V, the boost-restore technique is still enabled at first. As mentioned before, the technique is disabled when the voltage V_{BSBR} is lower than 3.8 V, and then, the BSBR power stage is controlled by the PFM operation. Fig. 15 shows the measured efficiency of boost converter under different load currents with and without BSBR technique when input voltage is 5 V. The effective efficiency of LED backlight driver composed of boost converter and constant

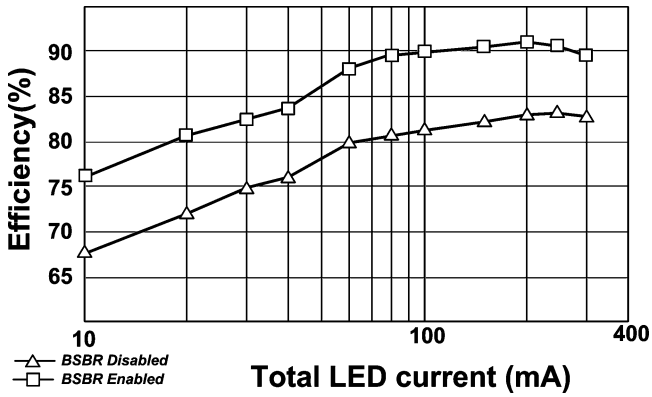
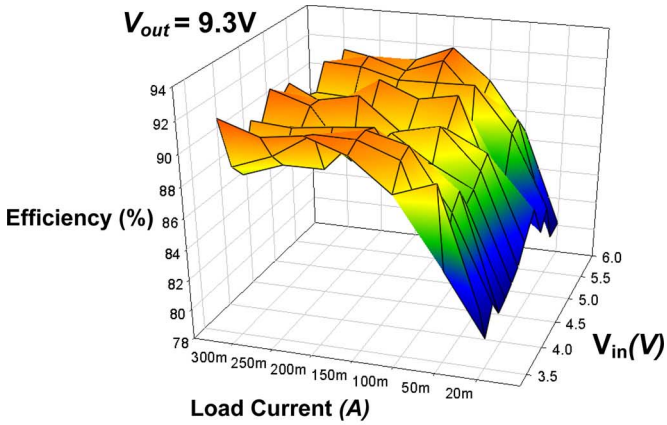


Fig. 15. Measured efficiency of the boost converter with and without BSBR technique enabled under different load current when input voltage is 5 V.

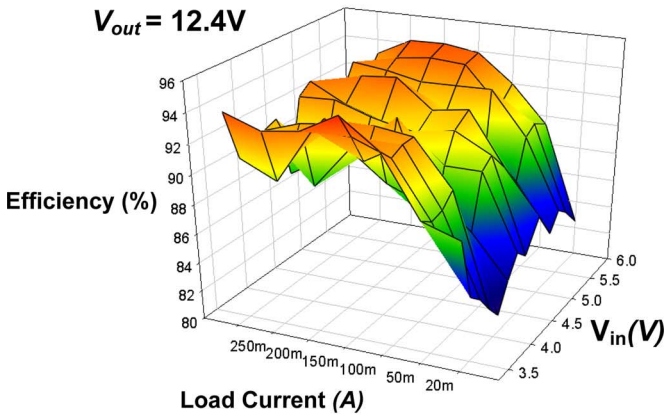
current generator is calculated as

$$\eta_{\mathrm{LED\_driver}} = \eta_{\mathrm{boost}} \times \frac{V_{\mathrm{LED}}}{V_{\mathrm{out}}} \tag{7}$$

where V_{LED} is the total voltage of the string LEDs and the V_{out} is the output voltage of the boost converter, as illustrated in Fig. 4. The variable $\eta_{\mathrm{LED\_driver}}$ indicates the efficiency of the LED driver. In addition, η_{boost} indicates the efficiency of the boost converter. Thus, the efficiency of LED backlight module with BSBR technique can be improved by 8%. Fig. 16(a) and (b) shows the measured efficiency of the boost converter versus load current under different input voltages when output voltages are 9.3 and 12.4 V, respectively. Moreover, the BSBR power stage not only can operate the BSBR techniques for reference tracking performance but can also supply the regulated voltage V_{BSBR} by the PFM operation technique.



(a)



(b)

Fig. 16. Measured efficiency of the boost converter versus load current under different input voltages are illustrated. (a) When output voltage is 9.3 V. (b) When output voltage is 12.4 V.

VI. Conclusion

The LED backlight module with FCS technique is becoming more and more popular due to low power consumption and high image quality. An RGB LED backlight driver is proposed for rapidly switching the output voltage between 9.3 and 12.4 V for driving four-series red and four-series green/blue LEDs in the backlight module, respectively. Since the converter produces large output voltage range, the reference tracking response and efficiency should be greatly taken into account. As a result, an innovative control mechanism, the BSBR technique, has been proposed to enhance the reference tracking response and reduce the power consumption of the LED backlight module. The proposed BSBR technique can store extra charge on the output capacitor to the recycling capacitor when the output voltage transits from high supplying voltage (12.4 V) to low supplying voltage (9.3 V). As a result, the power dissipation on constant current generator can be considerably improved. On the other hand, when the output voltage level is changed from low to high supplying voltage, the charge stored on the recycling capacitor can be used for raising the output voltage back to the high supplying voltage level. Therefore, extra charge can be recycled, and the overall power consumption of the backlight module can also be reduced. In addition, the regulated voltage can be utilized to implement other applications such as turning on white LEDs on the portable devices.

The proposed LED driver with BSBR technique was fabricated by 0.25 μm TSMC BCD 40 V technology. Experimental results show that the period of reference tracking procedure can be reduced within 20 μs during up-reference tracking and within 10 μs during down-reference tracking when the load current is about 100 mA. These results demonstrate that the fast reference tracking performance is achieved by the proposed BSBR technique. Furthermore, the maximum efficiency of charge recycling is up to 94% and the maximum efficiency of this boost converter is 94.5%. In this paper, the different display techniques were introduced and the BSBR technique applied for the FCS technique on the RGB LED backlight module was analyzed. Furthermore, it can efficiently recycle the extra charge and reduce the power consumption.

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