Chapter 3

Fabrication

The fabrication processes are discussed in this chapter. The first part is the self-alignment structure for bonding the multi-chip modules; the second is the micro optical bench, specifically the 135° mirror and photodetector integration in SOI substrates using SU-8.

3-1 Self alignment structures by KOH etching

Figure 3-1 shows the anisotropic etching equipments, including a hot plate and a temperature sensing bar to monitor and control the temperature of the solution. In addition, a magnetic stirrer is used to mix up the solution and keep the concentration and temperature uniform. The silicon wafer is anisotropically etched in a KOH/IPA solution at 80℃.

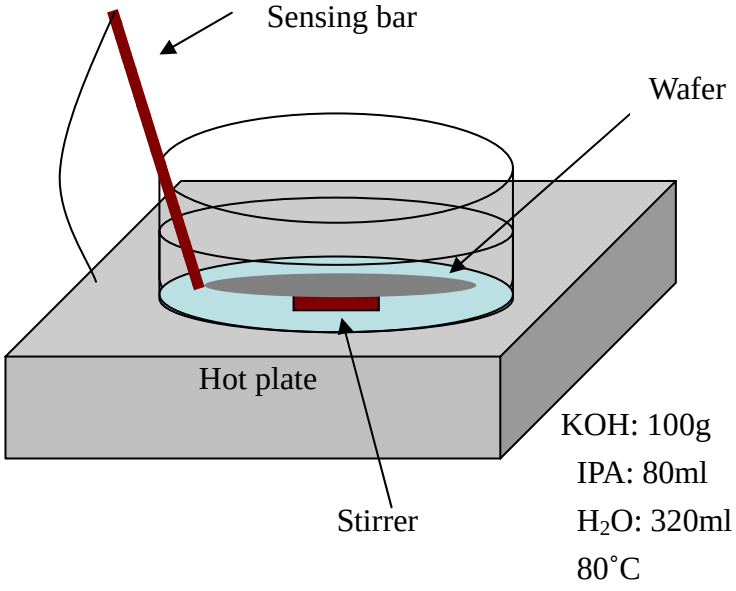


Figure 3-1: Equipments of the wet etching.

3-1-1 Fabrication process of self-alignment structures

Base on the design in Chapter 2, Figure 3-2 shows the layout of self-alignment structures. Figure 3-2 (a) shows the layout of groove structures and Figure 3-2 (b) shows the layout of ridge structures. The fabricated processes and cross sectional profiles along A-A' and B-B' are shown in Figure 3-3.

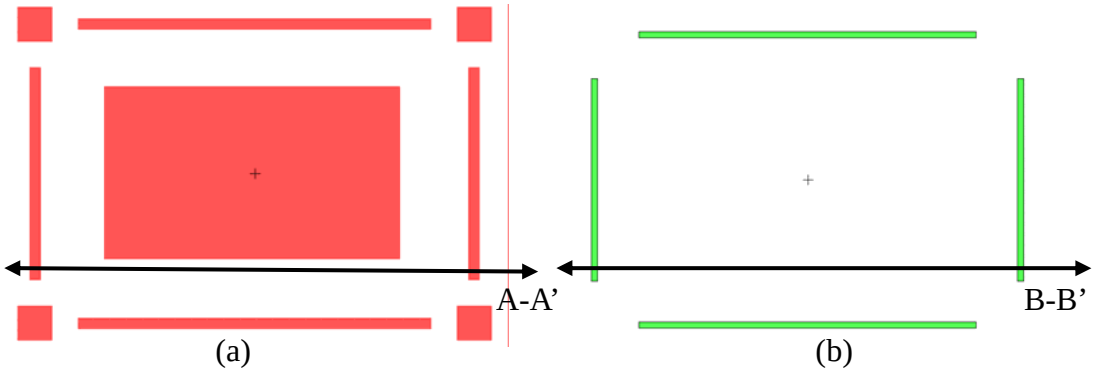


Figure 3-2: Layout of self alignment structure (a) groove structures (b) ridge structures.

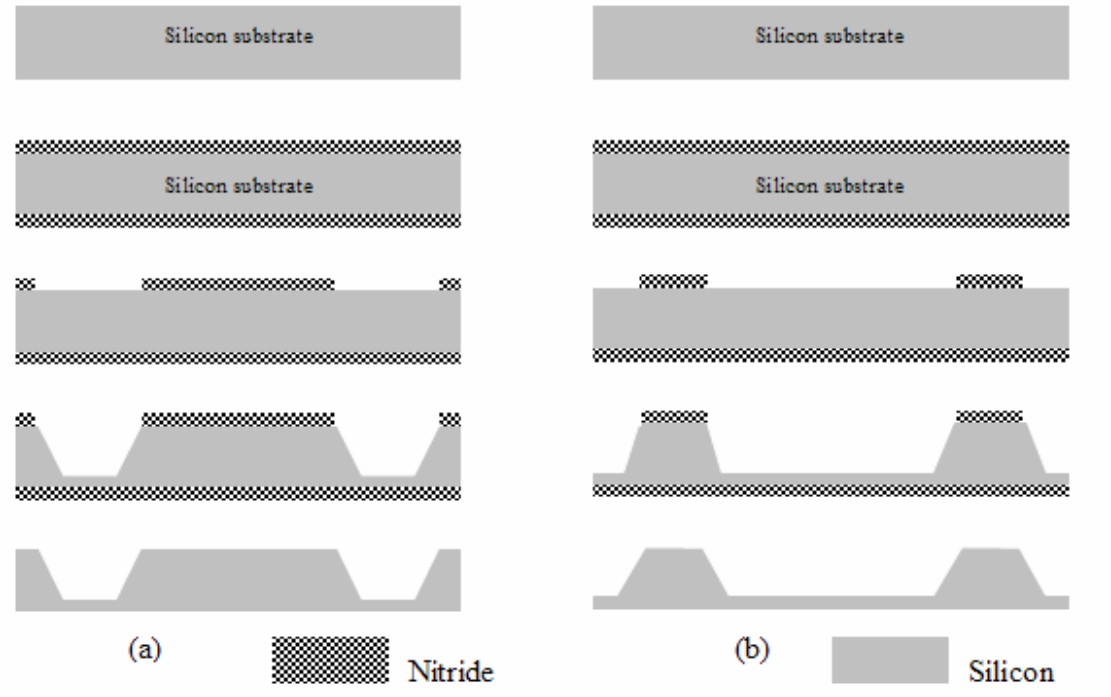


Figure 3-3: Fabrication process of the self-alignment structures. (a) groove structure (b) ridge structure.

- **Process flow**

(a) Groove structures (Figure 3-3(a))

In the first step, 0.1um-thick Si_3N_4 is deposited on the RCA cleaned bare silicon wafer by LPCVD. Then on the Si_3N_4 layer is spin coated HMDS and a layer of photoresist FH6400 as the etching mask for the subsequent Si_3N_4 RIE for the pre-alignment marks. Pre-alignment marks are used to find the crystalline orientation. Next, the groove or ridge area are patterned and aligned to the pre-alignment mark in the Si_3N_4 layer. Then, KOH solution is used to etch the silicon to form the groove structures. Finally, the Si_3N_4 layer is removed by H_3PO_4.

(b) Ridge structures (Figure 3-3(b))

The process flow of ridge structures is the same with groove structures. Only the layout is different.

3-1-2 Measurement of self alignment structures

Etching condition and equipment are discussed in Sec. 3-1. A WYKO-NT1100 interferometer is used to measure the depth of the structure and the smoothness of the (100) planes.

- **Average etching rate**

Figure 3-4 shows the measured etching rate of the (100) planes. A measurement was made every half hour for totally 2.5 hours. The average etching rate is 0.7um/min for the recipe discussed above. As shown in the figure, the rate shows variation because the temperature, concentration, and etching area are not always the same. So it is hard to control the depth by wet etching.

- **Smoothness**

The etching solution can affect the smoothness of the etched surfaces. Figure 3-5 (a) shows a scanning electron microscopy (SEM) picture of the etched (100) plane without IPA. Figure 3-5 (b) shows the measured average roughness to be about 250.96nm. Figure 3-6 shows the SEM picture and the smoothness of (100) plane etched with IPA. Compared with Figure 3-5, the average roughness is reduced to be about 50nm.

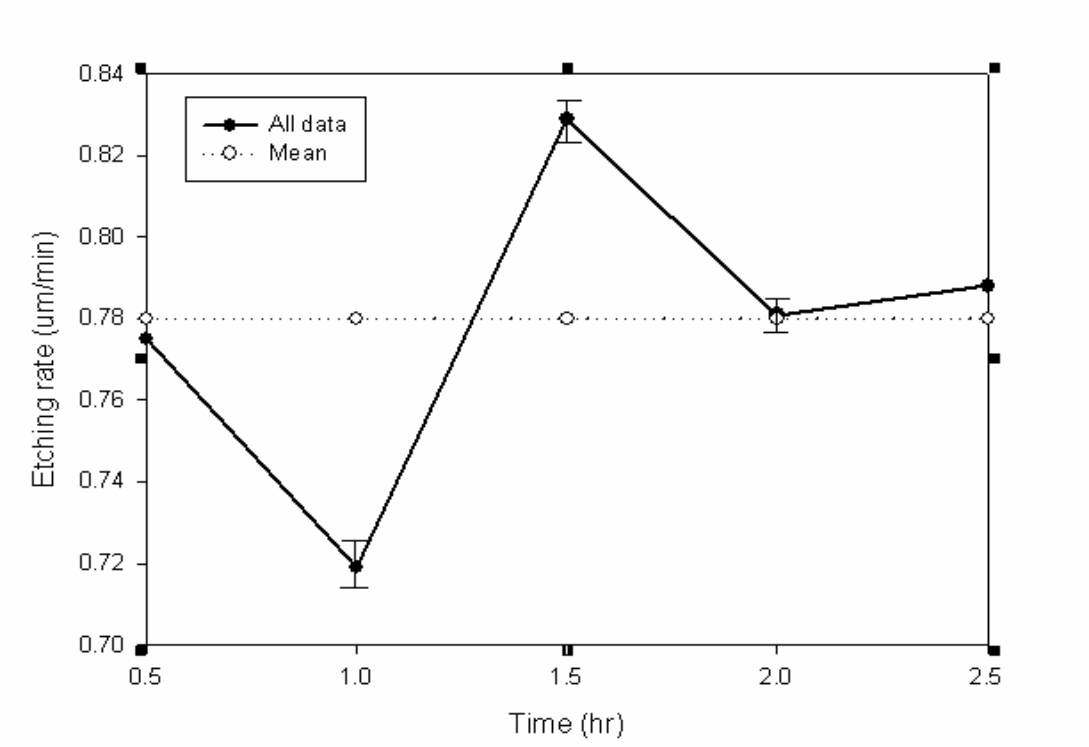
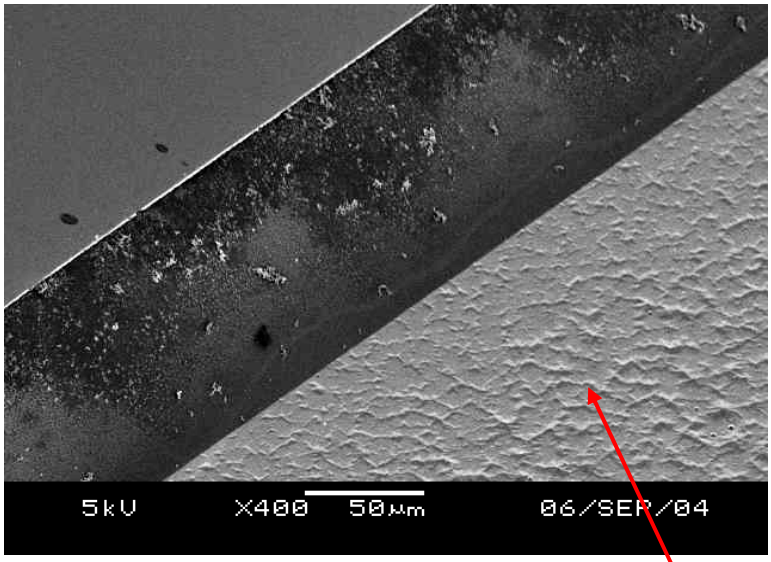
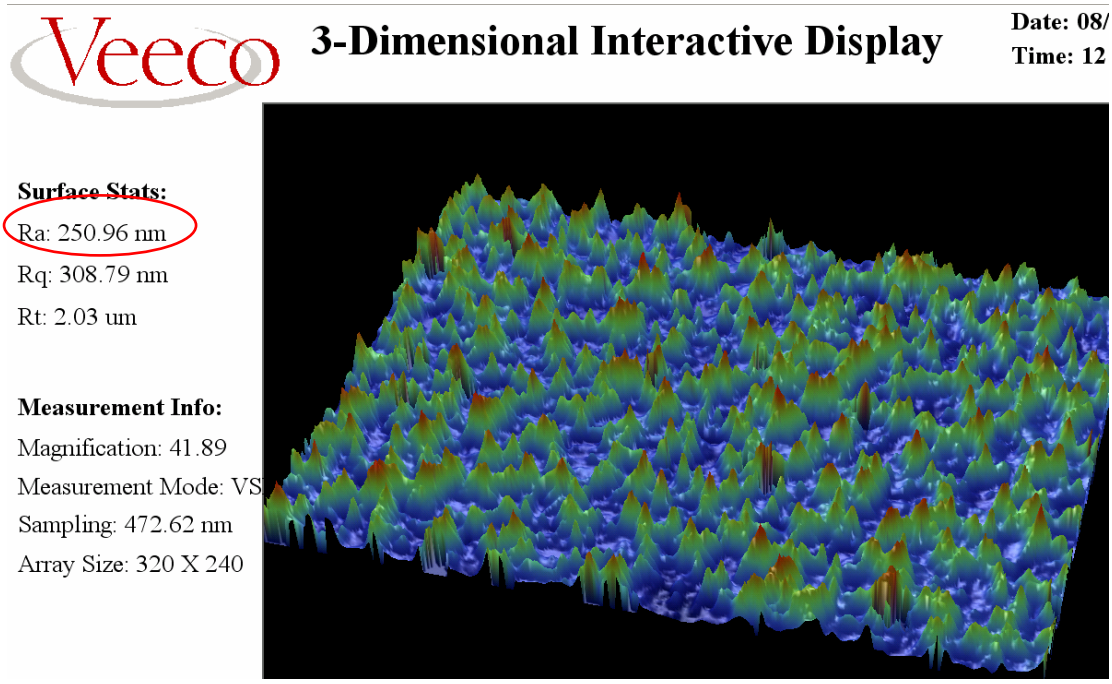


Figure3-4: Etching rate of the (100) planes.

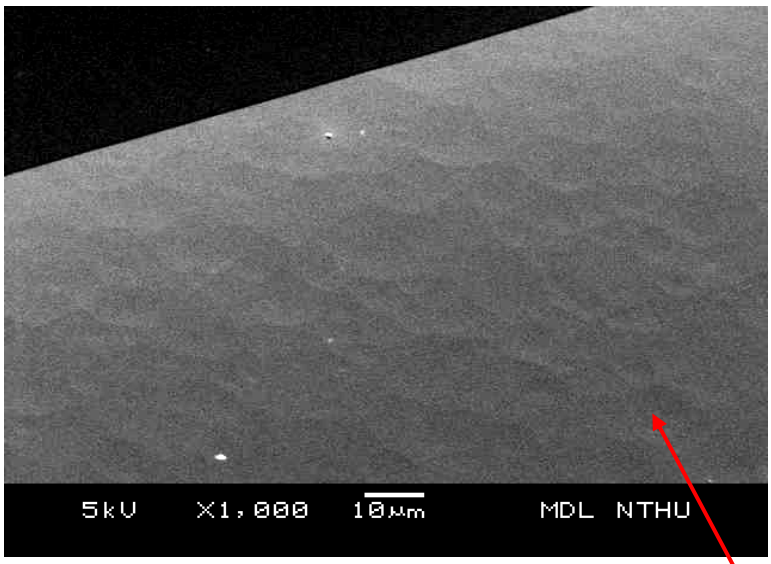


(a) Etched (100) surface.



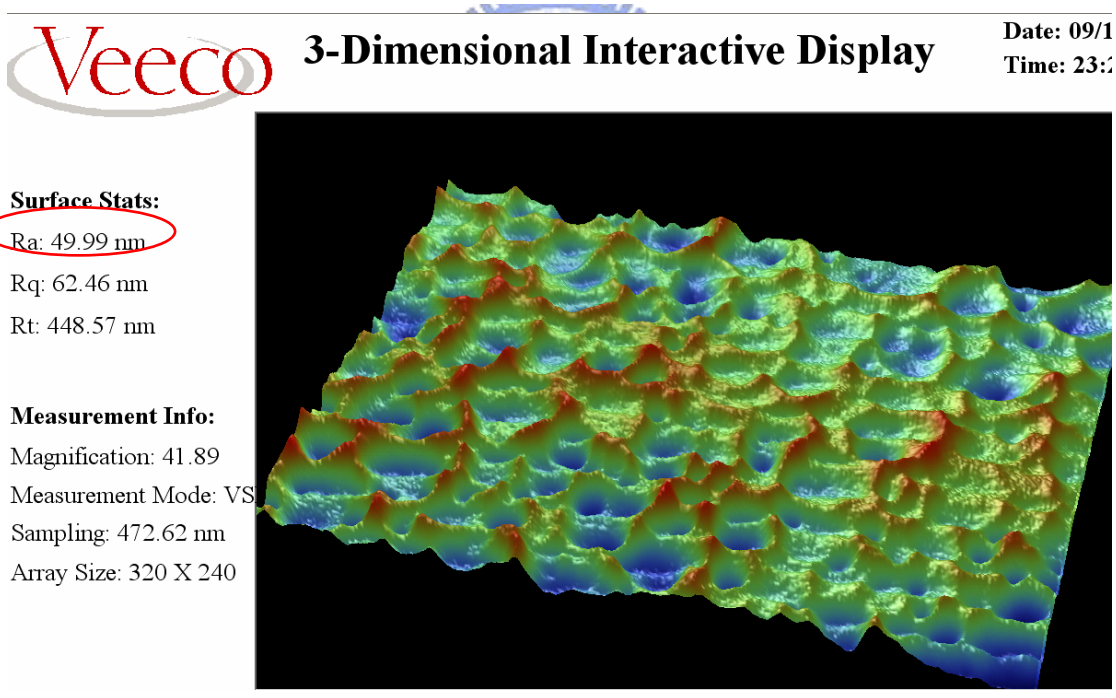
(b)

Figure 3-5: (a) SEM of the etched (100) surface without IPA. (b) WYKO measurement of the etched surface.



(a)

Etched (100) surface



(b)

Figure 3-6: (a) SEM of the etched (100) with IPA. (b) WYKO measurement of the etched surface.

3-1-3 Problems and discussion of self-alignment structures

In the fabrication process (shown in Figure 3-3), pre-alignment marks are generated to expose the crystal line orientation. These crudely aligned features can serve as alignment marks for the second, more precise photolithographic step. Otherwise, the etched misaligned (111) planes can be quite rough as shown in Figure 3-7. Figure 3-8 shows the (111) planes with pre-alignment and the smoothness are greatly improved. The smooth (111) plane can enhance the joint accuracy.

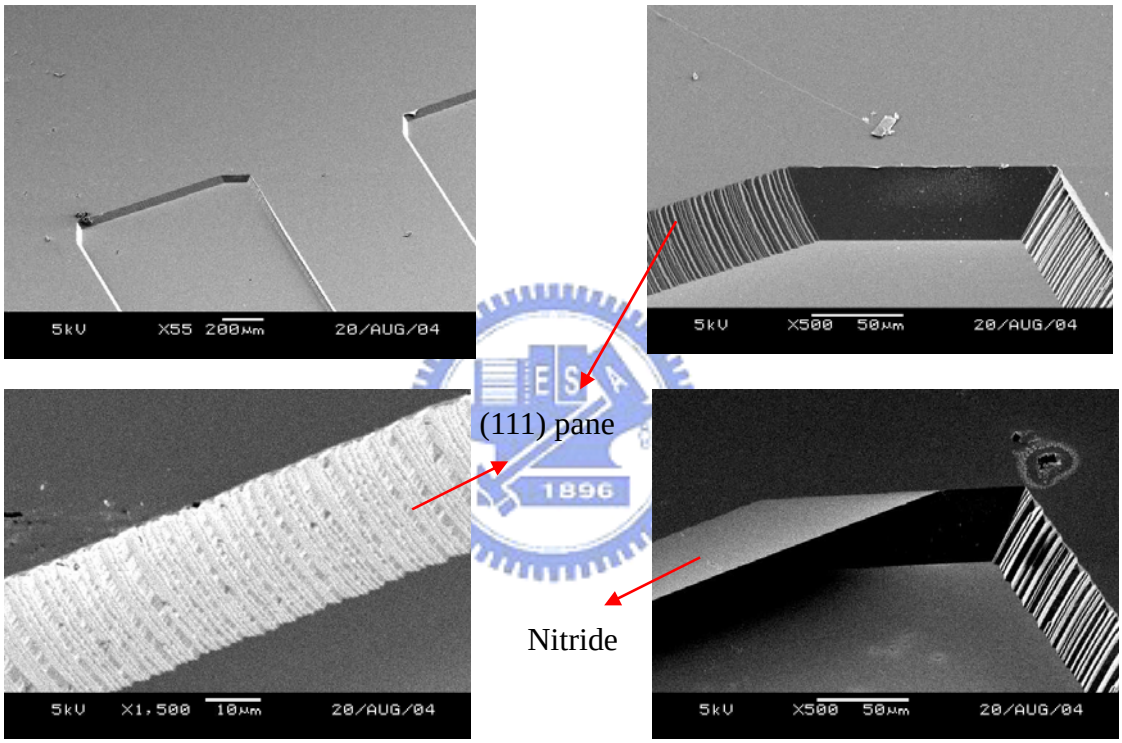


Figure 3-7: (111) faces without pre-alignment.

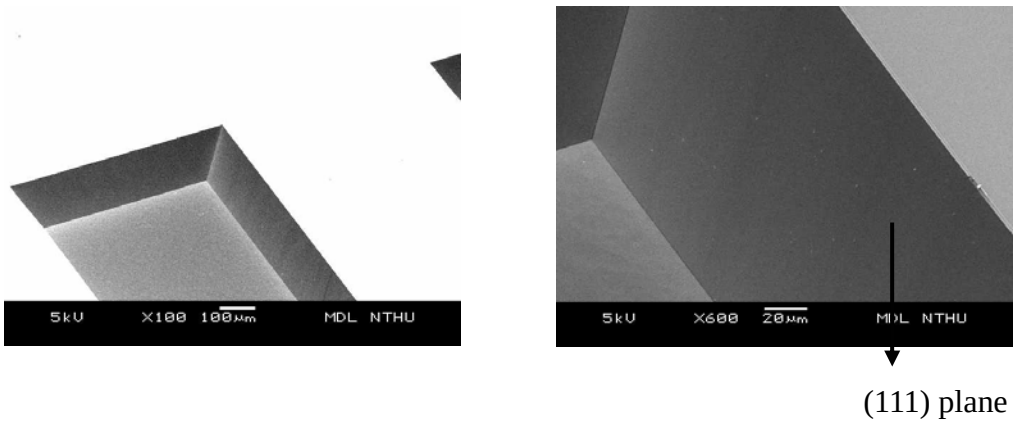


Figure 3-8: (111) face with pre-alignment.

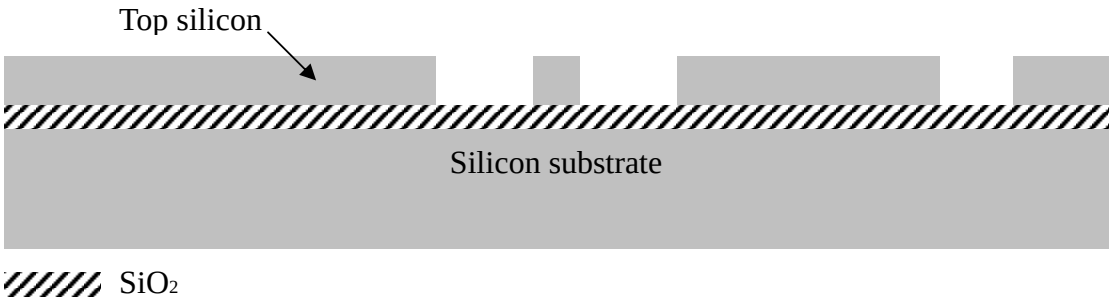
3-1-4 Conclusion

The precise etch depth control is difficult due to the variation of the etching rate. However, lateral alignment can still be achieved with large process tolerance, as discussed in Sec 2-2-1. Pre-alignment with the crystalline orientation proves to be an effective way to improve the smoothness of the etched (111) surfaces.

Since the silicon substrate is replaced with SOI substrates, the self alignment structures were not investigated in more details. Instead, a novel fabrication process is proposed to take advantage of the single crystalline nature of SOI substrates and the easiness of processing and optical transparency of SU-8.

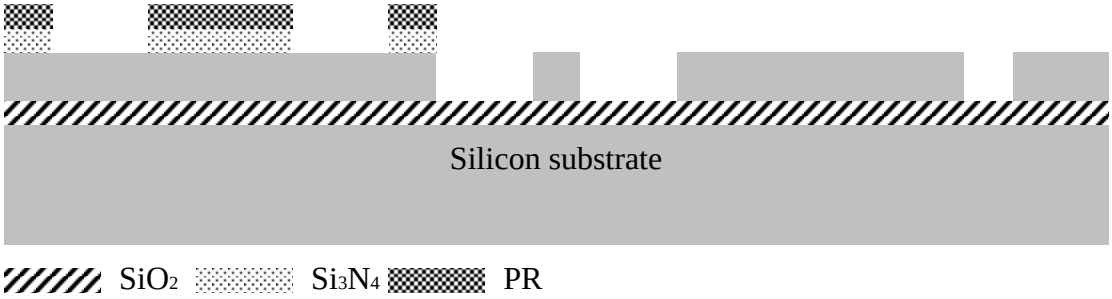
3-2 Integrated Device using SOI and SU-8

The integrated device is fabricated in a seven-mask process. In this section, the fabrication process is discussed. The A-A' crossection as shown in Figure 2-12 during processing is shown in Figure 3-9.

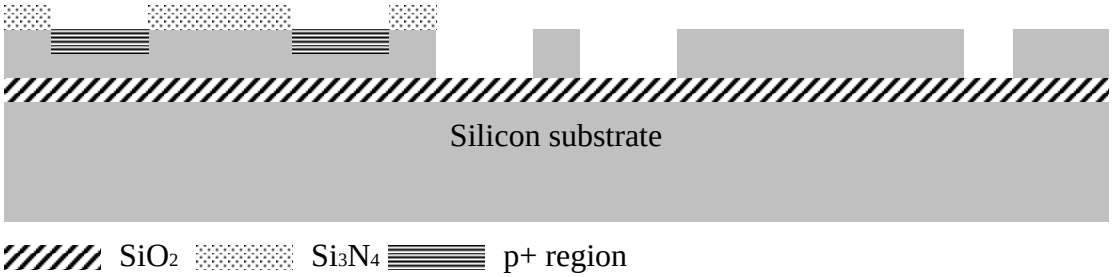


Step 1: Lithographically pattern the 5um-thick top silicon by inductively coupled plasma reactive ion etching ICP RIE.

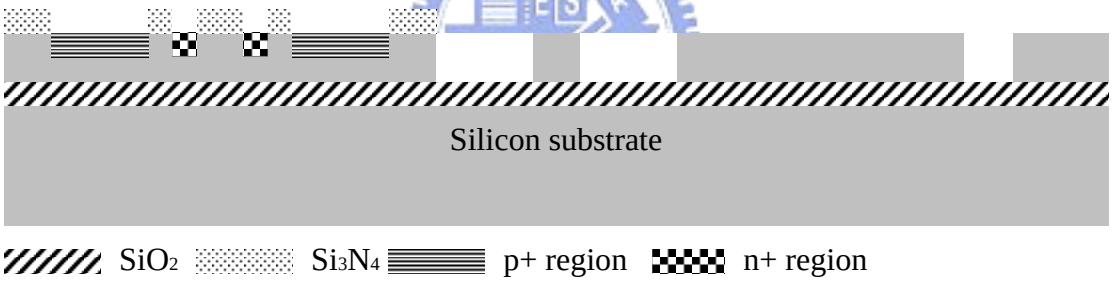
Figure 3-9: Fabrication process of the flipped mirror integrated with photo diodes.



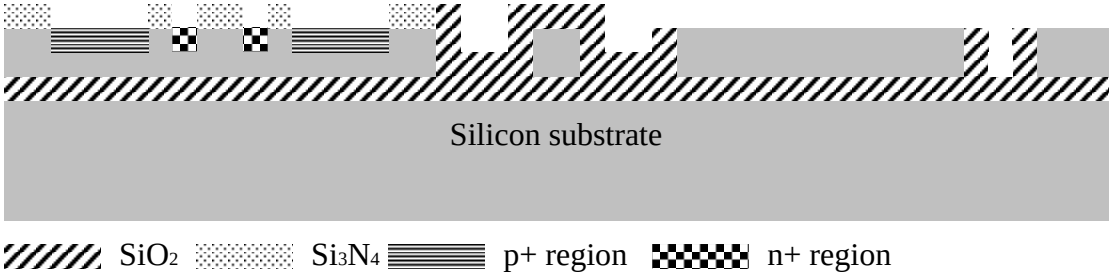
Step 2: Deposit a 0.6um-thick low stress Si_3N_4 layer by LPCVD and lithographically pattern the Si_3N_4 by ploy-RIE.



Step 3: Implant boron to form the p+ region and remove the PR.

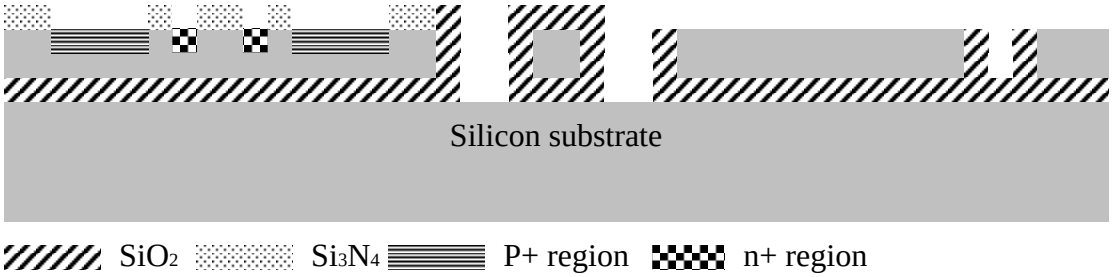


Step 4: Lithographically pattern a 0.6um-thick Si_3N_4 layer by poly-RIE and implant arsenic to form the n+ region and remove the PR.

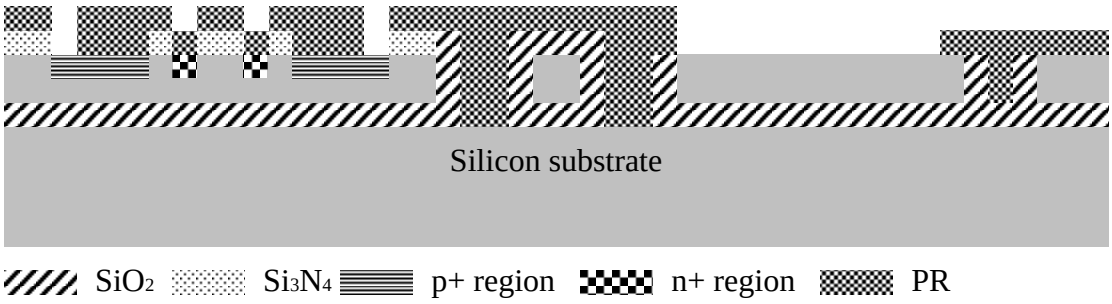


Step 5: Deposit the 2um-thick oxide sacrificial layer by PECVD and lithographically pattern the oxide.

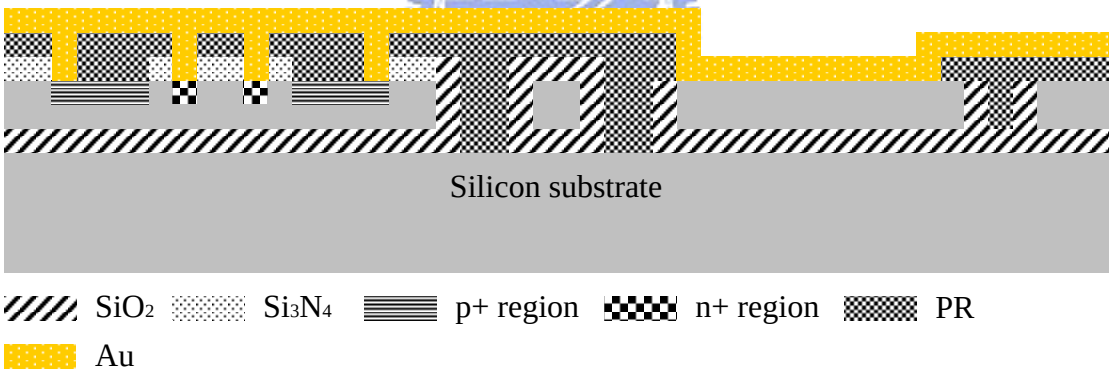
Figure 3-9: Fabrication process of the flipped mirror integrated with photo diodes. (Continued)



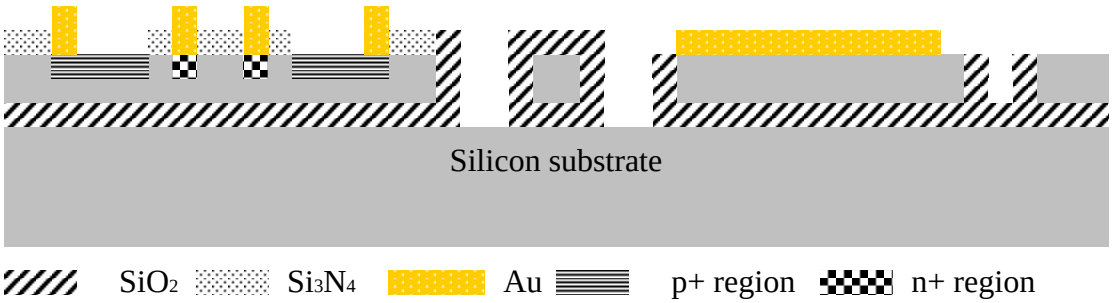
Step 6: Lithographically pattern the 4um-thick oxide.



Step 7: Coat 6um AZ4620 photoresist on top of silicon and pattern it.

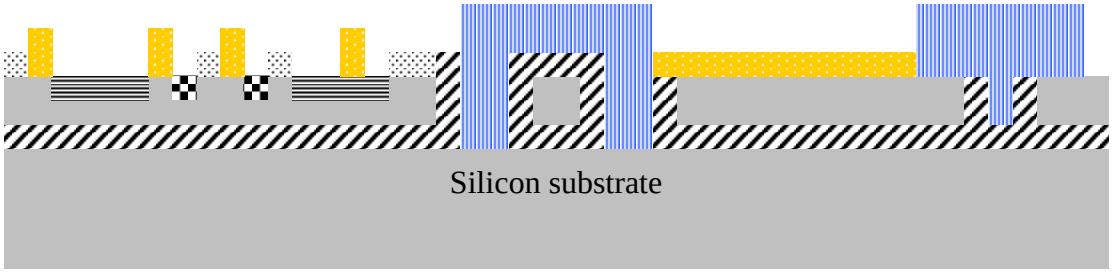


Step 8: Deposit the Au by E-beam evaporation.



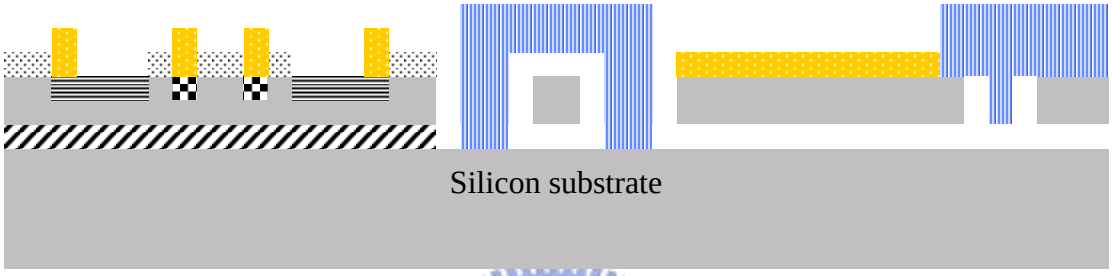
Step 9: Pattern the gold by lift-off.

Figure 3-9: Fabrication process of the flipped mirror integrated with photo diodes. (Continued)



SiO_2 Si_3N_4 Au p+ region n+ region
SU-8

Step 10: Coat SU-8 on top of silicon and lithographically pattern it for the stress beams and anchors.



SiO_2 Si_3N_4 Au p+ region n+ region
SU-8

Step 11: Release the structure by 49% HF vapor.

Figure 3-9: Fabrication process of the flipped mirror integrated with photo diodes. (Continued)

3-2-1 Fabrication Technology of the 135° flipped mirror integrated with diodes

In this section, the detail fabrication process technology of the 135° flipped mirror integrated with diodes is discussed. In the first step, on the RCA cleaned bare SOI wafer, FH6400 is spin coated with the recipe of spread cycle speed = 1000rpm for 10 seconds and spin cycle speed = 4000rpm for 30 seconds. Then ICP RIE is used to etch the top silicon of SOI wafer. Next, on the SOI wafer is deposited a 0.6μm-thick Si_3N_4 layer by LPCVD with the recipe of NH_3 flow rate = 105sccm,

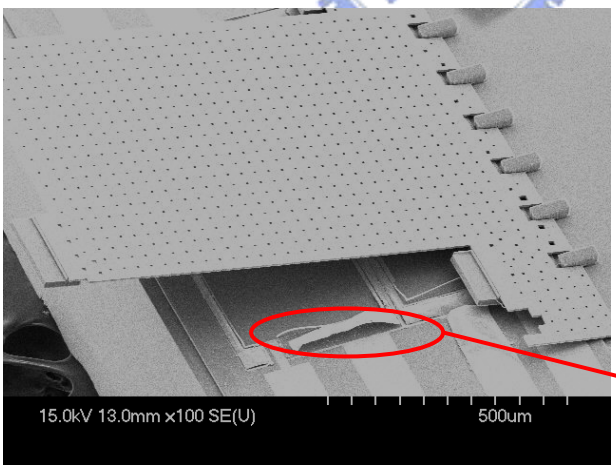
$SiHCl_2$ flow rate = 35sccm, temperature = 800℃, pressure = 140mTorr. It takes 60 minutes to deposit film. Then on the Si_3N_4 layer is spin coated with HMDS and a layer of thick photoresist AZ4620 as the etching mask for the subsequent oxide RIE for implantation region. Then the SOI wafer is sent to implant boron to form the p+ region in the n-type substrate (resistivity: 1-10 ohm-cm, thickness: 5um). The implantation energy was 15 KeV and the concentration of dopant was 5 10^{14} cm^{-2}. The sample was then annealed at 900°C for 10sec to activate the dopants. After removing of AZ4620, the 0.6um-thick Si_3N_4 layer is lithographically patterned by poly-RIE. Then arsenic is implanted to form the n+ region and remove the PR is removed. The implant energy was 60 KeV, the concentration of dopant was 5×10^{15} cm^2. The sample was then annealed at 900°C for 15sec to activate the dopants.

Next, on the top silicon of the SOI wafer is deposited a 2.0μm thickness SiO_2 layer by PECVD. The deposition time of the 2.0μm SiO_2 layer with 90sccm N_2O and 5sccm SiH_4 at 350℃, 400mTorr chamber pressure and 10W RF power is about 29 minutes. Before deposition, clean and dipping in B.O.E. is necessary. Then on the SiO_2 layer is spin coated HMDS and a layer of thick photoresist AZ4620 as the etching mask for the subsequent oxide RIE. The etching rate of RIE of the SiO_2 layer grown by SiH_4 and N_2O is about 1000 Å per 30 seconds with the recipe of SF_6 flow rate = 30sccm, CHF_3 flow rate = 10sccm, pressure = 50mTorr and 100W RF power. It takes 10 minutes to etch the thickness of 2.0μm SiO_2. In this step, wet etching by B.O.E. is another choice. But the undercut is a problem which makes the pattern larger and sidewall not perfect.

After the RIE, the photoresist is cleaned by H_2SO_4: H_2O_2 =3: 1. Then the oxide layer was patterned again for anchors. After the anchors are etched, the thickness of 5μm AZ4620 is spin coated. Then E-beam evaporation was used to deposit the Au (1000Å) and adhesion layer of chromium (300Å), which was patterned

by lift-off. Note that it is necessary to dip the wafer in diluted HF solution before depositing the gold and its adhesion layer, chromium. Otherwise, the gold layer deposited on the native oxide will peel off after releasing the device, as shown in Figure 3-10. Then, the photoresist and unwanted metal (atop the photoresist) are then removed in the acetone bath.

Then the SU8 is spin coated with the recipe of spread cycle speed = 1000rpm for 5 seconds, spin cycle speed = 3000 rpm for 30 seconds, soft bake step1: 65 ℃ for 1 minute and step2: 90 ℃ for 1 minute, exposure time = 5 seconds, post exposure bake time = 2 minutes in 90 ℃, development in SU8 developer = 1 minute, and hard bake = 20 minutes in 200 ℃. Finally, the sacrificial layer (SiO_2) is etched by the vapor of 49% HF solution and rinsed in IPA then the structure is released.



Au layer peeled off

Figure 3-10: Gold layer peels off after releasing.

3-2-2 Problems and Discussions of the novel electro-optical device

In this section, the problems encountered during fabrication and solutions are discussed.

(1) Adhesion of SU-8

After releasing the 135° flipped mirror integrated with diodes, the anchors made of SU-8 may peel off, as shown in Figure 3-11. There may be two reasons for peeling off. Small anchor contact area results in the weak adhesion between SU-8 and silicon. Therefore, the contact area of SU-8 must be enlarged.

Additionally, the native oxide between SU-8 and silicon can be etched by HF during releasing the structures and the SU-8 anchor is then defected from the silicon substrate. This issue can be solved by an HF dipping before SU-8 coating. Alternatively, the structures can be released by HF vapor, instead of HF solution, to avoid the surface tension of water.

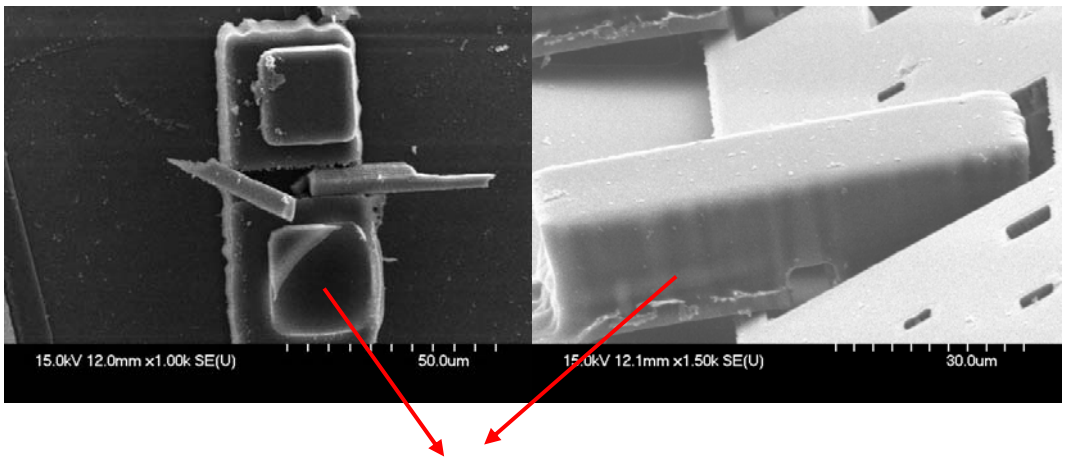


Figure 3-11: The anchor of the device made by SU-8 peeled off.

(2) SU-8 anchor

Figure 3-12 shows an SU-8 anchor before releasing and Figure 3-13 shows an anchor after releasing. In Figure 3-13, the gap of the anchor is large enough for the hinge bar to slide in. So, micromirror may get stuck if the probe controlled and assemble during assembly is not very well.

The solution is to use three probes to lift and assemble the micromirror. One probe can prevent the micromirror from moving forward and the other probes can lift and turn the device. Alternatively, the SU-8 can be anchored on the top silicon of the SOI wafers to avoid gaps. Therefore, the hinge bar will not slide into the gap shown in Figure 3-13.

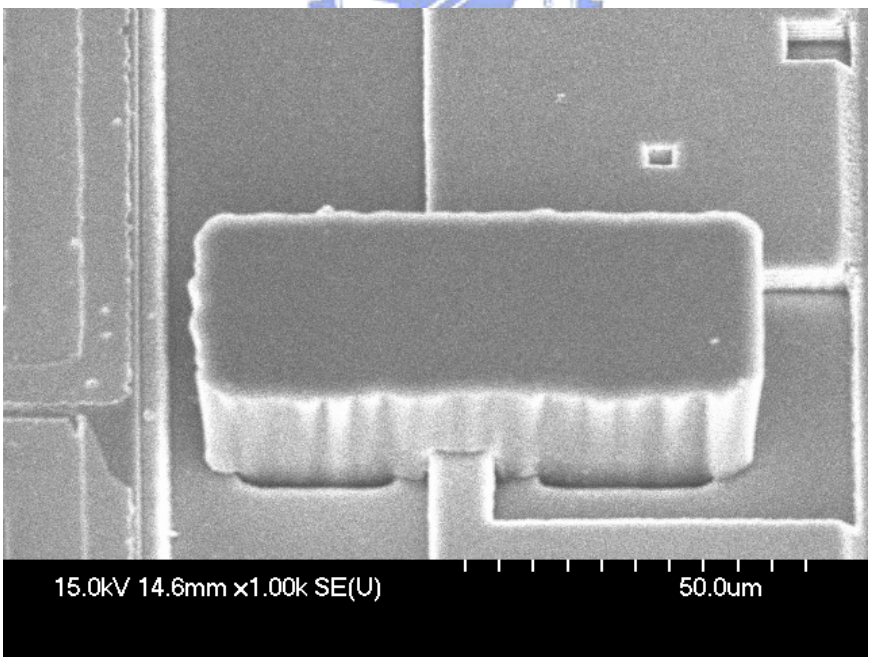


Figure 3-12: SU-8 anchor before releasing.

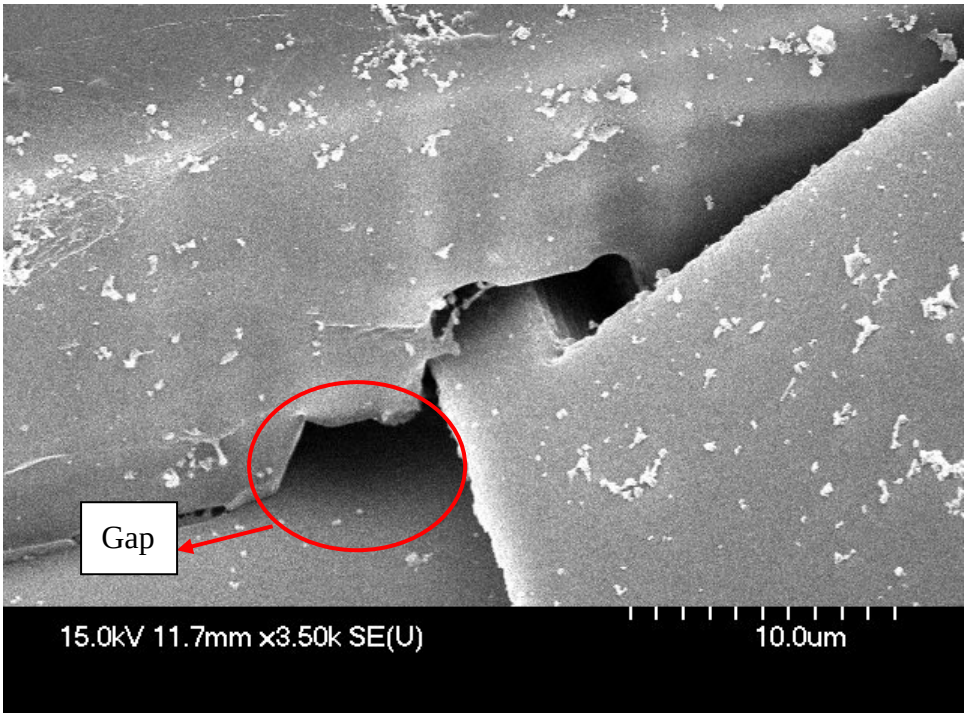


Figure 3-13: SU-8 anchor after releasing.

(3) Latch design

In the original design, the latch has only one anchor, as can be seen in Fig 3-14. This design has two disadvantages. Since the adhesion of SU-8 to silicon was poor, the latch can be easily lost when the anchor is not strong enough. Secondly, the orientation of such a latch during assembly is difficult to control due to the relatively large clearance between the hinge bar and the staple. Therefore, the contact area or the anchor and the number of hinges should be increased to improve the yield and orientation control. Another problem is that the space near the latch was not large enough. Therefore, the probe is hard to slide in to turn the latch.

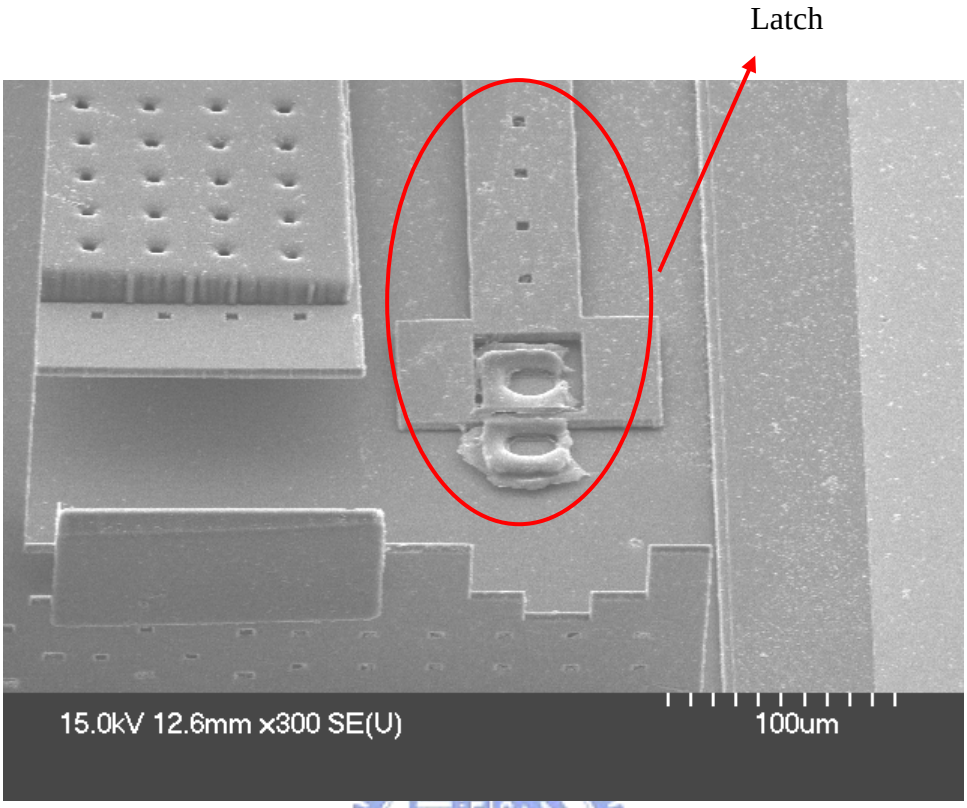


Figure 3-14: The view of single latch.