

國立交通大學
電機與控制工程研究所
碩士論文

應用於無線個人通訊

低功率分時帶通和差調變類比數位換器



A Low Power Time Interleaved Band-pass
Sigma Delta A/D Converter
for Wireless Personal Communication

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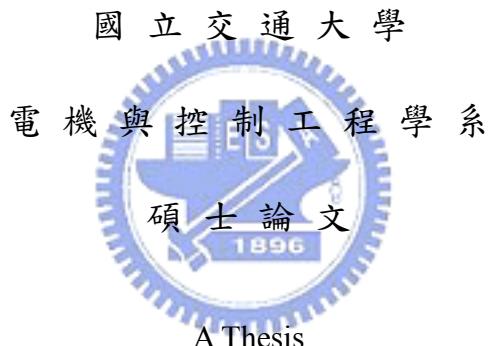
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摘要

帶通類比數位轉換器對電容的誤差以及高速度的處理上，面臨著對誤差極為靈敏，以及功率消耗極高的問題。因此我們採用了分時系統 (Time Interleaved System) 並且搭配上合成雜訊轉移函式 (NTF Synthesis)，利用四個低通的三角積分 ($\Delta \Sigma$) 類比數位轉換器合成一帶通類比數位轉換器。利用四個 ADC 的 channel 分時操作，每個一個 ADC 通道僅須操作在四分之一的帶通類比數位轉換器的工作頻率，如此一來除了可大幅降低 ADC 的功率消耗，延長電池的使用時間。此外，由於每一個 ADC channel 為一個 single loop low-pass sigma delta ADC，此架構之 ADC 對於電容的不匹配，及 OP DC gain 的要求較為寬鬆不靈敏，因此我們亦可在設計電路上得到附加的好處，以及避免掉非理想效應及製程飄移所帶來的問題，以達到所求之解析度。

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National Chiao Tung University



The thesis proposes a low power four path time-interleaved sigma-delta modulator with switched-opamp technique for personal wireless communication applications, such as the GSM system. In this thesis, we design a time interleaved bandpass sigma delta modulator by using four channels with lowpass sigma delta modulator, and implement by TSMC.18 μ m 1P6M CMOS models. And, to avoid gain and offset mismatch produce by each channel, additional reference channel calibrated the errors by off-chip digital calibration technique described in section 3.3. We implement the bandpass A/D converter by low power technique and we overcome the non-ideal effect by off-chip calibration.

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