CHAPER 1
INTRODUCTION

1.1 Motivation

The recent explosion of interest in wireless personal communications systems is motivating the development directed toward reducing power dissipation, increasing signal bandwidth and ensuring flexibility in the system architecture.

For the flexibility, it comes naturally to digital signal processing (DSP), where different functionality may often be implemented in software. The analog circuitry, being more specific to the task, is more difficult to adapt, which favors moving into digital signal representation as soon as possible. In order to achieve this, the signal can be digitized at the first intermediate frequency (IF) instead of the baseband [1]. A bandpass $\Delta\Sigma$ modulator provides a high performance analog-to-digital conversion of a narrow-band high frequency signal, making it a strong candidate for direct IF digitization [1]-[4]. And it's different from traditional Zero-IF architecture by using Digital-IF. It does not only reduce the error from analog circuitry but also reduce the analog design complexity.

However, for the design of the bandpass sigma delta modulator, we need a high performance operational amplifier such as high gain, wide bandwidth, and high slew rate. And we also need high capacitor accuracy to avoid center frequency drifting, notch depth variation. Due to the reasons, the bandpass sigma modulator is not only high power consumption but also sensitive to the capacitor mismatch. To reduce the power consumption and the design complexity, the time-interleaved and noise transfer function synthesis architecture is used. Many ADCs operate in parallel, using different clock phases [5]-[7], as shown in figure 1.1. The analog de-multiplexer selects sequentially each ADC, which therefore operates at low speed. The digital multiplexer

interleaves the digital output of the ADCs, thus producing the overall analog-to-digital conversion result. Each of them operates at a clock frequency fs/N, where fs is the overall sampling frequency and N is the number of channels (or paths) used. To achieve the same performance of bandpass sigma delta modulator, we just need four channel lowpass sigma delta modulators with 1/4 operational sampling frequency. It reduce not only power consumption but also design complexity.

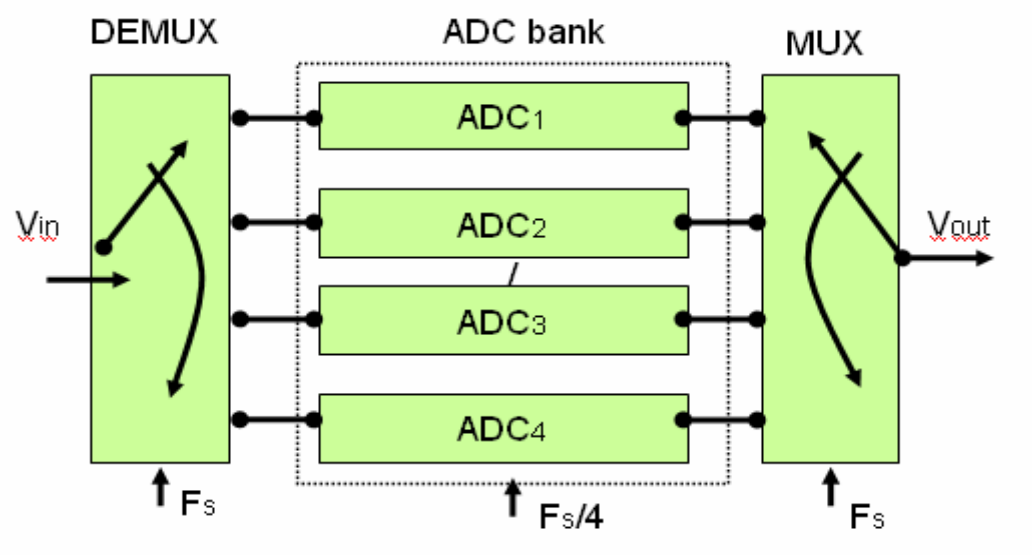


Figure 1.1 Block diagram of a time interleaved ADC

1.2 Thesis Organization

This thesis is divided into five chapters, of which this is the first chapter.

Chapter 2 introduces the background of the sigma delta modulator with quantization noise and lowpass, bandpass modulator. Chapter 3 discusses the system architecture and specifications. It has been introduced the theory of design the bandpass sigma delta A/D converter. Chapter 4 discusses the building blocks of the switched-capacitor (SC) sigma-delta modulator including the clock generator, bias, operational amplifier, comparator, and clock generator. In the end of this chapter is the results and layout of the sigma-delta modulator. Chapter 5 is the conclusions of this work. And take the comparison with other's design..

CHAPER 2

SIGMA – DELTA MODULATOR

Some of the fundamental issues in the design of sigma-delta modulators (SDM) will be reviewed in this chapter. The discussion beings with the basic concept of how the sigma-delta modulators work, the basic lowpass (LP) and bandpass (BP) sigma-delta modulators model are reviewed and related performance issues. The basic concept of the noise shaping sigma-delta modulator is described in Section 2.1. Then the LP and BP SDM are discussed in Section 2.2 and 2.3.

2.1 The Basic Concept of Sigma-Delta A/D Converter

2.1.1 Quantization Error

The use of quantization introduces an error, q(n), which is defined as the difference between the input signal x(n) and the output signal y(n). The error is called quantization noise [9]. In this chapter, these errors are modeled as being equivalent to an additive noise source and find the power of this noise source. In Figure 2.1, the output signal, y(n), is equal to the closest quantized value of x(n). This model is exact if one recognizes that the quantization error is not an independent signal but maybe strongly related the input signal, x(n). This linear model becomes approximate when assumptions are made about the statistical properties of q(n), such as q(n) being an independent white noise signal or like thermal noise.

In order to deal with the more general properties of the quantization noise signal, a stochastic approach is typically used [10]. We can approximate that q(n)=y(n)-x(n) or, correspondingly, Q=Y-X . With the input X having zero mean, and the quantizer assumed to be symmetric. It follows that the quantizer output Y and therefore the quantizztion error Q, will also have zero mean. Thus, for a partial statistical

characterization of the quantizer in terms of the output signal-to-quantization noise ratio, it has to be found only the mean-square value of the quantization error Q.

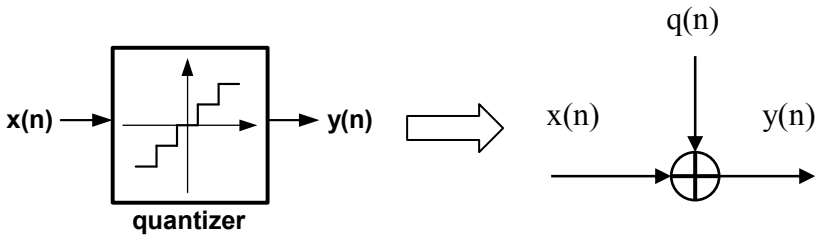


Figure 2.1 Quantizer and its linear model.

Consider that an input x(n) of amplitude in the range ($-V_{ref}$, V_{ref}), assuming a uniform quantizer . The step-size of the quantizer is given by

$$\Delta = V_{LSB} = \frac{2V_{ref}}{L}. \tag{2.1}$$

where L is the total number of representation levels. For a uniform quantizer, the quantizer error E will have its sample values bounded by

$$-\frac{\Delta}{2} \le q(n) < \frac{\Delta}{2}. \tag{2.2}$$

The probability density function for such an error signal, $f_Q(q)$, is a constant value, as shown in Figure 2.2. Thus, the probability density function of the quantization error Q is expressed as follows:

$$f_Q(q) = \begin{cases} \frac{1}{\Delta}, & -\frac{\Delta}{2} \le q(n) < \frac{\Delta}{2}. \\ 0, & otherwise \end{cases} \tag{2.3}$$

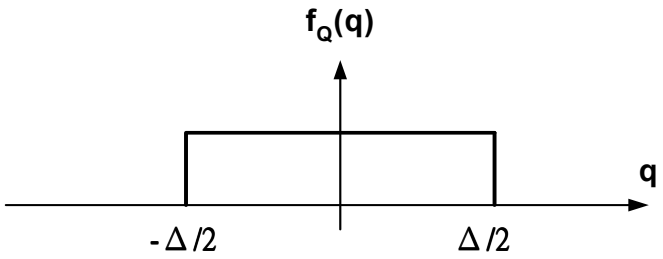


Figure 2.2 The probability density function for the quantization error.

With the mean of the quantization error being zero, its variance is the same as the mean-square value that equals the R.M.S. value of the quantization error:

$$V_{Q,rms}^2 = \sigma_Q^2 = E[Q^2] = \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} q^2 \cdot f_Q(q)dq \,. \tag{2.4}$$

Substituting Equation (2.3) into (2.4), the equation can be written as

$$V_{Q,rms}^2 = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} q^2 dq = \frac{\Delta^2}{12}. \tag{2.5}$$

In general, when the quantization noise signal is uniformly distributed over the interval $\pm V_{LSB}/2$, the r.m.s. quantization noise voltage equals ($\pm V_{LSB}/\sqrt{12}$) and is independent of the sampling frequency, f_S, and input signal. Also, the power spectral density of q(n), $S_q(f)$, is white and all its power is within $\pm f_S/2$ [11]. The power spectral density height is calculated by noting that the total noise power is $\Delta^2/12$ and, with two-side definition of power, equals the area under $S_q(f)$ within $\pm f_S/2$, or mathematically,

$$V_{Q,rms}^2 = \frac{\Delta^2}{12} = \frac{1}{\Delta}\int_{-\frac{S}{2}}^{\frac{S}{2}} S_q(f)df = \int_{-\frac{S}{2}}^{\frac{S}{2}} h_q df = h_q f_S \,. \tag{2.6}$$

Solving this relation gives

$$S_q(f) = h_q = \frac{\Delta^2}{12 f_S}. \tag{2.7}$$

From Equation (2.7), the power spectral density is inversely proportional to the sampling frequency.

Let N denote the number of bits per sample used in the construction of the binary code. It may be written as $L = 2^N$, the V_{LSB} can be expressed

$$V_{LSB} = \Delta = \frac{2V_{ref}}{2^N}. \tag{2.8}$$

So the size of V_{LSB} is halved for each additional bit. Assuming that V_{ref} is constant, it can be found that from Equation (2.5) that the noise power decreases by 6-dB for each additional bit in the A/D converter (i.e., flash ADC or quantizer). Thus, given an input signal waveform, a formula can be derived giving the best possible signal-to-noise ratio (SNR) for a given number of bits in an ideal A/D converter.

For example, a commom SNR formula is to assume that V_{in} is a sinusoidal waveform between $-V_{ref}$ and V_{ref}. Thus, the AC r.m.s. value of the sinusoidal wave is

$$V_{in,rms} = \frac{V_{ref}}{\sqrt{2}}. \tag{2.9}$$

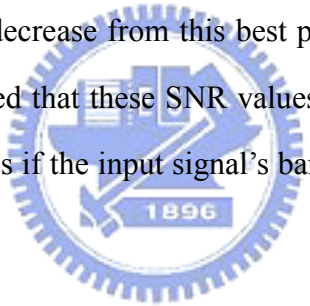
Then the SNR is given by

$$SNR = 20\log_{10}\left(\frac{V_{in,rms}}{V_{Q,rms}}\right) = 20\log_{10}\left(\frac{\frac{V_{ref}}{\sqrt{2}}}{\frac{V_{LSB}}{\sqrt{12}}}\right) = 20\log_{10}\left(\sqrt{\frac{3}{2}}2^{N}\right) \tag{2.10}$$

SNR can be expressed in dB:

$$\text{SNR}=6.02\text{N}+1.76 \text{ dB}. \tag{2.11}$$

Note that Equation (2.10) gives the best possible SNR for an N-bit A/D converter. However, the idealized SNR decrease from this best possible value for reduced input signal levels. It should be noted that these SNR values could be improve through the use of oversampling techniques if the input signal's bandwidth is much lower than the Nyquist rate.



2.1.2 Oversampling Technique

Since oversampling can make it possible to implement sharper cutoff anti-aliasing filtering by incorporating digital filtering and decimation. Oversampling, subsequent discrete-time filtering and downsampling also permit an increase step size Δ of the quantizer or, equivalently a reduction in the number of bits required in the quantizer [12].

Oversampling occurs when the signals of interest are bandlimited to f_0 yet the sample rate is at f_S, where $f_S > 2f_0$. $2f_0$ is the Nyquist rate or, equivalently, the minimum sampling rate for signal bandlimited to f_0. It can be defined the oversampling ratio, $OSR = f_S / 2f_0$.

To explore the relation between oversampling and quantization step size, the system in Figure 2.3 is considered. To analyze the effect of oversampling in this

system, assume initially that x(n) is already bandlimited to f_0. Using the additive noise model shown in Figure 2.1. Figure 2.3 can be instead of the Figure 2.4(a). The ideal low-pass filter in Figure 2.3 can be implemented by decimation filter with unity gain and cutoff frequency $f_c = f_0$. It can be defined that the transfer function of the low-pass filter is L(f) as shown in Figure 2.4(b). Since the system of Figure 2.4 is linear and the quantization noise is independent of the signal, the two sources can be treat separately in computing the respective powers of the signal and noise components at the output. Our goal is to determine the signal-to-quantization noise ratio as a function of the quantizer output bits, N, and the oversampling ratio, OSR.

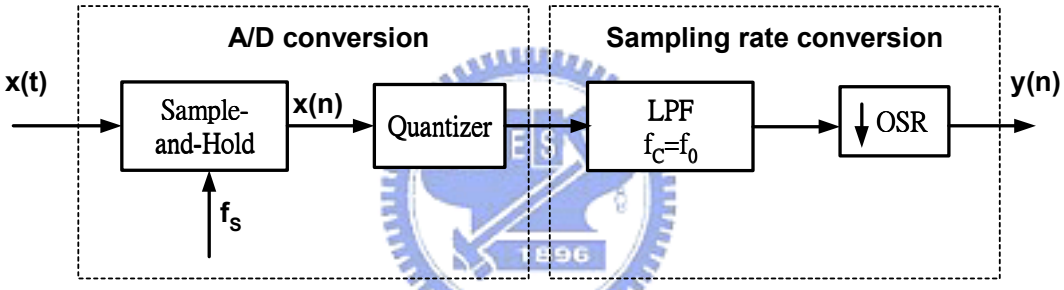
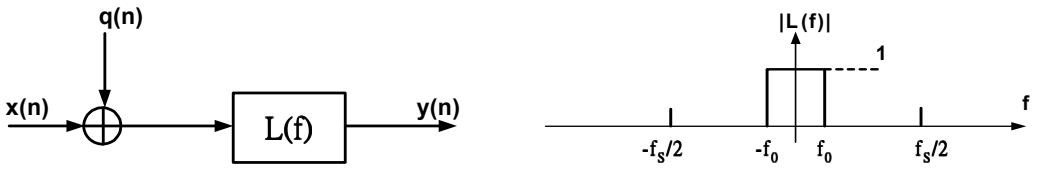


Figure 2.3 Oversampled ADC with simple quantization and downsampling.



(a) (b)

Figure 2.4 (a) A simplified oversampled A/S conversion and (b) the magnitude frequency response of the low-pass filter.

After calculate above function, we can get the signal power Ps and quantization noise power P_Q :

$$P_S = \frac{V_{ref}^2}{2} = \frac{1}{2} \cdot \left(\frac{\Delta L}{2} \right)^2 = \frac{\Delta^2 L^2}{8} = \frac{\Delta^2 2^{2N}}{8}. \tag{2.12}$$

$$P_Q = \int_{-\frac{S}{2}}^{\frac{S}{2}} S_q(f) \cdot |L(f)|^2 df = \int_{-f_0}^{f_0} S_q(f) \cdot 1 \cdot df \,. \tag{2.13}$$

$$= \frac{\Delta^2}{12} \cdot \frac{2f_0}{f_S} = \frac{1}{12 \cdot OSR} \cdot \left(\frac{2V_{ref}}{2^N} \right)^2$$

Equation (2.13) shows quantization noise can be attenuated by increasing the oversampling ratio (OSR). Since the signal power is independent of OSR, increasing OSR will increase the signal-to-quantization noise ratio. Alternatively, for a fixed quantization noise power, the required value for N is

$$N = -\frac{1}{2}\log_2 OSR - \frac{1}{2}\log_2 P_Q + \log_2(2v_{ref}) \,. \tag{2.14}$$

From Equation (2.13), for every doubling of the oversampling ratio OSR, 1/2 bits need to be less to achieve a given signal-to-quaiitization-noise ratio.

To explain the advantage of oversampling technique more clearly, it shows the quantization-noise power spectral density of the Nyquist rate and oversampling conversion in Figure 2.5. Because the total quantization noise power is only dependent on the step size of the quantizer, the shaped rectangle and unshaped rectangle will have the same area. For Nyquist rate sampling where the sampling frequency $f_S' = 2f_0$, so all the quantization noise power occurs in the signal bandwidth. However, the sampling frequency in the oversampling case is much larger than $2f_0$, so its power spectral density is spread over larger frequency range (i.e., - f_S /2 ~ f_S /2). There is only a small fraction of the noise power falls in the signal band, and the out-of-band noise can be removed by a low-pass digital Filter that mentioned above.

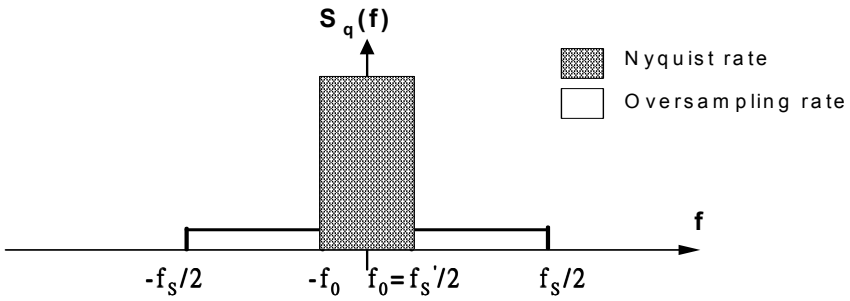


Figure 2.5 The PSD of quantization noise in Nyquist and oversampling techniques.

It can be also calculated that the maximum SNR (in dB) to be the ratio of the maximum sinusoidal power to the quantization noise power at the output of the system in Figure 2.4(a).

$$SNR_{\max} = 10\log_{10}\left(\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2}{12\cdot OSR}}\right) = 10\log_{10}\left(\frac{3\cdot 2^{2N}\cdot OSR}{2}\right)$$

$$= 6.02N + 1.76 + 10\log_{10}(OSR) \quad \text{dB} \qquad (2.15)$$

The first term is the SNR due to the N-bit quantizer while the OSR term is the SNR enhancement obtained from oversampling technique. Here it can be seen that straight oversampling gives a SNR improvement of 3dB/octave. The reason for this SNR improvement through the use of oversampling is that when quantized samples are averaged together, the signal portion adds linearly, whereas the noise portion adds as the square root of the sum of the squares (i.e., r.m.s.).

2.1.3 Noise-Shaped Sigma-Delta Modulator

In the previous section, the oversampling and decimation can improve the signal-to-quantization-noise ratio. It implies that it can be, in principle, used very

crude quantization in our initial sampling of the signal, and if the oversampling ratio is high enough, an accurate representation of the original samples can still be obtained by doing digital computation on the noisy samples. For example, to reduce the number of bits from 13 to 10 would require OSR = $4^{(13-10)}$ = 64. This seems to be a rather high cost. However, a much more dramatic improvement in SNR will be seen when the input signal is oversampled as compared to oversampling the input signal with **noise spectrum shaping** by feedback. Broadly speaking, oversampling A/D converters exchange resolution in time for that in amplitude by combining sampling at well above the Nyquist rate with coarse quantization embedded within a feedback loop in order to suppress the amount of quantization noise appearing in the signal band. The quantizer output is then digitally filtered to generate a lower data-rate, higher resolution encoding of the signal. This type of A/D converters is called **Sigma-Delta Oversampling Analog-to-Digital Converter (ΣΔ ADC)** [13].

The system architecture of a ΣΔ oversampling A/D converter is shown in Figure 2.6. The first stage is a continuous-time anti-aliasing filter and is required to bandlimit the input signal to frequencies less than one-half the oversampling frequency, f_S. When the oversampling ratio is large, the anti-aliasing filter can often be quite simple, such as a simple RC low-pass filter. Following the anti-aliasing filter, the continuous-time signal, $X_C(t)$. is sampled by a sampled-and-hold. This signal is then processed by the ΣΔ modulator, which converts the analog signal into a noise shaped low-resolution digital signal. The third block in the system is a decimator. It converts the oversampled low-resolution digital signal into a high-resolution digital signal at a lower sampling rate usually equal to twice the frequency of the desired bandwidth of the input signal. As discussed before, the decimation filter can be conceptually thought of as a low-pass filter followed by a down sampler, although in many systems the decimation is performed in a number of stages. It should be mentioned that in many realizations where the ΣΔ modulator is realized using switched-capacitor circuitry, a separate sample-and-hold is not required, as continuous-time signal is

inherently sampled by the switches and input capacitors of the SC ΣΔ modulator.

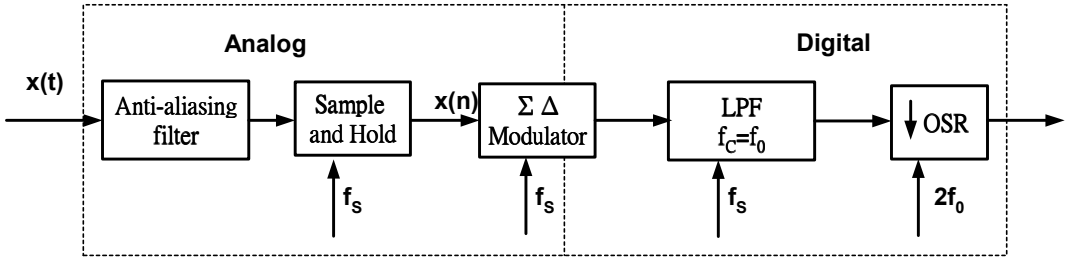


Figure 2.6 Block diagram of an oversampling ΣΔ A/D converter.

A general noise-shaped sigma-delta modulator and its linear model are shown in Figure 2.7. Figure 2.7(a) shows a block diagram of how the system is implemented with integrator circuits. The integrator is a switch-capacitor discrete-time integrator. The A/D converter can be implemented in many ways. In order to simplify the explanation, assuming the A/D converter is a simple 1-bit quantizer or comparator. The D/A converter takes the digital output and converts it back to an analog signal that is subtracted from the input signal at the input to the integrator. This system can be represented by the discrete-time equivalent linear model shown in Figure 2.7(b). The switch-capacitor integrator is represented by its transfer function H(z), and the feedback path represents the 1-bit D/A converter. In fact, multibit quantizer and DAC are gaining in popularity.

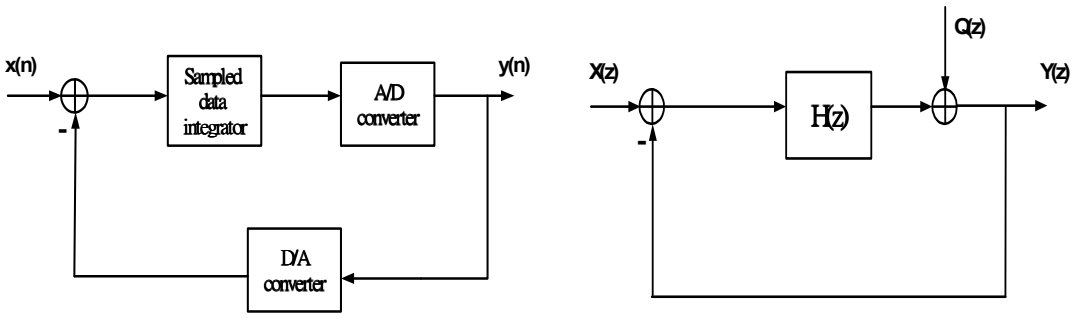


Figure 2.7 (a) a general ΣΔ modulator (b) linear model of the ΣΔ odulator.

Treating the linear model shown in Figure 2.7(b) as having two independent inputs, input signal X(z) and quantization noise Q(z). it can be derived a signal transfer function, $S_{TF}(Z)$. by setting Q(z)=0.

$$S_{TF}(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1+H(z)}. \tag{2.16}$$

It can also be derived a noise transfer function, $N_{TF}(z)$, by setting X(z)=0

$$N_{TF}(z) = \frac{Y(z)}{Q(z)} = \frac{1}{1+H(z)}. \tag{2.17}$$

From Equation (2.17), the zero of the noise transfer function, $N_{TF}(Z)$, will be equal to the poles of H(z). In other words, when H(z) goes to infinity, from Equation (2.17), the $N_{TF}(Z)$ will go to zero. The output signal as the combination of the input signal and the noise signal can also be written with each being filtered by the corresponding transfer function. In the discrete frequency domain, it shows

$$\begin{aligned} Y(z) &= S_{TF}(z)\cdot X(z) + N_{TF}(z)\cdot Q(z) \\ &= \frac{H(z)}{1+H(z)}\cdot X(z) + \frac{1}{1+H(z)}\cdot Q(z). \end{aligned} \tag{2.18}$$

In order to shape the quantization noise in a useful manner, H(z) is properly chosen such that its magnitude is large from DC to f_0 (i.e., over the frequency band of interest). With such a choice, the signal transfer function, $S_{TF}(Z)$, will approximate unity over the frequency band of interest very similarly to an op-amp in unity-gain feedback configuration. Furthermore, the noise transfer function, $N_{TF}(z)$. will approximate zero over the same band. In other words, $N_{TF}(z)$ will have a high-pass response. Thus the quantization noise is reduced over the frequency band of interest (i.e., baseband) while the signal itself is unaffected.

2.2 The Lowpass Sigma Delta Modulator

2.2.1 First Order Lowpass Sigma Delta Modulator

In Figure 2.8, there is a simple first-order 1-bit ΣΔ modulator. It comprises a discrete-time integrator and a 1-bit quantizer that maps its input to both an analog and

a digital output [9][14]. First, it will be discussed why the First-order ΣΔ modulator is combined by these components. To realize first-order noise shaping, the noise transfer function, $N_{TF}(z)$, should a zero at DC, equivalently H(z) should laid a pole at DC (i.e., have a pole at z=1). So the quantization noise is high-pass Filtered at low frequency, and it can be obtained first-order noise shaping by letting H(z) be a discrete-time integrator which has a pole at z=1.

$$H(z) = \frac{1}{z-1} = \frac{z^{-1}}{1-z^{-1}}. \tag{2.19}$$

Then, the signal transfer ftinction, $S_{TF}(Z)$ and noise transfer function, $N_{TF}(z)$, are

$$S_{TF}(z) = \frac{H(z)}{1+H(z)} = \frac{\frac{1}{z-1}}{1+\frac{1}{z-1}} = z^{-1} \quad , \quad N_{TF}(z) = \frac{1}{1+H(z)} = \frac{1}{1+\frac{1}{z-1}} = 1-z^{-1} \tag{2.20}$$

So the total transfer function of this system is

$$Y(z) = X(z)\cdot z^{-1} + Q(z)\cdot(1-z^{-1}). \tag{2.22}$$

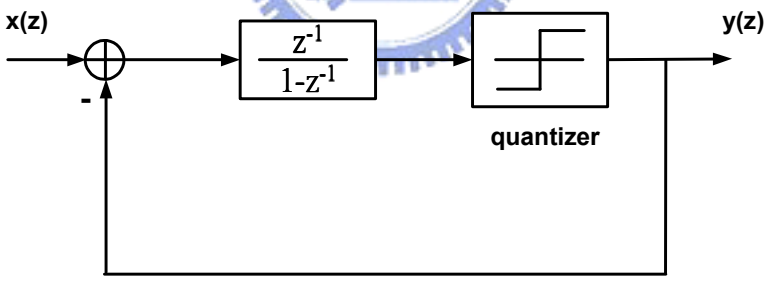


Figure 2.8 A first order oversampled ΣΔ modulator.

From Equation (2.20), the $S_{TF}(z)$ is simply a delay (i.e., z^{-1}). In other words, the output signal component only delays the input signal $1/f_S$ seconds. But the noise transfer function is a high-pass filter (i.e. a discrete-tune differentiator). Recalling

$$z = e^{j\omega} = e^{j2\pi f / f_S}. \tag{2.23}$$

By substituting Equation (2.23) into (2.21) . We can get tthe noise transfer function as

$$\Rightarrow N_{TF}(f) = 1 - e^{-j2\pi f / f_S} = \sin\left(\frac{\pi f}{f_S}\right) \cdot 2j \cdot e^{-j\pi f / f_S} \qquad (2.24)$$

The quantization noise power at the decimation filter (i.e., a low-pass filter) output is given by ,

$$P_Q \approx \frac{\Delta^2}{12 f_S} \int_{-f_0}^{f_0} \left[2 \cdot \left(\frac{\pi f}{f_S} \right) \right]^2 df = \left(\frac{\Delta^2}{12} \right) \left(\frac{\pi^2}{3} \right) \left(\frac{2 f_0}{f_S} \right)^3 = \frac{\Delta^2 \pi^2}{36} \left(\frac{1}{OSR} \right)^3 . \qquad (2.25)$$

Form Equation (2.25), again, a trade-off between the oversampling ratio OSR and the quantization step size Δ. Therefore, to achieve a given quantization-noise power $P_{Q,}$ it must have

$$N = -\frac{3}{2}\log_2 OSR + \log_2\left(\frac{\pi}{6}\right) - \frac{1}{2}\log_2 P_Q + \log_2(2V_{ref}) . \qquad (2.26)$$

Comparing Equation (2.26) with (2.24), whereas the direct quantization a doubling of the oversampling ratio OSR gained 0.5 bits in quantization, the use of noise shaping results in a gain 1.5 bits [5].

Assuming the input signal is a sinusoidal wave, its maximum peak value is $V_{ref.}$ So we can get the maximum SNR for a first-order ΣΔ modulator:

$$SNR_{\max} = 10\log_{10}\left(\frac{P_S}{P_Q}\right) = 10\log_{10}\left[\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3}\right] = 10\log_{10}\left(\frac{9 \cdot 2^{2N} \cdot OSR^3}{2\pi^2}\right)$$

$$= 10\log_{10}\left(\frac{3}{2}2^{2N}\right) + 10\log_{10}\left(\frac{3}{\pi^2}\right) + 10\log_{10}(OSR^3) \qquad (2.27)$$

$$= 6.02N + 1.76 - 5.17 + 30\log_{10}(OSR) \qquad \text{dB.}$$

Figure 2.9 shows the power spectral density of the first-order ΣΔ modulator. It is clear to observe that the total noise power is increased from $\Delta^2/12$ at the output of the direct oversampled case to $\Delta^2/6$ at the output of the noise-shaping system. However, the quantization noise has been shaped in such a way that more of the noise power is outside the signal band, f_0, than in the direct oversampled case, where the noise spectrum is flat.

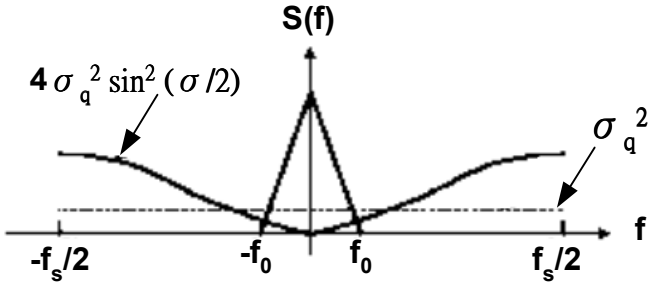


Figure 2.9 The power spectral density of a first order oversampled ΣΔ modulator.

2.2.2 Second Order Lowpass Sigma Delta Modulator

The second-order ΣΔ modulator shown in Figure 2.10 realizes second-order quantization noise shaping [12]. Its fundamental theory is the same as a first-order ΣΔ modulator. However, to realize the second-order noise shaping, the noise transfer function, $N_{TF}(Z)$, must be a second-order highpass function. For the modulator shown in Figure 2.10, the total transfer function is given by

$$Y(z) = X(z)\cdot S_{TF}(z) + Q(z)\cdot N_{TF}(z)$$

$$= X(z)\cdot z^{-2} + Q(z)\cdot (1-z^{-1})^2 . \qquad (2.28)$$

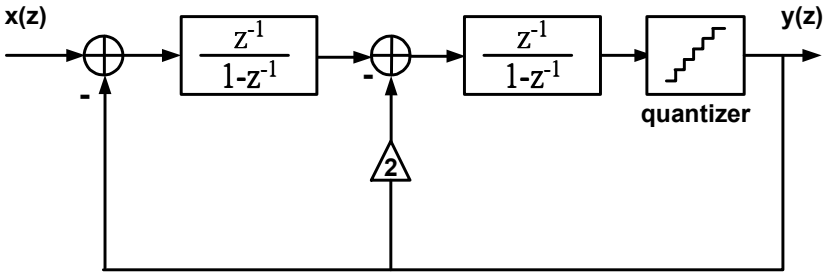


Figure 2.10 A second order oversampled ΣΔ modulator.

Like the first order sigma delta modulator, we can calculate the SNR of the second order sigma delta modulator. The peak SNR is:

$$SNR_{\max} = 6.02N + 1.76 - 12.9 + 50\log_{10}(OSR) \quad \text{dB.} \qquad (2.29)$$

From Equation (2.29), doubling the OSR gives an SNR improvement for

a second-order modulator of 15 dB,or equivalently, a gain of 2.5 bits.

We can see the total noise power at the output of second-order noise-shaping system is greater than for the first-order case, more of the quantization noise of second-order case lies outside the signal band. Figure 2.4 shows the general shape of zero-, first-, and second-order noise-shaping curves. The in-band noise power decreases as noise-shaping order increases. However, the total and out-of-band quantization noise powers increase for the higher-order modulators. In the following section, these higher-order modulators will be discussed.

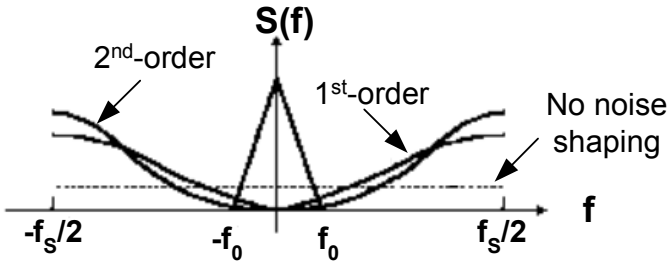


Figure 2.11 The power spectral density of zero-, first-, second-order oversampled ΣΔ modulator.

2.2.3 High Order Lowpass Sigma Delta Modulator

In a ΣΔ modulator, feedback loop and integrator shape the spectrum of the quantization noise, placing most of its energy outside the signal band. The orders of noise transfer would determine how much noise placed outside the signal band. In general, the characteristics of the filter included in the forward path and the feedback types determine the noise transfer function and the shape of the spectrum. In this section, two types of ΣΔ modulators that have higher-order noise shaping than second-order ΣΔ modulators will be introduced.

A L_{th}-order ΣΔ modulator should have a noise transfer function, $N_{TF}(z)$, as

$$N_{TF}(z) = (1 - z^{-1})^{L}. \tag{2.30}$$

it ca be derive that quantization noise power of a L_{th}-order ΣΔ modulator with N bits quantizer in the signal bandwidth.

$$P_Q = \int_{-f_0}^{f_0} S_q(f) \cdot |N_{TF}(f)|^2 \cdot |L(f)|^2 \cdot df = \frac{\Delta^2}{12 f_S} \int_{-f_0}^{f_0} \left[2\sin\left(\frac{\pi f}{f_S} \right) \right]^{2L} df$$

$$\Rightarrow P_Q \approx \frac{\Delta^2}{12 f_S} \int_{-f_0}^{f_0} \left[2 \cdot \left(\frac{\pi f}{f_S} \right) \right]^{2L} df = \left(\frac{\Delta^2}{12} \right) \left(\frac{\pi^{2L}}{2L+1} \right) \left(\frac{2 f_0}{f_S} \right)^{2L+1} \tag{2.31}$$

$$= \frac{\Delta^2 \pi^{2L}}{12(2L+1)} \left(\frac{1}{OSR} \right)^{2L+1}$$

Then the maximum SNR is

$$SNR_{\max} = 10\log_{10}\left(\frac{P_S}{P_Q} \right) = 10\log_{10}\left[\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2 \pi^{2L}}{12(2L+1)} \left(\frac{1}{OSR} \right)^{2L+1}} \right] = 10\log_{10}\left(\frac{3 \cdot 2^{2N} \cdot (2L+1) \cdot OSR^{2L+1}}{2\pi^{2L}} \right)$$

$$= 10\log_{10}\left(\frac{3}{2} 2^{2N} \right) + 10\log_{10}\left(\frac{2L+1}{\pi^{2L}} \right) + 10\log_{10}(OSR^{2L+1}) \tag{2.32}$$

$$= 6.02N + 1.76 + 10\log_{10}\left(\frac{2L+1}{\pi^{2L}} \right) + (20L+10)\log_{10}(OSR) \quad \text{dB.}$$

From Equation (2.32), doubling the OSR improves the SNR for a L_{th}-order noise-shaping ΣΔ modulator by (6L+3) dB, or equivalently, (L+0.5) bits For a given oversampling ratio, a high-order modulator is capable of much greater SNR than a simple second-order loop. This improvement is a function of the oversampling ratio; high oversampling ratios benefit the most from high-order loop filters, whereas low oversampling ratios (<16) do not show as much improvement when high-order loop filters are used. The peak SNR v.s. OSR with different order sigma delta modulator is shown in Figure 2.12.

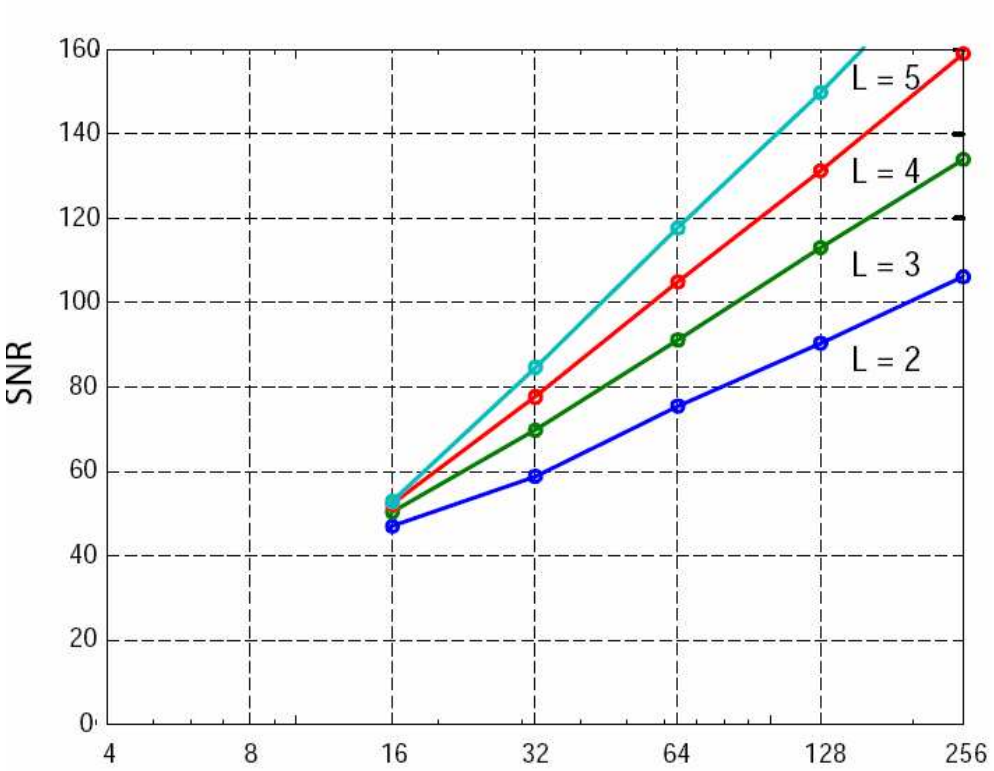


Figure 2.12 The SNR v.s. OSR with different order sigma delta modulator

The main difficulty with higher-order modulator is stability. Linear analysis of such modulators is not reliable, because the quantizer is nonlinear in nature. The gain or the quantizer must be high to guarantee the stability of the high order loop. This will be achieved by keeping the input of the quantizer small since the output amplitude of the quantizer is fixed. Thus the input of the loop filter may be restricted and /or some limiter may be added at the output of the loop filter to reduce the signal swing.

2.3 The Bandpass Sigma-Delta Modulator

A bandpass sigma-delta modulator can be constructed by connecting a filter and quantizer in a loop, as shown in Fig. 2.13. The resonator may be implemented as a discrete-time filter using, such as switched-capacitor (SC)[15].

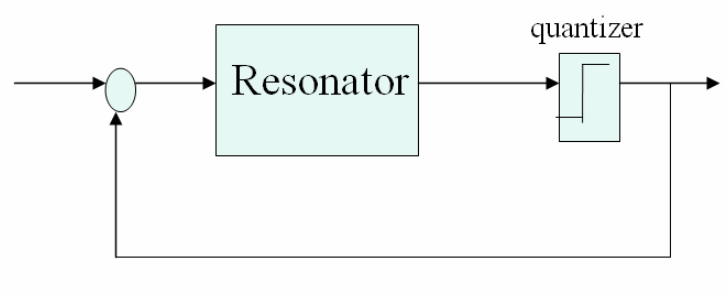


Figure 2.13 A Bandpass Sigma-Delta Modulator

2.3.1 Transformation of the LP and BP Sigma Delta Modulator

Comparing the lowpass and bandpass sigma delta modulators in Figure 2.14, we can easily understand the difference of the two modulators. The integrator of the original lowpass sigma delta modulator is replaced by a bandpass filter. For the noise transfer function, the lowpass sigma delta modulator is a highpass frequency response and it can remove the quantization noise to the high frequency range outside the signal band. In a similar way, bandpass sigma delta modulator is a band-stop frequency response, and the quantization noise can be removed. Figure 2.15 is shown the STF and NTF curve of the bandpass modulator at 3/4 sampling frequency.

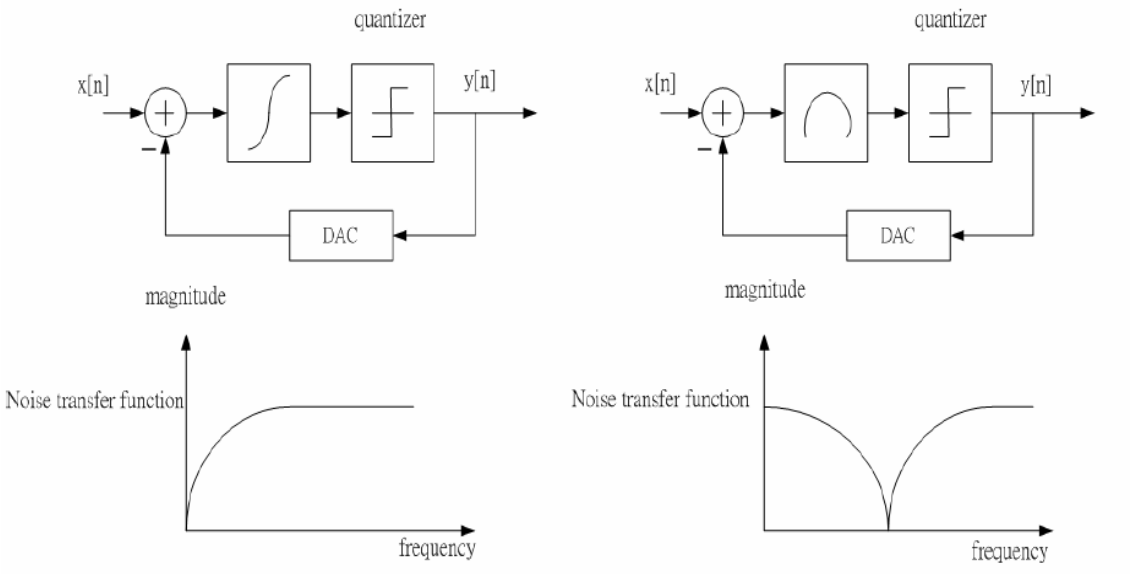


Figure 2.14 (a) Lowpss Sigma Delta Modulator (b)Bandpass Sigma Delta Modulator

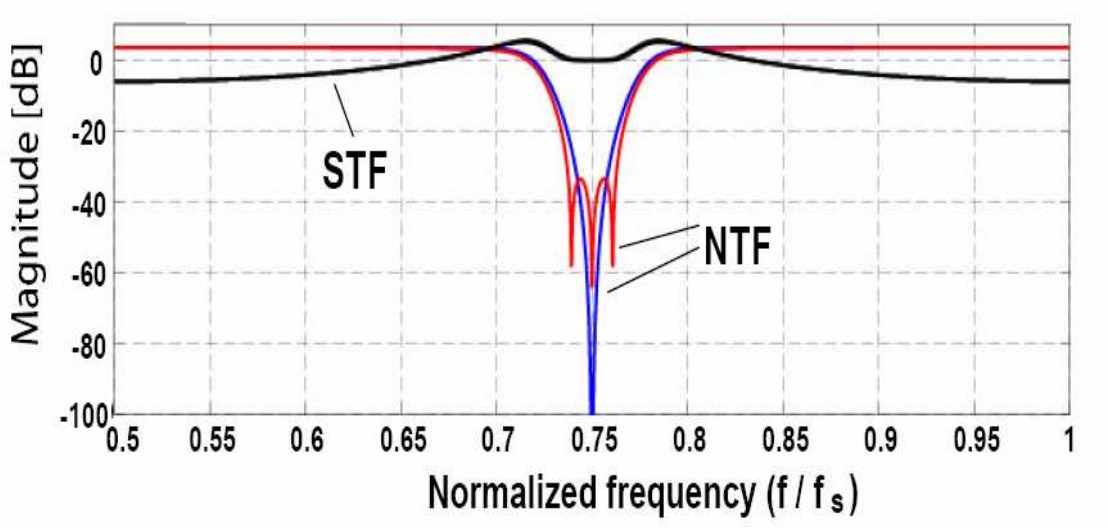


Figure 2.15 STF & NTF of The Bandpass Modulator at 3/4 Sampling Frequency

A simple way of designing bandpass sigma delta modulators is to perform a lowpass to bandpass transformation. One such transformation in the discrete-time domain is achieved by the following change of variable [16]:

$$Z^{-1} \rightarrow -Z^{-2} \tag{2.33}$$

This transformation maps the zeros of the lowpass modulator from DC to ± Fs/4, suppressing the noise in the bandpass modulator around Fs/4 and 3Fs/4 frequency. The zeros of the noise transfer function for this type of second order modulator are shown in Figure 2.15, together with a similar lowpass case.

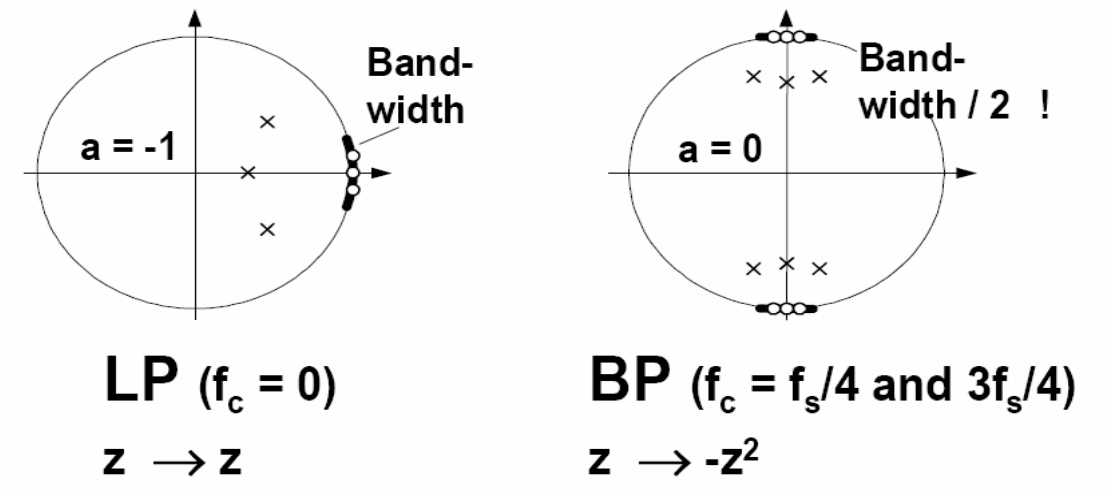


Figure 2.16 NTF Poles and Zeros for Lowpass and Bandpass Modulator

2.3.2 Second Order Bandpass Sigma Delta Modulator

A second-order bandpass sigma-delta modulator is shown in Figure. 2.17. We can derive the noise transfer function, NTF(z), and signal transfer function, STF(z).

$$NTF(Z) = (1 + Z^{-2}) \qquad STF(Z) = -Z^{-2} \tag{2.34}$$

The modulator Y(Z) is express by

$$Y(Z) = -Z^{-2}X(Z) + (1 + Z^{-2})E(Z) \tag{2.35}$$

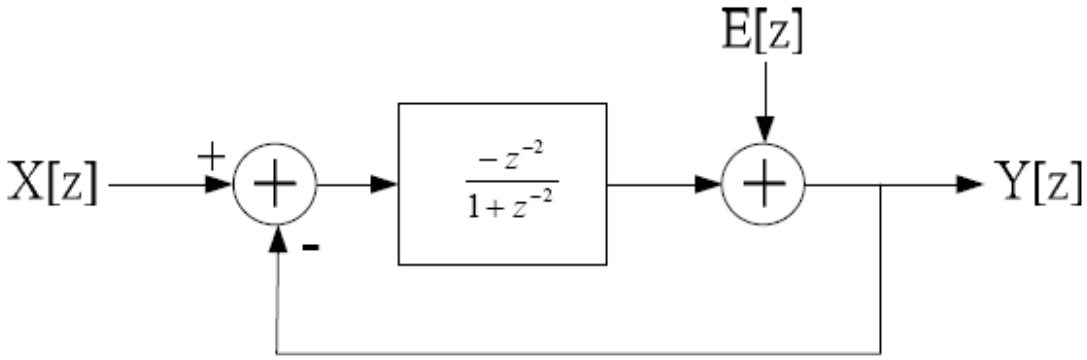


Figure 2.17 The Second Order Bandpass Sigma Delta Modulator

Note that this second-order example has poles at $\pm j$, and therefore the noise transfer function, NTF(Z), has only one zero at +j and another zero at –j. For this reason, the SNR increase of a second-order bandpass converter equals that of a first-order lowpass converter that also has only one zero at dc. The NTF(Z)'s frequency response is shown in Fig. 2.18.

The in-band quantization noise after the noise-shaping will be given by:

$$\sigma_{ey}{}^2 = \int_{f_c-\frac{f_B}{2}}^{f_c+\frac{f_B}{2}} E^2(f)\,|1+Z^{-2}|\,df = \int_{f_c-\frac{f_B}{2}}^{f_c+\frac{f_B}{2}} \frac{\sigma_e^2}{\frac{f_s}{2}}\,|1+Z^{-2}|\,df$$

$$\approx \frac{\Delta^2}{12}\frac{\pi}{3}\left(\frac{2f_B}{f_s}\right)^3 \tag{2.36}$$

Because the in-band noise is the same as the first-order lowpass sigma-delta modulator, each doubling of the sampling frequency decreases the in-band noise by 9dB, but increases the resolution by 1.5 bits [17].

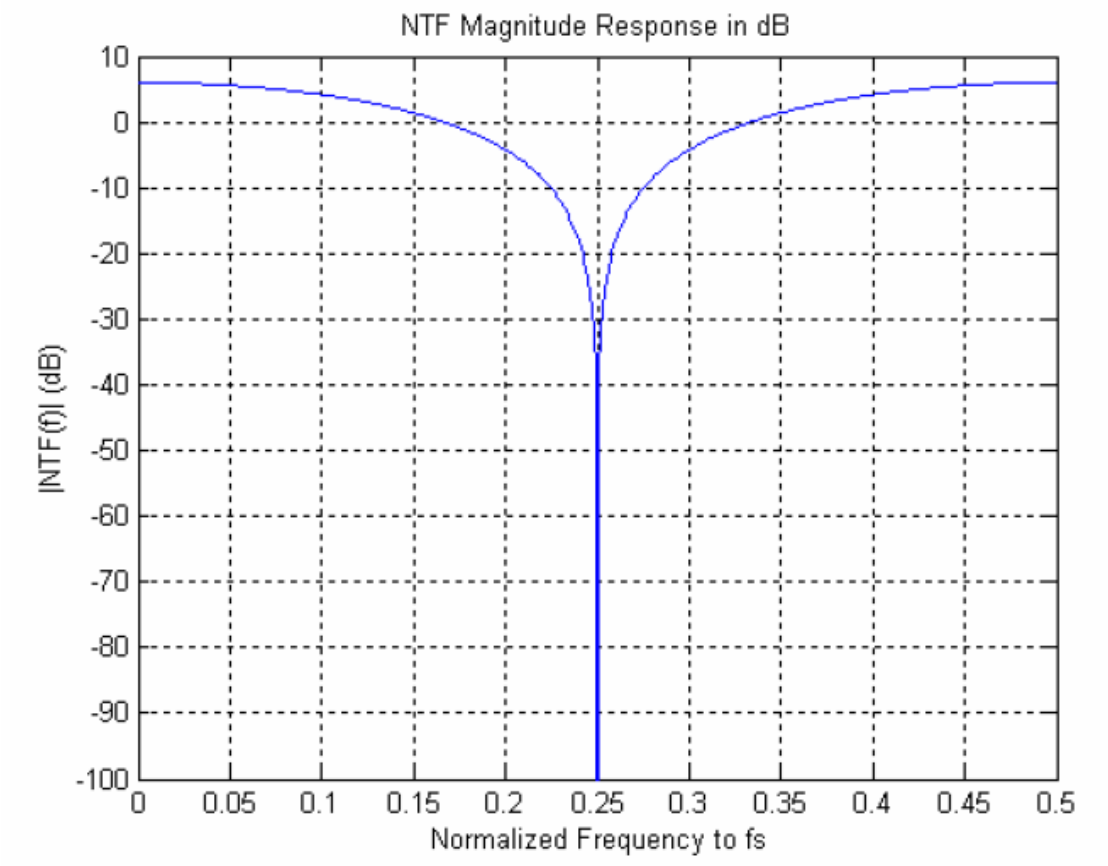


Figure 2.18 NTF(Z) Frequency Response of 2nd Bandpass Modulator

2.3.3 Four Order Bandpass Sigma Delta Modulator

A fourth-order bandpass sigma-delta modulator is shown in Fig. 2.19. We can derive the noise transfer function, NTF(z), and signal transfer function, STF(z).

$$NTF(Z) = (1 + Z^{-2})^2 \qquad STF(Z) = -Z^{-2} \tag{2.37}$$

The modulator output Y(z) is express by

$$Y(Z) = -Z^{-2}X(Z) + (1 + Z^{-2})^2 E(Z) \tag{2.38}$$

The NTF(Z) frequency response is shown in Fig. 2.20.

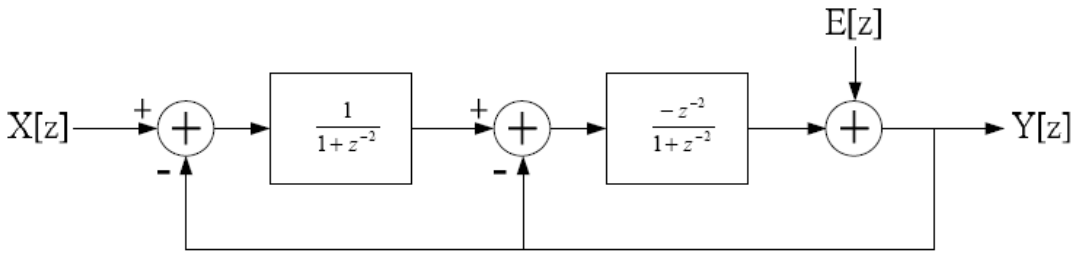


Figure 2.19 The Four Order Bandpass Sigma Delta Modulator

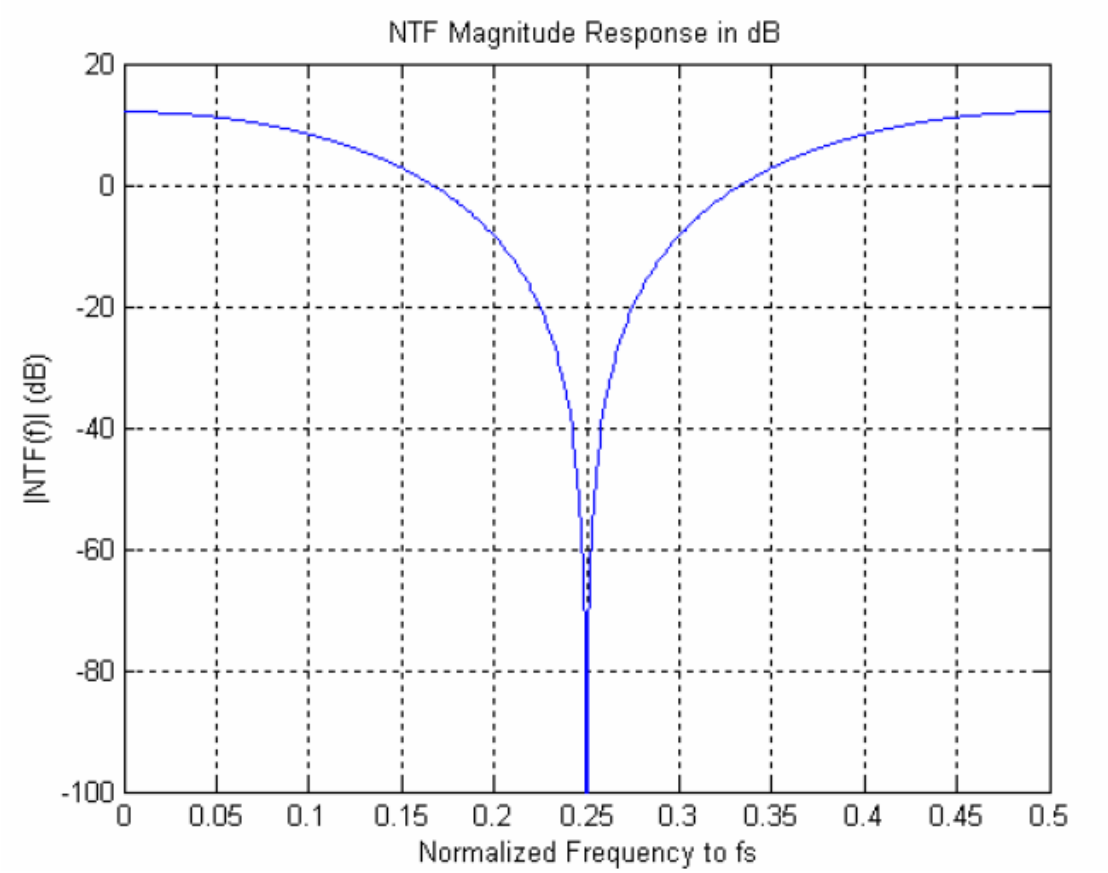


Figure 2.20 NTF(Z) Frequency Response of 4th Bandpass Modulator

Since the fourth-order bandpass sigma-delta modulator has two zeros fall in the band of interest, it is sharper than the second-order bandpass sigma-delta modulator. The in-band noise is the same as second-order lowpass sigma-delta modulator. Each doubling of the sampling frequency decreases the in-band noise by 15 dB, but increases the resolution by 2.5 bits.

According to the discussion above, bandpass sigma-delta converters employing Lth-order modulators display a SNR performance that improves at the rate of 6L+3 dB per octave increment with the oversampling ratio tio $_{s}{}_{B}f$ 2 f and also increase the resolution by L+0.5 bits [18].

CHAPER 3
DESIGN OF THE LOW POWER BANDPASS SIGMA DELTA MODULATORS

The low power devices is the trend with the personal communication and WLAN developed. Low power is the most important reason to extend the lifetime of the battery. In this chapter we describe the low power bandpass sigma delta A/D converter by time interleaved architecture. In section 3.1, the different architectures of the resonator for bandpass SDM are reviewed [2][19]. In section 3.2, we introduce the time interleaved architecture for bandpass application. And it's shown the design of the four-path bandpass sigma delta A/D converter by using four-channel lowpass channels. In section 3.3 we discuss the mismatch effect of the time interleaved system, and a fully digital background calibration will be proposed.

3.1 Prototype of switched-capacitor resonator

3.1.1 Resonator in Z-Domain [20]

In -domain a resonator has ideally two poles on the unit circle, but due to different non-idealities the radius (γ) differs from the ideal value of one; the complex pole pair can be written as

$$z_{p1,2} = \gamma(\cos(\theta) \pm j\sin(\theta)) = \gamma e^{\pm j\theta} \qquad (3.1)$$

where θ=2πfc/fs is the notch frequency in radians. The transfer function of the resonator is

$$H_{res}(z) = \frac{1}{(z - z_{p1})(z - z_{p2})} = \frac{z^{-2}}{1 - 2\gamma\cos(\theta)z^{-1} + \gamma^2 z^{-2}} \qquad (3.2)$$

If the gain of the resonator is g_0, we can write the transfer function as follows:

$$H_{res}(z) = \frac{g_0 z^{-2}}{1 - p_1 z^{-1} + p_2 z^{-2}} \tag{3.3}$$

By comparison to (3.2), we have relationships

$$\gamma = \sqrt{p_2} \qquad \theta = \arccos\left(\frac{p_1}{2\sqrt{p_2}}\right) \tag{3.4}$$

There is special interest in resonators with the notch frequency of $f_s/4=\pi/2$, because it relaxes the design of the digital part in radio [21]. Then the term p_1 is ideally zero and the p_2 should be one to guarantee the maximum notch *Q*-value, which is ideally infinite or the pole lies on the *jw*-axis in the *s*-domain.

For $f_s/4$-resonator the relative frequency error is

$$\frac{\Delta f}{f_o} = \frac{|\pi/2 - \theta|}{\pi/2} = \left|1 - \frac{2}{\pi}\arccos\left(\frac{p_1}{2\sqrt{p_2}}\right)\right| \rightarrow \frac{\Delta f}{f_o} \approx \left|\frac{p_1}{\pi}\right| \tag{3.5}$$

We note that the possible frequency error is caused by the p_1-term (near zero) and the effect of the error in the p_2–term (near one) is negligible.

When we have pole $s_p = \sigma_p + jw_p$ in the *Q*-domain, the notch -value is determined by

$$Q_s = \frac{\sqrt{\sigma_p^2 + \omega_p^2}}{2|\sigma_p|} \tag{3.6}$$

The s_p mapped to the *z*-domain is

$$z_{sp} = e^{(\sigma_p + j\omega_p)T} = e^{\sigma_p T + j\omega_p T} = \gamma e^{j\theta} \tag{3.7}$$

and we get the relationships

$$\omega_p = \theta / T \qquad \sigma_p = \ln(\gamma)/T \tag{3.8}$$

Now the notch Q-value can be written in the z-domain as

$$Q_z = \frac{\sqrt{(\ln(\gamma))^2 + \theta^2}}{2\,|\ln(\gamma)|} \tag{3.9}$$

and using the terms p1 and p2

$$Q_z = \frac{\sqrt{(\ln(\sqrt{p_2}))^2 + (\arccos(\frac{p_1}{2\sqrt{p_2}}))^2}}{2\,|\ln(\sqrt{p_2})|} \quad \Rightarrow \quad Q_s \approx \frac{\pi}{4(1-\sqrt{p_2})} \tag{3.10}$$

Hence, the notch Q-value is mainly determined by the term p2 (near one) and the error in p1 (near zero) has a negligible effect on the magnitude of the notch Q.

3.1.2 Discrete-Time Resonator Topologies

A discrete-time resonator can be implemented with different structures , such as forward Euler (FE), lossless discrete integrator (LDI)[2] or double delay (DD)[19].

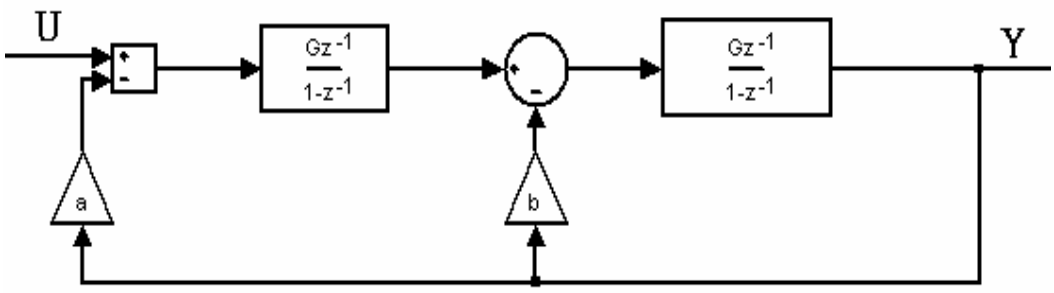


Figure 3.1 Forward Euler Resonator (FE)

The FE resonator (Figure 3.1) consists of two identical integrators with the feedback terms a and b. If the gain error of integrators due to capacitor mismatch is ε_c, the transfer function is

$$H_{FE}(z) = \frac{(1+e)^2 z^{-2} U(z)}{1-(2+b(1+e))z^{-1} + (1-a(1+e)^2 + b(1+e))z^{-2}} \tag{3.11}$$

The notch frequency can be moved by the parameter **a**. If we select **a=b=-2** the

notch is fixed ideally at fs/4. We noticed that both the notch frequency and the notch Q-value are dependent on the gain error. Therefore, this structure is not favored.

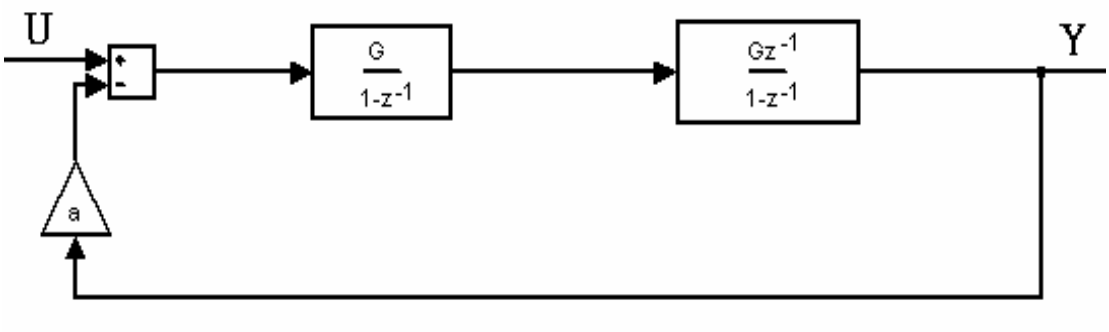


Figure 3.2 Lossless Discrete Integrator (LDI)

The LDI resonator (Figure. 3.2) also consists of two integrators, but the other is delay free and the loop has only one feedback coefficient **a**. The transfer function can be found to be

$$H_{LDI}(z) = \frac{(1+e)^2 z^{-2} U(z)}{1-(2+a(1+e)^2)z^{-1}+z^{-2}} \tag{3.12}$$

Now the notch frequency can be changed by the parameter **a** and with **a= -2** it is ideally fixed at fs/4. We have a notch Q of infinity, yet its requency is dependent on the integrator gain errors. In this sense it could be regarded as better than FE, but the gain error affects the notch frequency more than in FE and the inaccurate notch frequency decreases the performance.

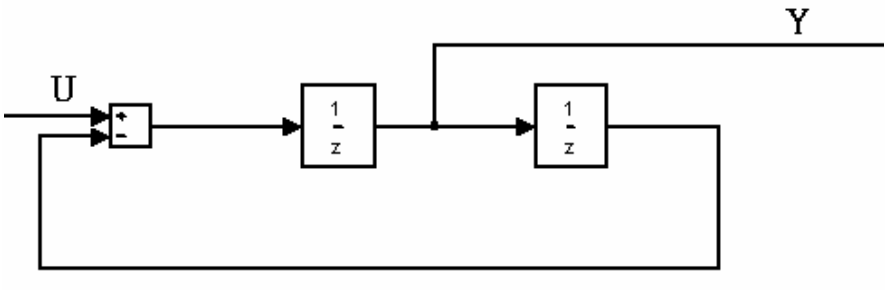


Figure 3.3 Double Delay Resonator (DD)

The DD resonator (Figure. 3.3) consists of two delay, it is sensitive to the integrator gain **g**. The transfer function can be found to be:

$$H_{DD}(z) = \frac{(1+e)\ z^{-1}U(z)}{1+gz^{-2}} \tag{3.13}$$

This is exactly the inverse of the LDI loop in the sense that the angle (frequency) of the poles is fixed, but the magnitude (notch depth) is sensitive to the loop gains. The disadvantage of this structure is that it must have a high DC gain OP design.

3.1.3 The Design Challenge of Bandpass Sigma Delta Modulator

Due to the above discussion, we got know that the performance of the bandpass sigma delta modulator is more sensitive to capacitor mismatch than the lowpass sigma delta modulator. The capacitor mismatch causes the center frequency and notch depth drift (FE and LDI). And the bandpass sigma delta modulator is operated at very frequency, so the operational amplifier must have wide bandwidth and high slew rate, even high gain (DD) to avoid non-ideal effect [8]. The higher speed operation the more complex design need. To reduce the high speed operation and complex design, we combine the time interleaved system and noise transfer function synthesis to design the bandpass sigma delta by using four paths lowpss sigma delta modulator.

3.2 Design A Time-Interleaved Bandpass Sigma Delta ADC

3.2.1 Time Interleaved System & Noise Transfer Function Synthesis

An attractive way to increase the conversion rate of ADCs is to use time-interleaved techniques where several ADCs, using different clock phases, are operated in parallel [22] [23]. This enables higher total conversion, make high speed is possible.

The concept of time-interleaving (or called N-path structure) is illustrated in Figure 3.4. The HPi(Z) is a A/D converter channel. The converters can be of any type and are operated at Fs/N where Fs is the total sampling frequency of the time-interleaved ADC and N is number of channels. The speed requirements on each converter are relaxed by a factor N but the number of converters is at the same time increased by the same factor. It is trade off between performance (SNDR, operational bandwidth) and cost (power consumption, die area).

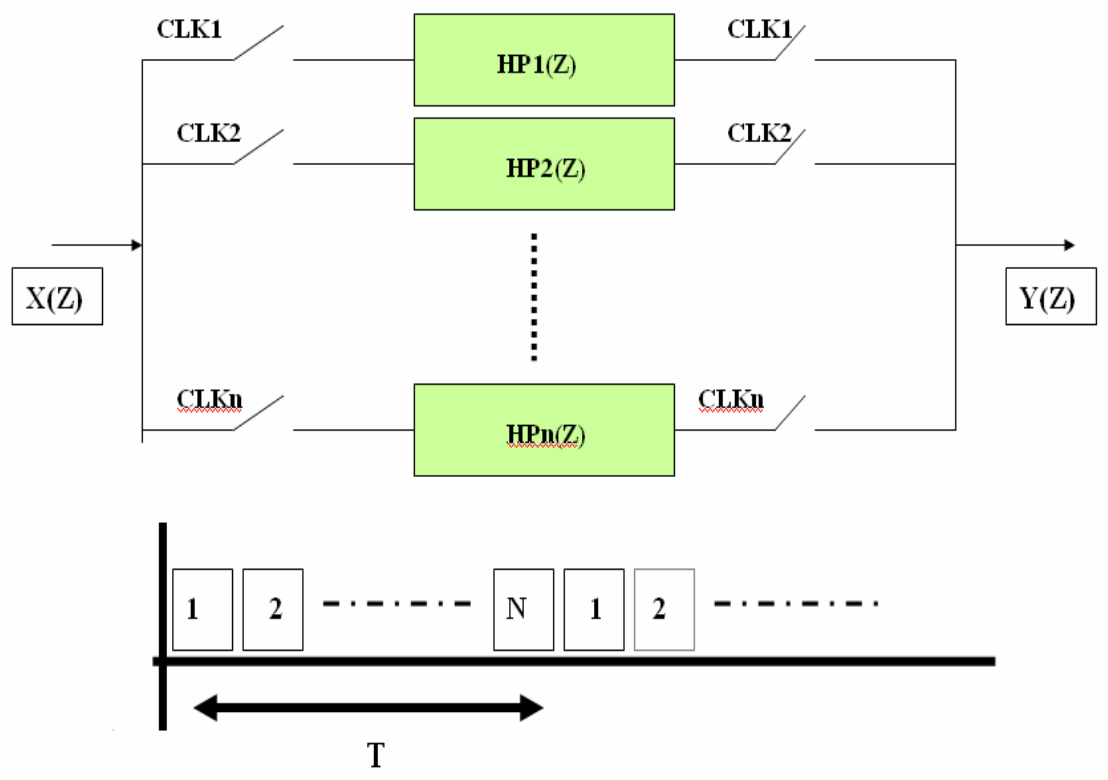


Figure 3.4 Time Interleaved System (N-Path Structure)

We can implement the resonators by **N-path structure with Noise Transfer Synthesis** [24] [25]**.** In the block diagram of a generalized N-path converter shown in Figure 3.4, the N channels comprising the structure, $H_1(Zp)$, $H_2(Zp)$,… …, $H_N(Zp)$, are nominally identical. From the clocking diagram in Figure 3.4, it is seen that the paths are clocked in an interleaved fashion and that the sampling rate of each path channel is reduced by a factor N relative to the effective throughput rate of the overall N-path structure. Thus, the constituent circuits of the individual path channels have settling requirements that are relaxed by a factor of N with respect to the requirements imposed by a direct single-path implementation of the same transfer function.

If the paths in the N-path channels of Figure 3.4 are assumed to match perfectly, such that $H_1(Zp) = H_2(Zp) = \cdots = H_N(Zp) = H(Zp)$, then the Z-domain transfer function of the structure is

$$\frac{Y(Z)}{X(Z)} = H(Zp)\big|_{Zp=Z^N} \tag{3.14}$$

Where H(Zp) denotes the transfer function of each identical path channel [26]. In this expression, Zp corresponds to the Z variable of a single path, and Z_p^{-1} is interpreted as a single delay with respect to the sampling rate of a single path. Z^{-1} represent a single delay with respect to the effective throughput rate of the N-path channel, as implied by the relationship $Z_p = Z^N$ [3]**.**

According above description, we can make a bandpass notch at 1/4 sampling frequency by synthesizing four channel lowpass sigma delta ADCs. Because each channel has lowpass shape, it's attenuation spectra is replicated every Fs/8, as shown in Figure 3.5, thus leading to the desired bandpass NTF.

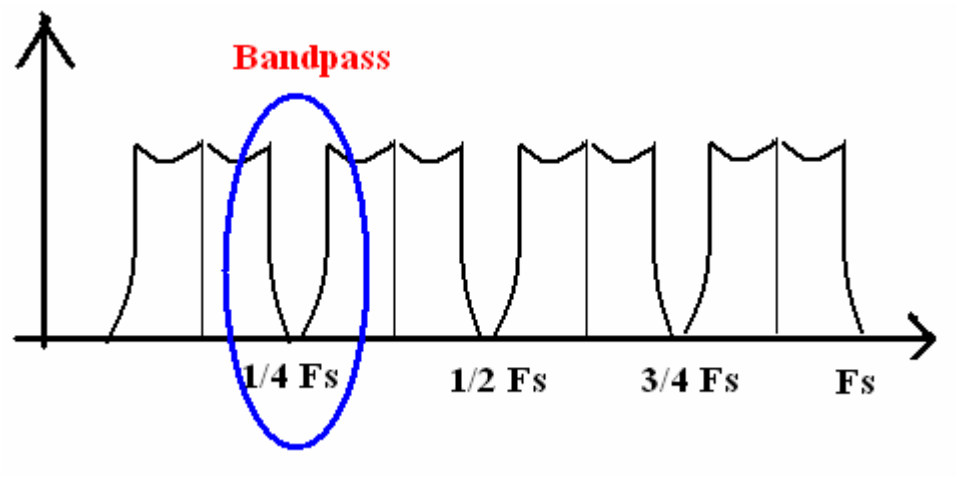


Figure 3.5 Output Spectrum of the Four Path Modulator

3.2.2 System Level Design and Simulation of a Bandpass Modulator

The application of the bandpass sigma delta modulator is GSM system. The signal bandwidth is 200 KHz, center frequency is 20 MHz, sampling frequency is 80 MHz, and the oversampling ratio, OSR, is 200. The system design and simulation by Matlab tools [27].

In the Matlab simulation, the system architecture is shown in Figure 3.6. The $\Sigma\Delta$ block is the lowpass sigma delta modulator operated in Fs/n. The Z-delay in the front and the back of the modulator operated in full speed Fs is modeling the signal switch from the input to each channel to synthesize the bandpass noise transfer function.

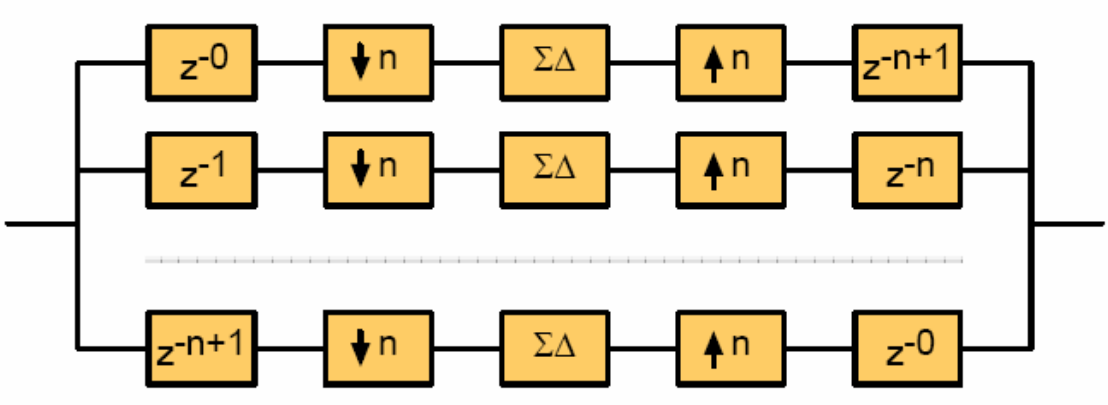


Figure 3.6 System Architecture of Matlab Simulation

The ADCs in the each channel are the same. The basic component in the time-interleaved system is the lowpass sigma delta modulator and it is operated in 1/4 sampling frequency. Due to the specification of the bandpass sigma delta for GSM application, we get the unit ADC is a second order lowpass sigma delta modulator shown in the Figure 3.7[27].

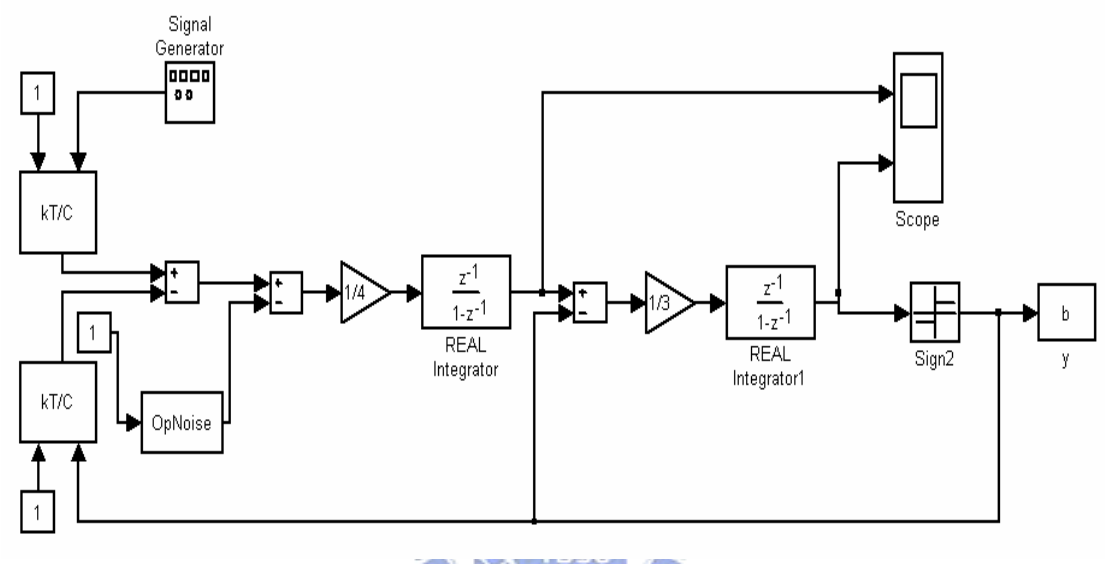


Figure 3.7 The Second Order Lowpass Sigma Delta Modulator

Because the power spectrum of the lowpass SDM will be replicated every Fs/8, the bandwidth of the lowpass SDM just to be 100 KHz, not 200 KHz. And each lowpass SDM is operated in 1/4 sampling frequency, 20 MHz. The block “Real Integrator” in Figure 3.7, it models the gain, unit-gain bandwidth, slew rate, output swing, and input noise of the operation amplifier. The block “kT/C” models the thermal noise by input capacitor size. The test signal is -6dB at 90 KHz and the SNDR is 69 dB calculated by 65536 points FFT. The power spectrum density is shown in Figure 3.8. The summary of the simulation result lists in the table 3.1.

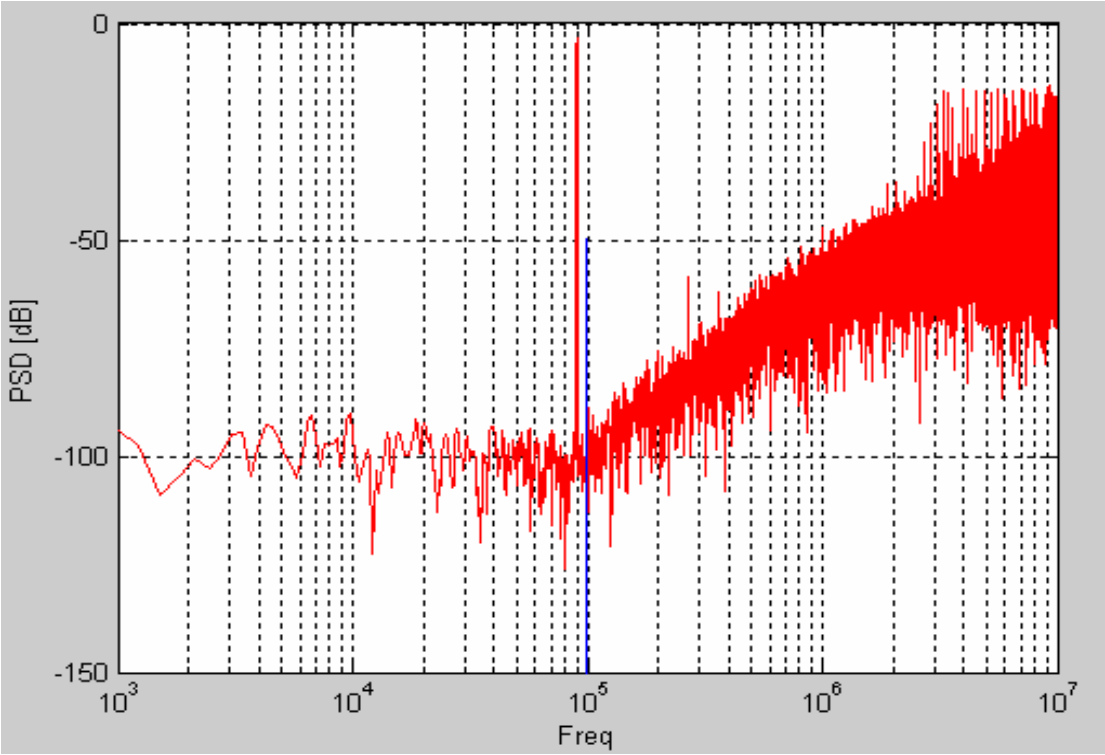


Figure 3.8 The Power Spectrum Density of the Second Order Lowpass SDM

Frequency	20 MHz	Gain	60 dB
Bandwidth	100 KHZ	UG-BW	200 MHz
OSR	100	Slew-Rate	60 v/us
Peak-SNR	69 dB	Output Swing	1 Vref

Table 3.1 Simulation Result of Second Order Lowpass SDM

After designing the lowpass sigma delta modulator, we combine the time interleaved technique and noise transfer function synthesis to design the bandpass sigma delta modulator with the bandwidth 200 KHz, and the center frequency located at 20 MHz. In the Figure 3.9 is showing the architecture of the bandpass sigma delta modulator. The blocks “Path1” ~ “Path4” are the same ADC, lowpass sigma delta modulator, in Figure 3.7. Then give the test input signal in -6 dB at 20 MHz, the SNDR is 77 dB calculated by 65536 points FFT. The power spectrum density is shown in Figure 3.10.

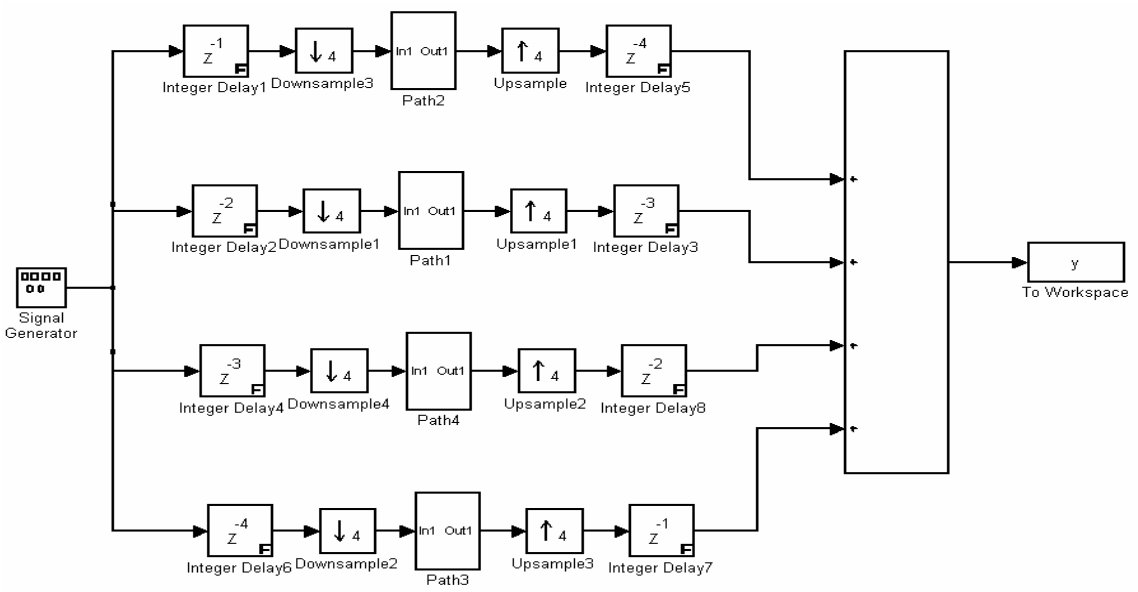


Figure 3.9 The Four Path Bandpass Sigma Delta Modulator

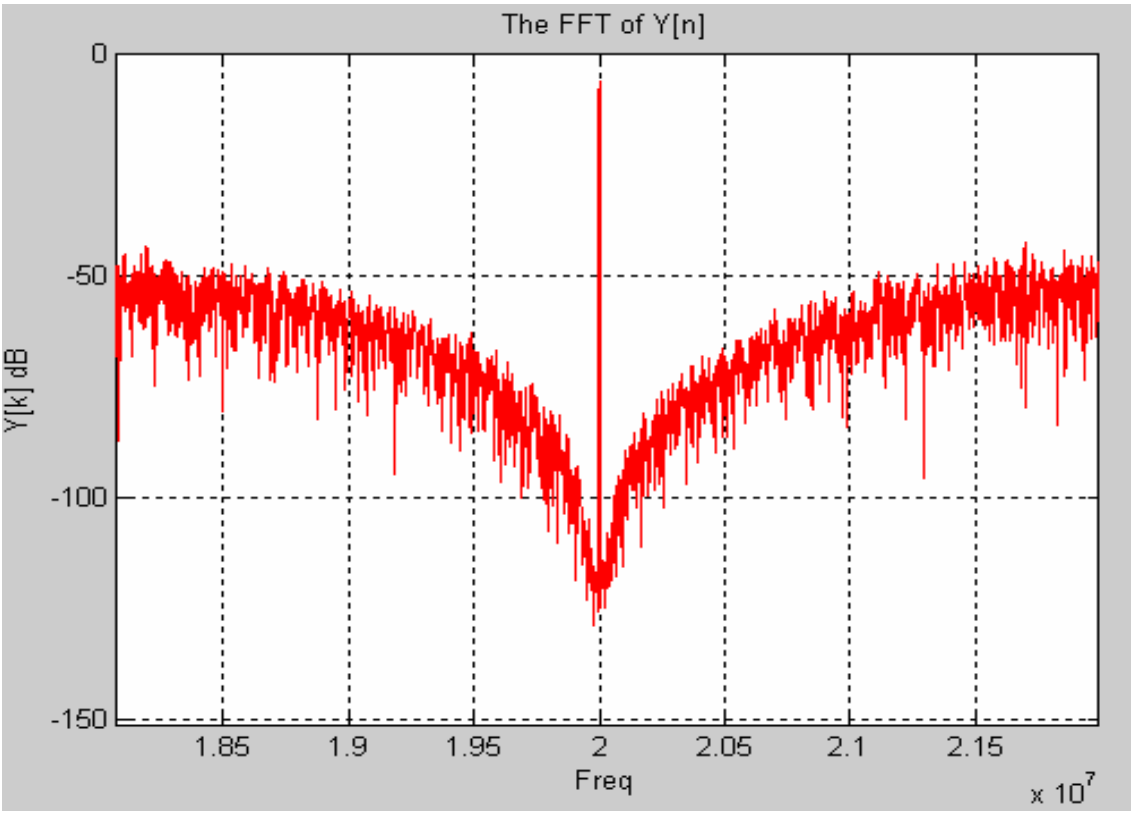


Figure 3.10 The Power Spectrum Density of the Four Path Bandpass SDM

3.3 Gain and Offset Calibration in Time Interleaved System

3.3.1 The Gain and Offset Mismatch in Time Interleaved System

Although the four path time-interleaved bandpass sigma delta modulator can operate 1/4 sampling frequency to reduce the power consumption and each channel, lowpass sigma delta modulator, is easy to design and non-sensitive to the capacitor mismatch.

Unfortunately, the penalty of capacitor mismatch transfers to the channel mismatch. The performance of interleaved ADC's is sensitive to mismatches between the individual channels [23][28][29]. Channel offset mismatches cause additive tones at integer multiples of the channel sampling rate Fs/N. Channel gain mismatches result in amplitude modulation of the input samples, causing scaled copies of the input spectrum to appear centered around integer multiples of the channel sampling rate. Errors in the sample times result in phase modulation of the input samples, which also causes scaled copies of the input spectrum to appear centered at the same frequencies as the spurious components stemming from gain mismatch. All these mismatches increase the noise floor of the ADC system and degrade the signal-to-noise ratio.

The tone produced by offset mismatch is independent of the input frequency, it appears in:

$$\frac{f_s}{N} \bullet m \qquad m = 0.1.2...N-1 \tag{3.15}$$

And the tone produced by gain mismatch is dependent of the input frequency, it appears in

$$f_{in} + \frac{f_s}{N} \bullet k \qquad f_s - (f_{in} + \frac{f_s}{N} \bullet k) \qquad k = 0.1.2...k-1 \tag{3.16}$$

Because of the gain and offset mismatch, the SNDR of the ADC is reduced. We must to do something to calibrate the mismatch effect.

3.3.2 The Fully Digital Background Calibration

Calibration techniques have been proposed in the past to solve the problem. They can be divided in two groups: offline and online.

The former are easier to be implemented since they can be performed in factory by trimming voltages/currents as illustrated in [30]. However, this offline solution is unable to track offset variations with temperature or ageing over time. Another solution is based on calibration procedures applied in foreground as illustrated in [31]. However, the calibration process interrupts the input signal conversion. Finally, an offline solution specifically dedicated to modulators is reported in [32]. This solution is based on finding the optimum value for a cross-coupling coefficient by carrying out extensive simulations during the design step. Again this solution cannot correct variations of the offsets with temperature or ageing.

On-line calibration techniques are more difficult to implement, since they operate in background while the ADC is working normally. Several solutions for achieving online calibration has been presented in literature [33] [34], usually in the digital domain. Unfortunately, most of them are only suitable for deterministic time-interleaved ADCs and cannot be applied to modulators in view of their stochastic behavior, which makes the output signals obtained with the same input signal at different times different, depending on the previous history.

To avoid complex calibration way such like [33][34], we using a fully digital calibration circuit [35]. The offset and gain variations are considered but only offset calibration circuit is implemented. The proposed calibration circuit is an extension version of [35] that implement both offset and gain calibration function. Moreover, power consumption of calibration circuit is also considered not only in calibration process but in normal functional mode as well to construct a true low-power A/D. The I/O of ADCALI is as shown in figure 3.11. Signal “CAL” is to switch to calibration mode. Signal “GO” is to tell ADCALI to start calibration process. “CH1” to “CH4”

are inputs of channel to channel 4 and signal “CHR” is the reference channel. The output signal “READY” means that ADCALI is ready to calibrate one of these channels. Signal “SUCCESS” is asserted when channel is calibrated successfully. If calibration process is failed due to divide-by-zero, “SUCCESS” will be low and “DIVBYZ” will be asserted.

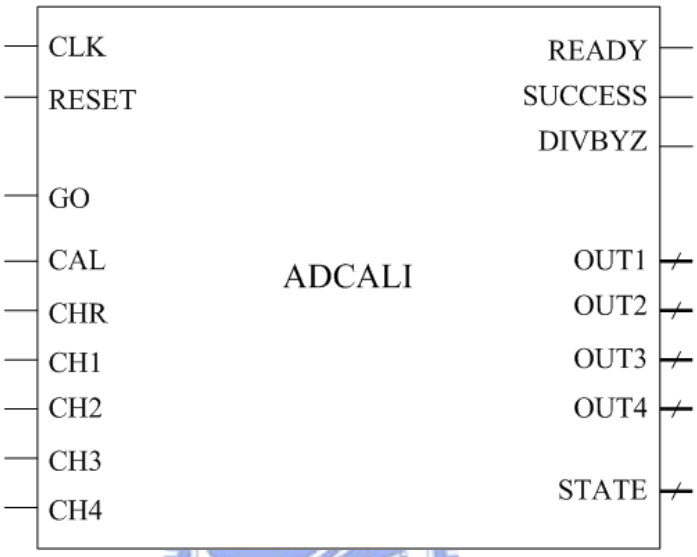


Figure 3.11 The Top View of The Calibration Circuit

As shown in figure 3.12 the ADCALI is constructed by four parts, namely OffGain, FSM_T, CLK_gen, and ACC respectively. These subparts of ADCALI are described in sequel of the thesis.

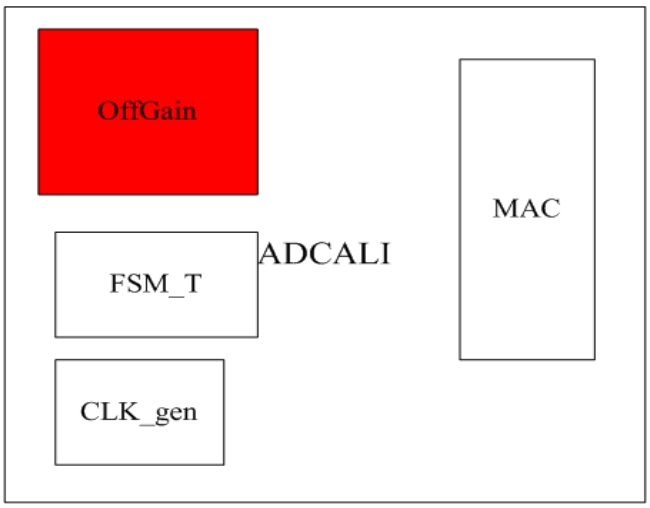


Figure 3.12 Blocks of The Calibration Circuit

FSM_T

The finite state machine is the main controller of ADCALI. The state diagram is shown in figure 3.13. It consists of six states, namely RST, RUN, CAL1, CAL2, CAL3 and CAL4 respectively. When “RESET” is high, it will stay at RST state. When A/D is operated in normal mode (“CAL” is low), it will stay at RUN state. CAL1 to CAL4 is for calibration of channel 1 to channel 4. When it is at these states, the gated clock will be released and OffGain is live to calibration. It means that when state is RUN, the unnecessary power consumption of OffGain will be reduced to minimum.

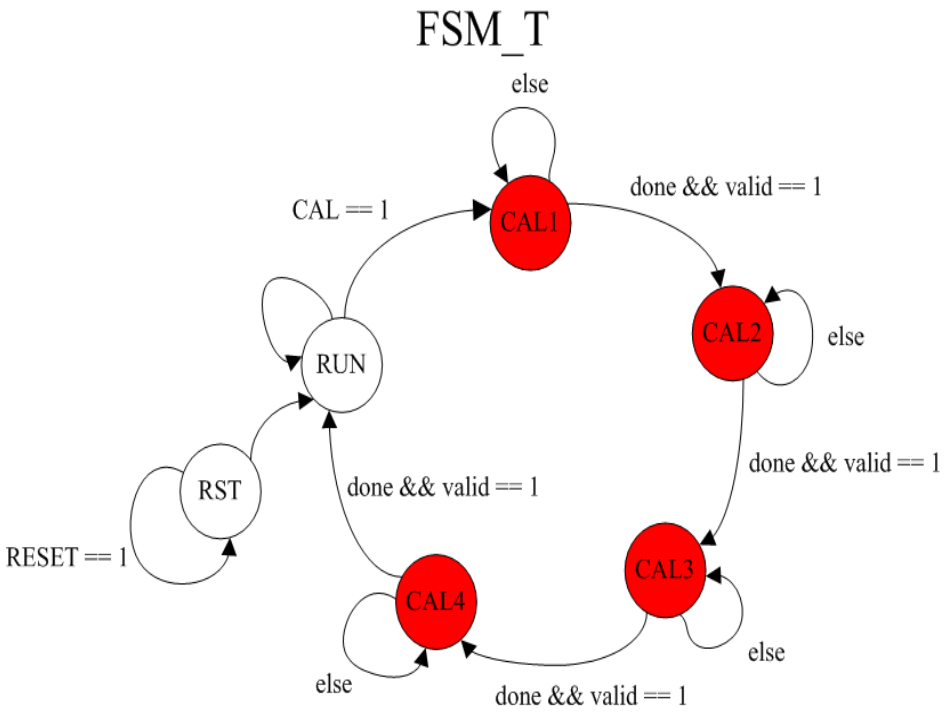


Figure 3.13 The State Diagram of The FSM_T

CLK_gen

The clock generator is actually a clock gating circuit. As shown in figure 3.14, it consisted of a negative-edge-triggered flip-flop and a AND gate. When signal "START" is high, clock signal can observed at "Clk_g". The purpose of this flip-fop is to prevent the glitch when "START" signal is switching.

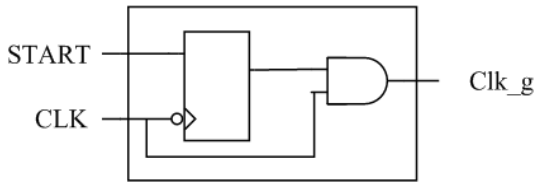


Figure 3.14 Clock Generator

OffGain

There is another controller in OffGain to control calibration process in detail. The state diagram of FSM_O is shown in figure 3.15. There are nine states in FSM_O. RST is to reset the whole OffGain and RST_TIMER_ACC is to reset timer and accumulators. If the state is RDY, signal "READY" will be asserted to indicate it's ready to calibrate. When "GO" is high, calibration process is really started. The WAIT_ACC is to wait accumulator for specific clock cycles. When the accumulation is completed, the difference will be save at SAVE_OFF state. If channel 1 is in calibration, the division is not needed and it will switch to DONE state. The reset channels will need division and START_DIV is to trigger divider. WAIT_DIV is to wait for divider to complete division. Gain parameter will be saved when the state is SAVE_GAIN. If the divider warns divide-by-zero condition, signal "valid" (not shown in figure) will be de-asserted and this calibration will be indicated not successful.

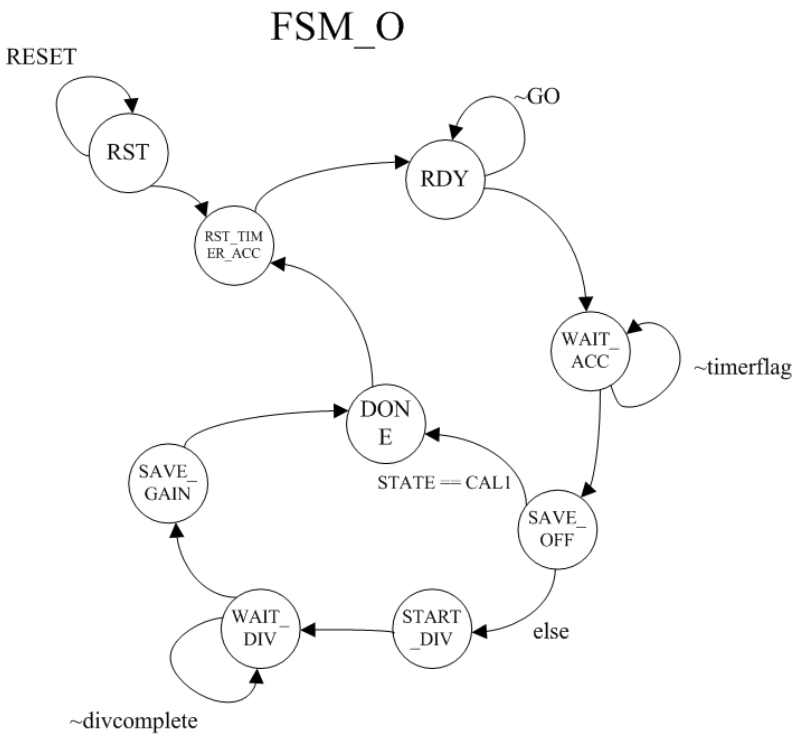


Figure 3.15 The State Diagram of FSM_O

OffGain calculates the difference between reference channel and normal channel and is the main part of ADCALI. The concept datapath diagram of OffGain is shown in figure 3.16. As in [35], the offset parameter is calculated by the difference between the accumulation of reference channel and the accumulation of specified channel. The Timer is to count a specific clock cycles for Accumulator and AccumulatorR. The default cycle number is 4096. If the counting number is 4096, Timer will be stopped and timerflag will be asserted. Note that signal “timerflag” controls two AND gate arrays (the yellow blocks in fig 3.16) to gate the result of accumulators. The subtraction will be operated only when the accumulation completed to reduce the power consumption during calibration. The difference will be sent to registers specified by FSM_O. Meanwhile, it will also be sent to either Dividend register or Divisor register. According to the calibration equation of gain parameter in [35], the real destination is depend on which channel is in calibration. If channel 1 is in calibration, the difference will be in divisor register. And the differences of the reset

channel will be in dividend register. When the division is completed, the quotient will be sent to specified gain register.

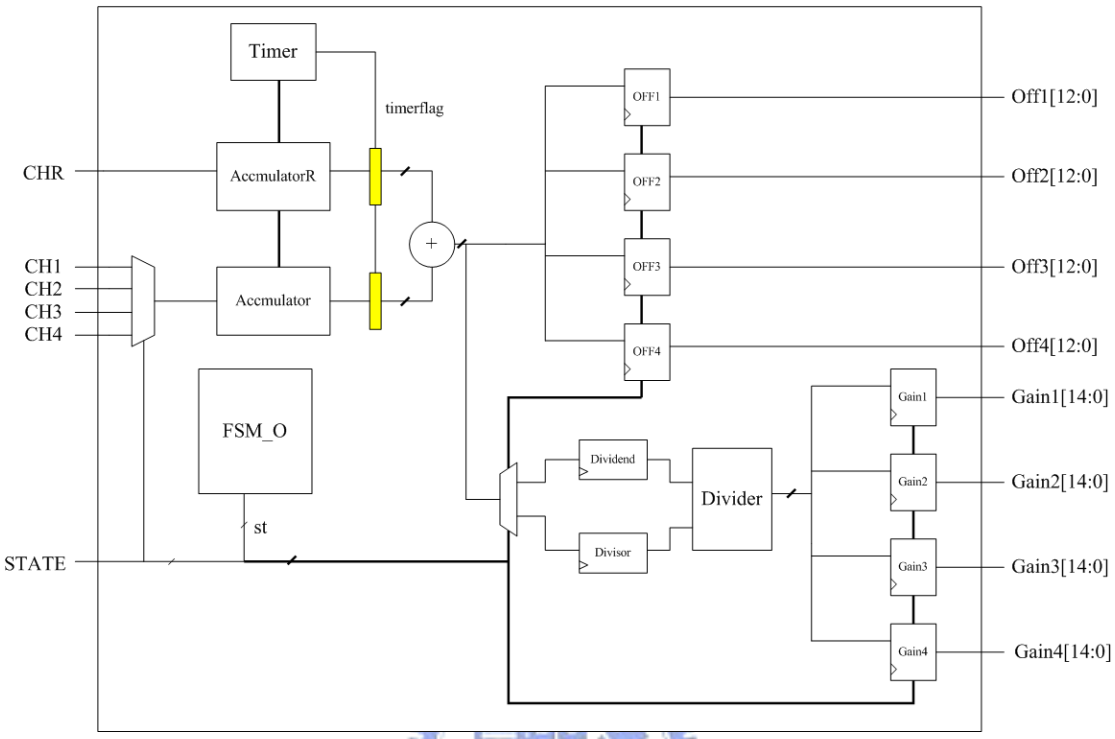


Figure 3.16 The Concept Datapath Diagram of OffGain

ACC

The ACC is to output the real channel value after the calibration is completed. The actual function of ACC to determine whether the output is the addition of gain parameter and offset parameter or zero since the input of channel is just one bit. Consequently, the EQUATION in [35] will be simply reduced to a adder and a multiplexer. The circuit diagram is as shown in figure 3.17.

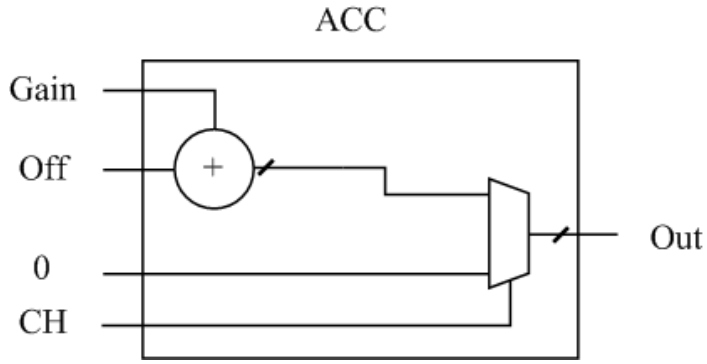


Figure 3.17 The Final Output After Calibration

CHAPER 4

IMPLEMENTATION OF A BANDPASS SIGMA – DELTA MODULATOR

This chapter describes and implementation of a fs/4 bandpass modulator that utilizes the four-path architecture proposed in chaper3. First review the switch phase in the time interleaved system, and show the sigma delta modulator how to work in the switch-capacitor circuit. Then the components of the design, wide-swing bias, folded-cascode operational amplifier, comparator, two phase clock generator, and etc are shown in section 4.2. Final simulate and layout with TSMC 0.18 μm CMOS process.

4.1 Block Diagram of Four Path Bandpass Modulator

4.1.1 Four Path Bandpass Sigma Delta Modulator

Like the system level design of the four path bandpass modulator, it needs a multiplexer to select the channel to transfer the input signal and de-multiplexer to transfer the signal to output. Channel selection is the most important to implement the time interleaved system, so the clock phase of each channel must to take care. The clock phase of the switch selection is shown in Figure 4.1.The clock phase of each channel are different and the four path have four clock phase. We can use a clock divider to reduce the clock frequency from 80 MHz to 20 MHz and generate four different phase clock with 25% duty cycle.

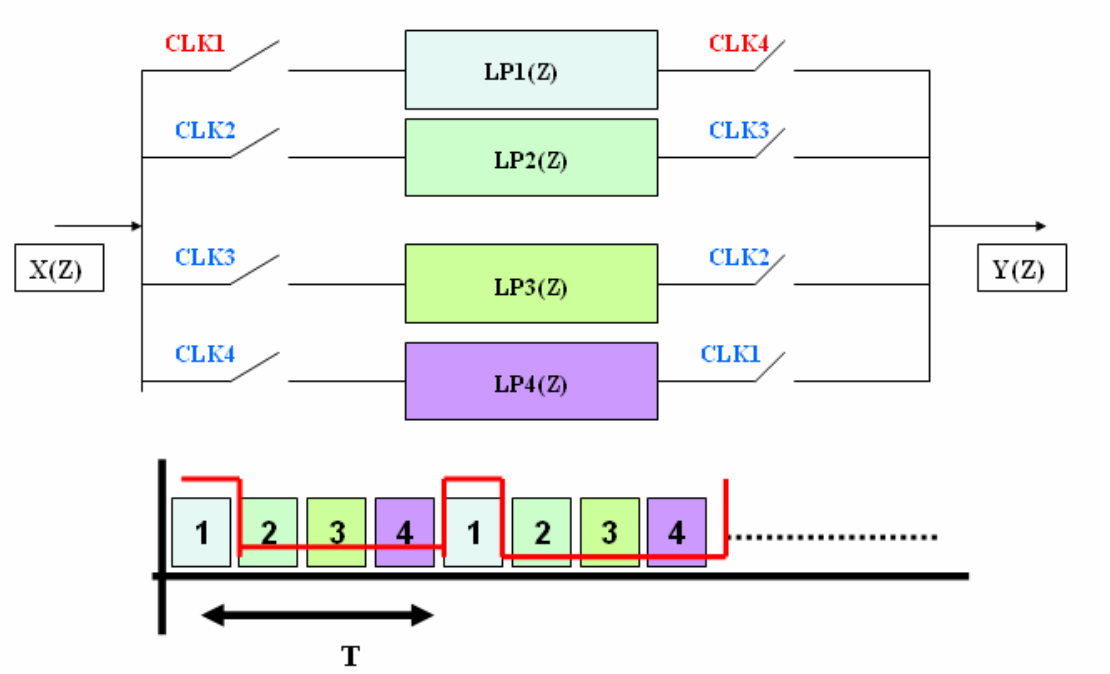


Figure 4.1 Clock Path of Four Path Bandpass Sigma Delta Modulator

4.1.2 Second Order Sigma Delta Modulator

Figure 4.2 shows a fully differential switched-capacitor implementation of the modulator consisting of two identical parasitic-insensitive switched-capacitor integrators, a comparator that serves as a 1-bit ADC, and a distributed two level (1-bit) DAC. The modulator operates on a two-phase non-overlapping clock, similar to that employed in many digital systems. During phase 1, switches S1 and S3 conduct so that the differential input to the modulator is sampled onto the left sides of he first integrator's sampling capacitors, C1, while the right sides are connected to the desired common-mode input voltage of the operational amplifier, Vcmi. Likewise, the differential output of the first integrator is sampled onto capacitors C1 of the second integrator. The comparator is strobed during phase 1, when the output of the second integrator is not changing.

At the end of phase 1, switches S3 are opened slightly ahead of switches S1 to reduce signal-dependent charge injection onto the sampling capacitors C1[17]. Since

switches S3 are near the virtual ground of the operational amplifier, and therefore at the same potential, ideally no differential charge is injected onto the sampling capacitors C1 when they are turned off. When switches S1 are opened a short time later, the rght sides of the sampling capacitors C1 are floating so that no differential charge from S1 is injected onto these capacitors.

During phase 2, switches S4 are closed and the left sides of the sampling capacitors C1 are connected via the switches S2 to either Vref+ or Vref-, depending on the result of the comparison performed during phase 1. This action performs both the D/A conversion and subtraction functions. As a result, a packet of charge proportional to the difference between each integrator's input and the DAC's output is transferred to the integrating capacitors C2. At the end of phase 2, switches S4 are opened slightly ahead of switches S2 to isolate the inputs of the operational amplifiers from the differential charge injection introduced by opening S2. The comparator is reset during phase 2 in preparation for the next comparison.

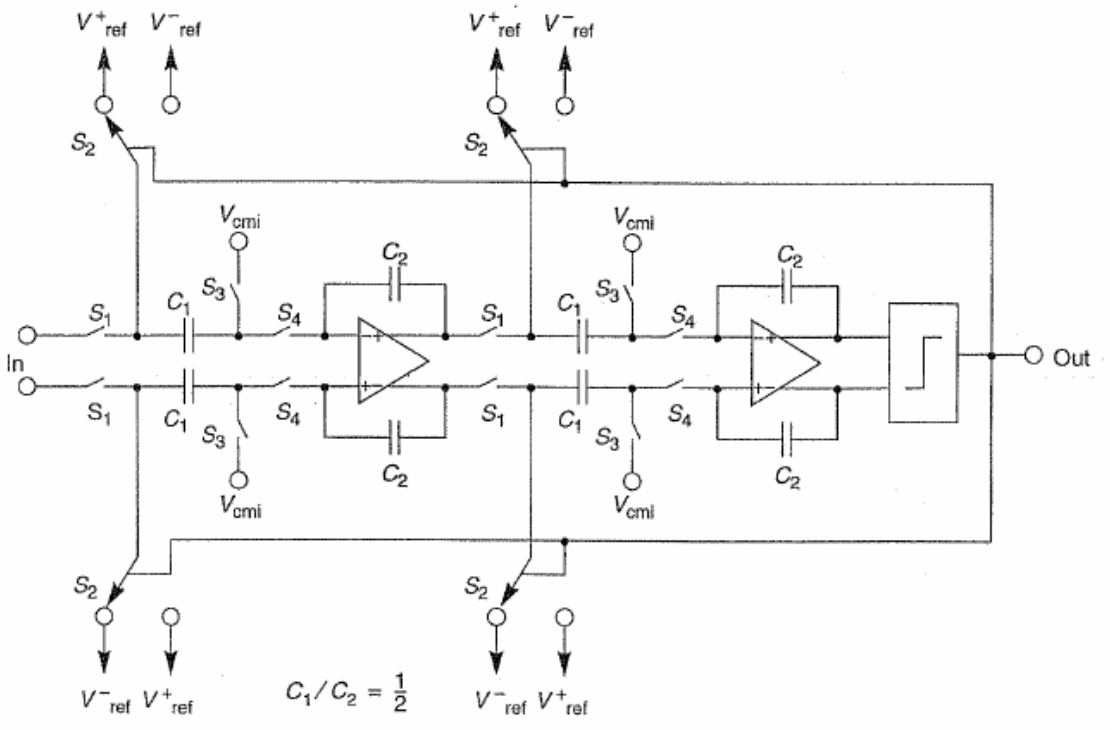


Figure 4.2 Fully Differential CMOS implementation of a 2nd SDM

4.2 Design and Simulation of Sub-Circuits

4.2.1 Wide Swing Constant-Transconductance Bias Circuit

It is possible to incorporate wide-swing current mirrors into the constant –trans-conductance bias circuit. This modification greatly minimizes most of the detrimental second-order imperfections caused by the finite-output impendence of the transistors, without greatly restriction signal swings. The complete circuit is shown in Fig. 4.3. [36]This circuit consists of bias loop , cascade bias and start-up circuitry.

The n-channel wide-swing cascade current mirror consists of transistors M1 - M4, along with the diode-connected biasing transistor M5. The pair M3,M4 acts similarly to a diode-connected transistor at the input side of the mirror. The output current comes from M1. The gate voltages of cascade transistors M1 and M4 are derived by the diode-connected transistor M5. The current for this biasing transistor is actually derived from the bias loop via M10 and M11.

Similarly, the p-channel wide-swing cascade current mirror is realized by M6 - M9. Transistors M8 and M9 operate as a diode-connected transistor at the input side of the mirror. The current-mirror output current is the drain current of M6. The cascade transistors M6 and M9 have gate voltages derived from diode-connected M14, which has a bias current derived from the bias loop via M12 and M13.

The bias loop does have the problem that at start-up it is possible for the current to be zero in all transistors, and the circuit will remain in this stable state forever. To ensure this condition does not happen, it is necessary to include start-up circuitry that affects only the bias-loop in the case that all currents in the loop are zero.

Table 4.1 shows the W/L ratios of transistors in the bias circuit.

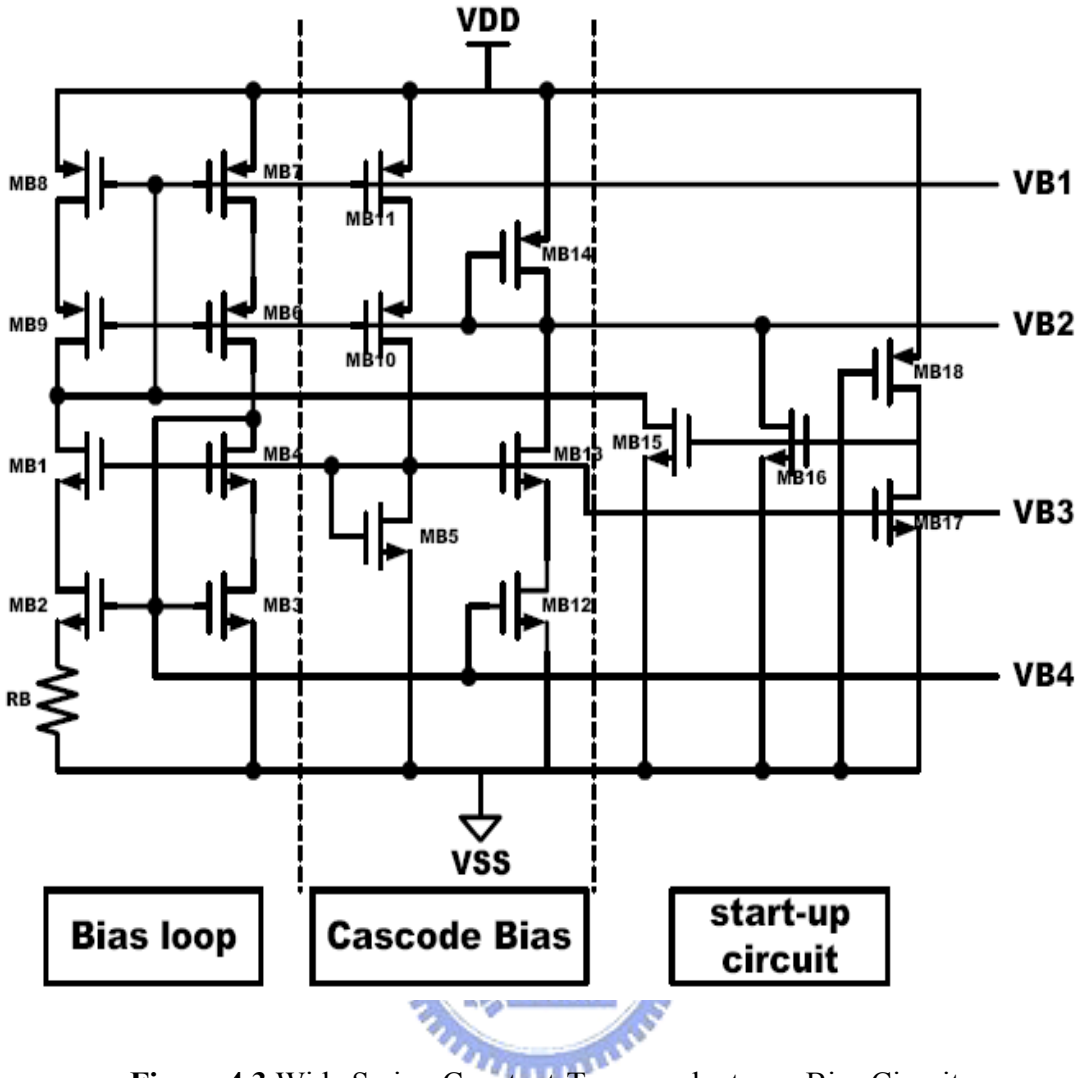


Figure 4.3 Wide Swing Constant-Transconductance Bias Circuit

Table 4.1 Transistors Size of the bias circuit

Transistor	Type	W/L （μm）	M
M1, M3, M4	**n-type**	**3 / 0.3**	**1**
M2	**n-type**	**12 / 0.3**	**1**
M5	**n-type**	**0.6 / 0.3**	**1**
M6, M7, M8, M9	**p-type**	**15 / 0.3**	**1**
M10	**p-type**	**15 / 0.3**	**1**
M11	**p-type**	**15 / 0.3**	**1**
M12 , M13	**n-type**	**15 / 0.3**	**1**
M14	**p-type**	**15 / 0.3**	**1**
M15, M16, M17	**n-type**	**15 / 0.3**	**1**
M18	**p-type**	**0.8 / 6**	**1**
RB		**2.2** KΩ	

4.1.2 The fully Differential Folded Cascode Operational Amplifier

As discussed in the previous section, the low-pass sigma delta modulator is implemented by SC technique. Hence, the operational amplifier in the integrator determines the operation speed and performance of the modulator.

Since in the SC application the op amp usually does not drive the resistive load, the Operational Transconductance Amplifier (OTA) structures have been employed and optimized for SC sigma–delta modulator applications [8], [37]. In these applications, the gain of the OTA should usually be reasonably high. The larger the opamp gain is the better the modulator performance is. Then the phase margin is chosen to be at least $45^\circ \sim 60^\circ$ in order to provide a good settling behavior. High gain-bandwidth (GBW) product makes it possible to operate the sigma–delta modulator at a high speed, thus allowing wideband operation. Good slew rate (SR) performance is needed to avoid nonlinear settling due to fast changes at the output of the resonators. Low noise and total harmonic distortion (THD) are also required for SC sigma–delta modulator applications.

For reasons given above, a fully differential folded-cascode op amp shown in Fig4.4 [38] has been designed, where VB1, VB2, VB3 and VB4 are generated from a constant-transconductance bias circuit. VCOM is a feedback signal obtained from a common-mode feedback circuit discussed in the following subsection. The input stage is composed by a PMOS differential pair, which has less flicker noise (1/f noise) than its NMOS counterpart since their majority carries are less likely to be trapped. Furthermore in a CMOS p-substrate process, PMOS transistors are isolated substrate-noise by n-well protection. Hence, for low-noise and high-accuracy consideration, we should choose PMOS transistors as input devices. The transistor sizes for the fully-differential folded-cascode operational amplifier are summarized in Table4.2.

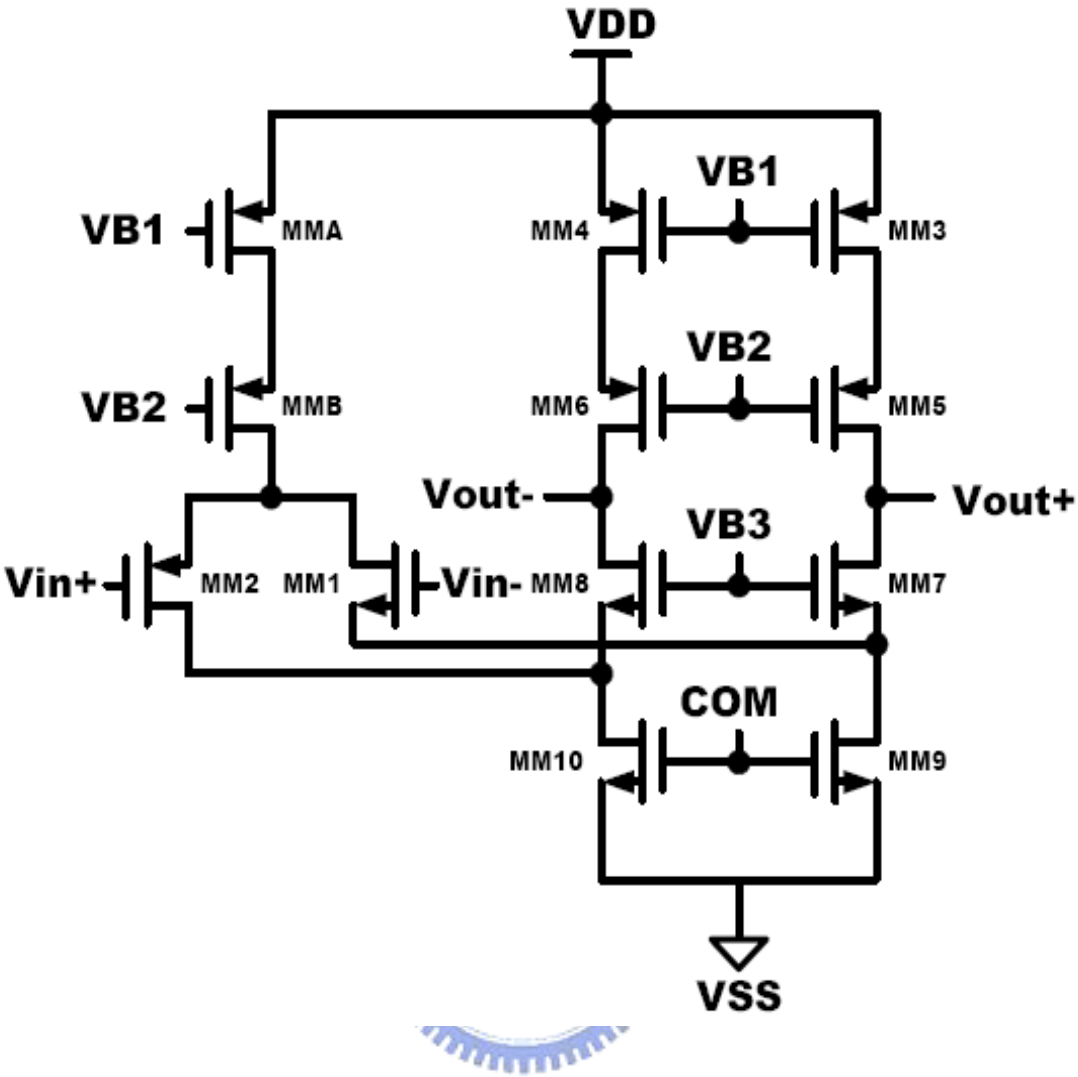


Figure 4.4 The fully Differential Folded Cascode Operational Amplifier

Table 4.2 Transistors Size of the Operational Amplifier

Transistor	Type	W/L （μm）	M
M1, M2	**p-type**	**3 / 0.2**	**108**
MA	**p-type**	**3 / 0.3**	**56**
MB	**p-type**	**3 / 0.3**	**56**
M3, M4	**p-type**	**3 / 0.6**	**132**
M5, M6	**p-type**	**3 / 0.6**	**72**
M7, M8	**n-type**	**3 / 0.6**	**25**
M9, M10	**n-type**	**3 / 0.6**	**20**

When using the fully differential circuit in a feedback application, the applied feedback can determine the differential signals. Unfortunately, the common-mode

voltage is not affected by the applied feedback. It causes the requirement for the common-mode feedback circuit (CMFB). It exists two typical ways to implement CMFB circuits which can be divided into continuous-time type and discrete-time type. Though the speed of continuous-time CMFB is faster than discrete-time type, it may dissipate more power. In order to avoid dissipate additional power, the type of the CMFB we adopted is discrete-time.

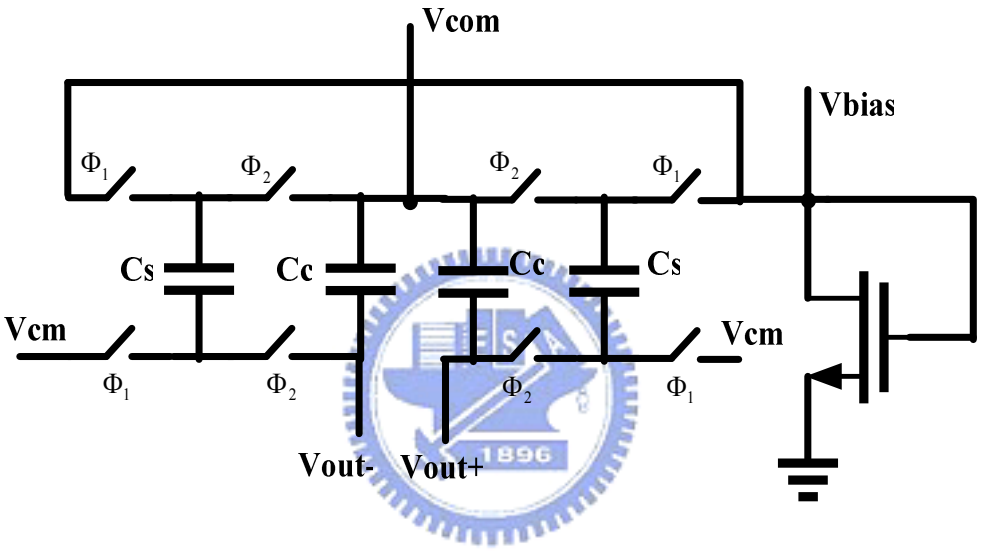


Figure 4.5 Common-mode Feedback Circuit

A switched-capacitor CMFB circuit is shown in Fig. 4.5. Capacitors Cc generate the control voltage for the opamp's bias, CMFB. Cs and the associated switches act as a resistor to lowpass the DC bias voltage, Vbias. Cs might be between one-quarter and one-tenth of Cc depending on lowpass filter property. Phi1 and phi2 are two non-overlapping clocks. Fig. 4.6 shows the HSPICE simulation results of the opamp. Table 4.3 lists the performance of the opamp.

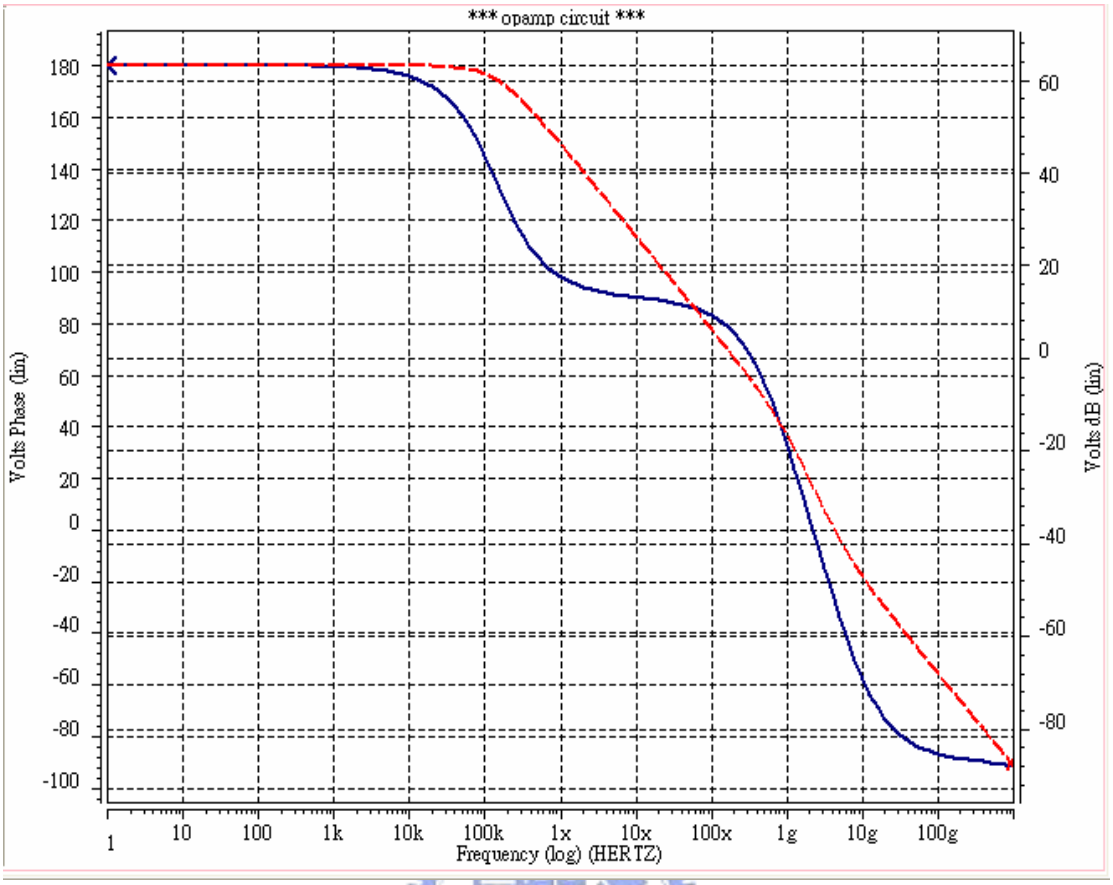


Figure 4.6 Simulation Gain and Frequency Response of the OPamp with 3pF load

Table 4.3 Performance summary of the Operational Amplifier

Process	TSMC .18	ICMR	0.12 ~ 1.46 V
Power Supply	1.8 V	OSR	0.21 ~ 1.69 V
DC Gain	63 dB	Slew Rate	52 / 76 V/us
Phase Margin	76	Cap Load	3p F
Unity Gain BW	200 MHz	Power	1.584 m W

4.1.3 Comparator

The purpose of the comparator in a sigma delta modulator is to quantize the signal in the loop and provide the output of the modulator. There exist non-idealities for comparator, such as hysteresis and offset. Hysteresis is a memory effect causing decisions to be dependent on the pervious state. Offset is a mismatch effect caused by

input transistors. The performance of a sigma delta modulator is relatively insensitive to the above mentioned non-idealities since these impairments are attenuated through noise shaping. A latch comparator shown in Fig.4.7 is used as a one-bit quantizer [39]. It consists of a differential input pair (MP2, MP3), a CMOS latch circuit, and an S-R latch. The CMOS latch is composed of a n-channel flip-flop (MN3, MN4) with a pair of n-channel transfer gates (MN1, MN2) for strobing and an n-channel switch (MN9) for resetting, and a p-channel flip-flop (MP5, MP6) with a pair of p-channel pre-charge transistors (MP4, MP7).When ϕ_2 is high, the differential input are compared and the comparator is in a reset mode. Then when clock ϕ_2 is low and ϕ_1 is high, the comparator enters a latch mode. The comparator output is stored in the output of the NAND-gate latch. The transistors sizes and passive component values of the bias circuit are summarized in Table 4.4.

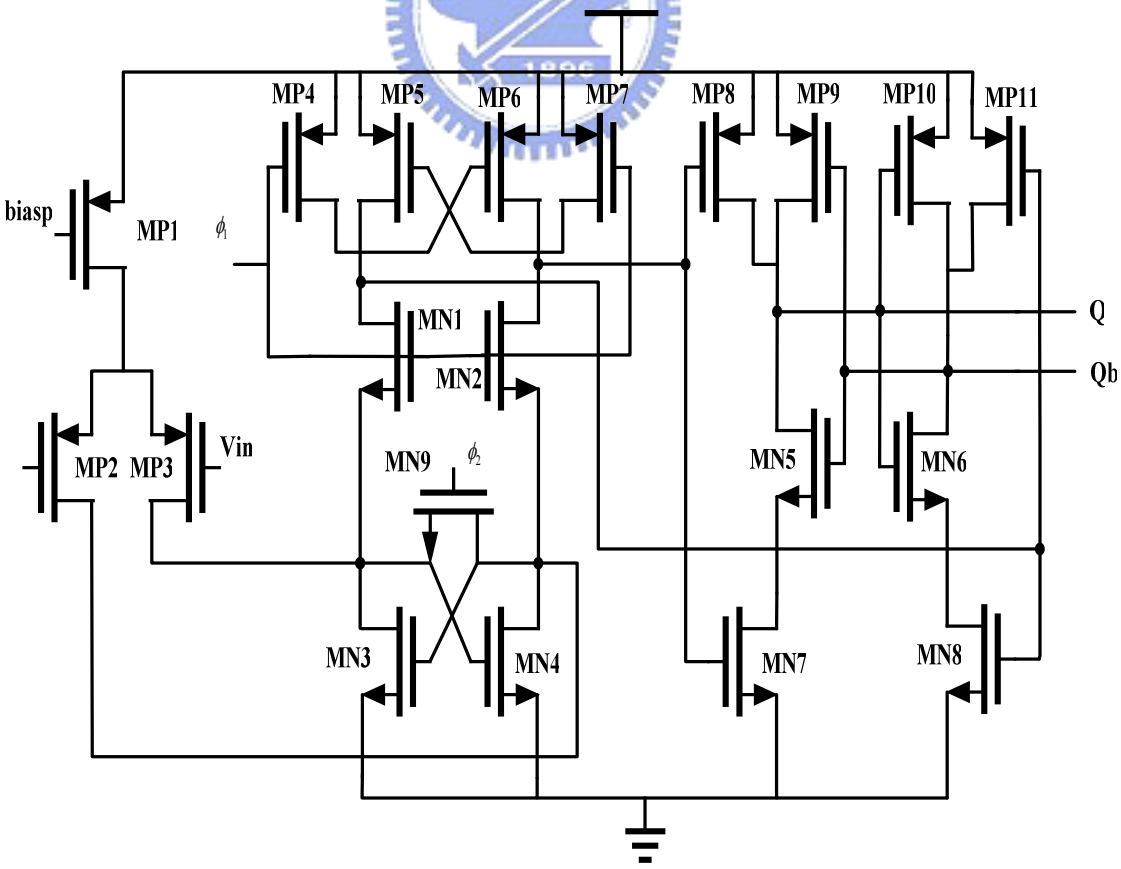


Figure 4.7 The Latch Comparator Circuit

Table 4.4 Transistor Size of the latch comparator

Transistor	Type	W/L （μm）	M
MP1	**p-type**	**5 / 0.3**	**1**
MP2, MP3	**p-type**	**5 / 0.3**	**1**
MP4, MP5	**p-type**	**1 / 0.2**	**1**
MP6, MP7	**p-type**	**2 / 0.2**	**1**
MP8, MP9	**p-type**	**2.5 / 0.2**	**1**
MP10, MP11	**p-type**	**2.5 / 0.2**	**1**
MN1, MN2	**n-type**	**2.5 / 0.2**	**1**
MN3, MN4	**n-type**	**1 / 0.2**	**1**
MN5, MN6	**n-type**	**2 / 0.2**	**1**
MN7, MN8	**n-type**	**2 / 0.2**	**1**
MN9	**n-type**	**1.5 / 0.2**	**1**

4.1.4 Clock Generator

The purpose of the clock generator is to produce non-overlapping clocks in switched-capacitor circuits. These clocks determine when charge transfers occur and they must be non-overlapping in order to guarantee charge is not inadvertently lost. In Fig.4.8, the required clock phases are phi1, phi1a, phi2, phi2a. phi1 and phi2 are non-overlapping clocks and phi1a and phi2a fall slighter advanced than phi1 and phi2 in order to reduce charge injection. Adjusting the W/L ratio of the inverters can properly adjust the non-overlap period. Fig.4.9 shows the timing waveforms of two phase non-overlap clock.

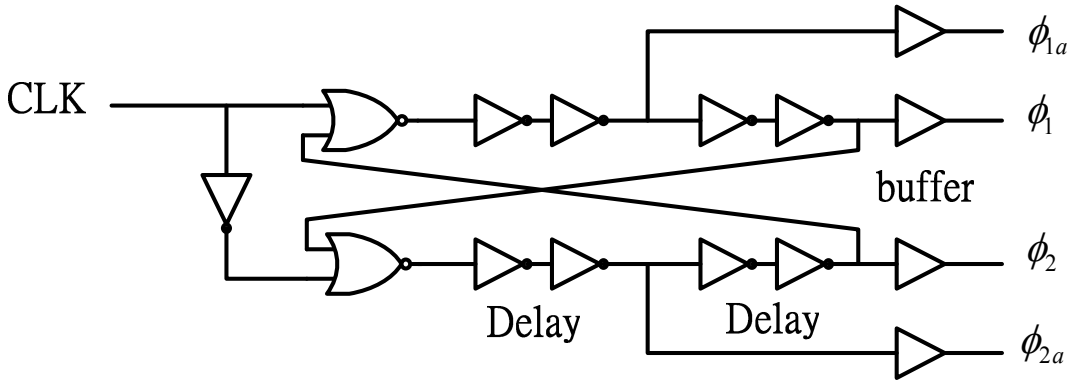


Figure 4.8 Two Phase Non-overlap Clock Generator

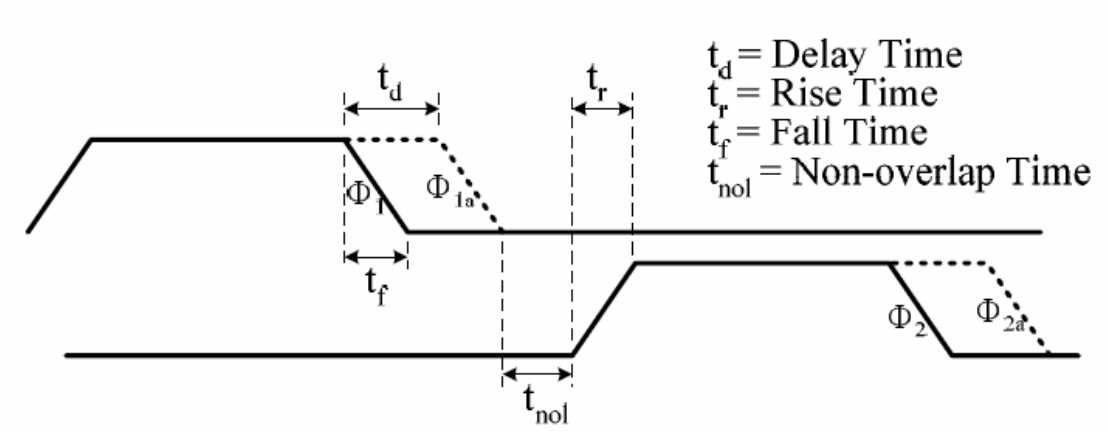


Figure 4.9 Tim waveforms of two phase non-overlap clocks

4.3 Implementation and Simulation Report

4.3.1 Layout Floorplan and Layout Consideration

There are three things we need to take care in the layout of the four path bandpass sigma delta modulator. First, because of the channel mismatch reduce the SNDR, the capacitors symmetry of the four paths is very important. We set the all capacitors in the center of the layout such as figure 4.10, and place the capacitors with symmetry. The placement of the capacitors is shown in figure 4.11 and table 4.5.

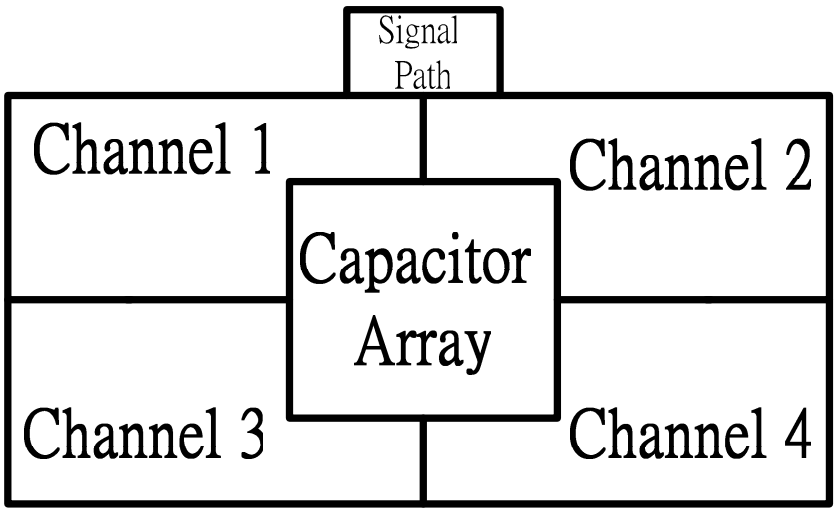


Figure 4.10 The Layout Floorplan of the Four Path Bandpass Modulator_A

Table 4.5 The Capacitor Array Name

Name		Channel	Integrator	Path	Number	
AP	PA	Channel_1	First	Positive	x4	x16
BP	PB	Channel_2	First	Positive	x4	x16
CP	PC	Channel_3	First	Positive	x4	x16
DP	PD	Channel_4	First	Positive	x4	x16
AN	NA	Channel_1	First	Negative	x4	x16
BN	NB	Channel_2	First	Negative	x4	x16
CN	NC	Channel_3	First	Negative	x4	x16
DN	ND	Channel_4	First	Negative	x4	x16
AS	SA	Channel_1	Second	Positive	x4	x8
BS	SB	Channel_2	Second	Positive	x4	x8
CS	SC	Channel_3	Second	Positive	x4	x8
DS	SD	Channel_4	Second	Positive	x4	x8
AQ	QA	Channel_1	Second	Negative	x4	x8
BQ	QB	Channel_2	Second	Negative	x4	x8
CQ	QC	Channel_3	Second	Negative	x4	x8
DQ	QD	Channel_4	Second	Negative	x4	x8
Unit Capacitor : 125 fF Total Capacitor: 256						

The second consideration is that the analog circuits are very sensitive to the noise such as clock and switches, so we need to separate the analog circuits and digital circuits as far as we can. According to this reason, so our layout floorplan for each channel is shown in figure 4.12. Final, the thing we need to take care is the signal and clock skew. To solve the problem, the length of the layout must to be the same at each

channel input and clock. And the complete layout is shown in figure 4.13.

PA	PB	PC	PD	QA	SA	NA	NB	NC	ND	QD	SD	PA	PB	PC	PD
PB	PC	PD	PA	QB	SB	NB	NC	ND	NA	QC	SB	PB	PC	PD	PA
PC	PD	PA	PB	QC	SC	NC	ND	NA	NB	QB	SC	PC	PD	PA	PB
PD	PA	PB	PC	QD	SD	ND	NA	NB	NC	QA	SA	PD	PA	PB	PC
SD	SC	SB	SA	AP	AQ	BP	BQ	CP	CQ	DP	DQ	SA	SB	SC	SD
QD	QC	QB	QA	AS	AN	BS	BN	CS	CN	DS	DN	QA	QB	QC	QD
NA	NB	NC	ND	BP	BQ	CP	CQ	DP	DQ	AP	AQ	NA	NB	NC	ND
NB	NC	ND	NA	BS	BN	CS	CN	DS	DN	AS	AN	NB	NC	ND	NA
NC	ND	NA	NB	CP	CQ	DP	DQ	AP	AQ	BP	BQ	NC	ND	NA	NB
ND	NA	NB	NC	CS	CN	DS	DN	AS	AN	BS	BN	ND	NA	NB	NC
SA	SB	SC	SD	DP	DQ	AP	AQ	BP	BQ	CP	CQ	SD	SC	SB	SA
QA	QB	QC	QD	DS	DN	AS	AN	BS	BN	CS	CN	QD	QC	QB	QA
PA	PB	PC	PD	SD	QD	NA	NB	NC	ND	QA	SA	PA	PB	PC	PD
PB	PC	PD	PA	SB	QC	NB	NC	ND	NA	QB	SB	PB	PC	PD	PA
PC	PD	PA	PB	SC	QB	NC	ND	NA	NB	QC	SC	PC	PD	PA	PB
PD	PA	PB	PC	SA	QA	ND	NA	NB	NC	QD	SD	PD	PA	PB	PC

Figure 4.11 The Placement of the Capacitors

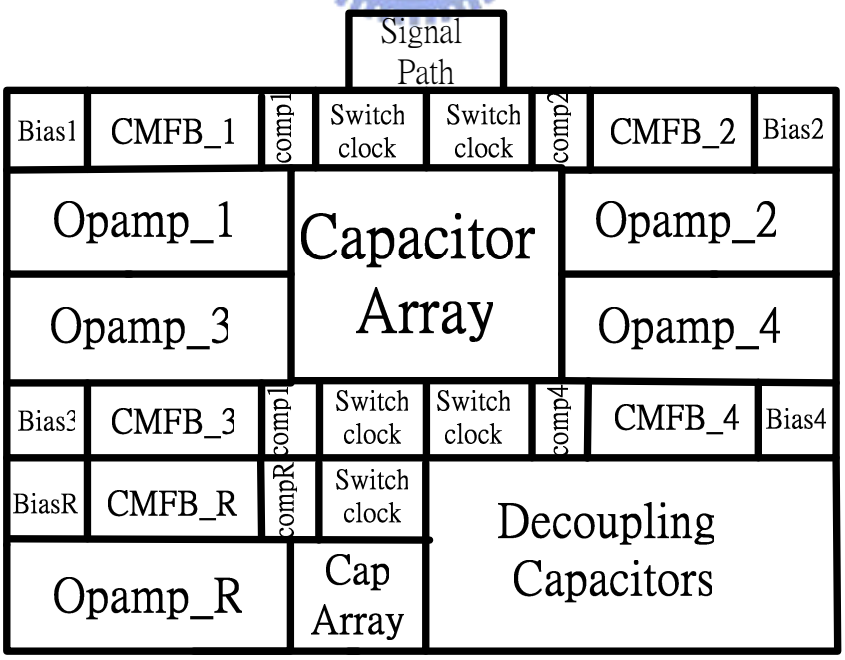


Figure 4.12 The Layout Floorplan of the Four Path Bandpass Modulator_B

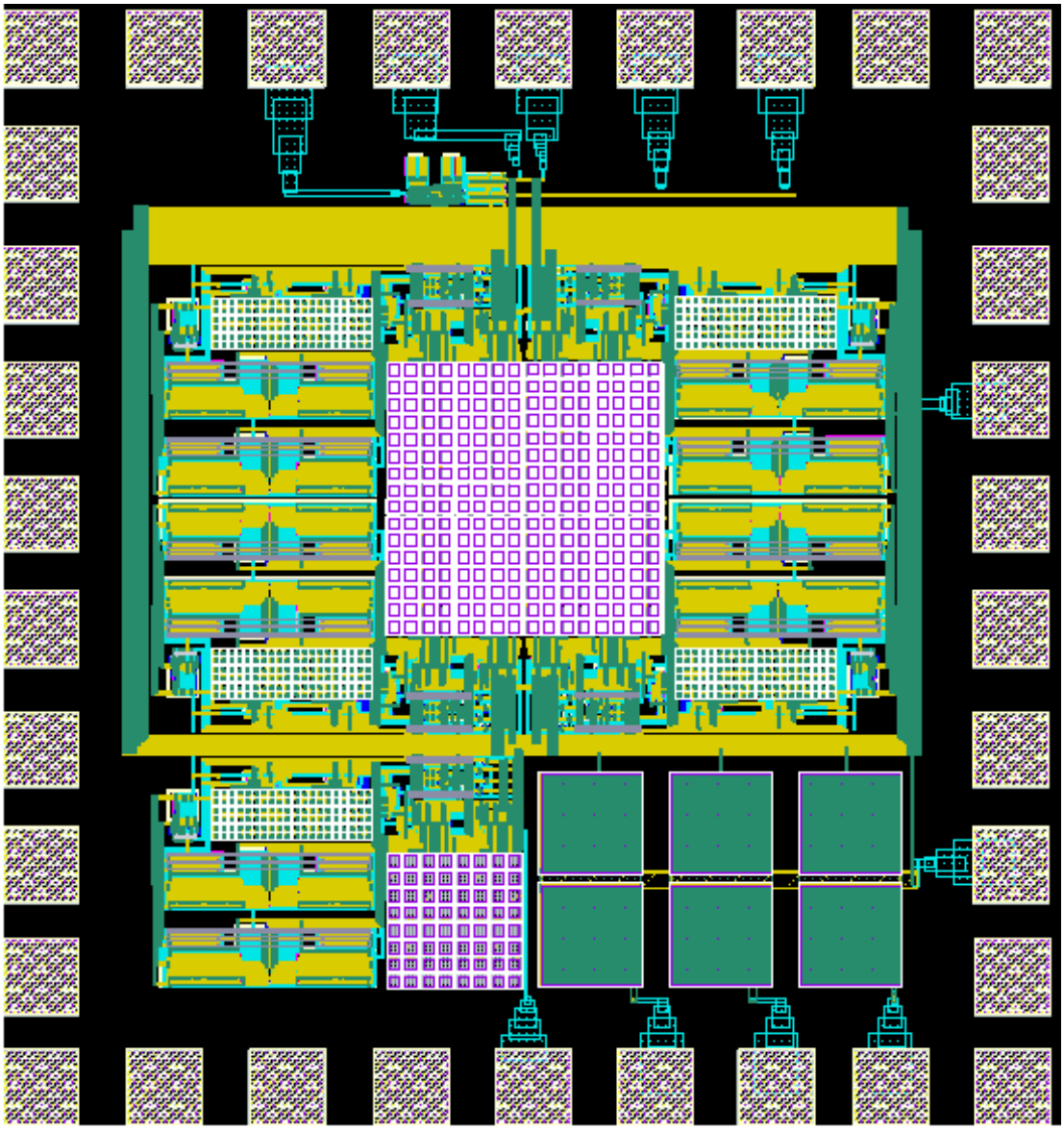


Figure 4.13 The Layout of the Four Path Bandpass Sigma Delta Modulator
The Size of Layout is 0.4*0.6 mm

4.3.2 Simulation Result of the Four Path Bandpass Modulator

Finally, we simulate the performance of the four path bnadpass modulator by giving a 20 MHz sine wave with -6 dB. Using the transient analysis of the Hspice to print the data, then using Matlab to calculate the SNDR with 65536 points FFT. The figure 4.14 show the power spectrum density of the modulator, the Peak SNDR is 69 dB and power consumption is 16 mW with TT corner, 25℃, 1.8V voltage power

supply, simulated by TSMC .18 process. Then the table 4.6 shows the SNDR with five corner and ± 10% power supply variation and the different operational temperature.

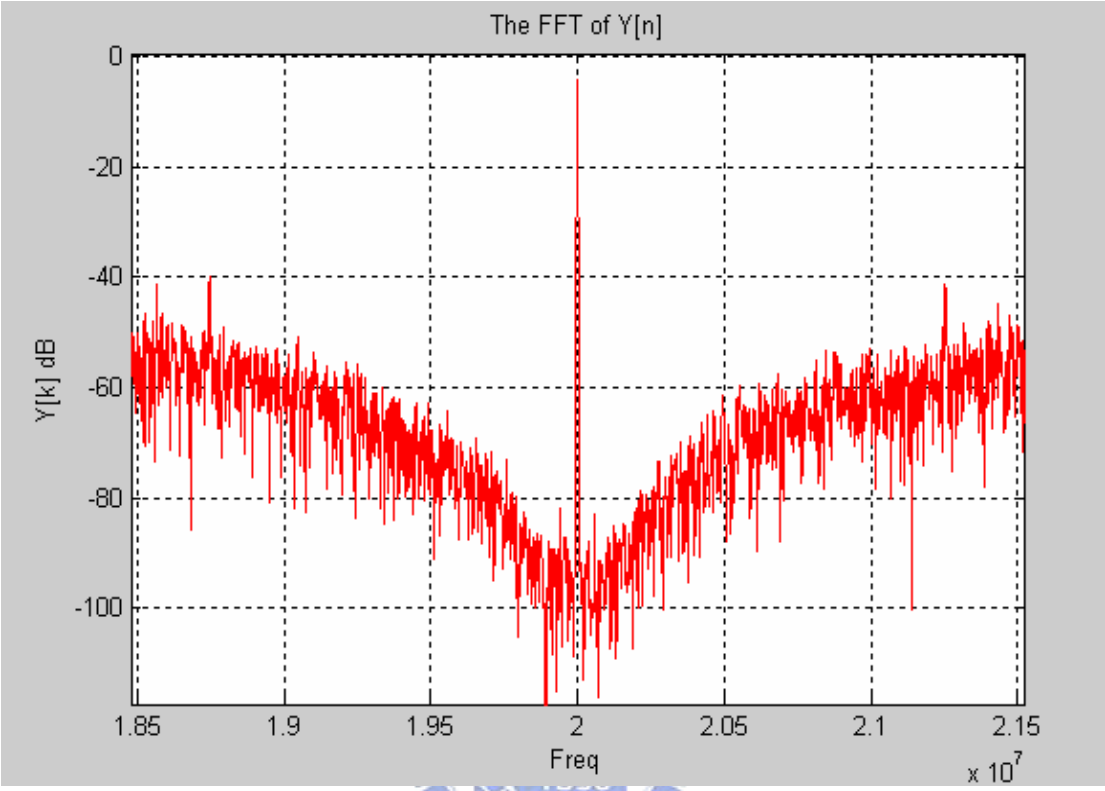


Figure 4.14 TT Corner Power Spectral Density
SNDR = 69.350 dB Power=16.1794 mw

Table 4.6 Summary of the Simulation

項次	TT	FF	FS	SF	SS	1.8V	1.98V	1.62V	25°	75°	125°	SNDR (dB)	Power (mw)
1	●					●			●			69.350	16.1794
2		●				●			●			72.298	16.6928
3			●			●			●			70.626	13.9940
4				●		●			●			71.245	16.1834
5					●	●			●			67.358	16.0255
6	●						●		●			69.820	18.4924
7	●							●	●			66.914	14.0810
8	●					●				●		70.994	18.0591
9	●					●					●	67.112	19.6181

CHAPER 5
CONCLUSIONS

5.1 Summary

According to the section 4.3, we get the specification of the four path bandpass sigma delta A/D converter with bandwidth 200 KHz, sampling frequency 80 MHz, center frequency 20 MHz, peak SNDR 69 dB (ENOB=11.5 bit), and the power just 16mW. It is a low power design for bandpass A/D converter.

For the trend of the wireless communication, it's trade off between performance (such as bandwidth or resolution) and power consumption. We define a parameter FOM [40] to normalize all parameter in the converter. The smaller of the FOM, the better performance is. Finally, we compare the FOM with others shown in Table 5.1. The result of this work is simulated by Hspice, others are measurement results.

$$FOM = \frac{Power}{2^{ENOB} * DOR} \times 10^{12}$$

Table 5.1 Comparison with other works

Reference	DOR	Center / Sample	ENOB	Process	Power	FOM
[3]	0.4 MHz	20 / 40 MHz	11.6 bit	0.6 um	72 mw	5.80
[41]	0.4 MHz	10.7 / 42.8 MHz	9.8 bit	0.8 um	157 mw	44.03
[42]	0.4 MHz	2.5 / 5 MHz	8.7 bit	0.35 um	5.5 mw	3.31
[43]	0.4 MHz	10.7 / 42.8 MHz	10.2 bit	0.35 um	76 mw	16.15
[4]	0.54 MHz	20 / 80 MHz	12 bit	0.35 um	56 mw	2.53
[44]	0.54 MHz	20 / 80 MHz	13 bit	0.35 um	24 mw	0.54
[45]	0.4 MHz	10.7 / 37.05 MHz	12 bit	0.18 um	88 mw	5.37
This work	0.4 MHz	20 / 80 MHz	11.5 bit	0.18 um	16 mw	1.38

In this thesis, we design a time interleaved bandpass sigma delta modulator by using four channels with lowpass sigma delta modulator, and implement by TSMC.18 μm 1P6M CMOS models. And, to avoid gain and offset mismatch produce by each channel, additional reference channel calibrated the errors by off-chip digital calibration technique described in section 3.3. We implement the bnadpass A/D converter by low power technique and we overcome the non-ideal effect by off-chip calibration.

5.2 Future Work

5.2.1 Clock Skew Calibration

For reducing power consumption and design complexity, we using multi-path architecture with four lowpass sigma delta modulators. However, the channel mismatch produce not only offset and gain mismatch, but also phase skew. The digital calibration described in section 3.3 just can calibrate the offset and gain mismatch. In the future, we need to find a way to calibrate the clock skew by a digital calibration technique.

5.2.2 Wide Bandwidth & High Resolution

For the application of wireless communication, low power, wide bandwidth and high resolution are the trend. Base on the time interleaved system with low power, we try to improve the SNDR and increase the bandwidth. First, we can use multi-bit quantizer to increase the SNDR, where each additional bit used in the quantizer will yield a 6 dB improvement in the SNDR. Second, we can use multi-stage to increase NTF order to apply for wide bandwidth, such as IS-95 and WCDMA.

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