Impact of Gate Leakage on Performances of Phase-Locked Loop Circuit in Nanoscale CMOS Technology

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***Abstract*—In the nanoscale CMOS technology, the thin gate oxide causes large gate-tunneling leakage. In this brief, the influence of gate-tunneling leakage in the MOS capacitor (used in the loop filter) on the circuit performance of the phase-locked loop (PLL) in the nanoscale CMOS technology has been investigated and analyzed. The basic PLL with a second-order loop filter is used to observe the impact of gate-tunneling leakage on the performance degradation of the PLL in a 90-nm CMOS process. The MOS capacitors with different oxide thicknesses are used to investigate their impact on the PLL performance. The locked time, static phase error, and jitter of the second-order PLL are found to be degraded by the gate-tunneling leakage of the MOS capacitor used in the loop filter.**

***Index Terms*—Gate-tunneling leakage, loop filter, MOS capacitor, phase-locked loop (PLL).**

I. Introduction

THE REDUCTION of power consumption is very important to the portable microelectronic products. In general, the most common and efficient way to reduce the power consumption in CMOS very large scale integrated circuits is to reduce the power-supply voltage. The standard supply voltage has been scaled down from 2.5 V to 1 V or even lower. The gate-oxide thickness of the MOS transistor becomes thinner to reduce its normal operation voltage (power-supply voltage). The thinner gate-oxide thickness causes large gate-tunneling leakage (gate leakage current) in the nanoscale CMOS technology. In digital circuits, the gate-tunneling leakage results in the high standby power consumption [1]. Therefore, to suppress the impact of gate-tunneling leakage is a very important circuit-design issue in the nanoscale CMOS processes [2], [3].

Recently, clock synthesizers have been widely used in the high-speed data-processing devices such as microprocessors, DSPs, and communication systems. A clock synthesizer generates several sets of clock signals with different frequencies or phases from a reference clock signal. Clock synthesizers are usually implemented with the phase-locked loop (PLL). The demand on low-jitter PLL has become strong to avoid the time-skew problem between the clock and the data signals. To improve the PLL performance, the loop filter is added into the PLL to make it stable and to filter out the noise. The loop filter was usually formed with resistor and capacitor. The capacitor of the loop filter needs a large capacitance to make the PLL stable, which is often realized with MOSFET (MOS capacitor) to reduce the occupied silicon area. However, the MOS capacitor with thinner gate-oxide thickness in the loop filter will also have a larger gate-tunneling leakage in the advanced CMOS technology, which will influence the PLL performance. Recently, some compensation techniques, such as the modified capacitor structure [4], [5], opamp-based compensation [6]–[8], nonopamp-based compensation [9], capacitor multiplier [10]–[12], and digital filter techniques [13], have been developed to compensate the gate-tunneling current of the MOS capacitor used in the loop filter of the PLL. However, the impact from the gate-tunneling leakage of the MOS capacitor in the loop filter on the PLL performance was not clearly investigated and reported in the literature.

In this brief, the influence of the gate-tunneling leakage on the performance of the PLL is investigated and analyzed in a 90-nm CMOS process [14]. The normal operating voltage of the MOSFET device is only 1 V in such a 90-nm CMOS process. The gate-tunneling leakage of the MOS capacitor is simulated by SPICE with BSIM4 model. The BSIM4 model was included with the gate-tunneling leakage [15]–[17]. The MOS capacitors realized with thick or thin gate oxides in the loop filter are used to investigate the impact of gate-tunneling leakage on the PLL performance.

II. PLL

A PLL is basically an oscillator whose frequency is locked onto some frequency component of an input signal. Fig. 1 shows the basic PLL with a second-order low-pass loop filter [18]. PLL is a second-order negative-feedback system similar to the RLC circuit. PLL may be stable or unstable, depending on its phase margin. Stability affects PLL performance, such as settling time, static phase error, and jitter. The capacitor of the loop filter is used to integrate the charge-pump (CP) current and to generate an averaged control voltage, which ensures the proper output frequency for the PLL. The loop filter is also used to generate the pole and zero to adjust the bandwidth and the phase margin of the PLL. In general, the bandwidth of

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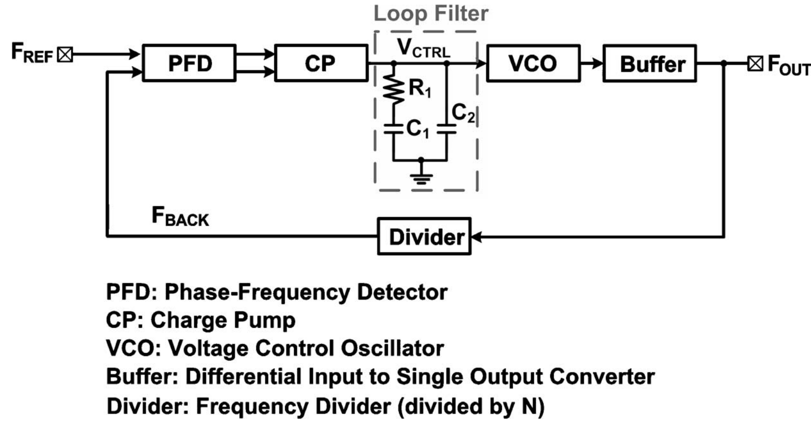

Fig. 1. Basic PLL with a second-order low-pass loop filter.

the PLL is usually designed about only 1/10–1/20 of the input reference frequency for system stability. A PLL consists of a phase/frequency detector (PFD), a CP, a loop filter, a voltage-controlled oscillator (VCO), and a frequency divider (divided by an integer N). The negative feedback synchronizes the internal signal $(F_{\rm BACK})$, which is from the frequency divider, to the external reference signal $(F_{\rm REF})$ by comparing their phases. The PFD develops two output signals, which are proportional to the phase errors. The CP is used to convert the logic states of PFD into analog signals for controlling the VCO, where the frequency of the output signal will be changed by charging or discharging the loop filter. In the loop filter, extra poles and zeros should be introduced to filter out high-frequency signals from the PFD and the CP. The PLL will be "locked" when the phase difference between $F_{\rm REF}$ and $F_{\rm BACK}$ is kept constant. Therefore, the phases of $F_{\rm REF}$ and $F_{\rm BACK}$ are aligned, and the frequency of the output signal $(F_{\rm OUT})$ is N-times of the input reference signal $(F_{\rm REF})$. The loop filter realized with a second-order low-pass filter has been widely used in the PLL design to improve the stability and to suppress the high-frequency noise. The on-chip capacitor in the second-order loop filter can be realized by PMOS and NMOS transistors, respectively, as shown in Fig. 2(a) and (b). In general, the filter capacitor C_1 has a typical range from 50 to 400 pF. The capacitor C_2 smoothes the large IR ripple on the signal of $V_{\rm CTRL}$. The resistor R_1 provides the instantaneous phase correction without affecting the averaged frequency of the VCO.

The capacitor of the loop filter needs a large capacitance to make the PLL stable, but it also has a large gate-tunneling leakage through the MOS capacitor in the loop filter to degrade the PLL performance in the nanoscale CMOS technology. The gate-tunneling leakage of the MOSFET has been modeled as [15]–[17]

$$J_g = A\left[\frac{T_{\rm oxref}}{t_{\rm ox}}\right]^{\rm ntox}\frac{V_g V_{\rm aux}}{T_{\rm ox}^2}e^{-B(\alpha-\beta|V_{\rm ox}|)(1+\gamma|V_{\rm ox}|)t_{\rm ox}} \quad (1)$$

where $A = q^2/8\pi h\phi_B$, $B = 8\pi\sqrt{2qm_{\rm ox}}\phi_B^{3/2}/3h$, $m_{\rm ox}$ is the effective carrier mass in oxide, ϕ_B is the tunneling barrier height, $t_{\rm ox}$ is the oxide thickness, $T_{\rm oxref}$ is the reference oxide thickness, and $V_{\rm aux}$ is an auxiliary function which approximates the density of the tunneling carriers. α, β, and γ are the physical parameters defined by device technology. V_g is the gate voltage of the MOSFET device, ntox is a fitting parameter, and $V_{\rm ox}$ is the voltage across the oxide of the MOSFET device.

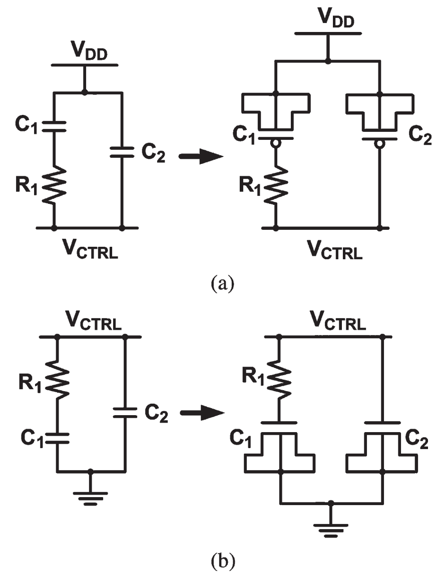

Fig. 2. Second-order loop filter realized with (a) PMOS and (b) NMOS capacitors.

The MOS capacitor of the loop filter is operated in the strong-inversion region in the PLL. In (1), the gate-tunneling-leakage density strongly depends on the oxide thickness, device size, and voltage across the oxide of the MOSFET. Fig. 3 shows the dependence of the gate-tunneling leakage on the NMOS and PMOS capacitors with different threshold voltages under different gate voltages in a 90-nm 1-V CMOS technology. The normal operating voltage of the MOSFET device is only 1 V, and the typical oxide thickness of the MOSFET device is 2.33 nm in the given 90-nm CMOS process. The NMOS capacitor has larger gate-tunneling leakage than that of the PMOS capacitor. The electron conduction-band (ECB) tunneling is the dominant component of the gate-tunneling leakage in the NMOS device, whereas it is the hole valance-band (HVB) tunneling in the PMOS device. Because the barrier height for HVB (4.5 eV) is significantly greater than that of ECB (3.1 eV), this results in the much lower gate-tunneling leakage in the PMOS device [15]. The summary of gate-tunneling leakage per unit area of the

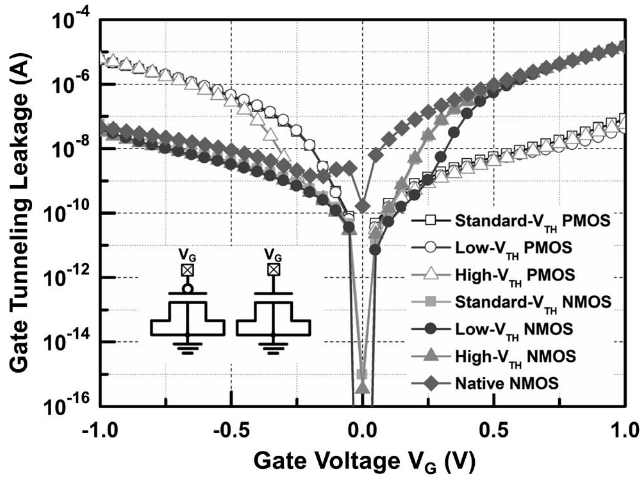

Fig. 3. Simulated gate-tunneling leakage on the different threshold-voltage NMOS and PMOS capacitors under the different gate voltages in a 90-nm 1-V CMOS technology.

TABLE I
GATE-TUNNELING LEAKAGE PER UNIT AREA OF NMOS AND PMOS CAPACITORS WITH DIFFERENT THRESHOLD VOLTAGES IN A 90-NM CMOS PROCESS

MOS Capacitor			
NMOS		PMOS	
Structure	Gate Tunneling Leakage	Structure	Gate Tunneling Leakage
Standard-V_{TH}	1.11 nA/μm^2	Standard-V_{TH}	0.654 nA/μm^2
High-V_{TH}	0.764 nA/μm^2	High-V_{TH}	0.401 nA/μm^2
Low-V_{TH}	1.161 nA/μm^2	Low-V_{TH}	0.701 nA/μm^2
Native NMOS	1.571 nA/μm^2		

NMOS and PMOS capacitors with different threshold voltages in the given 90-nm CMOS process is shown in Table I. The gate voltage V_G is set to 0.492 V in the loop filter of the PLL in this study. The thin-oxide NMOS device with the low threshold voltage has larger gate-tunneling leakage than the other devices in the same 90-nm CMOS process.

III. EFFECT OF GATE-TUNNELING LEAKAGE IN MOS CAPACITOR ON THE PERFORMANCE OF THE PLL CIRCUIT

The static phase error, settling time, and jitter are the key factors in the PLL design and application, which will cause the time-skew problem to induce system malfunction. In this work, the PLL with a second-order low-pass loop filter is used to investigate the impact from gate-tunneling leakage of the MOS capacitor on the PLL performance. The design parameters and simulated results of the second-order PLL in a 90-nm CMOS process are shown in Table II. To compare the impact of gate-tunneling leakage in the MOS capacitor on the PLL performance, the loop filter (C_1, C_2, and R_1) in the second-order PLL is simulated with ideal capacitor and resistor in Table II as a reference. The C_1 and C_2 capacitors of the low-pass loop filter in the PLL, as shown in Fig. 2, are replaced by the MOS capacitors with different oxide thickness to investigate the impact of gate-tunneling leakage on the PLL performance. The capacitances of the different MOS capacitors C_1 and C_2 are 85.172 and 8.782 pF, respectively, under the gate voltage of

TABLE II
DESIGN PARAMETERS AND SIMULATED RESULTS OF THE SECOND-ORDER PLL IN A 90-NM CMOS PROCESS

Design Parameters of PLL in a Standard 90-nm CMOS Process			
Operating Voltage	1 V	C1	85.172 pF
Input Frequency	25 MHz	C2	8.782 pF
Output Frequency	200 MHz	R1	3.2168 kΩ
Charge Pump Current	50 μA	Phase Margin	57°
Divided by N	8	Loop Bandwidth	1.8 MHz
VCO Gain	625 MHz	Damping Factor	≈ 1.1
Simulated Results of PLL in a Standard 90-nm CMOS Process			
Locked Time	1.3 μsec	Output Jitter at 200 MHz	2.7 psec
Static Phase Error	45 psec	Total Power Consumption	4.8647 mW

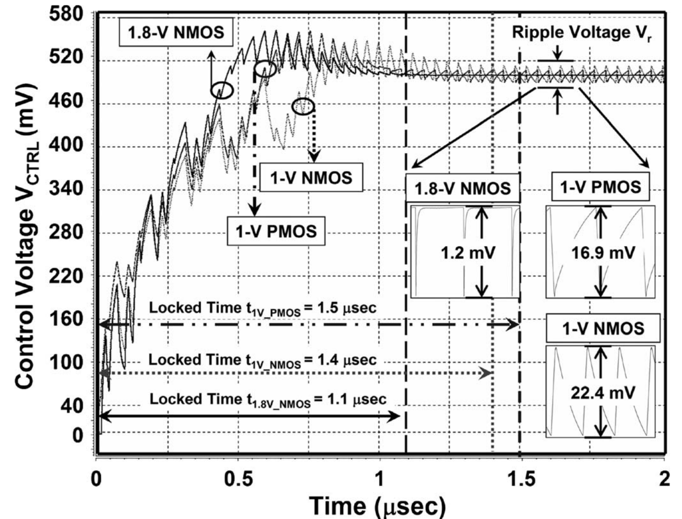

Fig. 4. Simulated transition waveforms of control voltage (V_{CTRL}) to find the locked time under the MOS capacitors with different oxide thickness in the second-order PLL.

0.492 V. Fig. 4 shows the simulated transition waveforms of the control voltage (V_{CTRL}) to find the locked time under the MOS capacitors with different oxide thickness in the second-order PLL. The PLL design with thin-oxide MOS capacitors (1-V NMOS and PMOS) has longer locked time and larger ripple voltage V_r than that with thick-oxide MOS capacitor (1.8-V NMOS). The simulated static phase error Δt under the MOS capacitors with different oxide thickness in the second-order PLL is shown in Fig. 5. The thin-oxide MOS capacitors (1-V NMOS and PMOS) cause larger static phase error Δt than that with thick-oxide MOS capacitor (1.8-V NMOS) in the second-order PLL. The simulated voltage waveforms to find the jitter under the MOS capacitors with different oxide thicknesses in the second-order PLL is shown in Fig. 6. The thin-oxide MOS capacitors (1-V NMOS and PMOS) cause larger jitter than that with thick-oxide MOS capacitor (1.8-V NMOS) in the second-order PLL, due to the large ripple voltage at the V_{CTRL} node. The dependence of the different input-signal frequencies on the jitter and ripple voltage under the MOS capacitor with different oxide thickness in the second-order PLL is shown in Fig. 7.

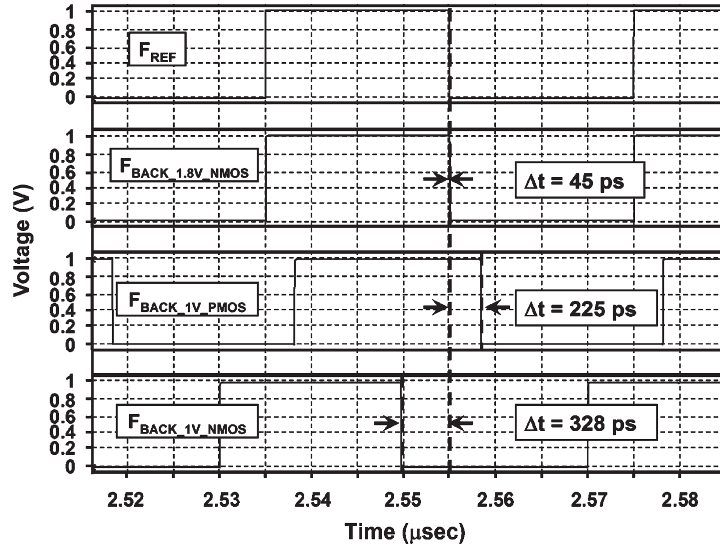

Fig. 5. Simulated static phase error Δt under the MOS capacitors with different oxide thickness in the second-order PLL.

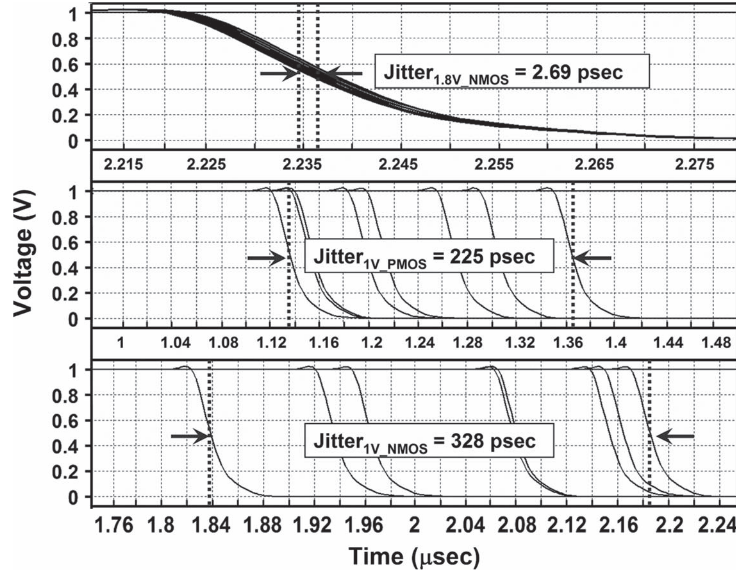

Fig. 6. Simulated voltage waveforms to find the jitter under the MOS capacitors with different oxide thicknesses in the second-order PLL.

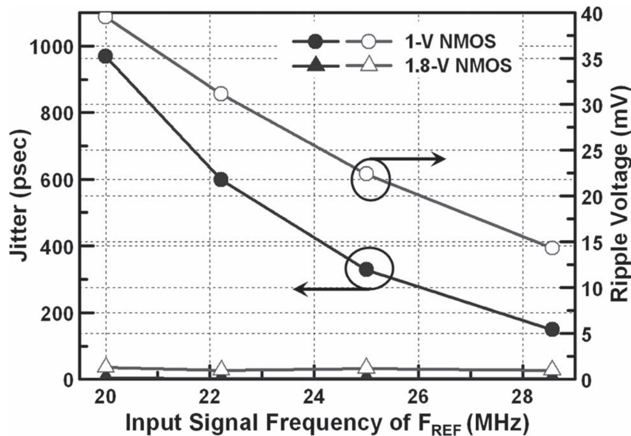

Fig. 7. Dependence of different input-signal frequencies on the jitter and ripple voltage under the MOS capacitors with different oxide thickness in the second-order PLL.

The higher input-signal frequency F_{REF} has a smaller jitter in the second-order PLL due to the gate-tunneling leakage.

IV. Discussion

In general, the capacitance of the MOS capacitor C_1 is larger than that of the MOS capacitor C_2 in the second-order PLL design, as shown in Fig. 1. Because the capacitance of the MOS capacitor is proportional to the device size and oxide thickness, the gate-tunneling leakage of the MOS capacitor C_1 is larger than that of the capacitor C_2. The circuit schematic of Fig. 1 can be simplified to that of Fig. 8, where the current I_{CP} is the CP current, and the current $I_{\mathrm{GTL,LF}}$ is the total gate-tunneling leakage of the MOS capacitors C_1 and C_2. The CP current I_{CP}, which is controlled by the phase difference between F_{REF} and F_{BACK} signals through the PFD, is working as a constant current source. The effective charge current I_C through

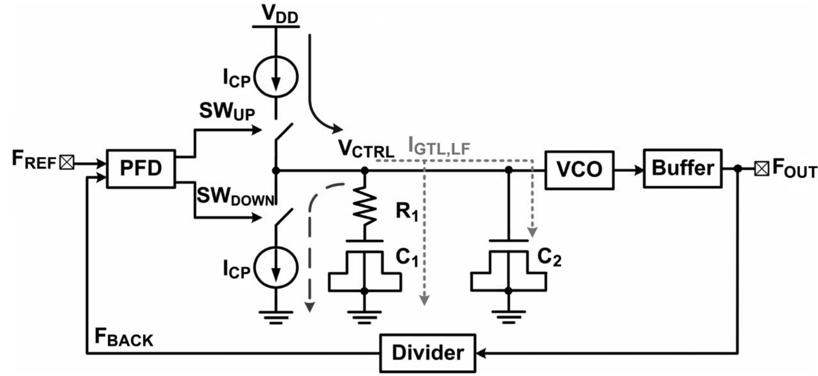

Fig. 8. Schematic of the second-order PLL including the gate-tunneling leakage in the loop filter.

MOS capacitors C_1 and C_2 in the second-order PLL can be expressed as

$$I_C = I_{\rm CP} - I_{\rm GTL,LF}. \quad (2)$$

To reach the locked state (phase difference between $F_{\rm REF}$ and $F_{\rm BACK}$ is constant), the second-order PLL needs a setting time for system stability. The gate-tunneling leakage reduces the effective charge current I_C, therefore, the PLL needs more charge time to make the control voltage $V_{\rm CTRL}$ into the static state for controlling the VCO oscillation at the correct frequency. The locked time of the second-order PLL is increased due to the gate-tunneling leakage of the MOS capacitor.

In the locked state, the dependence of gate-tunneling leakage on the ripple voltage V_r in the second-order PLL can be written as

$$\Delta V_r = \frac{I_{\rm GTL,LF} \times T_{\rm REF}}{C_1} \quad (3)$$

where $T_{\rm REF}$ is the period of input signal $F_{\rm REF}$. The amount of ripple voltage V_r is proportional to the gate-tunneling leakage. The large gate-tunneling current of the MOS capacitor will cause a large ripple voltage at the $V_{\rm CTRL}$ node in the second-order PLL. In (3), the ripple voltage V_r is also proportional to the period of input signal $F_{\rm REF}$, Therefore, the higher input-signal frequency causes a smaller ripple voltage in the second-order PLL, as shown in Fig. 7. According to (3), the dependence of gate-tunneling leakage on the jitter of the second-order PLL can be expressed as

$$\text{Jitter} \propto \Delta V_r \times K_{\rm VCO} = \frac{I_{\rm GTL,LF} \times K_{\rm VCO}}{f_{\rm REF} \times C_1} \quad (4)$$

where the $K_{\rm VCO}$ (Hz/V) is the gain of the VCO, and $f_{\rm REF}$ is the input frequency of input signal $F_{\rm REF}$. The large ripple voltage ΔV_r and the low input frequency of $F_{\rm REF}$ cause large jitter in the second-order PLL. Therefore, the gate-tunneling leakage of the MOS capacitor in the loop filter has serious impact on the PLL performance. To reduce the impact from the gate-tunneling leakage of the MOS capacitor in the loop filter on the PLL performance, the PLL should be designed with small $K_{\rm VCO}$ gain in the VCO.

When the PLL is operating in the locked state, the feedback clock signal $(F_{\rm BACK})$ compares with the reference clock signal $(F_{\rm REF})$ via the CP to generate loop voltage $(V_{\rm CTRL})$ for controlling the VCO frequency. The CP has always supplied the current pulses to compensate the gate-tunneling leakage of the MOS capacitor. The dependence of gate-tunneling leakage on the static phase error Δt of the second-order PLL can be expressed as

$$\Delta t \propto \frac{I_{\rm GTL,TL}}{I_{\rm CP}} \times T_{\rm REF}. \quad (5)$$

To reduce the static phase error in the second-order PLL, the CP should be designed with a large constant current.

The different layout structures will also influence the gate-tunneling leakage of the MOS transistor in the nanoscale CMOS process. When the equivalent gate-oxide resistance is also reduced due to the oxide thickness scaling down, the gate resistor (poly resistance) may lead to an effective gate-bias drop resulting in the decrease of drain current and tunneling leakage. As a result, the threshold voltage of a thin-oxide device is apparently increased by the voltage drop on gate poly resistor and fluctuates due to the gate-tunneling leakage [19]. Because the gate-tunneling leakage of the MOSFET is proportional to the voltage drop through the gate oxide, the MOS capacitor should be drawn in the layout with fewer gate fingers to reduce the negative impact of gate-tunneling leakage on the PLL performance.

V. Conclusion

The influence from the gate-tunneling leakage of the MOS capacitor on the circuit performance in the second-order PLL has been analyzed and investigated in a 90-nm 1-V CMOS process. The locked time, static phase error, and jitter of the second-order PLL were degraded by the gate-tunneling leakage of the MOS capacitor in the loop filter. The higher input-signal frequency can be used to reduce the negative impact of gate-tunneling leakage on the performance of the second-order PLL in nanoscale CMOS technology. The PMOS device with high threshold voltage and thick oxide thickness can be used to realize the MOS capacitor in the loop filter for achieving the second-order PLL with low-jitter performance.

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