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Japanese Journal of Applied Physics 48 (2009) 086001 **REGULAR PAPER**

Effects of Plasma Damage on Metal–Insulator–Metal Capacitors and Transistors for Advanced Mixed-Signal/Radio-Frequency Metal–Oxide–Semiconductor Field-Effect Transistor Technology

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The effects of damage on mixed-signal (MS)/radio-frequency (RF) circuits integrated with metal–insulator–metal (MIM) capacitors and advanced metal–oxide–semiconductor field-effect transistors (MOSFETs) are studied in this work. The impact of damage on an MIM oxide is evaluated by connecting its capacitor top metal (CTM) to an upper-level metal with a large antenna ratio (AR_{CTM}) used in an actual CTM circuit connected to an interconnect. In addition to the dielectric degradation of a transistor, we also investigate the damage-enhanced negative bias temperature instability (NBTI) degradation of a transistor with its gate electrode connected to an MIM capacitor with a large AR_{CTM} for various gate oxide thicknesses. A model is proposed to explain the experimentally observed dependence of NBTI degradation on AR_{CTM} and accurately simulate failure distributions in the presence of plasma damage. © 2009 The Japan Society of Applied Physics

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1. Introduction

The integration of mixed-signal (MS)/radio-frequency (RF) components with capacitors in logic metal–oxide–semiconductor field-effect transistors (MOSFETs) requires a high quality factor and reliable performance.[1)] Plasma-processing-induced damage (P^2ID) is well known to degrade both dielectric and transistor reliability.[2)] In silicon wafer manufacturing, many plasma-processing steps, such as polycrystalline silicon (poly-Si) etching,[3)] high-density-plasma chemical vapor deposition (HDP-CVD),[4)] metal interconnect etching,[5)] and photoresist ashing,[6)] are widely employed. During plasma processing, a local imbalance of surface voltage potential across the oxide results in current flowing through the capacitor top metal (CTM) or gate electrode. The plasma damage current I_{plasma} can potentially break the Si–O bonds with increasing oxide leakage current and decreasing breakdown voltage V_{BD}. Moreover, trap states in bulk SiO_2 or a SiO_2/Si substrate interface cause both threshold voltage instability and mobility degradation. Although subsequent annealing can eliminate the effects of P^2ID, weak points in the bulk oxide and the SiO_2/Si substrate interface resulting from P^2ID can further degrade the transistor reliability after reliability stressing. Although the P^2ID-enhanced degradation in reliability of a single MOSFET[7)] or a stand-alone metal–insulator–metal (MIM) capacitor[8)] has been previously studied, there have been no studies on this issue for circuits comprising both MOSFETs and MIM capacitors.

In this study, both the damage mechanism and degradation models for MIM oxides and transistor gate oxides are proposed. In addition to the dependence of plasma-induced degradation of floating-MIM capacitors, the effects of damage on an MIM capacitor with its capacitor bottom metal (CBM) connected to the substrate directly or through transistors (i.e., a tied-down MIM) were also investigated. More importantly, we also present, for the first time, the effect of damage on a transistor with its gate electrode connected to the CBM of an MIM capacitor (i.e., a tied-up transistor). In these structures, we demonstrate that the impact of damage on transistor reliability strongly depends on gate oxide thickness, and we propose a power-law dependence for the degradation of reliability of a tied-up transistor on the antenna ratio of the CTM (AR_{CTM}) of the MIM capacitor. Our models can accurately predict the failure distributions of negative bias temperature instability (NBTI) degradation due to P^2ID.

2. Experimental Procedure

2.1 Wafer processing

Advanced MOSFETs with gate oxide thicknesses ranging between 1.5 and 3.5 nm were investigated in this study. Many process steps including shallow trench isolation (STI), and the formation of a triple well, dual polygate, shallow junction, and Co salicide were integrated for high-performance circuit operation. In addition, to investigate a generic logic MOSFET process, MIM capacitors were constructed using advanced low-k/Cu technology. In this study, MIM capacitors were usually formed between two upper metal layers with an improved Q factor through reduced parasitic resistance. A lower-level metal (Mn-1) layer was used as a CBM, as shown in Fig. 1(a), and an oxide layer of approximately 30 nm thickness was subsequently deposited by plasma-enhanced chemical vapor deposition (PECVD) as an insulator. It was followed by the deposition and patterning of a thin TiN layer to serve as the CTM, which was then connected to an upper-level metal (Mn) through via holes. In contrast, for the tied-down MIM capacitors, the CBM was connected to either the active-area region (i.e., the substrate) or the transistor gate through a lower-level metal layer and a contact process, as shown in Figs. 1(b) and 1(c).

2.2 Test structure design

Figure 1(a) shows the test structure of the floating-MIM capacitor. During the plasma process, the plasma ions attacked the top area of the upper-level metal (Mn) while the dielectric film was deposited above the Mn layer by HDP-CVD system. The CTM, connected to the large antenna area of the Mn layer, was designed to investigate the effect of charging damage on the MIM capacitor and transistor yield. The antenna ratio was defined as

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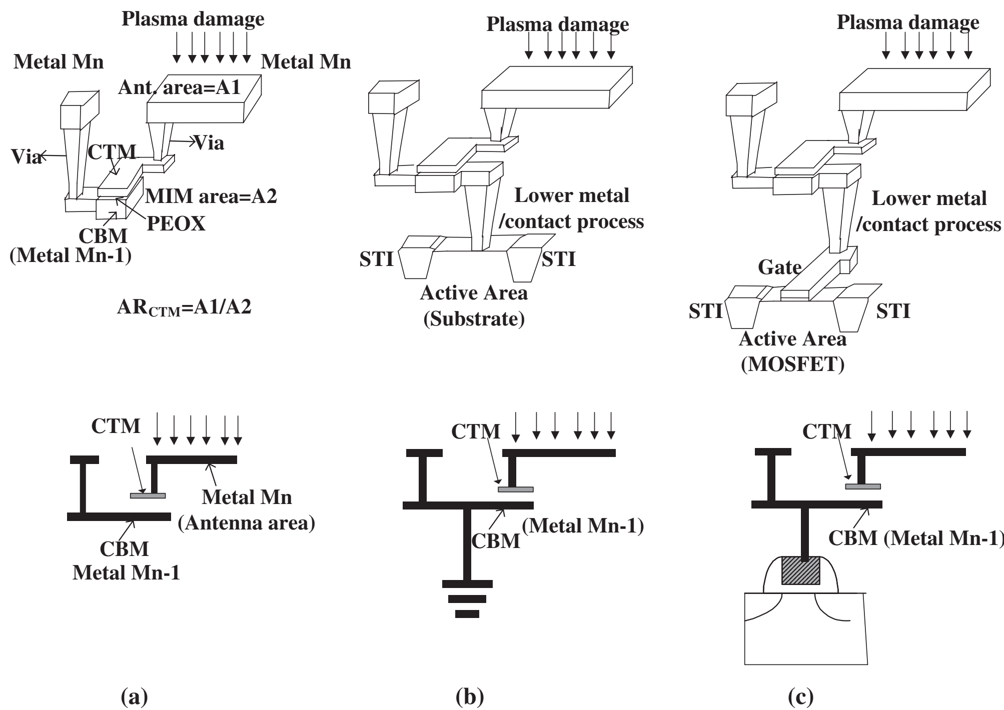

Fig. 1. Schematic diagram of (a) floating-MIM capacitor, (b) tied-down MIM capacitor with CBM connected to substrate, and (c) tied-down MIM capacitor with CBM connected to transistor gate.

$$\mathrm{AR_{CTM}} = \frac{\text{Area of upper metal layer connected to the CTM}}{\text{Area of MIM capacitor}}. \tag{1}$$

Here, the MIM capacitor area is $5 \times 5\,\mu\mathrm{m}^2$ and values of $\mathrm{AR_{CTM}}$ of $100\times$, $250\times$, and $1000\times$ are used for detecting various charging effects. The test structures of tied-down MIM capacitors are shown in Figs. 1(b) and 1(c). In contrast to the test structures of floating-MIM capacitors, the CBM of tied-down MIM capacitors was connected directly to the active area, as shown in Fig. 1(b), or to a transistor, as shown in Fig. 1(c). In the case of the tied-down MIM capacitors connected to the transistor gate electrode, as shown in Fig. 1(c), the transistor size was designed to have a unit area of $1\,\mu\mathrm{m}^2$. The transistor length and width were 0.2 and $5\,\mu$m, respectively.

2.3 Electrical measurements

The failure of the MIM capacitor was defined as a one-order increase in the leakage current compared with that of the undamaged MIM capacitor. The leakage current of the MIM capacitors was measured under an electric field of approximately 3 MV/cm. The gate oxide breakdown voltage V_{BD} was measured by a voltage ramp method. The failure ratio of the MIM capacitor or transistor gate oxide was defined as the fraction of failed samples out of the total measured samples. In addition, NBTI measurements were performed on p-channel MOSFETs (PMOSFETs) under electric fields of 8–10 MV/cm at 125 °C using an Agilent 4156 system. The NBTI lifetime was defined as the time until the transistor exhibited a 50 mV shift in threshold voltage.

3. Results and Discussion

3.1 Oxide degradation

3.1.1 Oxide damage model

Oxide breakdown was defined as the moment when a cluster of disconnected Si–O bonds from the $\mathrm{SiO_2/Si}$ substrate interface (i.e., the bottom plate) reaches the poly-Si/$\mathrm{SiO_2}$ interface (i.e., the top plate). It is widely believed that defects existing in bulk oxides usually produce weak spots or trap centers that can trap charges. During plasma processing, the damage current flowing through the dielectric can be simulated with an equivalent voltage stress V_{st} or electric field stress E_{st}, and is able to generate a large number of defects at the interface and bulk oxide region.[9] In addition, $\mathrm{P^2ID}$ enhances the degradation of the dielectric owing to the extra current paths generated by the equivalent voltage stress V_{st} across the oxide during $\mathrm{P^2ID}$. To simplify the analysis of the MIM capacitors and transistors damaged during wafer fabrication, the dependence of the effect of damage on $\mathrm{AR_{CTM}}$ is introduced in terms of the damage current I_{plasma} to simulate the damage characterization. By assuming a fixed $\mathrm{AR_{CTM}}$ for a given plasma process, I_{plasma} can be approximated as a constant current source of "damage current" passing through the oxide layer. With increasing $\mathrm{AR_{CTM}}$, the total damage current passing through the oxide layer increases proportionally to the $\mathrm{AR_{CTM}}$. Figure 2 shows the current–voltage curves for different oxide thicknesses and values of $\mathrm{AR_{CTM}}$. I_{plasma} can be approximated as a constant current for a given plasma process,[10] and can be written as $I_{\mathrm{plasma}} = k \cdot \mathrm{AR_{CTM}}$, where k is the plasma current when $\mathrm{AR_{CTM}} = 1$ (i.e., an antenna ratio of unity). During the plasma processing, oxide breakdown occurs at a plasma current density of approximately $2\text{–}20\,\mathrm{A/cm^2}$ according to

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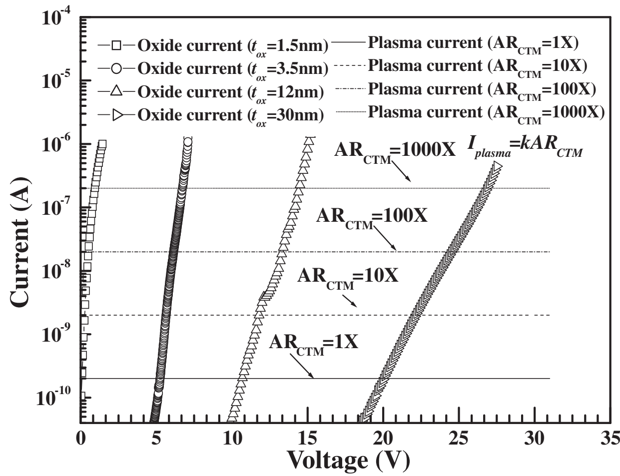

Fig. 2. Characteristics of measured oxide current and simulated damage current with respect to voltage. The oxide current curves were measured for gate oxide thicknesses of 1.5, 3.5, 12, and 30 nm. The damage current curves were simulated for antenna ratios AR_{CTM} of 1×, 10×, 100×, and 1000×.

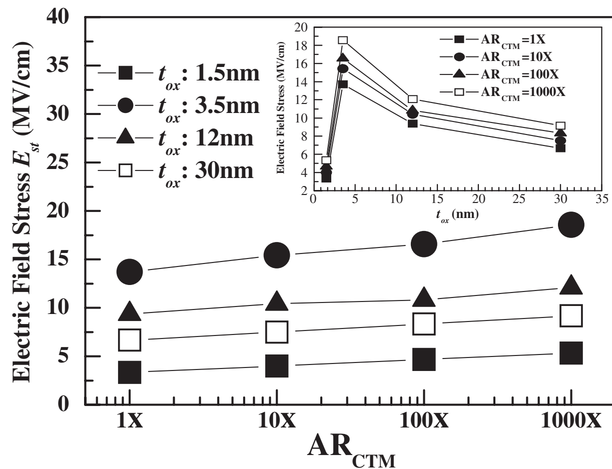

Fig. 3. Estimated electric field stress (E_{st}) during plasma processing as a function of AR_{CTM} for different oxide thicknesses. The inset shows E_{st} as a function of oxide thickness for different AR_{CTM}.

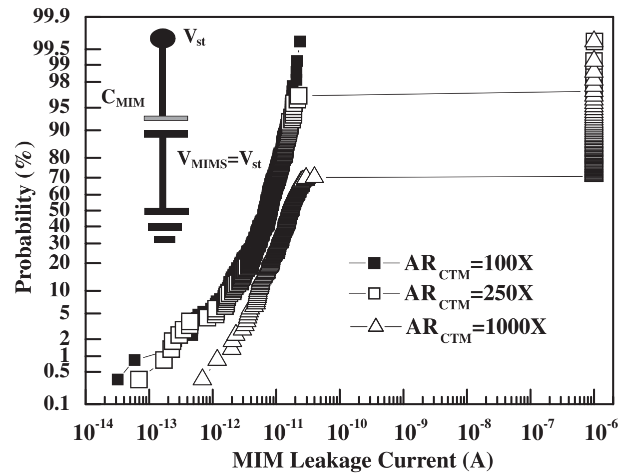

Fig. 4. Failure probability of leakage current for MIM capacitor connected directly to active area for various AR_{CTM}. The inset shows a schematic of the capacitor configuration.

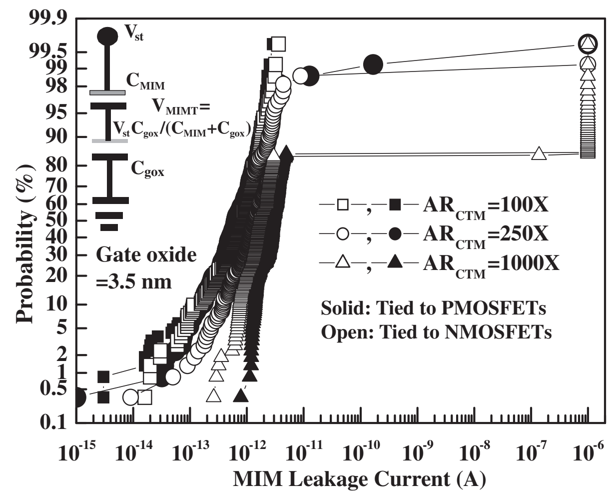

Fig. 5. Failure probability of leakage current for MIM capacitor connected to transistor gate for various AR_{CTM}. The inset shows a schematic of the capacitor configuration.

a previous study.[11] Thus, the value of k can be assumed to be 2×10^{-10} A in our experiments with a transistor size of 1 μm^2 (i.e., for damaged structures with $AR_{CTM} = 100\times$, $I_{plasma} = 2$ A/cm^2 and with $AR_{CTM} = 1000\times$, $I_{plasma} = 20$ A/cm^2). Moreover, for a tied-down MIM capacitor connected through a transistor, as shown in Fig. 1(c), it is evident that oxides with thicknesses of 30 and 3.5 nm show the effects of damage due to a damage current during the plasma process, as shown in Fig. 2. Comparing the plasma current–voltage characteristics with those of the oxide, I_{plasma} corresponds to a voltage stress V_{st} on the oxide during plasma processing. Enhanced oxide degradation resulting from plasma damage is also regarded as an increase in the equivalent voltage stress V_{st} across the oxide during plasma processing. Clearly, V_{st} not only depends on AR_{CTM} but is also affected by oxide thickness t_{ox}. E_{st}, defined as V_{st}/t_{ox}, is a function of AR_{CTM}, as shown in Fig. 3, i.e., a larger AR_{CTM} results in a larger E_{st}, causing much greater degradation of oxide reliability for all oxide thicknesses. Moreover, E_{st} also strongly depends on oxide thickness, which is predominantly related to the oxide tunneling mechanism. When the oxide thickness is greater than 3.5 nm, the oxide tunneling mechanism is dominated by Fowler–Nordheim (FN) tunneling, and it exhibits a greater AR_{CTM} dependence on E_{st} during the plasma process. In contrast, when the oxide thickness is reduced to 1.5 nm, the oxide tunneling mechanism is dominated by direct tunneling, resulting in a lower AR_{CTM} dependence on E_{st} compared with the thick-oxide case.

3.1.2 Results for damage to tied-down MIM capacitors

Figures 4 and 5 show the failure probabilities in leakage current of MIM capacitors for various AR_{CTM} with the CBM connected to the active area (i.e., the substrate) directly [Fig. 1(b)], and with the CBM connected to a transistor gate [Fig. 1(c)], respectively. Both of these test structures of tied-down MIM capacitors clearly show a significant failure distribution in leakage current as I_{plasma} increases, and the failure ratio depends on AR_{CTM}. Furthermore, comparing

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these two test structures of tied-down MIM capacitors, the structure with the CBM connected to the transistor gate exhibits better resistance to damage than that with the CBM connected to the substrate directly. For an AR_{CTM} of 1000×, the failure ratio of tied-down MIM capacitors connected to the substrate is about 30%, which was reduced to 15% when the tied-down MIM capacitors were connected to the transistor. Theoretically, the increase in charge-induced surface potential can be obtained by considering the substrate as two capacitors in series, which is similar to a voltage divider. During the plasma process, the voltage stress V_{st} across the MIM oxide for the tied-down MIM capacitor connected to the substrate directly is denoted as V_{MIMS}, as shown in Fig. 1(b); then, the voltage drop across the MIM oxide for the tied-down MIM capacitor connected to the transistor, denoted as V_{MIMT}, as shown in Fig. 1(c), is given by

$$V_{MIMT} = V_{st} \frac{C_{gox}}{C_{MIM} + C_{gox}}, \qquad (2)$$

where C_{MIM} is the capacitance of the MIM capacitor and C_{gox} is the capacitance of the gate oxide. From eq. (2), it is evident that V_{MIMT} is smaller than V_{MIMS}, which results in a lower failure ratio in leakage current for the tied-down MIM capacitors connected to the transistor, consistent with the results shown in Figs. 4 and 5. To increase the resistance of the MIM capacitors and transistors to P^2ID, it is possible to add a reverse-biased diode, as shown in Fig. 6, which is connected to the upper metal antenna with a large AR_{CTM}. As a result, a large amount of charge collected from the upper metal antenna can be discharged to the substrate and does not accumulate on the CTM and damage the MIM capacitors and transistors. As shown in Fig. 6, an antenna structure with a reverse-biased diode for protection results in a damage-free MIM capacitor, independent of AR_{CTM}, even for a large AR_{CTM} of 1000×.

3.1.3 Results for damage to floating-MIM capacitors

From the proposed model, $I_{plasma} = k \cdot AR_{CTM}$, the value of k not only depends on the process conditions[12] but is also related to the configuration of the MIM capacitor. As shown in Fig. 7, the floating-MIM capacitor does not exhibit any effects of damage, irrespective of AR_{CTM}. In addition, using the above concept of a voltage divider, the voltage drop across the floating-MIM oxide is denoted as V_{MIMF}, where

$$V_{MIMF} = V_{st} \frac{1}{1 + (C_{MIM}/C_{IMD})}. \qquad (3)$$

The inter-metal-dielectric (IMD) layer is defined as the insulating layer between the CBM and the substrate with a thickness of approximately 300–1000 nm, which is much thicker than the MIM oxide (i.e., only about 30 nm). From eq. (3), it is noted that V_{MIMF} is smaller than V_{st} owing to the large value of C_{MIM}/C_{IMD}. Therefore, during the plasma process, the voltage drop is greater across the IMD oxide than the MIM oxide, and negligible damage current flows through the MIM oxide. To prevent damage to the tied-down MIM capacitor shown in Fig. 6, although it is possible to add an extra reverse-biased diode to discharge the charge, this increases the parasitic capacitance and leakage current. Therefore, in this study, we propose the use of a floating-MIM capacitor, whose CBM can then be reconnected to the substrate or a transistor by an additional higher-level metal (Mn+1) rather than being tied down directly. In this way, damage and parasitic effects can both be eliminated simultaneously to meet the requirements of MS/RF applications.

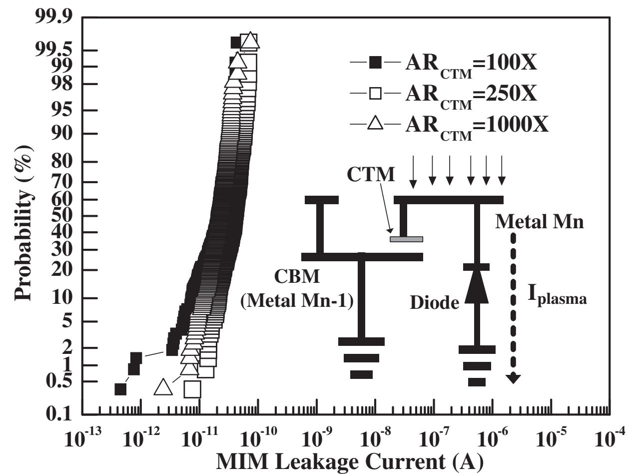

Fig. 6. Failure probability of leakage current for tied-down MIM capacitor upon adding a diode for protection to reduce the charging damage for various AR_{CTM}. The inset shows a schematic of the test structure.

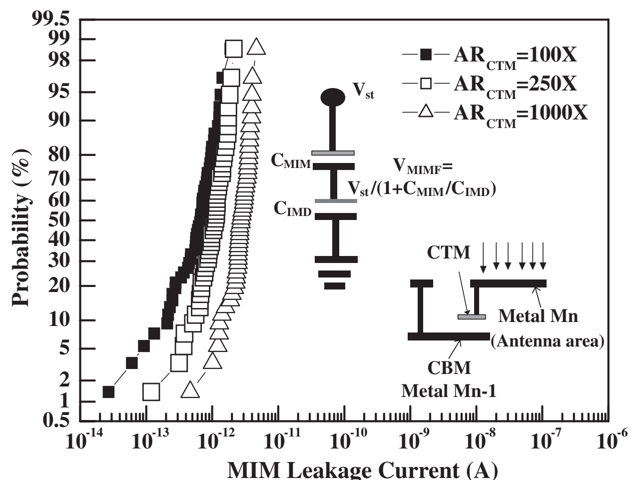

Fig. 7. Failure probability of leakage current for floating-MIM capacitor for various AR_{CTM}. The insets show schematics of the test structure and capacitor configuration.

3.2 MOSFET reliability degradation

3.2.1 Gate oxide degradation

According to the discussion in §3.1.1 for the transistor gate electrode connected to the MIM capacitors with a large AR_{CTM}, an equivalent voltage stress V_{st} can be created on the transistor gate oxide, resulting in a damage current flowing through the gate oxide during the plasma process. To measure such a transistor with its gate connected to the CBM of an MIM capacitor, as shown in Fig. 1(c), n-channel MOSFETs (NMOSFETs) and PMOSFETs with $t_{ox} = 3.5$ nm were fabricated and characterized. Figure 8 shows that the gate oxide failure ratio increases as a result of damage and is

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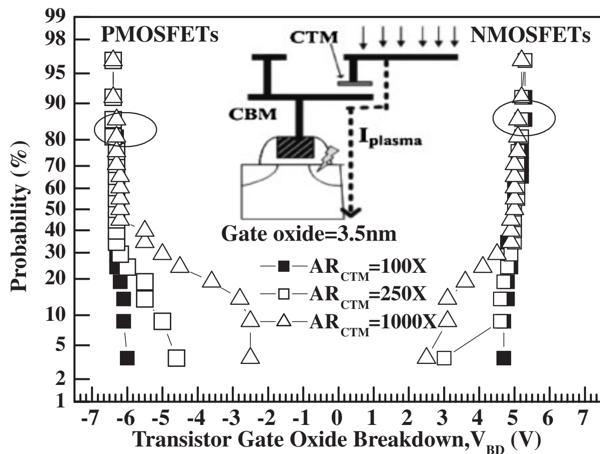

Fig. 8. Failure probability of gate oxide breakdown V_{BD} measured on NMOSFETs and PMOSFETs with $t_{ox} = 3.5$ nm and their gate connected to the CBM of the MIM capacitor for various AR_{CTM}. The inset shows a schematic of the test structure.

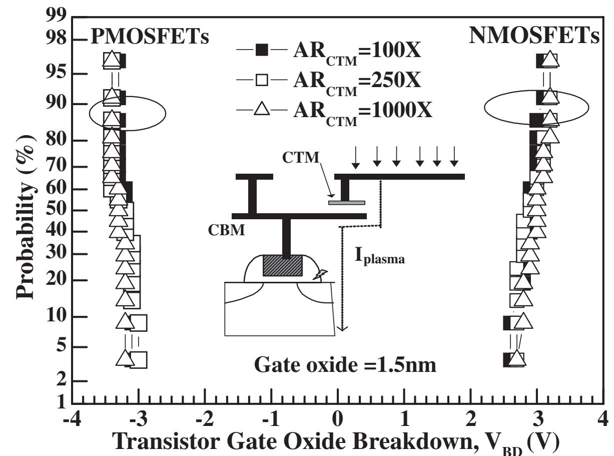

Fig. 9. Failure probability of gate oxide breakdown voltage V_{BD} measured on NMOSFETs and PMOSFETs with $t_{ox} = 1.5$ nm and their gate connected to the CBM of the MIM capacitor for various AR_{CTM}. The inset shows a schematic of the test structure.

dependent on AR_{CTM}, consistent with our damage model. In addition, the difference in the failure ratios between PMOSFETs and NMOSFETs is due to the oxide current–voltage characteristics. During a plasma process with a given I_{plasma}, PMOSFETs are stressed with a higher stress voltage, and therefore, the failure ratios of PMOSFETs are larger than those of NMOSFETs. Comparing the results of Figs. 8 and 5, it is noted that the failure probability of the gate oxide with $t_{ox} = 3.5$ nm is larger than that of the MIM oxide with $t_{ox} = 30$ nm, consistent with the dependence of E_{st} on the oxide thickness for various AR_{CTM}, as shown in Fig. 3. To investigate the effect of charging damage for a large AR_{CTM} on the core circuit, we further extend this study to ultrathin gate oxide transistors. For transistors fabricated with $t_{ox} = 1.5$ nm, the oxide-tunneling mechanism is dominated by direct tunneling, resulting in a smaller voltage stress V_{st} on the gate oxide during a given plasma process. The results of Fig. 9 again confirm that there is no failure in the transistor gate oxide, even for a large AR_{CTM}. Obviously, for a given plasma process condition, E_{st} strongly depends on the gate oxide thickness. More importantly, Fig. 3 shows that E_{st} is a function of oxide thickness and exhibits a maximum in the range of 3.5–5.0 nm, independent of AR_{CTM}. In addition, this range of oxide thickness results in the strongest AR_{CTM} dependence on E_{st}. This E_{st} dependence implies that plasma-charging damage is a less serious concern for the transistor with an ultrathin gate oxide than for the transistor with a thick gate oxide. Correspondingly, a thinner gate dielectric was found to be robust against plasma-induced damage.[13] This is because V_{st} decreases to near or below the anticipated operational voltage. The effect of damage on reliability is expected to be one of the most serious issues for input/output (I/O) circuit applications in advanced MOSFET technologies, where the gate oxide thickness is in the range of 3.0–5.0 nm and the operational voltage is approximately 1.8–2.5 V. The failure probability of the gate oxide is effectively suppressed for an ultrathin gate oxide of 1.5 nm (Fig. 9) compared with that for a gate oxide thickness of 3.5 nm (Fig. 8). These results are consistent with our proposed model, according to which, a lower operation voltage results in a lower V_{st} that is near the operation voltage; thus, a negligible failure probability of the gate oxide was found in the thin-gate-oxide region during the MIM capacitor plasma process.

3.2.2 Transistor reliability degradation model

P^2ID is usually evaluated by monitoring the oxide leakage current[13] or oxide breakdown voltage[14] as demonstrated in the above sections. The occurrence of additional gate oxide leakage indicates that additional current paths have been generated within the gate oxide. However, prior to the formation of a conductive path within the SiO_2 bulk, the SiO_2/Si substrate interface must accumulate a sufficient number of defects due to the damage process, resulting in the degradation of transistor reliability including the occurrence of hot-carrier-injection (HCI) stress[15] or NBTI stress.[16] In other words, the degradation of transistor reliability occurs before the gate leakage increases. Comparing the plasma with the oxide current–voltage characteristics shown in Fig. 10, I_{plasma} corresponds to a voltage stress V_{st} on the transistor gate oxide during processing. Aggravated transistor degradation resulting from plasma damage is therefore understood as an increase in the voltage stress ΔV_{st} across the gate oxide during processing. Moreover, we can express the relationship between AR_{CTM} and ΔV_{st} as

$$\ln(AR_{CTM}) = C\Delta V_{st}, \quad (4)$$

where C is the slope of the gate oxide current–voltage characteristics shown in Fig. 10 and strongly depends on the gate oxide thickness. From eq. (4), we assume that the plasma damage in the gate oxide of transistors is similar to that caused by gate voltage stress. Defects introduced by the plasma damage are not usually evident following MIM capacitor processing because the postmetallization annealing passivates them.[17] However, subsequent electrical stress, such as NBTI, can reveal their existence since these defect sites are generally weaker than undamaged sites. Transistor reliability characteristics, such as NBTI, are greatly affected by interface/bulk trapping. Assuming that the gate voltage

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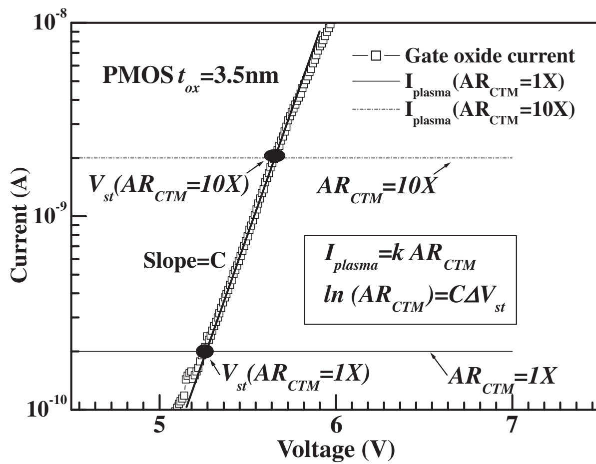

Fig. 10. Characteristics of measured oxide current and simulated damage current with respect to voltage as a function of AR_{CTM} on PMOSFET with t_{ox} = 3.5 nm.

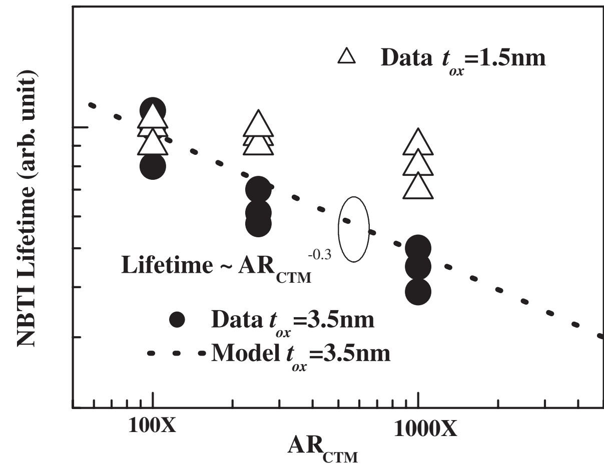

Fig. 11. PMOSFET NBTI lifetime versus AR_{CTM} for transistors with t_{ox} = 3.5 and 1.5 nm.

stress V_{st} generated from plasma is uniform across the wafer, the number of interface states generated by the capture of Si–H bonds at the SiO_2/Si substrate interface ΔN_{it} resulting from the gate stress can be written in terms of the increase in the gate voltage stress ΔV_{st} as[18)]

$$\Delta N_{it} = Bt_p^n \exp(\gamma_p \Delta E_{st}) = Bt_p^n \exp(\gamma_p \Delta V_{st}/t_{ox}), \quad (5)$$

where t_p is the duration of the plasma process and $n = 0.2$. γ_p is the field acceleration factor, which depends on the process conditions, and is about 0.1–0.2 (decades/MV/cm) during plasma processing.[19,20)] B is a constant related to process conditions.

During NBTI stress, holes in the inversion layer gain sufficient energy to dissociate the weak Si–H bonds, resulting in the generation of interface states. It is evident that all devices (i.e., the control and antenna) exhibit NBTI degradation. However, antenna devices are expected to have a higher concentration of weak Si–H bonds at the interface. For a constant gate oxide thickness t_{ox}, the threshold voltage shift ΔV_{TH} can be modeled as

$$\Delta V_{TH} = Ht^n \mathrm{AR_{CTM}}^{\alpha}, \quad (6)$$

where t is the duration of NBTI electrical stress, H is a constant, and

$$\alpha = \gamma_p/(t_{ox}C). \quad (7)$$

The failure time t_f, defined as the time required to reach a critical threshold voltage shift ΔV_c, is

$$t_f = G\Delta V_c \mathrm{AR_{CTM}}^{-m}, \quad (8)$$

where G is a constant and $m = \alpha/n$.

3.2.3 Results for degradation of transistor reliability

Damage-enhanced NBTI degradation was also studied for the tied-down MIM capacitor connected to PMOSFETs of $t_{ox} = 3.5$ and 1.5 nm. Figure 11 shows the AR_{CTM} dependence of the NBTI degradation of the PMOSFETs. For transistors with $t_{ox} = 3.5$ nm, the AR_{CTM} dependence of the NBTI degradation follows a power-law relationship consistent with eq. (8). It further demonstrates that both the model and the experimental data show a power-law relationship between the NBTI lifetime and AR_{CTM} with $m = -0.3$. From Fig. 10, it is evident that C is determined by the oxide conduction mechanism, and the antenna dependence m in eq. (8) can be significantly reduced with a larger C for ultrathin gate oxide transistors. Moreover, from Figs. 2 and 3, the smaller V_{st} and E_{st} suggest that damage is not a serious concern for the tied-up transistors with an ultrathin gate oxide compared with that for the transistors with a thick gate oxide. As a result, upon damage-enhanced NBTI lifetime degradation in ultrathin gate oxide transistors, a smaller and negligible dependence of NBTI degradation on AR_{CTM} is also found, as shown in Fig. 11. On the basis of our experimental results, we confirm the impact of plasma damage during the MIM process on the transistor reliability for thick gate oxide transistors. However, because of the strong t_{ox} dependence of the damage process, the damage becomes insignificant for transistors with an ultrathin gate oxide of less than 1.5 nm.

3.3 Prediction of transistor reliability failure distribution

From eqs. (4)–(8), one can predict the functional dependence of the NBTI degradation on plasma damage and the design parameters of AR_{CTM} and t_{ox}. However, the amount of plasma damage may vary among transistors owing to different plasma conditions and values of AR_{CTM}, and t_{ox} due to variations during processing. It is believed that all these process variations should follow normal distributions, resulting in a lognormal distribution of V_{st} from eq. (4). Accordingly, from eq. (5) it is expected that the variation in ΔN_{it} during plasma damage should follow a normal distribution across a wafer. The NBTI lifetime is affected by the variation in ΔN_{it} from eqs. (6)–(8). By assuming a nominally identical AR_{CTM} and t_{ox}, and with the further assumption of a normal distribution of $\Delta N_{it}(\mu, \sigma)$, a corresponding distribution of threshold voltage shift will be generated during NBTI stressing. Therefore, the mean value μ and standard variation σ of the distribution of ΔN_{it} are both parameters dependent on AR_{CTM}, as shown in eqs. (5) and (6). In this way, it is possible to construct a Monte Carlo simulation of the distributions of NBTI from the corresponding ΔN_{it} distribution across the wafer.

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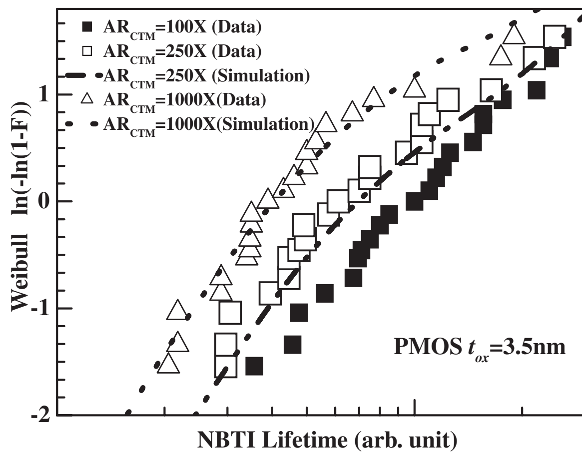

Fig. 12. Simulation results of PMOS NBTI lifetime distribution for various AR_{CTM} for transistors with t_{ox} = 3.5 nm.

Figure 12 shows the NBTI lifetime distribution as a function of AR_{CTM}. In this case, the simulated distributions are in excellent agreement with those determined experimentally.

From Fig. 12, the impact of plasma damage on the transistor failure distribution is that it causes a severe distortion of the lognormal distribution at high percentiles. At low percentiles, the distribution slope is almost independent of AR_{CTM}, and failure times are reduced in accordance with eqs. (4)–(8). Moreover, there is no indication in the experimental data of the presence of an early failure distribution arising from a defective subpopulation, as required for our proposed model.

4. Conclusions

In this study, plasma-induced damage creates significant numbers of defects and weakened interface bonds in both the MIM oxide and the transistor gate oxide that can be easily damaged during reliability testing. The increased rate of generation of bulk/interface states leads to enhanced oxide failure and transistor degradation. We have conducted a comprehensive study of the effect of MIM plasma damage on capacitor and transistor reliability. Our results show that the degradation of the MIM capacitor and the transistor depend on the antenna ratio of the upper-level metal connected to the CTM (AR_{CTM}) and the oxide thickness. In addition, our model shows that the NBTI degradation of transistors exhibits identical dependence on a design parameter of the MIM capacitor, i.e., AR_{CTM}. We further confirm that the transistor with a thick gate oxide is more susceptible to plasma damage than that with a thin oxide for a tied-down MIM capacitor. We have experimentally verified our transistor reliability degradation model and shown that the plasma damage failure distribution deviates significantly from the lognormal distribution with increasing AR_{CTM}, as a result of variations in plasma processing between transistors in the presence of MIM plasma damage.

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