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Effect of bias stress on mechanically strained low temperature polycrystalline silicon thin film transistor on stainless steel substrate

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This paper reported the variation in performance of bias stressed low-temperature polycrystalline silicon thin film transistors (LTPS TFTs) fabricated on metal foil substrate for flexible display applications. The mobility, threshold voltage (V_{th}), and trap density (N_t) of the proposed *p*-channel poly-Si TFT as a function of curvature radii were investigated. The significant increase in V_{th} by 9% was observed as the compressive or tensile mechanical strain increases to 0.1%. In addition, the hole mobility increases by 7% due to an increased compressive strain of 0.1%, while hole mobility decreases by 3.5% with the increase in tensile strain of 0.1%. After dc bias stressing, the LTPS TFT with mechanical strain had better performance than that on flat state in both the mobility drop and V_{th} shift. Mechanical strain influences the lattice arrangement and electric field at the drain electrode region that resisted device degradation in early stressing period. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3193654]

Among many foldable substrate candidates, steel foil substrate is very attractive due to its thin, lightweight, flexible, and rugged characteristics.[1] As compared with plastic substrates, the steel foil substrate is compatible with the traditional manufacture process of thin film transistors (TFTs) due to its higher melting point and better blocking against water vapor and oxygen permeability. In addition, the polycrystalline-Si (poly-Si) TFTs has attracted much attention because of the higher field-effect mobility than any other kinds of TFTs.[2] Previous researchers have reported the effect of tensile strain on the mobility of poly-Si TFTs.[3] However, no further investigation was reported for the influence of bias stress on the mechanically strained poly-Si TFT devices. In this work, therefore, we study the effect of bias stress on the variations in threshold voltage, mobility, and trap density for the *p*-channel poly-Si TFT under uniaxial compressive and tensile strain induced by substrate mechanically bending.

The poly-Si TFT devices were fabricated on a stainless steel foil with Young's modulus 200 GPa (thickness $=70\ \mu$m, area$=10\times10\ \text{cm}^2$) by conventional low-temperature polycrystalline silicon (LTPS) process. Because the roughness of bare steel foil was not suitable for TFT process, it was mechanically polished first. A 2 μm thick spin-on-glass (SOG) buffer layer was coated on the polished steel foil in order to obtain a smoother surface with surface roughness (R_a) of about 0.499 nm compared to polished surface 0.89 nm. The SOG was formed by spin coating and baked in an oven under 450 °C for 2 h. A 0.3 μm thick SiO_2 buffer layer and a 50 nm thick amorphous hydrogenated silicon (*a*-Si:H) layer were deposited sequentially at a plasma-enhanced chemical vapor deposition (PECVD) system. Following the dehydrogenation, the *a*-Si film was crystallized by typical XeCl excimer laser annealing (ELA) with a wavelength of 308 nm and an energy density of 400 mJ/cm^2. After ELA process, poly-Si channel layer was patterned and a 100 nm thick silicon dioxide as gate dielectric was deposited by PECVD. A self-aligned boron doping technology was used to form p^+ source and drain regions with a dose of 2×10^{15} ions/cm^2 at 70 keV. Thermal annealing was conducted at 450 °C by rapid thermal process to activate the dopant in the source and drain regions. After the deposition of a 300 nm thick PECVD interlayer dielectric SiN_x for passivation layer, a metallization consisting of a 200 nm thick chromium (Cr) was applied for the source/drain metal electrode. The compressive strain or tensile strain was applied to the poly-Si TFTs on metal foil parallel to the source-drain current path. The characteristic of TFT devices was measured as a function of strain under mechanical bending inward or outward. Both channel width (W) and channel length (L) of the poly-Si TFT device are 20 μm. Under dc stress condition, we applied drain and gate bias voltage of −20 V, with stressing times 0, 1000, and 2000 s under flat, compressive ($R_n=10$) and tensile ($R_p=10$ mm) status.

The *p*-channel LTPS TFT has exhibited superior field-effect mobility of 92 $\text{cm}^2/\text{V s}$, a threshold voltage of −5.7 V, and an on/off current ratio higher than 10^7 and subthreshold slope of 0.85 V/decade without mechanical stress. Figure 1 shows the variation in field-effect mobility (μ) and V_{th} of poly-Si TFTs on metal foil under tensile and compressive strains with curvature radius (R). The strain on the surface is calculated by[4]

$$\varepsilon_{\text{surface}} = \left(\frac{d_f + d_s}{2R}\right)\frac{(1+2\eta+x\eta^2)}{(1+\eta)(1+x\eta)}, \tag{1}$$

where $\eta=d_f/d_s$ and $x=Y_f/Y_s$, where $d_f=2.8$ and $d_s=70\ \mu$m are film and substrate thickness, respectively. Young's modulus of film and substrate for both Y_f and Y_s are 200 GPa.[5] The V_{th} increased as the mechanical strength enlarged. The breakage of weak Si–Si bonds during mechanical

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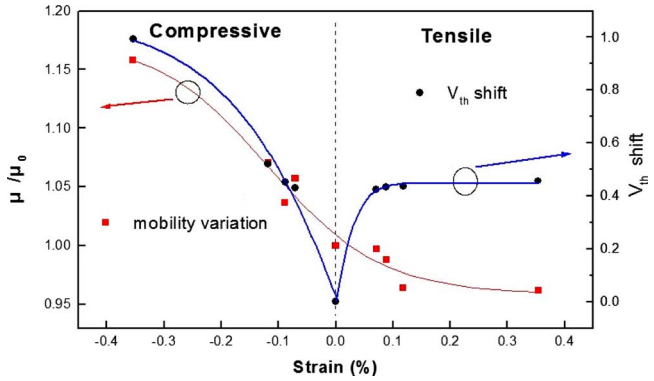

FIG. 1. (Color online) The field-effect hole mobility variation and threshold voltage shift (ΔV_{th}) as a function of strain with bending radius $R=\infty$, ± 50, ± 40, ± 30, and ± 10 mm, respectively, at $V_D=-10$ V. μ_0 is the initial hole mobility of poly-Si TFT on flat substrate, while μ is the one after mechanical strain.

strain lead to creation of the dangling bonds and defect traps. The bond strength can be affected by the mechanical strain and thus the creation of dangling bonds depends on the substrate curvature.[6]

The variations in trap density of poly-Si film were extracted to investigate the strain influence on the poly-Si TFT device. From Seto's theory, it can be modeled the relationship between grain boundary potential barrier V_B and doping concentration N_D (cm^{-3}). When doping concentration N_D increased more than N_t/L, the grain boundary potential barrier height V_B can be expressed as the following equation:

$$V_B = \frac{qn}{2\varepsilon_s}\left(\frac{N_t}{2n}\right)^2 = \frac{qN_t^2}{8\varepsilon_s n},$$

where N_t (cm^{-2}) is the density of acceptorlike traps at grain boundary, V_B is the grain boundary potential barrier height, and n (cm^{-3}) is the carrier concentration. As proposed by Levinson *et al.*[7] and a better approximation for channel thickness t_{ch} in an undoped material,[8] the *I-V* characteristics including the trap density can be obtained by the following equation:

$$I_D = \mu_0 C_{ox}\frac{W}{L}(V_G - V_{FB})V_D \exp\left(-\frac{q^2 N_t^2\sqrt{\varepsilon_{ox}/\varepsilon_s}}{C_{ox}^2(V_G - V_{FB})^2}\right).$$

The effective trap state density then can be obtained from the slope of the curve $\ln[I_D/(V_G - V_{FB})]$ versus $(V_G - V_{FB})^{-2}$. We calculated the trap density variation rate under different bending condition as shown in Fig. 2(a). Both tensile and compressive strain increased the trap density. The curve of trap density variation shows strong correlation with V_{th} shift but not with μ variation in Fig. 1. It was known that the carrier mobility is strongly correlated with trap density and reversely proportional to the trap density in the poly-Si film.[9] The known theory generally serves the poly-Si TFT device without mechanical strain and the variation in carrier effective mass. In this work, however, experimental results indicate that the trap density would not solely dominate the carrier mobility of the strained poly-Si TFT devices. The integral effects originated from lattice torsion, carrier effective mass, and trap density should be considered for the mechanically strained TFT, which can be totally reflected in the parameter of activation energy (E_a). The values of E_a for the poly-Si TFT under different strain states was extracted by the

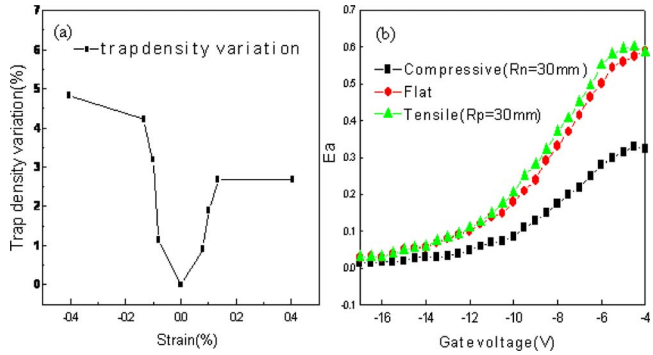

FIG. 2. (Color online) (a) The trap density variation rate under bending radius $R=\infty$, ± 50, ± 40, ± 30, and ± 10 mm, respectively. (b) The extracted activation energy E_a for the poly-Si TFT under different bending conditions.

varied temperature measurement ranging from 25 to 120 °C, as shown in Fig. 2(b).[10] The energy barrier height under the compressive stress is the lowest than those on the states of the flat and the tensile. A reduced E_a can contribute the enhanced hole mobility to the *p*-channel poly-Si TFT. Therefore, the compressive strain on poly-Si TFT results in the highest mobility among any other strain types discussed in Fig. 1.

According to the study of *p*-channel metal oxide semiconductor (PMOS) devices, biaxial tensile strains could improve PMOS and *n*-channel metal oxide semiconductor drain current simultaneously but uniaxial strain effects improve one device and depraving the other instead.[11] Three factors affect single crystalline silicon mobility: silicon thickness, surface orientation, and strain. In poly-TFT devices, the effects of uniaxial tensile and compressive strain split the energy band of light hole and heavy hole, and then reduce scattering effect, indicating the increase in mean free time.[12,13] In addition, the mechanical strain makes apparent band warping, reducing the hole effective mass. Mobility is proportional to electric charge, mean free time, and reversed to electric/hole effective mass, and resultantly the uniaxial compressive could increase mobility.[14]

In PMOS devices, the highest hole mobility was in the (110) direction parallel the source/drain current path because of carrier repopulation.[12] When the bending direction paralleled to the surface orientation (110), the tensile condition got low carrier mobility, whereas compressive condition get higher carrier mobility. Though poly-Si contains other sur-

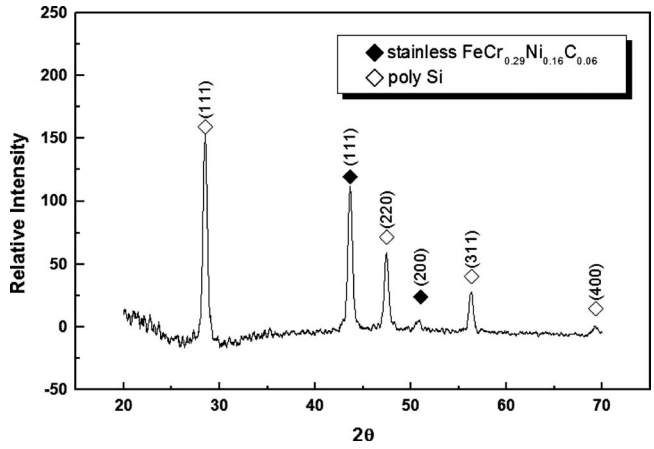

FIG. 3. XRD analysis of polycrystalline Si film on steel metal foil.

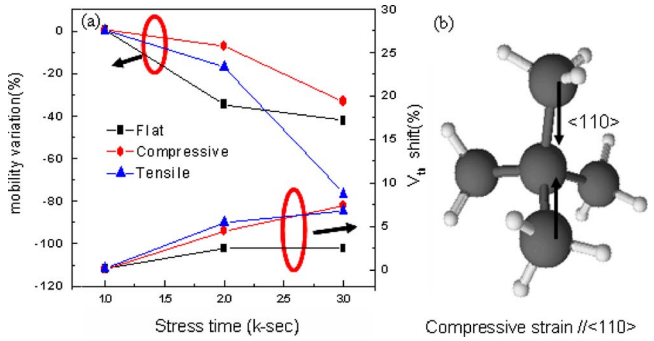

FIG. 4. (Color online) (a) The mobility variation and threshold voltage shift in *p*-channel LTPS TFT devices under different mechanical strain as function of dc stress time under gate and drain voltage of −20 V and (b) the applied compressive strain effect along Si surface orientations (110).

face orientations of grain, the (110) surface acts as major effect when strain is performed. In Fig. 3, the grain orientation of poly-Si film on metal foil was analyzed by using x-ray diffractometer (XRD). The orientation of (111), (110), and (100) is indicated in our samples. The signal pulses of (400), (220), and (222) are the same to orientation (100), (110), and (111), respectively. The obvious signal intensity of (110) indicated higher drain current could be obtained while the poly-Si TFT device under compressive stress state.

Effects of bias stress on the mechanically strained poly-Si TFT device also were investigated in this work. In Fig. 4(a), the compressive strain leads to less mobility drop than the flat and the tensile strain under initial stressing period (<1000 s). The effect of compressive strain lightened carrier (i.e., hole) effective mass resultantly increased carrier mobility. The mobility enhancement originated from compressive strain partially compensated for an influence of dc stress on the mobility degradation. Figure 4(b) illustrates the applied strain effect along Si surface orientations (110). The strain effect on mobility shows good resistance to the degradation after bias stress. Higher carrier mobility under compressive strain makes TFT devices more stable in dc bias stress condition.

In summary, the LTPS TFTs were fabricated on steel foil. Threshold voltage shift and trap density variation were observed under compressive and tensile strains. The holes mobility was enhanced by compressive strain while degraded by tensile strain. In addition, the carrier mobility and on-state current are decreased obviously after dc bias stress with mechanical strain applied. Mechanical strain influences the lattice distance and electric field at the drain region, which resist device degradation in early stressing period. The proposed poly-Si TFT maintained good electrical characteristics, even when subjected to compressive or tensile mechanical strain with a bending radius of 10 mm under bias stress condition.

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