A Comparative Study of Carrier Transport for Overlapped and Nonoverlapped Multiple-Gate SOI MOSFETs

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***Abstract*—This paper provides a comparative study of carrier transport characteristics for multiple-gate silicon-on-insulator MOSFETs with and without the nonoverlapped source/drain structure. For the overlapped devices, we observed Boltzmann law in subthreshold characteristics and phonon-limited behavior in the inversion regime. For the nonoverlapped devices, however, we found insensitive temperature dependence for drain current in both subthreshold and inversion regimes. Our low-temperature measurements indicate that the intersubband scattering is the dominant carrier transport mechanism for narrow overlapped multigate field-effect transistors (MuGFETs). For the nonoverlapped MuGFETs, the voltage-controlled potential barriers in the nonoverlapped regions may give rise to the weak localization effect (conductance reduction) and the quantum interference fluctuations.**

***Index Terms*—Carrier transport, MOSFET, multiple-gate, nonoverlapped, overlapped.**

I. INTRODUCTION

MULTIGATE silicon-on-insulator (SOI) MOSFET (MuGFET) structures provide superior electrostatic integrity needed for MOSFET scaling entering the deca- to nanometer regime [1]. The benefits of multigate field-effect transistor (MuGFET) have been extensively investigated regarding issues of short-channel effects, leakage current, threshold voltage (V_T) fluctuations, mobility, and so on [2].

For MuGFET device design, source/drain engineering is crucial because of the parasitic drain/source resistance [3] and the parasitic fringing/overlap capacitance that may limit circuit performance [4]. Two options in the source/drain engineering are the overlapped structure with light-doping-drain/source (LDD/LDS) and the nonoverlapped structure. Whether the various source/drain engineering will impact the carrier transport in nanoscale MuGFETs merits examination. In this paper, we conduct a systematic comparison of carrier transport between overlapped and nonoverlapped multigate SOI MOSFETs. The investigation has included measurements from $T = 300$ K to 56 K.

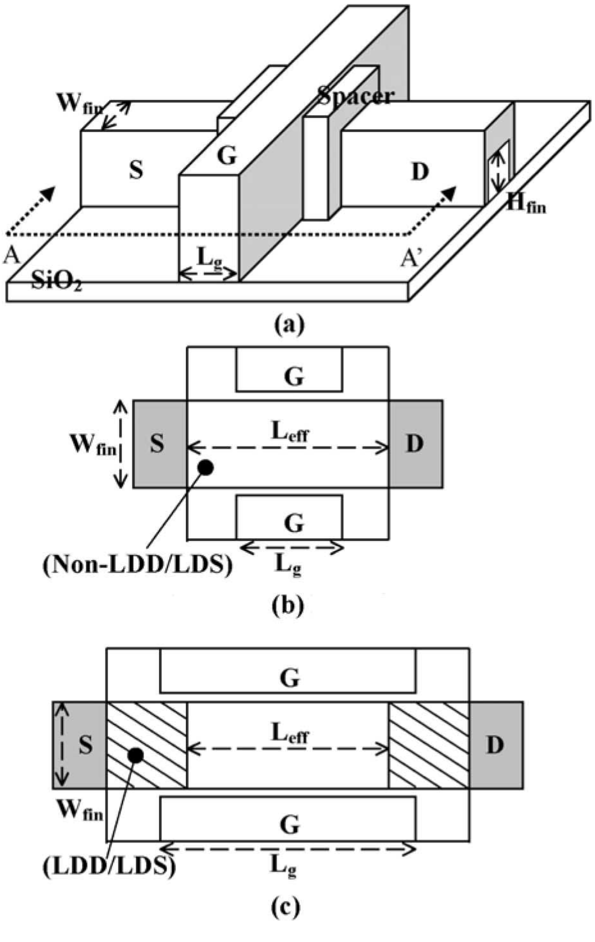

Fig. 1. (a) Multiple-gate FinFET SOI structure investigated in this work and its cross-sectional AA' view along the channel direction showing (b) nonoverlapped gate to source/drain structure and (c) overlapped gate to source/drain structure.

II. DEVICES

Fig. 1(a) shows a schematic view of the multigate SOI MOSFET investigated in this study. Our devices were fabricated on SOI wafers using standard CMOS optical lithography [5]. The Si-body thickness, H_{fin}, was thinned down to about 40 nm by thermal oxidation. The fin-width, W_{fin}, was defined by wet etching. After W_{fin} was developed, the Si-body fin was doped with BF$_2$ implantation and annealed. Using optical lithography and anisotropic reactive ion etching, the gate length, L_g, was defined. Note that the LDD/LDS implantation was performed for the overlapped structure [Fig. 1(c)] and was skipped for the

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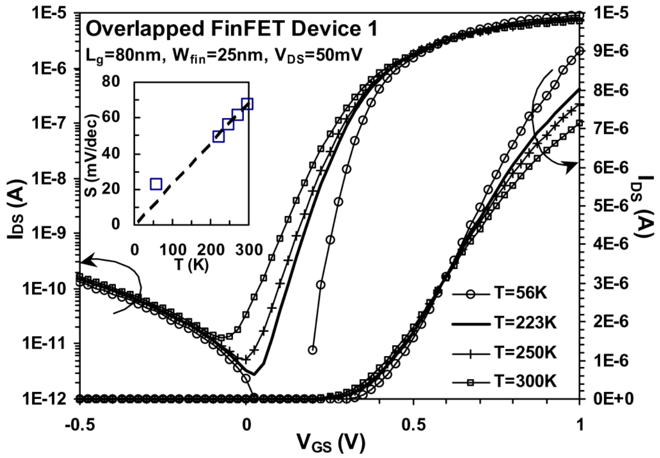

Fig. 2. Measured $I_{\rm DS}$ versus $V_{\rm GS}$ at $V_{\rm DS} = 50$ mV under $T = 300$ to 56 K for the overlapped FinFET device 1 with $W_{\rm fin} = 25$ nm and $L_g = 80$ nm.

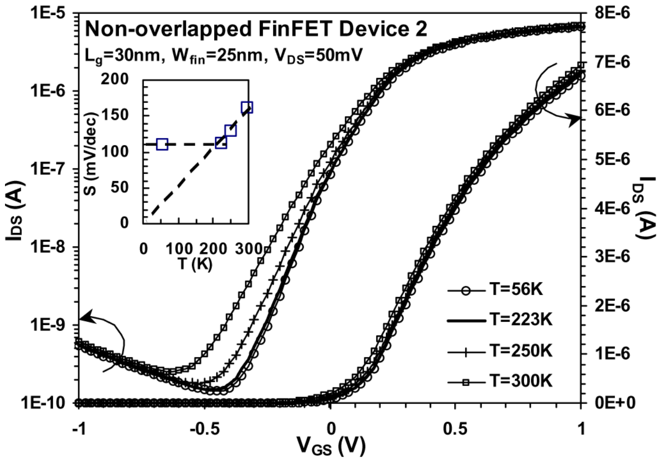

Fig. 3. Measured $I_{\rm DS}$ versus $V_{\rm GS}$ at $V_{\rm DS} = 50$ mV under $T = 300$ to 56 K for the nonoverlapped FinFET device 2 with $W_{\rm fin} = 25$ nm and $L_g = 30$ nm.

nonoverlapped structure [Fig. 1(b)] before developing the composite spacer of silicon oxide and nitride. Finally, heavily doped N$^+$ source/drain was made. In this study, we compare these two types of devices based on the same effective source-drain length $L_{\rm eff}$.

III. EXPERIMENT

Current-voltage measurements $(I_{\rm DS} - V_{\rm GS})$ at $V_{\rm DS} = 50$ mV under $T = 300$ K to 56 K were performed with a 25-mV $V_{\rm GS}$ step for the overlapped device 1 with $W_{\rm fin} = 25$ nm and $L_g = 80$ nm (Fig. 2) and for the nonoverlapped device 2 with $W_{\rm fin} = 25$ nm and $L_g = 30$ nm (Fig. 3). Fig. 2 shows that the subthreshold swing S for the overlapped device 1 decreases with temperature. We have confirmed that the S–T characteristic follows the Boltzmann law $S = n(k_BT/q)\ln(10)$ with the body effect coefficient $n \approx 1.16$. The linear temperature dependence of S is a feature of fully depleted SOI [8] and has also been observed in trigate SOI MOSFETs [13].

For the nonoverlapped device 2, however, the linear temperature dependence of S can only be seen when temperature is higher than 223 K (Fig. 3). For temperature below 223 K, S is constant and does not follow the Boltzmann law. This suggests that for the nonoverlapped device 2, tunneling current dominates the fundamental limitation of leakage current instead of the thermal current [12]. We have noted that similar S behavior has been reported at $T < 100$ K for the planar nonoverlapped nMOSFET in [12]. It implies that the leakage current associated with thermionic emission is suppressed in our MuGFET.

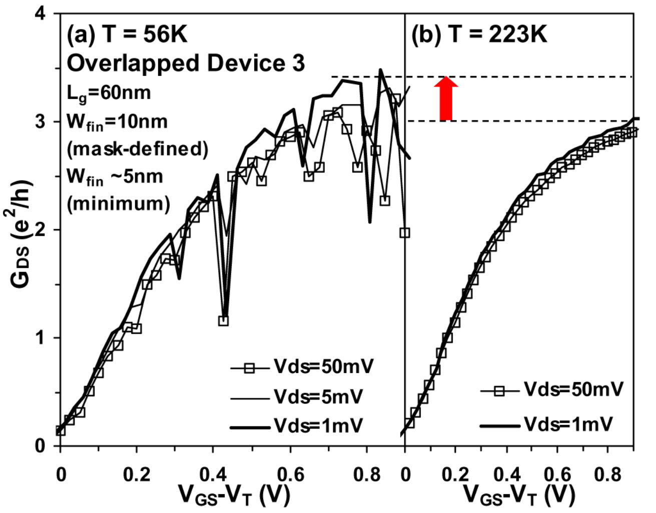

Fig. 4. Measured channel conductance $(G_{\rm DS})$ versus $(V_{\rm GS} - V_T)$ characteristics for the overlapped device 3 with $L_g = 60$ nm and $W_{\rm fin} = 10$ nm at various $V_{\rm DS}$ under (a) $T = 56$ K and (b) $T = 223$ K.

The insensitive temperature dependence of $I_{\rm DS}$ can also be found in the strong inversion region for the nonoverlapped device 2 (Fig. 3). In contrast to that of the overlapped device 1 (Fig. 2), the $I_{\rm DS}$ for $V_{\rm GS} > 0.6$ V is nearly independent on temperature. These results indicate that carrier transport in the strong inversion region is determined by the phonon-limited mobility for the overlapped device 1, but not for the nonoverlapped device 2.

To further compare the carrier transport characteristics for overlapped and nonoverlapped devices, we have investigated channel conductance $(G_{\rm DS} = I_{\rm DS}/V_{\rm DS})$ with low $V_{\rm DS}$. Fig. 4 shows the measured $G_{\rm DS}$ versus $V_{\rm GS}$ characteristics for the overlapped device 3 with $W_{\rm fin} = 10$ nm and $L_g = 60$ nm. Significant $G_{\rm DS}$ fluctuations can be seen at $T = 56$ K [Fig. 4(a)]. Similar $G_{\rm DS}$ fluctuations have been reported in [6] and attributed to the intersubband scattering. While the number of populated subbands increases with increasing $V_{\rm GS}$, the intersubband scattering also increases with each new subband [7]. In other words, when $V_{\rm GS}$ increases, the $G_{\rm DS}$ increases due to new populated subbands and then decreases due to the mobility reduction (i.e., the increase of intersubband scattering). Thus, fluctuations can be seen in the $G_{\rm DS} - V_{\rm GS}$ characteristics. We have noted that the $G_{\rm DS}$ fluctuations almost occur at the same $V_{\rm GS}$, such as the spike at $V_{\rm GS} - V_T = 0.425$ V [Fig. 4(a)]. We have also noted that for the wider overlapped devices (i.e., device 1) with negligible subband splitting, the $G_{\rm DS}$ fluctuations can not be found.

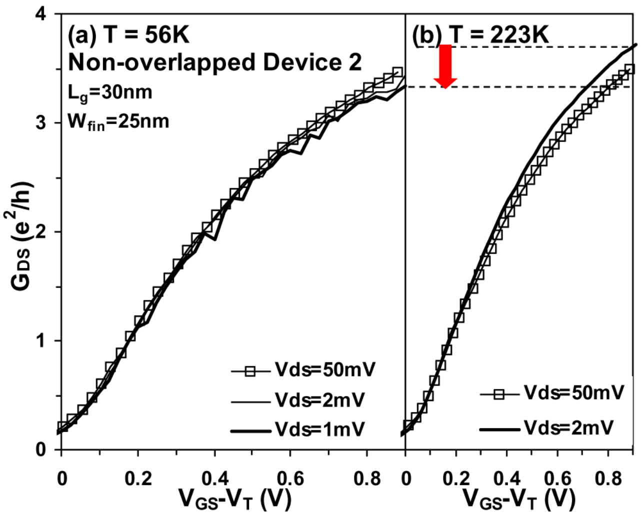

Fig. 5. Measured $G_{\rm DS}$ versus $(V_{\rm GS} - V_T)$ characteristics for the nonoverlapped device 2 with $L_g = 30$ nm and $W_{\rm fin} = 25$ nm at various $V_{\rm DS}$ under (a) $T = 56$ K and (b) $T = 223$ K.

One important criterion to observe the intersubband scattering effect is that the $qV_{\rm DS}$ and k_BT are not significantly larger than the subband energy split ΔE [7]. It is worth noting in Fig. 4(a) that the $G_{\rm DS}$ fluctuations can be observed at $V_{\rm DS} = 50$ mV under $T = 56$ K. Considering the voltage drop across the access resistances (i.e., source/drain resistances, contact resistance and back-end metal resistance), the effective $qV_{\rm DS}$ over the channel and therefore ΔE may be about 20 to 30 meV. This is also consistent that with the observed $G_{\rm DS}$ fluctuations at $V_{\rm DS} = 1$ mV under $T = 223$ K shown in Fig. 4(b). Besides, we have noted in our process that the final minimum $W_{\rm fin}$ at the channel center is smaller than the mask-defined 10-nm $W_{\rm fin}$ (final minimum $W_{\rm fin} \sim 5$ nm) due to over etching.

An important signature for intersubband scattering is that conductance reductions (i.e., mobility reduction) occur as $V_{\rm DS}$ increases [6]. This is because the drain bias forces electrons to jump from higher to lower subbands and thus enhances intersubband scattering and reduces the carrier mobility [7]. It is worth noting that the reductions in $G_{\rm DS}$ due to mobility reduction can also be observed at $V_{\rm DS} = 1$ mV when temperature increases from 56 K to 223 K. Similar $V_{\rm DS}$ and temperature dependence in $G_{\rm DS}$ have also been observed for trigate SOI MOSFETs in [6] and [7].

For the nonoverlapped device 2 in the high $V_{\rm GS}$ regime, the $G_{\rm DS}$ increases with $V_{\rm DS}$ and temperature as can be observed in Fig. 5(a) and (b), respectively. Such $V_{\rm DS}$ and temperature dependence of $G_{\rm DS}$ are completely opposite to that of the overlapped device 3 (Fig. 4) and cannot be ascribed to the intersubband scattering effect. In addition, Fig. 5 also shows interesting fluctuations with negative differential resistance in the $G_{\rm DS}$. Although the $G_{\rm DS}$ fluctuations in Fig. 5 were observed in the same measurement conditions as Fig. 4, one can safely state that it does not result from the intersubband scattering. In the next section, we will give more discussions for the anomalous temperature dependence and the $G_{\rm DS}$ behavior of the nonoverlapped device 2.

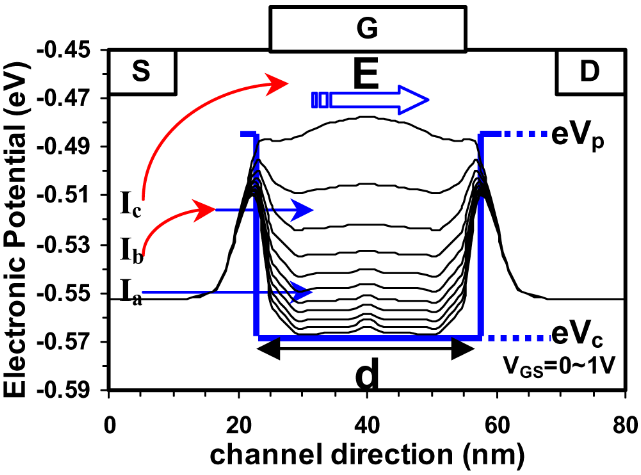

Fig. 6. Calculated electronic potential for the nonoverlapped gate to source/drain structure at $V_{\rm GS} = 0$ V to 1 V. V_p: peak potential value in the nonoverlapped region. V_c: potential value at the channel center. E: carrier energy. d: width of the effective quantum well. I_a: direct tunneling through the potential barrier of the nonoverlapped region. I_b: thermally associated tunneling. I_c: thermionic emission.

IV. INTERPRETATION

Fig. 6 shows the electronic potential calculated using ISE device simulation [16] for our nonoverlapped device. The nonoverlapped gate to source/drain regions act as the voltage-controlled potential barriers along the channel. Therefore, carrier transport from source to drain is significantly influenced by the barriers as illustrated in Fig. 6: directly tunneling (I_a), thermally associated tunneling (I_b), and thermionic emission (I_c). The contribution of these three mechanisms to $I_{\rm DS}$ depends on $V_{\rm GS}$ and temperature. For high $V_{\rm GS}$, I_a is dominant. With decreasing $V_{\rm GS}$, increased electronic potential diminishes I_a and thus I_b and I_c become important. In other words, $I_{\rm DS}$ in the subthreshold region results mainly from I_b and I_c for the nonoverlapped device. It is worth noting that carrier transport by I_c requires more thermal energy and may be suppressed under low temperature.

Fig. 7 shows the temperature sensitivity of $I_{\rm DS}$ $(\Delta\log(I_{\rm DS})/\Delta T)$ versus $V_{\rm GS}$ characteristics extracted from Figs. 2 and 3 under high and low temperatures. For the nonoverlapped device in the strong inversion region, the insensitive temperature dependence manifests the importance of I_a. On the other hand, the negative temperature dependence for the overlapped device in the strong inversion region indicates phonon scattering. In addition, it can be noted in Fig. 7(a) that $\Delta\log(I_{\rm DS})/\Delta T$ significantly increases with decreasing $V_{\rm GS}$ for both overlapped and nonoverlapped devices. This suggests that in the high temperature regime the subthreshold current of the nonoverlapped device is dominated by I_c, similar to the overlapped device. When temperature decreases, however, the thermionic emission I_c is suppressed and the I_b component with weak temperature dependence becomes dominant. In other words, the suppression of I_c under low temperature is the main reason of S saturation for the nonoverlapped device. It should be noted that such mechanism of S saturation is different from lateral tunneling through

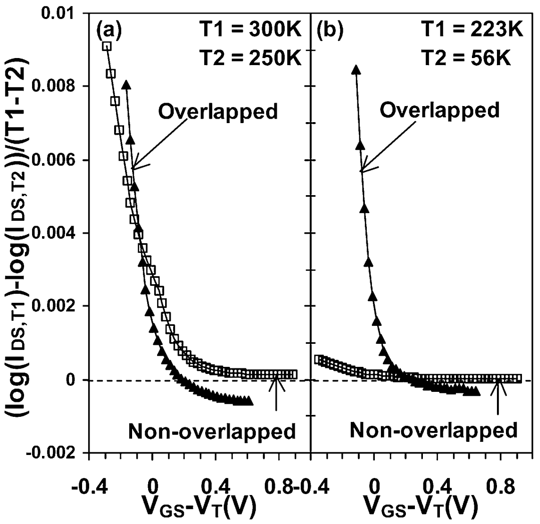

Fig. 7. Measured temperature sensitivity of drain current $(\Delta\log(I_{\rm DS})/\Delta T)$ versus $(V_{\rm GS}-V_T)$ characteristics for overlapped and nonoverlapped devices under (a) high temperature, T = 300 to 250 K and (b) low temperature, T = 223 to 56 K.

the channel, as presented for ultrashort devices in [12] and [17].

Fig. 6 also shows an equivalent quantum well under the gate in the nonoverlapped device [12]. It is worth noting that the height of the voltage-controlled potential barriers in the nonoverlapped regions increases with $V_{\rm GS}$. The consequence is the plausibility of electron-wave confined between the barriers. When the length of the quantum well, d, is smaller than the inelastic-scattering (e.g., phonon scattering) length, the phase-coherent electron wavefunction over the entire channel as well as quantum interference between coherent electron waves occur. The quantum interference enhances the electron backscattering probability [9], [10] and thereby reduces the conductivity expected classically. Such quantum correction to the conductivity is the weak localization effect [9], [10] and logarithmically dependent on temperature as $\Delta\sigma = (pe^2/\pi h)\ln(T)$, where the value of p depends on the scattering process. When T = 56 K, the carriers at $V_{\rm DS} = 50$ mV experience more heating (more phonon scattering) and thus less localization effect than those at $V_{\rm DS} = 1$ or 2 mV. Therefore, the $G_{\rm DS}$ measured at $V_{\rm DS} = 50$ mV is larger than that at $V_{\rm DS} = 1$ or 2 mV (Fig. 5). From the $G_{\rm DS}$ data at $V_{\rm DS} = 2$ mV under $T = 56$ K and 223 K in Fig. 5, we can estimate that $p \approx 1$, which is close to the results in [11] for the 2-D electron gas in Si MOSFETs.

The quantum-mechanical interference for an electron wave passing through a quantum well also results in oscillating transmission probability, *Tr*, as [14]

$$Tr = \left|\frac{\exp(-ik_1 d)}{\cos(k_2 d) - i(\omega/2)\sin(k_2 d)}\right|^2 \tag{1}$$

where $\omega = k_1/k_2 + k_2/k_1, k_1$ and k_2 are the wave vectors in the nonoverlapped region and in the quantum well, respectively. The wave vectors are determined from

$$k_1 = \sqrt{2m(E - eV_p)}/\hbar \tag{2}$$

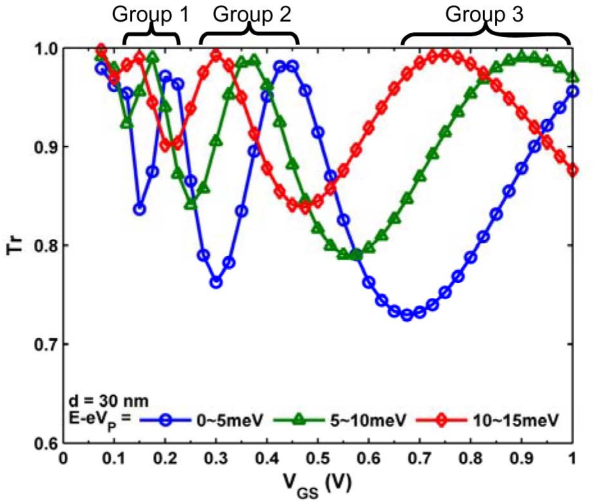

Fig. 8. Calculated transmission probability *Tr* versus $V_{\rm GS}$ for $d = 30$ nm and $E - eV^p = 0$–5, 5–10, and 10–15 meV.

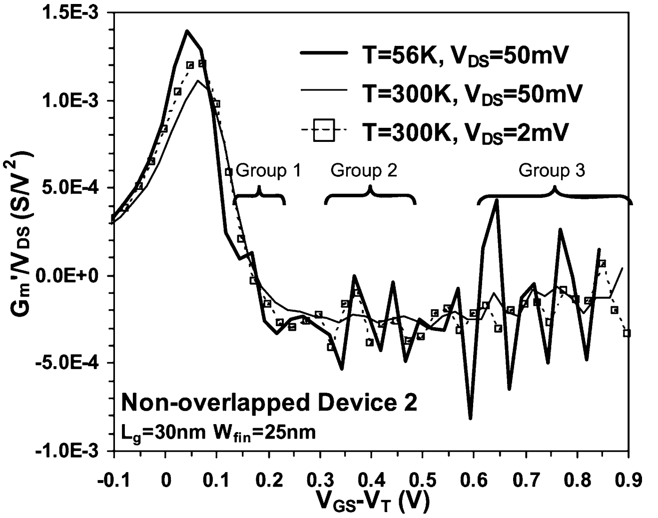

Fig. 9. Measured $G'_m/V_{\rm DS}$ versus $(V_{\rm GS}-V_T)$ characteristics for the nonoverlapped device 2 with $L_g = 30$ nm and $W_{\rm fin} = 25$ nm at various $V_{\rm DS}$ and temperature. $(G'_m = dG_m/dV_{\rm GS}$ and $G_m = dI_{\rm DS}/dV_{\rm GS})$.

$$k_2 = \sqrt{2m(E - eV_c)}/\hbar \tag{3}$$

where m and E are the effective mass and energy of the electron. Fig. 8 shows the calculated *Tr* for the quantum well in Fig. 6. The values of d and $(E - eV_p)$ used in Fig. 8 are based on our experiments. It is worth noting that the *Tr* oscillation becomes obvious with increasing $V_{\rm GS}$ as well as the depth of the quantum well. From the *Tr* calculation based on $d = 30$ nm and $(E - eV_p) = 0 - 5$ meV (Fig. 8), we can observe three transmission maxima due to constructive interference (i.e., *Tr* = 1) at $V_{\rm GS} \approx 0.2$, 0.43, and 1 V. When $(E - eV_p)$ increases, we observed smaller *Tr* oscillations and shifts in the corresponding transmission maximum. In other words, the electron energy distribution may result in group-like *Tr* oscillations as shown in the groups 1–3 of Fig. 8. We found that such group-like fluctuations can also be seen in the $G'_m\,(G'_m = dG_m/dV_{\rm GS},\ G_m = dI_{\rm DS}/dV_{\rm GS})$ characteristics in

Fig. 9 as well as in the G_{DS} characteristics shown in Fig. 5(a). We have noted that nearly every peak in G'_m (Fig. 9) can correspond to the peak in G_{DS} [Fig. 5(a)]. It is worth noting that the G'_m oscillation of Group 3 is more significant and wider than that of groups 1 and 2, which is consistent with the simulation results in Fig. 8. Remind that both the potential barrier height in Fig. 6 and G_{DS} fluctuations in Figs. 5 and 9 increase with V_{GS}. For devices with the same size, similar G'_m oscillations can also be observed and have been presented in our previous study [15].

V. CONCLUSION

We have conducted a comparative study of carrier transport characteristics for MuGFETs with and without the nonoverlapped source/drain structure. For the overlapped devices, we observed Boltzmann law in subthreshold characteristics and phonon-limited behavior in the inversion regime. For the nonoverlapped devices, however, we found insensitive temperature dependence of I_{DS} in both subthreshold and inversion regimes. Our low-temperature measurements indicate that the intersubband scattering is the dominant carrier transport mechanism for narrow overlapped MuGFETs. For the nonoverlapped MuGFETs, the voltage-controlled potential barriers in the nonoverlapped regions may give rise to the weak localization effect (conductance reduction) and the quantum interference fluctuations.

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