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碩 士 論 文

適用於雙頻帶接收機前端電路之

共電流低雜訊放大器和低電壓微混頻器

Concurrent Dual-Band LNA For Dual-Band Receiver

Front-End and Low-Voltage Micromixer

研究生：顏欽賢

指導教授：周復芳　博士

中 華 民 國 九 十 四 年 六 月

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研究生：顏欽賢　　**Student：Chin Hsien Yen**

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中文摘要

本論文的第一部份分三個方面研究共電流雙頻帶低雜訊放大器電路設計方法，包含輸入匹配，雜訊指數，和功率消耗，並且以電路元件來表示這些特性。實作的共電流雙頻帶低雜訊放大器顯示在 2GHz 和 5.25GHz 分別有 7.45 dB 和 6.06 dB 的增益，-12.8 dB 和-12.9 dB 的輸入返回損耗，3.54 dB 和 4.80 dB 的雜訊指數，並且僅消耗 7.21mw 的低功率損耗。第二部份針對採用偶次諧波混頻器而只需單一頻率合成器的新式共電流雙頻帶接收機架構實作共電流雙頻帶接收機前端電路。此電路在 2.45GHz 和 5.25GHz 分別達到 17.2 dB 和 11.8 dB 的電壓增益，-15.9 dB 和-15.8 dB 的射頻端輸入返回損耗，及-21.0 dBm 和-15.3 dBm 的 P_{1dB}。第三個部份是操作在 1V 的 2.45GHz 低電壓微混頻器。此電路在 1.72mw 的低功率消耗下有 14.9 dB 的射頻端輸入返回損耗，8.28 dB 的轉換增益，-5.63 dBm 的 P_{1dB} 和 4.21 dBm 的 IIP3。本論文中的三顆晶片均使用標準 0.18um CMOS 製程設計和實作，並且在國家晶片系統設中心完成量測。

A Study of Concurrent Dual-Band LNA For Dual-Band Receiver Front-End

Student: Chin Hsien Yen Advisor: Dr. Christina F. Jou

Institute of Communication Engineering

National Chiao Tung University

Abstract

In the first part of the thesis the design method of concurrent dual-band LNA topology is studied and analyzed in three respects, including input matching, noise figure, and power dissipation. These characteristics are expressed in terms of circuit elements. The implemented concurrent dual-band LNA demonstrates 7.45 dB and 6.06 dB power gain, -12.8 dB and -12.9 dB input return loss, 3.54 dB and 4.80 dB noise figure at 2GHz and 5.25Gz, respectively, with low power consumption of 7.21mw. In the second part a concurrent dual-band receiver front-end for wireless LAN 802.11a/b/g applications is implemented base on the new concurrent dual-band receiver architecture which needs only one frequency synthesizer by employing sub-harmonic mixer. It achieves 17.2 dB and 11.8 dB voltage gain, -15.9 dB and -15.8 dB RF port input return loss, -21.0 dBm and -15.3 dBm P_{1dB} at 2.45GHz and 5.25GHz, respectively. The third part is the 2.45GHz low-voltage micromixer for 1V operation. It has 14.9 dB RF port return loss, 8.28 dB conversion voltage gain, -5.63 dBm P_{1dB}, and 4.21 dBm IIP3 with 1.72mw low power dissipation. The three ICs in this thesis are all designed and fabricated using CMOS 0.18um process and measured in National Chip Implementation Center (CIC).

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Chapter 1

Introduction

1.1 Motivation

Wireless communication has developed dramatically in recently years and extensively applied in many fields, such as telegram, phone, and radio. Recently integrated-circuit technology on fabrication brings new process and improved properties gradually. Wireless local area network (WLAN) or some interactive devices with wireless technique become popular since device technologies capable to produce high volumes at extremely low cost. System on chip (SOC) integration with complementary metal oxide semiconductor (CMOS) technology may potentially come true because of the requirement of low cost, low power dissipation and small chip size. The low-voltage circuit design also becomes important because of the low power requirement for portable products.

The multi-standard wireless LAN transceiver using CMOS technologies are becoming the major design because of the figures of low-cost and high-integrated. In the applications of wireless LAN, IEEE 802.11a and IEEE 802.11b/g use frequency bands of 5.15GHz~5.35GHz and 2.4GHz~2.4835GHz, respectively. Therefore a dual-band RF receiver front-end is needed for the integration of wireless LAN. The following thesis presents a concurrent dual-band LNA, a dual-band receiver front-end and a low-voltage micromixer for 1V operation. These circuits are simulated with EldoRF and fabricated using CMOS 0.18um process.

1.2 Thesis Organization

This thesis discusses about the analysis and design of concurrent dual-band LNA and a concurrent dual-band receiver front-end, in chapter 2 and chapter 3, respectively. A low-voltage CMOS micromixer is proposed in appendix A.

In chapter 2, first we introduce the design flow of concurrent dual-band LNA and analysis the characteristic of the circuit compared with single-band LNA. The input matching, noise figure and power dissipation of single-band and dual-and LNA are expressed in terms of circuit elements in section 2.3 and 2.4. Also the experimental results, discussions and circuit comparisons are also presented in the chapter.

In chapter 3, a concurrent dual-band receiver front-end with low-IF architecture for wireless LAN 802.11a/b/g applications is designed and implemented. We will start from the wireless local-area-network (LAN) standards, which occupies the dual frequency bands near 2.45GHz and 5.25GHz, in section 3.1. In section 3.3 we propose a new concurrent dual-band receiver architecture with only one frequency synthesizer. Then we present a concurrent dual-band receiver front-end designed for this architecture. The design details of the front-end which consists of a concurrent dual-band LNA, a sub-harmonic mixer and a Gilbert-cell mixer, and experimental results are presented in section 3.3 and 3.4.

In chapter 4, we propose a low-voltage micromixer. Firstly we review the topology and operation theory of basic micromixer in section 4.1. The proposed low-voltage CMOS micromixer is presented in 4.2. Section 4.3 discusses layout and measurement considerations of micromixer. Finally, the experimental results and comparisons are presented in 4.4 and 4.5.

In chapter 5 these works are summarized and concluded. Also, there is some future work.

Chapter 2

Concurrent Dual-Band Low-Noise Amplifier

2.1 Introduction

As wireless applications become popular, demands for RF circuits which can support multiple band standards are rapidly increasing. These demands are typically addressed by having two or three sets of key RF blocks which can handle the bands, for example, the architecture shown in Figure 2.1.1[1]. These increases die area, the number of components, and the overall foot print, which in turn increases cost [2]. Two ways to solve these problems are wideband and multi-band structures. Wideband circuits are more sensitive to out-of-band signals due to nonlinearity of transistors [3]. Therefore we choose the dual-band structure, one set of RF blocks which can operate for multiple bands, as the system solution. In the applications of wireless local-area-network (LAN), IEEE 802.11a and IEEE 802.11b/g use frequency bands of 5.15GHz~5.35GHz and 2.4GHz~2.4835GHz, respectively. To integrate the two bands into a single receiver, a dual-band wireless LAN transceiver using CMOS technologies are becoming the major design because of the figures of low-cost and high-integrated. We propose a new concurrent dual-band receiver operating at 2.45GHz and 5.25GHz [4], as shown in Figure 2.1.2. To implement the receiver, a concurrent dual-band low-noise amplifier is firstly studied and designed here. In this chapter we try to analysis the concurrent dual-band LNA by deriving the input

matching, noise figure, and power dissipation in terms of circuit elements. The analysis of single-band LNA is also reviewed to make a comparison clearly for the readers.

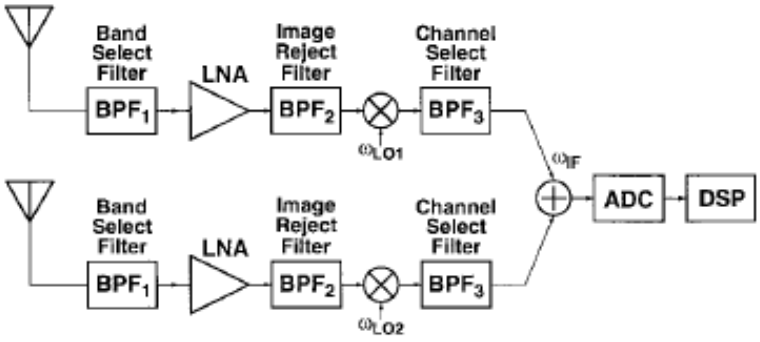


Figure 2.1.1 Traditional dual-band receiver with two individual paths

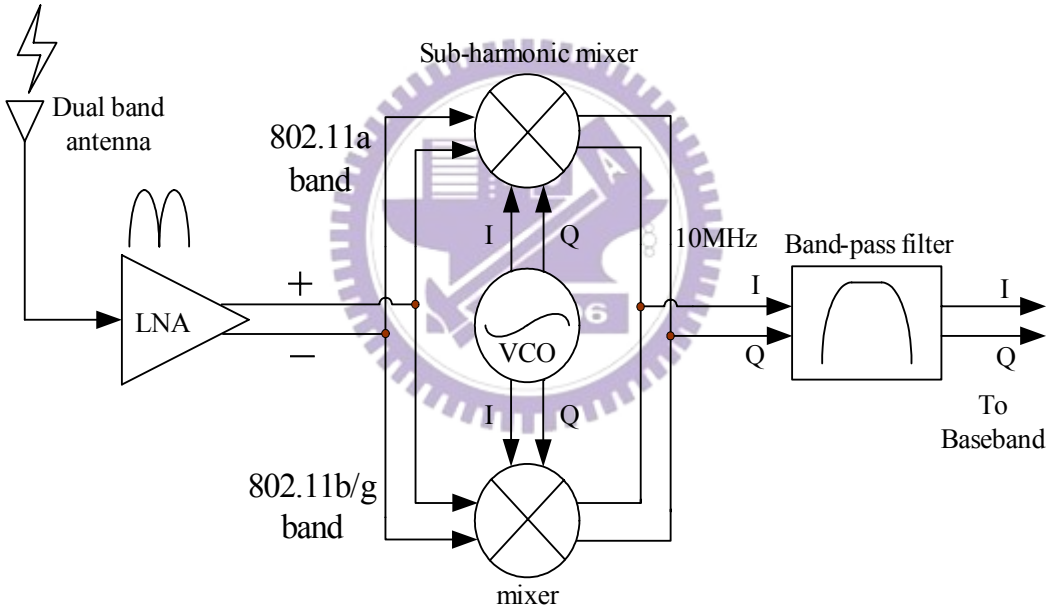


Figure 2.1.2 Concurrent Dual-band receiver block diagram

2.2 Architecture

The architecture of the concurrent dual-band LNA is shown in Figure 2.2.1. To minimize the power dissipation and to improve the linearity, the single-stage is

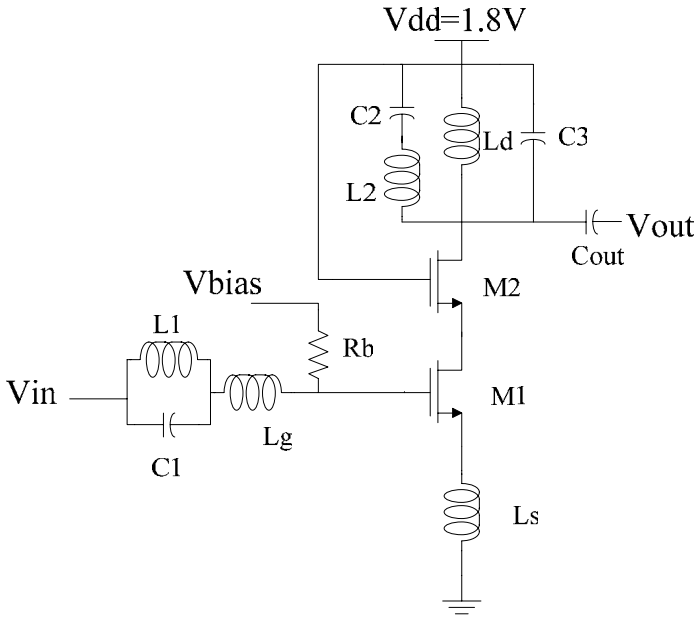


Figure 2.2.1 Schematic of the dual-band LNA

accepted. A cascode configuration is used for better reverse isolation [5]. In detail, the common gate, M2, plays two important roles in the LNA [6].

(1) It improves the stability of the circuit by minimizing the feedback from the output to the input.

(2) It lowers the LO leakage produced by the following mixer.

To achieve both the input and noise matching simultaneously the inductive degeneration topology is used. The differences between single-band LNA and dual-band one are an excess LC tank (L_1 and C_1) and LC branch (L_2 and C_2) at the gate of M_1 and the drain of M_2. The LC tank resonate the gate impedance, providing the dual-band input matching. The LC branch introduces a zero in the transfer function of the LNA and performs a notch between 2.45GHz and 5.25GHz to improve the receiver's image rejection [7]. Typically both the input and output impedance are designed to be 50Ω for measurement consideration.

The first step in designing the LNA is to determine the optimum MOS transistor size in the input stage. An expression of the width of the optimum size can be found in [8]：

$$W_{opt} = \frac{3}{2}\frac{1}{\omega L C_{OX} R_S Q_{SP}} \approx \frac{1}{3\omega L C_{OX} R_S} \qquad (2.1)$$

Therefore we can find the optimum size is about 280um and 130um for 2.45GHz and 5.25GHz, respectively. Owing to have better performance at two frequencies, the optimum size is chosen between that at 2.45GHz and at 5.25GHz. The following two sections we discuss some circuit performances in single-band LNA and dual-band LNA.

2.3 A Review of Single-Band LNA

The theoretical analysis of single-band LNA with inductive degeneration structure is available in some masterpiece RF textbooks [8]. To help the designer understand the operation mechanism of the single-band LNA, the formulas have been transfer to the new forms in terms of the circuit elements [9]. These formulas, including input matching, noise figure and power dissipation, are reviewed in summary here. Figure 2.3.1 is the traditional single-band cascode LNA with inductive degeneration structure. The following analysis is based on this circuit. These will be the basis of the analytic method of the dual-band LNA in next section.

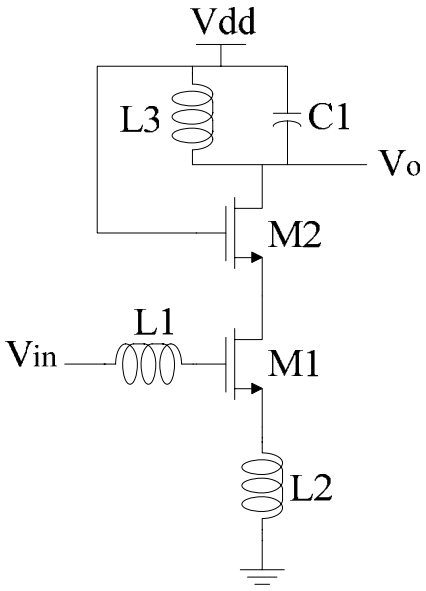


Figure 2.3.1 Traditional single-band low-noise amplifier

2.3.1 Input Matching

Figure 2.3.2 is the small-signal equivalent circuit of the single-band LNA. Applying KVL to the input loop in Figure 2.3.2 we have

$$V_{in} = I_{in}\left(j\omega L_1 + j\omega L_2 \right) + I_{in}\left(\frac{1}{j\omega C_{gs}} \right) + I_o j\omega L_2 \tag{2.2}$$

Independently,

$$I_o = g_m V_{gs} = g_m I_{in} \frac{1}{j\omega C_{gs}} \tag{2.3}$$

Substituting equation (2.3) into equation (2.2) yields

$$V_{in} = I_{in}\left[j\omega\left(L_1 + L_2 \right) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_2}{C_{gs}} \right] \tag{2.4}$$

Therefore,

$$Z_{in} = \frac{V_{in}}{I_{in}} = j\omega\left(L_1 + L_2 \right) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_2}{C_{gs}} \tag{2.5}$$

For matching, Zin = Rs, and so

$$\omega_c\left(L_1 + L_2 \right) = \frac{1}{\omega_c C_{gs}} \tag{2.6}$$

and

$$R_s = \frac{g_m}{C_{gs}} L_2 \tag{2.7}$$

From the preceding equation it can be seem that matching occurs only at

$$\omega_c = \frac{1}{\sqrt{\left(L_1 + L_2 \right) C_{gs}}} \tag{2.8}$$

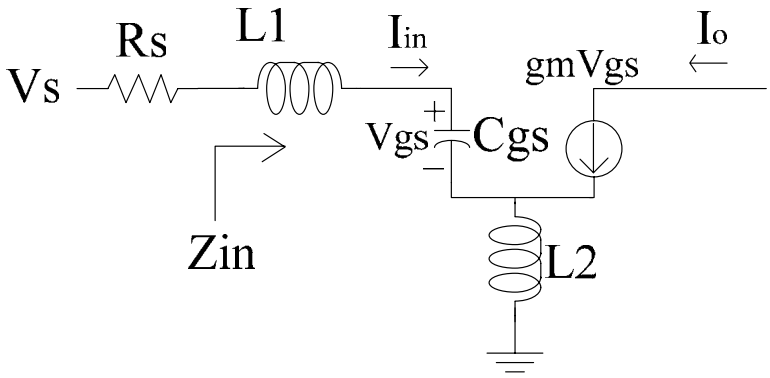


Figure 2.3.2 Small signal equivalent circuit of the single-band LNA

2.3.2 Noise Figure

It is well-known that the noise figure of any cascade network is dominated by the first stage due to the Friis formula, then we assume that the noise is dominated by the noise from M_1. We further assume that noise from M_1 is dominated by thermal noise of the drain current [9]. Figure 2.3.3 shows the small-signal equivalent circuit with noise generators. From the noise analysis in [9] the relationship of $\overline{v_i^2}$ and $\overline{i_d^2}$ has been derived as

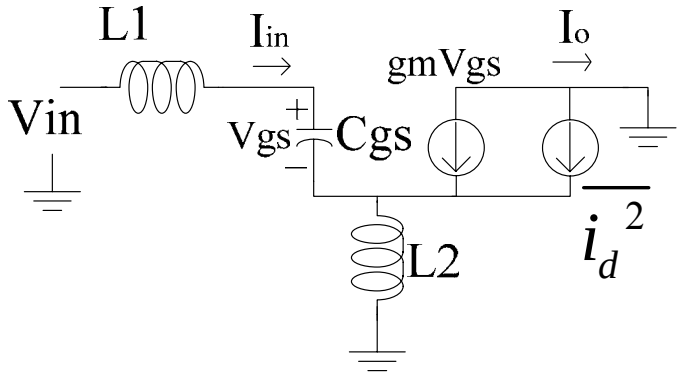


Figure 2.3.3 Small-signal equivalent circuit of single-band LNA with noise generators

$$\overline{v_i^2} = \frac{\overline{i_d^2}}{|G_m|^2} \tag{2.9}$$

where G_m denotes the transconductance of the whole amplifier. Also G_m has been derived in terms of V_{gs}, V_{in} and g_m as

$$G_m = g_m \frac{V_{in}}{V_{gs}} = g_m \frac{1}{Z_{in} j\omega C_{gs}} \tag{2.10}$$

So the noise of the single-band LNA can be expressed as

$$NF = \frac{N_{dev} + N_{in}}{N_{in}} = 1 + r\frac{(Z_{in}\omega C_{gs})^2}{g_m R_s} \tag{2.11}$$

At matching condition, equation (2.11) becomes

$$NF = 1 + \gamma \frac{R_s\left(\omega_c C_{gs}\right)^2}{g_m} = 1 + \frac{\gamma}{g_m Q^2 R_s} \tag{2.12}$$

where $Q = \frac{1}{R_s \omega_c C_{gs}}$ denotes the quality factor of the input series resonant circuit.

2.3.3 Power Dissipation

In this subsection, we derive the dependence of power dissipation on technology and circuit parameters under matching condition and for a given (V_{gs}-V_t) which is usually fixed for a design. First

$$P = I_D V_{DD} \tag{2.13}$$

where I_D is the drain current of M_1. Since M_1 operates in the saturation region, we have the equation

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_T\right)^2 \tag{2.14}$$

Therefore we get

$$P \propto \mu C_{ox}\frac{W}{L} \tag{2.15}$$

From $C_{gs} = \frac{2}{3} WLC_{ox}$ and $g_m = \mu C_{ox} \frac{W}{L}(V_{GS} - V_T) \propto \mu C_{ox} \frac{W}{L}$, we have

$$P \propto \mu C_{ox} \frac{W}{L} \propto \frac{{g_m}^2}{C_{gs}} \frac{L^2}{\mu} \tag{2.16}$$

Furthermore, under matching condition $C_{gs} = \frac{1}{\omega_c^2} \frac{1}{(L_1 + L_2)}$, which is derived from equation (2.6), and $g_m = \frac{R_s C_{gs}}{L_2}$, which is derived from equation (2.7), we have

$$P \propto \frac{L^2}{\mu} \left(\frac{R_s}{\omega_c} \right)^2 \frac{1}{L_2^3 \left(1 + \frac{L_1}{L_2} \right)} \tag{2.17}$$

where L and μ are technology parameters, R_S and ω_c are constant in a certain design, and others are circuit parameters.

2.4 Analysis of Concurrent Dual-Band LNA

The concurrent dual-band LNA has been discussed and analyzed in recent years. [3,7] Of course the circuit analysis and noise model are also been established in some published papers. However these analyses are less helpful when designing the circuits because of the unreadable equations. In this section we try to derive some formulas using the methods used in the single band LNA. The input matching, noise figure and power dissipation are analyzed in terms of circuit elements under the two assumptions described in last section [10]. Some simulations are performed in this section to prove the analysis equations. Under these equations we kindly hope the designers could have strong impressions how to link the elements and the circuit performance, even inspire the motivation for some readers to study the more difficult theoretical circuit analysis about dual-band LNA derived in the above-mentioned papers.

2.4.1 Input Matching

Figure 2.4.1 shows the small-signal equivalent circuit of dual-band LNA. Applying KCL to the input loop in Figure 2.4.1 the input impedance can be derived as following

$$Z_{in}=\frac{sL_1}{1-\omega^2 L_1 C_1}+s\left(L_g+L_s\right)+\frac{1}{sC_{gs}}+R_G+g_m\frac{L_s}{C_{gs}} \tag{2.18}$$

where R_G denote the gate distributed resistance of M_1. The input impedance is designed to match 50Ω at both resonance frequency points of interest:

$$R_G+g_m\frac{L_s}{C_{gs}}=R_s \tag{2.19}$$

$$\frac{sL_1}{1-\omega^2 L_1 C_1}+s\left(L_g+L_s\right)+\frac{1}{sC_{gs}}=0 \tag{2.20}$$

Solving equation (2.20), the two frequency points of interest can be obtained as

$$\omega_1=\left(\frac{X+\sqrt{X^2+Y}}{2\left(L_g+L_s\right)L_1 C_{gs} C_1}\right)^{1/2} \quad \omega 2=\left(\frac{X-\sqrt{X^2+Y}}{2\left(L_g+L_s\right)L_1 C_{gs} C_1}\right)^{1/2}$$

where X denotes $L_1C_{gs}+L_gC_{gs}+L_sC_{gs}+L_1C_1$ and Y denotes $4\left(L_g+L_s\right)L_1C_{gs}C_1$.

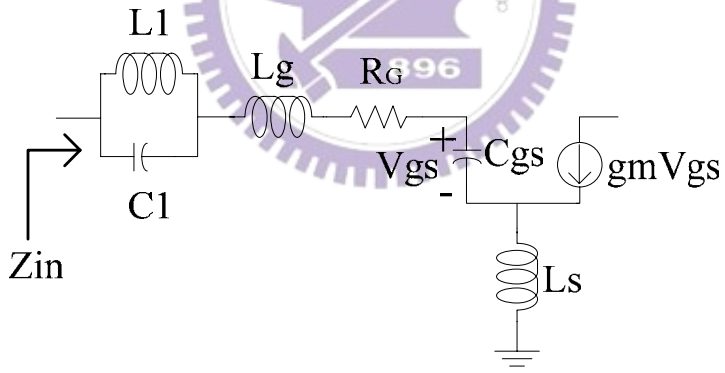


Figure 2.4.1 Small-signal equivalent circuit of dual-band LNA

2.4.2 Noise Figure

Now we try to analysis a dual-band low noise amplifier in the similar way shown in subsection 2.3.2. The small-signal equivalent circuit of dual-band LNA with noise generator is shown in Figure 2.4.2. Figure 2.4.3 represents Figure 2.4.2 with input-referred noise voltage $\overline{v_i^2}$ and current $\overline{i_i^2}$ at the input, followed by a noiseless

small-signal model of the amplifier with transconductance G_m.

First of all it is easy to prove that equation (2.11) is also suitable for dual-band LNA. The equation tells us that (NF-1) is proportional to $(Z_{in} \cdot \omega)^2$. In order to find the effect of finite Q inductor on noise, we take the series parasitic resistance of L_1, which is represented as R_1 , into consideration. Therefore the quality factor of L_1, Q_1can be expressed as

$$Q_1 = \frac{\omega_c L_1}{R_1} \tag{2.21}$$

The not-quite-parallel RLC tank composed of R_1, L_1 and C_1 can be converted to a purely parallel RLC tank composed of R_P, L_P and C_P with the quality factor Q_1 as shown in Figure 2.4.4 [8]. The input impedance can be derived as

$$Z_{in} = Z_{in,p} + j\omega L_g + R_G + \frac{1}{j\omega C_{gs}} + j\omega L_s + g_m \frac{L_s}{C_{gs}} \tag{2.22}$$

where $Z_{in,p}$ = the impedance of parallel R_P L_P C_P

$$= \left[\omega^2 R_p L_p^2 + j\left(\omega R_p^2 L_p - \omega^3 C_p R_p^2 L_p^2 \right) \right] / X_1$$

and $X_1 = \omega^4 R_p^2 L_p^2 C_p^2 + \omega^2 L_p^2 \left(1 - 2\frac{C_p}{L_p} R_p^2 \right) + R_p^2$

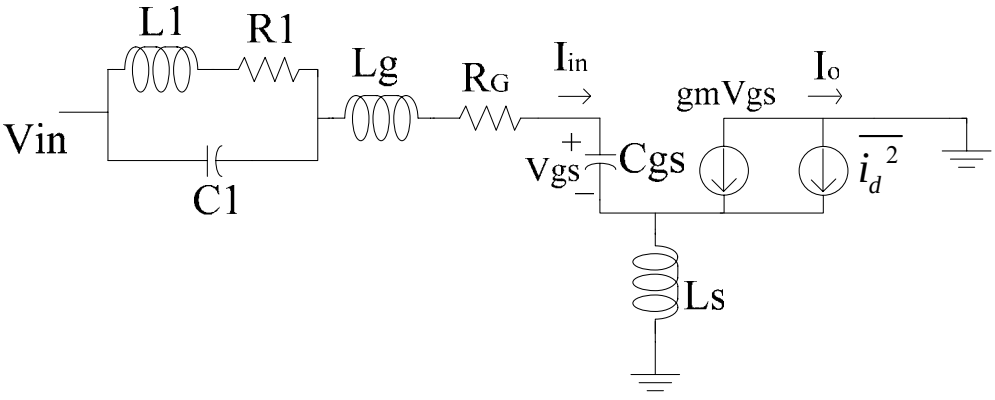


Figure 2.4.2 Small-signal equivalent circuit of dual-band LNA with noise generators

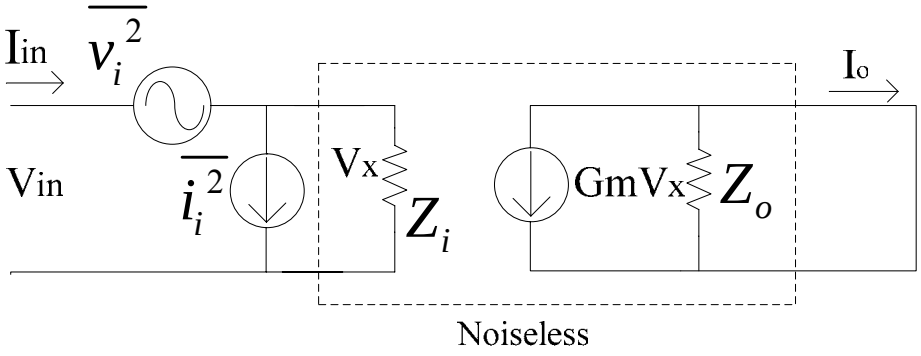


Figure 2.4.3 Representation of Figure 2.3.3 by two input noise generators

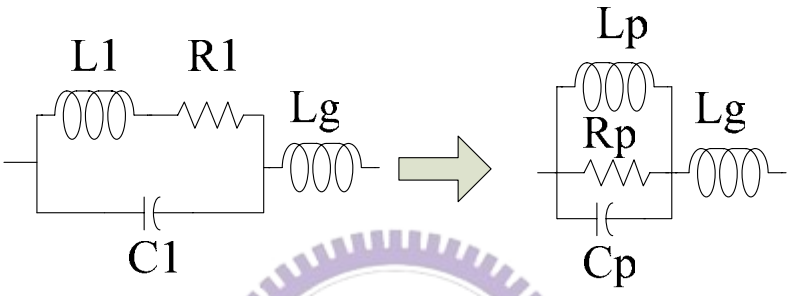


Figure 2.4.4 Purely parallel RLC tank

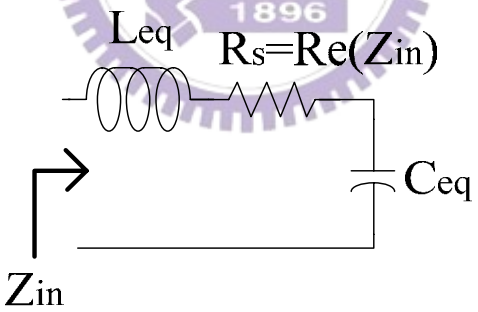


Figure 2.4.5 Input equivalent series RLC model

Also at matching condition, Z_{in} matches to R_S.

$$R_s = \mathrm{Re}\left(Z_{in}\right) = R_G + g_m \frac{L_s}{C_{gs}} + \frac{\omega^2 R_p L_p^2}{X_1} \tag{2.23}$$

$$L_{eq} = L_g + L_s + \frac{L_p R_p^2}{X_1} \tag{2.24}$$

$$\frac{1}{C_{eq}} = \frac{1}{C_{gs}} + \frac{\omega^4 C_p R_p^2 L_p^2}{X_1} \tag{2.25}$$

Hence we can redraw the input network in terms of R_S, L_{eq} and C_{eq}, as shown in Figure 2.4.5. The quality factor Q_{eq} of the input network can be derived as

$$\begin{aligned} Q_{eq} &= \frac{1}{R_s}\sqrt{L_{eq}C_{eq}} \\ &\approx \frac{1}{R_s\sqrt{C_{gs}}}\sqrt{L_g + L_s + \frac{L_1}{\omega_c^2 \frac{L_1^2}{R_1^2}\frac{1}{Q_1^2} - 2\omega^2 L_1 C_1 + 1}} \end{aligned} \tag{2.26}$$

From equation (2.10), we have the relationship of V_{in} and V_{gs} as

$$\frac{V_{in}}{V_{gs}} = \frac{1}{Z_{in} j\omega C_{gs}} = \frac{G_m}{g_m} \tag{2.27}$$

For matching condition, we can rewrite equation (2.27) as

$$\frac{V_{gs}}{V_{in}} = \frac{1}{R_s j\omega_c C_{gs}} = \frac{G_m}{g_m} \tag{2.28}$$

Now we try to express ω_c in terms of Q_{eq} and C_{eq}.

$$\omega_c = \frac{1}{\sqrt{L_{eq}C_{eq}}} = \frac{1}{C_{eq}\sqrt{\frac{L_{eq}}{C_{eq}}}} = \frac{1}{C_{eq}}\frac{1}{Q_{eq}R_{eq}} = \frac{1}{C_{eq}Q_{eq}R_s} \tag{2.29}$$

Submitting equation (2.29) into equation (2.28), we have

$$\frac{V_{gs}}{V_{in}} = \frac{Q_{eq}C_{eq}}{jC_{gs}} \tag{2.30}$$

which implies equation (2.31)

$$G_m^2 = \left(\frac{Q_{eq}C_{eq}}{C_{gs}}\right)^2 g_m^2 \tag{2.31}$$

Again submitting equation (2.31) into equation (2.9), we can get

$$\overline{v_i^2} = \frac{4kT\gamma g_m \Delta f}{G_m^{\ 2}} = \frac{4kT\gamma g_m \Delta f}{g_m^{\ 2} Q_{eq}^2 (C_{eq}/C_{gs})^2} \tag{2.32}$$

Finally the noise figure can be derived from (2.11) with $N_{dev} = \frac{\overline{v_i^2}}{\Delta f}$ as

$$NF = 1 + \frac{N_{dev}}{N_{in}} = 1 + \frac{\frac{\overline{v_i^2}}{\Delta f}}{4kTR_s} = 1 + \frac{\gamma}{g_m R_s Q_{eq}^2} \frac{C_{gs}^2}{C_{eq}^2} \approx 1 + \frac{\gamma}{g_m R_s Q_{eq}^2} \tag{2.33}$$

$$= 1 + \frac{\gamma R_s C_{gs}}{g_m (L_g + L_s + \frac{L_1}{\omega_c^{\ 2} \frac{L_1^2}{R_1^2} \frac{1}{Q_1^{\ 2}} - 2\omega_c L_1 C_1 + 1})}$$

The noise figure of dual-band low-noise amplifier in equation (2.33) has a similar form to that of a single-band one in equation (2.12). The design concept that noise figure can be reduced by improving the quality factor of input matching series RLC tank, Q_{eq} , under matching condition works in dual-band LNA design as well as in single-band one. Moreover we can improve Q_{eq} by choosing inductor L_1 with better Q_1. To illustrate this in practice, we simulate the noise figure of the dual-band LNA with three inductors L_1, which have Q-factor from 10 to 40. It can be seen in Figure 2.4.6 that the noise figure can be improved with better Q_1.

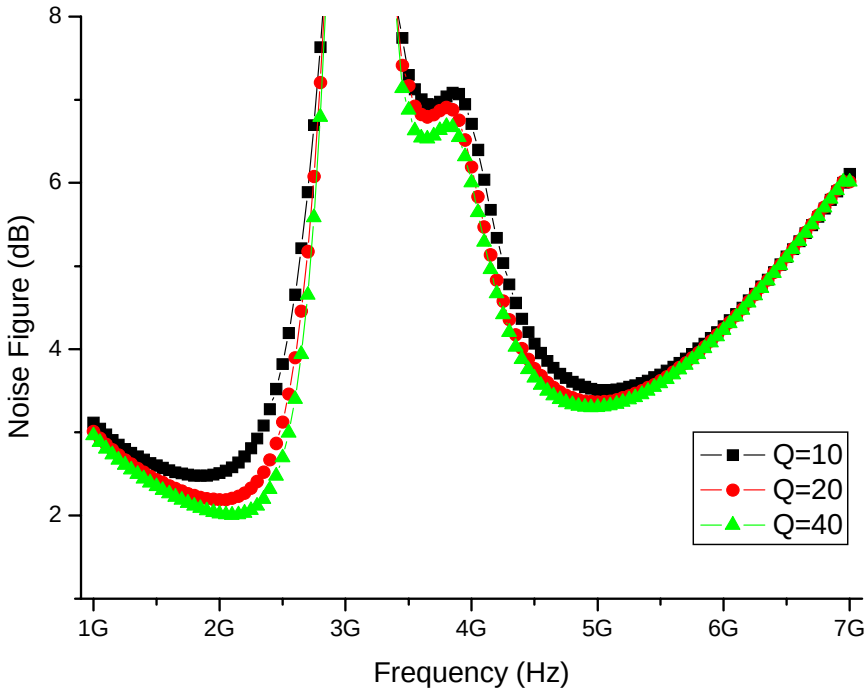


Figure 2.4.6 Simulation result of noise figure under different Q_1

2.4.3 Power Dissipation

In this section, we will derive the dependence of power dissipation in the similar method used in 2.3.3. Under matching condition of dual-band LNA, equation (2.20) which implies that

$$C_{gs} = \frac{1}{\omega_c^2\left(L_g + L_s + \dfrac{L_1}{1-\omega_c^2 L_1 C_1}\right)} \tag{2.34}$$

Also, from equation (2.19) we can get

$$g_m = \frac{C_{gs}}{L_s}\left(R_s - R_G\right) \tag{2.35}$$

First substituting equation (2.35) into equation (2.16), we have

$$P \propto \left[\frac{C_{gs}}{L_S}\left(R_S - R_G\right)\right]^2 \frac{1}{C_{gs}}\frac{L^2}{\mu} = \frac{C_{gs}}{L_S^{\,2}}\left(R_S - R_G\right)^2 \frac{L^2}{\mu} \tag{2.36}$$

Finally substituting equation (2.32) into equation (2.36), we have

$$P \propto \frac{L^2}{\mu_n}\left(\frac{R_s - R_G}{\omega_c}\right)^2 \frac{1}{L_S^3\left(1+\frac{L_g}{L_S}+\frac{L_1}{L_S(1-\omega_c^2 L_1 C_1)}\right)} \qquad (2.37)$$

We get a similar result that the power dissipation is proportional to technology parameters, some standard constants and circuit parameters as equation (2.17). We can reduce the power dissipation by using larger L_S from the equation (2.37). The dual-band LNA circuit is to be simulated with three different inductors L_S. Figure 2.4.7 shows the relationship of the power dissipation of the dual-band LNA and the inductance of L_S. In deed the power dissipation can be reduced by increasing L_S. Moreover, the variance of L_S will affect the input impedance so the choice of L_S becomes the trade-off between power dissipation and input matching.

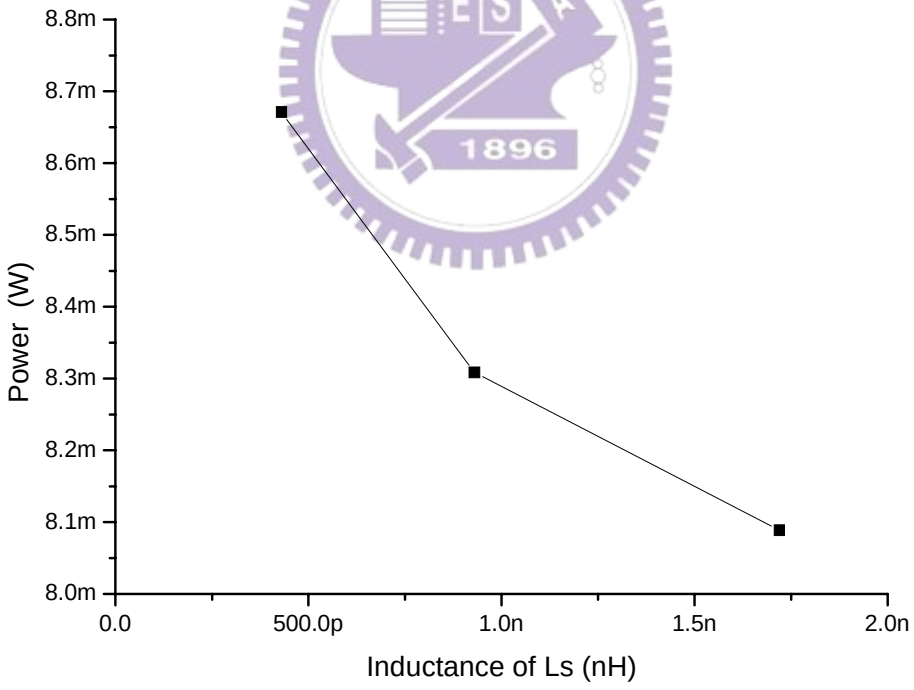


Figure 2.4.7 Simulation result of power dissipation under different L_S

2.5 Layout Considerations

The layout skill is very important for radio frequency circuit design because it may affect circuit performance very much. In this work we discuss three topics about the layout, the elements, the connections, and the element placement. To decrease noise the MOSFET is used as multi-finger, which is made of an array of 6 2.5μm/0.18μm MOSFETs. The 0.18μm (minimum) gate length was chosen to get the highest speed, and the 2.5μm gate width was chosen as a compromise between low polysilicon gate resistance and low drain/source contact resistance. The MIM (Metal-Insulator-Metal) capacitors without shield (the capacitance of per unit area $\approx 1 fF / \mu m^2$) and hexagonal spiral inductors (the Q-value is below 18) are used in this work. The poly without silicide resistance is used for gate bias. Guard-rings are added wit all elements to prevent substrate noise and interference. A shielded signal GSG pad structure is used in RF input and RF output to reduce the coupling noise from the noisy substrate.

As for the connection lines, the power lines are considered for the current density while the signal lines are designed as short as possible. All interconnections between elements are taken as a 45° corner. Last but not the least; the element placement also should be careful. Separate inductors away to decrease the mutual inductance. The RF input and the RF output are placed on opposite sides of the layout to avoid the high frequency signals coupling. The layout of the dual-band LNA is shown in Figure 2.5.1. The chip size is 1.32mm x 1.18mm. The chip photo is shown in Figure 2.5.2.

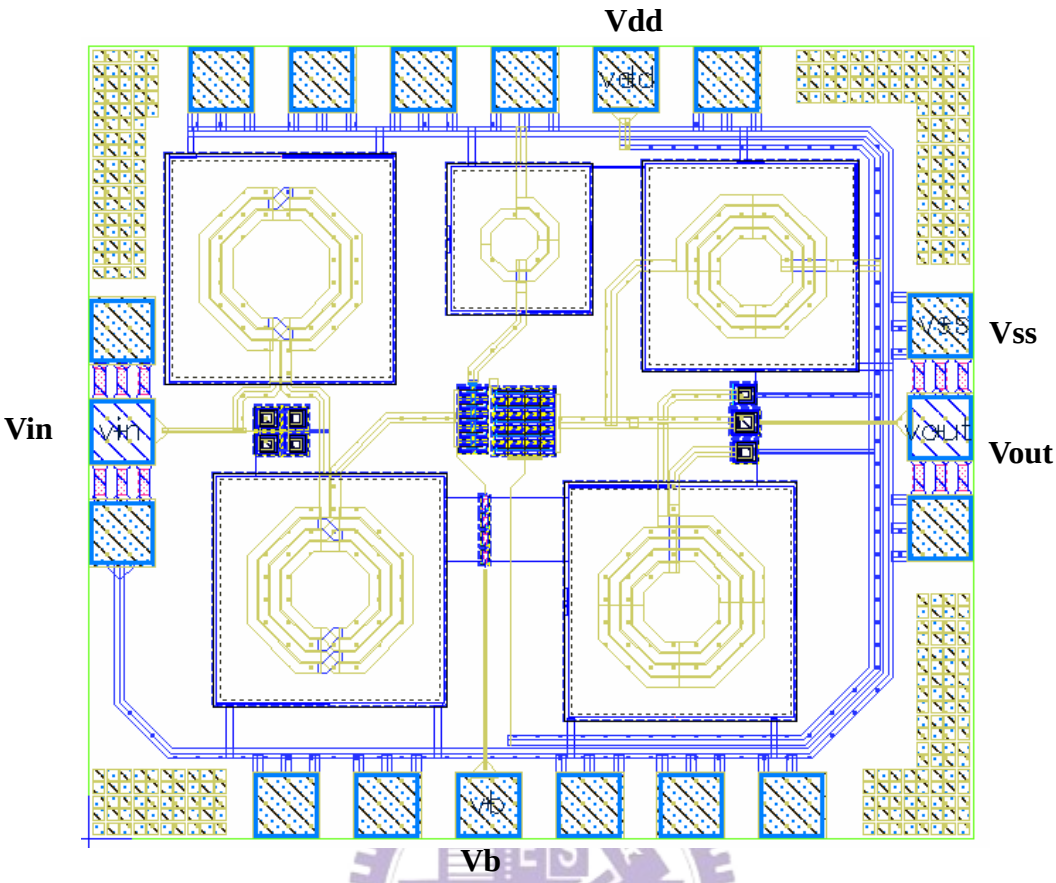


Figure 2.5.1 Layout of the dual-band LNA

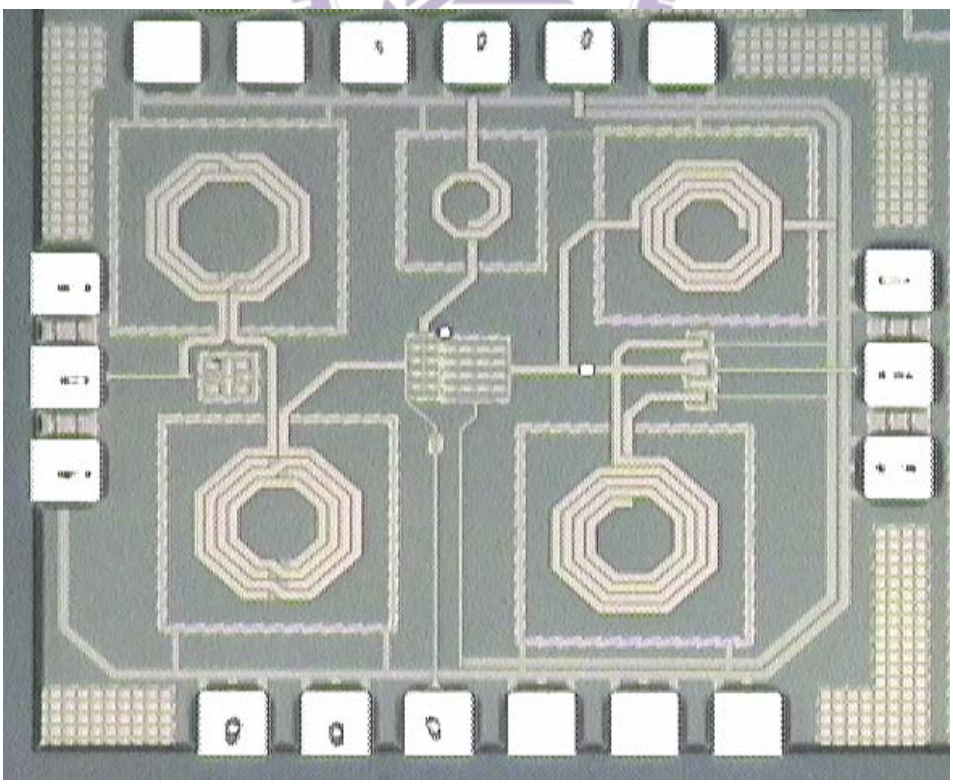


Figure 2.5.2 Chip Photo of the dual-band LNA

2.6 Measurement Considerations

The dual-band LNA is designed for on-wafer measurement so the layout must follow the rules of CIC (Chip Implementation Center)'s probe station testing rules. This circuit needs two 3-pin DC PGP probes and two RF GSG probes for on-wafer measurement. The correlative rules are illustrated in Figure 2.5.1. Some other rules about layout are that the minimum distance of RF pad and DC pad are 200 um and the minimum pad size is 80um x 80um [11]. Figure 2.6.2 shows the on-wafer measurement setup with four probes. The top and bottom probes are DC PGP probes which provide the power supply voltage and bias voltage for the circuit. The left and right probes are RF GSG probes. A large coupling capacitor is needed in the input of the dual-band LNA to isolate the dc between circuit and equipment. Figure 2.6.3 is the picture of the on-wafer measurement setup with four probes. Figure 2.6.4 ~ Figure 2.6.6 show the measurement setup for S-parameters, noise figure, 1dB compression point and third-order intercept point. We use the RF IC measurement system powered by LabView to measure the linearity of the dual-band LNA. We will discuss the experimental and testing results of this circuit in following sections.

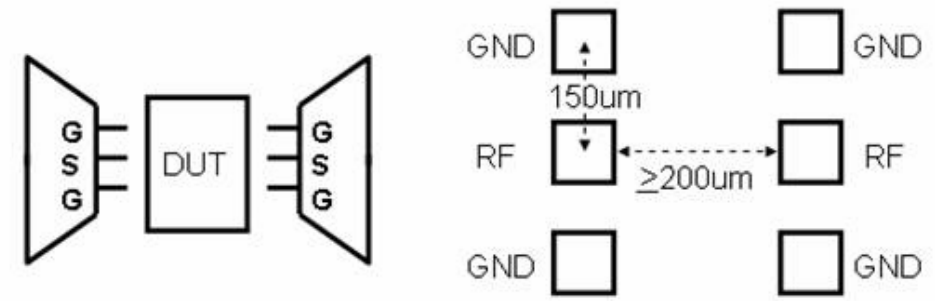


Figure 2.6.1 RF probe rules for measurement

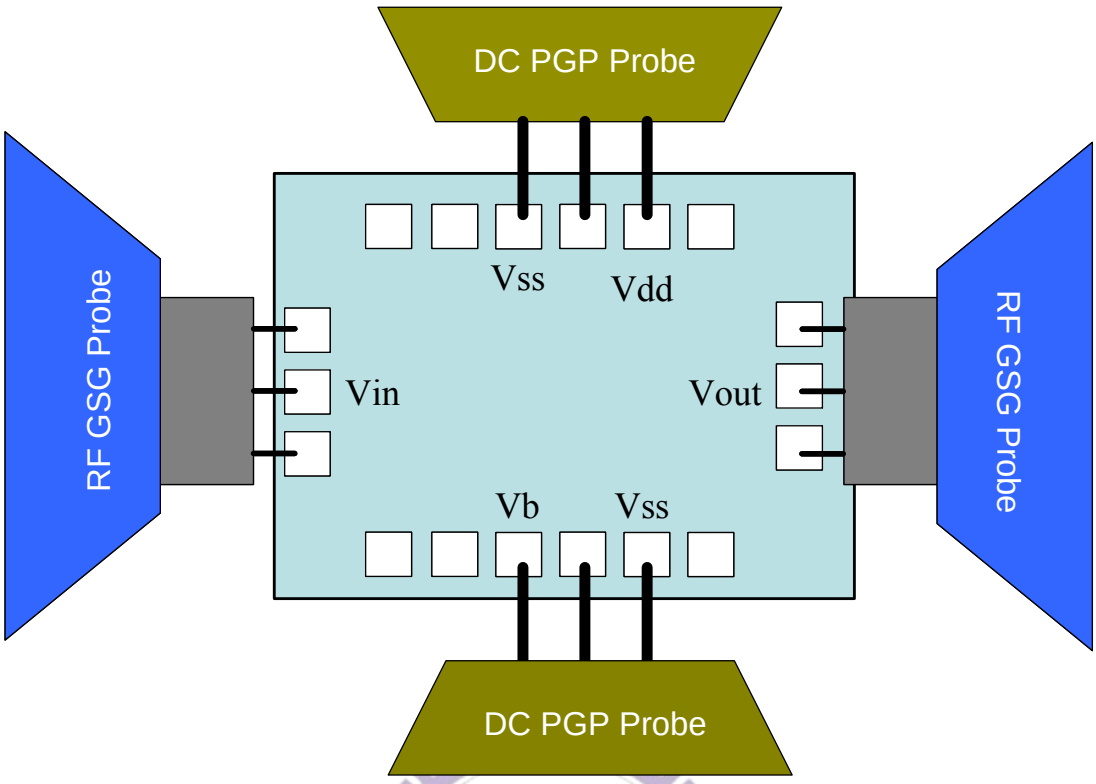


Figure 2.6.2 On-wafer measurement test diagram

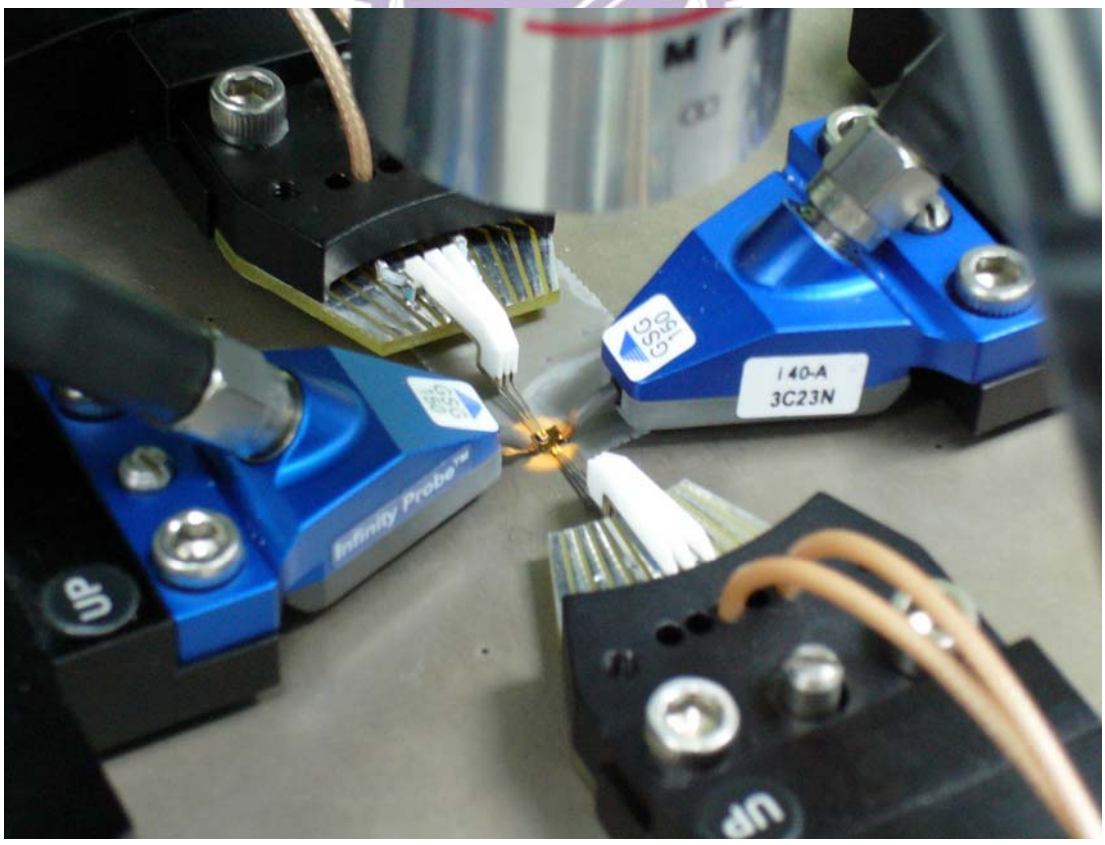
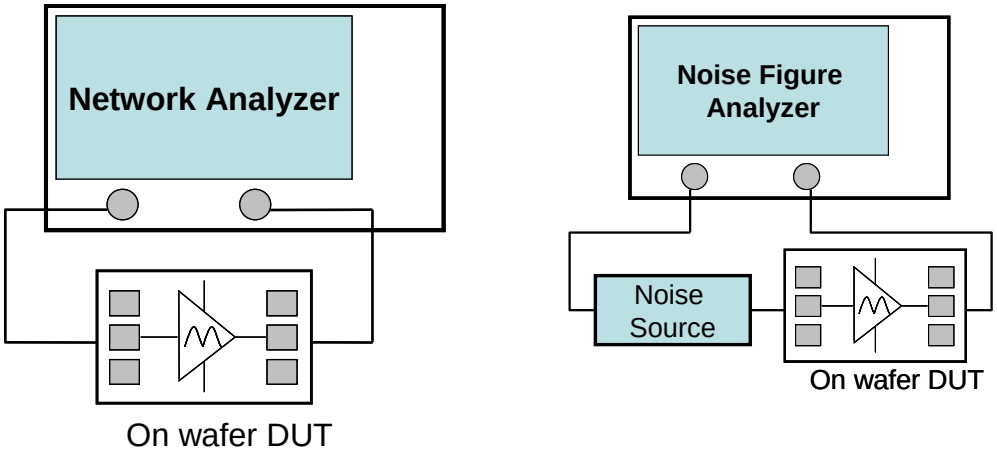


Figure 2.6.3 Picture of on wafer measurement setup with four probes



(a) (b)

Figure 2.6.4 Measurement setup for (a) S-parameters (b) noise figure

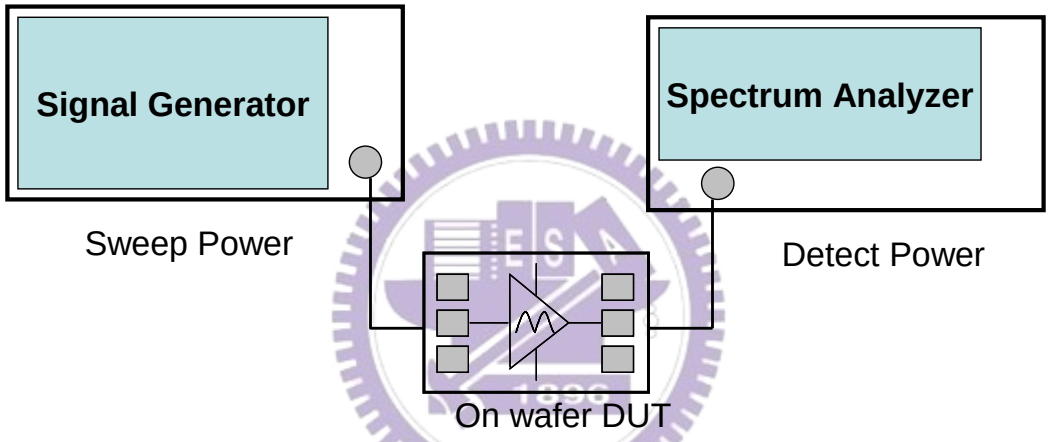


Figure 2.6.5 Measurement setup for 1 dB Compression Point

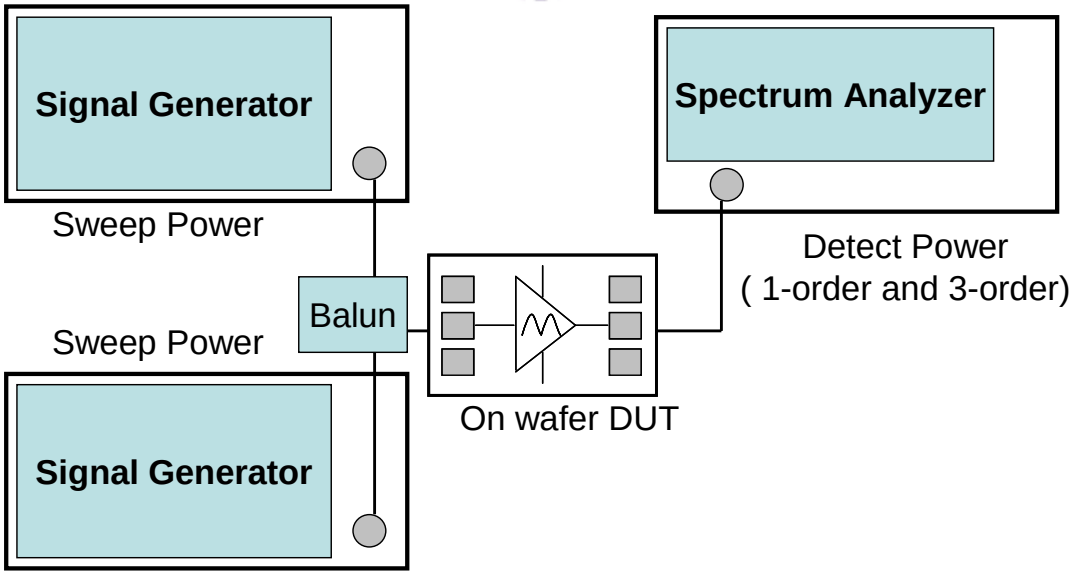


Figure 2.6.6 Measurement setup for third-order intercept point

2.7 Experimental Results and Discussions

The measured data reveals 7.45 dB and 6.06 dB power gain, -12.8 dB and -12.9 dB input return loss, 3.54 dB and 4.80 dB noise figure, -7.43 dBm and -9.66 dBm P_{1dB}, and 6.84 dBm and 2.76 dBm IIP3 at 2GHz and 5.25Gz, respectively. From Figure 2.7.1 ~ Figure 2.7.4, It can be observed that the lower band of the dual-band LNA designed at 2.45GHz was shifted to 2GHz around while the higher band designed at 5.25GHz is roughly matched with simulation. The measured results reveal the fact that the most difficult part of the design is to provide exact input and output matching at both bands simultaneously with on-chip passive components. In other words the matching performance is very sensitive to variation of passive components, like inductors and capacitors. Fortunately the circuit has a fairly performance at the shifted band compared to the lower band, so the measured results at the shifted band is compared with the simulated performance at the lower band in stead of the measured results at the original band. Surely the reason why the lower band is shifted to 2GHz is also discussed in this section by modifying the original simulation results. The modified simulation gives us a reasonable explanation the difference between simulation and measurement.

The measurement results reveal that the matching network of the dual-band LNA is not as well as what we expect, so we try to modify the simulation to fit the measurement results. We consider the ±10% variation of passive components while the size of the transistors is kept the same as original simulation. There are two reasons why we have to consider the variation of passive components though the physical models of the spiral inductors and MIM capacitors provided by the foundry were used in the simulation. First only some certain size of the spiral inductors are

measured and fitted. For example, the spiral inductor of W=15um, S=2um, R= 30um, 60um, 90um, 120um, and N=1.5, 3.5, 5.5 where W is the inductor track width, S is the spacing between tracks, R is the inner radius, and N is the number of turns. The inductance of the inductors whose size is not matched to the certain size is computed by interpolation or extrapolation using other measured physical models. For instance the spiral inductor L_1 with size of W=15um, S=2um, R=72um, and N=3 might be computed form the inductor models with sizes of W=15um, S=2um, R=60um, 90um, and N=1.5, 3.5. The variation of the spiral model would be unignorable if the measured models are not very accurate, especially for the matching network sensitive to passive components. The similar problem also hit the models of MIM capacitors. The other reason is the parasitic capacitors from metal lines to substrate can not be predicted precisely though the layout parasitic extraction (LPE) had been applied on the design proceedings of the circuit design.

According to the foregoing reasons we modified the dual-band LNA with variation of passive components to fit the measurement results. The comparisons of the simulation, measurement, and modified simulation results are shown in Figure 2.7.1 ~ Figure 2.7.9. These data are summarized in Table 2.7.1. The modified S-parameters are approximately fit to the measurement results in both frequency bands except for certain magnitude difference. This implies that the variation of passive components could course the shift of the frequency band. The measured linearity performances in both bands are better than modified simulation because of the degradation of the power gain. The measured noise figure is close to the modified simulation owing to the layout technique including the guard rings and shielding RF GSG pad. The measured results show the dual-band LNA achieves balanced performance at both the lower and higher band under low power consumption.

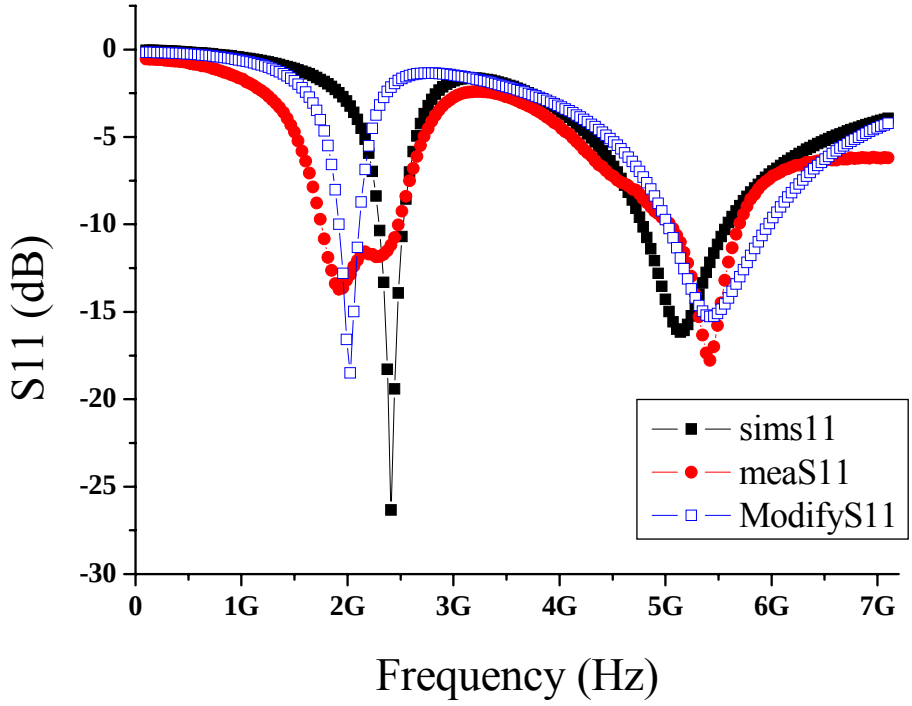


Figure 2.7.1 Comparison between simulation and measurement of S11

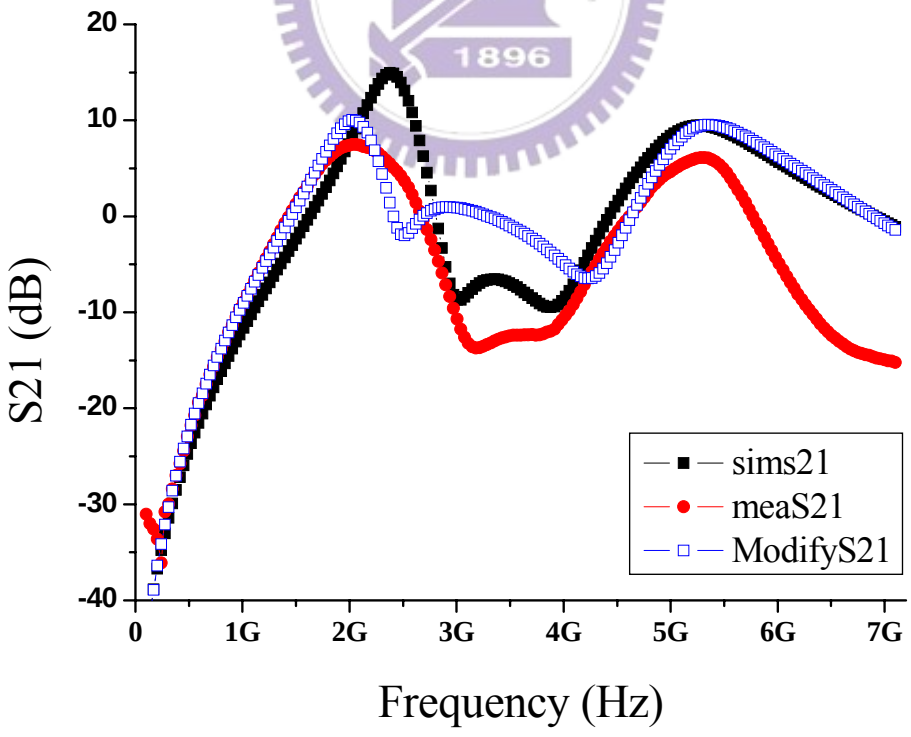


Figure 2.7.2 Comparison between simulation and measurement of S21

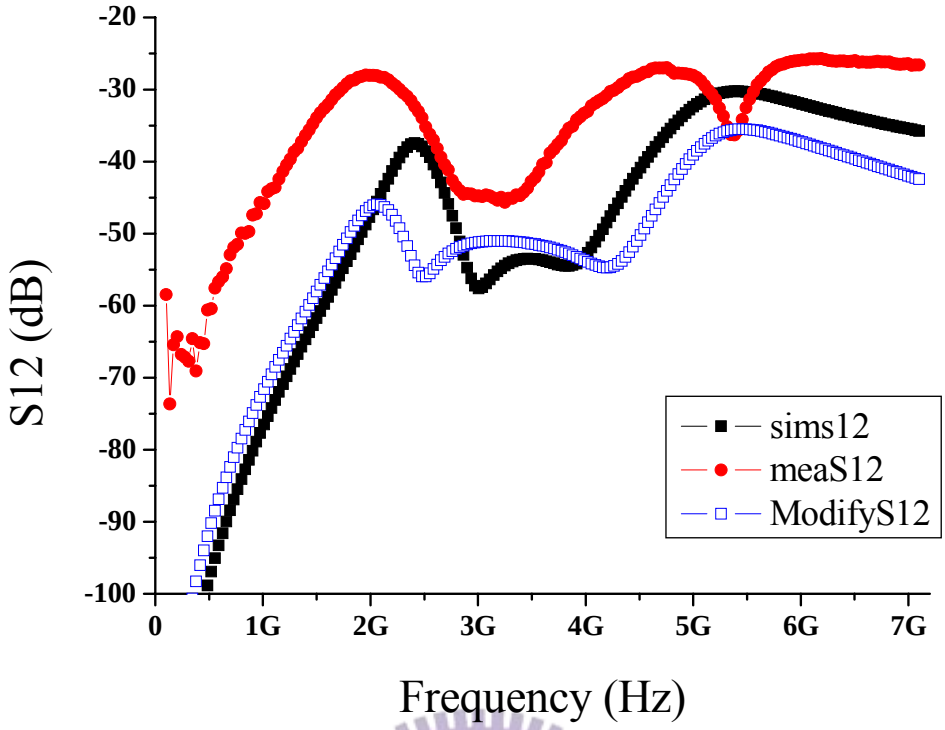


Figure 2.7.3 Comparison between simulation and measurement of S12

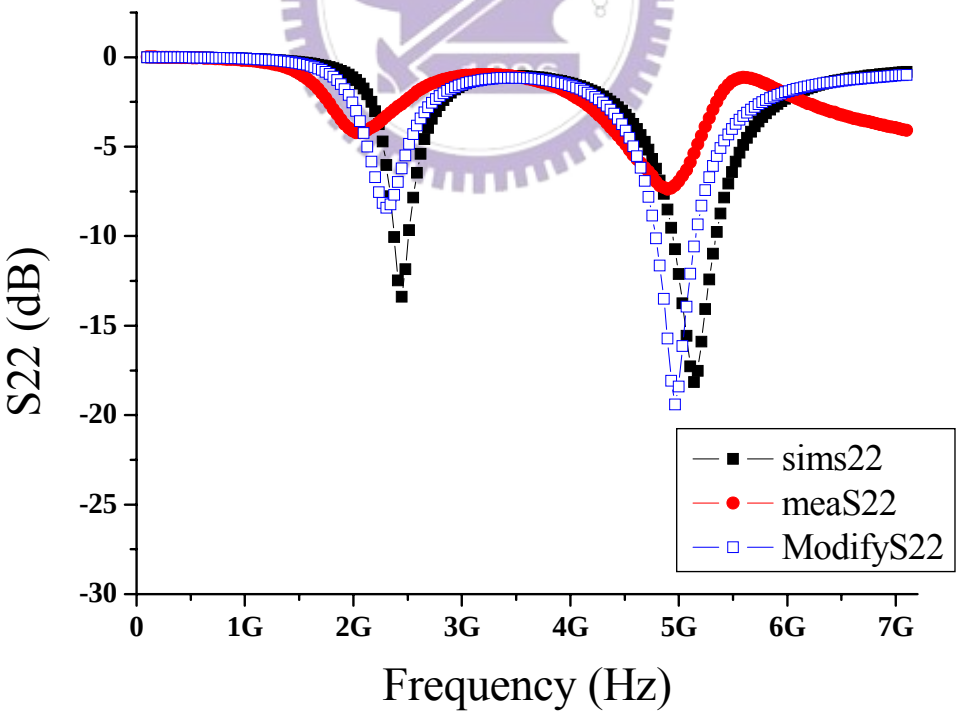


Figure 2.7.4 Comparison between simulation and measurement of S22

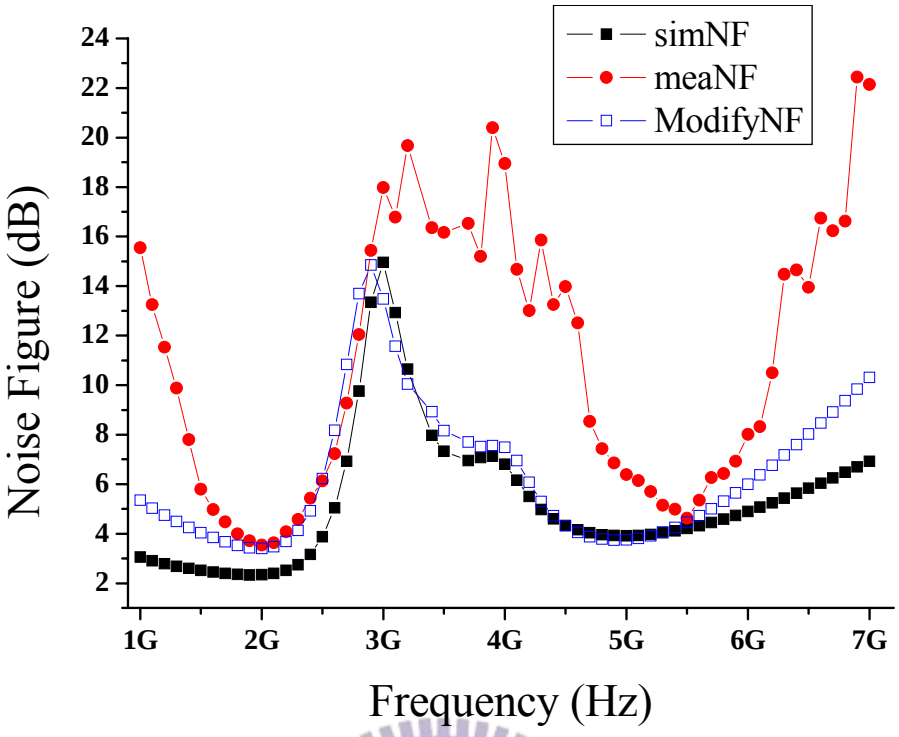


Figure 2.7.5 Comparison between simulation and measurement of noise figure

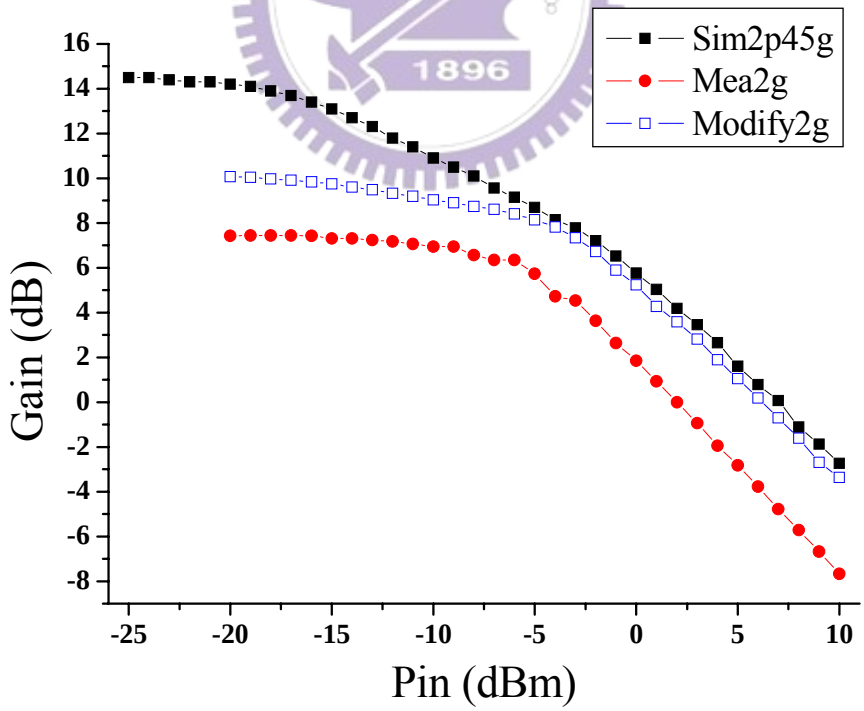


Figure 2.7.6 Comparison between simulation and measurement of P_{1dB} for lower band

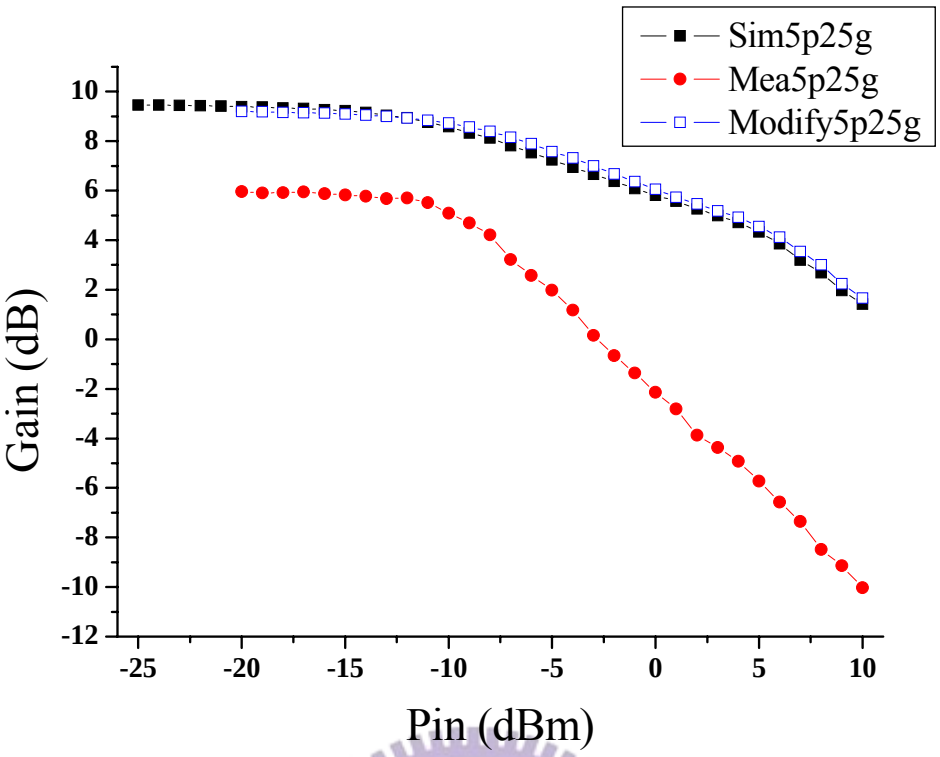


Figure 2.7.7 Comparison between simulation and measurement of P_{1dB} for higher band

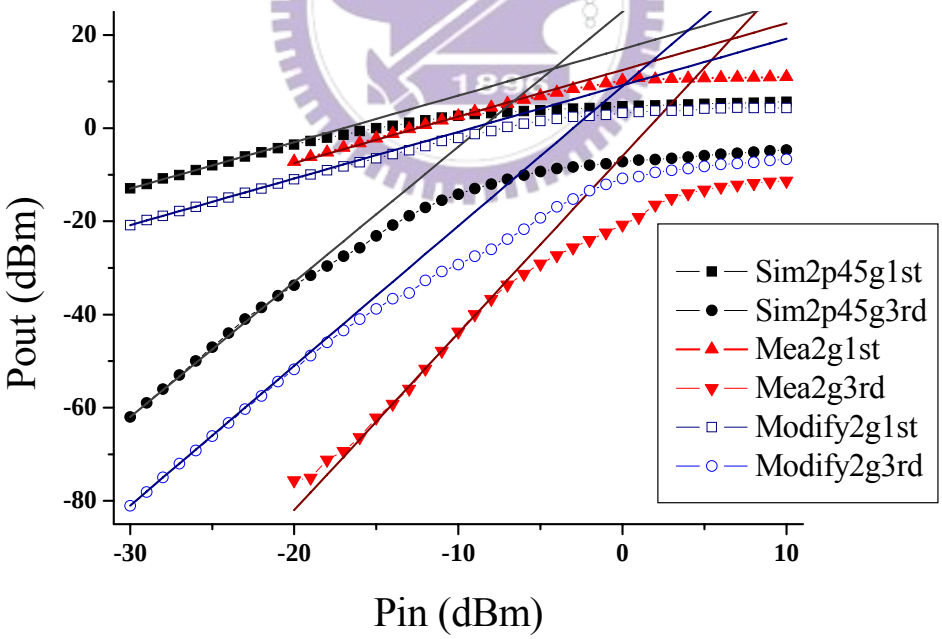


Figure 2.7.8 Comparison between simulation and measurement of IIP3 for lower band

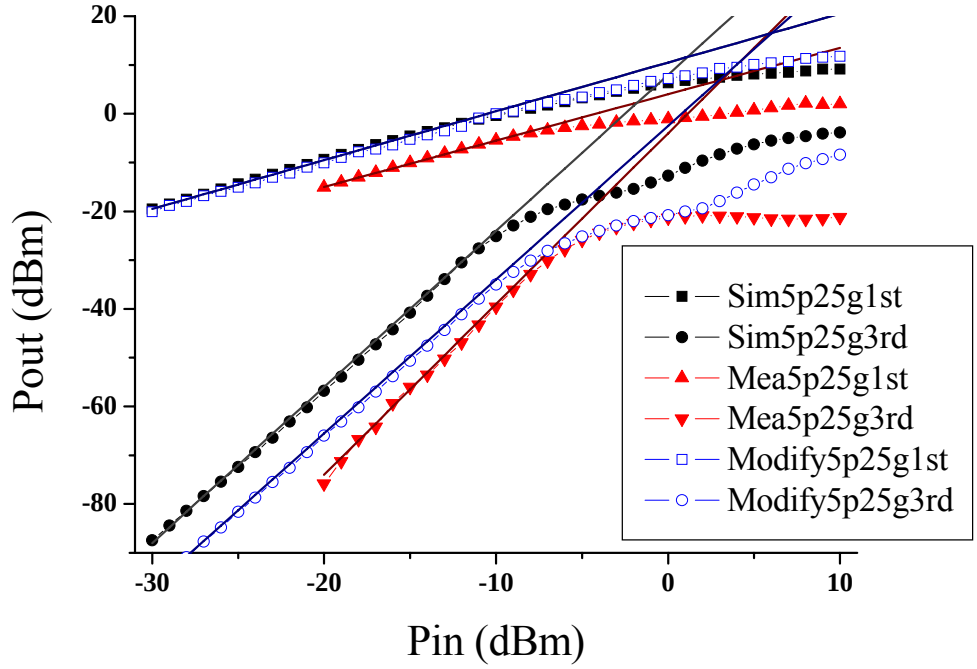


Figure 2.7.9 Comparison between simulation and measurement of IIP3 for higher band

Table 2.7.1 Performance summary of concurrent dual-band LNA

Specification	Simulation		Measurement		Modified Simulation	
Frequency(GHz)	2.45	5.25	2	5.25	2	5.25
S11 (dB)	-18.4	-15.2	-12.8	-12.9	-18.4	-13.7
S21 (dB)	14.5	9.47	7.45	6.06	10.0	9.30
S12 (dB)	-37.6	-30.5	-28.0	-32.5	-46.07	-36.14
S22 (dB)	-13.3	-13.9	-4.2	-3.8	-3.00	-7.43
NF (dB)	3.49	3.97	3.54	4.80	3.40	4.00
Pin-1dB (dBm)	-16.3	-10.4	-7.43	-9.66	-10.3	-7.18
IIP3 (dBm)	-5.90	-1.32	6.84	2.76	-0.12	6.09
Vdd (V)	1.8		1.8		1.8	
Power (mw)	7.93		7.21		7.93	

2.8 Comparisons

Table 2.8.1 shows the comparisons of this work and recent dual-band LNA papers. It can be seen that the concurrent dual-band LNA presented in this chapter achieves a good performance with low power consumption. The circuit will be applied to a concurrent dual-band receiver front-end in the next chapter.

Table 2.8.1 Comparisons of concurrent dual-band LNA

Ref	Process	Power	Frequency Band(Hz)	S21 (dB)	S11 (dB)	NF (dB)	P1dB (dBm)	IIP3 (dBm)
[7] 2002	CMOS 0.35um	10mw @2.5V	2.45G	14 (Av)	-25 *	2.3	-8.5	0
			5.25G	15.5 (Av)	-15 *	4.5	-1.5	5.6
[12] 2003	CMOS 0.18um	14.2mw @ 1V	2.4G	11.6	-5.1	2.3	-7.9	N/A
			5G	10.8	-26.3	2.9	-7.1	N/A
[13] 2003	CMOS 0.25um	19mw @1.5V	1.8G	18	-13	3.5	N/A	N/A
			5.8G	10	-10	5	N/A	N/A
[14] 2003 ※	CMOS 0.25um	31.2mw @ 2.5V	2.45G	13.2	-11.6	1.7	-5.1	10.1
			5.25G	10.5	-8.3	2.4	-5.1	19.9
[3] 2003	CMOS 0.25um	37mw @ 2.5V	2.45G	5.78	-20.4	4.7	-3.5	7
			5.25G	3.24	-12.8	5.69	6.5	17
This Work	CMOS 0.18um	7.21mw @1.8V	2G	7.45	-12.8	3.54	-7.43	6.84
			5.25G	6.06	-12.9	4.80	-9.66	2.76

※：simulation results

＊：off-chip input matching network

Chapter 3

Concurrent Dual-Band Receiver Front-End

3.1 Wireless LAN Standard Review

In this section, we will review the wireless LNA standard, IEEE 802.11a, IEEE 802.11b and IEEE 802.11g. The IEEE 802.11b standard at the 2.4GHz ISM (industrial, scientific, and medical) band provides data rate up to 11Mbits/s with the direct sequence spread spectrum (DSSS). The standard was released by IEEE in 1999. The 802.11a standard at 5GHz U-NII band provides data rate up to 54Mbits/s using OFDM (orthogonal frequency division multiplexing) modulation. Released in 2003, the IEEE 802.11g standard, operating at the same band of 802.11b, uses OFDM modulation and provides data rate up to 54Mbits/s. In this section these three wireless LAN standards will be briefly described respectively.

3.1.1 IEEE 802.11a

As shown in Figure 3.1.1 the 802.11a standard has three U-NII (Unlicensed National Information Infrastructure) bands, including the lower band (5.15GHz~5.25GHz), the middle band(5.25~5.35GHz) and the upper band (5.725GHz~5.825GHz). The lower and middle sub-bands accommodate eight channels in a total bandwidth of 200MHz. The upper band accommodates four

channels in a bandwidth of 100MHz. The centers of the outermost channel shall be at a spacing of 30MHz from the edge of band for the lower and middle bands, and 20 MHz for the upper band. The bandwidth of each channel is 20MHz, and each channel has 52 sub-carriers for OFDM modulation with each sub-carrier has bandwidth of 312.5 KHz. Each sub-carrier can be either a BPSK, DQPSK, 16QAM, 64QAM signal. The data rate versus modulation is shown in Table 3.1.1. The input signal dynamic range is from -82dBm to -4dBm [15].

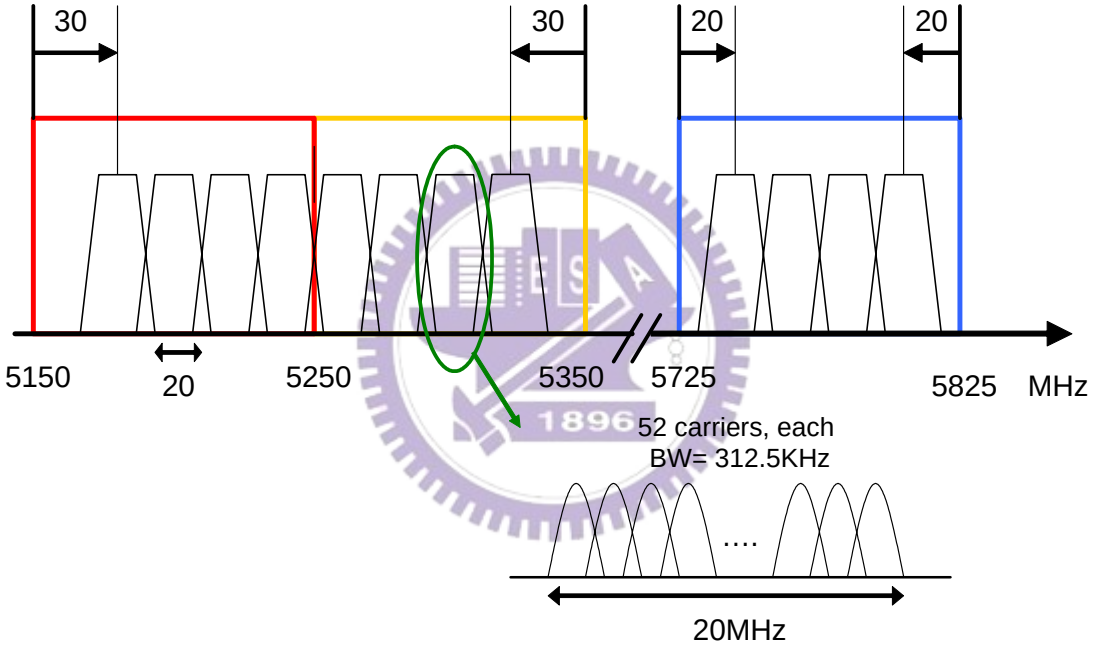


Figure 3.1.1 Channel allocation of IEEE 802.11a standard

Table 3.1.1 IEEE 802.11a modulation versus data rate

Modulation	Data Rate (Mbps)
BPSK	6 , 9
DQPSK	12 , 18
16QAM	24 , 36
64QAM	48 , 64

3.1.2 IEEE 802.11b

IEEE 802.11b standard can be discussed by two operation areas: North American and European. The frequency range for North American is from 2400MHz to 2472MHz while the range for European is from 2400MHz to 2483.5MHz. Here we will discuss the North American operation. For non-overlapping operation three channels are used and the channel center frequencies are: 2412MHz, 2437MHz, and 2462MHz. As for overlapping operation, six channels are selected. The center frequency of each channel has a distance of 10MHz from others. Figure 3.1.2 shows the channel location of 802.11b standard. IEEE 802.11b provides a data rate up to 11Mbps and uses direct sequence spread spectrum (DSSS) and complementary code keying (CCK) modulation [16].

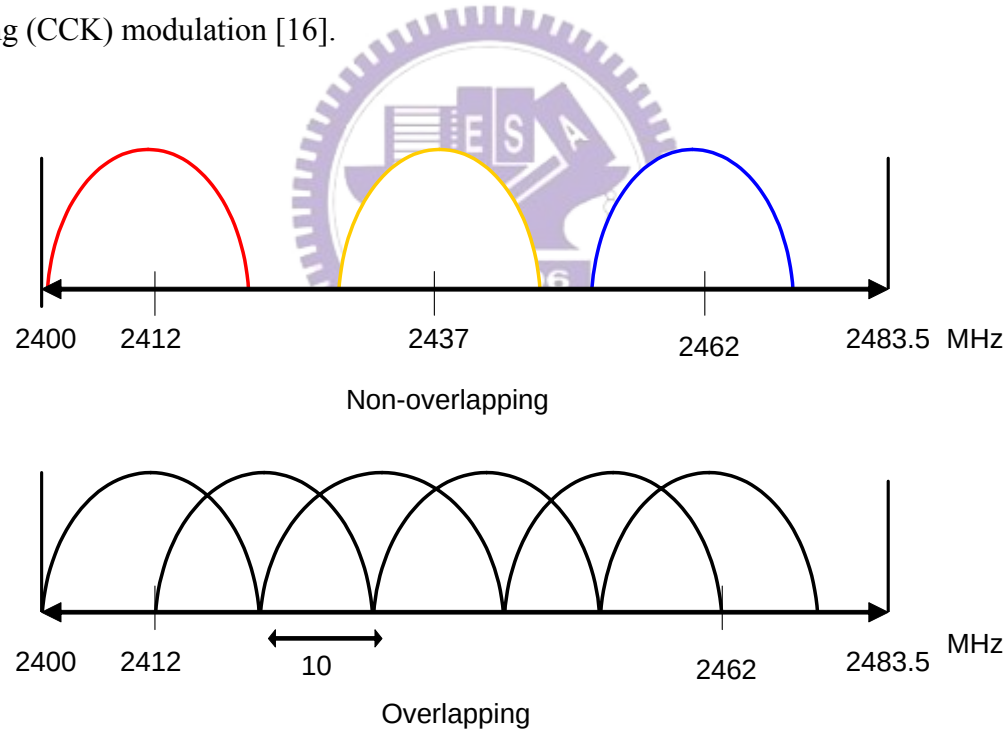


Figure 3.1.2 Channel allocation of 802.11b standard

3.1.3 IEEE 802.11g

The operation frequency of 802.11g is from 2412MHz to 2483MHz, and the

bandwidth of each channel is 20MHz. It extends the data rate of 802.11b to 54Mbps in the 2.4GHz band using OFDM modulation. Similar to 802.11b, 802.11g has three non-overlapping channels [17]. Table 3.1.2 lists the overview of IEEE 802.11a/b/g.

Table 3.1.2 Overview of wireless LAN standard

Mode	Data Rate (Mbps)	Modulation Method	Frequency (MHz)	Available Spectrum (MHz)	Channel Spacing (MHz)
802.11a	6-54	OFDM	5150 - 5350 5725 – 5825	300	20
802.11b	1-11	CCK	2400 – 2483	83.5	25
802.11g	6-54	OFDM	2400 - 2483	83.5	25
	1-11	CCK			25

3.2 Review of Receiver Architecture

The aggressive design goals of radio frequency transceivers may include low cost, low power dissipation, and small chip size. The architecture and frequency plan of the RF transceiver play an important role in the complexity and performance of the overall system. The base band signal feed into the transmitter is sufficiently strong, so there are fewer transmitter architectures thane those of receivers which small input signal is feed into. Some important issues such as noise, interference rejection, and band selectivity are serious discussed in the design of receivers. In this section we review some of recently popular receiver architectures, including heterodyne, homodyne, and low-IF. The benefits and drawbacks of them will be discussed in the following pages.

3.2.1 Heterodyne Architecture

The first kind of receiver architecture is the heterodyne receivers shown in Figure 3.2.1. The RF input signal is firstly amplified, and then converted to a lower intermediate frequency (IF) by a local oscillator signal (LO). The low-noise amilifier (LNA) in front of the down-conversion mixer is used to amplify the RF signal and to reduce the noise figure of the following stage because of the high noise mixer. The IF filter suppress out-of-channel interferes and performs channel selection. This architecture suffers from a number of drawbacks. The problem of image is serious in heterodyne receivers. The most common approach to suppressing the image is through the use of an image-reject filter placed before the mixer. However the choice of IF becomes a trade-off between the image noise and the designs of IF filter. If the IF is high the image can be suppressed but complete channel select becomes difficult, and vice versa. In other word, the designer has to trade-off between selectivity and sensitivity.

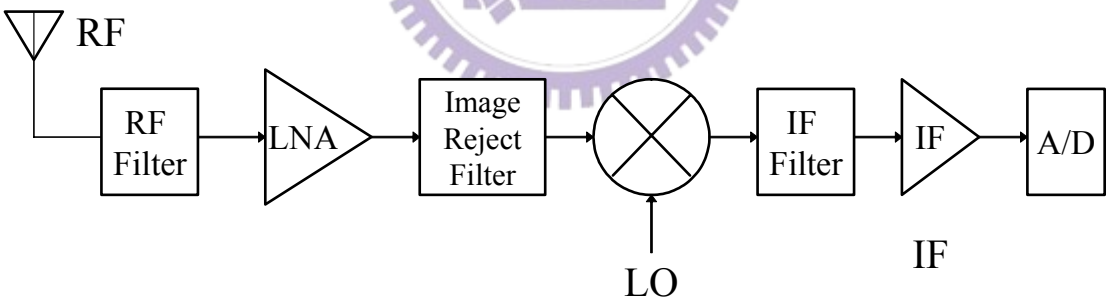


Figure 3.2.1 Heterodyne receiver architecture

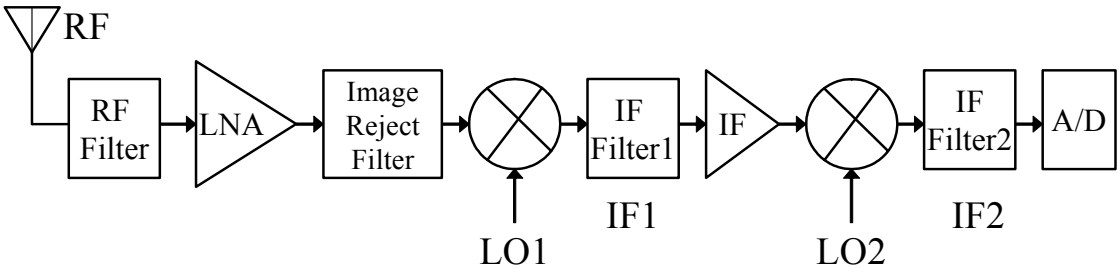


Figure 3.2.2 Super-heterodyne receiver architecture

To solve the trade-off between selectivity and sensitivity, the super-heterodyne receiver, as shown in Figure 3.2.2, are presented. Most RF communication receivers use this conventional architecture. To release the requirement of filters' Q- value we can down convert the RF signal by two steps, and perform the image rejection and channel selection between these stages. The drawback of super-heterodyne architecture is the numerous components. The filters which are commonly implemented with external SAW filters will be difficult to be integrated into a single chip while the on-chip filters would occupy unreasonable large areas.

3.2.2 Homodyne Architecture

Homodyne receivers, also called direct-conversion receivers or zero IF receivers, translates the RF signal directly to zero frequency. Figure 3.2.3 shows the architecture of the homodyne receivers. It has two important advantages over heterodyne architecture. First, the problem of image is circumvented because of zero IF. As a result, on image filter is required in front of the LNA. Second, the IF filters and subsequent down-conversion stages are replaced with low-pass filters and base-band amplifiers that are easy to monolithic integration. The drawbacks of the homodyne architecture may include the dc offset, I/Q mismatch, even-order distortion and flicker noise problem and the LO leakage to the antenna. The details about these problems and some possible solutions have been discussed in [18].

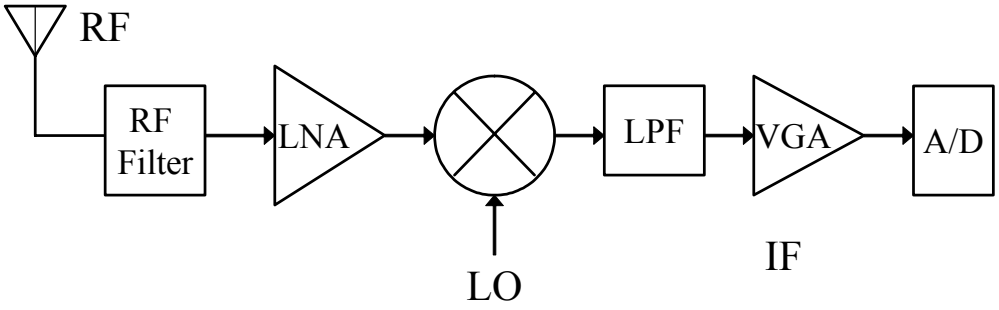


Figure 3.2.3 Homodyne receiver architecture

3.2.3 Low-IF Architecture

Comparing with the homodyne architecture converting the RF signal to zero IF directly, the other architecture converts the RF signal to low IF signal, which is so called low-IF architecture. Low-IF receiver architecture has gained much interest recently because it avoids the use of expensive discrete components such as image-reject filters, allowing a higher level of integration. As a non-zero IF receiver architecture, dc offset and LO self-mixing problems in low-IF receivers are not so severe compared to those in zero-IF receivers. On the other hand, low-IF receivers do have image problems. The most common techniques to remove the image in low-IF receivers are to use image reject architecture or polyphase filters [19]. The comparisons of these receiver architectures are summarized in Table 3.2.1

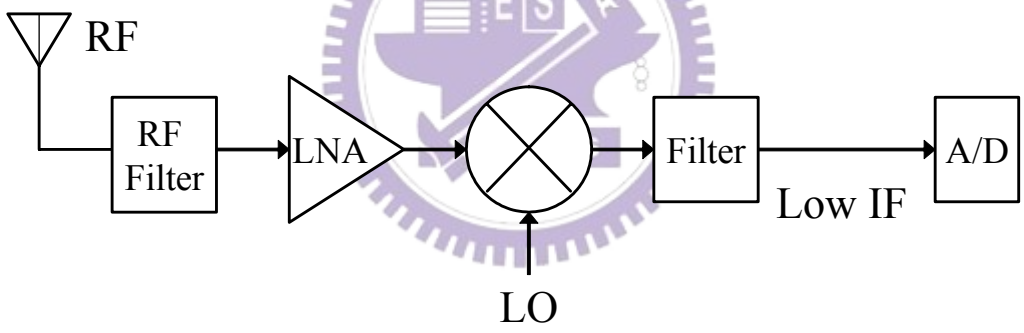


Figure 3.2.4 Low-IF receiver architecture

Table 3.2.1 Comparisons of different receiver architectures

Architecture	IF frequency	Image reject filter	DC-offset problem	SoC
Heterodyne (Superheterodyne)	High	Off-chip	No	Low
Homodyne	Zero	None	High	High
Low-IF	Low	On-chip	No	High

3.3 Design of Concurrent Dual-Band Receiver Front-End

In this section a new concurrent dual-band receiver using only one frequency synthesizer with tuning range of around 2.4 GHz for WLAN applications is introduced first. Figure 3.3.1 shows the concurrent dual-band receiver block diagram which has been proposed in [4]. It provides a RF concurrent dual-band receiver solution for IEEE 802.11a/b/g. The receiver consists of a differential concurrent dual-band LNA, a sub-harmonic mixer for 2.45GHz, a Gilbert-cell mixer modified from sub-harmonic topology for 5.25GHz, a quadrature voltage-controlled oscillator (VCO) and a multi-modulus frequency synthesizer. Appling such mixer operating at 2.45 GHz or 5.25 GHz with the same architecture can reduce the design complexity significantly. On-chip IF Gm-C filters are used for noise bandwidth limiting and anti-aliasing reasons. The concurrent dual-band receiver front-end is designed for this receiver block diagram as the marked area in Figure 3.3.1, which is designed and implemented cooperatively by the author and the other one [21].

Based on the comparisons of differential receiver architectures in last section, we choose low-IF receiver architecture in this work because of high degree of integration. The IF frequency is chosen at 10MHz because of the noise and receiver architecture considerations. The receiver frequency plan is shown in Figure 3.3.2. It can be seen that the tow LO frequencies are very close because of the usage of sub-harmonic mixer. Hence one frequency synthesizer is enough to provide the tuning range of LO signals around 2.4GHz. Compared with traditional topology with two Gilbert-cell mixers two frequency synthesizers may be needed owning to large frequency difference of two LO signals for two bands.

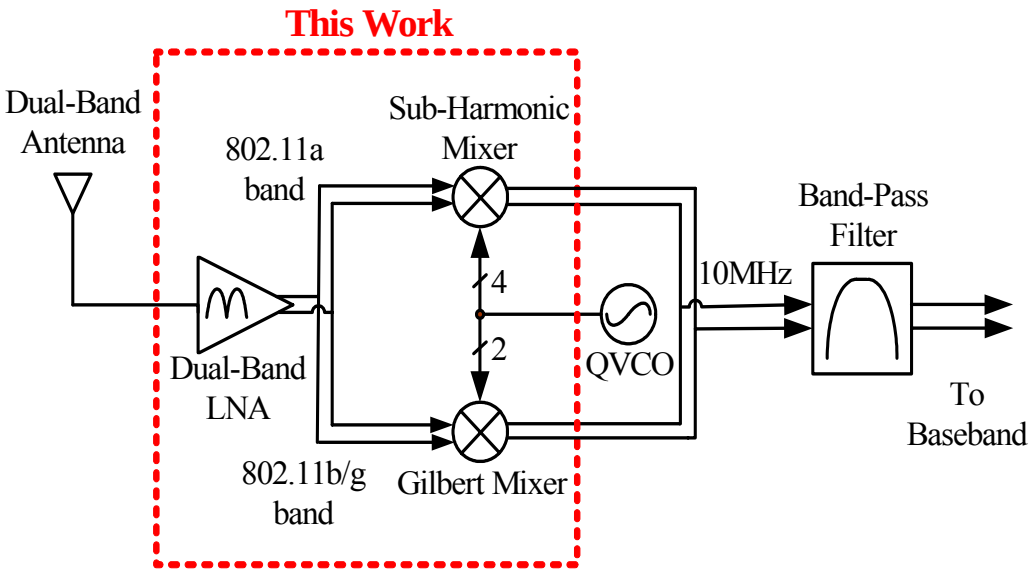


Figure 3.3.1 New concurrent dual-band receiver and concurrent dual-band

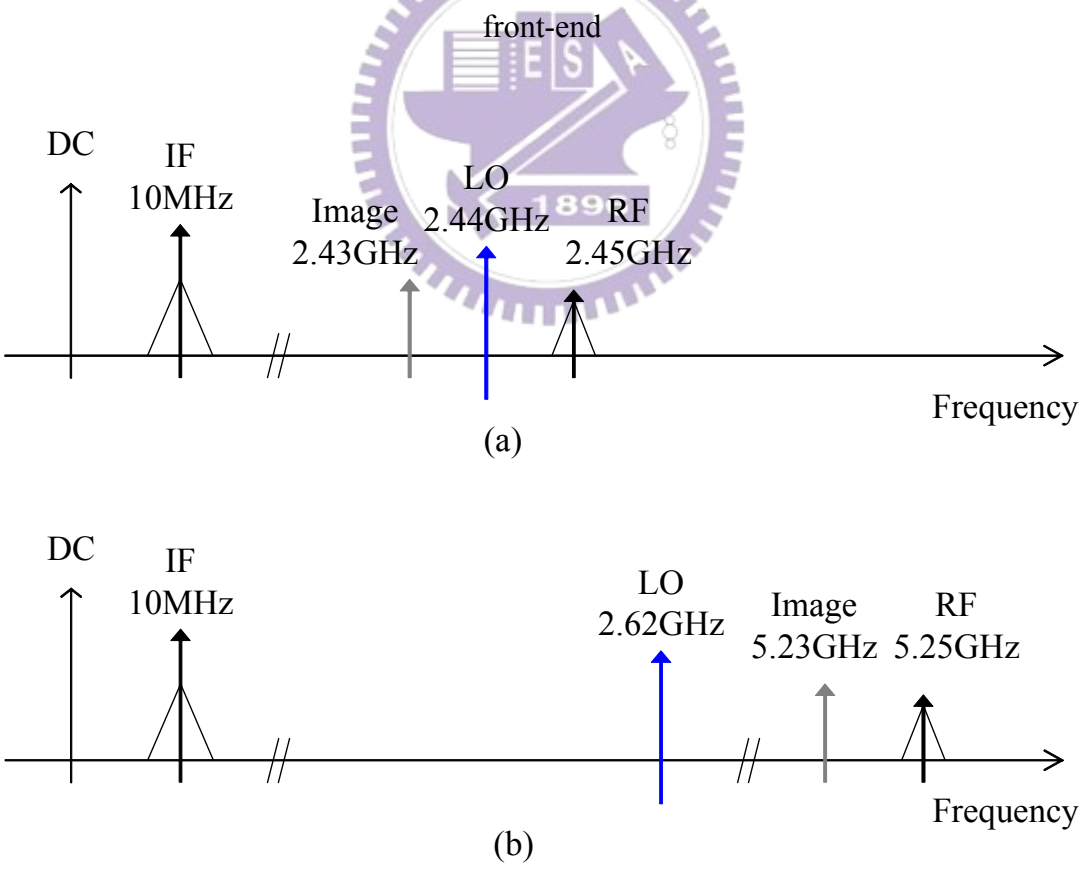


Figure 3.3.2 Receiver frequency plan (a) 2.45GHz (b) 5.25GHz

The architecture of concurrent dual-band LNA for receiver front-end is shown in Figure 3.3.3. It has a similar architecture as the one discussed in last chapter except the spiral inductor Ls is replaced by the bondwire inductor $L_{bondwire1}$. Two other bondwires are needed in the RF input pad and power supply pad, so the input matching network and output matching network must be redesigned by considering the effect of the parasitic inductor from the bondwire. The inductance of bond wire is predicted as 1nH per 1mm length. Figure 3.3.4 illustrates the comparison of operation principles of conversional mixer and sub-harmonic mixer. The role of switching transistor (Qs) is evenly distributed to two parallel-connected transistors (Qs1, Qs2) in sub-harmonic mixer, thus it needs only half LO frequency compared to conversional mixer. Figure 3.3.5 and 3.3.6 show the topologies of the two mixers for receiver front-end. The design details about sub-harmonic mixer and Gilbert-cell mixer modified from sub-harmonic mixer can be found in [21].

The challenge of integrating LNA and mixers comes from the inter-stage design. In the design procedure we try to match the output matching of differential dual-band LNA and RF input matching of two mixers to the same impedance, for instance, 500 ohms parallel with 100pF, rather 50ohms. Large coupling capacitors are added between LNA and mixers for RF signal coupling and dc isolation. Some other circuits, like quadrature balun, balun, LO port matching network, and IF low-pass-filter, are implemented on PCB with lumped elements. The chip layout occupies area of 1.45mm x 1.45mm, and is shown in Figure 3.3.7. Figure 3.3.8 is the chip photograph of this work.

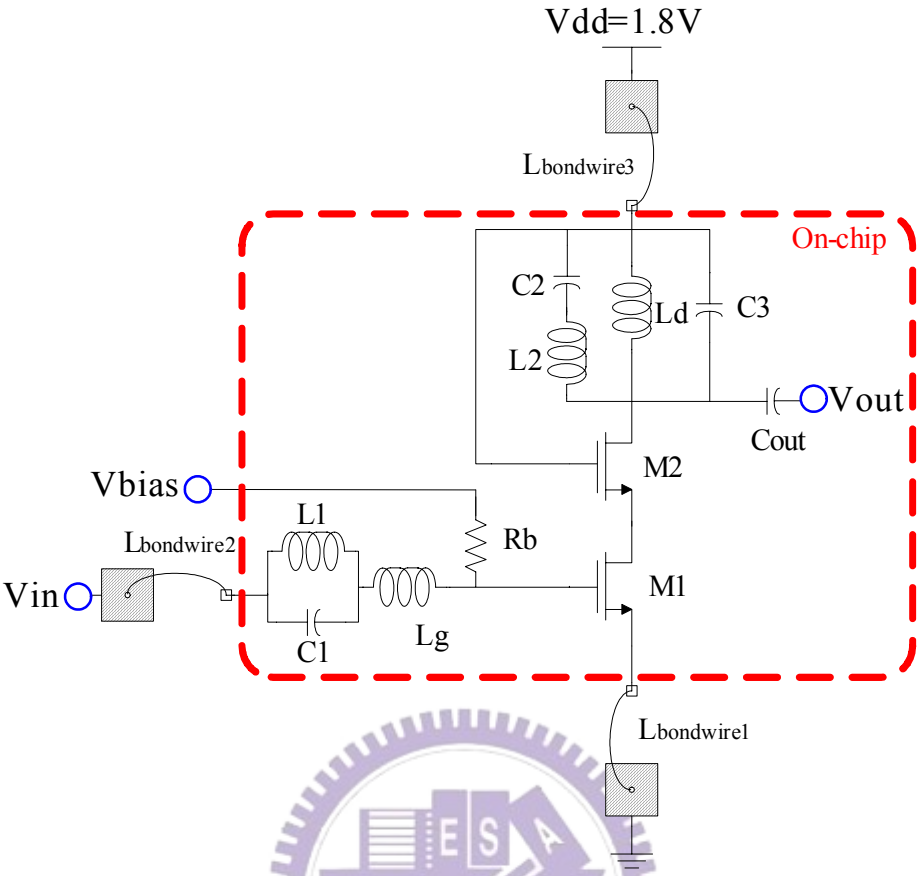


Figure 3.3.3 Concurrent dual-band LNA for receiver front-end

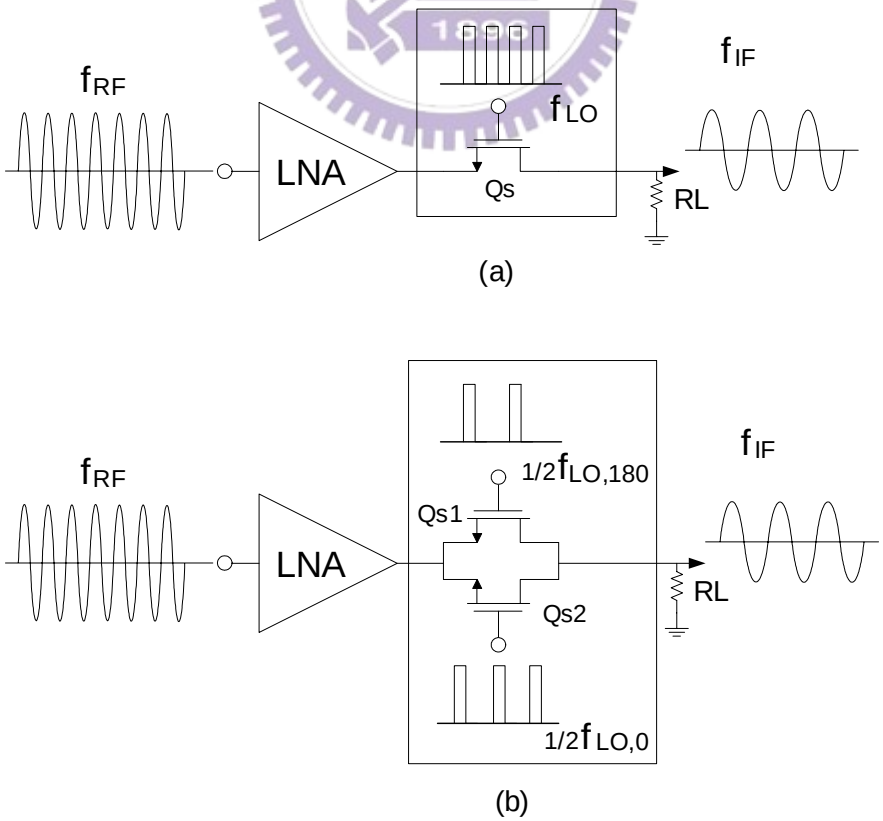


Figure 3.3.4 Basic concept of (a) conversional mixer (b) sub-harmonic mixer

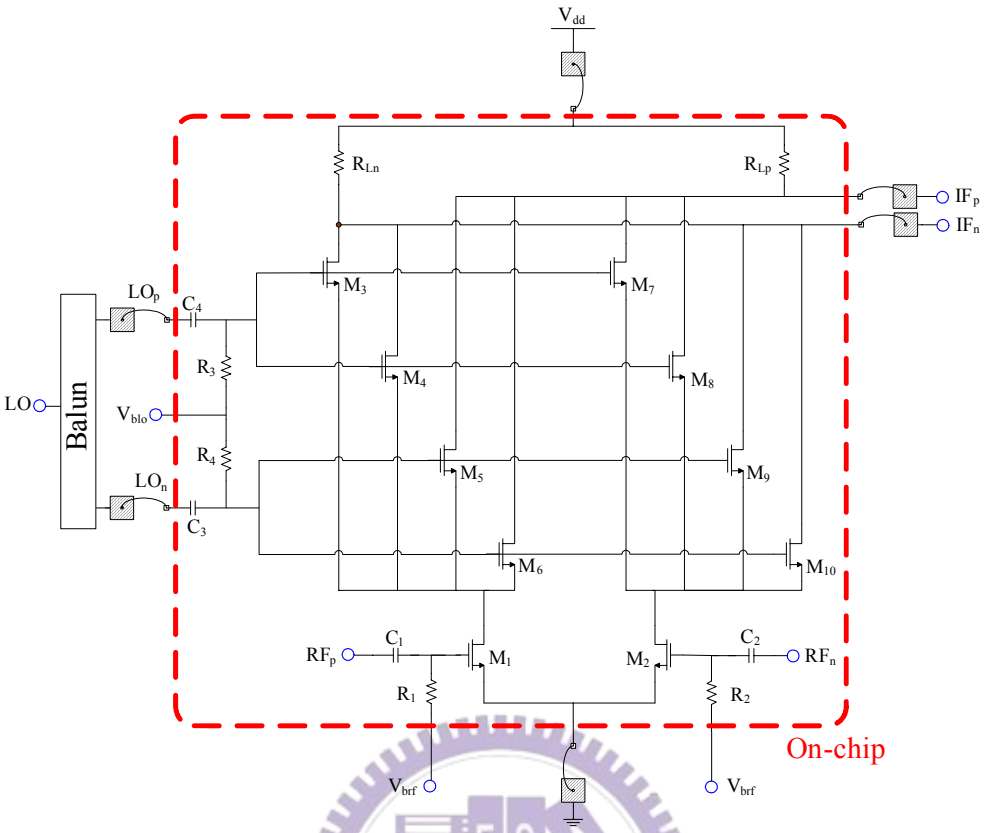


Figure 3.3.5 Gilbert-cell mixer for 2.45GHz front-end

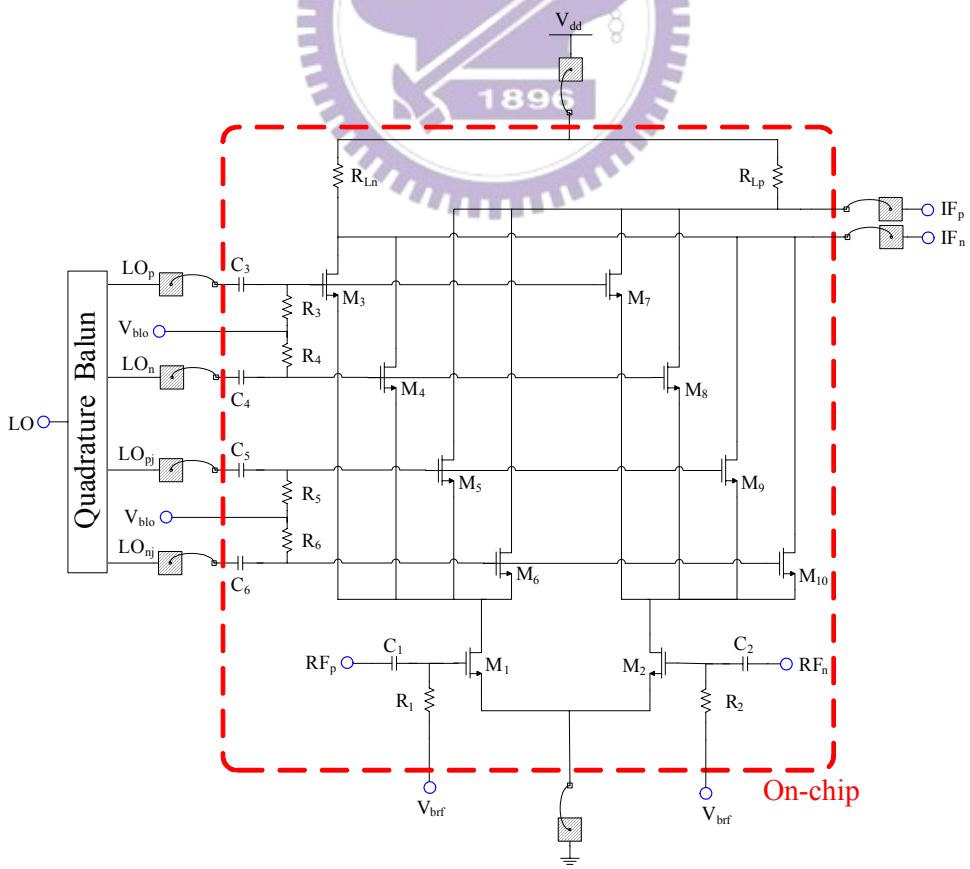


Figure 3.3.6 Sub-harmonic mixer for 5.25GHz front-end

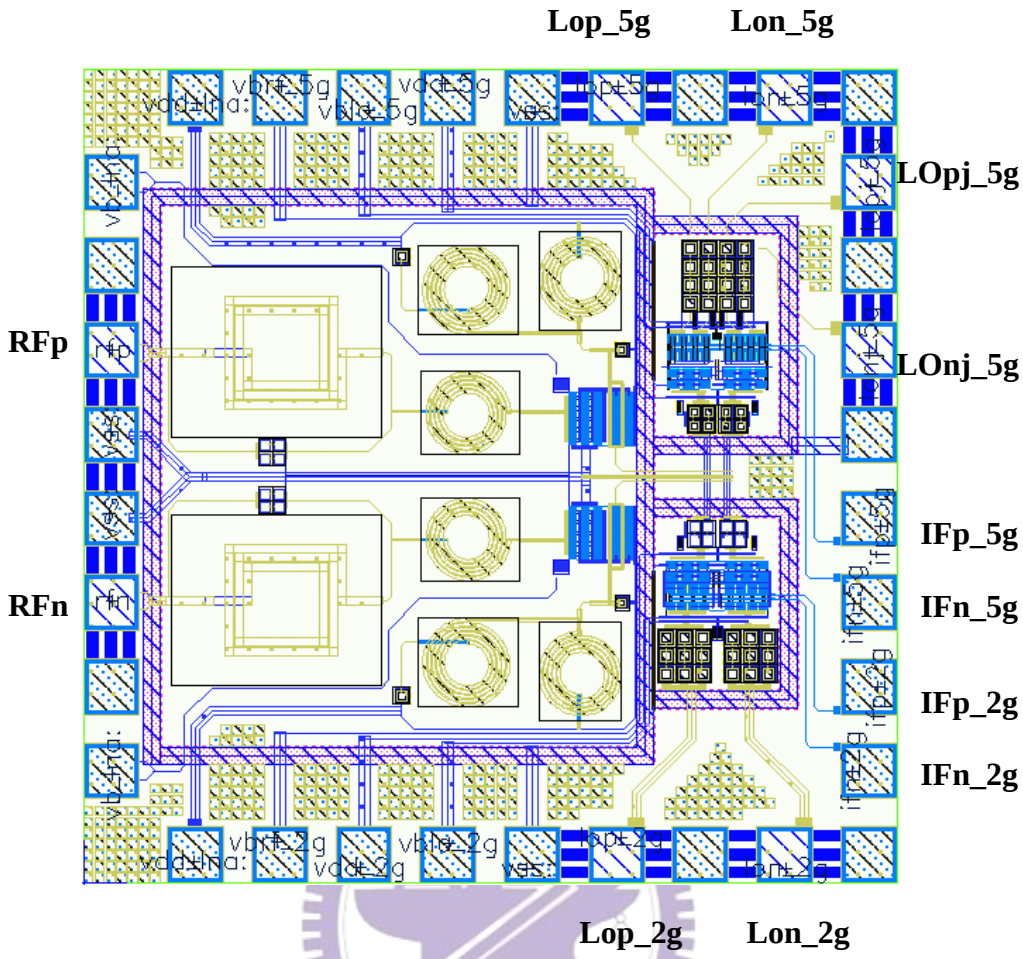


Figure 3.3.7 Chip layout of concurrent dual-band front-end

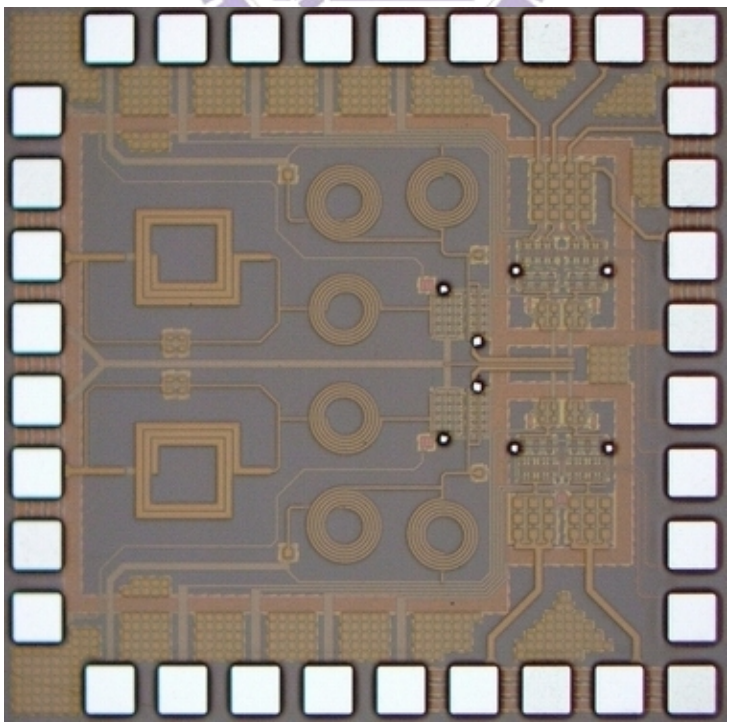


Figure 3.3.8 Chip photo of concurrent dual-band front-end

3.4 Experimental Results and Discussions

The concurrent dual-band receiver front-end is measured by two PCB boards, 2.45GHz and 5.25GHz, rather one PCB board, because of large size off-chip passive baluns, too many on-board decoupling capacitors, and complicated dc bias routing for circuits. As shown in section 3.3, a balun for 2.44GHz and a quadrature balun for 2.62GHz are needed to provide differential and quadrature LO signals, which are shown in Figure 3.4.1 and 3.4.2, respectively.

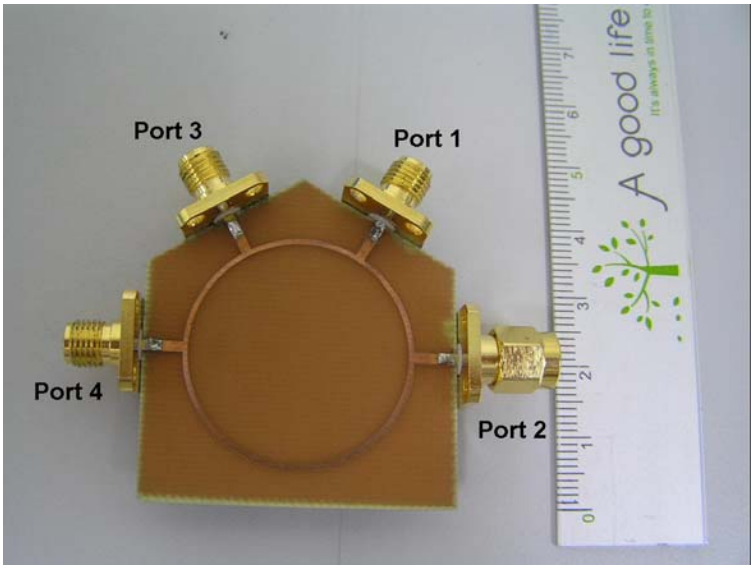


Figure 3.4.1 Balun for 2.44GHz

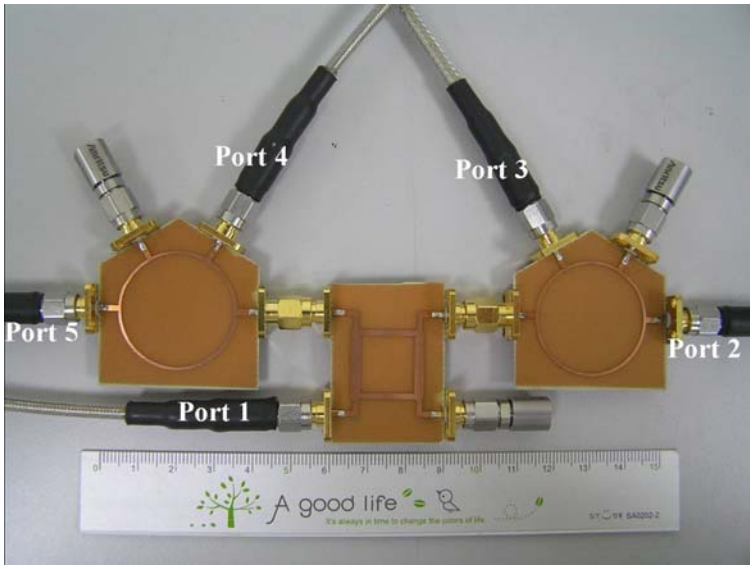


Figure 3.4.2 Quadrature balun for 2.62GHz

The measured transmission coefficients of the 2.44GHz rat-race is

$$[S]_{rat-race} = \begin{bmatrix} 0.029\angle 117.4° & 0.678\angle 135.56° & 0.689\angle 135.4° & 0.016\angle -94.2° \\ 0.678\angle 135.14° & 0.045\angle 0.2° & 0.024\angle -161.7° & 0.675\angle -42.5° \\ 0.688\angle 134.95° & 0.023\angle -162.5° & 0.029\angle 34.6° & 0.677\angle 137.62° \\ 0.016\angle -93.8° & 0.675\angle -42.1° & 0.678\angle 138.15° & 0.057\angle 41.1° \end{bmatrix}$$

when all other ports are terminated with matched loads. The measured transmission coefficients of the quadrature balun composed of two rat-races and quadrature hybrid from port1 to port 2-port 5 are

$$S_{21} = 0.444\angle -125.75° \ ; \ S_{31} = 0.442\angle 54.82° \ ;$$

$$S_{41} = 0.452\angle 142.04° \ ; \ S_{51} = 0.452\angle -35.27°$$

Selecting port 3 as phase reference we have phase relationship as

Port 2：179.43° ; Port 3：0° ;

Port 4：87.22° ; Port5：269.91°

The characteristic of quadrature balun satisfies the requirement for the LO port of sub-harmonic mixer though there are small phase and magnitude errors.

PCB layouts and practical FR4 PCB circuits with SMA connectors are shown in Figure 3.4.3 and 3.4.4. There are some comments on PCB boards. Firstly the width of RF and LO signal paths on PCB are drawn as 50 ohms-line for impedance matching. Lumped Coupling capacitors (1uF) are placed in the RF paths for dc isolation. To filter out the ineluctable noise and spur from the power supplies we add four lumped decoupling capacitors (100pF, 10nF, 100nF, and 1uF) between each dc voltage and ground. IF low-pass-filters composed of lumped capacitors and resistors are placed at the IF outputs to depress the high frequency noise. The signal lines for differential or quadrature signals should be symmetric to avoid the phase error caused by the PCB transmission lines.

The block diagram of PCB on board testing for dual-band receiver front-end is

shown in Figure 3.4.5. LO port has two paths for 2.45GHz front-end because of differential balun and four paths for 5.25GHz front-end because of quadrature balun. Two RF baluns are needed in the measurement, one for 2.45GHz and the other for 5.25GHz, to convert the RF signal from single to differential. The oscilloscope will be connected to the IF port to measure the output waveform because of 1M high input impedance.

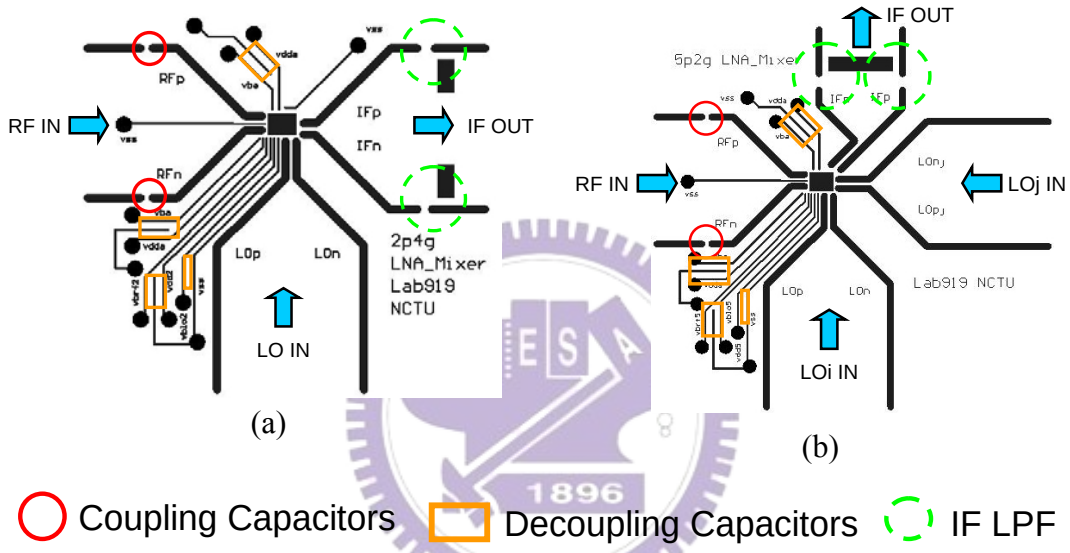
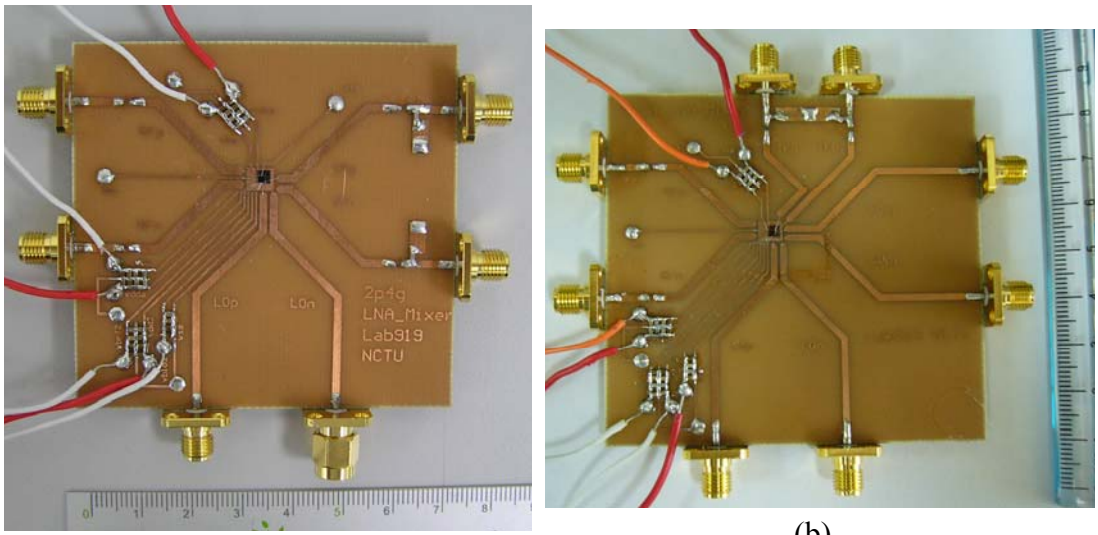


Figure 3.4.3 PCB layout for (a)2.45GHz (b) 5.25GHz front-end



(a) (b)

Figure 3.4.4 Photograph of PCB board for (a)2.45GHz (b)5.25GHz front-end

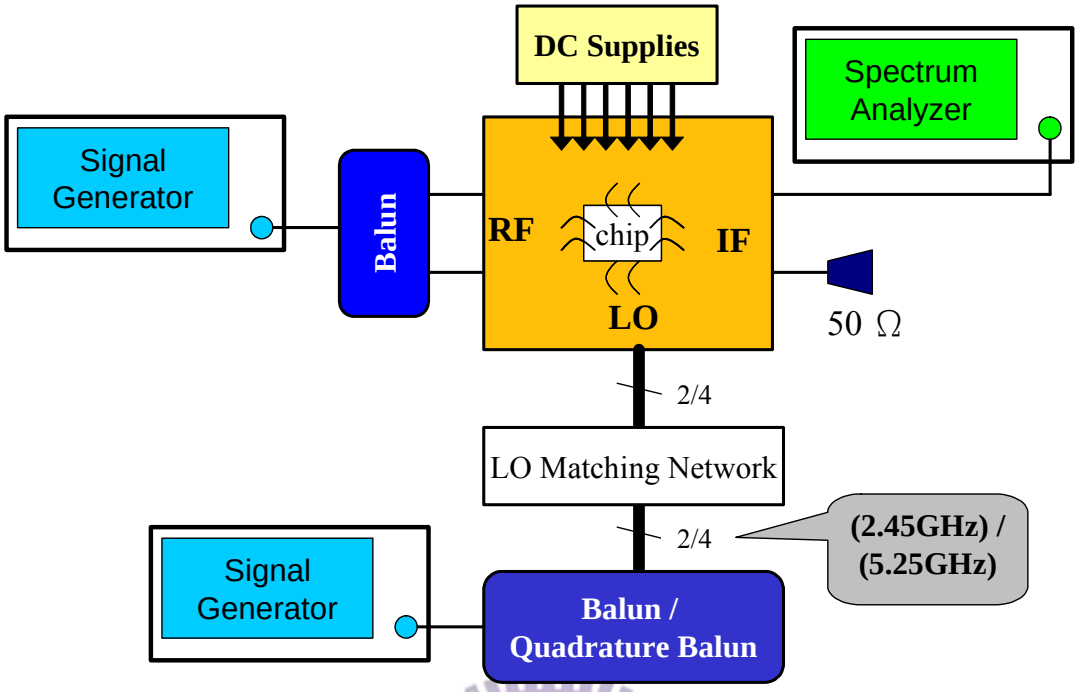


Figure 3.4.5 Block diagram of PCB on-board testing for dual-band front-end

Table 3.4.1 summaries the performance of this work, including simulation and measurement results. The concurrent dual-band receiver front-end was fabricated using 0.18um CMOS 1P6M process. The RF input return loss of LNA are -15.9 dB and -15.8 dB at 2.45GHz and 5.25GHz, as shown in Figure 3.4.6. The LO port input return loss of two mixers are -13.4 dB and -13.1 dB, as shown in Figure 3.4.7 and 3.4.8. Figure 3.4.9 ~ Figure 3.4.12 show the measured linearity of the front-end characterized by the overall RF-to-IF -21.0 dBm and -15.3 dBm P_{1dB} and the overall RF-to-IF -4.2 dBm and 4.9 dBm IIP3 for RF signals in two frequency bands. It demonstrates 17.2 dB and 11.8 dB voltage gain, 7.22 dB and 10.78 dB noise figure concurrently at two frequency bands with 28.8mw power dissipation. Finally the 10MHz output waveforms measured by oscilloscope are shown in Figure 3.4.13.

Here are some discussions about the experimental results. The good RF input return loss may be owing to the accurate prediction of bondwire inductance and on-chip

circular spiral inductors which were designed, measured, and modeled by our group, rather foundry. The good LO input return loss comes from the accurate LO matching network composed of lumped inductors and capacitors. It may take great efforts to tune the matching network from the finite lumped element libraries. Although this work has good port input return loss, the performance of gain and noise figure does not meet our anticipation. There are three major factors. First, the inter-stage design may be interfered by the parasitic capacitors and resistors, causing the impedance mismatch between the output of differential dual-band LNA and RF input of mixers. Second, the quality factor Q values of the inductors are not good enough due to parasitic resistances. The Q-values of these inductors involved in this work is from 7.08 to 8.27. The gain and output matching of the concurrent dual-band LNA will be seriously affected by the poor Q-value of inductors. Finally the absence of output buffers at IF output impacts the driving capability of the front-end. These factors may depress the gain and increase noise figure of the concurrent dual-band receiver front-end.

Table 3.4.1 Performance summary of dual-band receiver front-end

	2.45GHz Front-End		5.25GHz Front-End	
	Sim.	Mea.	Sim.	Mea.
LO Power (dBm)	-3	8	-3	7
RF Return Loss (dB)	-18.4	-15.9	-13.4	-15.8
LO Return Loss (dB)	-13.2	-13.4	-18.3	-13.1
Conversion Gain (dB)	14.7	6.0	2.57	-12.0
Voltage Gain (dB)	26.5	17.2	19.9	11.8
Noise Figure (dB)	3.77	7.22	7.28	10.78
P1dB (dBm)	-20.6	-21.0	-22.1	-15.3
IIP3 (dBm)	-7.8	-4.2	-4.5	4.9
Power (mw)	17.9	28.8	17.9	28.8

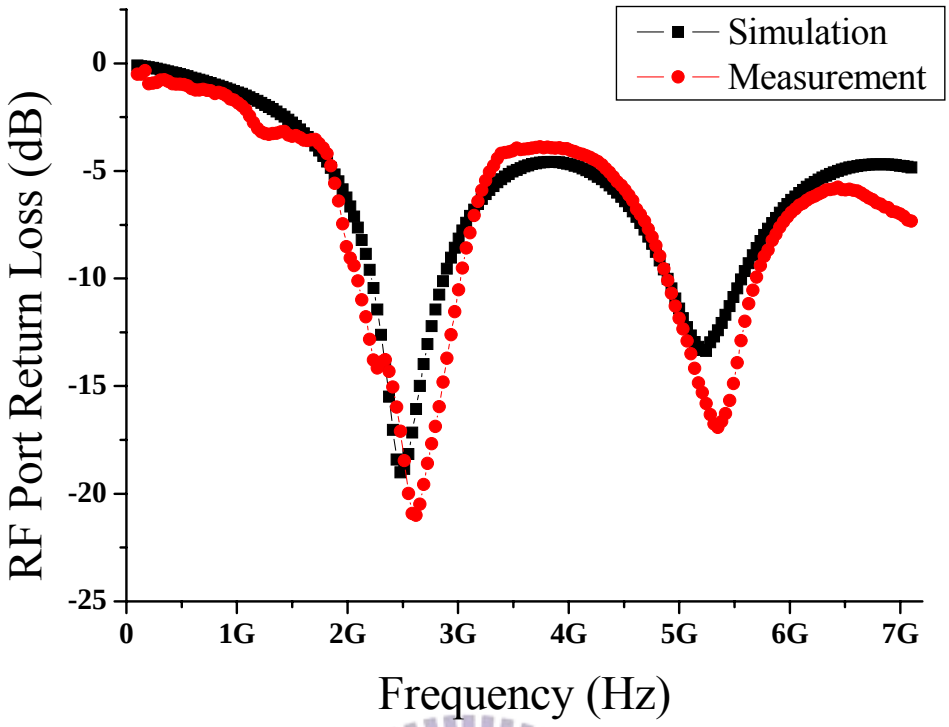


Figure 3.4.6 Comparison between simulation and measurement RF input return loss

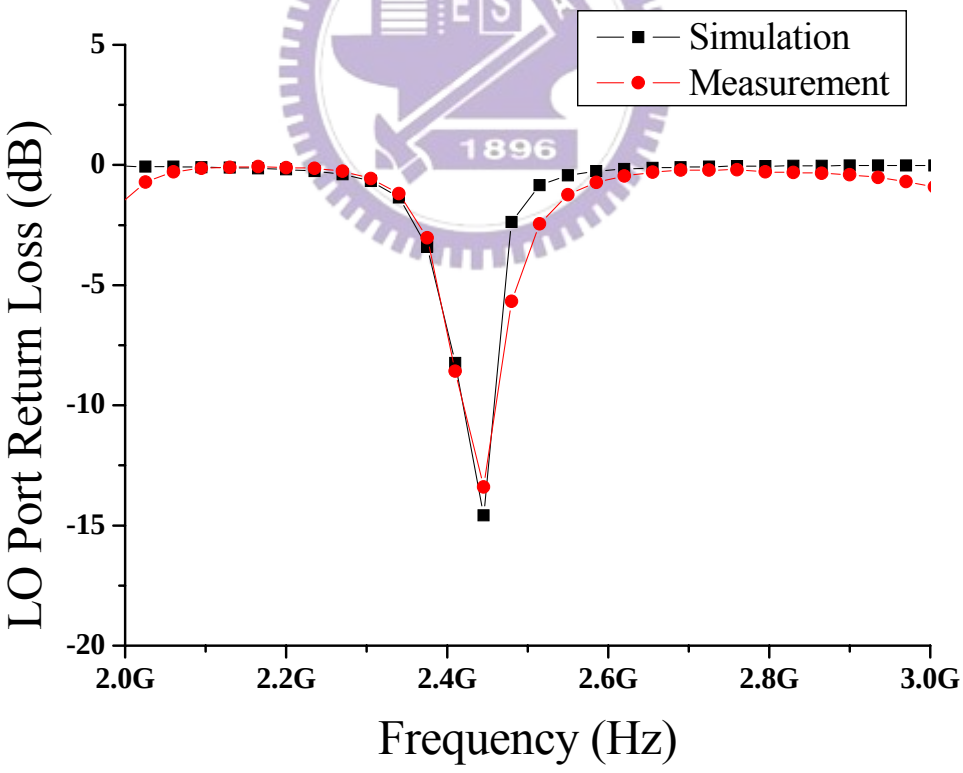


Figure 3.4.7 Comparison between simulation and measurement
LO input return loss of 2.45GHz Gilbert-cell mixer

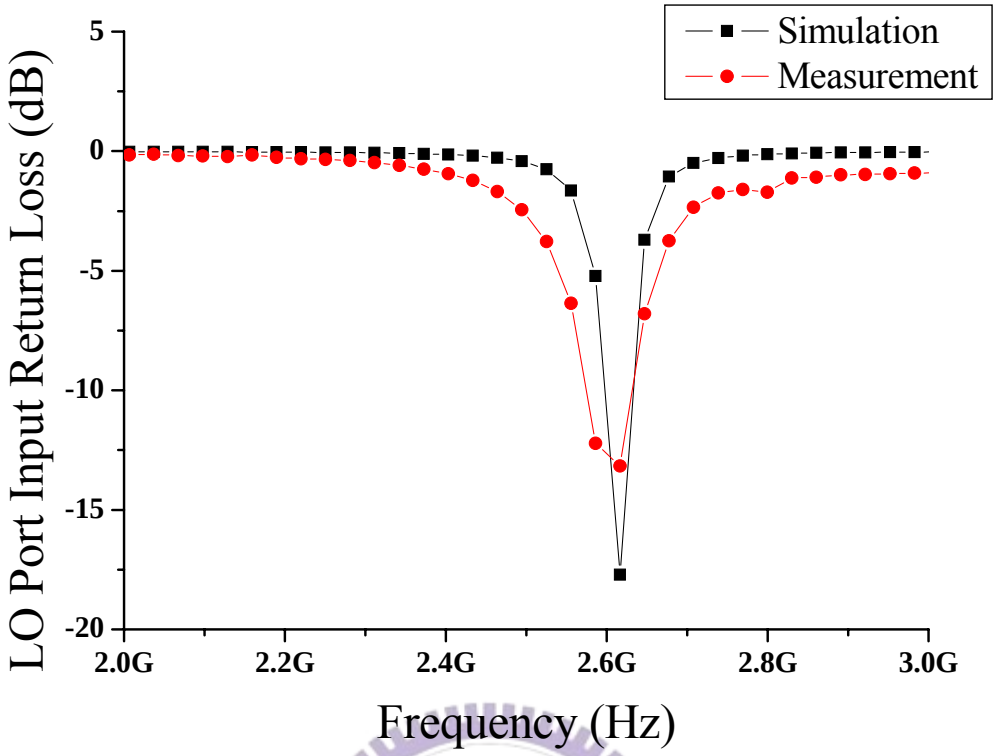


Figure 3.4.8 Comparison between simulation and measurement
LO input return loss of 5.25GHz sub-harmonic mixer

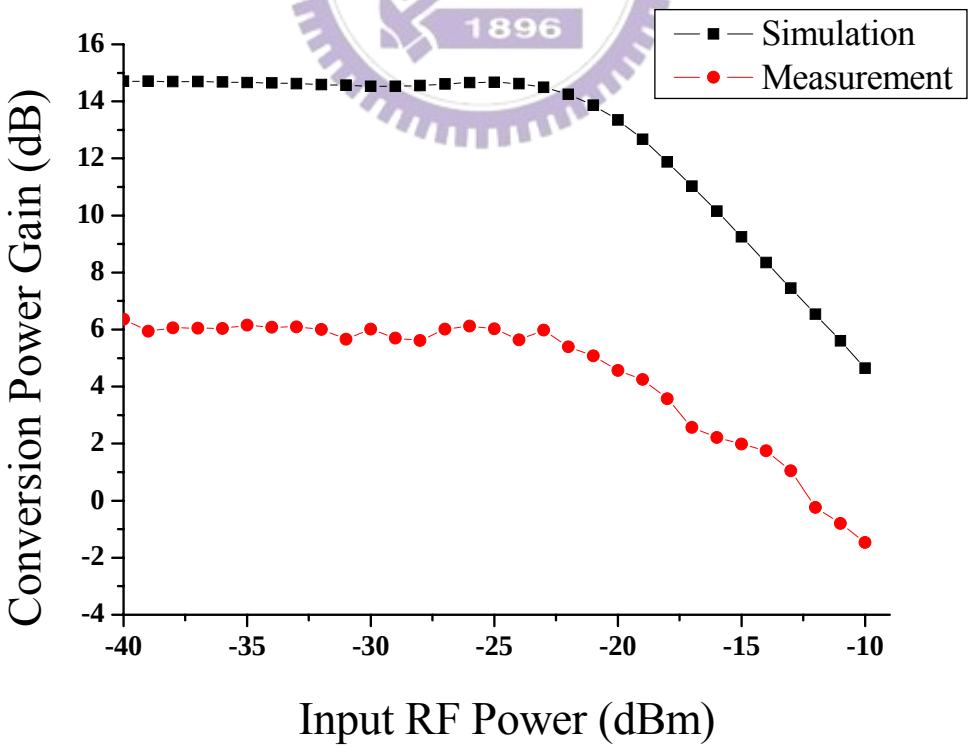


Figure 3.4.9 Comparison between simulation and measurement of P_{1dB}
of 2.45GHz front-end

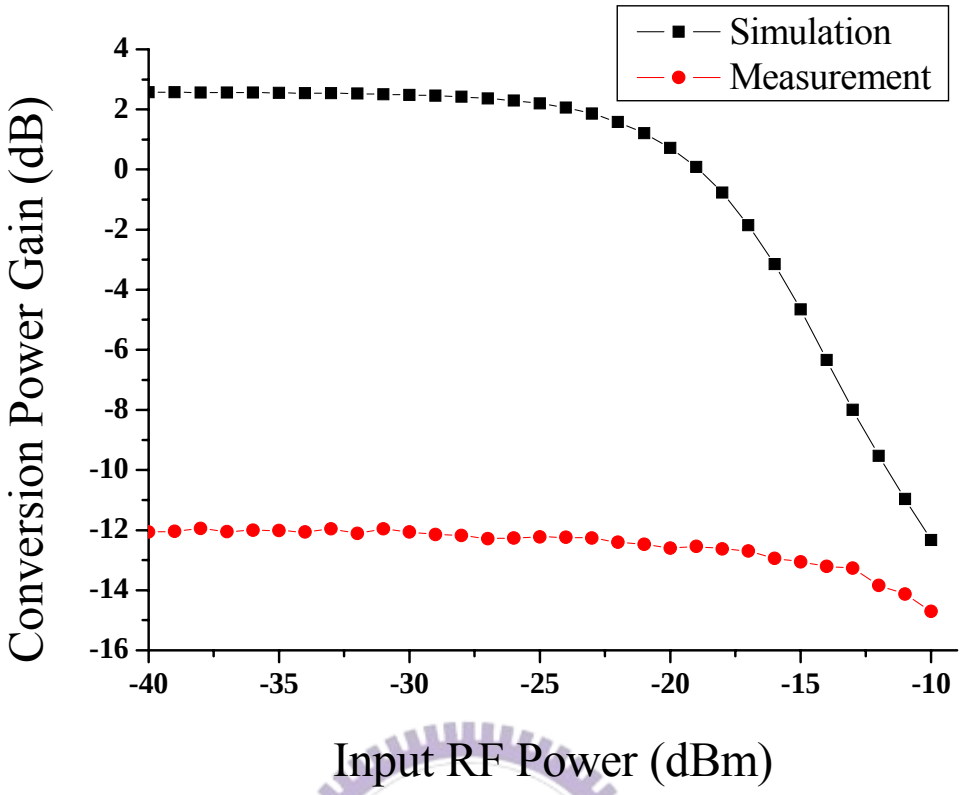


Figure 3.4.10 Comparison between simulation and measurement of P_{1dB} of 5.25GHz front-end

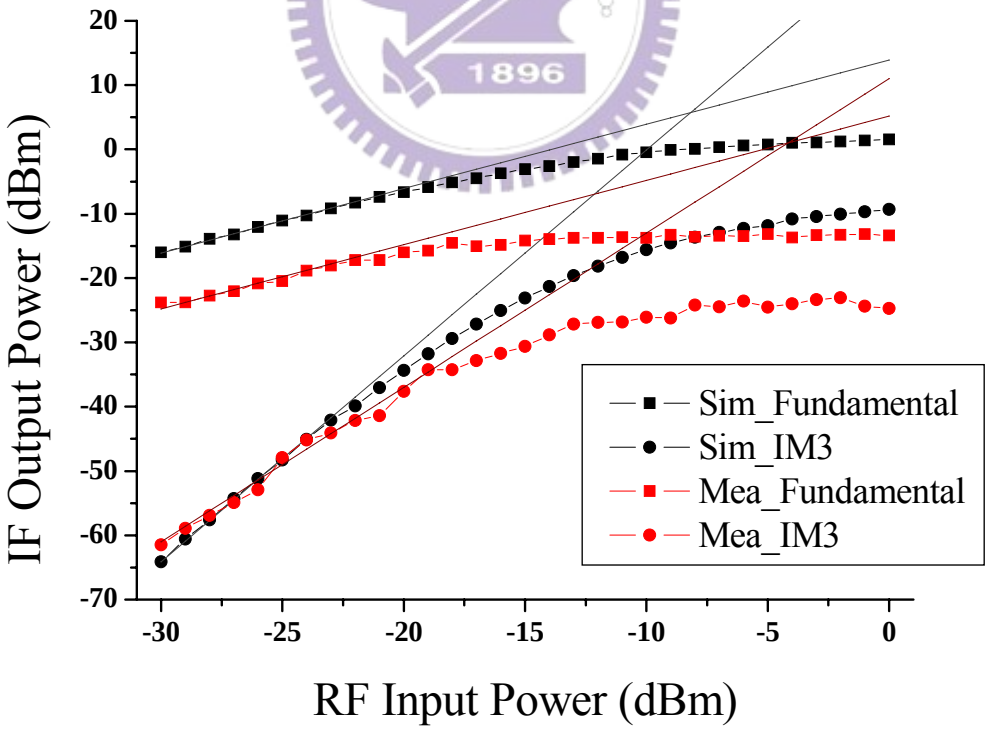


Figure 3.4.11 Comparison between simulation and measurement of IIP3 for 2.45GHz front-end

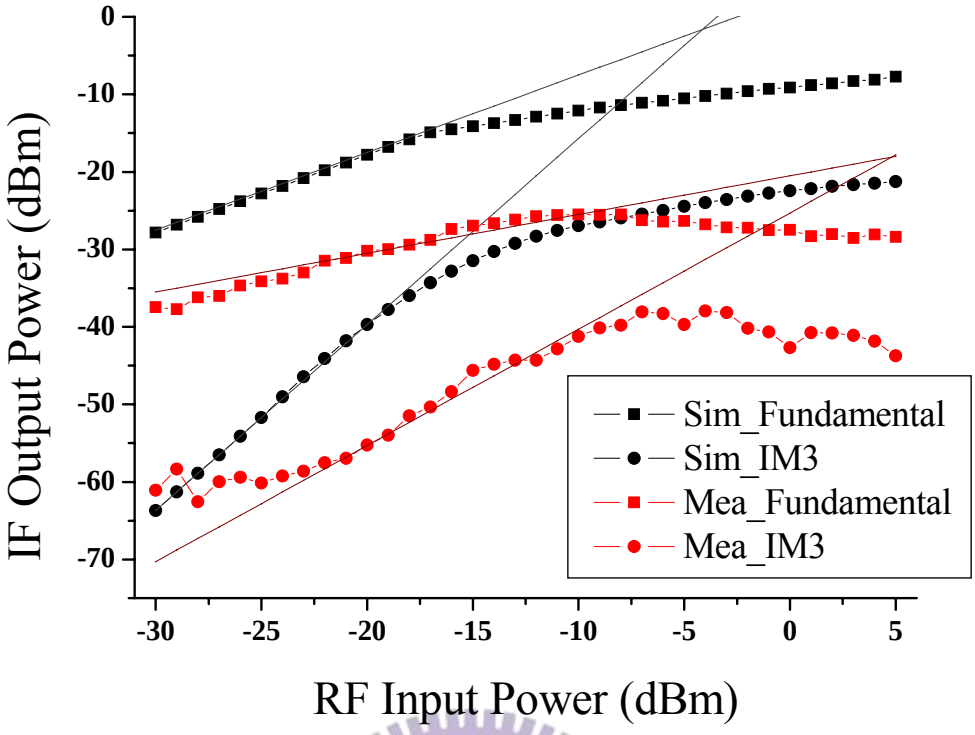
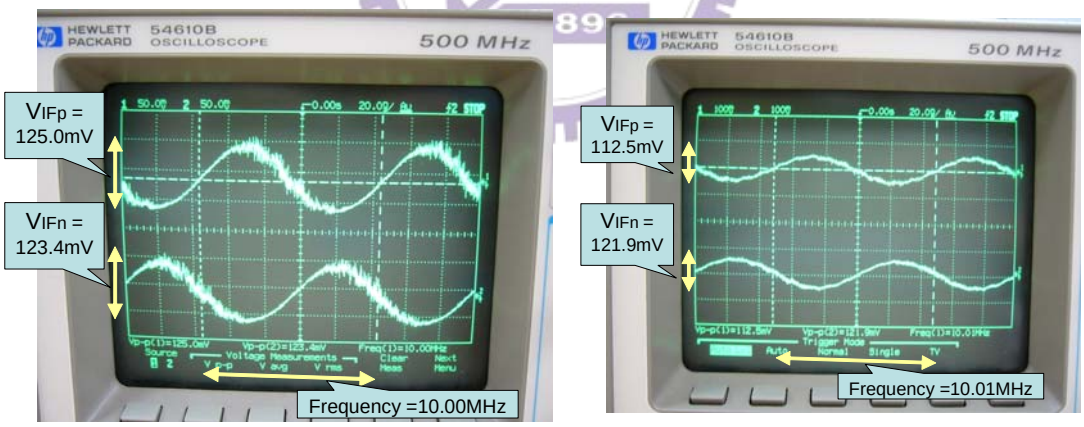


Figure 3.4.12 Comparison between simulation and measurement of IIP3 for 5.25GHz front-end



(a) (b)

Figure 3.4.13 Output waveform of (a) 2.45GHz (b) 5.25GHz front-end

3.5 Comparisons

Table 3.5.1 shows the comparisons of this work and other recently dual-band receiver front-end papers. Compared with other dual-band front-end this work achieves comparable performances with nearly equal chip area and lower power dissipation under concurrent operation for two frequency bands.

Table 3.5.1 Comparisons of dual-band receiver front-end

Ref	[2] 2004		[22] 2004		[23] 2005		This Work			
Process	CMOS 0.18um		CMOS 0.18um		CMOS 0.18um		CMOS 0.18um			
Power	41.5mw @1.8V		24mw @1.8V		53.9mw* @1.8V		17.9mw @1.8V		28.8mw @1.8V	
Frequency (GHz)	2.4	5.15	2.4	5.2	2	5	2.45	5.25	2.45	5.25
Gain (dB)	39.8	29.2	20	18.8	33	31	26.5	19.9	17.2	11.8
S11 (dB)	-8	-10.8	N/A	N/A	<-15	<-15	-18.4	-13.4	-15.9	-15.8
NF (dB)	1.5	4.1	3.1	3.55	4.7	5.1	3.77	7.28	7.22	10.7
P1dB (dBm)	-21	-12	N/A	N/A	N/A	N/A	-20.6	-22.1	-20.0	-15.3
IIP3 (dBm)	-12.7	-4.1	-13.4	-11.4	-1	-11.8	-7.8	-4.5	-4.2	4.9
Condition	Mea.		Mea.		Mea.		Sim.		Mea.	
Architecture	switched dual-band LNA+ Gilbert mixers		concurrent dual-band LNA + Gilbert mixers		two LNAs + Gilbert mixers		concurrent dual-band LNA + sub-harmonic mixers			
Chip area (mm^2)	0.98 x 1.13		1.21 x 1.46		1.4 x 3.5		1.45 x 1.45			

*：IF mixer is included

Chapter 4

Low-Voltage Micromixer

4.1 Review of Basic Micromixer

The down-conversion mixer is a key building block in a receiver system. Its main function is to translate the incoming RF signal to an intermediate frequency for further processing. It dominates the system linearity and determines the performance requirements of its adjacent blocks. Among many proposed active mixers the Gilbert-cell mixer has been widely used because of it's LO suppression at the IF output. However the circuit linearity is limited by MOSFET transistor linearity, which is the common source MOSFET transconductance [24]. The small-signal linearity of the input stage, and thus the third-order intercept point, can be greatly improved using several techniques, notably, source degeneration, the multi-tanh doublet and triplet. However the 1-dB gain compression point still falls short of what may be required in handling large input signals without significant intermodulation. Further these RF stages do not provide an accurate match to the source [25]. Therefore the micromixer was proposed in [25] to overcome these problems. The topology of the basic micromixer is shown in Figure 4.1.1.

The micromixer follows the general form of Gilbert-cell mixer except for the use of a bisymmetric class-AB RF stage based on the translinear principles while the mixer core is identical to the Gilbert-cell mixer. The class-AB RF stage provides well-defined matching impedance and much lower input related nonlinearity.

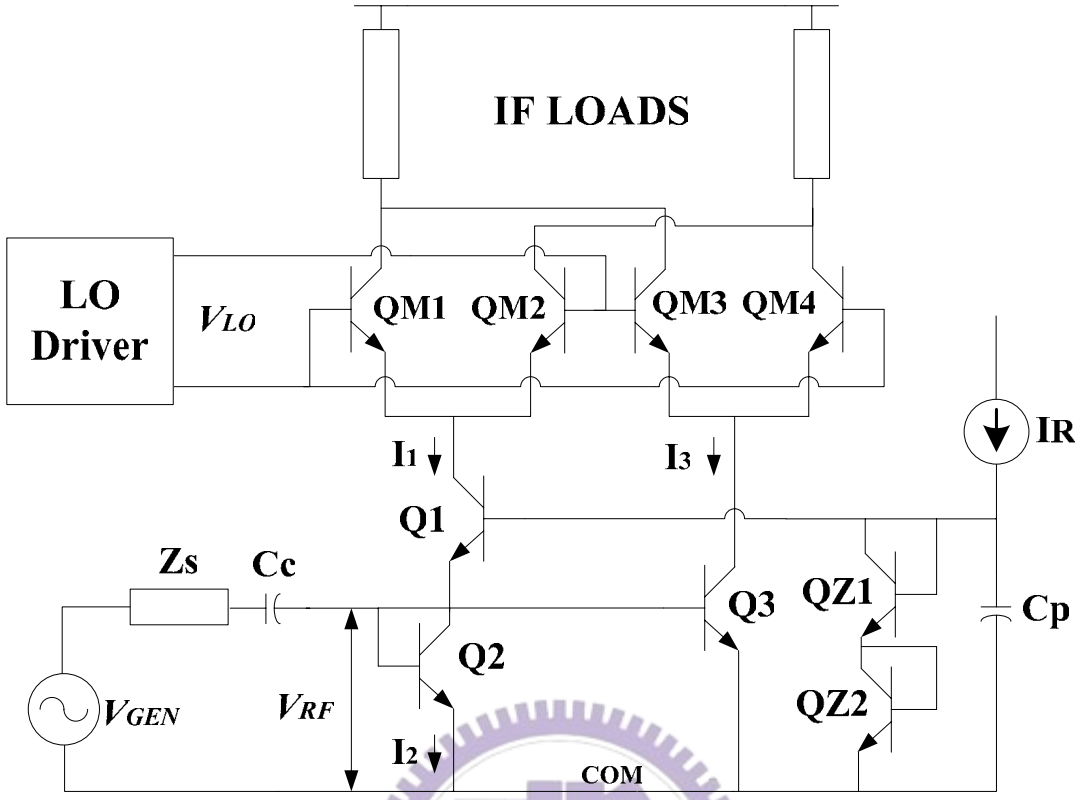


Figure 4.1.1 Basic micromixer

Although the micromixer does not have inherent gain compression in RF stage, the 1-dB compression point of the micromixer will often be determined by limitations on the output IF signal amplitude, rather than by the RF stage. The noise figure of the micromixer depends on design details and is acceptable for many receiver applications although it is generally not as low as in mixers specially optimized for noise performance.

In Figure 4.1.1, Q1 can be viewed as a grounded-base stage. It delivers its output I_1 to the mixer pair QM1-QM2 in phase. It can, in principle, handle unlimited amounts of current during large negative excursion of V_{GEN}. On the other hand, the current mirror sub-cell Q2-Q3 can handle essentially unlimited amounts of current during positive excursion of V_{GEN} both at its input node and at its inverted-phase current output I_3, which drives QM3-QM4. Acting together, these two sub-cells provide an

overall transfer characteristic which is symmetric to both positive and negative inputs, and which is in principle not limited by the choice of bias level. The differential current output I_1-I_3 is linear with I_{RF}, although the individual currents are quite nonlinear. [25]

Because of the advantage of easily matching and wide dynamic range the micromixer is also applied to the CMOS process in recently years [26]. Replacing the BJT with MOSFET, we can derive two simple expressions for low-frequency small-signal input resistance and voltage gain under the assumption of ideal transistors and neglecting parasitic effects for simplifying [27]. The low frequency small-signal input resistance of RF input stage is approximately

$$R_{IN} = \mathrm{Re}(Z_{in}) = \frac{1}{2g_m} \tag{4.1}$$

which implies the micromixer RF input stage can be matched to 50Ω as long as we choose proper bias current. Assume perfect impedance matching to 50Ω, the low frequency small-signal voltage gain is approximately

$$G_V \equiv \frac{V_{IF}}{V_{RF}} \approx \frac{1}{2} \cdot g_m \cdot \frac{2}{\pi} \cdot 2R_L = \frac{2}{\pi} \cdot g_m R_L \tag{4.2}$$

These two equations will be very helpful when designing the micromixer.

4.2 Low-Voltage Micromixer

In recent years low-voltage circuit design has become an important issue because of the consideration of battery design and power reduction. However the traditional micromixer is inapplicable for the low voltage design due to the stack of the four stage cascode architecture. Here we propose a modified micromixer applicable for low-voltage operation, as shown in Figure 4.2.1.

The main improvement of the low-voltage micromixer is the RF stage, while the switch-stage of the low-voltage micromixer is identical to the basic micromixer. The RF signal is feed in between R_1 and M_2, and coupled to the RF stage by $CcRF_1$ and $CcRF_2$. We bias the transistors M_1 and M_2 separately using V_{g1} and V_{g2}. The improved RF stage overcomes the bias-relative problem and retains the characteristic of class

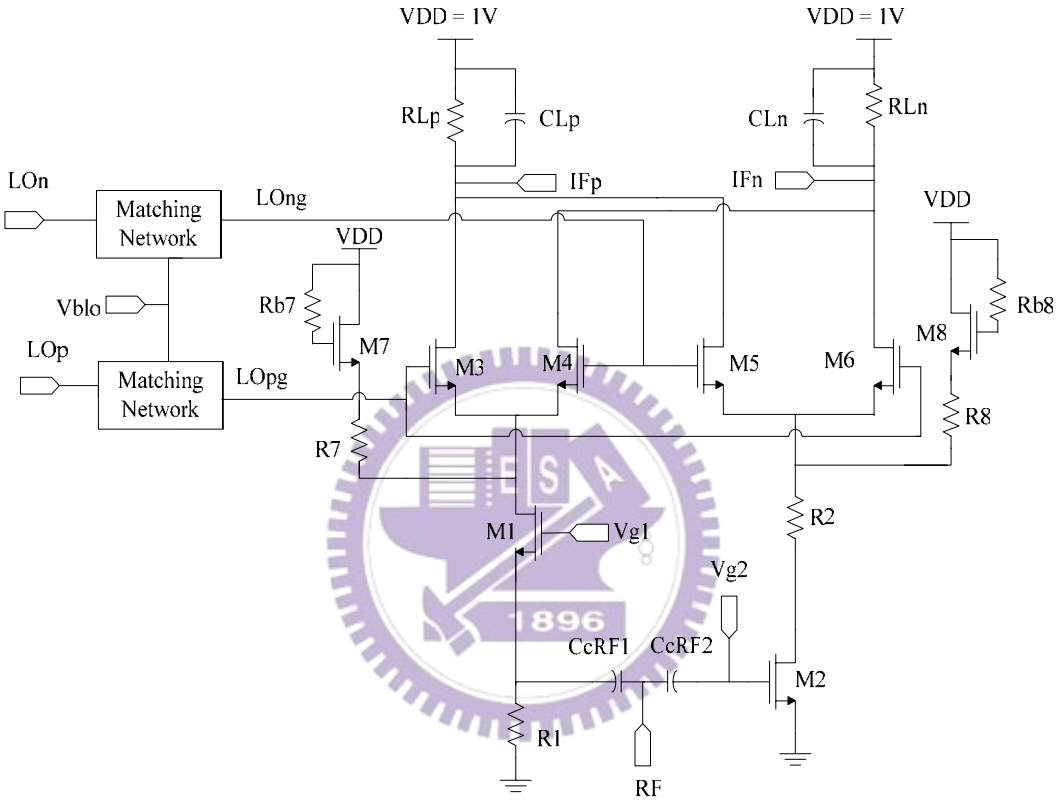


Figure 4.2.1 Low-voltage micromixer

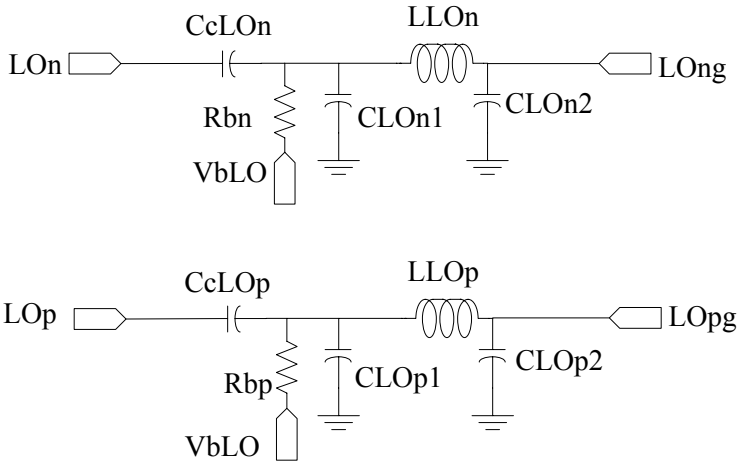


Figure 4.2.2 LO matching network

AB stage in the basic micromixer. The pi-matching network is added at the LO port for the narrow band input matching to 50 ohms for measurement consideration. Figure 4.2.2 shows the topology of the LO port on-chip pi-matching network composed of two MIM capacitors and one spiral inductor. The LO stage bias voltage is feed with bias resistors in the matching network. To keep the output IF waveform symmetric the two resistors R_1 and R_2 in the RF stage adjust the transconductance and current balance of M_1 and M_2.

In the low-voltage micromixer we adopt the charge injection method to improve the gain [28]. According the relationship of transconductance and IP3 with current in the traditional mixer architecture

$$A_v = \sqrt{K_n I_{ss}} R_L \frac{2}{\pi} \tag{4.3}$$

$$IP3 \approx \sqrt{\frac{32}{3} \frac{I_{ss}}{\beta_n}} \tag{4.4}$$

which imply the mixer gain and IP3 are proportional to the bias current flowing in the input MOSFETs, $\sqrt{I_{SS}}$. Because the micomixer has identical operational model as the Gilbert-cell mixer, the two equations are also applicable to the micromixer. The charge injection method can improve the micromixer gain and linearity, compensating the disadvantage of low supply voltage and low transconductance in CMOS process. In Figure 4.2.1, M_7 and M_8 work as current sources, and provide extra charge current feeding into the RF stage. R_7 and R_8 provide high impedance to prevent the small signal from going to the current sources so that the charge injection stage will not interfere with the function of low-voltage micromixer.

4.3 Layout and Measurement Considerations

The circuits elements of low-voltage micromixer are all on-chip except for the IF port low pass filters, so we choose the PCB (printed circuit board) on-board testing for the micromixer. The layout of low-voltage micromixer is shown in Figure 4.3.1 and chip photo is shown in Figure 4.3.2. The circuit occupies chip area of 1mm x 0.85mm. Figure 4.3.3 shows the on-board testing PCB layout. The photograph of the realized PCB with chip is shown in Figure 4.3.4.

The circuit ground and substrate are separated in the layout and the bondwire works as RF choke to prevent the circuit from the noisy substrate. In the design process the parasitic effects of bondwires and bond-pads have been taken into consideration. Typically, the inductance of bond wire is about 1nH per 1mm length and the parasitic capacitance of a 100umx100um bond-pad is approximate 150fF to the ground. We also consider the process variation by the TT, FF and SS corner simulations with libraries provided by the foundry.

Two extra circuits are needed in the measurement of low-voltage micromixer. First the LO ports use a differential 2.44GHz signal so we need a balun suitable for 2.44GHz to convert the signal generator output to differential form. Secondly to filter out the high frequency noise in the 10MHz output waveform, the IF low pass filters composed with lumped resistors and capacitors are made on board at the IF output pads. The simplified block diagram of PCB on-board testing is shown in Figure 4.3.5. We can follow the simplified block diagram to measure the RF and LO port input return loss, conversion gain, third-order intercept point, and noise figure of the low-voltage micromixer. It should be noted that the losses of cable, balun, SMA connectors, and PCB board itself must be taken account for calibration and calculation in measurement results.

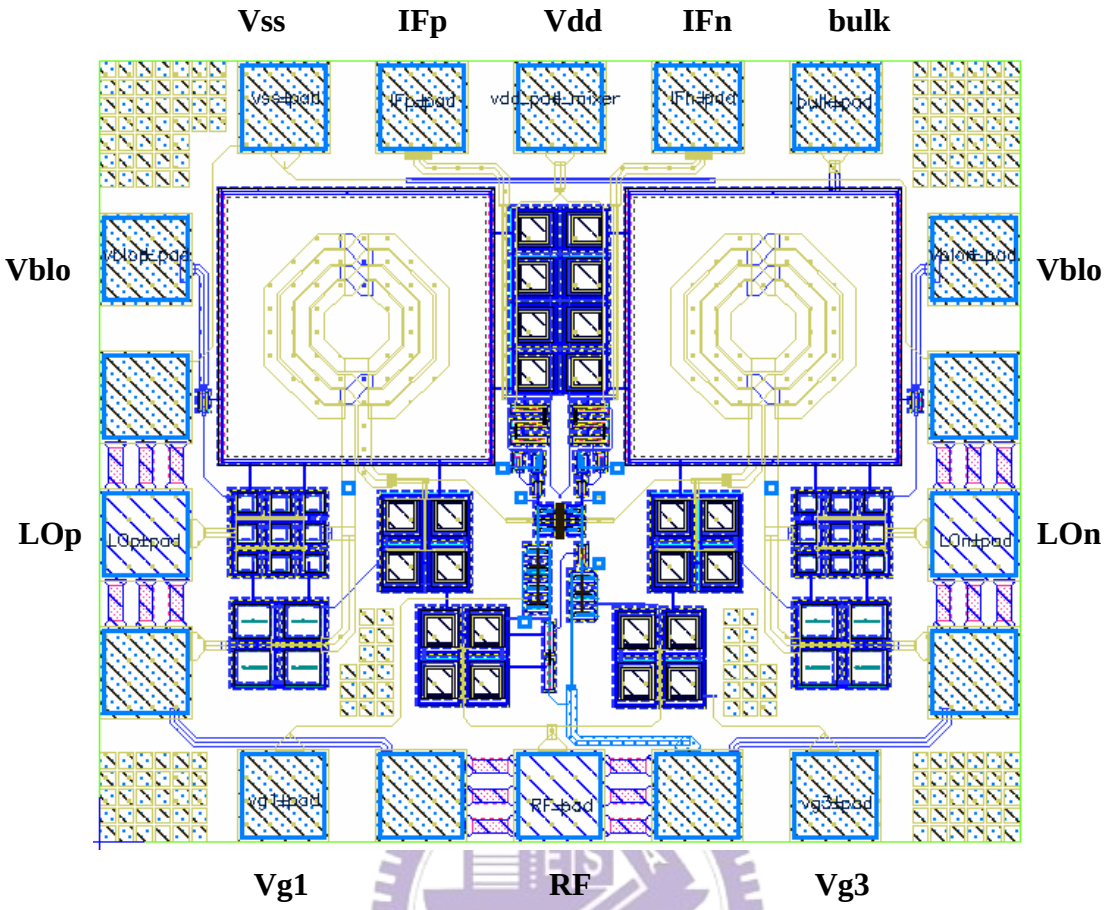


Figure 4.3.1 Chip layout of low-voltage micromixer

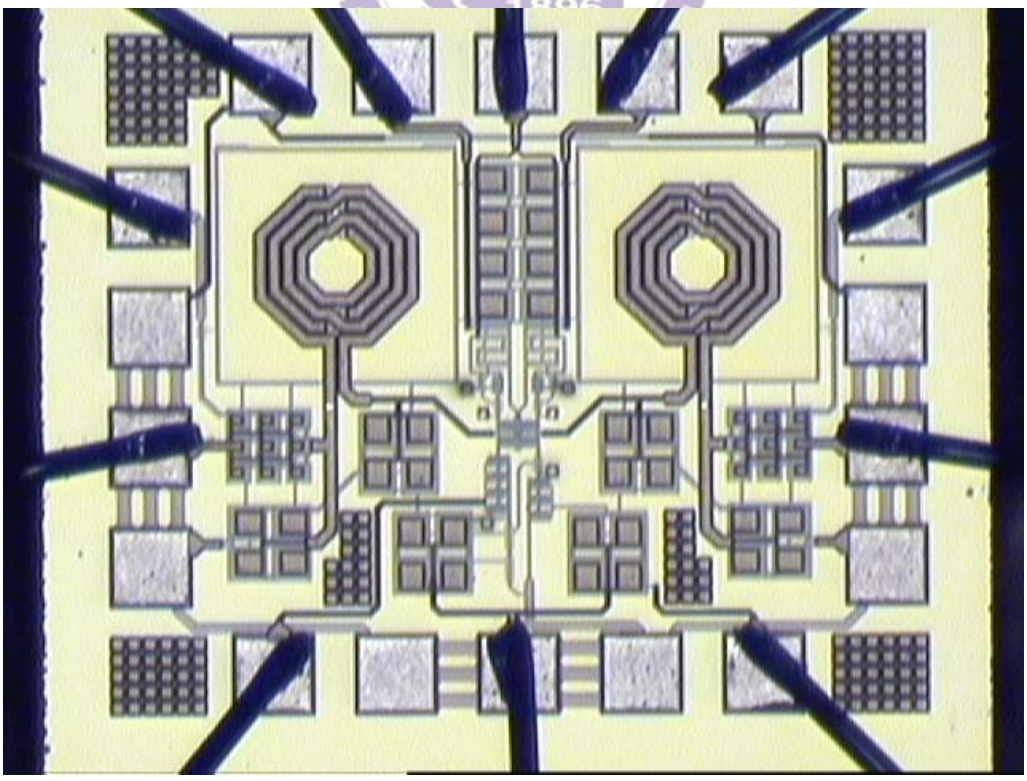


Figure 4.3.2 Chip photo of low-voltage micromixer

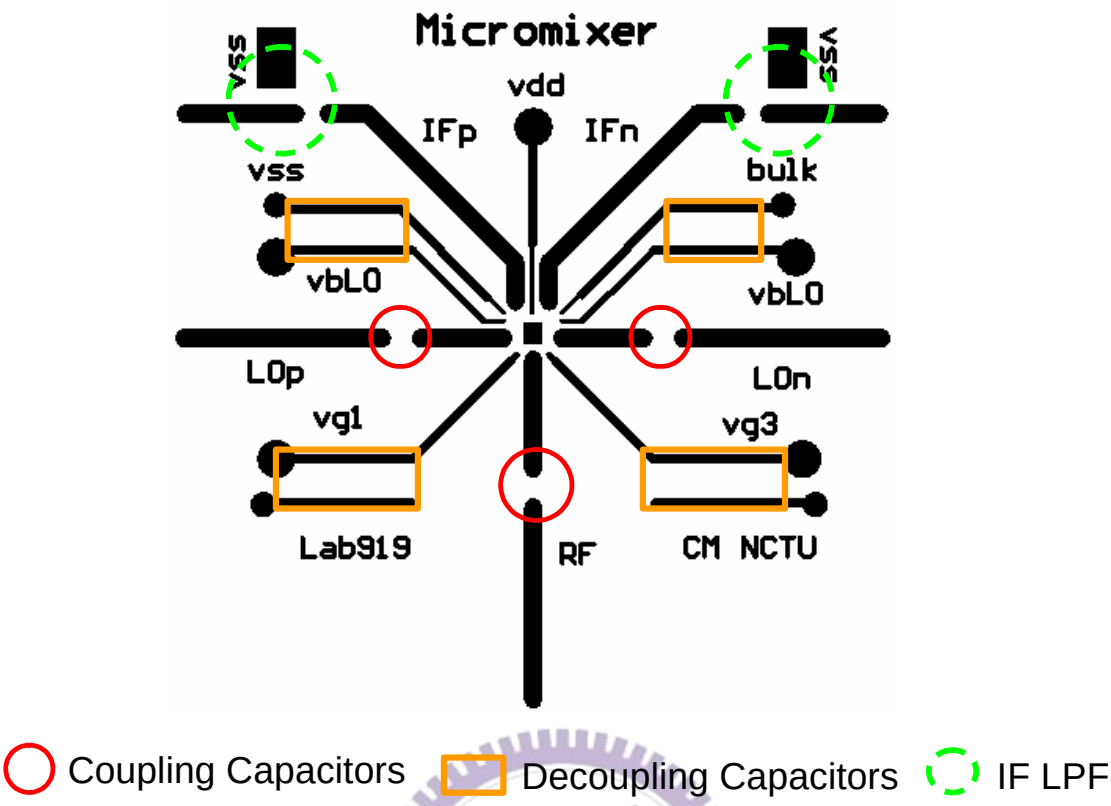


Figure 4.3.3 PCB layout for low-voltage micromixer

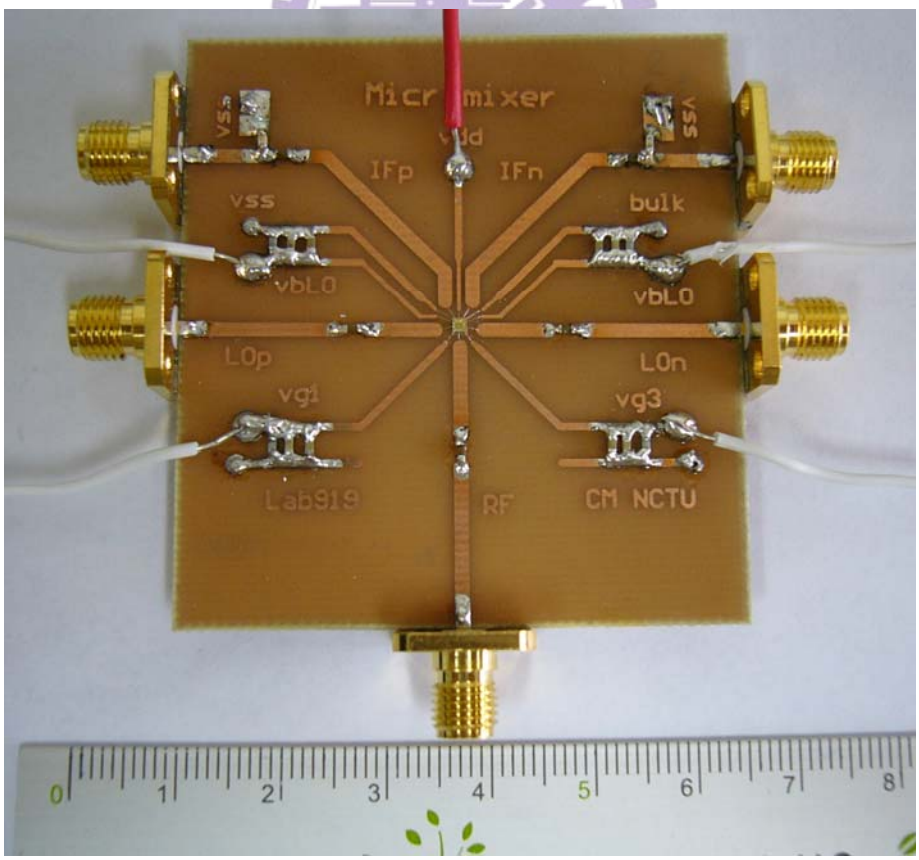


Figure 4.3.4 Photograph of PCB for low-voltage micromixer

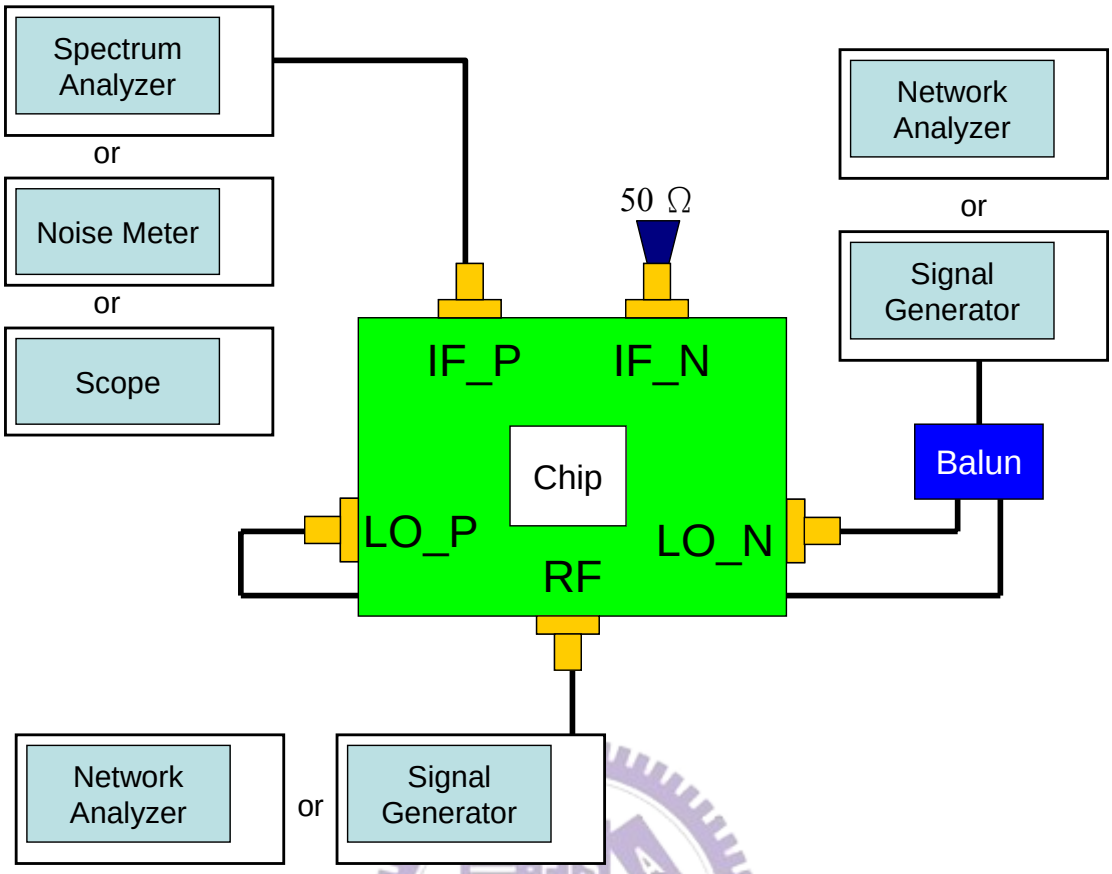


Figure 4.3.5 Simplified block diagram of PCB on-board testing for micromixer

4.4 Experimental Results and Discussions

The low-voltage micromixer was simulated and fabricated using CMOS 0.18um process. The measurement results shows that it has 14.9 dB RF port return loss, 8.28 dB conversion voltage gain, -5.63 dBm P_{1dB}, and 4.21 dBm IIP3. The total power dissipation of the low-voltage micromixer is 1.72mw from 1V voltage supply. Figure 4.4.1 shows the RF port input return loss is better than 10 dB between 2.1GHz and 4.2GHz, which proves the well-defined input impedance of micromixer topology. Figure 4.4.2 shows the measured optimum LO power is 0 dBm while the simulated one is -5 dBm for the maximum conversion voltage gain. The measured conversion voltage gain is a little bit less than simulation, which may be caused by less power consumption. The linearity of the low-voltage micromixer is characterized by 1dB

compression point and third-order intercept point. Figure 4.4.3 shows the 1dB compression point and Figure 4.4.4 shows the third-order intercept point. In summary the measurement results are very close to simulations. The low-voltage micromixer has good RF port matching, high conversion gain, high linearity, and very low power consumption under 1V low power supply. The differential 10MHz IF output waveforms are shown in Figure 4.4.5. Table 4.4.1 summaries the simulation and measurement performance of the low-voltage micromixer.

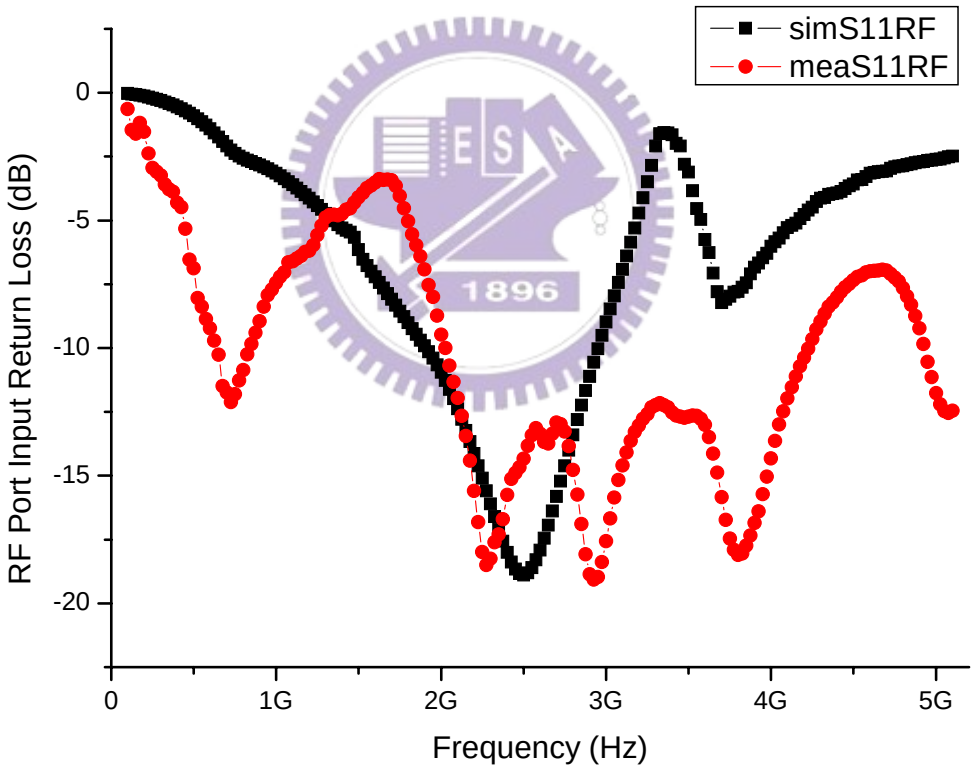


Figure 4.4.1 Comparisons between simulation and measurement of RF port input return loss

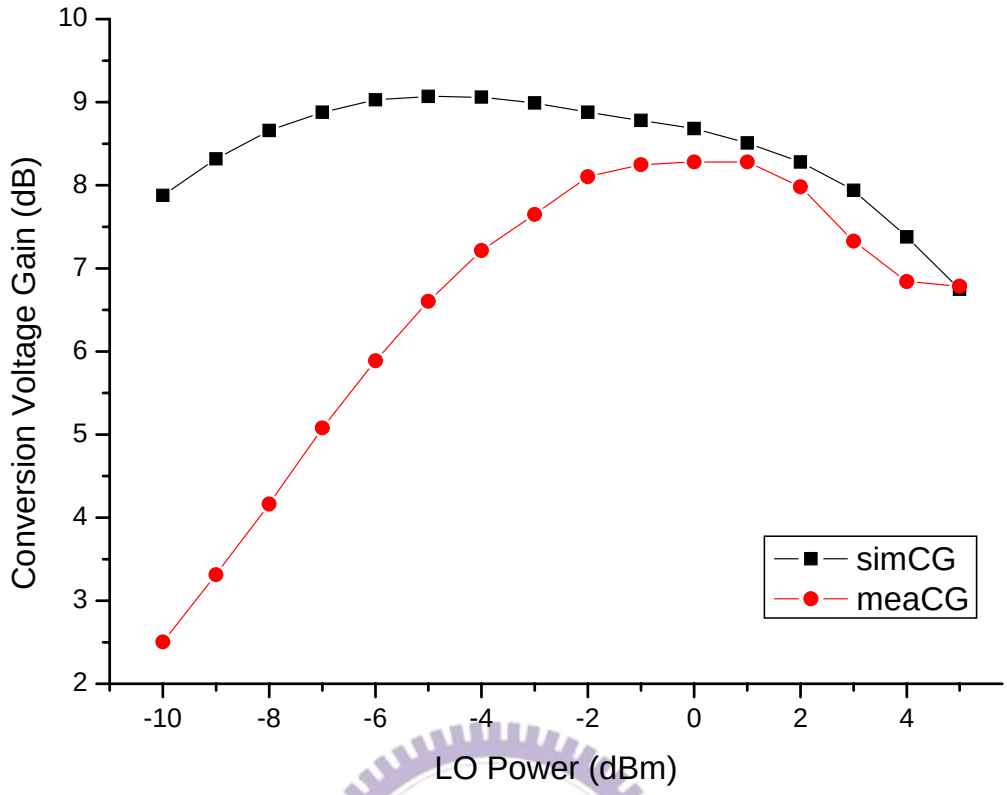


Figure 4.4.2 Comparisons between simulation and measurement of conversion gain and optimum LO power

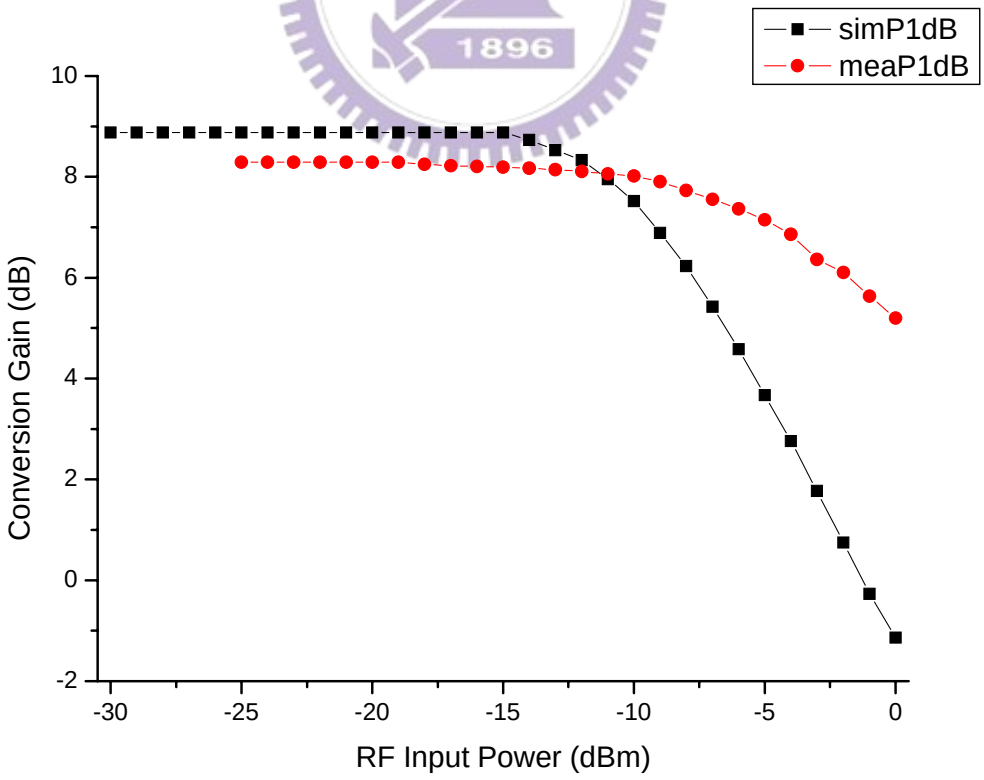


Figure 4.4.3 Comparison between simulation and measurement of 1dB compression point

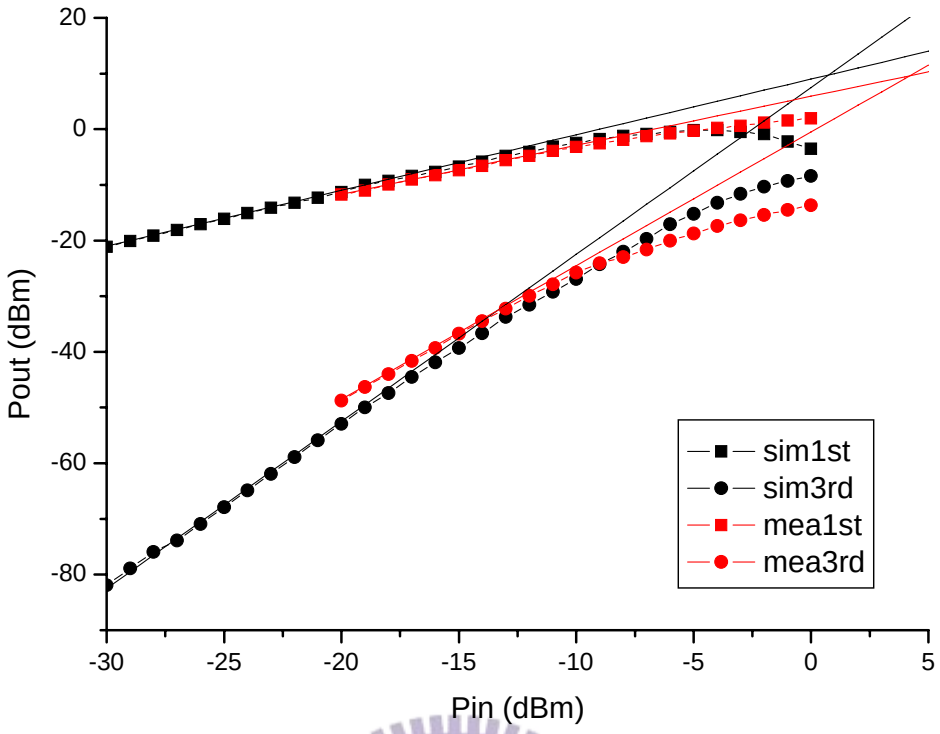


Figure 4.4.4 Comparison between simulation and measurement of third order intercept point

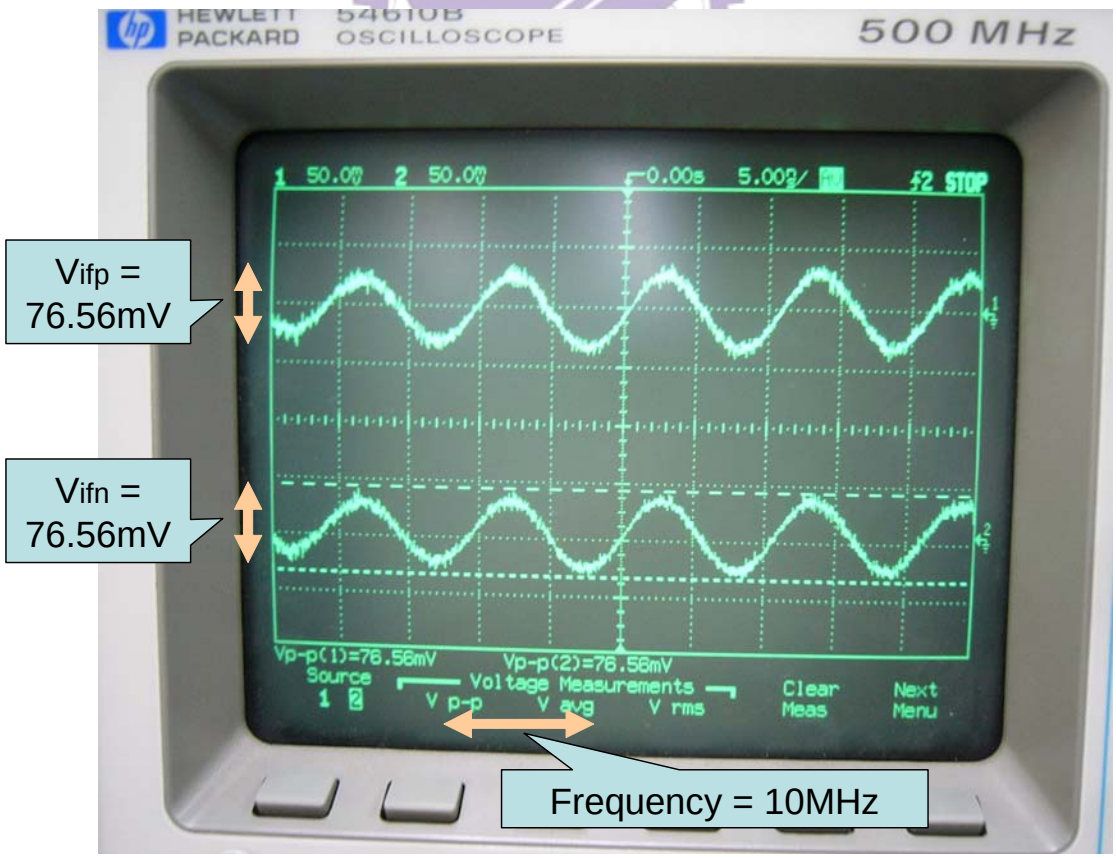


Figure 4.4.5 Output waveform of low-voltage micromixer

Table 4.4.1 Performance summary of low-voltage micromixer

	Simulation	Measurement
Supply Voltage (V)	1	1
Current (mA)	1.80	1.72
RF port RL (dB)	14.2	14.9
Conversion Voltage Gain (dB)	8.88	8.28
Noise Figure (dB)	13.0	N/A
P-1dB (dBm)	-10.8	-5.63
IIP3 (dBm)	0.75	4.21

4.5 Comparisons

Table 4.5.1 shows the comparisons of this work and other low-voltage mixers. Compared with other low-voltage mixers, this work has well-defined RF port input matching, comparable conversion gain, higher linearity and lower power dissipation under 1V low supply voltage.

Table 4.5.1 Comparisons of low-voltage mixers

Ref	[29] 2003	[30] 2004	[31] 2004	This Work	
Process	CMOS 0.13um	CMOS 0.35um	CMOS 0.18um	CMOS 0.18um	
Power	40mw @1V	9.4mw @2V	2.8mw @1V	1.8mw @1V	1.72mw @1V
Frequency	RF=2.15GHz IF=150MHz	RF=2.4GHz IF=100MHz	RF=2.4GHz IF=1MHz	RF=2.45GHz IF=10MHz	
Gain (dB)	5.5	9.48	9	8.88	8.28
NF (dB)	14.5	17.6	12	13.0	N/A
P_{1dB} (dBm)	-10	-8.72	N/A	-10.8	-5.63
IIP3 (dBm)	0	3	-1	0.75	4.21
Condition	Mea.	Sim.	Sim.	Sim.	Mea.
Topology	transformer based	dual-gate	folded-switching	micromixer	

Chapter 5

Conclusion and Future Work

5.1 Conclusion

This thesis analyzes the design method of concurrent dual-band LNA, and this circuit is demonstrated with balanced performance in both frequency bands. A concurrent dual-band receiver front-end is composed of the former LNA and sub-harmonic mixers. The receiver front-end needs only one frequency synthesizer with turning range of around 2.4GHz for 802.11a/b/g applications. Finally a low-voltage micromixer is proposed and demonstrated with low power consumption, high conversion gain and high linearity. The three ICs have been fabricated using CMOS 0.18um process. In this thesis we have presented the design concepts, simulation results, experimental results, discussions and comparisons for the two works. All of the circuits were simulated by Eldo-RF and measured in CIC.

The concurrent dual-band LNA topology is studied and analyzed in three respects, including input matching, noise figure, and power dissipation. These characteristics are analyzed in terms of circuit elements. Some simulations are also demonstrated to prove the analysis equations. The analysis equations for single-band LAN are also provided in the thesis to make a comparison clearly for readers. This circuit is designed and implemented using CMOS 0.18um process. It achieves balanced performances in two frequency bands though the lower band has been shifted from 2.45GHz to 2GHz because of variation of on-chip passive elements. The measured

data reveals 7.45 dB and 6.06 dB power gain, -12.8 dB and -12.9 dB input return loss, 3.54 dB and 4.80 dB noise figure, -7.43 dBm and -9.66 dBm P_{1dB}, and 6.84 dBm and 2.76 dBm IIP3 at 2GHz and 5.25Gz, respectively. It dissipates low power consumption of 7.21mw from 1.8V power supply.

Developing the receiver architecture inheriting from the dual-band LNA, a concurrent dual-band receiver front-end is designed and implemented based on a new RF dual-band receiver architecture for IEEE 802.11a/b/g. The new dual-band receiver architecture needs only one frequency synthesizer with tuning range of around 2.4GHz, rather two frequency synthesizers, by employing a sub-harmonic mixer which operates at 5.25GHz and needs LO signal of 2.62GHz. The dual-band receiver front-end consists of a differential concurrent dual-band LNA, which has a similar topology of the former one, a sub-harmonic mixer and a modified Gilbert-cell mixer, which are designed by the other co-agent in [20]. The two mixers adopt the same topology, which reduces the design complexity of the receiver front-end.

The front-end is also designed and implemented using CMOS 0.18um process. It performances 17.2 dB and 11.8 dB voltage gain, -15.9 dB and -15.8 dB RF port input return loss, 7.22 dB and 10.78 dB noise figure, -21.0 dBm and -15.3 dBm P_{1dB} and -4.2 dBm and 4.9 dBm IIP3 at 2.45GHz and 5.25Gz, respectively. The total power dissipation is 28.8mw from 1.8V power supply. Compared with other dual-band front-end this work achieves comparable performances with nearly equal chip are and lower power dissipation under concurrent operation for two frequency bands.

The low-voltage micromixer, which is modified from the basic micromixer, is proposed in the thesis. The RF signal is feed between R_1 and M_2 by the two coupling capacitors $CcRF_1$ and $CcRF_2$ so that M_1 and M_2 can be biased separately using V_{g1} and V_{g2}. The charge injection method can improve the micromixer gain and linearity, compensating the disadvantage of low supply voltage and low transconductance in

CMOS process. The measurement results shows that it has 14.9 dB RF port return loss, 8.28 dB conversion voltage gain, -5.63 dBm P_{1dB}, and 4.21 dBm IIP3. The total power dissipation of the low-voltage micromixer is 1.72mw from 1V voltage supply. The measurement results approximately meet the simulation results.

5.2 Future Work

For higher frequency applications more accurate RF CMOS component models such as large size MIM capacitors and different inductance spiral inductors with higher Q-value should be built up for exactly matching network design in the future. All parasitic effects including parasitic capacitance, resistance and inductance must be considered more carefully. A more accurate and efficient EDA tool for extracting parasitic effects is quietly important.

The concurrent dual-band LNA may be improved as gain-controllable one for higher dynamic linearity application and lower noise figure to depress the total noise figure of the receiver. As for the dual-band receiver front-end, it has been proved as feasible by the implementation in this thesis, so the fully integrated dual-band transceiver, including receiver front-end, power amplifier, up-mixer, quadrature VCO, multi-modulus frequency synthesizer, and IF Gm-C filters may be realized for future system-on-chip (SOC) design. The multi-band or wide-band transceiver innovation marching forwards SOC design, either in circuit topology or transceiver architecture will be the most challenging design in the future.

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