國立交通大學

電信工程學系碩士班

碩 士 論 文

射頻 BiCMOS 功率放大器設計

用於 IEEE 802.11a/b/g 與藍芽系統

RF BiCMOS Power Amplifier Design

For IEEE 802.11a/b/g and Bluetooth Systems

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A Thesis

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中文摘要

這篇論文的第一部分敘述一個適用於無線區域網路 802.11a 及 802.11b/g 之雙頻帶 CMOS 前驅放大器，為了線性度及效率的考量選擇 Class AB 的偏壓點，並設計閘極偏壓電路以求電源供應簡單化。利用兩個類似 Diplexer 形式的電路，以集總元件在印刷電路板上設計出所需單一輸入/單一輸出端的雙頻匹配網路。量測結果所示 P_{1dB} 在 2.4-GHz 和 5.2-GHz 為 8.3dBm 及 7.2dBm，所對應的功率增加效率分別為 17.1%、9.3%。

論文的第二部分則敘述兩個適用於藍芽系統之 SiGe BiCMOS Class F 功率放大器。第一個功率放大器以集總元件在 PCB 板上設計輸入/輸出匹配電路及諧波負載網路。量測結果顯示此放大器可提供約 20dBm 之輸出功率，功率增加效率約為 40%。承接第一次的設計經驗，第二個功率放大器為全整合 Class F 功率放大器，唯輸出匹配電路在晶片之外。量測結果所示輸出功率為 20dBm，功率增加效率為 34.2%。

RF BiCMOS Power Amplifier Design
For IEEE 802.11a/b/g and Bluetooth Systems

Student: Jia-Liang Chen Advisor: Dr. Christina F. Jou

Institute of Communication Engineering

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Abstract

The first part of this thesis describes a dual-band driver amplifier for WLAN 802.11a and 802.11b/g applications. For the concern of linearity and efficiency, Class AB biasing is chosen for this amplifier, and an on-chip biasing network is designed to simplify the usage of power supply. The single-input/single-output dual-band matching networks are implemented by two Diplexer-liked networks composed of lumped elements on PCB. Measurement results show that P_{1dB} in 2.4-GHz and 5.2-GHz are 8.3dBm and 7.2dBm, with corresponding PAE of 17.1% and 9.3%, respectively.

The second part of this thesis describes two SiGe BiCMOS Class F power amplifiers for Bluetooth system. The input/output matching and harmonic loading networks of the first Class F power amplifier are composed of lumped elements on PCB. Measurement results show that the amplifier could provide an output power of about 20dBm with PAE of about 40%. From the experience of the first design, the second is a fully integrated Class F power amplifier, leaving only the output matching network off-chip. Experiment results show that the output power is 20dBm, and the PAE is 34.2%.

Acknowledgement

首先要感謝我的指導教授周復芳老師，從大三專題進入實驗室起即感受老師的關懷，讓我們在喜歡的研究領域自由發揮，並給予良好的環境使研究更加順利。

也要感謝博士班鄭國華學長在專業領域上提供許多寶貴的意見，引領我在 IC 設計的世界裡成長茁壯，並不厭其煩地指導我在研究上遇到的困難，引領我正確的方向。以及胡政吉學長在量測方面所給予的指導和意見，讓我能夠迅速找到問題的癥結，及時採取對應補救的措施，不至於浪費寶貴的時間與晶片。

其次要感謝這幾年來實驗室的學長姐及同學、學弟們，你們是我研究生涯裡不可或缺的夥伴，在一起的分享、學習和指教是我充實進步的原動力，更讓我能保持輕鬆愉快的心情從事研究。

最後要感謝我的家人和女友麗華，一路上給我最大的肯定和支持，讓我有信心面對所有的難題，順利地完成碩士學業。

所有關心和陪伴我的人們，祝福你們。

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Chapter 1
Introduction

1.1 Background

In recent years, wireless local-area network (WLAN) is fast growing owing to the insatiable demand for the market. For example, the wireless mobile devices in the enterprise, the seamless connectivity of networks inside/outside our home, and the wireless broad-band network between buildings and into homes are included of WLAN applications. With the Federal Communications Commission (FCC) allocation of 300-MHz bandwidth in the 5-GHz frequency band for the unlicensed national information infrastructure (UNII), high-data-rate (up to 54 Mb/s) WLANs become increasingly popular and important for mobile connectivity.

Table 1.1 Wireless Standards

Standard	Spectrum	Max. Data rate	Modulation scheme
802.11a	5 GHz	54 Mbps	OFDM
802.11b	2.4 GHz	11 Mbps	DSSS with CCK
802.11g	2.4 GHz	54 Mbps	OFDM (>20 Mbps) DSSS with CCK (<20 Mbps)
Bluetooth	2.4 GHz	2 Mbps	FHSS
Home RF	2.4 GHz	10 Mbps	FHSS
HiperLAN1	5 GHz	10 Mbps	CSMA/CA
HiperLAN2	5 GHz	54 Mbps	OFDM

The choice of the optimum semiconductor technology for wireless applications is a crucial issue. In the past few years, high-speed components such as silicon bipolar, SiGe heterojunction bipolar transistors (HBTs), CMOS as well as GaAs MESFET HBT and HBT were extensively announced and proposed. The argument of which is

the best technology is tedious and contentious, what we should do is to choose one that mostly fit to us from their characteristics. The key transistor technology figures of merit for RF design of wireless communication products are:

1. Shout current gain bandwidth (f_T) — important for analog and digital circuits;
2. Maximum power gain bandwidth ($f_{\max}$) — vital for analog and digital circuits;
3. Minimum noise figure — LNAs, wide dynamic range front ends, mixers;
4. Maximum power-added-efficiency (PAE) — power amplifiers;
5. Linearity — amplifier, front ends;
6. Yield — related to price and performance.

The various components' performance listed in 1994 with several compared competing semiconductor technologies appears in Table 1.2.

Table 1.2 Performances of various technologies for wireless communication

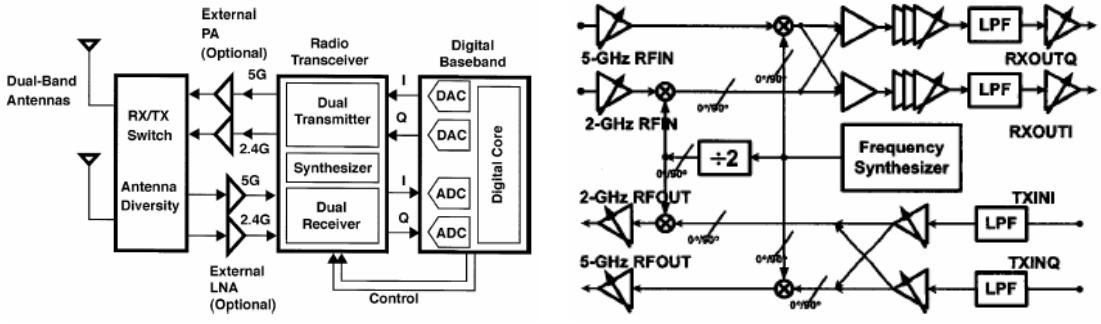
Spec.	Si BJT	Si/SiGe HBT	GaAs MESFET	GaAs HBT
f_T (GHz)	32	55	50	30
$f_{\max}$ (GHz)	35	55	60	70
$G_{\max}$ @2GHz(dB)	24	28	20	19
NF@2GHz(dB)	1.0	0.5	0.3	1.5
IP3/ P_{1dB}	9	9	12	16
PAE@3V(%)	--	70	60@5V	70

Recently, successful integration of receivers and transmitters on single chips has been reported [1-8]. Integrating one of the most important components in a transmitter – the power amplifier (PA), still remains a challenge. The PA stays a significant power consuming component in a transceiver, despite of the moderate levels of power requirements of applications such as Bluetooth and WLAN. Realizing PA's in CMOS is impeded by the technology's low breakdown voltage, low current drive, and lossy substrate, however pioneering efforts have demonstrated the

impairment of likelihood of full-scale integration of CMOS process. On the other hand, PA's dominated by Ⅲ/Ⅴ compound semiconductors could have excellent RF characteristics, but cost disadvantages. In order to realize a complete transceiver on a chip, issues related with power amplifier specifications, CMOS/BiCMOS PA designs had been dealt with in this thesis.

1.2 Introduction of Designed Circuits

The first work presents a 0.18 μm CMOS 2.45- & 5.25-GHz self-biased dual-band driver amplifier. It is designed since we attempt to implement a CMOS concurrent dual-band transceiver for IEEE 802.11a/b/g in the National Science Council (NSC) Project. Figure 1.1 indicates several architecture of the recently reported dual-band transceiver [1-8]. It is observed that most of them employ two completely separate signal paths to achieve dual-band mode. Though this approach is simple and results in better performance, it doubles the assemble area and number of components required, and consequently the cost. Furthermore, PA's of the transmitters are either external or omitted to mention.



(a) (b)

Figure 1.1 Recently reported dual-band transceiver architecture

The proposed dual-band transmitter and driver-amplifier topologies in this work are shown in Figure 1.2. It needs only one synthesizer because of the usage of

sub-harmonic mixer for 5.2-GHz path. Moreover, two paths could share the same concurrent dual-band amplifier. The approach of using a concurrent dual-band PA reduces the size and cost by almost half compared with using a conventional paralleled PA. Thus tremendous power consumption can be saved by this architecture. And due to the failure of the two-stage amplifier designed by the senior, this driver-amplifier is used for verifying the topology.

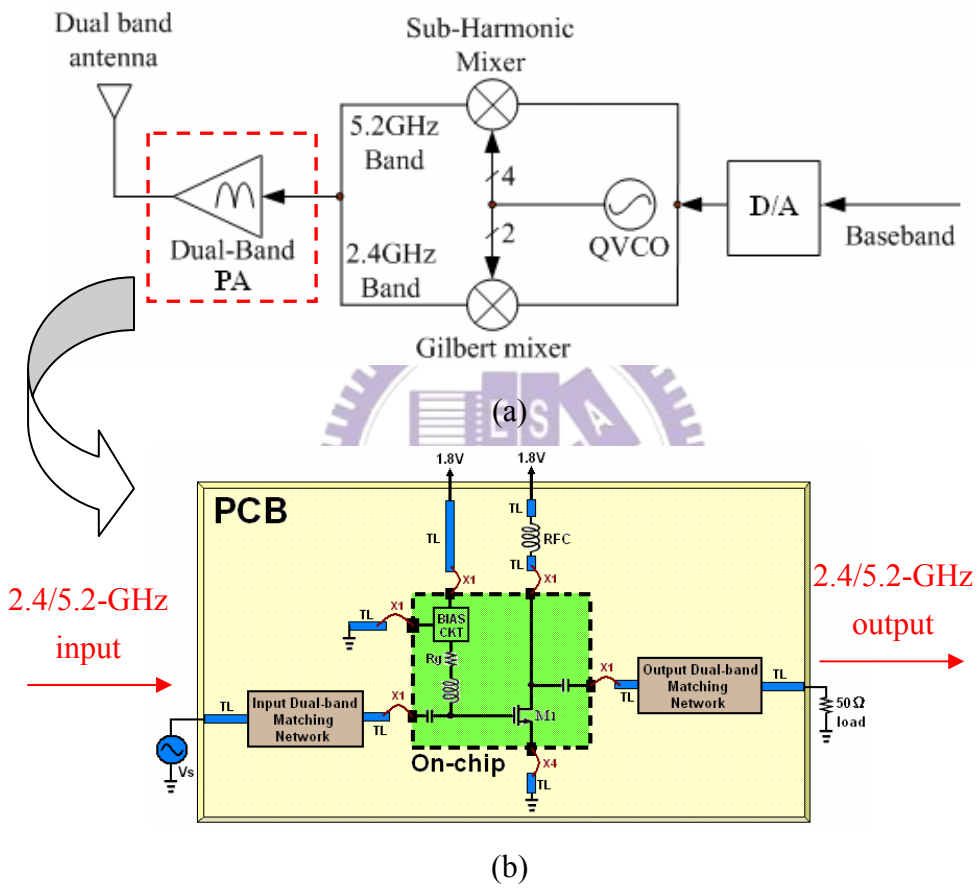
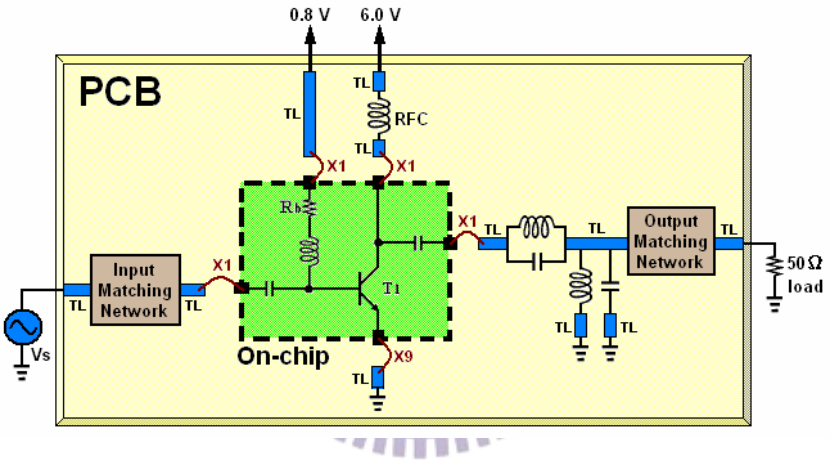


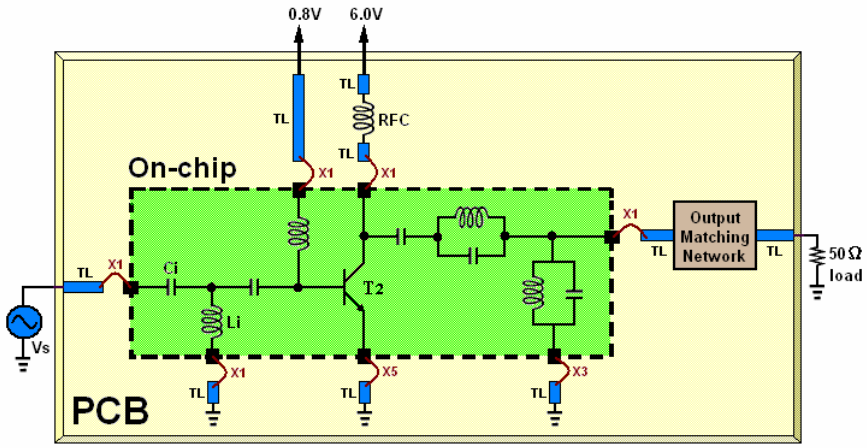
Figure 1.2 Proposed dual-band (a)transmitter (b)driver amplifier architecture

The second work contains two 0.35 μm SiGe 2.4-GHz Class F power amplifier designs. Without the drawbacks of CMOS process, SiGe HBT technology provides high gain and good thermal conductivity, which are especially useful for a power amplifier design. Aim of the work is the realization of a high efficiency power amplifier. Observing recent researches, only two types of amplifier tunings appropriate for high frequency operation, i.e., Class E and Class F, have been

explored. Since the attainable operation frequencies are somewhat higher than those for Class E circuits, Class F has been chosen for the design architecture. The first design (Figure 1.3(a)) utilizes Murata lumped elements to implement on-board input/output matching and harmonic loading networks. Except for the device characteristics verification, the usage of components with Q-factor higher than on-chip ones makes this design have another target: high performances. To further integrate the input matching and loading network components, efforts have been continuously made to complete the second design, a fully integrated Class F PA (Figure 1.3(b)).



(a)



(b)

Figure 1.3 Schematics of (a)the first (b)the second designed Class F power amplifiers

All the simulation and measurement results of the two works are shown in Table 1.3 (Dual-band driver amplifier) and Table 1.4 (Class F PA's), respectively. Comparison between the works and recently papers are also listed in the tables. The difference between simulation and measurement would be discussed in detail in chapter 2 and chapter 3.

Table 1.3 Comparisons of the dual-band driver amplifier with the previously reported PA's

Ref.	Process (μm)	Frequency (MHz)	Pout (dBm)	Gain (dB)	PAE (%)	Condition
[9] 2001	0.35 CMOS	2400	<17.5	<13.9	<16	Meas.
[10] 2002	0.18 CMOS	5200	15.4	14.1	27.1	Meas.
[11] 2003	0.25 CMOS	5250	11.8	5.3	8.0	Meas.
[12] 2003	0.25 CMOS	2450	21	19	26	Sim.
		5250	21	6.0	18	
[13] 2003	0.25 CMOS	2450	20	11.2	28	Meas.
[14] 2004	0.18 CMOS	2450	9.7	N/A	N/A	Meas.
		5250	19.5	>17.1	15.3	
[15] 2004	0.18 CMOS	5500	2.0	5.3	9.3	Meas.
[16] 2004	GaAs HBT	2450	27	25	42	Meas.
		5250	27.2	15	31.2	
[17] 2004	GaAs HBT	2450	27	<34	<40	Meas.
		5250	24	<25	<22	
This Work	0.18 CMOS	2450	10	9.0	24.8	Sim.
			8.3	6.3	17.1	Meas.
		5250	9.7	5.7	25.6	Sim.
			7.2	3.2	9.3	Meas.

Table 1.4 Comparisons of the Class F PA's with the previously reported PA's

Ref.	Process (μm)	Frequency (MHz)	Pout (dBm)	PAE (%)	Class	Condition
[18] 1999	0.35 CMOS	1980	30	41	E	Meas.
[19] 2000	0.24 CMOS	2400	23	39	B	Meas.
[20] 2001	0.6 CMOS	1900	22.8	42	F	Meas.
[21] 2001	0.25 CMOS	900	31.8	43	F	Meas.
[22] 2001	0.25 CMOS	900	29.5	41	E	Meas.
[13] 2003	0.25 CMOS	2450	20	28	AB	Meas.
[23] 2003	0.18 SiGe	2200	<10	25	F	Meas.
[24] 2003	0.35 CMOS	2400	20	59	E	Sim.
[25] 2003	0.35 CMOS	2400	18	33	E	Meas.
[26] 2003	0.35 CMOS	2650	25.2	38	E	Meas.
[27] 2004	0.18 CMOS	8000	20	38	F	Meas.
[28] 2004	GaAs pHEMT	900	22	71.4	F	Meas.
[29] 2005	GaAs pHEMT	2000	19.9	70.5	F	Meas.
1st design of this work	0.35 SiGe	2400	22.5	53.5	F	Sim.
			10	40.7	F	Meas.
2nd design of this work	0.35 SiGe	2400	21.8	40.6	F	Sim
			20.0	34.2	F	Meas.

1.3 Thesis Organization

This thesis is divided into four chapters. Chapter 1 contains the background, motivation, and simple introductions of this research. Two major topics, “A CMOS 2.45 & 5.25 GHz Self-Biased Dual-Band Driver Amplifier for WLAN Applications” and “A 2.4GHz Si/SiGe BiCMOS Class F Power Amplifier for Bluetooth Application,” are described in Chapter 2 and Chapter 3, respectively.

In Chapter 2, a CMOS self-biased dual-band driver amplifier for 802.11a/b/g applications will be introduced. The specifications of WLAN, design methodology, and general considerations are discussed in detail in this chapter. Simulation and measurement results are also compared in the last section.

Chapter 3 presents the design of SiGe Class F power amplifiers for Bluetooth application. Similarly, this chapter consists of the Bluetooth specification, design concepts and experimental results.

Finally, the conclusions and future works will be presented in Chapter 4.

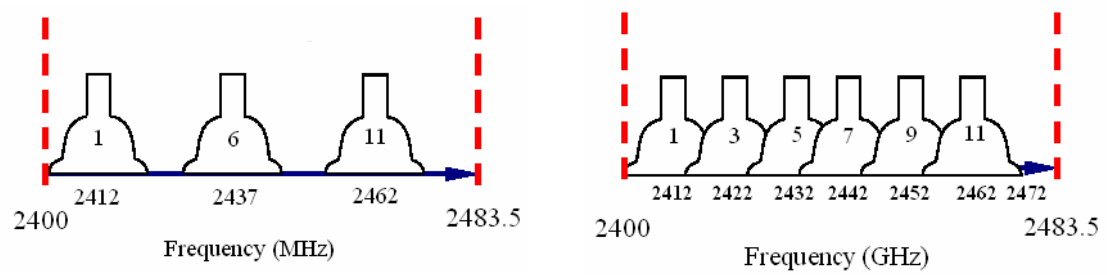
Chapter 2
A CMOS 2.45 & 5.25 GHz Self-Biased Dual-Band Driver Amplifier for WLAN Applications

2.1 Specification Introduction — Wireless LAN System

In November 1990, Institute of Electrical and Electronic Engineers (IEEE) convened the IEEE 802.11 committee to draw up the wireless local network standard. The committee proposed to make the first draft in 1990. Until 1995, they have laid down the first draft. As with other standards in the 802 family, IEEE 802.11 describes a media access control (MAC) sub-layer and multiple physical (PHY) layers.

- 802.11b

802.11b uses the 2.4-GHz ISM band (2.412 ~ 2.462-GHz for U.S., Canada, ETSI and 2.412 ~ 2.484-GHz for Japan) which is an unlicensed band. The 802.11 Specification uses spread spectrum technologies, one is Direct Sequence Spread Spectrum (DSSS) and the other is Frequency Hopping Spread Spectrum (FHSS). DSSS takes the normal narrow-band transmission and spreads it over a larger range, thus preventing interference from blocking out the entire signal, 802.11 defines 11 separate channels (Figure 2.1). DSSS can support data rates of 1, 2, 5.5, and 11 Mbps (All 11 Mbps 802.11 devices are DSSS). Most products will automatically transmit at the highest possible data rate based on the node current signal-to-noise ratio (SNR).



(a) (b)

Figure 2.1 IEEE 802.11b/g operating channels (North American channel selection) (a)Non-overlapping (b)Overlapping

- 802.11a

IEEE 802.11a provides a total bandwidth of 300MHz which is nearly four times as wide as that of the IEEE 802.11b. It operates in the 5-GHz UNII band which is not as crowded as the 2.4-GHz band. The band allocation is illustrated in Figure 2.2. A continuous 200-MHz part from 5.15- to 5.35-GHz covers lower band and middle band, and a separated 100-MHz portion from 5.725- to 5.825-GHz is the upper band. As shown in Figure 2.2, IEEE 802.11a provides a channel bandwidth of 20-MHz with each channel consisting of 52 modulated sub-carriers.

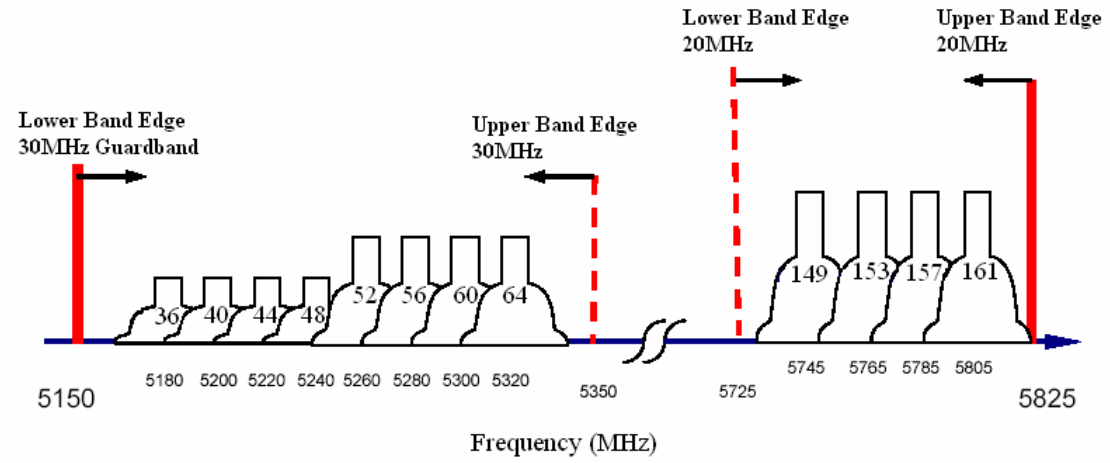


Figure 2.2 IEEE 802.11a operating channels

The IEEE 802.11a employs orthogonal frequency division multiplexing (OFDM) modulation, with each channel containing 52 sub-carriers. Each sub-carrier can be modulated as BPSK, QPSK, 16-QAM or 64-QAM while being transmitted in parallel.

This subdivision provides a means to different data rates. The selection of modulation and data rate depends on the propagation conditions, that is, if the receiving SNR is higher, the high data rate modulation is chosen. The highest data rate provided by 64-QAM is 54 Mbps, which is almost 5 times faster than 11 Mbps in the 802.11b.

Peak-to-average power ratio (PAPR) is the problem that is introduced with OFDM modulation. Assume each of the 52 sub-carriers carries a sinusoid, in the worst case, with 52 peaks of the sine waves adding together, the resulting PAPR will be $10\log(52) \approx 17\text{dB}$ [30]. It influences the RF transmitter design significantly since the high PAPR translates directly into the power back-off in a transmitter and the extension of dynamic range. The receiver must be able to process the signal which is much larger than the average value, and the transmitter must be able to deliver higher output power level. If transceiver cannot handle such a large signal, the waveform will be clipped or distorted. In practice, a finite peak clipping can be tolerated without heavily degrading the system performance.

- 802.11g

IEEE has approved the draft of a new wireless LAN standard, 802.11g, which will provide raw data speed of 54Mbit/sec. in the same 2.4-GHz frequency band now used by the older and widely used 802.11b standard. The 802.11g standard has all the speed 802.11a equipped, but can also work with existing 802.11b networks. However, there are only three channels for 802.11g system compared to thirteen channels for 802.11a system. Table 2.1 shows the detail description about the IEEE wireless family.

Table 2.1 Comparison of IEEE wireless standard

	802.11b	802.11a / 802.11a turbo mode	802.11g
Power Levels	1000mW(USA) 100mW(Europe) 10mW/MHz(Japan)	40mW(5.15-5.25GHz) 200mW(5.25-5.35GHz) 800mW(5.725-5.825GHz)	Same as IEEE 802.11b
Data Rates	11Mbps	54Mbps / 72Mbps	54Mbps
Frequency	2.4GHz	5GHz	2.4GHz
Available Spectrum	83.5MHz	300MHz	83.5MHz
Modulation Encoding	DSSS / CCK	OFDM	DSSS / PBCC
Channels / non-overlapping	11 / 3	12 / 8	11 / 3

2.2 General Consideration

2.2.1 Process Choice

Comparing with other technologies, such as SiGe or GaAs, CMOS technology is less suited for designing RF power amplifier. There are several problems inherent in CMOS process, including oxide breakdown, poor transconductance, large device sizes, and hot carrier effect.

The crucial drawback in PA designs is its lower breakdown voltage since PA demands high output power. Oxide breakdown problem limits the maximum signal swing of the drain of the MOS. The output voltage swing is determined by the breakdown voltage and the knee voltage as shown in the equation:

$$P_{\mathrm{RF}} = \frac{1}{2} I_{\mathrm{pk}} V_{\mathrm{pk}} = \frac{1}{2} \left(\frac{V_{\mathrm{breakdown}} - V_{\mathrm{knee}}}{2} \right) \left(\frac{I_{\max} - I_{\min}}{2} \right)$$

And it has no question that CMOS devices have poor transconductance comparing to BJT. GaAs has a significantly higher mobility than silicon, so the amount of current generated for a given input overdrive is also large. The issue of

poor transconductance leads to two potential solutions, both of which have their pitfalls: first, increasing the drive signal amplitude, or, second, increasing the device size. Unfortunately, these two methods will reduce the efficiency of the CMOS PA implementation.

Another drawback is its higher knee voltage. It can also be shown in the equation above that for larger output power, lower knee voltage is required. Not only does high knee voltage reduce the output power capability, but it degrades the efficiency seriously. For PA's in portable device application, efficiency is a prime issue since in portable device application the battery demands persistence. Efficiency also has a great connection to the heat issue which should be paid great attention to in PA design.

Finally, hot carrier effect, a problem of reliability, will degrade the performance because of the increase of the device threshold voltage. When a CMOS PA continuously operates 70 ~ 80 hours, the output power will decrease in the order 1-dB due to the hot carrier effect [31].

However, recently it is a trend to integrate the whole RF transceiver onto a single chip. The low cost, high performance and high integration technology are needed for system-on-a-chip (SoC) designs. Though with so many disadvantages, CMOS, seems a good candidate for SoC implementation due to the already mature CMOS digital / analog circuit designs. And the fast development of CMOS transistors makes designing the RF front-end circuits, such as low noise amplifiers (LNAs), Phase-Locked-Loops (PLLs) and mixers for operating frequency toward 5-GHz be possible. This chapter contains some circuit schemes to mitigate the drawbacks of the PA design fabricated using TSMC 0.18 μm 1P6M CMOS process.

2.2.2 Dual-Band PA Design

Comparing with narrow band power amplifier, dual-band power amplifier design

is no doubt even more difficult. Figure 2.3 contains the configurations of conventional dual-band PA designs.

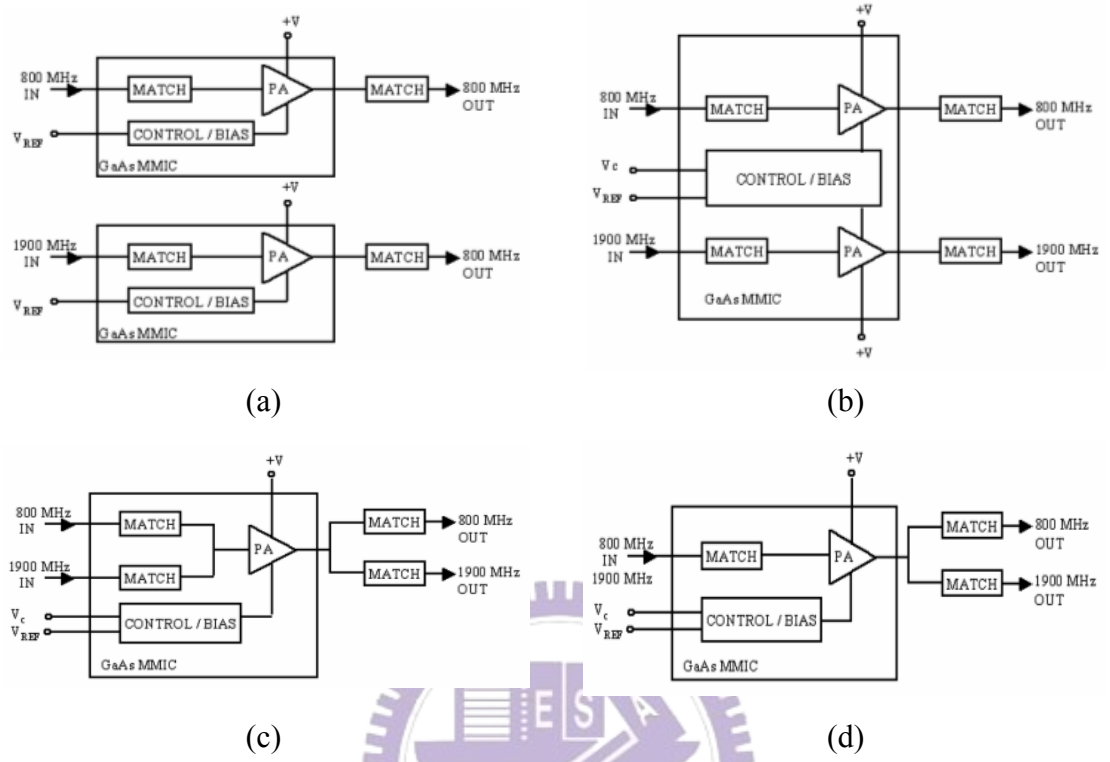


Figure 2.3 (a)Two independent amplifier solution (b)Two amplifiers share the same control/bias circuit (c)One amplifier solution with two input, single output (d)One amplifier solution with single input and single output

The first two configurations allow two amplifiers to be optimized individually for their own operating band. The third and the fourth configurations apply switched matching elements to provide single chain power amplifier solutions with good performance. The best solution does not actually exist, the last two configurations offer manufacturers a significant reduction in component count, board space and cost at the expense of small sacrifice of the performance. On the other hand, the first two provide better performance with a significant penalty in board space, component count and cost [32].

Besides the topologies above, this design applies a single-input/single-output dual-band topology shown in Figure 2.4. The purposed dual-band amplifier utilizes

dual-band matching networks in the input and output ends.

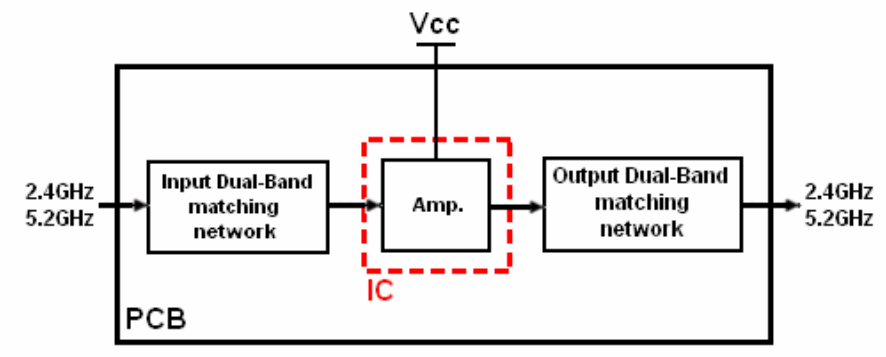


Figure 2.4 Purposed Amplifier in single-input/single-output configuration

2.2.3 Linear Amplifier

RF Power Amplifiers usually can be divided into two categories: one is called "linear" (or amplification mode) amplifier; another is called "nonlinear" (or switch mode) amplifier. A linear amplifier has a linear relationship between the input and output, and the transistors nominally act as current sources. Class A, AB, B, and C belong to this type. The transistor of nonlinear or switch mode power amplifier acts as a switch. This category has Class D, E, and F.

In Class A operation, the transistor operates in the active region at all times thus that it is always conducting current. As a result, the advantage of Class A amplifier is better linearity because its output is the amplification of input. But its efficiency is very poor (less than 50%) since the transistor is always on. In the Class B amplifier, the gate bias is set at the threshold of conduction to shut-off the output device half of every cycle. Therefore, the efficiency of Class B is higher than that of Class A (the theoretical peak efficiency is 78.5%) at the cost of poor linearity. The transistor of a Class C amplifier, as you can image, is on for less than half cycle so as to improve the efficiency. When conduction angle decreases toward zero, the efficiency can be increased toward 100%. Since this causes the output power to decrease toward zero, the drive signal power must be sufficiently large. For this reason, Class C is not suited

to portable applications.

Class AB amplifier, to be worthy of the name, conducts between 50% and 100% cycle, which depends on the bias level it choose (Figure 2.5). The device is biased to a quiescent point which is somewhere in the region between the cutoff point and the Class A bias point. As so, the output signal of this type is zero for part, but less than half of the input sinusoidal signal. Consequently, Class AB amplifier is chosen in this dual-band amplifier design since it's a compromise between efficiency and linearity.

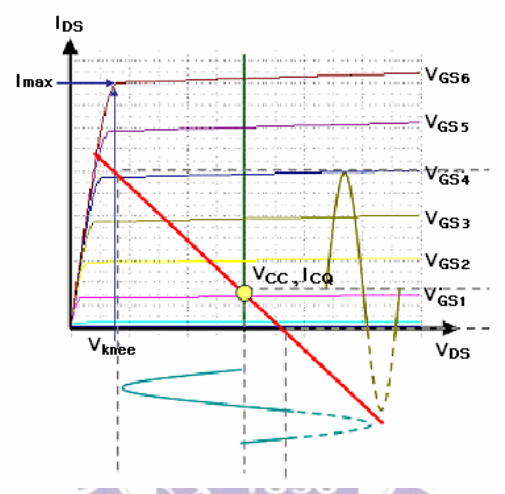


Figure 2.5 Class AB operation point

2.3 Circuit Design

In this work, a TSMC 0.18 μm CMOS 2.4 / 5.2-GHz dual-band self-biased Class AB driver amplifier for 802.11a/b/g application is designed, and the schematic is shown in Figure 2.6. The design concepts will be illustrated as follows.

2.3.1 Device Size and Bias Point

The desired output power at 1-dB compression point is 10dBm, and the power efficiency is about 25%. Because different size and bias condition will lead to different output power and efficiency, repeat tests should be needed to determine the quiescent point. The total gate width of M1 in Figure 2.6 is 80 μm, with single gate width 2.5 μm.

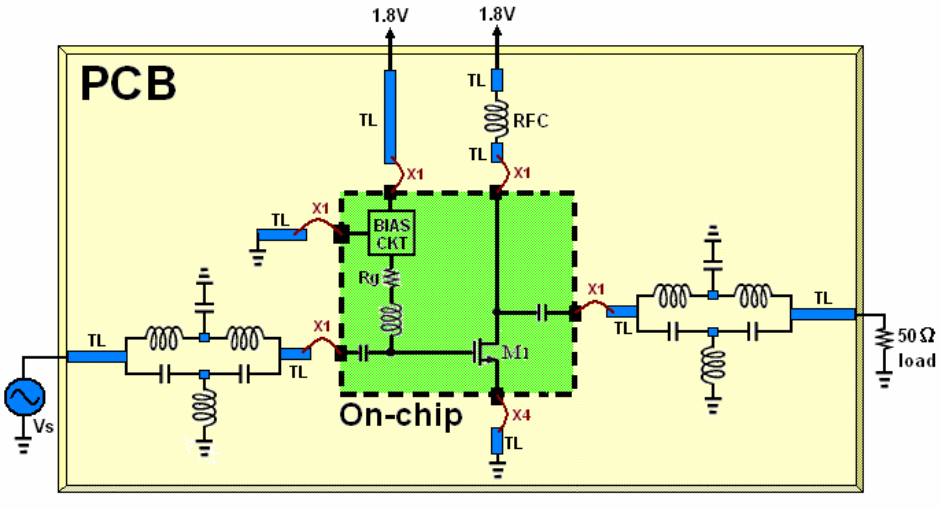


Figure 2.6 Schematic of the dual-band CMOS amplifier

The I-V curve of the driver amplifier is shown in Figure 2.7, since Class AB biasing is chosen, a bias voltage of 1.0V and bias current of 15.67mA are derived.

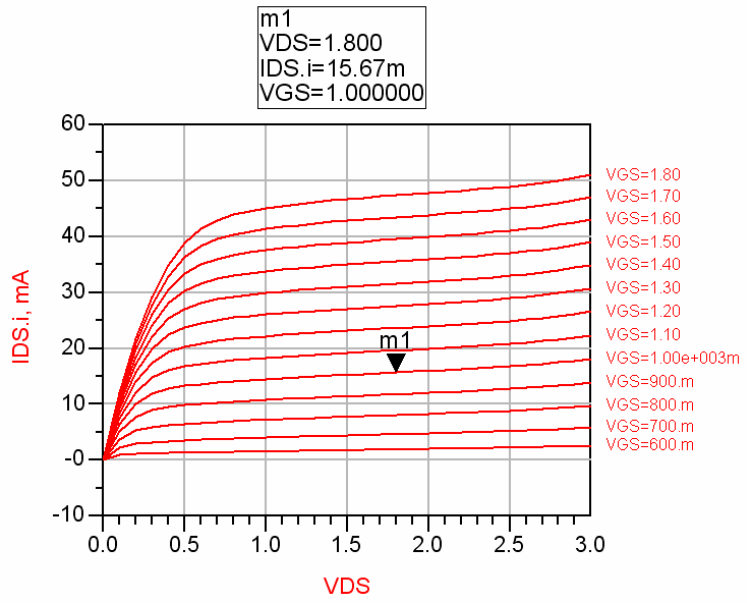


Figure 2.7 I-V curve of NMOS with gate length = 0.18 μm, gate width = 80 μm

2.3.2 Stability (K factor and $|\Delta|$)

As designing a power amplifier, stability is the most important issue. Because the gain of the power amplifier is large in the wide range from dc to millimeterwave frequency, the circuits are very easy to satisfy the condition of oscillation in some frequencies and lead circuits to be broken. An effective solution of the oscillation

problem is to add a small resistor Rg to the gate bias (as shown in Figure 2.6). Figure 2.8 indicates that the measured K > 1and $|\Delta| < 1$ in the interested frequency band, a sufficient condition for unconditional stability of this design.

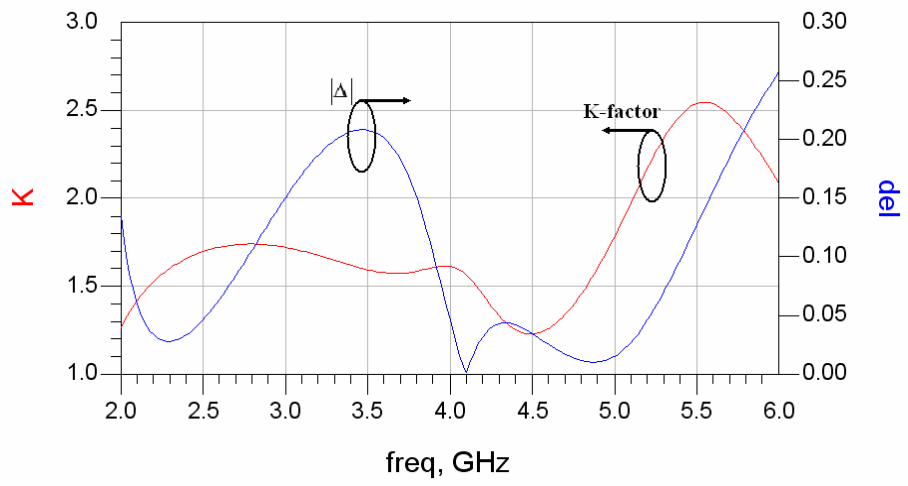


Figure 2.8 Stable factors

2.3.3 Biasing Circuit

Power-supply sensitivity can be greatly reduced by the use of the so-called bootstrap bias technique, also referred to as self-biasing. The threshold-referenced (V**t**) current source with a typical start-up circuit used in MOS technologies is illustrated in Figure 2.9(a) [33]. The current mirror composed of matched transistors T1 and T2 dictates that I_{IN} is equal to I_{OUT}. The zero-current state can be avoided by using the start-up circuit (T5–T7) to ensure that some current always flows in the transistors in the reference. The biasing circuit is designed to provide 1V for the gate voltage. An additional requirement is that the start-up circuit must not interfere with the normal operation of the reference. As a result, a large resistor R**1** (about 10kΩ) and PMOS bypass capacitor C**b** of about 20pF (Figure 2.9(b)) are used to function as a shielding to prevent biasing circuit from interfering with the operation of the driver amplifier.

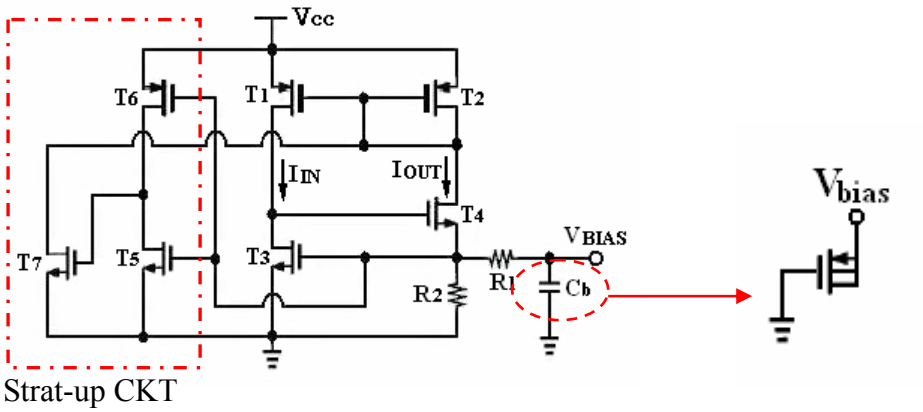


Figure 2.9 (a)Self-biasing Vt reference with start-up circuit (b)Schematic of PMOS capacitor

Figure 2.10 shows the simulated transient plot of the biasing circuit to simulate the turn-on situation of the real supply voltage. It indicates that the bias circuit can respond immediately even when Vcc turns on in just 10 μs .

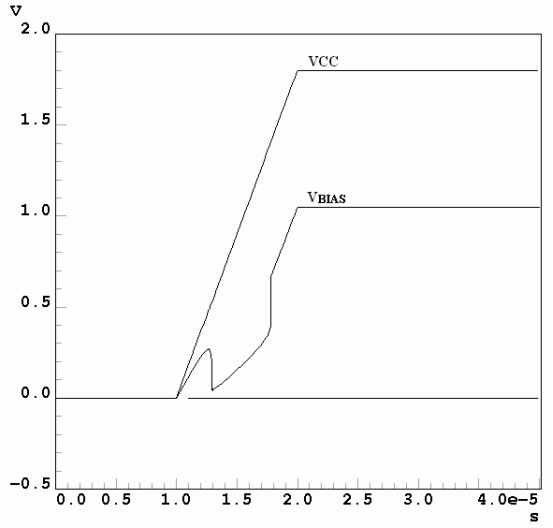


Figure 2.10 Transient plot of biasing circuit

2.3.4 Matching Networks

Instead of using the maximum power transfer theorem (gain match condition), it usually adopts power match condition for RF power amplifiers since the power transistors have larger device peripheral compared with those used in different functions [34]. It's not entirely clear how to define impedances in a large-signal,

nonlinear system. A more important reason is that even if we can solve the problem and subsequently arrange for a complex conjugate match, the current swing of the PA's would be limited by the device I-V curve, resulting in 1-3dB lower output power compared with power matched PA's, and the efficiency would be only 50% because equal amounts of power are then dissipated in the source and load. Consequently, PA's usually have small optimum load resistance to achieve as large as output power, PAE, etc..

The so-called load- / source- pull measurements are the most practical and precise way to measure the large signal characteristics. One of the commercial computer controlled load-pull measurement system is shown in Figure 2.11. The purpose to measure the output is to derive the maximum output power, and that to measure the input is to derive the minimum reflected power.

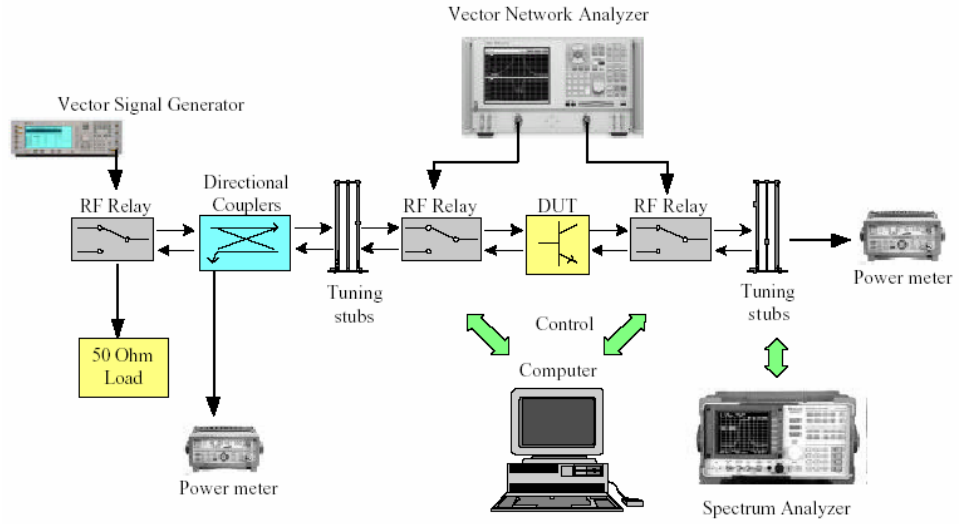
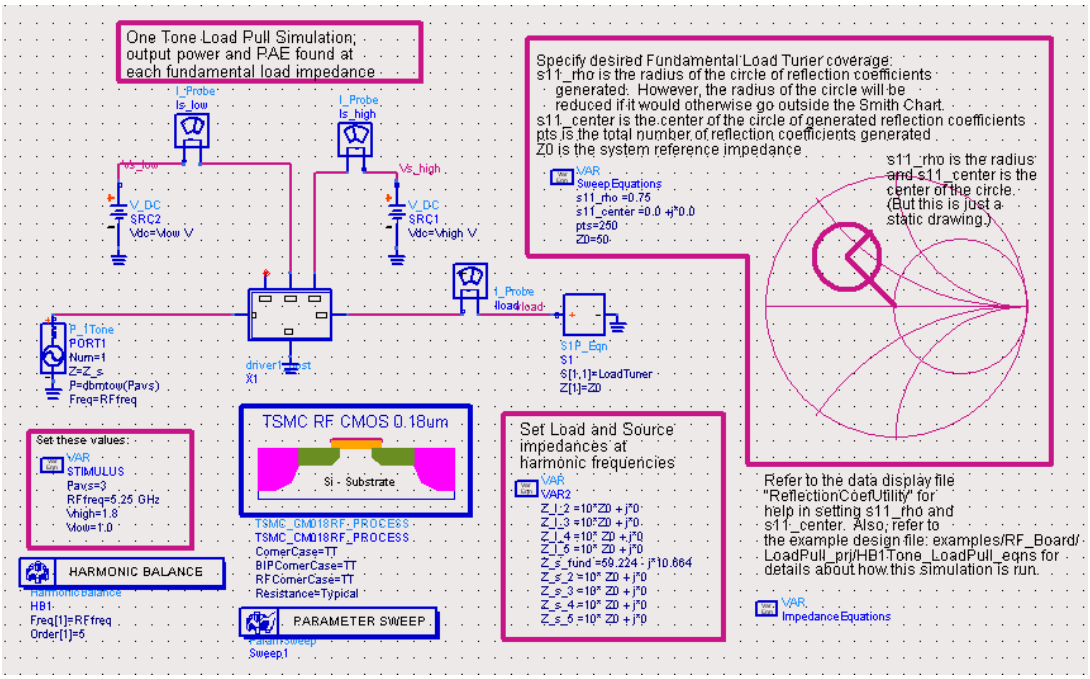
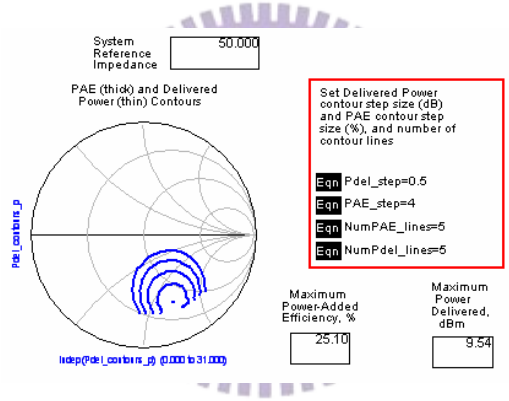


Figure 2.11 Focus computer controlled load / source pull measurement system

Figure 2.12 is the load-pull simulation environment of ADS, it helps to predict the output power of each load impedance on Smith chart. And from the load- / source-pull measurement results, designers can clearly know how to match the transistor by those constant power contours.



(a)



(b)

Figure 2.12 (a)ADS load-pull simulation environment (b)Simulation results

A major hindrance for full integration onto a single chip using standard CMOS technologies is that the on-chip passives, such as inductors, capacitors, and filters, require high-Q values, which is also one of the challenges of designing the dual-band matching networks. The conventional matching topologies include low pass-high pass diplexer, switched element filter network, and a combination of both [32]. For the sake of high Q values and verification of the topology, the input / output matching networks presented in this design, as shown in Figure 2.13, is in diplexer form utilizing Murata lumped-elements and microstrip transmission lines. Theoretically,

the 2.4- and 5.2-GHz input signals are fed from the single port through a low-pass filter (LPF) and high-pass filter (HPF), respectively. After the signals are amplified with a common amplifier, they are divided again by an LPF and HPF and delivered to output port. In the diplexer-matching configuration, signal isolation between frequency bands must be maintained.

The off-chip matching networks also have its convenience for some tuning if there is any mismatch between simulation and practical situation. By tuning these elements, the desired impedances of each interested band can be synthesized.

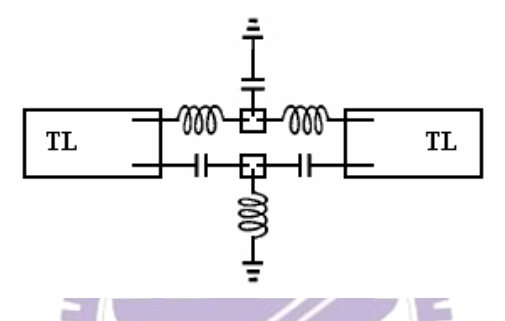
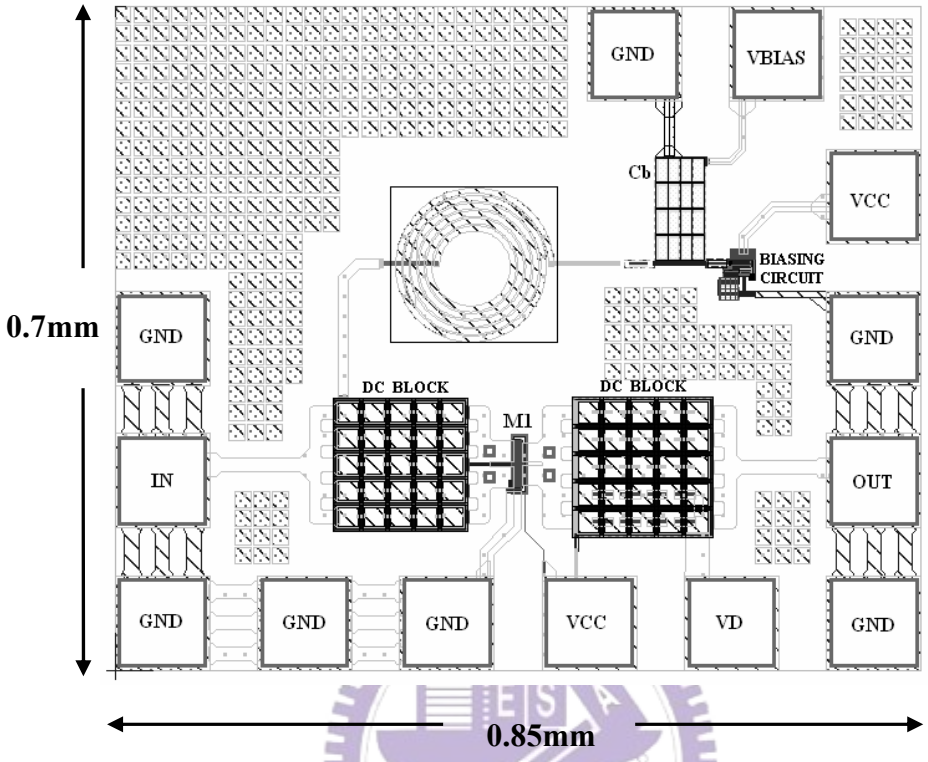


Figure 2.13 Diplexer –liked dual-band matching network

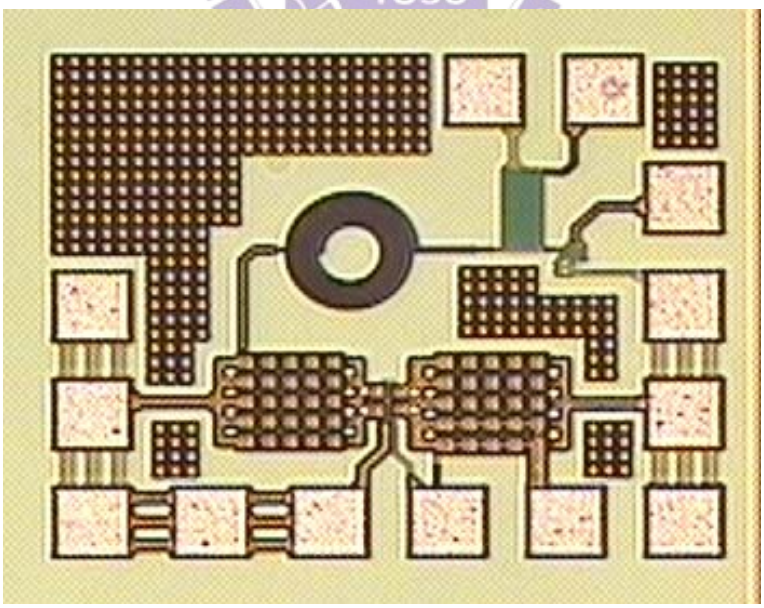
2.4 Layout Considerations

The driver amplifier is laid out using LAKER layout tool. The die, as shown in Figure 2.14, which occupies an area of 0.85 mm by 0.7 mm, was mounted chip-on-board on Rogers RO4003 PCB. Four bond-pads are used to ground the source of the transistor for preventing from source degeneration and unstable condition, which result in an inductance of about 0.75nH. Additional pad is added between biasing circuit and the driver amplifier to measure the bias circuit's output and to supply bias voltage directly if the bias circuit does not operate properly. Furthermore, for metal density and antenna rule concern, diode-liked cells are added to the free space of the die. To cope with the process variation, the resistor R2 of the biasing

circuit in Figure 2.9 is laid out with a width of $5\,\mu m$ (normally $2\,\mu m$), and the dummy resistors are also equipped.



(a)



(b)

Figure 2.14 The (a)layout and (b)die photo of the dual-band pre-amplifier

The input DC-blocking capacitor is implemented with 12.8pF MIM capacitor

formed by 25 MIM capacitors of 515fF for the concern of Q and the output one is also implemented as large as 14.4pF. Each of the elements is surrounded by guard ring fabricated using bottom Metal connected to Si-substrate and can also be bonded-wire to PCB to provide a more clean environment for the integration with other front-end circuits, such as, LNA, Mixer, VCO.

2.5 Simulation and Measurement Results

The circuit is simulated using both Agilent ADS and Mentor Eldo-RF. The bond-wire effect, off-chip matching networks, biasing circuit, and the variation of process, temperature, and supply voltage are considered in the simulations.

- Measurement Considerations

Figure 2.15 shows the board level photo of the CMOS driver amplifier. In the beginning, though the foundry of the monolithic elements provides model files (*.s2p) of their products, it's found that some of the elements do not perform quite well at high frequency (above 5-GHz), especially for larger capacitance and inductance. This leads to serious mismatches between simulation and measurement, and becomes the main challenge to design the matching circuits at 5.25-GHz.

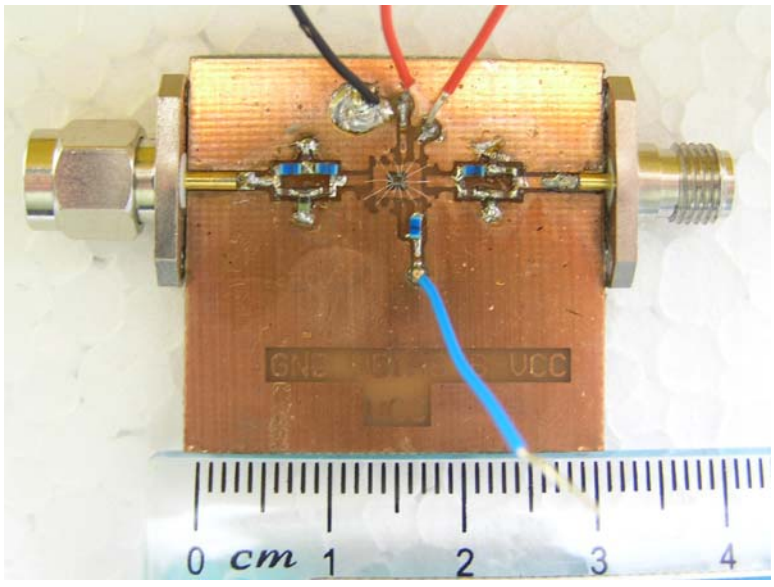


Figure 2.15 Board level photo of the dual-band driver amplifier

To solve the problem, each element is measured to re-build the model files for simulation. Figure 2.16 indicates the ”Through, Reflection, Line (TRL)” calibration way. It’s worthy to note that the frequency of $\frac{\lambda}{4}$ line of “Load” is 4.0-GHz since we wonder the frequency band of 2.0-GHz to 6.0-GHz. It’s an effective solution to re-design the matching network.

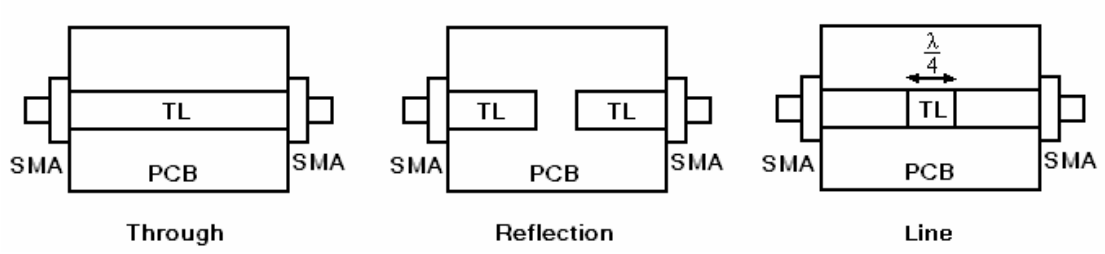


Figure 2.16 TRL calibration

As a matter of course, on PCB measurement is adopted. The measurement can be done by the setups shown in Figure 2.17 to measure such as, S-parameters, P_{1dB}, Gain, PAE, and IP3, etc.. Figure 2.18 shows the practical measurement setups provided by the Chip Implementation Center (CIC), P_{1dB}, Gain, and IP3 can be measured by these instruments. And S-parameters are measured by Agilent 8720ES S-parameter Network Analyzer.

During the measurement, some amplifiers still start to oscillate or be broken even that they are stable and work properly in the initial stage. There are several points for attention: (1)50Ω loads should be connected to the input and output to terminate the reflection when measuring the DC characteristic. This protection is useful to avoid DC oscillation. (2)Ground should be connected first when using the power supply. If the positive electrode is connected first, the supply voltage will not be predictable (even above 20-V), and the circuit will suddenly be broken. (3)Because it needs quite high temperature to weld the SMA connector, the latter should be welded after the former becomes cooling. (4)Be careful when using the buzzer of the multimeter to

check if there is any short-circuit because the meter will provide a DC voltage about 1.2-V, which may cause damage to the amplifier. (5)Another issue of using power supply is that the voltage should be tuned slowly. If the tuned voltage variation is too large, it may become a trigger to lead to circuit oscillation. (6)Static ring is proposed to be put on all the time for preventing from the ESD issue. (7)Decouple capacitors should be placed at both V**bias** and Vcc to eliminate the feedback path.

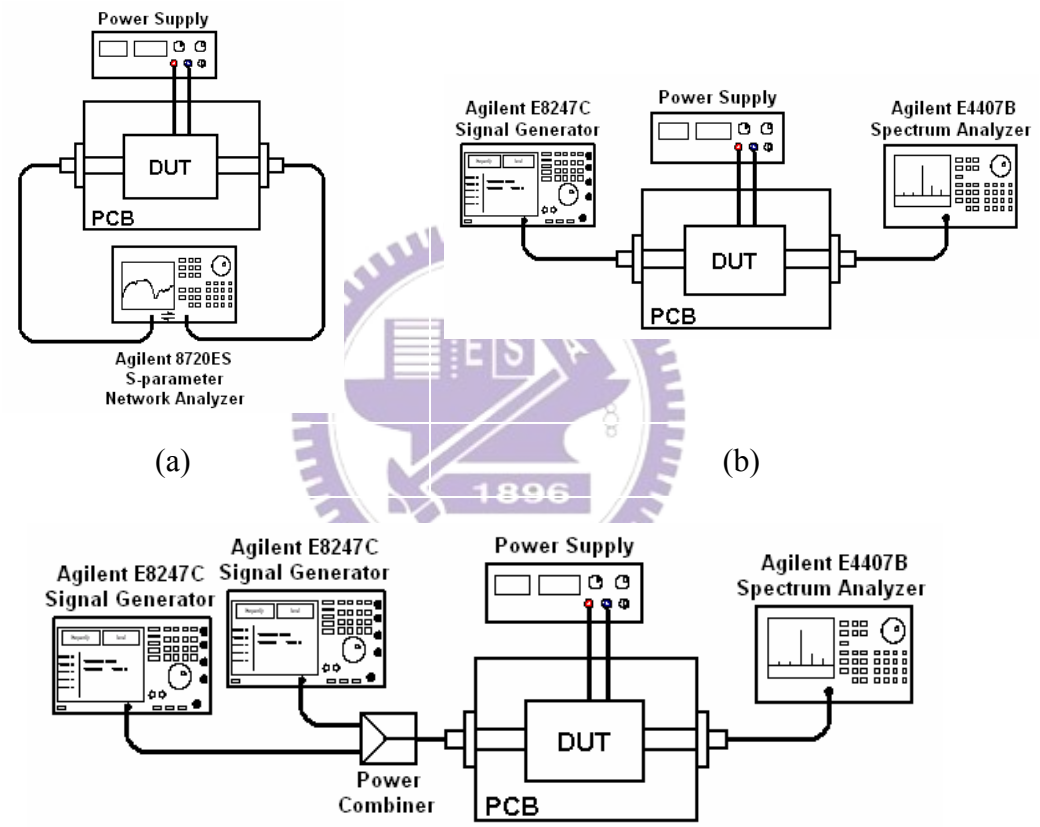


Figure 2.17 Various setups used to measure the performances of the PA: (a)S-parameters (b) P_{1dB}**, Gain, PAE (c)IM3, IP3**

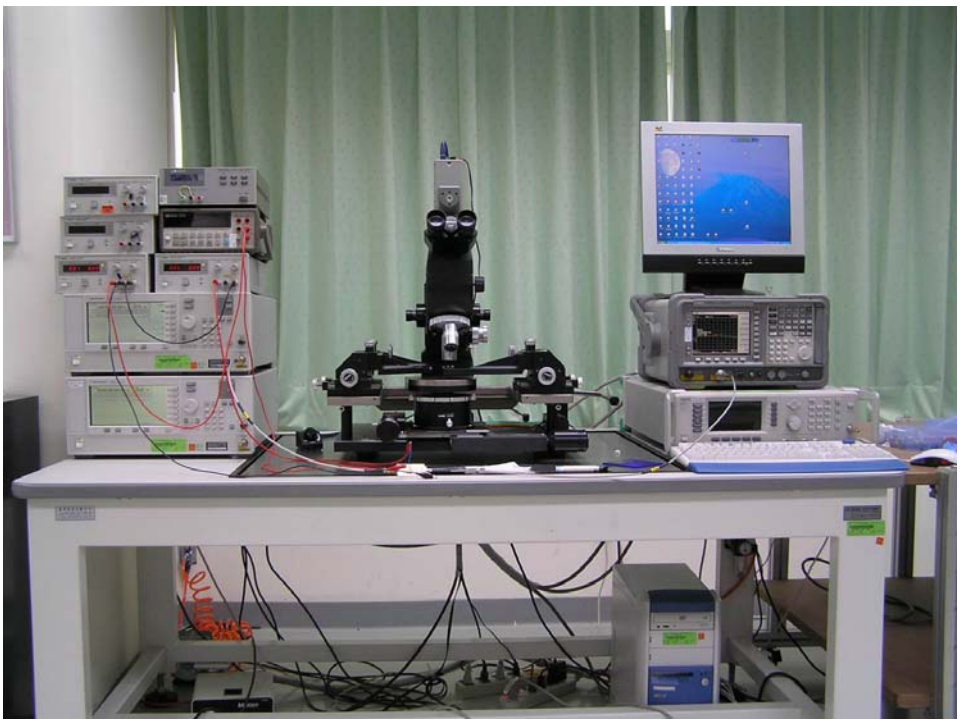


Figure 2.18 Measurement setups

- Performances at 2.45-GHz

Figure 2.19 and Figure 2.20 show the power parameters. The P_{1dB} occurs at Pin = 2.0dBm and the corresponding Pout = 8.3dBm with PAE = 17.1%. Figure 2.21 indicates the two-tone test (with f_1=2450-MHz and f_2=2451-MHz) with IIP3 = 13dBm and OIP3 = 16dBm.

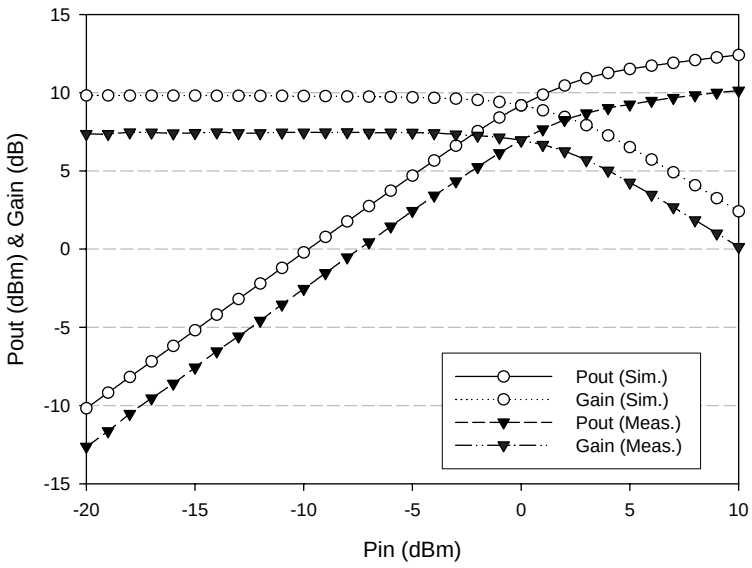


Figure 2.19 Pout & Gain vs. Pin @ 2.45-GHz

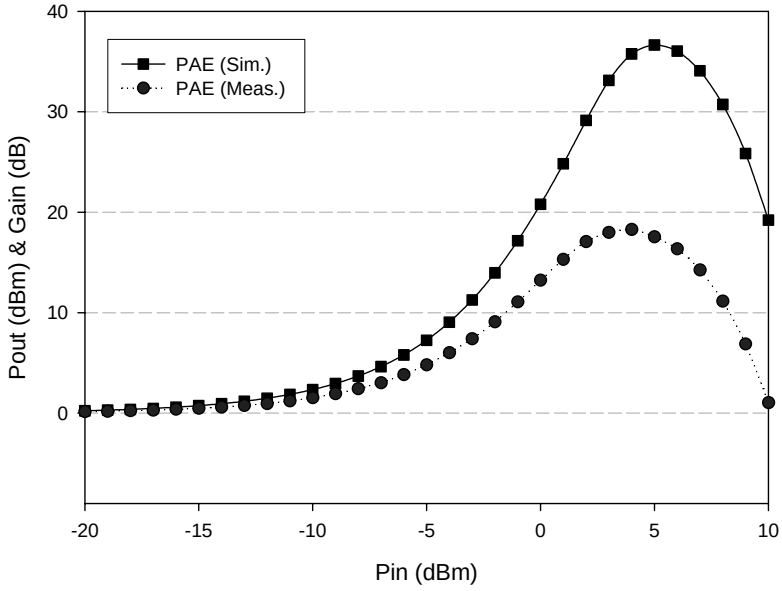


Figure 2.20 PAE vs. Pin @ 2.45-GHz

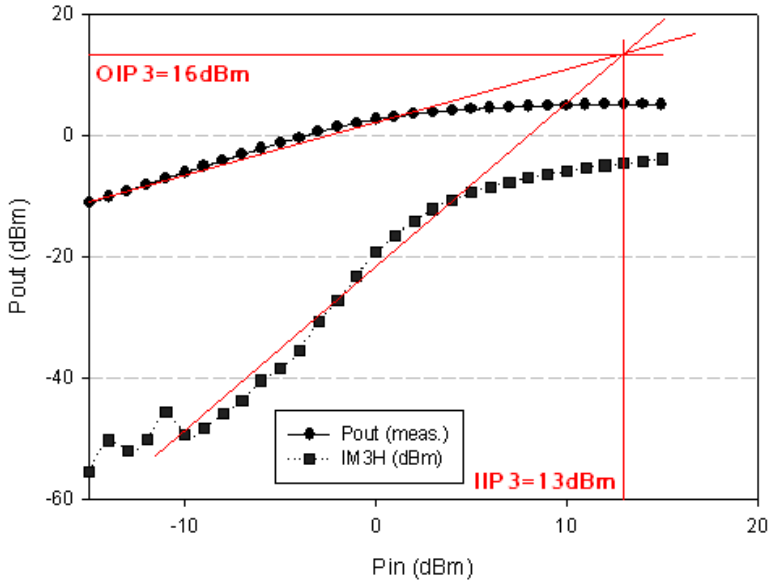


Figure 2.21 Two-tone test IIP3 and OIP3 measurement result @ 2.45-GHz

- Performances at 5.25-GHz

Figure 2.22 and Figure 2.23 show the power parameters. The P_{1dB} occurs at Pin = 4.0dBm and the corresponding Pout = 7.2dBm with PAE = 9.3%. Figure 2.24 indicates the two-tone test (with f_1=5250-MHz and f_2=5251-MHz) with IIP3 = 15dBm and OIP3 = 19dBm.

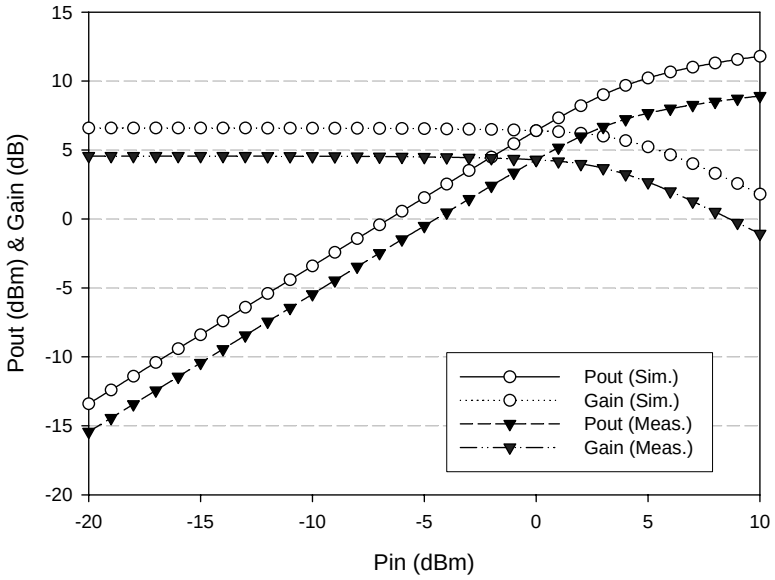


Figure 2.22 Pout & Gain vs. Pin @ 5.25-GHz

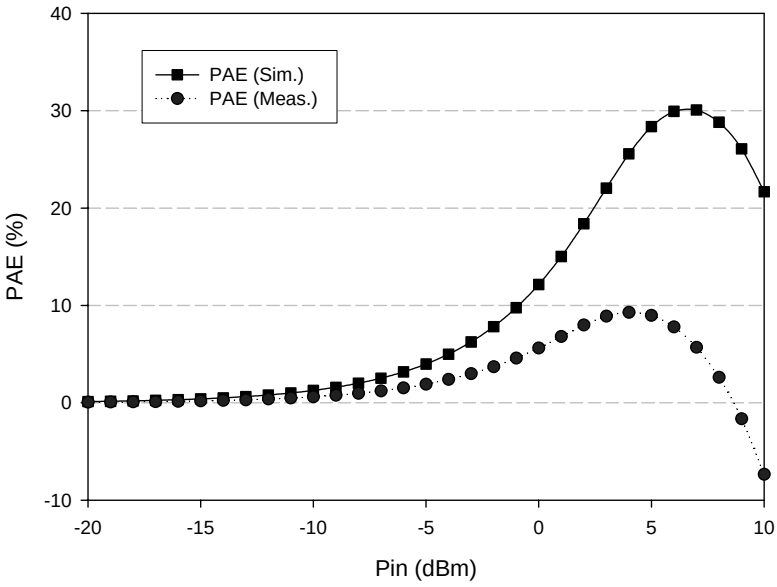


Figure 2.23 PAE vs. Pin @ 5.25-GHz

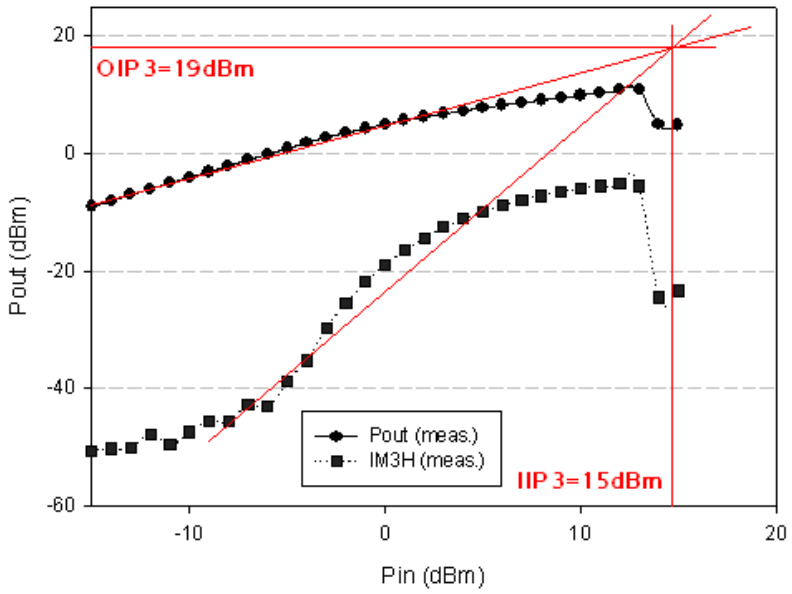


Figure 2.24 Two-tone test IIP3 and OIP3 measurement result @ 5.25-GHz

The S-parameters shown in Figure 2.25 indicate this driver amplifier can work both in 2.4-GHz frequency band and 5.2-GHz frequency band with reasonable performances.

The self-biased dual-band CMOS driver amplifier is fabricated by TSMC 1P6M 0.18 μm process. Matching networks are needed to be fabricated on PCB. Table 2.2 is the performance summaries and comparisons of the CMOS driver amplifier. From Table 2.2 we can observe that the gain performances are poor than the simulation results and cause the PAE decreasing with that, especially for 5.2-GHz band. Since the P_{1dB} and gain of PA are sensitive to the input and output matching networks, it's reasonable to suspect that the amplifier is not really matched well.

The S-parameters in Figure 2.25 indicate that the matching condition is not as bad as imagine, however, the S-parameters are derived with an input power of -25dBm. In other words, there may be something wrong with the matching condition if input power becomes larger.

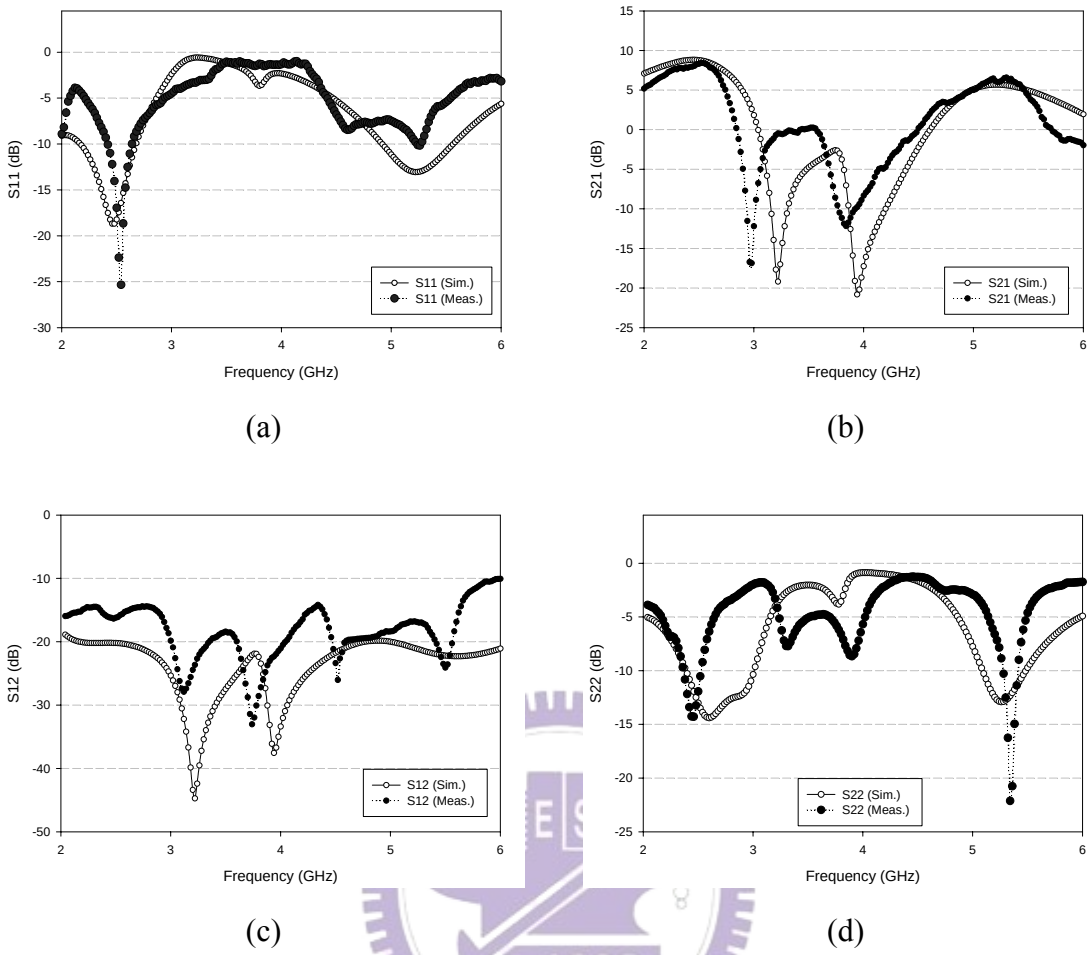


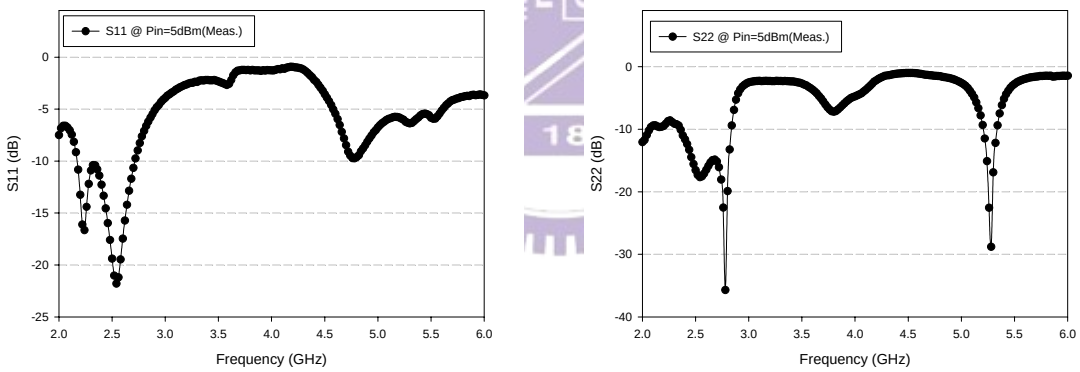
Figure 2.25 S-parameters (a)S11 (b)S21 (c)S12 (d)S22

Table 2.26 and Table 2.3 show the S-parameters with an input power of 5dBm, it can be observed that the 2.4-GHz band still has good matching networks, but the input return loss (S11) of 5.2-GHz is only about -6dB, which is the reason for poor performances of 5.2-GHz band.

In conclusion, we must consider the large input power operation of PA when designed, especially for high frequency. It is essentially not clear how to define the large signal model and impedance, which is the minor reason makes the PA design difficult. Table 2.4 is the comparisons between this works and recently papers.

Table 2.2 Performance summaries

Dual-band Driver-amplifier (TSMC 0.18 μm CMOS)				
Supply Voltage (V)	**1.8**			
Frequency (GHz)	**2.45**		**5.25**	
Spec.	**Sim.**	**Meas.**	**Sim.**	**Meas.**
Bias CKT o/p (V)	**1.05**	**1.05**	**1.05**	**1.05**
DC Current (mA)	**16.0**	**16.62**	**16.0**	**16.62**
IP1dB (dBm)	**1.0**	**2.0**	**4.0**	**4.0**
OP1dB (dBm)	**10.0**	**8.3**	**9.7**	**7.2**
Gain@1dB (dB)	**9.0**	**6.3**	**5.7**	**3.2**
PAE@1dB (%)	**24.8**	**17.1**	**25.6**	**9.3**
IIP3 (dBm)	**11.2**	**13.0**	**13.6**	**15.0**
OIP3 (dBm)	**21.0**	**16.0**	**20.0**	**19.0**
S11 (dB)	**-18.7**	**-12.2**	**-13.0**	**-10.2**
S22 (dB)	**-11.9**	**-14.3**	**-12.9**	**-8.8**



(a) (b)

Figure 2.26 Return loss @ Pin = 5dBm (a)input return loss (b)output return loss

Table 2.3 Return loss @ Pin = 5dBm

	2.45 GHz	**5.25GHz**
Input return loss (dB)	-12.3	-5.8
Output return loss (dB)	-11.6	-9.3

Table 2.4 Comparisons of the dual-band driver amplifier with the previously reported PA's

Ref.	Process (μm)	Frequency (MHz)	Pout (dBm)	Gain (dB)	PAE (%)	Condition
[9] 2001	0.35 CMOS	2400	<17.5	<13.9	<16	Meas.
[10] 2002	0.18 CMOS	5200	15.4	14.1	27.1	Meas.
[11] 2003	0.25 CMOS	5250	11.8	5.3	8.0	Meas.
[12] 2003	0.25 CMOS	2450	21	19	26	Sim.
		5250	21	6.0	18	
[13] 2003	0.25 CMOS	2450	20	11.2	28	Meas.
[14] 2004	0.18 CMOS	2450	9.7	N/A	N/A	Meas.
		5250	19.5	>17.1	15.3	
[15] 2004	0.18 CMOS	5500	2.0	5.3	9.3	Meas.
[16] 2004	GaAs HBT	2450	27	25	42	Meas.
		5250	27.2	15	31.2	
[17] 2004	GaAs HBT	2450	27	<34	<40	Meas.
		5250	24	<25	<22	
This Work	0.18 CMOS	2450	8.3	6.3	17.1	Meas.
		5250	7.2	3.2	9.3	

Chapter 3

A 2.4GHz Si/SiGe BiCMOS Class F Power Amplifier for Bluetooth Application

3.1 Specification Introduction — Bluetooth

The Bluetooth standard defines short-range wireless connection between mobile phones, mobile PCs and other portable devices. It specifies a 2.4-GHz frequency-hopped spread-spectrum (FHSS) system that enables the users to easily connect to a range (10m-100m) of computing and telecommunication devices without the need for wires or cabling of any kind. Space and cost considerations are among the primary motivators for the drive toward a single-chip radio solution.

Bluetooth communication occurs in the unlicensed Industrial Scientific Medicine (ISM) band from 2400 to 2483.5 MHz. The transceiver utilizes frequency hopping to reduce interference and fading. This means that every 625 μ sec. the channel will hop to another frequency. The communication channel can support both data (asynchronous) and voice (synchronous) communications with a total bandwidth of 1 Mb/sec.. The supported channel configurations are shown in Table 3.1.

Table 3.1 Supported channel configuration in Bluetooth system

Configuration	Max. Data Rate Upstream	Max. Data Rate Downstream
3 Simultaneous Voice Channels	64 kb/sec. × 3 channels	64 kb/sec. × 3 channels
Symmetric Data	433.9 kb/sec.	433.9 kb/sec.
Asymmetric Data	723.2 kb/sec. or 57.6 kb/sec. (upstream) 57.6 kb/sec. or 723.2 kb/sec. (downstream)	

The modulation scheme is Gaussian Frequency Shift Keying (GFSK), with frequency deviations of 160KHz around the carrier. A binary system is used where a "1" is signified by a positive frequency deviation and a "0" is signified by a negative frequency deviation. Based on signal transmission distance, the required transmitter power levels are classified to Class 1, Class 2, and Class 3, which are shown in Table 3.2. All Bluetooth classes are rated at about 1Mb/sec., with next generation products allowing anywhere from 2 to 12 Mb/sec..

Table 3.2 Three power class of Bluetooth system

Power Class	Maximum Output Power
1	100mW (20dBm)
2	2.5mW (4dBm)
3	1mW (0dBm)

Most portable Bluetooth devices will probably be in Power Class 2 or 3 (with a nominal output power of 4dBm or 0dBm) due to cost and battery life issues. A Power Class 1 device requires the utilization of a power control to limit the transmitted power over 0dBm. While a little more costly and power hungry, this will provide up to 100m of range, which should be sufficient for home networking and other applications that require a greater range.

3.2 General Consideration

3.2.1 Process Choice

Recently, there has been increasing applications of SiGe based BiCMOS to RF analog ICs in the cellular phones and in the wireless local area network systems, commercially. The current RF CMOS circuit and device design technology provides a useful solution for other RF circuits, but on the other hand, CMOS PA is far away

from clear design methodology. SiGe has the advantages of its high frequency characteristics over Si and higher potential of functional integration over GaAs. Moreover, process stability based on large size wafer Si LSI process technologies results in high yield, and offers lower chip costs. SiGe heterojunction bipolar transistors (HBTs) have also attracted much attention for RF power application because of their good microwave power performance, which becomes almost compatible with those of HBTs made of compound materials [35-38]. For the RF power transistors used in the power amplifiers of cellular phones, generally over 1W output power drivability is needed.

- Comparison of the key design parameters of Si-BJTs and SiGe-HBTs

From a designer's point of view, SiGe-HBTs are very similar to Si-BJTs. Basic principles gained in Si-BJT circuits can therefore be applied to SiGe-HBT circuit design in a straightforward manner. There are certainly several advantages of the SiGe technology:

(a) For a given collector current density, SiGe-HBTs require an input voltage V_{BE} that is lower as compared to pure silicon bipolar technology. This holds particularly, when the "true" heterojunction bipolar concept – in comparison with the drift transistor concept favored by other companies – is used: Due to the heterojunction effect, the collector current density is increased exponentially with the difference in bandgap between emitter and base, which is in turn proportional to the germanium (Ge) content in the base. Although part of this gain is sacrificed to a base doping concentration that is 10-20 times higher as compared to Si-BJT technology, to achieve a given collector current density, an input voltage V_{BE} is sufficient that is about 80-mV lower as compared to the Si-BJT. This is especially useful when moving to lower supply voltages, as demanded by all mobile communication systems.

(b) The SiGe heterojunction bipolar concept with inversion of the doping levels in emitter and base used in the process makes use of a lightly doped emitter layer. This reduces base-emitter capacitance C_{BE} drastically and therefore high speed and high gain can be achieved at a lower current density which is profitable to low power design.

(c) The high current gain achievable improves the input resistance and the low noise properties in the input stages of LNAs.

(d) Due to the high base doping concentration, the base width modulation by the base-collector voltage is less pronounced, leading to a higher early voltage as compared to Si-BJTs. This allows for high output resistance of amplifier stages and the realization of very stable current sources.

(e) Because of the high gain at frequencies above 2-GHz, a linearization by feedback is possible, which provides a good inter-modulation behavior in power amplifiers and low noise amplifiers.

The major disadvantage of Silicon bipolar technology for communication systems is the low breakdown voltage, which makes the high power design a demanding task. PA devices must withstand high voltage excursions (quantified by voltage standing wave ratio, VSWR), together with large current densities to survive in the hostile environments expected for consumer articles such as wireless telephones. The low breakdown voltage BV_{CEO} is hereby not a problem specific to SiGe but is a problem of all advanced Silicon bipolar processes, where the transit time is determined not any more by the base width but by the width of the collector layer.

- SiGe BiCMOS for power amplifiers

Power amplifiers are a core component in the high growth wireless communications industry. PA's are rapidly evolving in both architecture and the communication protocols which they must address. Bipolar transistors are the critical

building block of a PA, with silicon, slicon-germanium (SiGe) and Ⅲ/Ⅴ technologies competing as the technology of choice. The constant current gain as a function of temperature together with the high current density and low thermal resistance of the PA SiGe HBT technology makes it possible to make use of smaller output devices thereby minimizing parasitic effects. The low parasitics increase the inherent gain of the devices, which together with an efficient biasing scheme can be utilized for achieving high efficiency.

The technology used in this work is TSMC 0.35 μm 3P3M Si/SiGe BiCMOS process. Based on a volume-process presented in [39], [40], it features a bipolar junction transistor (BJT) with a f_T over 40-GHz and a three layer Al-metalization with a 2.8 μm thick upper layer.

3.2.2 Nonlinear Amplifier

As 2.2.3 introduces, another approach of PA is to use the device as a switch, the reasoning being that a switch ideally dissipates no power, for there is either zero voltage across it or zero current through it. Since the switch's I-V product is therefore always zero, the transistor dissipates no power and the theoretical efficiency must be 100%. The trade-off is poor linearity due to the switching nature. Therefore, switched-mode power amplifiers can only be suitable for the systems with constant envelope modulation scheme.

- Class D PA

The typical circuit of Class D PA is shown in Figure 3.1. Driving signals are applied to the gates in opposite polarities. The FETs are biased at the verge of conduction and the drive causes them to switch on and off alternately.

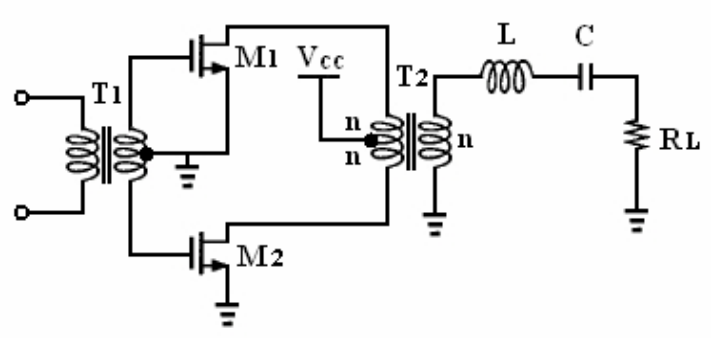


Figure 3.1 Schematic of Class D PA

During the half cycle when M1 is on, $V_{drain1} = 0$, hence a voltage $-V_{CC}$ is coupled to the output-transformer network. During the half cycle when M2 is on, a voltage of $+V_{CC}$ is similarly coupled to the output-transformer network. Since the voltage at the dc feed-point is fixed at Vcc, the drain voltage waveforms are square waves with levels of $2V_{CC}$ and 0.

The fundamental frequency component of the square wave on the output of T2 passes through the output filter to become the output voltage. The sinusoidal current following in the series-tuned output filter requires a corresponding current to flow through one drain or the other. The drain current waveforms are therefore half sinusoids. The current flowing into the dc feed-point of T1 is the sum of i_{D1} and i_{D2}, and is therefore a full wave rectified sinusoid. Ideally, the drain voltage is zero when the drain current is flowing, and the drain current is zero when the drain voltage is not. Consequently, an ideal Class D amplifier is 100% efficient.

One practical problem with this PA is that there is no such thing as a perfect switch. Nonzero saturation voltage guarantees static dissipation in the switches while finite switching speeds imply that the switch I-V product is nonzero during the transitions. Hence, switch-mode PA's function well only at frequencies substantially below f_T. Furthermore a particularly serous reduction in efficiency can result in bipolar implementations if, due to charge storage in saturation, one transistor fails to

turn completely off before the other turns on. Transformer action then attempts to apply the full supply voltage across the device that is not yet off, and the I-V product can be quite large.

- Class E PA

Figure 3.2 shows a conceptual picture of a Class E power amplifier. In operation, the input signal V_{in} toggles the switch (M_1) periodically with approximately 50% duty cycle. When the switch is on, a linearly increasing current is built up through the inductor. At the moment the switch is turned off, this current is steered into the capacitor C_1, causing the voltage across the switch Vs to rise. The tuned network is designed such that in steady state, Vs returns to zero with a zero slope, immediately before the switch is turned on. The fundamental component of Vs then selectively passes through the band-pass filter (C_2 and L_1) to the load, creating a sinusoidal output that is synchronized in phase and frequency with the input. In practical applications, V_{in} may be phase or frequency modulated, in which case the information embedded in the modulation is also passed to the output with a power amplification.

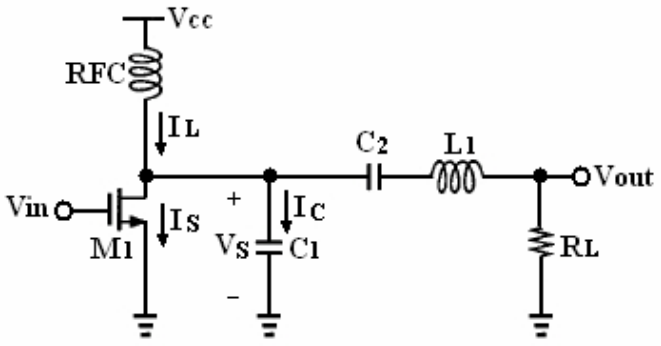


Figure 3.2 Schematic of Class E PA

In practice, the on/off transitions of the transistor will cause the drain voltage and current to be simultaneously non-zero for a short period of time, resulting in additional small power loss. This is aggravated giga-Hertz operation, since the signal

period is reduced, while the transistors' transition times remain unchanged. Thus, a major design aspect of RF Class E PA's is concerned with minimizing this transition loss. Moreover, Class E PA faces a problem of poor power capability (even worse than Class A) [34]. As a result, practical implementations of the Class E amplifier do not exhibit significantly superior efficiency to well-executed designs of other types.

- Class F PA

A Class F power amplifier improves efficiency and output power capability (over that of Class A) by using selected harmonic to shape its drain voltage and current waveforms. The circuit of a genetic Class F PA is shown in Figure 3.3(a). The basic principles of operation are as follows:

(a) Fundamental frequency drain voltage and current are shifted in phase by 180° from each other.

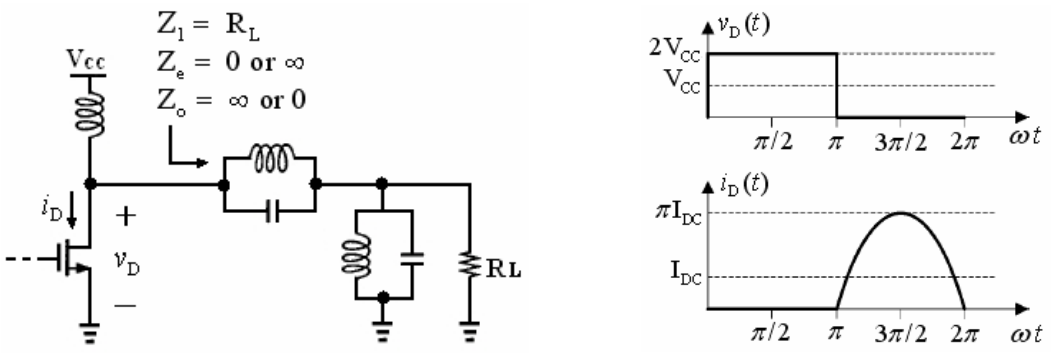
(b) One drain waveform (e.g., voltage) adds odd harmonics to build its shape to a square wave (Figure 3.3(b)).

(c) The other drain waveform (e.g., current) adds even harmonics to build its shape toward a half sine wave (Figure 3.3(b)).

(d) No power is generated at the harmonics because there is either no voltage or no current present at a given harmonic. Harmonic impedances are either zero or infinite.

(e) At microwave frequencies, the number of harmonics is usually relatively small.

(f) The RF power device acts as a saturating current source (e.g., a soft switch). Only when all harmonics are properly terminated can it act as a true switch. Negative voltage and current are not permitted.



(a) (b)

Figure 3.3 Class F PA (a)schematic (b)drain voltage and current waveforms

In Figure 3.3(b), it's noticed that the drain voltage waveform is a square wave while the drain current is a half-rectified sinusoid. From the output waveforms it's also noticed that in the ideal case, there is no overlapping between the drain voltage and current waveform. This suggests that the maximum achievable power efficiency of the PA is 100%, since there is no power loss in the output waveform. To accomplish this behavior, the active device has a bias point at the cutoff region (Class B) for switching operation.

The configuration in Figure 3.4 is also called "flattening", the loading network of which only consists of parallel resonant filters tuned to the fundamental and third harmonic components.

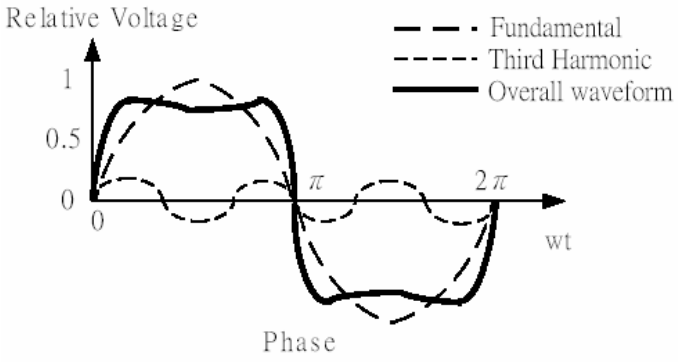


Figure 3.4 Phase vs. relative voltage of an ideal third order network

Note that the voltage of a third order network shown in Figure 3.3(a)

approximates a square wave, which, just like Class D and Class E PA's, causes inevitably power dissipation due to the little overlap between the output voltage and current waveform.

- Comparisons

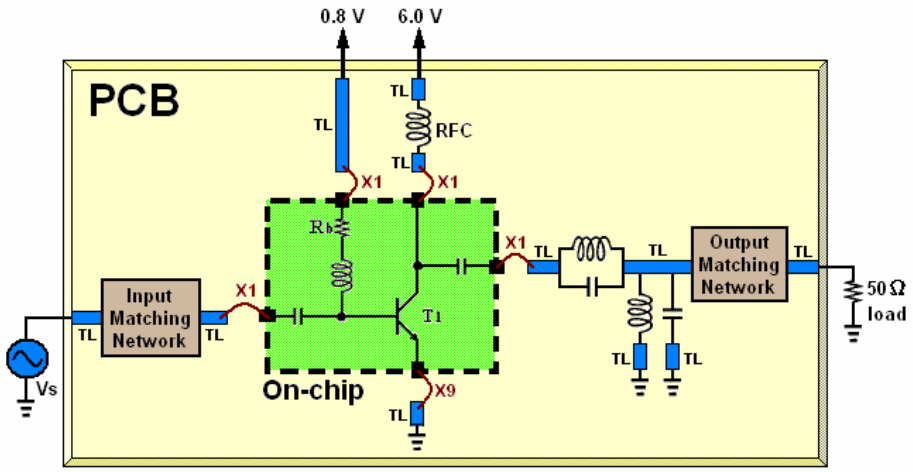
Unfortunately, only two types of amplifier tunings appropriate for high-frequency operation, i.e., Class E and Class F, have been explored. They have found most application as a higher performance alternative to Class D PA's because they may be implemented with a relatively simple circuit.

On the other hand, although Raab has shown that the efficiencies of properly tuned class E and Class F are identical when the efficiency is limited primarily the harmonic content of the waveforms [41], the case wherein the transistor is switching nearly ideally and the efficiency is limited primarily by the device's on-resistance would seem to favor Class F with their reduced peak drain voltages (V_{peak} = 3.6Vcc and 2Vcc for Class E and Class F, respectively). Additionally, the allowable output capacitance in the Class E case is limited. The switch parallel capacitance C_1 (in Figure 3.2), which must be at least as large as the transistor output capacitance, is determined by the output power, DC voltage, and operating frequency. This restriction on the size of the transistor can limit the performance of Class E amplifiers [42]. Class F tunings, however, can, in principle, utilize a transistor with any output capacitance provided that it is properly resonated out at the appropriate frequencies. Although this approach might be used to resonate part of the output capacitance of a Class E tuned transistor at each harmonic, the resulting circuit complexity would be at least that of Class F.

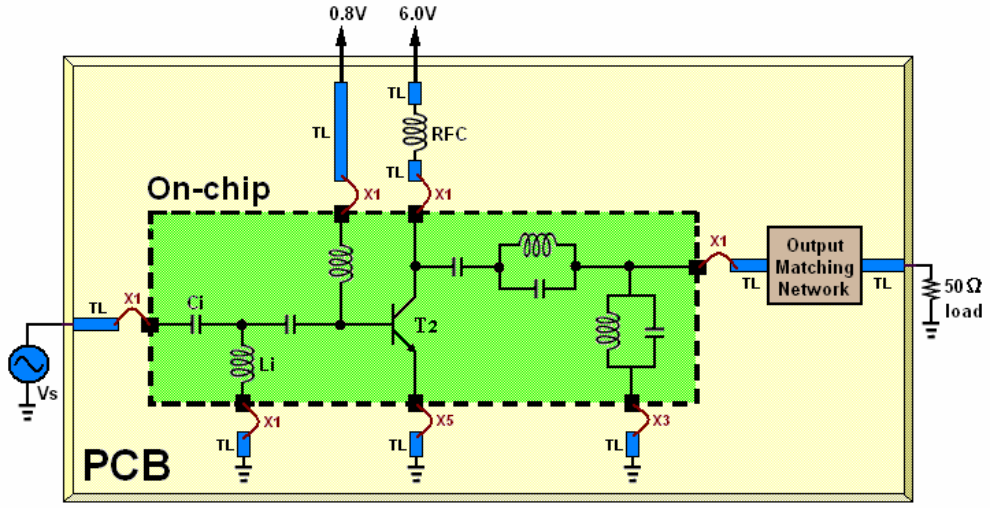
Prior to the availability of switching transistors suitable for Class D and Class E amplifiers, Class F would be our choice for this power amplifier design.

3.3 Circuit Design

In this work, two TSMC 0.35 μm 3P3M Si/SiGe BiCMOS 2.4-GHz Class F power amplifiers for Bluetooth application are designed, and the proposed schematics are shown in Figure 3.5.



(a)



(b)

Figure 3.5 Schematics of (a)the first (b)the second designed Class F power amplifiers

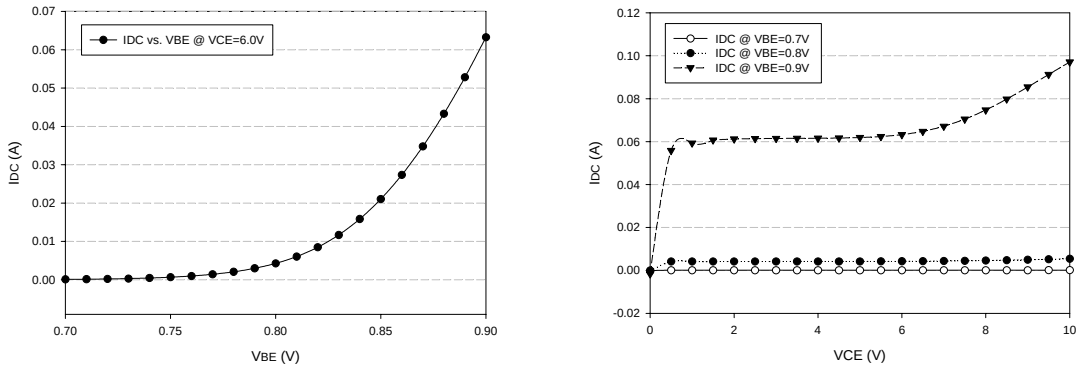
The first Class F power amplifier contains on-chip HBT, DC-blocking capacitors, and a RFC for base bias, the input/output matching networks and the harmonic loading network are implemented on PCB. The second one is a fully integrated Class

F power amplifier, leaving only the output matching network off-chip. The RFC for power feeding of both amplifiers also utilize Murata lumped elements for the concern of current density. The design concepts will be illustrated as follows.

3.3.1 Device Size and Bias Point

The desired output power at 1-dB compression point is 20dBm for Bluetooth Class 1, and the expected power efficiency is about 60% and 40% for the 1st and 2nd power amplifiers, respectively. Since the transistor of Class F power amplifier acts as a switch, Class B bias point is chosen. Moreover, a 6-V high voltage HBT is utilized to withstand large output voltage swing. The transistors T**1** and T**2** in Figure 3.5 are identical, and composed of two parallel HBTs. The total emitter length is 162.4 μm, with single emitter length/width of 20.3/0.9 μm.

Figure 3.6(a) is the curve of I_{DC} vs. V_{BE} @ V_{CE} = 6.0-V, which indicates that the turn-on voltage of the transistor is about 0.8V, the desired bias point. The IV-curve of the Class F power amplifiers is shown in Figure 3.6(b). The bias current at which no input power is 4.3mA, for Class F power amplifier, however, the dc current as well as the output optimum load, depends on the input power. As a result, the dc current at the input 1-dB compression point (about 10dBm) is about 50mA for both designs.



(a) (b)

Figure 3.6 I-V curves of HBT with emitter length/width = 162.4/0.9 μm (a)I_{DC} vs. V_{BE} @ V_{CE}=6.0V (b)I-V curve

3.3.2 Harmonic Loading Network

Briefly, a Class F amplifier derives its improved efficiency by using a multiple-resonator loading network to control the harmonic content of the collector voltage and/or collector current waveforms. A schematic diagram of a loading network commonly seen in final amplifier stages is shown in Figure 3.7. Here, the parallel network L1/C1 is resonant at the fundamental frequency f_0, while the parallel-resonant idler network L2/C2 is resonant at the third harmonic $3f_0$. In general, the series capacitor C3 is considered to be nothing more than a DC-blocking capacitor, but instead will now be considered as part of the overall loading network. At the fundamental frequency f_0, the third-harmonic idler L2/C2 represents a small inductance between the collector and the load which can be tuned out by adjusting the value of C3 to improve coupling to the load. In addition, at the second harmonic $2f_0$ the still inductive third-harmonic idler is in series with the now capacitive fundamental tank L1/C1 and the DC blocking capacitance C3. By proper selection of these five reactive elements, a loading network can be derived that will satisfy all three requirements simultaneously.

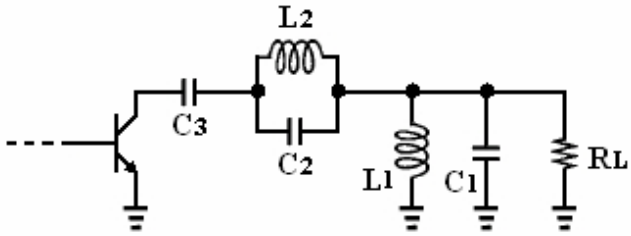


Figure 3.7 Third-order final networks

The design procedure begins with the selection of capacitor C1, which is determined by the load resistor RL, the centre frequency ω_0, and the desired bandwidth BW. The values for L1, L2, C2, and C3 are then determined in order as follows.

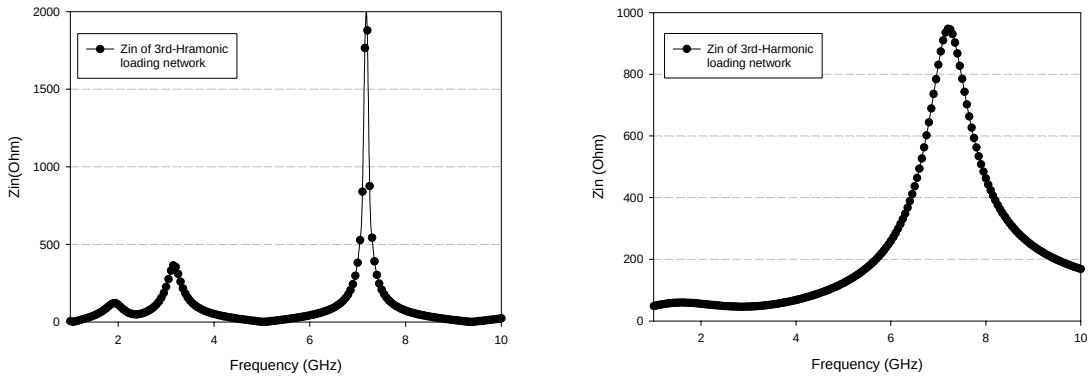
$$C_1 = \alpha/[(1-\alpha^2)\omega_0 R_L] \qquad \text{where} \qquad \alpha = (\omega_0 - \pi BW)/\omega_0$$

Now,

$$L_1 = 1/(\omega_0^2 C_1)$$
$$L_2 = 160 L_1 R_L^2/\{81[(3R_L)^2 + (2\omega_0 L_1)^2]\}$$
$$C_2 = 1/(9\omega_0^2 L_2)$$
$$C_3 = 8C_2$$

The component values derived here are approximations, as the parasitic reactances (normally capacitive) of the active devices will alter the resonances of the networks. Besides, the 0.35 μm SiGe process provides a minimum inductance of 0.6nH, which is still too large compared to the value derived from the equations above. As a result, there exist some difficulties to implement an ideal loading network. It is best to use these approximations as a starting point, referring the design to a computer optimization routine prior to committing to hardware. The simulated impedance curves of the two Class F loading network are shown in Figure 3.8 and Table 3.3.

In general, the best bandwidth is derived by designing the networks in such a manner as to cause the Q of the two resonant tanks and the Q of the second harmonic null to be nearly equal.



(a) (b)

Figure 3.8 Impedance curves of the (a)1st (b)2nd Class F PA loading network

Table 3.3 Impedance curves of the loading networks

Harmonics	1st Class F PA	2nd Class F PA
2.4GHz(f_0)	49.9 Ω	49.7 Ω
4.8GHz($2f_0$)	9.3 Ω	108.6 Ω
7.2GHz($3f_0$)	1878.8 Ω	947.5 Ω

Table 3.3 indicates that the 1st Class F PA performs better loading network impedance than the 2nd, because the loading networks of the 1st PA are implemented on PCB utilizing Murata lumped-elements and microstrip transmission lines. In addition to L1, C1, L2, C2 in Figure 3.7, adjusting the microstrip transmission line length can help to obtain the desired impedance. As for the fully integrated Class F power amplifier, the process limitations such as low-Q, limited on-chip inductance and capacitance, and lead length (including bond-wires) make it difficult to design a loading network satisfies all the circumstances.

3.3.3 Matching Networks

As shown in Figure 3.5, the input/output matching networks of the first PA design and the output matching network of the second PA design are implemented on PCB with Murata lumped elements and microstrip transmission lines. The L-section is used for its simplicity and practicability. The input matching network of the second designed PA, however, is integrated onto the chip, hence the parasitic bond-pad capacitors and the bond-wire inductors must be taken into account (as shown in Figure 3.9). The parasitic bond-pad capacitors fortunately can be eliminated by connecting the pad to the substrate, but the bond-wire inductors still increase the complexity of the matching network design. The inductances and capacitances used to synthesize the desired impedances are chosen according to the simulation results of ADS load/source pull at the beginning, and some fine tunes are needed then to adjust the practical situation.

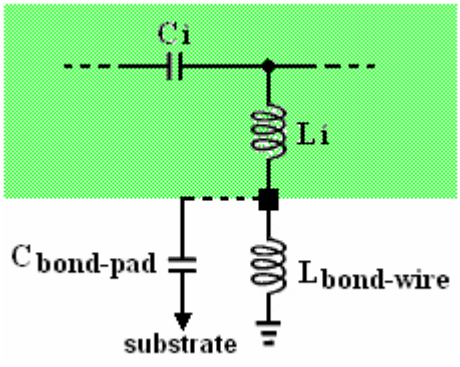
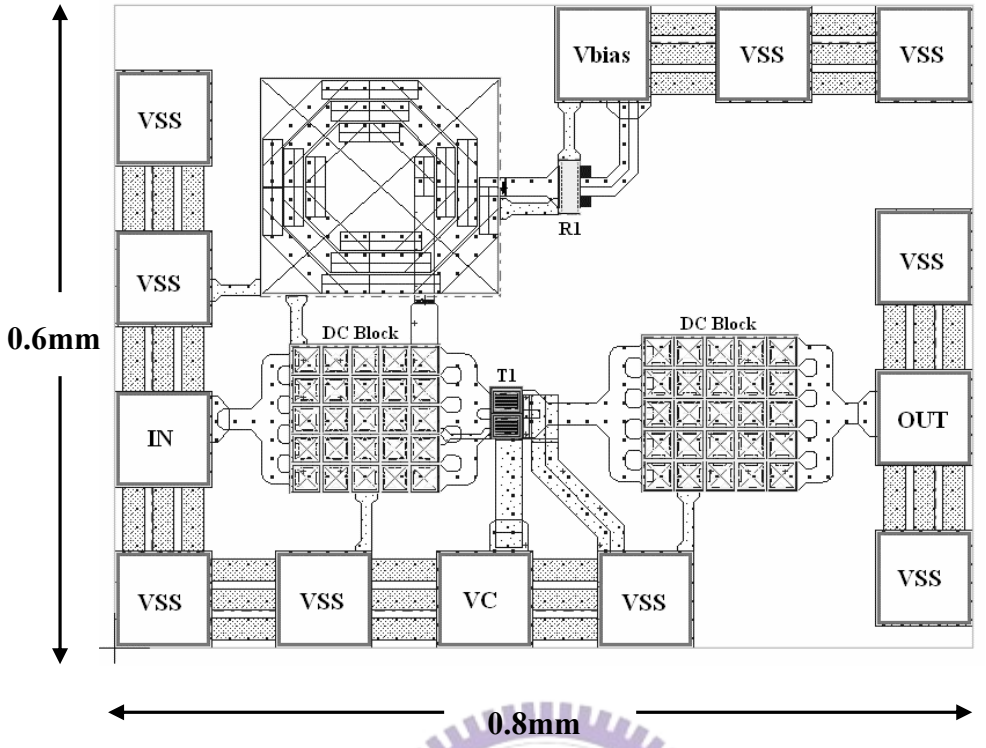


Figure 3.9 On-chip input matching network model

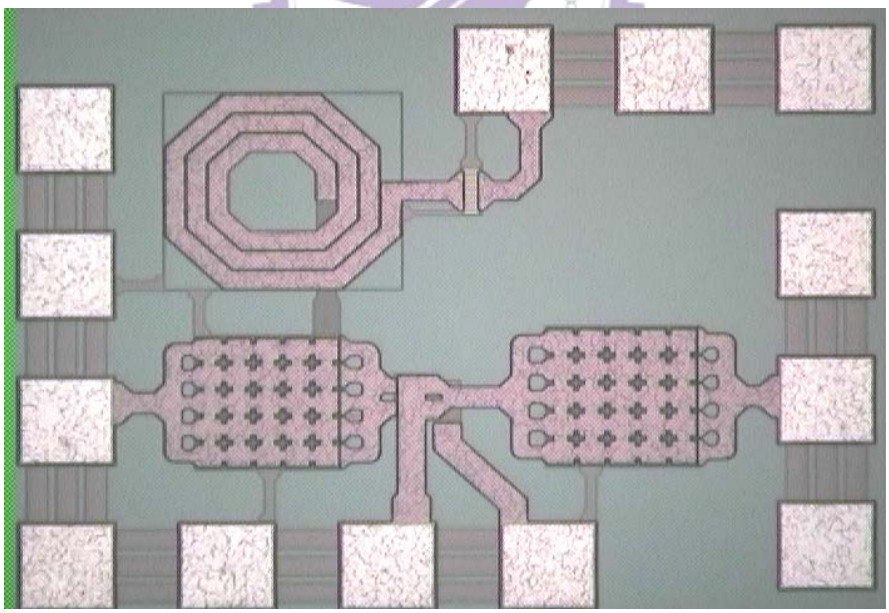
3.4 Layout Considerations

The power amplifiers are laid out using LAKER layout tool. Two experimental chips are designed and fabricated by TSMC 0.35 μm 3P3M BiCMOS technology. Figure 3.10 and Figure 3.11 are the overall layout of the first and second PA, respectively. The chip area of the fist PA is 0.8 mm by 0.6 mm, and the second one occupies an area of 1.2mm by 0.7mm.

Several Bond-pads are used to ground the emitter of the transistor to eliminate the inductance of the bond-wire. Since the DC current at 1dB point is large, wide and multi-layer metal lines can help to handle the current density. For the second design, a fully integrated Class F PA, spiral inductors and MIM capacitors are used to implement the input matching network, base bias RFC and output harmonic loading networks. Additionally, the guard-rings of the second design are separated into 3 parts to connect to the ground for the reason of preventing some feed-back behaviors. In order to reduce the mutual inductance between the inductors, the space between each inductor should be kept large enough.

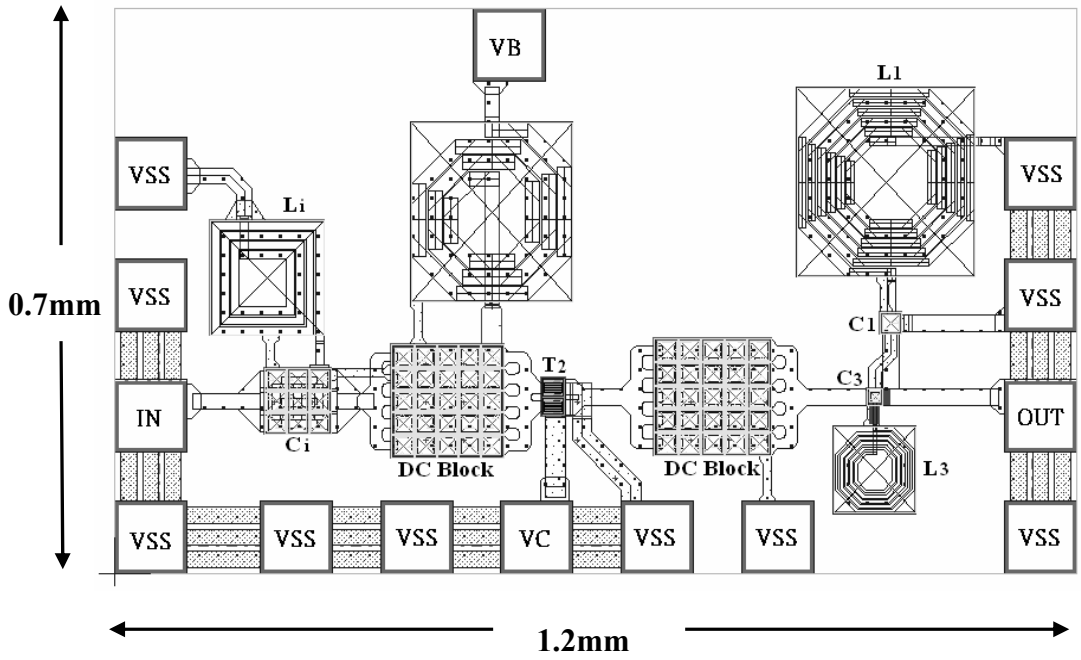


(a)

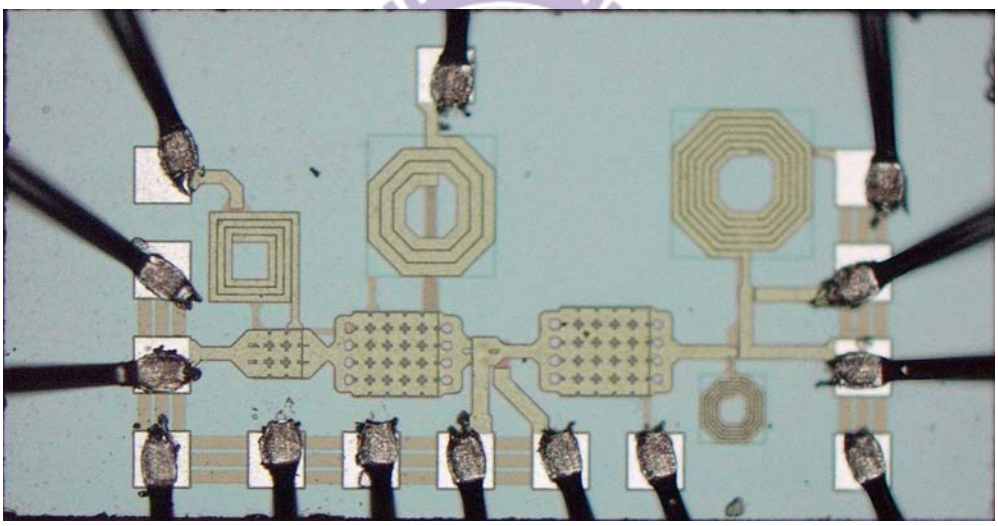


(b)

Figure 3.10 (a)Layout and (b)die photo of the first Class F PA design



(a)



(b)

Figure 3.11 (a)Layout and (b)die photo of the second Class F PA design

3.5 Simulation and Measurement Results.

The circuits are simulated using both Agilent ADS and Mentor Eldo-RF. The bond-wire effect, off-chip networks, microstrip transmission lines, and the variation of process, temperature, and supply voltage are considered in the simulations.

Adopting on PCB measurement, the power amplifier parameters, such as P_{1dB},

Gain, and IP3 can be measured by the setups and instruments (shown in Figure 2.17 and Figure 2.18) provided by the Chip Implementation Center (CIC). And S-parameters are measured by Agilent 8720ES S-parameter Network Analyzer.

- Performances of the 1st Class F power amplifier design

The first Class F power amplifier contains an on-chip HBT, DC-blocking capacitors, and a RFC for base bias, the input/output matching networks and the harmonic loading network are implemented on PCB. Table 3.4 shows the original simulated performances of this amplifier design. However, the 1st Class F power amplifier faces a serious DC oscillation problem in the initial stage of measurement. Even that the decouple capacitors are added and input/output ends are terminated with 50Ω loads, the PA still starts to oscillate when the power supply turns on. The noise of the power supply enters the PA and finds some feed-back paths to destroy the circuit. Simulation results show that not only the base-collector parasitic capacitor C_{bc} but the guard-ring may cause stability problem at low frequency.

Table 3.4 Original simulation results of the 1st Class F PA

BiCMOS Class F Power Amplifier	
Specification	**Result**
Frequency(GHz)	**2.4**
Supply Voltage (V)	**6.0**
Bias Voltage(V)	**0.8**
DC current@1dB(mA)	**57**
IP1dB (dBm)	**10.0**
OP1dB (dBm)	**22.2**
Gain@1dB (dB)	**12.2**
PAE@1dB (%)	**62.4**
S11 (dB)	**-13.6**
S22 (dB)	**-12.9**

Figure 3.12 shows the stable factors of the Class F power amplifier, it indicates that though the PA is stable in the interested band, unstable condition may occur at lower frequencies.

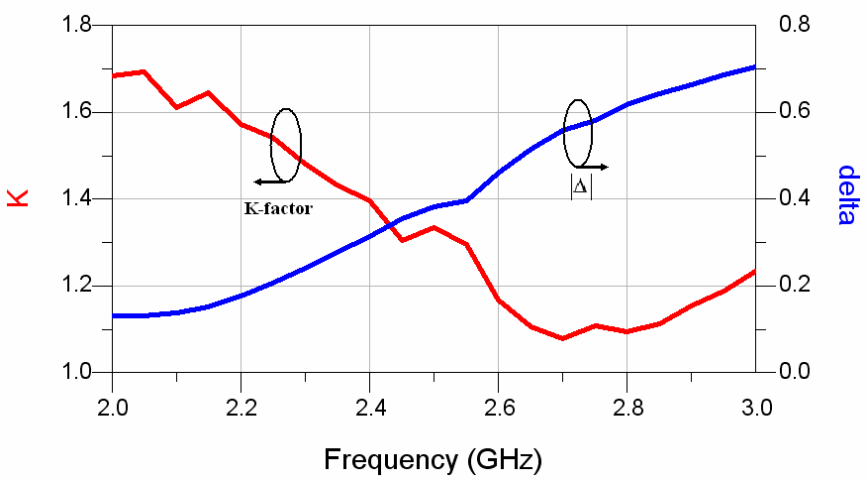


Figure 3.12 Stable factors of the first Class F PA design

The DC oscillation problem indicates that the RFCs at collector and base are not large enough. As a result, the RFC at collector is changed from 4.7nH to 22nH, and an additional RFC of 22nH is added to the base bias point, as Figure 3.13 shows. This protection successfully stop the DC oscillation, however, it also leads to some performance degradation of the modified PA.

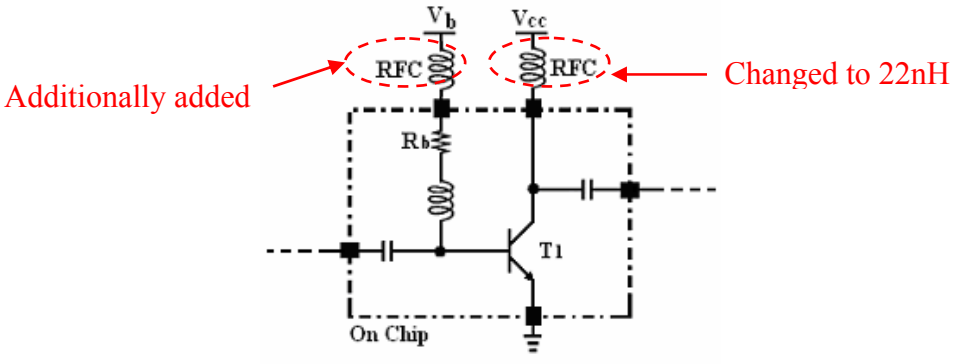


Figure 3.13 Reinforce the RFC to prevent DC oscillation

Figure 3.14 shows the board level photo of the Modified Class F power amplifier. Figure 3.15 and Figure 3.16 are the power parameters. The measured power curves

stop at input power of 10dBm in Figure 3.15 indicates that the SiGe high-voltage HBT can sustain about 20dBm output power.

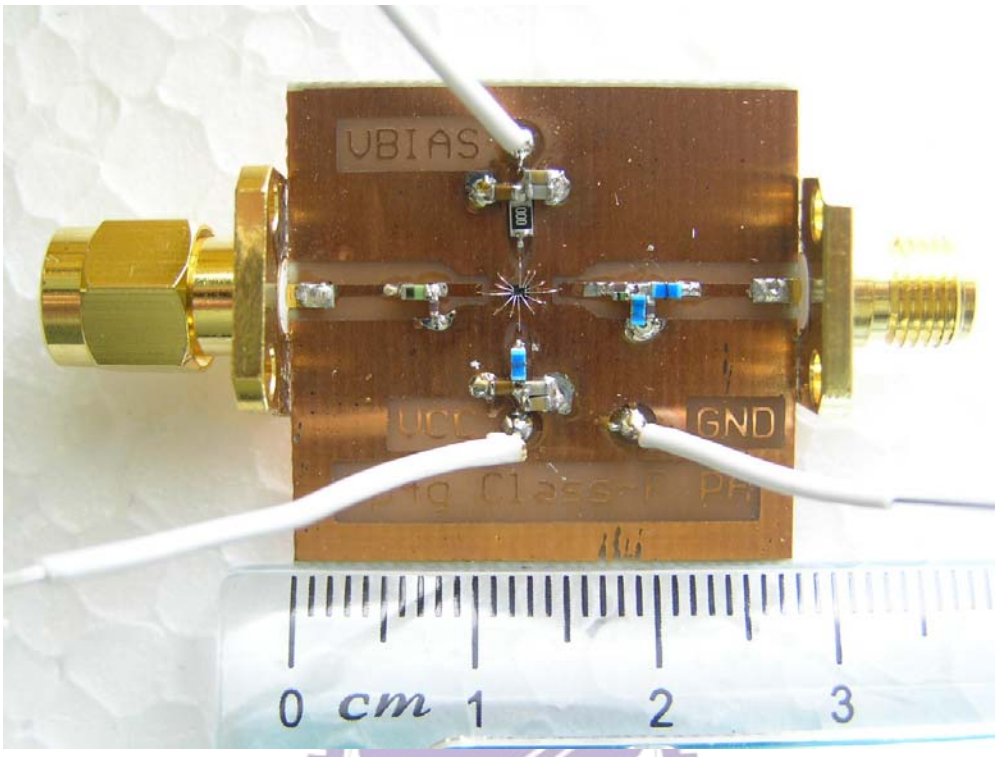


Figure 3.14 Board level photo of the modified Class F power amplifier

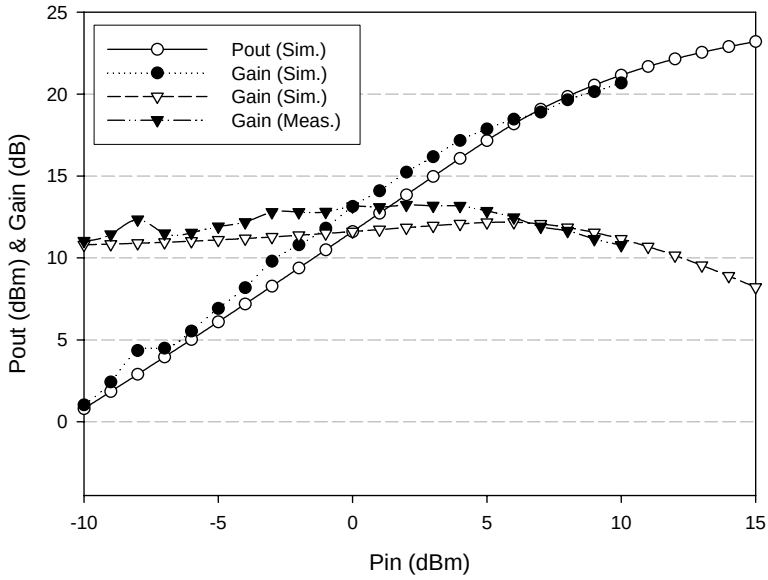


Figure 3.15 Modified Pout & Gain vs. Pin

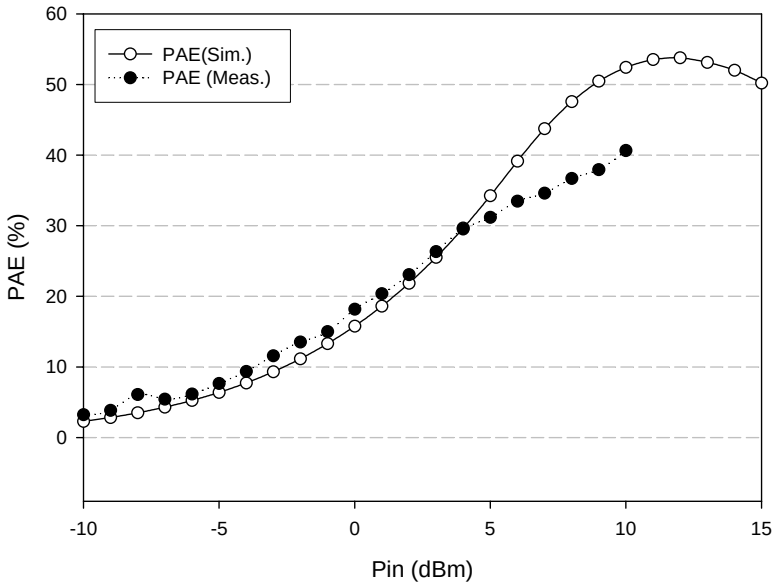
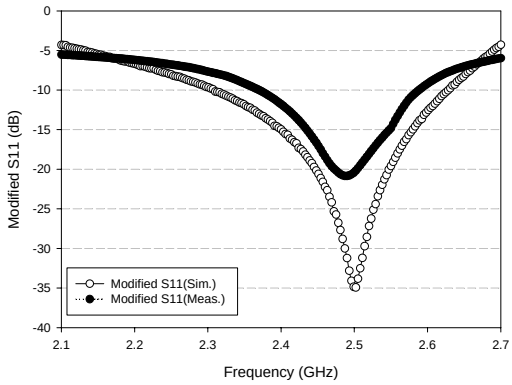


Figure 3.16 Modified PAE vs. Pin

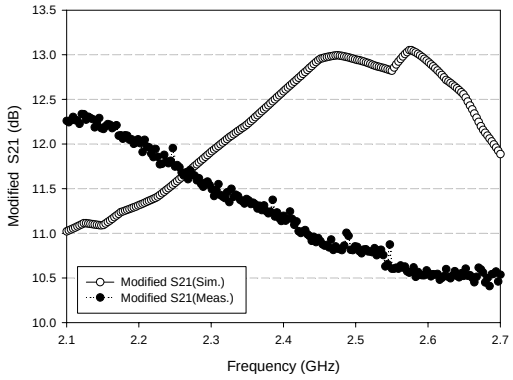
The PA has been broken since the input power exceeds 11dBm, which is supposed to be the breakdown limitation. From Figure 3.15 and Figure 3.16 the Pin of 1dB compression point should be larger than 10dBm and the corresponding Pout could be better than 20dBm with PAE above 40%.

The S-parameters shown in Figure 3.17 indicates that this power amplifier can work with reasonable performances. Figure 3.18 is the simulated transient waveform of the collector voltage, and Figure 3.19 is the simulated PAE in the Bluetooth frequency band (2400-MHz ~ 2483.5-MHz).

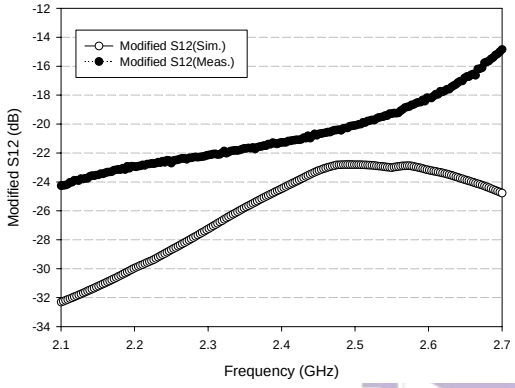
The Summary characteristics of the first Class F power amplifier design are shown in Table 3.5.



(a)



(b)



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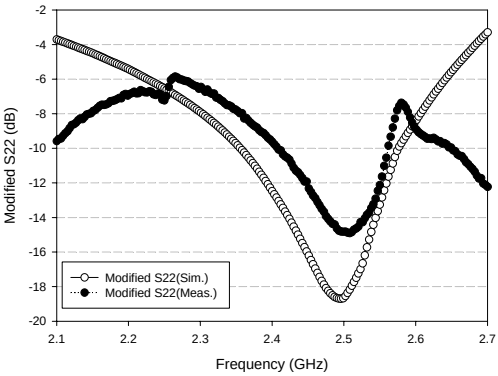


(d)

Figure 3.17 Modified S-parameters (a)S11 (b)S21 (c)S12 (d)S22

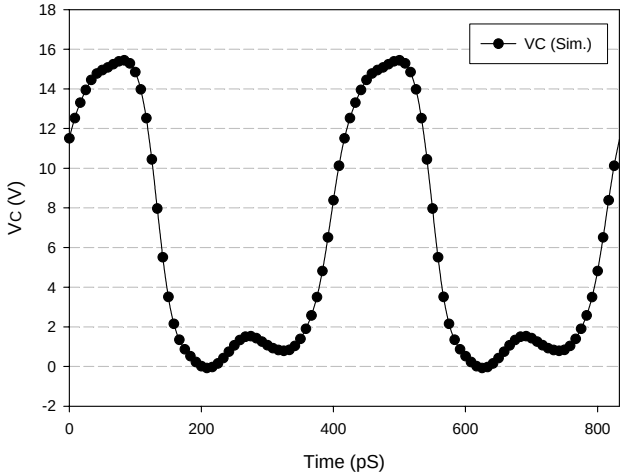


Figure 3.18 Modified transient plot of the collector voltage

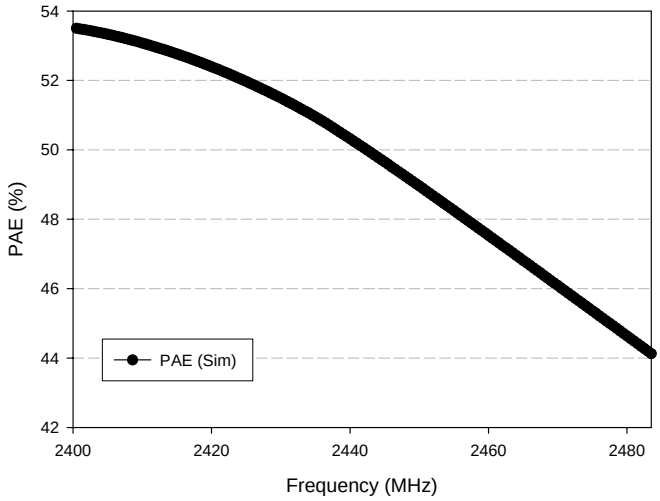


Figure 3.19 Modified PAE vs. frequency

Table 3.5 Summary characteristics of the first Class F power amplifier

Class F Power Amplifier (TSMC 0.35 μm SiGe BiCMOS)			
Spec.	**Original Simulation**	**Modified Simulation**	**Measurement**
Frequency(GHz)	**2.4**	**2.4**	**2.4**
Supply Voltage (V)	**6.0**	**6.0**	**6.0**
Bias Voltage(V)	**0.8**	**0.8**	**0.8**
I_{DC}@1dB (mA)	**57**	**53**	**N/A**
IP1dB (dBm)	**10.0**	**12.5**	**>10.0**
OP1dB (dBm)	**22.2**	**22.5**	≃ 20
Gain@1dB (dB)	**12.2**	**10.0**	**N/A**
PAE@1dB (%)	**62.4**	**53.5**	≃ 40
IIP3 (dBm)	**19.5**	**21.8**	**N/A**
OIP3 (dBm)	**35.5**	**36.0**	**N/A**
S11 (dB)	**-13.6**	**-15.0**	**-11.8**
S22 (dB)	**-12.9**	**-12.5**	**-9.6**

- Performances of the 2nd Class F power amplifier design

The second design is a fully integrated Class F power amplifier, leaving only the output matching network off-chip. Figure 3.20 shows the measured S-parameters, and

Table 3.6 is the original simulated performances of this amplifier design.

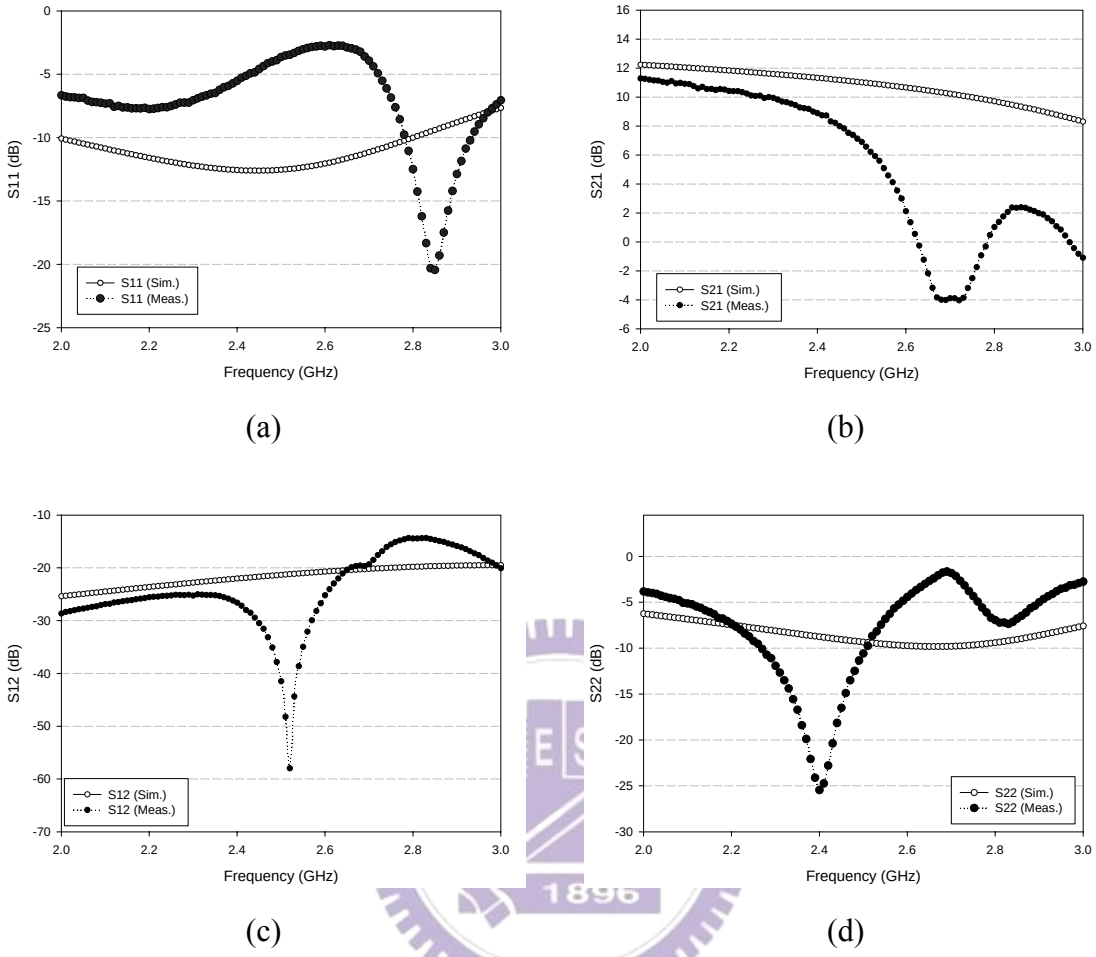
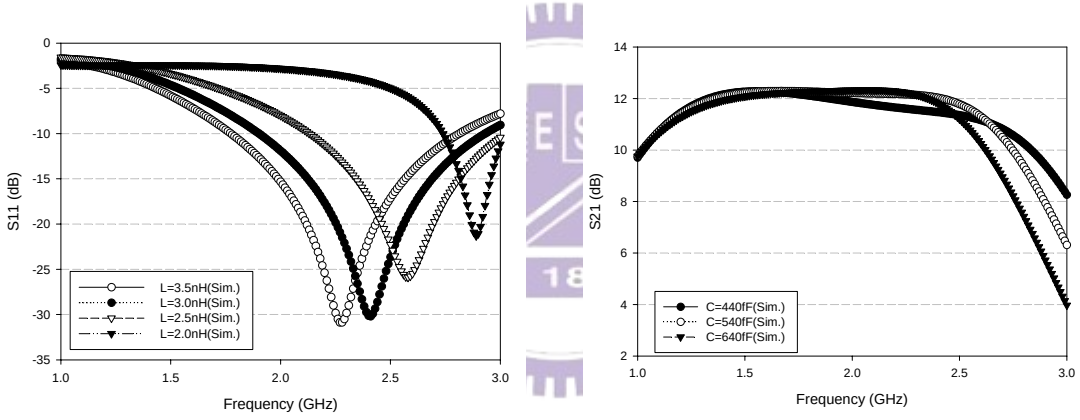


Figure 3.20 S-parameters (a)S11 (b)S21 (c)S12 (d)S22

Table 3.6 Original simulation results of the 2nd Class F PA

BiCMOS Fully integrated Class F Power Amplifier	
Specification	**Result**
Frequency(GHz)	**2.4**
Supply Voltage (V)	**6.0**
Bias Voltage(V)	**0.8**
DC current@1dB(mA)	**48**
IP1dB (dBm)	**10.0**
OP1dB (dBm)	**20.8**
Gain@1dB (dB)	**10.8**
PAE@1dB (%)	**39.6**
S11 (dB)	**-12.6**
S22 (dB)	**-11.3**

Figure 3.20 indicates that S11 shifts to about 2.85GHz, and S21 decays sharply above 2.5-GHz. Since it's a fully integrated power amplifier, the parasitic effects should be the reasonable suspect. As mentioned in 3.3.3, the bond-wire inductor ("L**bond-wire**" in Figure 3.9) plays an important part of the input matching network, and may be the most possible reason of the S11 mismatch. On the other hand, the collector bond-pad capacitor ("VC" in Figure 3.11(a)) is found to increase from 339fF to about 550fF, which causes the degeneration of S21 at frequency above 2.5GHz. For proving these points, Figure 3.21 shows the influences of L**bond-wire** on S11 and C**bond-pad** on S21. Furthermore, the bond-wire to ground the emitter could affect the whole performance, including helping the drifts of S11 and S21.



(a) (b)

Figure 3.21 (a)S11 with different input matching bond-wire inductors (b)S21 with different collector bond-pad capacitors

Since it's not easy to control the parasitic effects, additional input matching circuit is implemented on the PCB to have some fine tuning. Figure 3.22 shows the board level photo of the modified fully integrated Class F power amplifier.

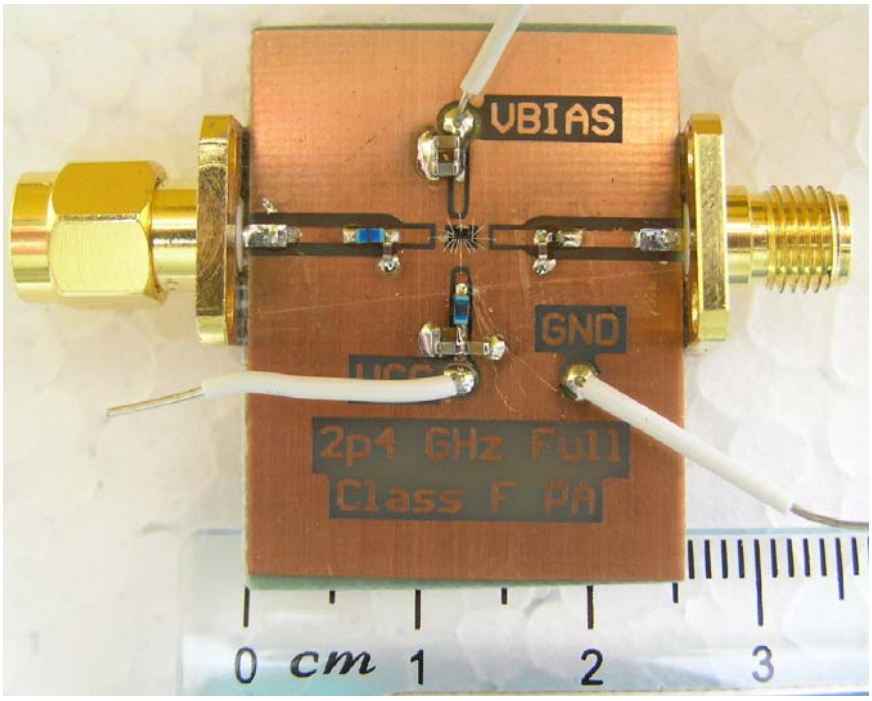


Figure 3.22 Board level photo of the modified fully integrated Class F power amplifier

Figure 3.23 and Figure 3.24 shows the modified power parameters. The P_{1dB} occurs at Pin = 10.0dBm and the corresponding Pout = 20.0dBm with PAE = 34.2%. Figure 3.25 indicates the two-tone test (with f_1=2400-MHz and f_2=2401-MHz) with IIP3 = 22dBm and OIP3 = 35dBm.

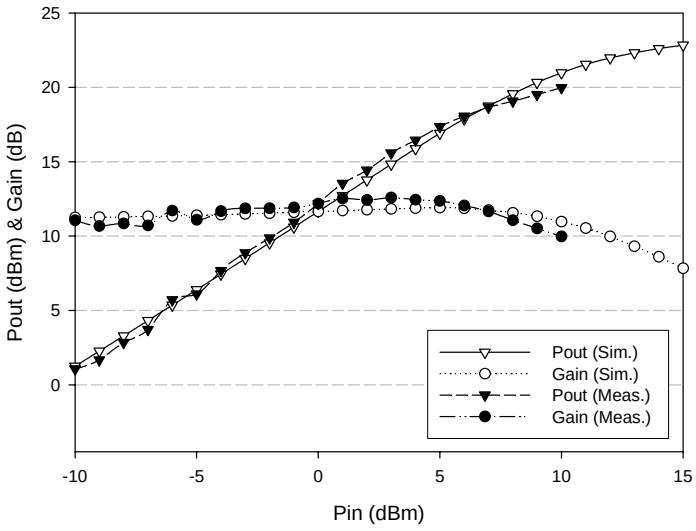


Figure 3.23 Pout & Gain vs. Pin

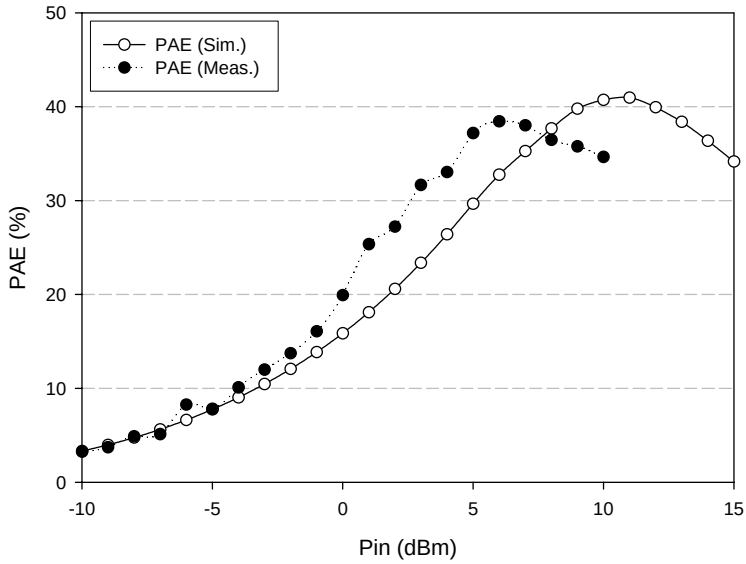


Figure 3.24 PAE vs. Pin

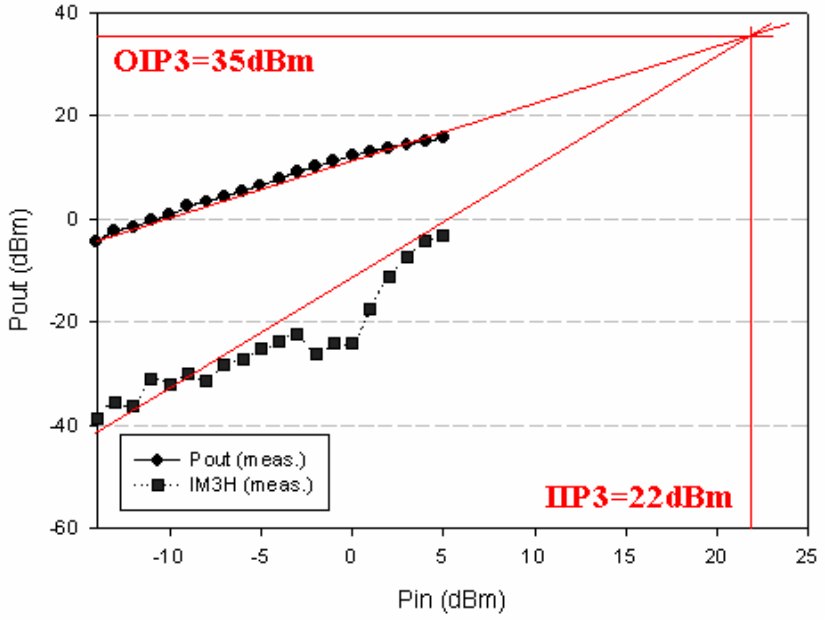


Figure 3.25 Two-tone test IIP3 and OIP3 measurement result

The modified S-parameters are shown in Figure 3.26. Figure 3.27 is the simulated transient waveform of the collector voltage, and Figure 3.28 is the measured PAE in the Bluetooth frequency band (2400-MHz ~ 2483.5-MHz). The Summary characteristics of the fully integrated Class F power amplifier design are

shown in Table 3.7. Table 3.8 is the comparisons between this works and recently papers.

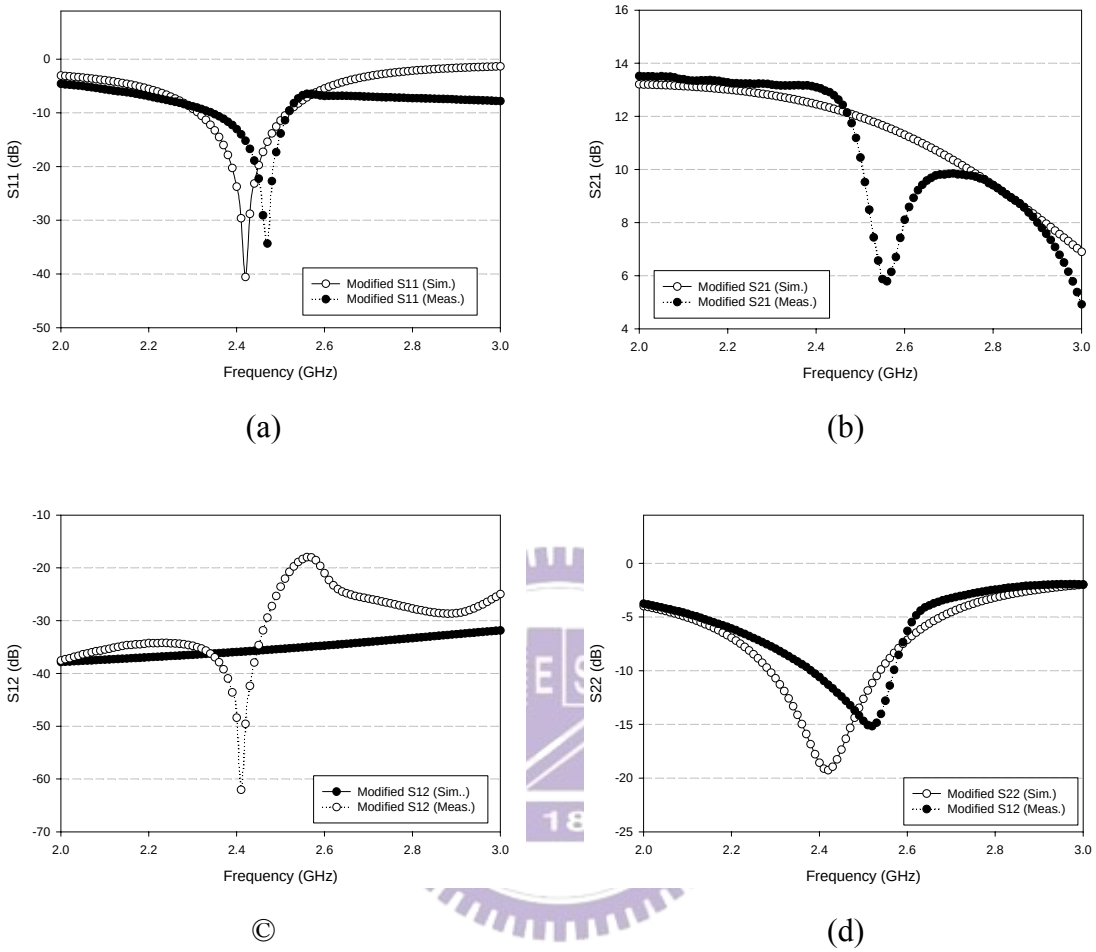


Figure 3.26 Modified S-parameters (a)S11 (b)S21 (c)S12 (d)S22

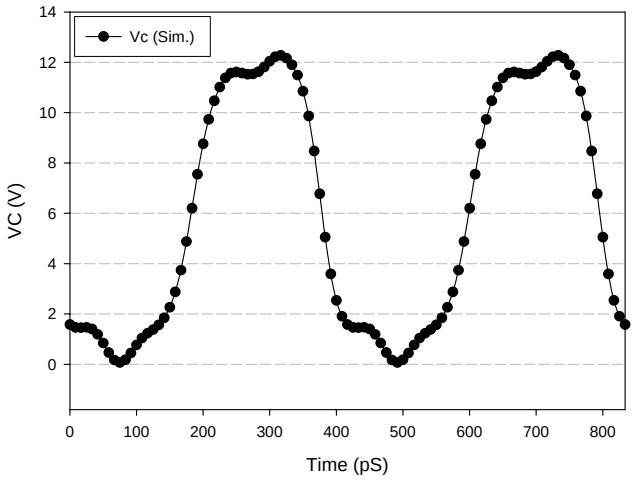


Figure 3.27 Modified Transient plot of the collector voltage

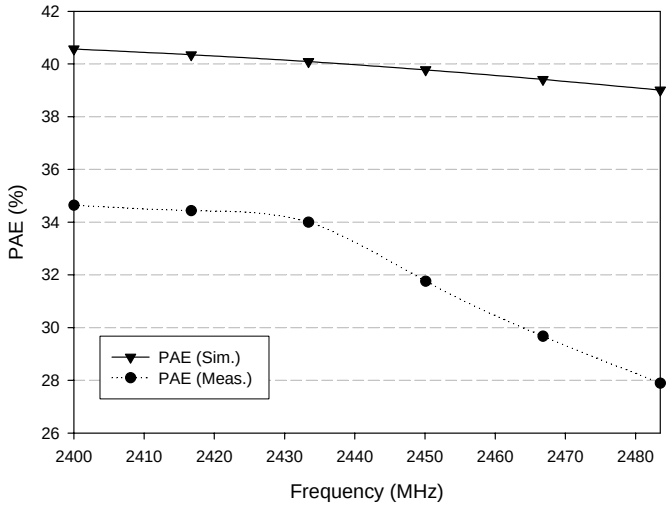


Figure 3.28 Modified PAE vs. frequency

Table 3.7 Summary characteristics of the second Class F power amplifier

Fully Integrated Class F Power Amplifier (TSMC 0.35 μm SiGe BiCMOS)			
Spec.	**Original Simulation**	**Modified Simulation**	**Measurement**
Frequency(GHz)	**2.4**	**2.4**	**2.4**
Supply Voltage (V)	**6.0**	**6.0**	**6.0**
Bias Voltage(V)	**0.8**	**0.8**	**0.8**
I_{DC}@1dB(mA)	**48**	**57**	**43**
IP1dB (dBm)	**10.0**	**11.5**	**10.0**
OP1dB (dBm)	**20.8**	**21.8**	**20.0**
Gain@1dB (dB)	**10.8**	**10.3**	**10.0**
PAE@1dB (%)	**39.6**	**40.6**	**34.2**
IIP3 (dBm)	**21.4**	**20.8**	**22.0**
OIP3 (dBm)	**35.5**	**33.0**	**35.0**
S11 (dB)	**-12.6**	**-23.7**	**-13.0**
S22 (dB)	**-11.3**	**-18.6**	**-10.6**

Table 3.8 Comparisons of the Class F power amplifiers with the previously reported PA's

Ref.	Process (μm)	Frequency (MHz)	Pout (dBm)	PAE (%)	Class	Condition
[18] 1999	0.35 CMOS	1980	30	41	E	Meas.
[19] 2000	0.24 CMOS	2400	23	39	B	Meas.
[20] 2001	0.6 CMOS	1900	22.8	42	F	Meas.
[21] 2001	0.25 CMOS	900	31.8	43	F	Meas.
[22] 2001	0.25 CMOS	900	29.5	41	E	Meas.
[13] 2003	0.25 CMOS	2450	20	28	AB	Meas.
[23] 2003	0.18 SiGe	2200	<10	25	F	Meas.
[24] 2003	0.35 CMOS	2400	20	59	E	Sim.
[25] 2003	0.35 CMOS	2400	18	33	E	Meas.
[26] 2003	0.35 CMOS	2650	25.2	38	E	Meas.
[27] 2004	0.18 CMOS	8000	20	39	F	Meas.
[28] 2004	GaAs pHEMT	900	22	71.4	F	Meas.
[29] 2005	GaAs pHEMT	2000	19.9	70.5	F	Meas.
1st design of this work	0.35 SiGe	2400	>20	≈40	F	Meas.
2nd design of this work	0.35 SiGe	2400	10	20	F	Meas.

Chapter 4
Conclusions and Future Works

4.1 Conclusions

In this thesis, three chips are designed and fabricated. The first describes a 0.18 μm CMOS self-biased dual-band driver amplifier for WLAN applications. With single chain (single input / single output) dual-band matching networks, the amplifier provides the same functionalities of two separated PA's optimized to different frequency bands. The proposed approach reduces almost half of the size, cost, and power consumption compared with conventional parallel architecture. Measurement results show that the dual-band amplifier can provide an IIP3 of 13.0 (15.0) dBm, output power of 8.3 (7.2) dBm with a PAE of 17.1 (9.3) % at 2.45- (5.25-) GHz. The chip occupies an area of 0.85 mm by 0.7 mm. Due to the unclear large signal model in high frequency, the amplifier does not match perfectly and results in unsatisfied performance in 5.2-GHz band.

The last two designs are both 0.35 μm SiGe BiCMOS Class F power amplifiers for Bluetooth system. The second contains on-chip HBT, DC-blocking capacitors, and a RFC for base bias, the input/output matching networks and the harmonic loading network are implemented on PCB using Murata lumped elements. Since the off-chip components have better Q-factor, this Class F amplifier is expected to achieve high efficiency. The other motivation of this design is to verify the characteristics of the HBT device. This amplifier faces a serious DC oscillation problem, the solution is to reinforce the RFC of both base and collector bias with some degradation of performance. The device goes breakdown when the input power exceeds 11dBm, and

the measured data show that the output power is about 20dBm with PAE about 40%. The chip area is $0.8 \times 0.6\ mm^2$.

Owing to the experience of the second design, the input matching and harmonic loading networks are further integrated onto the chip, hence the third design is a fully integrated Class F power amplifier. The chip size is as small as $1200\mu m \times 700\mu m$. The amplifier delivers an output power of 20dBm and a PAE as high as 34.2%, the experimental IIP3 is 22dBm. The bond-wire inductor of the input matching network component and incorrect parasitic bond-pad capacitor lead to some mismatches between simulation and measurement results. To remedy the problem, another input matching network is implemented outside the chip to do some fine tuning.

4.2 Future works

- Dual-band driver amplifier

From this design experience, we can get familiar with the characteristics of the $0.18\ \mu m$ process. The further researches focus on the improvement of performances in 5.2-GHz band. Moreover, since the Murata lumped elements do not work perfectly at high frequency, the matching networks should be integrated onto the chip. The integration could firstly contain only the capacitors, as for the inductors, a complete inductor library is needed to be built. The next step of the dual-band amplifier design is to accomplish the two-stage power amplifier, at that time, to solve the breakdown problem at high output power level is another issue.

- Class F power amplifier

Observing the measurement results, the SiGe HBT has very good power performance. The main drawback is its low breakdown voltage (though higher than that of CMOS). On the other hand, the smallest inductance of SiGe process is 0.6nH,

which is not small enough to design a perfect harmonic loading network for 3rd order harmonic. As a result, a complete inductor library is also waited to be built so that the PAE could be improved further. In addition, on-chip biasing network could be designed to simplify the use of power supply. Last but not least, a driver amplifier is needed to make the power amplifier more complete.

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Publication Remarks

- Conference Paper

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- Submitting

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