

A Phase-Locked Loop With Injection-Locked Frequency Multiplier in 0.18- μm CMOS for V-Band Applications

Chung-Yu Wu, *Fellow, IEEE*, Min-Chiao Chen, and Yi-Kai Lo

Abstract—In this paper, a novel CMOS phase-locked loop (PLL) integrated with an injection-locked frequency multiplier (ILFM) that generates the V-band output signal is proposed. Since the proposed ILFM can generate the fifth-order harmonic frequency of the voltage-controlled oscillator (VCO) output, the operational frequency of the VCO can be reduced to only one-fifth of the desired frequency. With the loop gain smaller than unity in the ILFM, the output frequency range of the proposed PLL is from 53.04 to 58.0 GHz. The PLL is designed and fabricated in 0.18- μm CMOS technology. The measured phase noises at 1- and 10-MHz offset from the carrier are -85.2 and -90.9 dBc/Hz, respectively. The reference spur level of -40.16 dBc is measured. The dc power dissipation of the fabricated PLL is 35.7 mW under a 1.8-V supply. It can be seen that the advantages of lower power dissipation and similar phase noise can be achieved in the proposed PLL structure. It is suitable for low-power and high-performance V-band applications.

Index Terms—Injection-locked frequency multiplier (ILFM), millimeter-wave circuits, phase-locked loop (PLL), RF CMOS.

I. INTRODUCTION

THE FREQUENCY synthesizer (FS) is a key building block of the RF integrated circuit (RFIC), which generates the carrier signal to convert transmission data up to the desired frequency band. The transmission and reception qualities in the wireless communication system are determined by the performance of the local oscillator (LO) that is generated by the FS. In the conventional FS [1]–[3], the voltage-controlled oscillator (VCO) is always operated at the highest frequency to generate the LO signal. Owing to the limited performance of the active and passive devices, the performance of the VCO is mainly determined by the device technology. The implementation of the high-frequency divider is another important design issue in the conventional FS structure. The injection-locked frequency divider (ILFD) [4] or Miller divider [5] are the popular options for the high-frequency divider design. Unfortunately, the division ratio of these dividers [4], [5] is not high. If the output frequency of these dividers is still higher than the frequency that a static divider can handle, a multistage of these

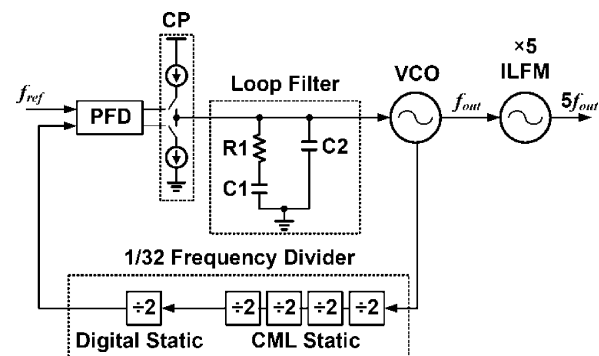


Fig. 1. Block diagram of the proposed V-band PLL.

dividers is required [6]. Since these high-frequency dividers are of narrowband characteristic, any frequency shift in each divider could cause the failure of the entire FS.

The other FS structure is composed of a low-frequency FS cascaded with a frequency multiplier to generate the desired output frequency [7], [8]. In this FS structure, the low-frequency FS is operated at the subharmonic of the desired frequency and the target frequency is generated by the frequency multiplier after the low-frequency FS. Obviously, it has the advantages of smaller division ratio and low power dissipation from the frequency divider. A frequency multiplier with a significant amount of power dissipation is, however, the main drawback [7]. Lately, a fully differential subharmonic injection-locked frequency multiplier (ILFM) has been proposed and demonstrated with low dc power consumption and large output power [9]. ILFM is, therefore, the feasible choice for the frequency multiplier in the design of the second FS structure.

In this paper, the design of a CMOS PLL cascaded with the ILFM for V-band applications is proposed and designed to verify the above design concept. The proposed CMOS ILFM is designed to generate the fifth-order harmonic frequency of the VCO output. The proposed PLL with ILFM is designed and fabricated using 0.18- μm bulk CMOS technology. The measured output frequency range is from 53.04 to 58.0 GHz, which is higher than the transition frequency ($f_T \sim 55$ GHz) of the device, but the highest frequency of the frequency divider in the proposed PLL structure is only 11.6 GHz. As a result, the total power dissipation can be reduced significantly as compared with previous work [1]–[3].

In Section II, the proposed architecture of the V-band phase-locked loop (PLL) and the building blocks of the proposed PLL including the VCO, ILFM, frequency divider, phase-frequency

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C.-Y. Wu and Y.-K. Lo are with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: cywu@alab.ee.nctu.edu.tw).

M.-C. Chen is with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan. He is now with the MStar Semiconductor Inc., Hsinchu 302, Taiwan.

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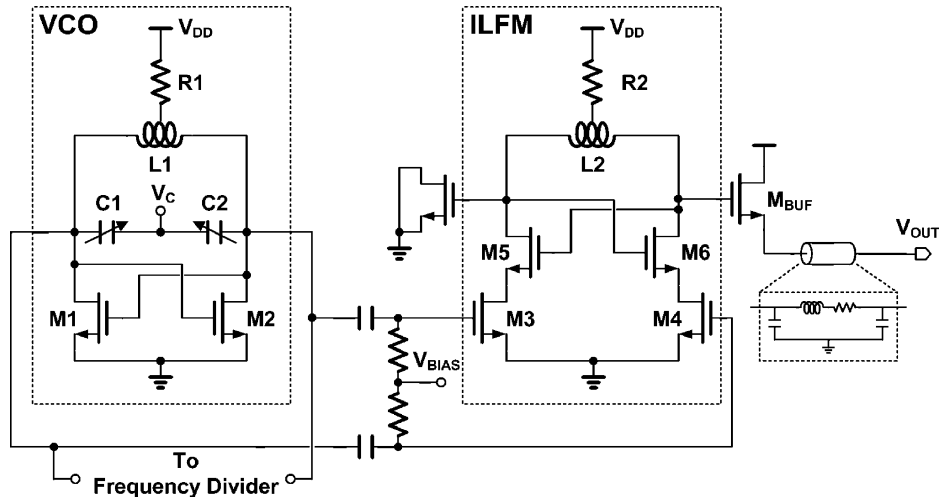


Fig. 2. Circuit diagram of both VCO and ILFM.

detector (PFD), charge pump (CP), and loop filter are described. The experimental results are shown in Section III. Finally, a conclusion is presented in Section IV.

II. PLL BUILDING BLOCKS

The proposed V -band third-order type-II CMOS PLL that is composed of a VCO, an ILFM, a $1/32$ frequency divider, a PFD, a CP, and a loop filter is shown in Fig. 1. The reference signal with the input power of 0 dBm and the frequency f_{ref} from 331.5 to 362.5 MHz is fed from the external signal generator. The output frequency ($5f_{out}$) with the frequency range from 53.04 to 58.0 GHz, which is five times the VCO output frequency (f_{out}), is generated by the ILFM.

A. VCO and ILFM

The circuit diagram of both the VCO and ILFM is shown in Fig. 2. The VCO is made of a cross-coupled pair M1/M2 to generate negative resistance for the compensation of the loss from the LC tank. An on-chip spiral inductor L1 with symmetric structure and accumulation mode MOS varactors C1/C2 are used in the VCO design. C1/C2 has the higher quality factor compared with pn-junction varactors. The poly-resistor R1 is designed for a proper bias condition of the cross-coupled pair. The utilization of resistor instead of PMOS current source is attributed to its free-of-flicker-noise property [10].

The schematic of the proposed ILFM can be divided into two stages [9]. The first stage is the frequency pre-generator stage and the second stage is the injection-locked oscillator (ILO) stage. The input signal from VCO is injected into the frequency pre-generator stage. The function of the frequency pre-generator stage that generates the fifth-order harmonic of the input injection signal is implemented by M3/M4. The conversion gain of the frequency pre-generator can be maximized by selection of an appropriate gate bias value of M3/M4 (V_{BIAS}). In addition, the locking range of the ILFM can be increased by an increase of the conversion gain of the frequency pre-generator [9].

The signal generated by the frequency pre-generator is directly transmitted into the ILO stage formed by M5/M6 and a symmetric spiral inductor L2. The value of the inductor L2 is chosen so that it can resonate with the total capacitances at the

drain of M5/M6 at the fifth-order harmonic frequency of the input frequency. M5/M6 is used to generate negative conductance to cancel the loss of the LC tank for higher output power of the ILO stage and to make the output signal differential. Without input signal, the output impedance of M3/M4 degrades the loop gain of the cross-couple pair M5/M6. However, when a large input signal is applied to the gates of M5/M6, M5/M6 are operated at the cutoff or linear region most times within a period of the input signal. Therefore, the effect of M3/M4 output impedance is not serious to degrade the performance of the ILO stage. Even with the loop gain degradation from M3/M4, the free-running output of ILFM can be designed in [9].

If the ILFM is designed with the loop gain larger than unity, free-running output signal of the ILFM occurs while there is no input injection. Hence, this type of ILFM is called an ILFM with free-running output. On the other hand, if the ILFM is designed with the loop gain less than unity, the ILFM does not produce any output signal, while there is no input injection because the oscillation condition of free-running output is not satisfied. Thus, this type of ILFM is called an ILFM without free-running output. In the latter case, the ILFM is similar to a conventional frequency multiplier, but with a positive-feedback load to increase the output amplitude.

The resistor R2 is designed for the improvement of the harmonic rejection ratio (HRR) at every undesired even-order harmonic [9]. Since the output frequency is higher than the transition frequency f_T of the device, the open-drain output buffer is not suitable in this design owing to the poor property of the device. A source follower is chosen as the output buffer for testing purposes. The simulated voltage loss from the output buffer is, however, still higher than 10 dB. Finally, the length of the interconnection metal line from the ILFM output to the testing pad is around $70 \mu\text{m}$. To avoid the frequency shift, the characteristic of this metal line is simulated by the 3-D electromagnetic (EM) computer-aided design (CAD) tool High Frequency Structure Simulator (HFSS).

Based upon the model developed in [9], the extension model for the proposed ILFM is shown in Fig. 3(a). The frequency pre-generator is modeled as the nonlinear characteristic function $f(v_I)$, the active devices of the ILO stage are modeled as

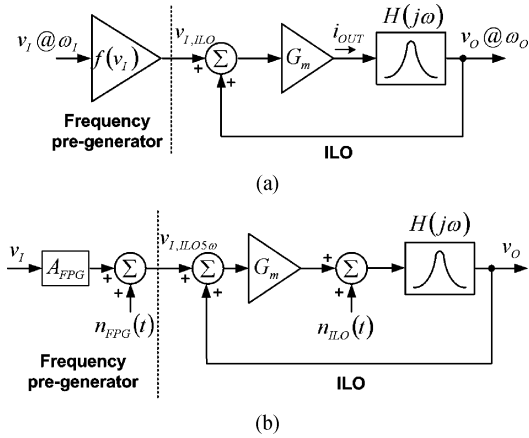


Fig. 3. ILFM model. (a) Simplified signal flow model. (b) Simplified noise source model.

the linear constant transconductance stage G_m , $H(j\omega)$ is the transfer function of the bandpass LC -tank filter in the output of the ILO stage, $v_I(t)$ is the incident signal with the input frequency ω_I , $v_O(t)$ is the output signal with the frequency $\omega_O = 5\omega_I$, $v_{I,IL\omega}(t)$ is the output signal of the frequency pre-generator, and i_{OUT} is the output current of the transconductance stage G_m .

Firstly, the model for ILFM with free-running output is developed. By use of the same process shown in [9] and extension of the nonlinear characteristic function $f(v_I)$ into the fifth-order polynomial, the normalized locking range of the ILFM with free-running output can be expressed as

$$\frac{|\omega - \omega_r|}{\omega_r} \leq \frac{1}{2Q} \sqrt{\frac{(a_5 V_i^5)^2}{(16V_o)^2 - (a_5 V_i^5)^2}} \approx \frac{1}{2Q} \left| \frac{a_5 V_i^5}{16V_o} \right| \quad (1)$$

where ω_r and Q are the resonant frequency and quality factor of the LC tank in the output of the ILFM, respectively, the coefficient a_5 is the nonlinear characteristic property of fifth-order term from frequency pre-generator, and V_i and V_o are the incident and output amplitude, respectively.

The simplified noise model of the proposed ILFM is shown in Fig. 3(b) [9] where the conversion gain of the fifth-order harmonic signal in the frequency pre-generator is simplified to be a constant value A_{FPG} and $v_{I,IL\omega}$ is the signal with frequency $5\omega_I$. The noise contribution from the frequency pre-generator and the ILO are modeled as $n_{FPG}(t)$ and $n_{ILO}(t)$, respectively. The linear phase-domain model [11], [12] is adopted to calculate the output phase noise. The derived output phase noise can be expressed as

$$S_{OUT}(\omega_m) = \frac{5^2}{1 + \left(\frac{\omega_m}{\omega_p}\right)^2} S_{INJ}(\omega_m) + \frac{1}{1 + \left(\frac{\omega_m}{\omega_p}\right)^2} S_{FPG}(\omega_m) + \frac{\left(\frac{\omega_m}{\omega_p}\right)^2}{1 + \left(\frac{\omega_m}{\omega_p}\right)^2} S_{ILO}(\omega_m) \quad (2)$$

where the corner frequency of the ILFM noise transfer function ω_p can be written as

$$\omega_p = \frac{\omega_r}{2Q} \frac{\eta}{1 + \eta} \quad (3)$$

$$\eta = \frac{A_{FPG} V_i}{V_o}. \quad (4)$$

In the above equations, ω_m is the offset frequency from output frequency ω_O and $S_{OUT}(\omega_m)$, $S_{INJ}(\omega_m)$, $S_{FPG}(\omega_m)$, and $S_{ILO}(\omega_m)$ are the noise spectral densities of output, input injection signal, frequency pre-generator, and ILO circuit, respectively.

The ILFM with free-running output has been discussed in [9]. The quality factor Q of the LC tank in this type of ILFM is maximized for low power consumption and large output power. It can be seen from (1) that the output frequency range of this type ILFM is decreased due to the selection of large quality factor Q of the LC tank. The output frequency range of the ILFM is only 2% [9]. The output frequency of the ILFM can be increased by the degradation of the LC tank quality factor. Extra power consumption is required to keep the oscillation condition. However, due to the limited performance of active devices in 0.18- μm CMOS technology, it is difficult to maintain ILFM oscillation with small quality factor Q of the LC tank. In addition, the value of a_5 in (1) is strongly dependent on the fifth-order harmonic conversion characteristic of the active device. However, the high-order harmonic conversion efficiency of the active device is not good. In other words, the value of a_5 in (1) is very small. Therefore, the locking range of the ILFM operated with free-running output is small. When the ILFM is integrated with a low-frequency VCO, the output frequency range is limited by the locking range of the ILFM due to the limited performance of active devices and high-order harmonic conversion efficiency.

Secondly, the ILFM without free-running output is discussed. In this case, the constraint of satisfying the free-running oscillation condition is removed; the output signal is always locked when it is produced. When an ILFM designed without free-running output is integrated with a low-frequency VCO, the output frequency range is determined by the tuning range of the low-frequency VCO multiplied by the harmonic ratio, not by the locking range in (1) of the ILFM designed with free-running output. Thus, the output frequency range is not affected by a_5 and can be increased by increasing the tuning range of the low-frequency VCO. The ILFM without free-running output is a better choice for wide output frequency applications. In this design, because the performance of active devices in 0.18- μm CMOS technology is limited and wide output frequency is desired, the ILFM without free-running output is designed. For the ILFM without free-running output, the phase-noise performance is the same as in (3) [13].

Fig. 4 shows the HSPICE simulated normalized fifth-order harmonic currents (I_{d5}/I_{dmax}) of the frequency pre-generator where I_{d5} is the magnitude of the output drain current at the fifth-order harmonic frequency, I_{dmax} is the magnitude of the output total drain current, and conduction angle θ_{CON} is the device turn-on angle within one period of the input signal. The simulation condition involves a 12-GHz input signal with 4-dBm input power and a MOSFET device with dimensions of $W/L = 18 \mu\text{m}/0.18 \mu\text{m}$. Due to the parasitic capacitances of

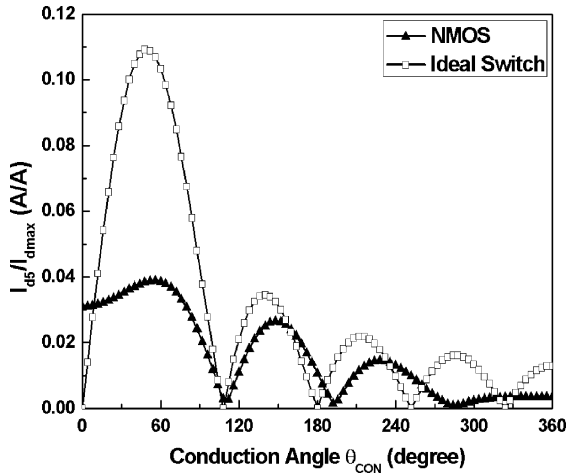


Fig. 4. HSPICE simulated coefficient of output harmonic current as a function of conduction angle.

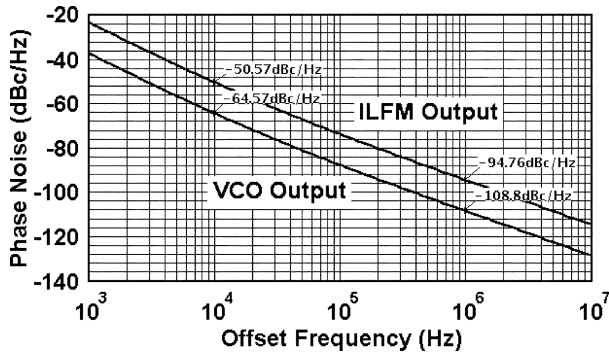


Fig. 5. Simulated output phase of VCO and ILFM.

the MOSFET device from gate–drain and drain–source, those undesired ac currents through gate–drain and drain–source are included in the output drain current I_{dmax} and I_{d5} . It can be seen from Fig. 4 that the normalized harmonic current curve is not the same as the ideal switch condition in [14].

In general, the fifth-order harmonic current is mainly determined by the coefficient of a_5 . In the case of an ILFM without free running, the output power is proportional to the coefficient a_5 because the larger fifth-order harmonic is generated; the larger desired fifth-order harmonic signal is transmitted to the ILO stage for signal amplification. The devices M3/M4 performed as the frequency pre-generator functions are, therefore, biased at a conduction angle θ_{CON} of 230° in the proposed ILFM for higher output power. Finally, the value of V_{BIAS} can be calculated by a given input power, the device threshold voltage, and a suitable conduction angle [14].

The simulated phase noises of VCO output and ILFM output are shown in Fig. 5. It can be seen from Fig. 5 that the phase-noise differences between VCO output and ILFM output at 10-kHz and 1-MHz offset are 14.0 and 14.04 dB, respectively. If the noise contribution from the frequency pre-generator is negligible, the output phase noise is 13.98 dB ($= 10\log(5^2)$) higher than that from the input signal with a small offset frequency (3). Therefore, the noise contributions from the frequency pre-generator to the output phase noise at

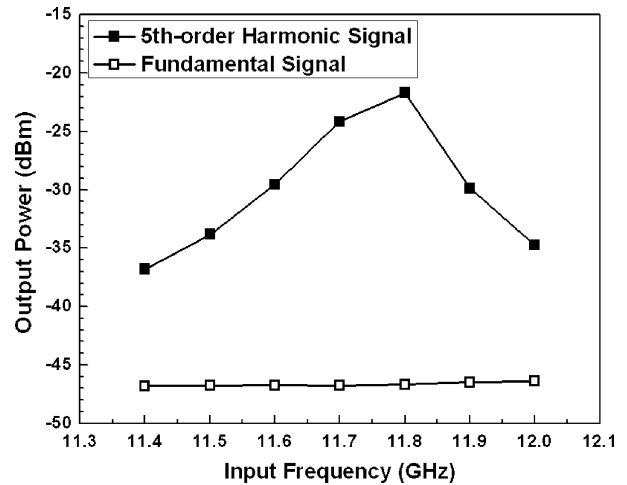


Fig. 6. Simulated ILFM output power at fundamental and fifth-order harmonic frequencies versus input frequency from 11.4 to 12.0 GHz.

10 kHz and 1 MHz are 0.02 and 0.06 dB, respectively. The simulated power consumption of VCO and ILFM are 6.72 and 6.08 mW, respectively.

Since the ILFM without free-running output is selected in this design, the output power is proportional to the impedance of the positive-feedback load. The simulated output signal with the frequency at the fifth-order harmonic of the input signal is a function of input frequency and is shown in Fig. 6. The maximum output power is -21.68 dBm, as the input frequency is 11.8 GHz. Due to the bandpass load of the ILFM, the fundamental signal is lower than -46 dBm at the ILFM output. The HRR to fundamental signal is larger than 10 dB in the desired frequency range.

B. Frequency Divider

The 1/32 frequency divider is composed of the four-stage current-mode logic (CML) divide-by-2 dividers and one-stage digital static flip-flop-based divide-by-2 divider. The CML divider [15] is made of a master–slave D-type flip-flop (DFF) with the output terminal (Q) connected to the input terminal (D) in inverted polarities. The CMOS CML divider has been demonstrated to have high-speed operation with low power dissipation because the full swing for internal operation is not required [16]. The schematic diagram of the master and slave latch is shown in Fig. 7(a). In the latch circuit, the sense stage consists of transistors M1, M3, and M4, whereas the latch stage comprises the transistors M2, M5, and M6. In order to increase the operational frequency, the output load is chosen as the poly-resistors R1/R2 for smaller parasitic capacitance instead of PMOS load [17]. Each CML divider stage is designed to drive the next stage directly at its operational frequency by changing the device ratios of sense stage and latch stage.

Since a full swing input for PFD is required, the last stage of the 1/32 frequency divider is designed as the digital-type frequency divider. The divide-by-2 divider comprises two ring-connected D-latches. The circuit diagram of the digital static divider is shown in Fig. 7(b). The simulated total power consumption of 1/32 frequency divider is 16.72 mW.

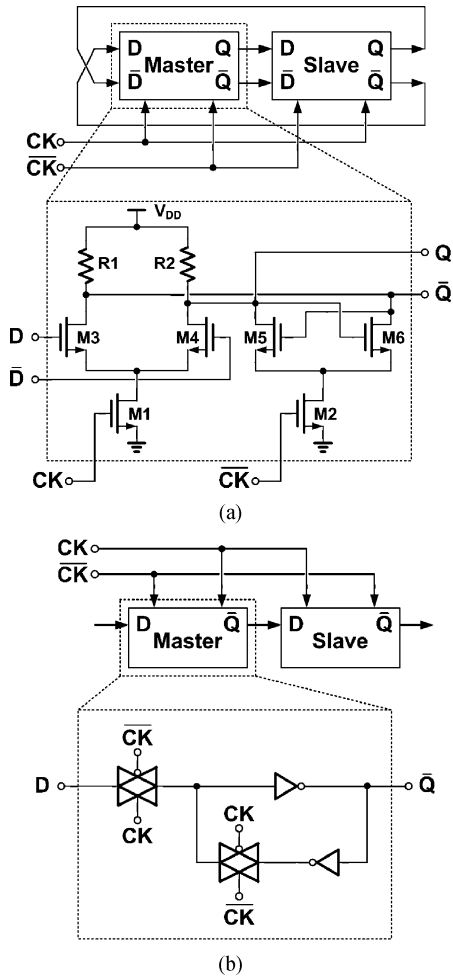


Fig. 7. Simplified schematic of frequency divider. (a) CML static divider. (b) Digital static divider.

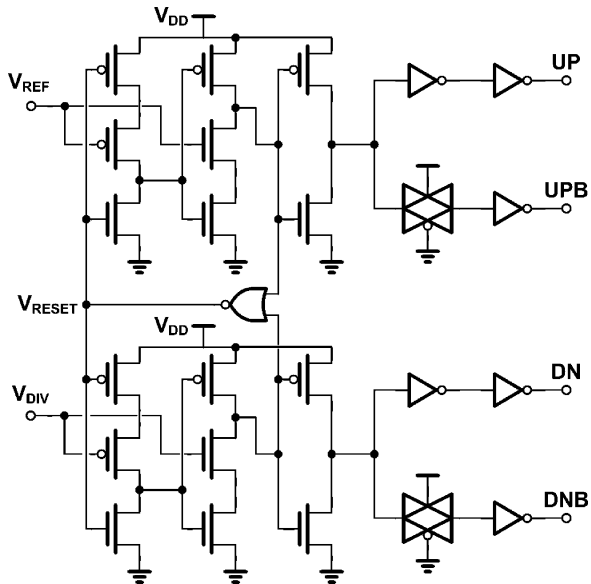


Fig. 8. Simplified schematic of the PFD.

C. PFD, CP, and Loop Filter

The circuit diagram of PFD [18] is shown in Fig. 8. The true single-phase-clock (TSPC) dynamic DFF is used for 100-MHz

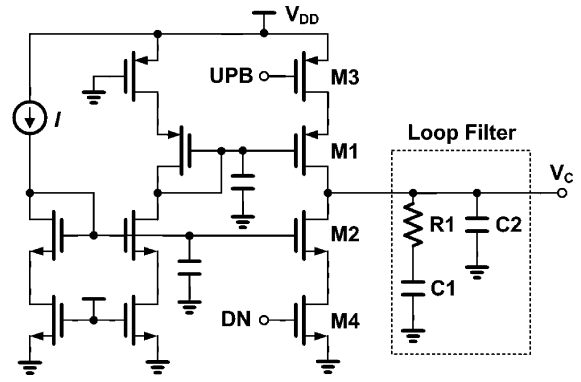


Fig. 9. Circuit diagram of the CP and loop filter.

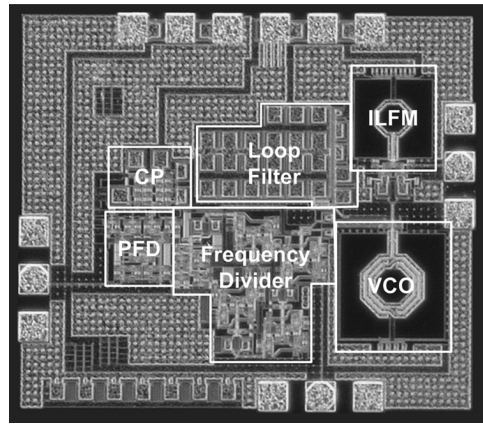


Fig. 10. Chip microphotograph of the proposed PLL.

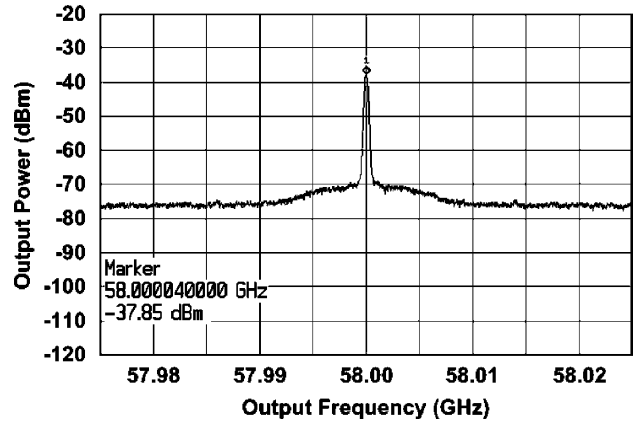


Fig. 11. Output spectrum of the proposed V-band PLL.

frequency operation in the PFD circuit implementation. A slow NOR gate is used to generate the reset signal (V_{RESET}) for reducing the dead-zone problem. Additionally, in order to reduce the skew between the complementary output signals, (UP/UPB) and (DN/DNB), complementary pass-transistor gates are used to match the delay of an inverter in the output of PFD.

The circuit diagram of the CP [19] and loop filter is shown in Fig. 9. A simple current-switched CP is used. Switches M3 and M4 are turned on at every phase comparison and may create the ripple on the control voltage (V_C). M1 and M2 are used to decrease the charge injection and clock feedthrough from M3

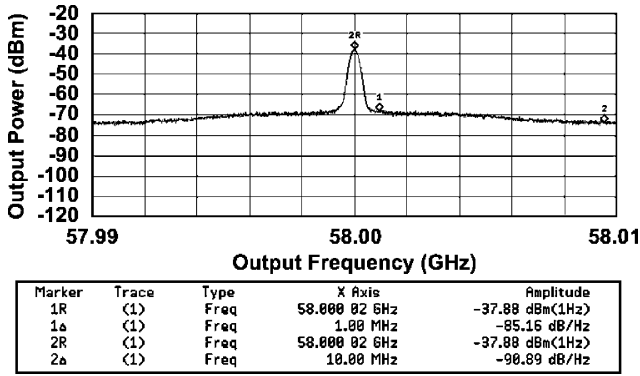
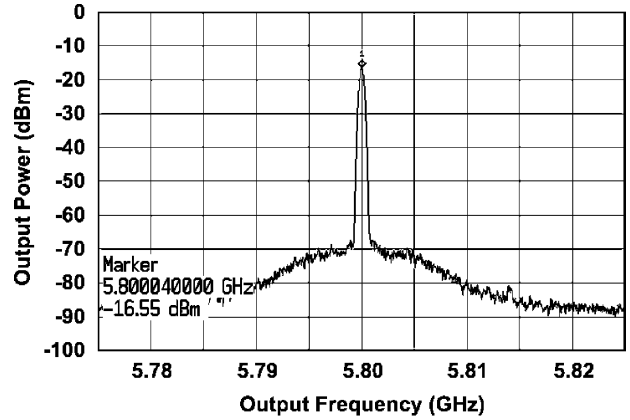
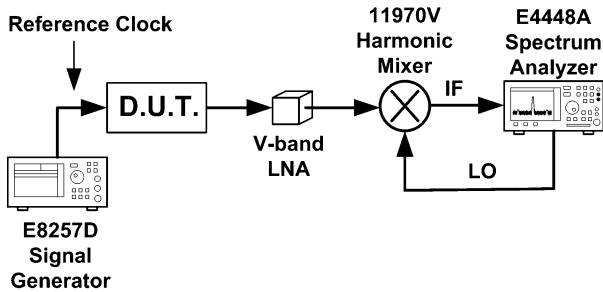


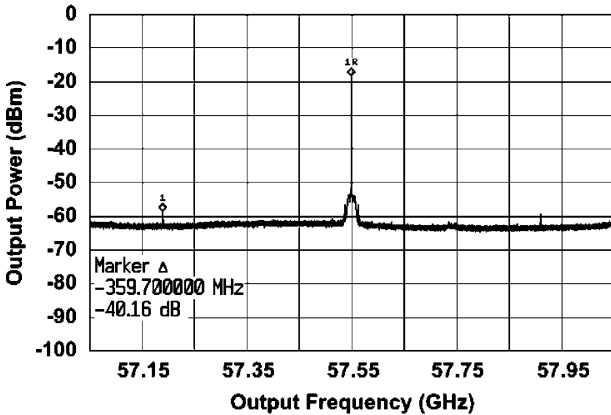
Fig. 12. Measured output phase noise.



(a)



(a)

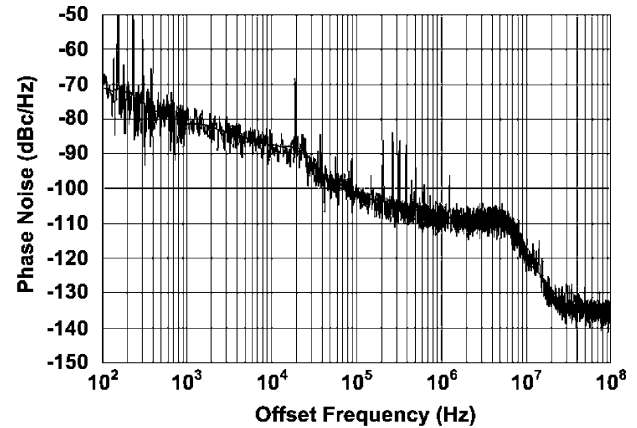


(b)

Fig. 13. (a) Measurement setup for the reference spur testing. (b) Measured reference spur.

and M4 to the output node (V_C) [20]. The small bandwidth of the loop filter is designed to reduce the effect of nonideal property of switches. Since there is no current-matched technique in the CP design, the reference spur is stronger than that with current-matched technique. The simulated charge and discharge current is $50 \mu A$ in this CP design.

In the loop filter design, all the passive components are implemented by the on-chip elements. The vertical metal-insulator-metal capacitors (MIMCaps) are used to realize the capacitors $C1 = 19.98 \text{ pF}$ and $C2 = 2.67 \text{ pF}$ with a reasonable chip area. The resistor $R1 = 11.4 \text{ k}\Omega$ is made of a poly-resistor. Since CP is designed without a current-matched technique, the selective loop bandwidth is only 2 MHz to filter out the nonideal effect of the reference spur.



(b)

Fig. 14. Measured: (a) output spectrum and (b) phase noise of the first divide-by-2 frequency divider.

III. EXPERIMENTAL RESULTS

The proposed V -band PLL is designed and fabricated by using $0.18\text{-}\mu\text{m}$ Al 1P6M standard CMOS technology with an ultra-thick metal of $2 \mu\text{m}$. The chip microphotograph of the proposed PLL is shown in Fig. 10 where the chip area including all the test pads and dummy metal is $0.96 \text{ mm} \times 0.84 \text{ mm}$. An on-wafer measurement system incorporating a probe station, ground-signal-ground (GSG) coplanar probes, and high-speed cables is used to measure chip performance. Since the VCO output load including the ILFM and frequency divider is large, the output signal from the VCO is not directly connected to the testing pad. In order to check the function of the low-frequency PLL, the output signal from the first divide-by-2 divider is connected to the testing pad.

The power consumption of the fabricated V -band PLL is 35.7 mW at a power supply of 1.8 V . The measured output spectrum of the locked ILFM is shown in Fig. 11 where all the losses from the probe, cable, adaptors, and external harmonic mixer have been deembedded. It can be seen from Fig. 11 that the proposed PLL structure provides the output power of -37.85 dBm with the output frequency of 58.0 GHz , which is higher than the transition frequency f_T . The measured total output frequency range of the fabricated PLL is from 53.04 to 58.0 GHz , which is limited by the tuning range of the VCO. The output power

TABLE I
COMPARISON WITH RECENTLY PUBLISHED V-BAND CMOS PLLS.

	Tech.	Frequency range (GHz)	Ref. frequency (MHz)	Phase noise (dBc/Hz)	Reference spur (dBc)	Supply voltage (Volt)	Power consumption (mW)	Chip area (mm \times mm)
This Work	0.18- μm CMOS	53.0 – 58.0	350	-85.2@1 MHz	-40.2	1.8	35.7	0.96 \times 0.84
[1]	0.13- μm CMOS	49.5 – 50.5	50	-72.0@1 MHz	-27 – -40	1.5	57	1.16 \times 0.75
[2] ^a	0.09- μm CMOS	58.0 – 60.4	234	-85.1@1 MHz	-50.5	1.2	80	1.0 \times 0.95
[3]	0.09- μm CMOS	61.1 – 63.1	60	-80.1@1 MHz	-49	1.2	78	1.2 \times 0.7
[6]	0.09- μm CMOS	73.5 \pm 0.32	2340	-88.0 ^b @100 kHz	-72	1.45	88	1.0 \times 0.8

a This work is a frequency synthesizer.

b This value is estimated from divider output.

at 53.04 GHz is about 10 dB lower than that at 58.0 GHz. The output phase noises marked at 1 and 10 MHz are measured as shown in Fig. 12. The measured output phase noises at 1- and 10-MHz offset from the carrier are -85.2 and -90.9 dBc/Hz, respectively.

Due to the large conversion loss from the external harmonic mixer and the small output power from the fabricated chip, the high-resolution setup for the spectrum analyzer is required in the reference spur measurement [6]. To reduce the time cost of the high-resolution setup, a V-band low-noise amplifier (LNA) is added before the external harmonic mixer. The output power to the spectrum analyzer is, therefore, large enough to reduce the resolution requirement. The measurement setup for output reference spur testing is shown in Fig. 13(a). As can be seen from the measurement results in Fig. 13(b), the measured reference spur level is -40.16 dBc. Since the cross-product between output frequency and reference spurs are generated in the non-linear frequency pre-generator stage, the frequency offset between the carrier and the spur tone is, therefore, the same as the reference frequency.

The performance of the first divide-by-2 frequency divider is also measured. The measured output power of -16.55 dBm at 5.8-GHz output frequency is shown in Fig. 14(a). The measured phase noise of the first divide-by-2 frequency divider output from 100 Hz to 100 MHz is shown in Fig. 14(b). The measured output phase noises at 100-kHz, 1-MHz, and 10-MHz offset from the carrier are -102, -108, and -121 dBc/Hz, respectively. The phase noise difference between the ILFM output and the first divide-by-2 frequency divider output at 1-MHz offset is 22.8 dB, which is 2.8 dB higher than the theoretical limit 20 dB ($= 10 \log(10^2)$), as can be seen from Figs. 12 and 14(b).

In Table I, the recently published V-band CMOS PLLs worked at the V-band are compared with the proposed PLL. It can also be seen that the proposed PLL can operate with a lower dc power consumption and a similar phase noise. Moreover, the output frequency range is larger than those in previous works [1]–[3], [6] because the ILFM with a wide operational frequency range is selected. Since the CP is not a current-match structure and larger VCO gain in this work, the reference spur is not as good as in pervious work. Finally, this design is the first CMOS PLL integrated with the ILFM in the millimeter-wave band.

IV. CONCLUSION

The proposed PLL integrated with a novel CMOS ILFM for V-band applications has been designed and fabricated using 0.18- μm standard CMOS technology. The proposed ILFM circuit has been introduced to multiply the frequency five times and successfully co-designed with a low-frequency PLL. As can be seen from the measurement results, the ILFM has great potential in the application of LO signal generators for high-frequency PLL design. In addition, the maximum operational frequency of the frequency divider in a PLL can be reduced to only one-fifth by use of the proposed ILFM. Since it is feasible to design a high-performance VCO at low frequency and to save the large power consumption from full-speed frequency dividers, the proposed PLL structure provides a solution to the low-power and high-performance PLL for V-band applications.

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Chung-Yu Wu (S'76–M'76–SM'96–F'98) was born in 1950. He received the M.S. and Ph.D. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1976 and 1980, respectively.

Since 1980, he has been a Consultant to high-tech industry and research organizations and has built up strong research collaborations with high-tech industries. From 1980 to 1983, he was an Associate Professor with National Chiao Tung University. From 1984 to 1986, he was a Visiting Associate Professor

with the Department of Electrical Engineering, Portland State University, Portland, OR. Since 1987, he has been a Professor with National Chiao Tung University. From 1991 to 1995, he was the Director of the Division of Engineering and Applied Science, National Science Council, Taiwan. From 1996 to 1998, he was the Centennial Honorary Chair Professor with National Chiao Tung University. He is currently the President and Chair Professor of National Chiao Tung University. In Summer 2002, he conducted post-doctoral research with the University of California at Berkeley. He has authored or coauthored over 250 technical papers in international journals and conferences. He holds 19 patents, including nine U.S. patents. His research interests are nanoelectronics, biomedical devices and system, neural vision sensors, RF circuits, and CAD and analysis.

Dr. Wu is a member of Eta Kappa Nu and Phi Tau Phi. He was a recipient of a 1998 IEEE Fellow Award and a 2000 Third Millennium Medal. He has also the recipient of numerous research awards presented by the Ministry of Education, National Science Council (NSC), and professional foundations in Taiwan.



Min-Chiao Chen was born in Miaoli, Taiwan, in 1980. He received the B.S. degree from the Institute of Electronics, Hsinchu, Taiwan, in 2002, and the Ph.D. degree in communication engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2008.

In 2009, he joined the MStar Semiconductor Inc., Hsinchu, Taiwan, as a Design Engineer responsible for RFIC design. His current research interests are the design of CMOS TV tuners and global system for mobile communications (GSM) transceivers.



Yi-Kai Lo received the B.S. and M.S. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2004 and 2006 respectively.

From 2006 to 2007, he was a Research Assistant with the Nanoelectronics and Gigascale Systems Laboratory, National Chiao-Tung University. Since April 2007, he attended compulsory military service with the Ministry of National Defense, Taiwan, as a Corporal of political warfare. He is currently with the Biomimetic System Research Center, National

Chiao-Tung University, where he designs bioelectronics circuits and systems. His research interests focus on RF and mixed-signal integrated circuit design for high-frequency communication systems and medical telemetry radio band applications.