Hardware Design and Implements for WirelessMAN Inner Receiver

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ABSTRACT

IEEE 802.16a is the standard for the wireless metro area connectivity (Wireless MAN). In this thesis, our goal is to develop cost-effective circuitry architecture for the inner receiver system based on the IEEE 802.16a standard. We design an integrated hardware system which contains packet detection, frequency offset estimation, frame synchronization and channel estimation. The hardware architecture is composed of four computation units and a shared memory bank, connected with a data bus. The four computation units are an auto-correlation engine for joined packet-detection /frequency-offset-estimation, a CORDIC (coordinate rotation digital computer) engine for frequency error compensation, a match filter engine for preamble detection, and the circuitry performing maximum likelihood channel estimation. The proposed integrated circuit architecture is area-efficient because of the high reusability of memory modules, which are commonly known to occupy most of the silicon area. Finally, the design is

ported to an Altera FPGA development board. The target system clock rate is running at 56 MHz, which is twice of the sample rate of IEEE 802.16a transmission signal for MMDS.