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碩 士 論 文

使用 CMOS 0.18μm 技術設計一個高整合性多頻帶三角積分調變分數型架構之頻率合成器及一個適用於 802.11a 規格之整數型頻率合成器

The Designs of Highly Integrated Multi-Band ΣΔ Fractional-N Frequency Synthesizer in 0.18μm CMOS and 802.11a Integer-N Frequency Synthesizer

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中 華 民 國 九 十 四 年 六 月

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中文摘要

此篇論文探討了三個電路設計，第一個部份探討高整合性多頻帶三角積分調變分數型頻率合成器電路設計，將 802.11a/b/g 無線網路系統與 GSM/DCS1800 手機系統的頻率合成器，利用 50%除頻方法，將四個系統整合於單晶片中；頻率鎖定時間為 30μs，相位雜訊-114dBc/Hz@1MHz，功率消耗 105mW。第二部份探討 802.11a 整數型頻率合成器之設計，使用 TSMC 0.25μm CMOS 製程，設計一正交信號壓控震盪器，輸出頻率 5.0~5.6GHz，相位雜訊-106Bc/Hz@1MHz。藉由設計吞波計數器（Pulse-Swallow Counter），將除數做程式化控制，除數範圍是 516~534，以達成頻率合成的目的；同時使用 4 階迴路濾波器，鎖定時間 40μs，相位邊際 58 度。第三部份則探討以 8 位元控制壓控震盪器輸出頻率之高解析度 LC 壓控震盪器設計，使用 TSMC 0.18μm CMOS 製程，藉由 8 組變容器，將壓控震盪器的輸出頻率解析度提高，並設計每個變容器的可調頻率範圍約 4.67MHz，壓控震盪器的相位雜訊是-107dBc/Hz@1MHz。利用此電路，在配合高準確性的頻率檢測器，將可達成全數位化高頻頻率合成器之目的，可免去使用外掛的迴路濾波器，提高晶片整合度，並將鎖頻時間加快數倍以上。

The Designs of Highly Integrated Multi-Band ΣΔ Fractional-N Frequency Synthesizer in 0.18μm CMOS and 802.11a Integer-N Frequency Synthesizer

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Abstract

In this thesis, we will discuss three circuit designs. In the first part, a high integration multi-bands ΣΔ fractional-N frequency synthesizer design is discussed. The 802.11a/b/g WLANs and GSM/DCS1800 mobile system frequency synthesizer are integrated in single chip by 50% frequency division technique. Frequency settling is 30μs. Phase Noise is -114dBc/Hz@1MHz. Total power consumption is 105mW. In the second, we discuss an 802.11a integer-N frequency synthesizer design. A quadrature voltage controlled oscillator is designed. The oscillation frequency ranges from 5.0GHz to 5.6GHz. Phase noise is -106Bc/Hz@1MHz. The pulse-swallow counter is used to program division number. Total division number is 516~534. Besides, the 4^{th} order loop filter structure is adopted for low noise consideration. Frequency settling time is 40μs. Phase margin is 58degrees. In the third part, we will discuss a technique to increase voltage controlled oscillator frequency resolution by 8-bit varactors. The average varactor tuning range is designed to be about 4.67MHz. Phase noise is -107dBc/Hz@1MHz. With this high frequency resolution voltage controlled oscillator, and a high precision frequency detector, we can design a new

all-digital frequency synthesizer. In this proposed structure, the loop filter is omitted, and chip integration is promoted. The frequency settling time is faster by several times.

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Chapter 1

Introduction

1.1 Background and Motivation

Modern life is mobile life. Wireless products and mobile phones have changed the communication method of the world. Technology helps people to live in a more convenient life. These benefits should thank a lot to the great improvements in Radio frequency integrated circuits (RFIC). In the past decade, wireless communication has become one of the most attractive industries for many researchers and investors. Mobile phones undoubtedly establish the major market of wireless applications and so will wireless local area network (WLAN) systems do. Both lead a trend for the requirement of highly integration, smaller dimension, lower cost and lower power consumption.

The successful experiences of RFIC system enable researchers to merge more than one application system in a chip. Projects of integrating multi-systems, such as 802.11a/b/g or GSM/GPRS, have proven that combining systems into a single chip is real and will make more economic profits. In this thesis, a design combining 802.11a/b/g and GSM/DCS1800 frequency synthesizer is discussed. This design further increases the possibility of implementing a quad-bands RFIC product. Today, consumers expect a powerful telecommunication product that will make their mobile phones capable of internet ability or notebook with mobile phone ability. With this quad-bands design, this powerful telecommunication product will come into life.

Today, most of the frequency synthesizer components, such as VCO, prescalar, modulator, PFD and charge pump, can be integrated in chip. But there is one

component used to be implemented by microwave components off-chip, the loop filter. Due to large resistance and capacitance value, the loop filter is seldom integrated into chip. In this thesis, I proposed an idea that would not require loop filter in frequency synthesizer. By designed an 8-bit voltage controlled oscillator and used a high sensitive frequency discriminator, the frequency synthesizer is digitally controlled. With this method, the frequency synthesizer is really full integrated on chip, and the locking time is also speeded up by more than ten times.

1.2 Thesis Organization

This thesis discusses a high-integration multi-band ΣΔ fractional-N frequency synthesizer fabricated by TSMC 0.18μm CMOS process and an 802.11a integer-N frequency synthesizer. Finally, propose a new all-digital frequency synthesizer architecture that would not require loop filter.

Chapter 2 introduces a 0.18μm CMOS, high integration frequency synthesizer that use only one voltage controlled oscillator to combined 802.11a/b/g and GSM/DCS1800 frequency synthesizer in single chip.

Chapter 3 introduces a 0.25μm CMOS, 802.11a integer-N frequency synthesizer architecture, building blocks and simulation results.

Chapter 4 introduces a new topology of frequency synthesizer that can omit off-chip loop filter and speeds up locking time. The 8-bit voltage controlled oscillator has been fabricated in TSMC 0.18μm CMOS technology.

Finally, chapter 5 gives the conclusions of the above three circuit designs and future work.

Chapter 2

Highly Integrated Quad-Bands ΣΔ Fractional-N Frequency Synthesizer

System integration is an important trend in modern electronic communication products [1][2][3][4][5][6]. The most famous product is the GSM mobile phone integrated with GPRS function which enables mobile phone the internet function. This is indeed a great idea to make our lives better. Another important integration is the wireless local area network (WLAN) integration. Under this trend, the relationship between notebook and mobile phone gets closer, which means that the mobile system would be eventually integrated with the WLAN system. However, these two main systems differ in too many aspects, such as channel bandwidth, central frequency, data rates, etc.; this integration doesn't come to the market. In this chapter, we will discuss and design an 802.11a/b/g, GSM, DCS1800 quad-bands frequency synthesizer integration using frequency division and fractional-N ΣΔ modulation methods. The chip is fabricated in TSMC 0.18μm CMOS process.

2.1 Background

Multi-bands frequency synthesizer has attracted a lot of attention recently. There are two methods to design this multi-bands circuit: multi-bands VCO, frequency doubling or diving. We will discuss both below.

1. A Single-Chip Quad-Band (850/900/1800/1900MHz) Direct Conversion GSM/GPRS RF Transceiver with Integrated VCOs and Fractional-N Synthesizer [1]

Circuit block diagram is shown in Fig.2-1.The voltage controlled oscillator is designed to oscillate between 1245MHz to 1650MHz. The voltage controlled oscillator output signals first pass a buffer amplifier. Then signals will proceed by divide-by-3 and multiply-by-2 circuit to generate triple-bands signals. Circuit performances are summarized in Tab.1. The multi-bands signals generation method is very similar to this thesis.

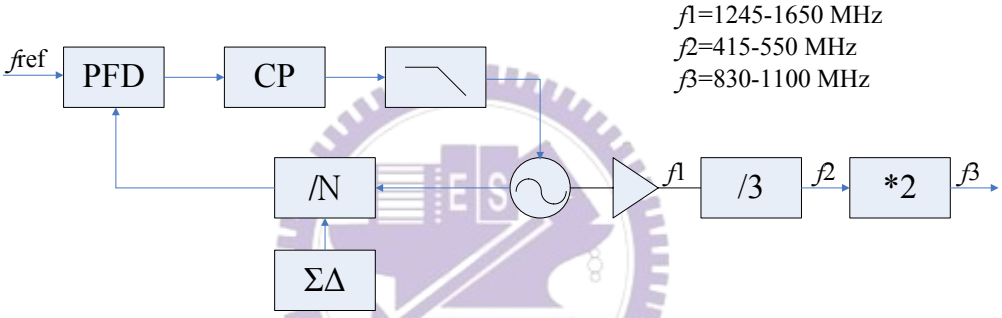


Fig.2-1 Quad-Bands (850/900/1800/1900MHz) frequency synthesizer block diagram

Tab.1 Quad-bands (850/900/1800/1900MHz) frequency synthesizer performances summary

Parameter	**Performance**
Tuning Range	1250~1650MHz
Frequency Resolution	3Hz
Locking Time（<100ppm）	175μs
Phase Noise @100KHz	-106dBc/Hz
Phase Noise @400KHz	-124dBc/Hz
Phase Noise @3MHz	-141dBc/Hz
Biasing Currrent	28mA

2. A △Σ Fractional-N Frequency Synthesizer with Multi-Band PMOS VCOs for 2.4 and 5GHz WLAN Applications [3]

Circuit block diagram is shown in Fig.2-2. Design two voltage controlled oscillator (2.4GHz, 5GHz). By switching these two oscillators, we can attain dual-bands frequency synthesizer design. Because two oscillators are required, the chip dimension is much larger than the former, but the dual-bands signals have greater output power due to directly output from oscillator. The circuit performances are summarized in Tab.2.

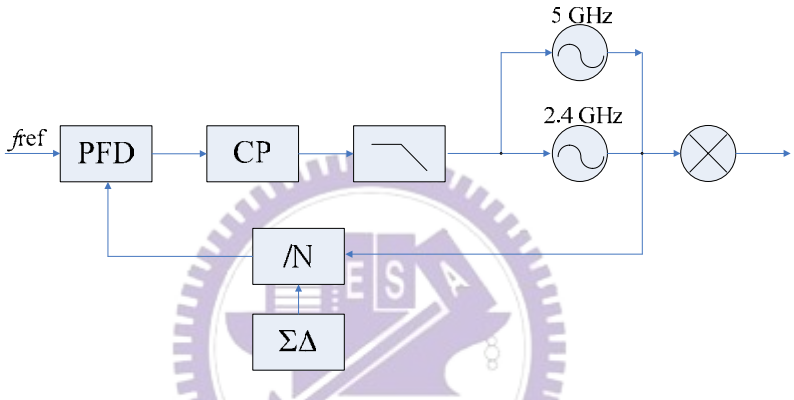


Fig.2-2 Dual-bands (2.4GHz, 5GHz) frequency synthesizer block diagram

Tab.2 Dual-bands (2.4GHz, 5GHz) frequency synthesizer performances summary

Parameter	**Performance**
High Frequency Tuning Range	4.93~5.35GHz
Middle Frequency Tuning Range	4.47~4.91GHz
Low Frequency Tuning Range	3.52~3.87GHz
Phase Noise	-120dBc/Hz @1MHz
In Band Noise	-93dBC/Hz
Loop Corner Frequency	150KHz
Reference Frequency	40MHz
Channel Resolution	1MHz
Reference Spur Noise	-56dBc
Supply Voltage	2.75V
Bias Current	84mA

2.2 System Integration

2.2.1 System Specifications

In this chapter, we try to integrate 802.11a/b/g and GSM/CS1800 frequency synthesizer. Three system specifications that frequency synthesizer concerned about are frequency band, channel bandwidth and phase noise. They are listed in Tab.3 (a).

Tab.3 (a) Each System specifications

Application	Frequency Band		Channel Bandwidth	Phase Noise (dBc/Hz)
	TX	RX		
802.11a	5.15~5.35 GHz		20 MHz	-110@1MHz
802.11b/g	2400~2483 MHz		10 MHz	-110@1MHz
DCS1800	1710~1785 MHz	1805~1880 MHz	200 KHz	-116@600KHz
GSM900	890~915 MHz	935~960 MHz	200 KHz	-121@600KHz

In order to generate quad-bands signals, we adopt frequency division method. The 802.11a signal is outputted directly from the voltage controlled oscillator. 802.11b/g signal is outputted from a divide-by-2 circuit. DCS1800 signal is outputted from a 50% divide-by-3 circuit. GSM signal is outputted from a 50% divide-by-6 circuit. The specifications of each application after integration are summarized in Tab.3 (b).

Tab.3 (b) System specifications after integrating to 5GHz

Application	Frequency Band		Channel Bandwidth	Phase Noise (dBc/Hz)
	TX	RX		
802.11a	5.15~5.35 GHz		20 MHz	-110@1MHz
802.11b/g	4.80~4.97 GHz		10 MHz	-110@2MHz
DCS1800	5.130~5.355 GHz	5.415~5.640 GHz	600 KHz	-116@1.8MHz
GSM900	5.340~5.490 GHz	5.610~5.760 GHz	1200 KHz	-121@3.6MHz

2.2.2 Phase Noise Considerations

In a perfect frequency divider, signal phase noise after division will be improved as described in Fig.2-3. Based on the frequency division theory, signal skirt would be narrower after division. If the divider is well-designed, signal phase noise will get about 6dB better from a divide-by-2 circuit and 9dB better from a divide-by-3 circuit. In this chapter, the voltage controlled oscillator phase noise simulation results is shown in Fig.2-4. By the perfect divider theorem and the phase noise simulation result, we can expect the quad-bands signal phase noise performance would meet the system specification, summarized in Tab.4. From the above comparison, we can conclude that designing oscillator at higher frequency then scaled the frequency down is a good choice. The chip dimension could be smaller because the inductance is smaller than lower frequency. Besides that, circuit phase noise performance will also satisfy the system specification.

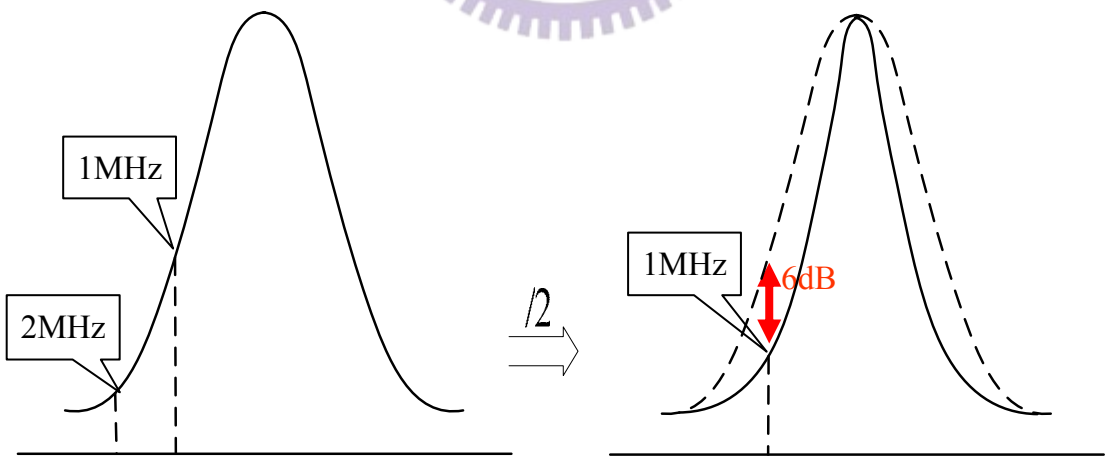


Fig.2-3 Signal spectrum description after division

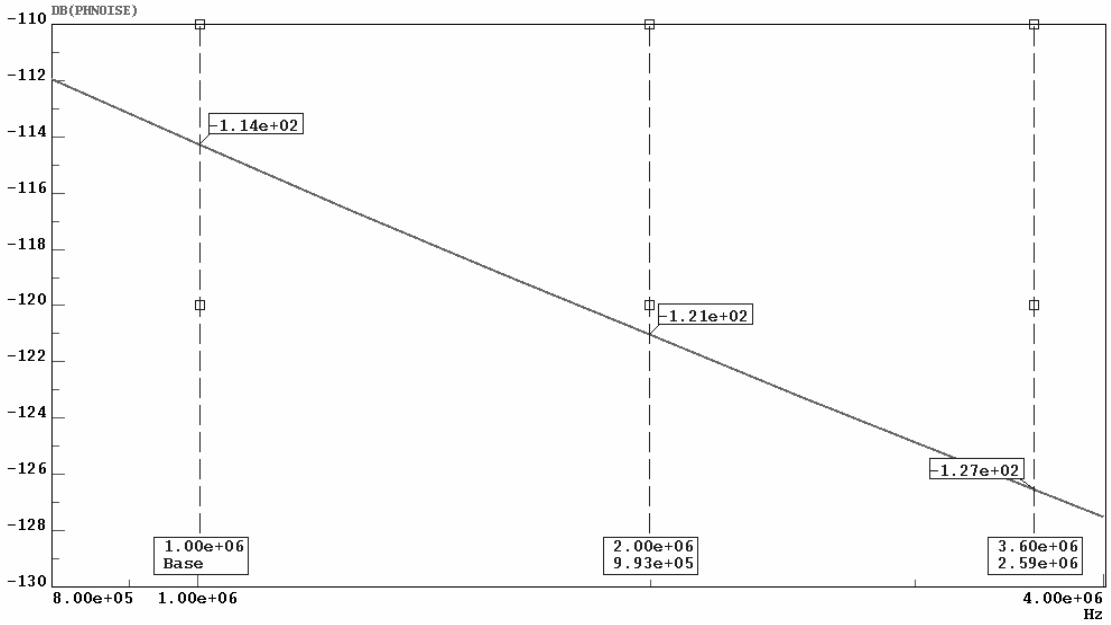


Fig.2-4 Voltage controlled oscillator phase noise simulation results

Tab.4 Phase noise comparison, system specifications vs. simulation

Application	**System Spec.**	**Simulation**
802.11a	-110 dBc/Hz @1MHz	-114 dBc/Hz @1MHz
802.11b/g	-110 dBc/Hz @1MHz	-121 dBc/Hz @1MHz
DCS1800	-116 dBc/Hz @600KHz	-120 dBc/Hz @600KHz
GSM	-121 dBc/Hz @600KHz	-127 dBc/Hz @600KHz

2.2.3 Frequency Considerations and Channel Code Allocations

From Tab.3 (b), the tuning range of voltage controlled oscillator (VCO) must cover from 4.8GHz to 5.8GHz. The tuning range of voltage controlled oscillator is about 20%, which will make system unstable because the oscillator is too sensitive. In

this thesis, we separate this 1GHz tuning range into 6 sections by designing 3 varactors in the voltage controlled oscillator. Tab.5 shows the frequency bands of each application after integrating to 5GHz vs. VCO varactor bank codes allocation. Since these varactors determine the oscillation frequency, they are the most important factor about the success of this quad-bands frequency synthesizer. The tuning range of VCO is shown in Fig.2-5.

Tab.5 System frequency bands after integration vs. varactor bank

Application	**Frequency Bands After Integration**	**Varactor Bank Code**
802.11a	5.15~5.35 GHz	3
802.11b/g	4.80~4.97 GHz	2
DCS1800	TX：5.130~5.355 GHz RX：5.415~5.640 GHz	3、5
GSM900	TX：5.340~5.490 GHz RX：5.610~5.760 GHz	4、6

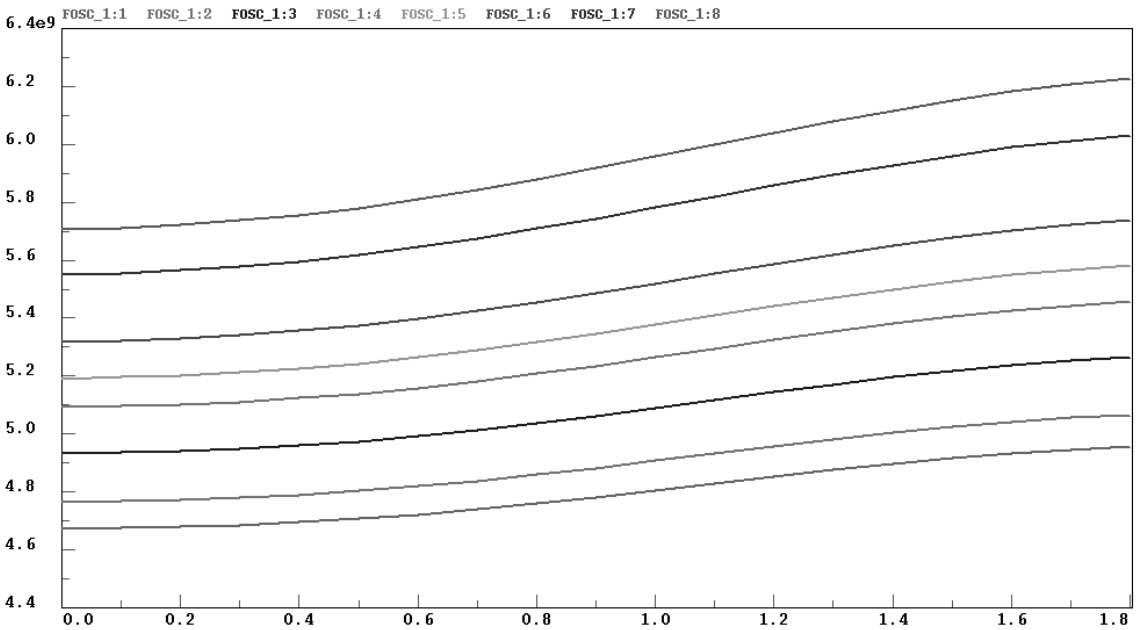


Fig.2-5 VCO each bank codes tuning range simulation results

2.3 Quad-Bands Frequency Synthesizer Architecture

Consider that 802.11a/b/g channel bandwidth (20MHz) is much larger than GSM/DCS1800 (200 KHz) system; we decided to separate these two systems into two paths. Circuit block diagram is shown in Fig.2-6. By design two ΣΔ modulators and use a switch, we can implement a quad-bands frequency synthesizer. But a problem exists in this architecture: because the 1.8GHz divider is connected to a 1.8GHz output buffer amplifier and a divide-by-2 circuit, the loading effect may cause the 50% divide-by-3 circuit malfunction!

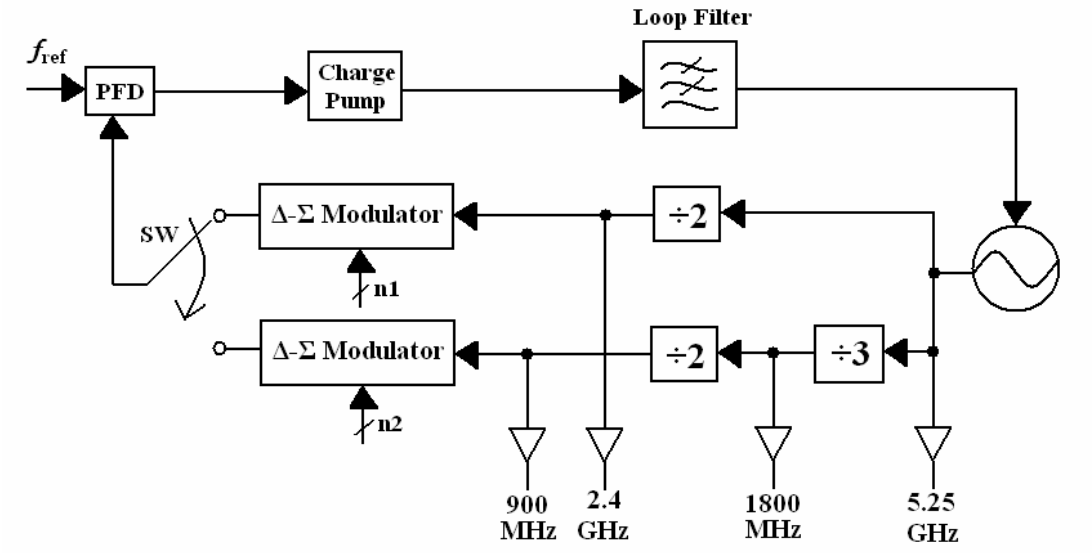


Fig.2-6 Quad-bands frequency synthesizer architecture

In order to make system more stable, we must minimize the loading effects of the 50% divide-by-3 circuit. We modified the quad-bands frequency synthesizer architecture as in Fig.2-7. Reader may find out that the 50% divide-by-3 circuit doesn't connect to divide-by-2 circuit anymore, thus the loading effect is lessened and system becomes more stable. Although 802.11a/b/g channel bandwidth differs from GSM/DCS1800 a lot, we can use the fine resolution ΣΔ modulator of GSM/DCS1800

to replace the coarse resolution of 802.11a/b/g ΣΔ modulator. The architecture of Fig.2-7 is single path architecture, so that the integration of system is improved. To attain fine resolution of GSM/DCS1800, the ΣΔ modulator is composed of 12-bit accumulator. The reference frequency is chosen to be 16MHz under the tradeoff of spur noise suppression and fast settling time.

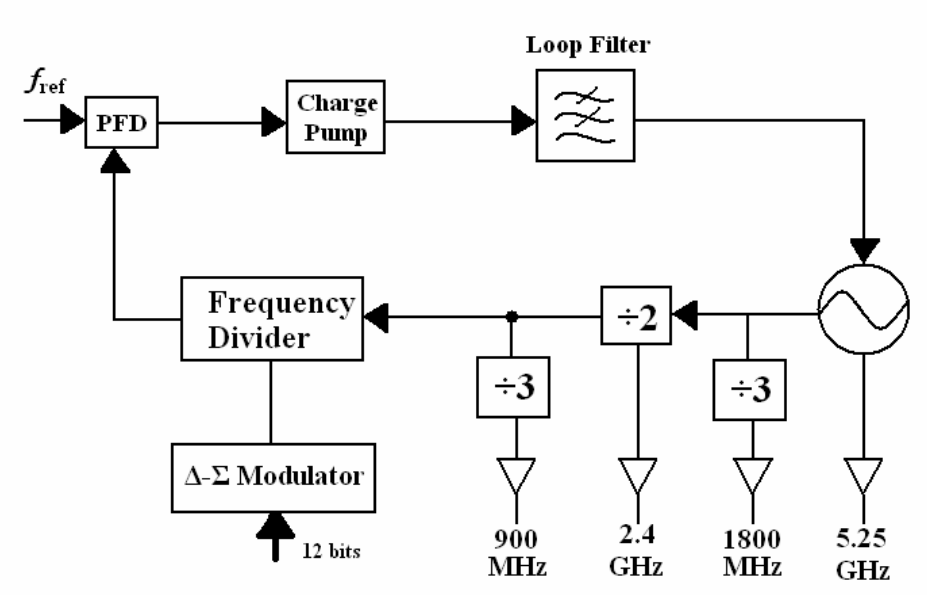


Fig.2-7 Modified quad-bands frequency synthesizer architecture

2.4 50% Divide by 3 Circuit [1][8]

Traditional frequency divider is based on positive edge trigger or negative edge trigger architecture, thus output signal has even period of input signal. To design a 50% divide-by-odd circuit, the trigger structure should be modified. Based on this idea, we should design a new DFF that has a new control signal: θ, to change the DFF trigger mechanism. When θ=H, circuit is positive edge trigger. When θ=L, circuit is negative edge trigger. The structure of this new DFF is shown in Fig.2-8.

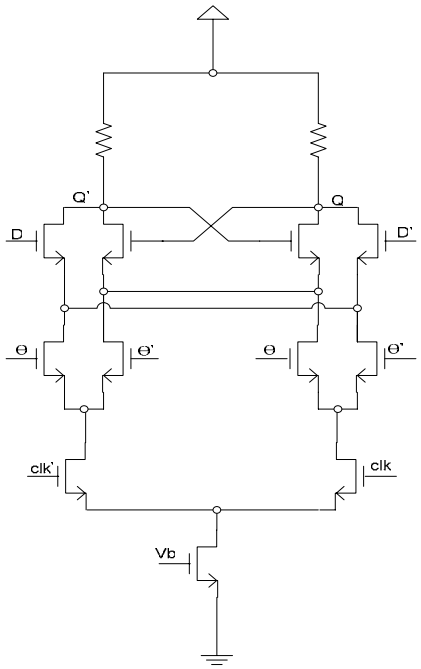


Fig.2-8 Trigger mechanism changeable DFF structure

By cascading N-stages DFF, we can design 50% divide-by-N circuit, no matter N is odd or even. In this thesis, we cascade 3-stage DFF, and let neighboring stage differ by 60 degrees. Timing diagram is shown in Fig.2-9.

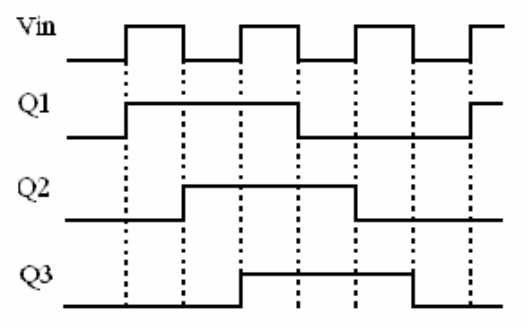


Fig.2-9 Timing diagram of 50% divide-by-3 circuit

Observing the control signals of each DFF, we summary the control signals below:

D1/θ1	D2/θ2	D3/θ3
Q3'/Q2	Q1/Q3'	Q2/Q1'

After we derived out each DFF control signals, the complete 50% divide-by-3 circuit is shown in Fig.2-10.

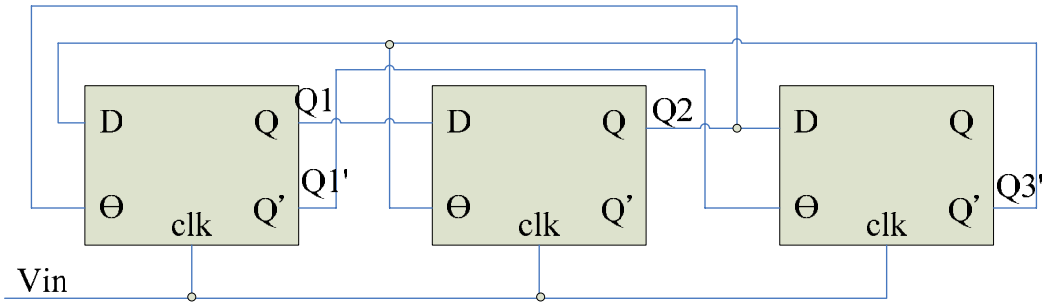


Fig.2-10 Complete divide-by-3 circuit structure

Fig.2-11 shows the simulation result of inputting 5.8GHz, amplitude 100mV sine wave to divide-by-3 circuit. The operation frequency of this circuit is 5-6GHz; minimum acceptable signal amplitude is 80mV which is quite satisfaction to this quad-bands frequency synthesizer design.

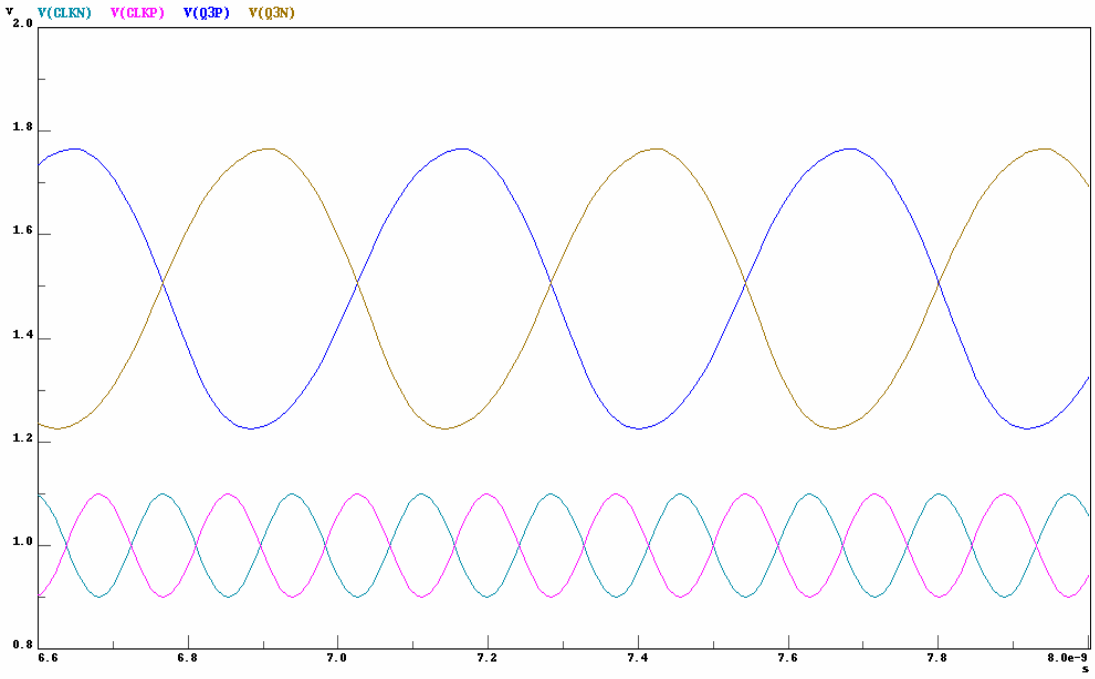


Fig.2-11 Input 5.8GHz, 100mV amplitude signal simulation result

2.5 3rd ΣΔ Modulator [9][10][11][12]

Because the channel bandwidth of GSM/DCS1800 is quite narrow, we use fractional-N structure in this quad-bands frequency synthesizer for faster settling without scarifying frequency resolution. Fractional-N architecture is based on accumulator carrier to control fraction division. Unfortunately, the carrier signal is a periodic signal which will cause intolerant spur noise close to signal wanted. To suppress the spur noise, we use a ΣΔ modulator to modulate the carrier signal.

The mono-type of ΣΔ modulator is shown in Fig.2-12. The ΣΔ modulator is composed of an integrator and a differentiator. After the differentiator, the quantization noise has been suppressed. The practical 1st ΣΔ modulator is shown in Fig.2-13. It explains that after a ΣΔ modulator, the quantization noise will be shaped by $(1-Z^{-1})$. Some modification has been made to simplify the 1st ΣΔ modulator. Fig.2-14 shows a modified 1st ΣΔ modulator structure. In Fig.2-14, 1st ΣΔ modulator is accomplished by an accumulator.

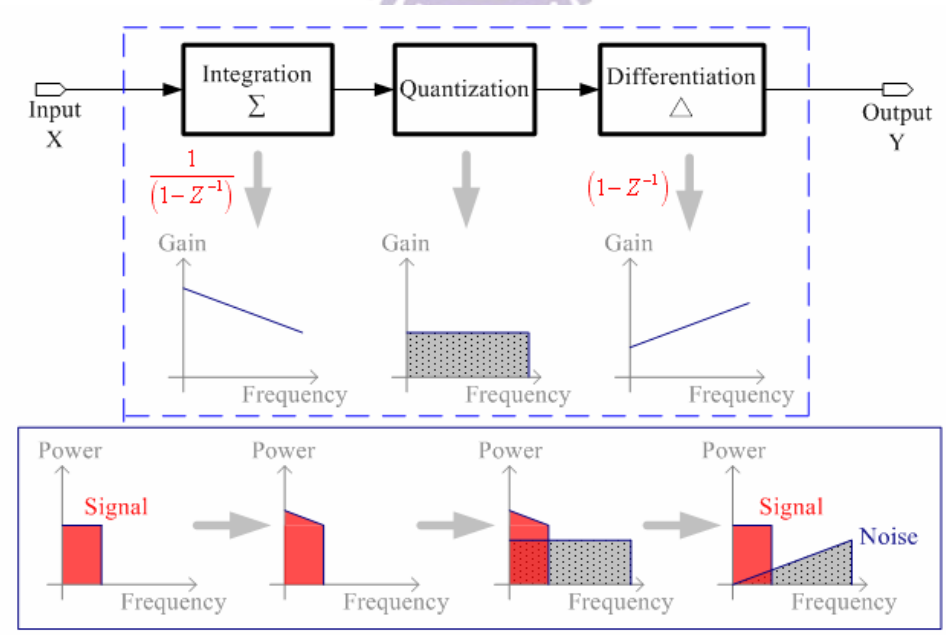
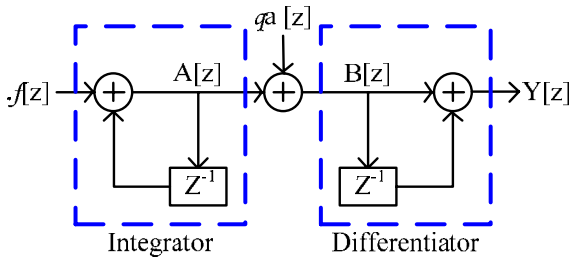


Fig.2-12 ΣΔ modulator Mono-type

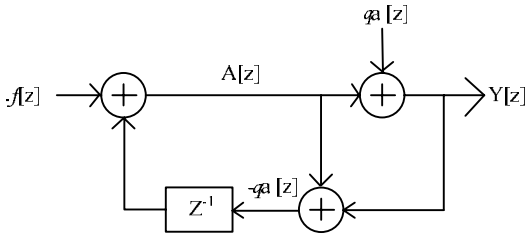


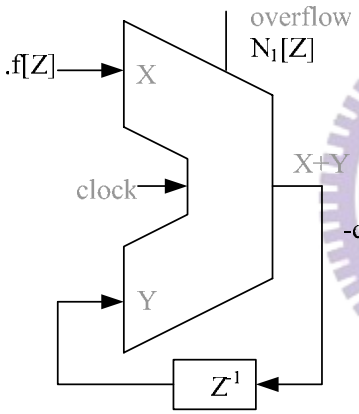
$$A[Z]=\frac{1}{1-Z^{-1}}.f[Z]$$

$$B[Z]=A[Z]+qa[Z]=\frac{1}{1-Z^{-1}}.f[Z]+qa[Z]$$

$$Y=.f[Z]+qa[Z](1-Z^{-1})$$

Fig.2-13 Basic type of ΣΔ modulator





$$A[Z]=.f[Z]-qa[Z](Z^{-1})$$

$$Y[Z]=A[Z]+qa[Z]=.f[Z]+qa[Z](1-Z^{-1})$$

Fig.2-14 Modified 1st ΣΔ modulator

In order to transform more quantization noise to high frequency, we decide to use 3rd ΣΔ modulator. The 3rd ΣΔ modulator structure is shown in Fig.2-15. The output signal is: $N[Z]=.f[Z]+(1-z^{-1})^3\times q_a[Z]$, which means that quantization noise, quantization noise, $q_a[Z]$, has been shaped to $q_e[Z]=(1-z^{-1})^3\times q_a[Z]$. The noise transfer function therefore is:

$$H_{noise}(f)=\left(1-z^{-1}\right)^3$$

$$H_{noise}(f)=\left|1-\exp\left(-\frac{j2\pi f}{f_{ref}}\right)\right|^3$$

$$H_{noise}(f)=\left|1-\cos\left(\frac{j2\pi f}{f_{ref}}\right)-j\cdot\sin\left(\frac{j2\pi f}{f_{ref}}\right)\right|^3$$

$$H_{noise}(f)=\left|2\cdot\sin\left(\frac{\pi f}{f_{ref}}\right)\right|^3$$

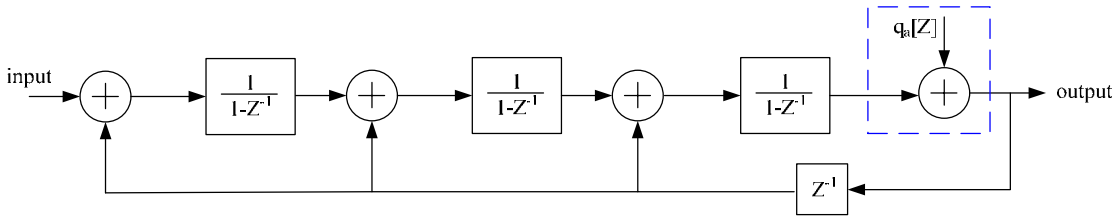


Fig.2-15 3rd ΣΔ modulator

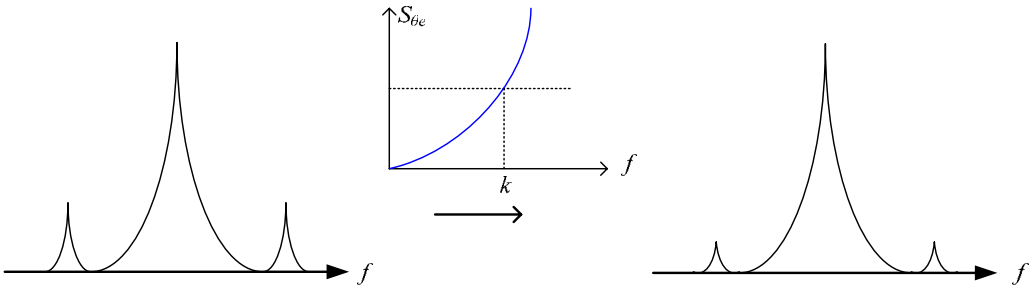
Assume power spectral density of quantization noise is $S_{q_a}(f)=\frac{1}{12\cdot f_{ref}}$. The output phase mismatch power spectra density would be:

$$S_{\theta_e}(f)=\left(\frac{f_{div}}{f\times N_T}\right)^2\times\left\{\frac{1}{12\cdot f_{ref}}\cdot\left[2\cdot\sin\left(\frac{\pi f}{f_{ref}}\right)\right]^6\right\}=\frac{16\cdot f_{ref}}{3\cdot\left(N_T\cdot f\right)^2}\sin^6\left(\frac{\pi f}{f_{ref}}\right)$$

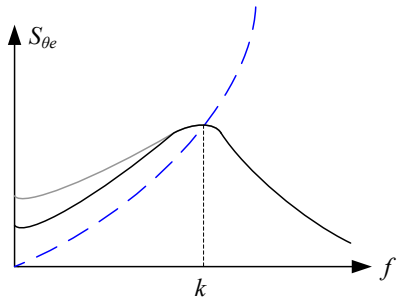
When close to center frequency, the phase mismatch power spectra density is:

$$S_{\theta_e}(f)\simeq\frac{16\cdot f_{ref}}{3\cdot\left(N_T\cdot f\right)^2}\cdot\left(\frac{\pi f}{f_{ref}}\right)6=\frac{16\cdot\pi^6\cdot f^4}{3\cdot {N_T}^2\cdot f_{ref}^5}$$

The spectrum is shown in Fig.2-16, which shows that quantization noise has been efficiently suppressed.



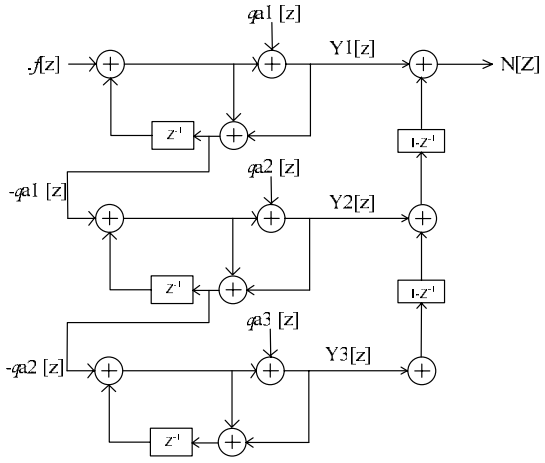
(a)



(b)

Fig.2-16 (a) Noise shaping of 3rd ΣΔ modulator (b) Suppression of 3rd ΣΔ modulator to in-band quantization noise

In this thesis, we adopt MASH-1-1-1 3rd ΣΔ modulator. The integrators of Fig.2-15 are replaced by 1st ΣΔ modulator to make system more stable. The complete structure is shown in Fig.2-17. Practical 3rd ΣΔ modulator structure is also shown in Fig.2-18, which uses accumulators to replace integrators.



$$Y1[Z] = .f[Z] + qa1[Z](1 - Z^{-1})$$
$$Y2[Z] = -qa1[Z] + qa2[Z](1 - Z^{-1})$$
$$Y3[Z] = -qa2[Z] + qa3[Z](1 - Z^{-1})$$

$$\rightarrow N[Z] = .f[Z] + qa3[Z](1 - Z^{-1})^3$$

Fig.2-17 3rd ΣΔ modulator

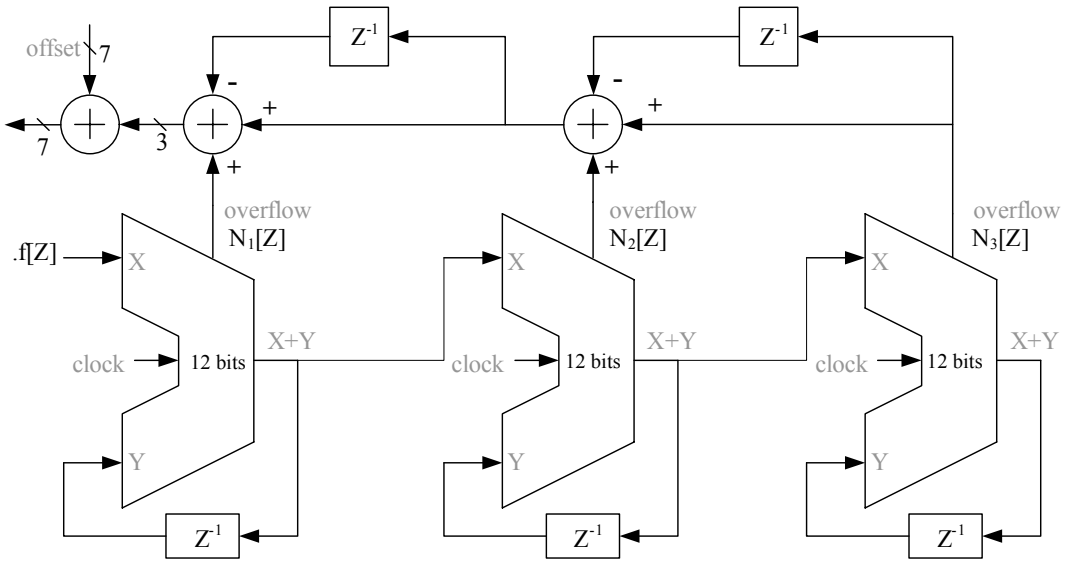


Fig.2-18 Practical 3rd ΣΔ modulator architecture

The 3rd ΣΔ modulator architecture is shown in Fig.2-14. To attain the 200 KHz frequency resolution of GSM/DCS1800 system, the accumulator is based on 12-bit. Since the reference frequency is 16MHz, the frequency resolution of each system is:

Application	Frequency Resolution
802.11a	$16M \div 2^{12} = 3.9$ KHz
802.11b/g	$16M \div 2^{11} = 7.8$KHz
DCS1800	$16M \div 2^{12} * 3 = 11.7$ KHz
GSM	$16M \div 2^{12} * 6 = 23.4$ KHz

The frequency resolution could be further increases by increasing the accumulator bits. Since the accumulator is a cascaded structure, signal delay is very critical in this design.

2.6 Whole System Simulation Results

2.6.1 5.18GHz Simulation Results

Use ELDO simulation tool to simulate circuit close-loop behavior. The 5.18GHz locking curve of VCO control voltage is shown in Fig.2-19. System enters locking state in 15μs, and stable locking in 30μs. Buffer output signal is shown in Fig.2-20. Signal swing is 520mV. Then apply FFT function to Fig.2-20, result shown in Fig.2-21. Fig.2-21 shows that circuit is locked at 5.18GHz and output power is -12.4dBm.

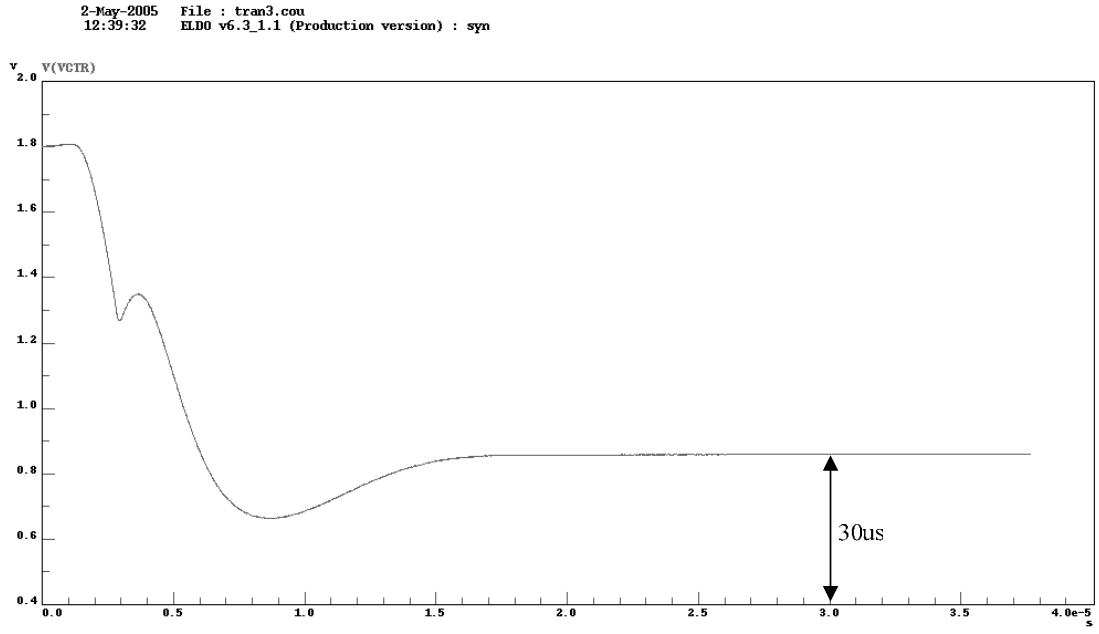


Fig.2-19 Transient curve of VCO control voltage

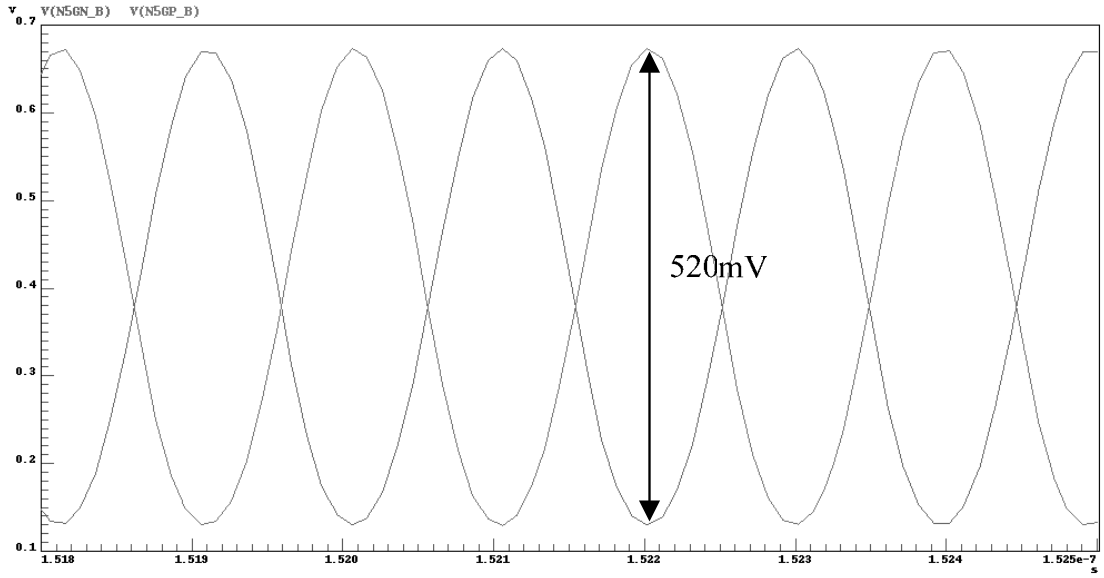


Fig.2-20 Buffer output signal transient analysis

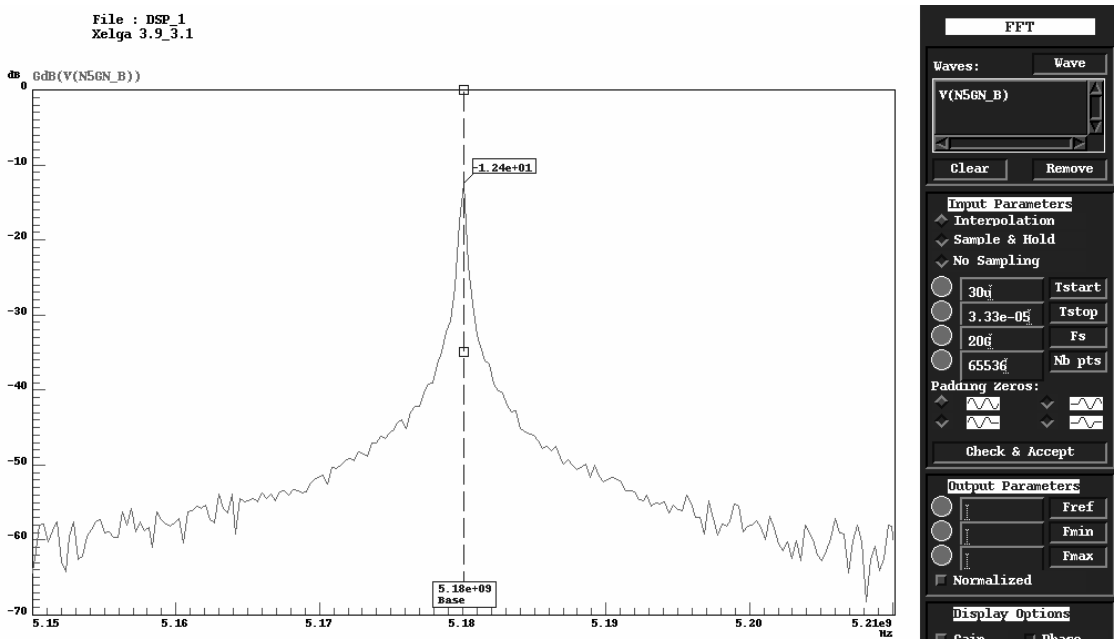


Fig.2-21 5.18GHz FFT simulation result

2.6.2 2.401GHz Simulation Results

The 2.401GHz locking curve of VCO control voltage is shown in Fig.2-22. System enters locking state in 15μs, and stable locking in 30μs. Buffer output signal is

shown in Fig.2-23. Signal swing is 250mV. Then apply FFT function to Fig.2-23, result shown in Fig.2-24. Fig.2-24 shows that circuit is locked at 2.401GHz and output power is -21.5dBm.

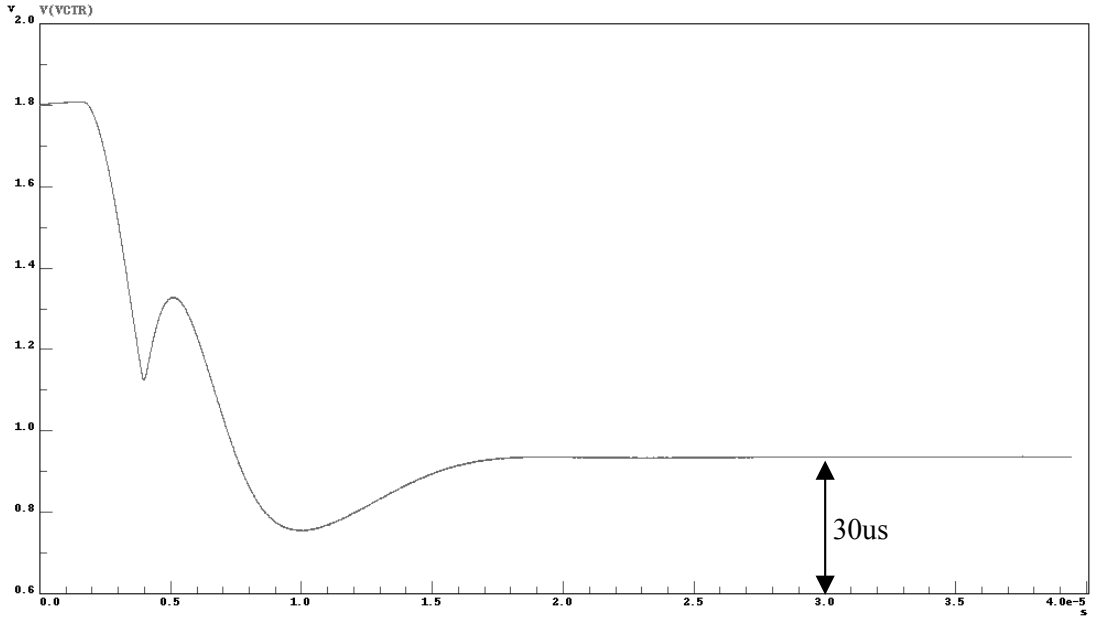


Fig.2-22 Transient curve of VCO control voltage

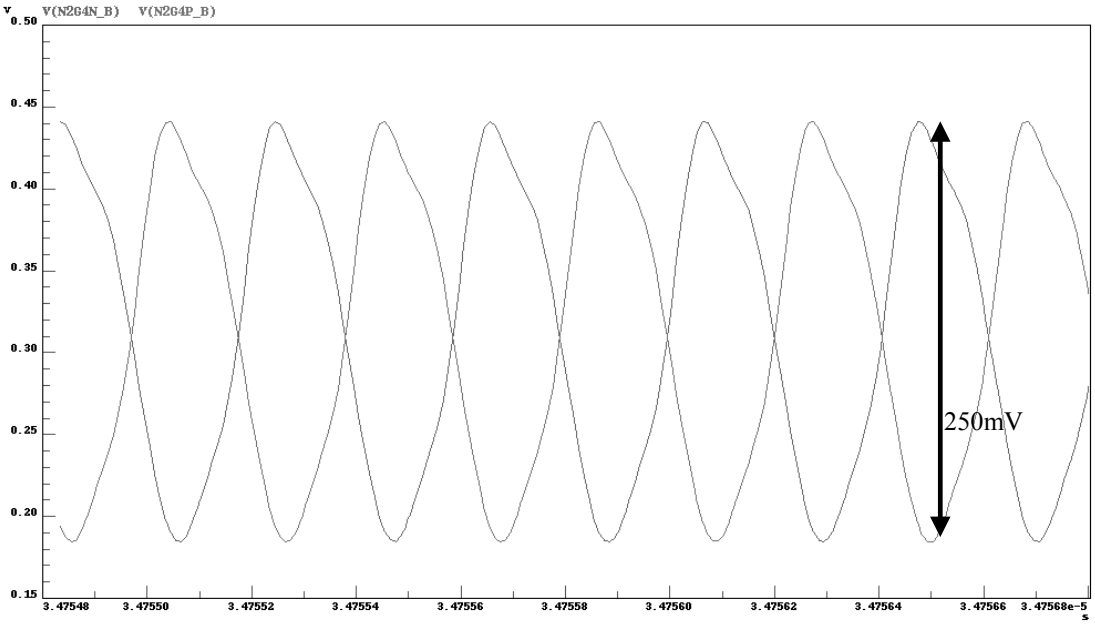


Fig.2-23 Buffer output signal transient analysis

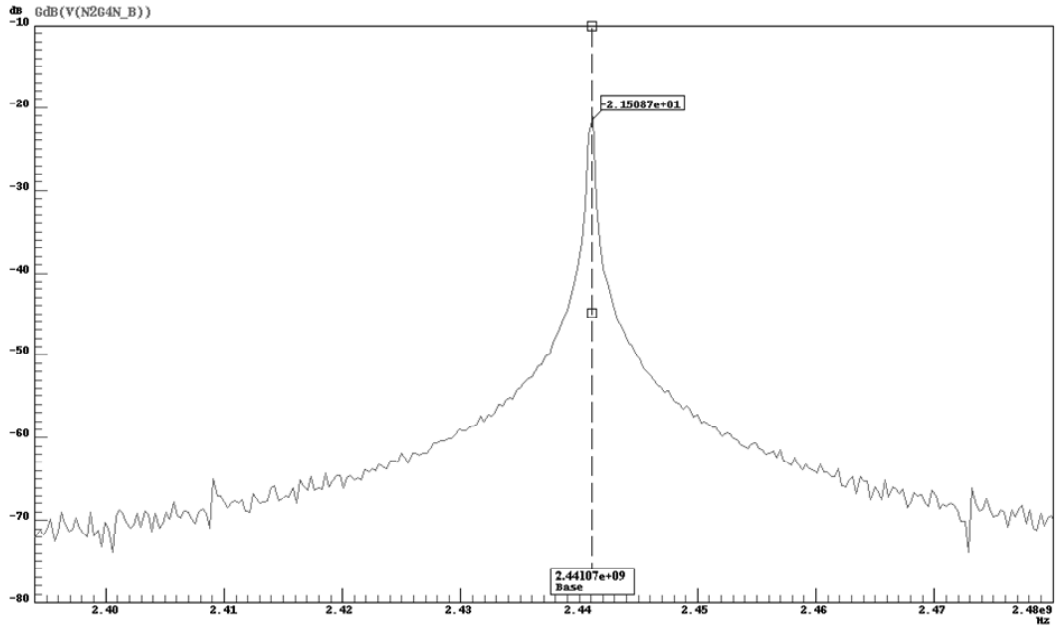


Fig.2-24 2.401GHz FFT simulation result

2.6.3 1.726GHz Simulation Results

The 1.726GHz locking curve of control voltage of VCO is shown in Fig.2-25. System enters locking state in 15μs, and stable locking in 30μs. Buffer output signal is shown in Fig.2-26. Signal swing is 260mV. Then apply FFT function to Fig.2-26, result shown in Fig.2-27. Fig.2-27 shows that circuit is locked at 1.726GHz and output power is -17.2dBm.

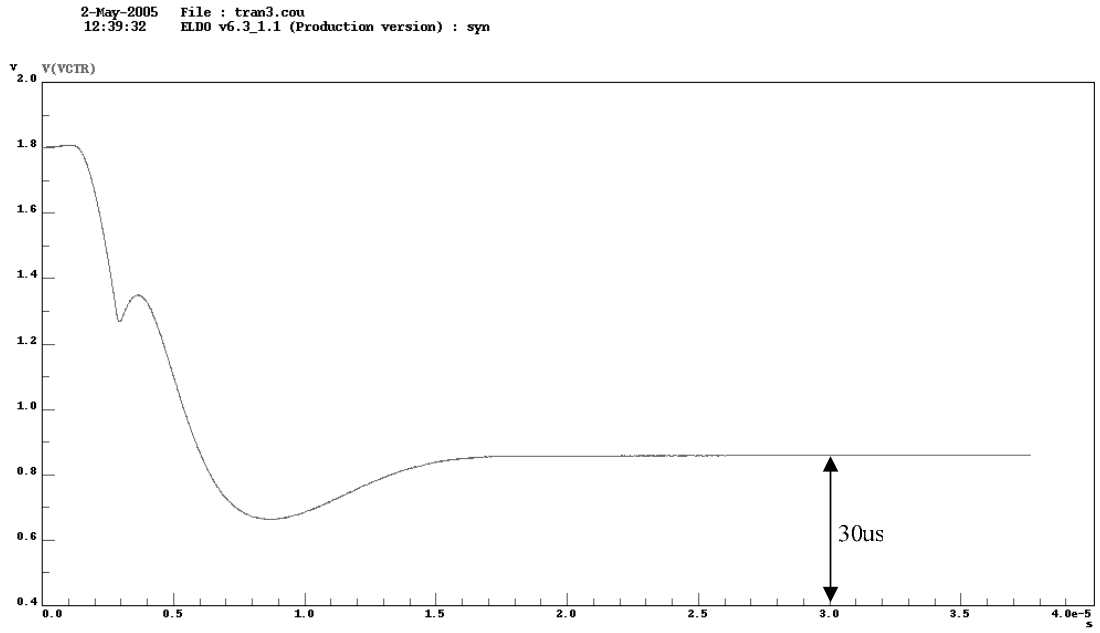


Fig.2-25 Transient curve of VCO control voltage

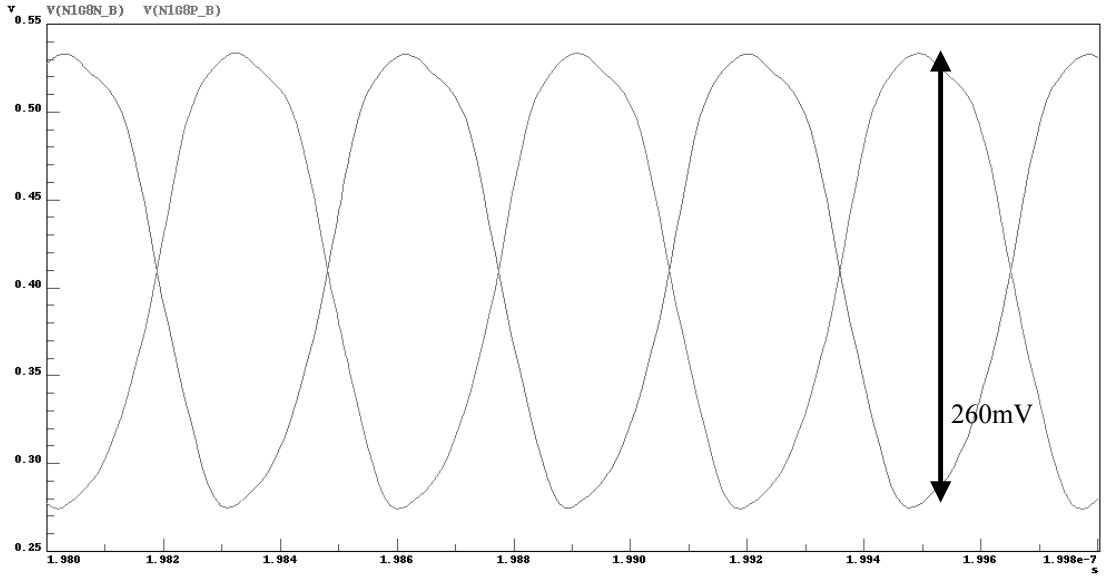


Fig.2-26 Buffer output signal transient analysis

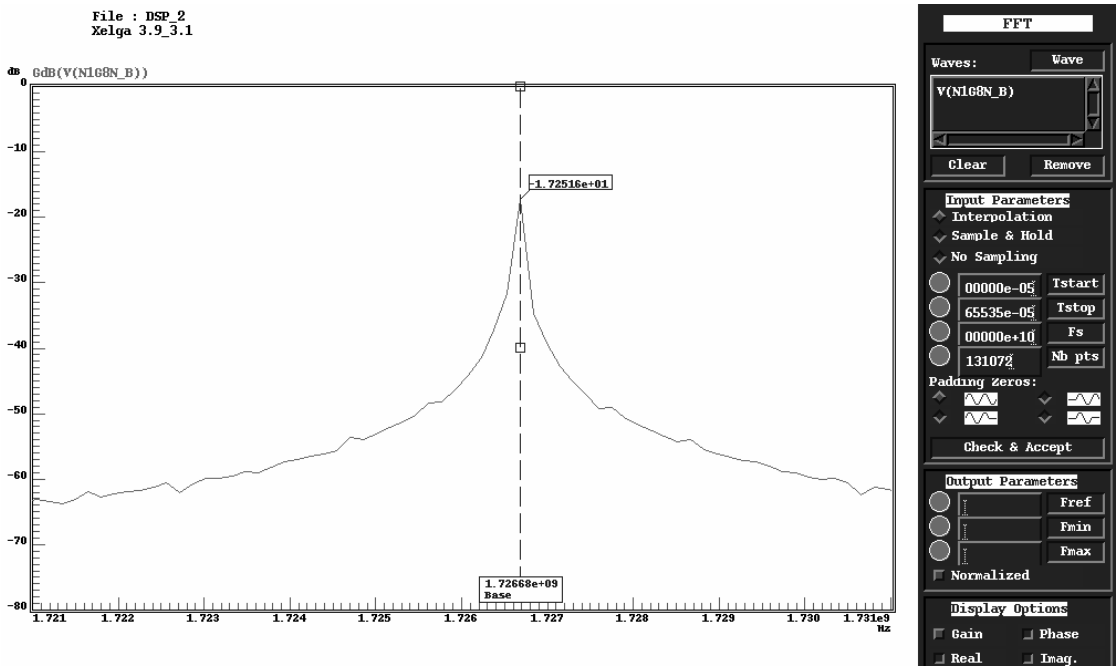


Fig.2-27 1.726GHz FFT simulation result

2.6.4 900.2MHz Simulation Results

The 900.2MHz locking curve of control voltage of VCO is shown in Fig.2-28. System enters locking state in 15μs, and stable locking in 30μs. Buffer output signal is shown in Fig.2-29. Signal swing is 150mV. Then apply FFT function to Fig.2-29, result shown in Fig.2-30. Fig.2-30 shows that circuit is locked at 900.2MHz and output power is -22.1dBm.

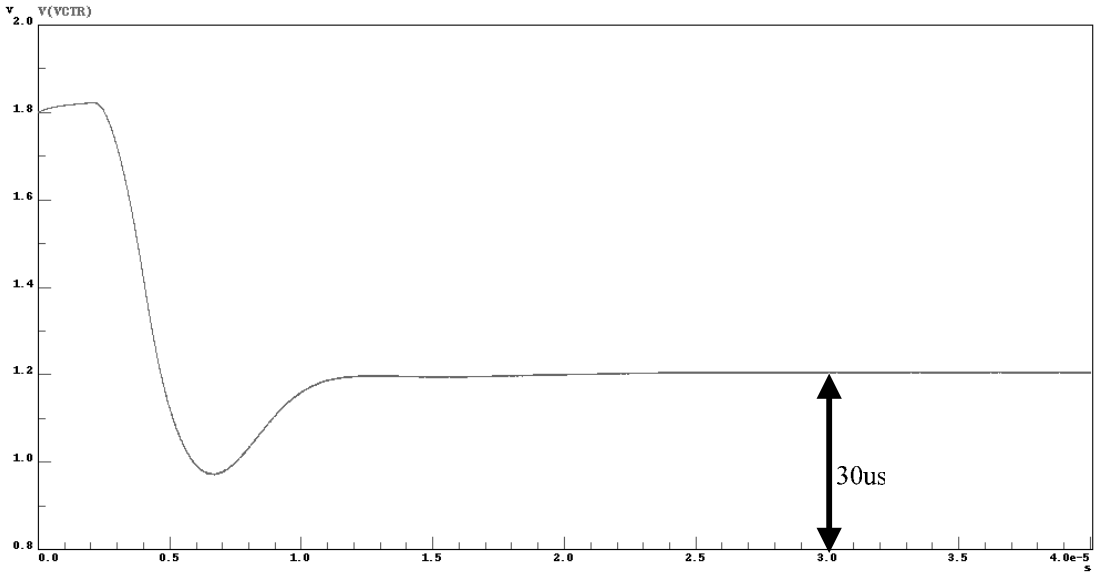


Fig.2-28 Transient curve of VCO control voltage

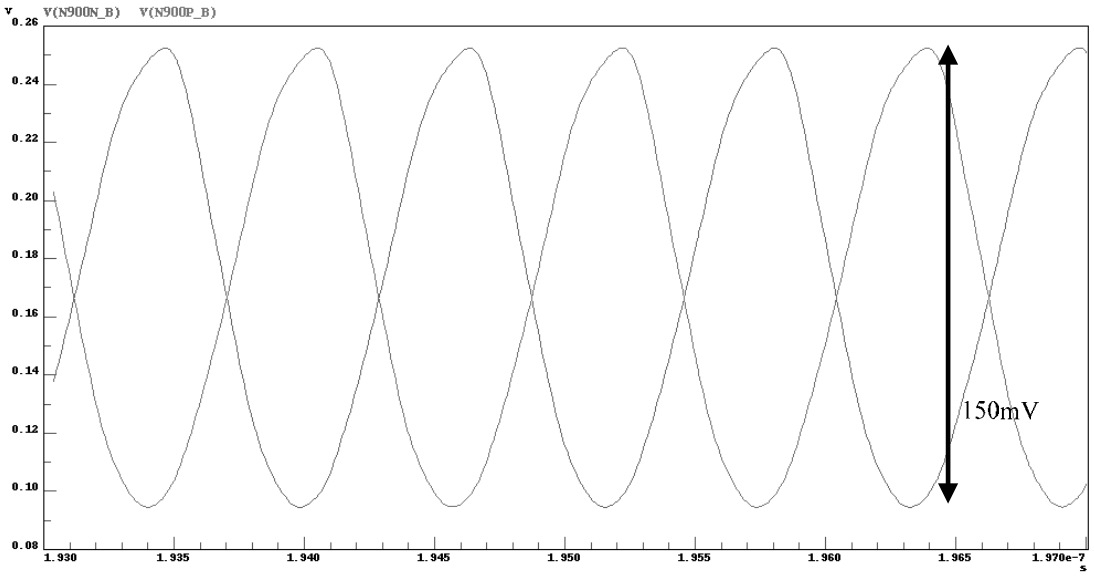


Fig.2-29 Buffer output signal transient analysis

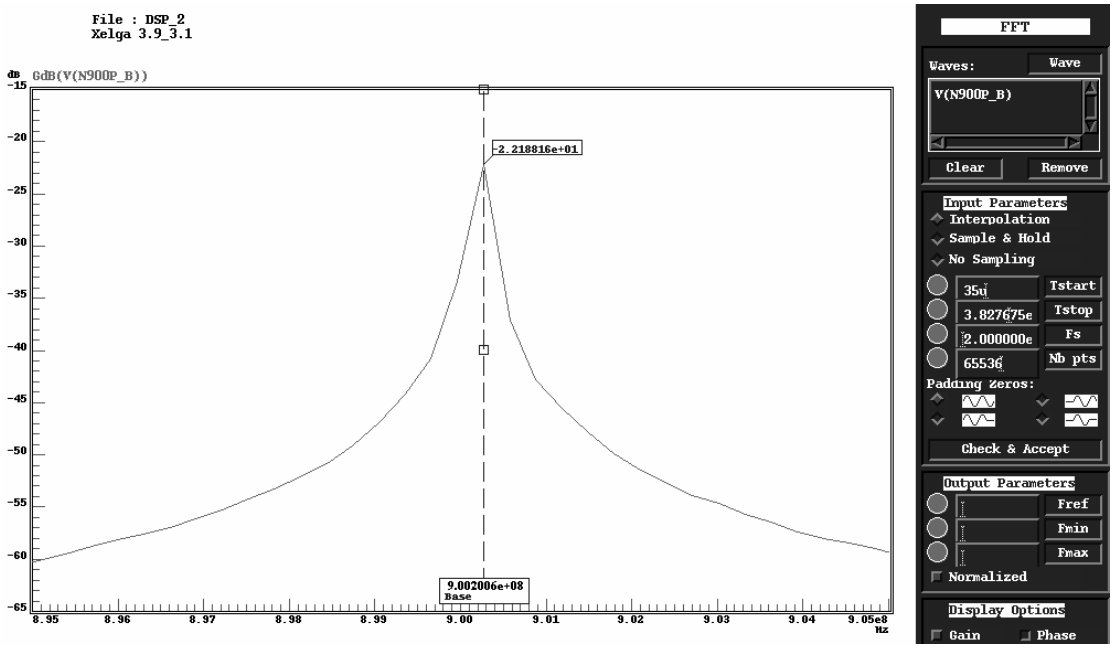


Fig.2-30 900.2MHz FFT simulation result

2.6.5 Simulation Results Summary

Tab.6 Highly integrated quad-bands frequency synthesizer performance summary

Parameter	Performance
Technology	0.18 um CMOS
Supported Application	802.11a/b/g、GSM/DCS1800
Power Supply	1.8 V
VCO Phase Noise (TT)	-114.26 dBc/Hz @1.0MHz
	-119.98 dBc/Hz @1.8MHz
	-121.05 dBc/Hz @2.0MHz
	-126.48 dBc/Hz @3.6MHz
VCO Bank Control Bits	3 bits
No. of Accumulator Bits	12 bits
Reference Frequency	16 MHz
Die Area	1.61 mm2

2.7 Chip Layout

Many frequency synthesizer designers suffer from large chip dimension because the ΣΔ modulator have lots of control signals that need to be input outside from the chip. Try to allocate a pad to each control bit may cause the chip size becomes extremely large. The troubled designer could consider designing a register for all digital control bits. The register is composed of a series of cascading DFFs, architecture shown in Fig.2-31. The Data is controlled by a switch, while Bot is controlled by a botton.

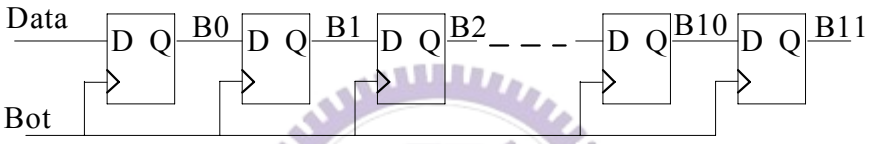


Fig.2-31 Register architecture

The quad-bands frequency synthesizer chip layout is shown in Fig2-32. The pad number has been reduced because two registers were used to load VCO varactor control bits and ΣΔ modulator control bits. Chip dimension is 1.45mm*1.114mm.

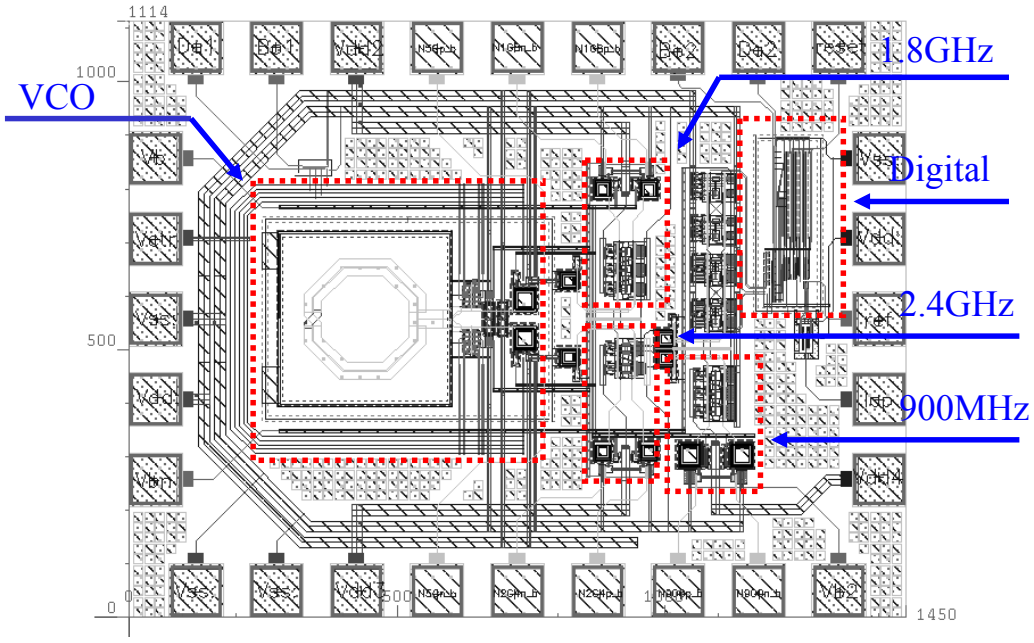


Fig.2-32 Quad-bands frequency synthesizer chip layout

2.8 Conclusion and Comparison

Since quad-bands frequency synthesizer has not yet been promoted, we take two dual-bands frequency synthesizers for comparison, as in Tab.7.

Tab.7 Multi-bands frequency synthesizer comparison

	This Work	**【3】【5】**	**【4】**
Technology	0.18um CMOS	0.5um SiGe BiCMOS	0.35um CMOS
Power supply	1.8V	2.75V	2V
Current Consumption	58mA	36mA	40mA
Supported Application	**802.11a/b/g GSM/DCS**	802.11a/b/g Japan 2.4GHz	802.11a/b/g
VCO Phase Noise	-114dBc/Hz @1MHz	-120dBc/Hz @1MHz	-114dBc/Hz @5MHz
Reference Frequency	16MHz	40MHz	N/A
NO. of Accumulator Bits	12 bits	6bits	10+6 bits
Die area	**1.61mm^2**	3.22mm^2	3.52 mm^2

Multi-system is getting more and more attention recently. In this chapter, we have demonstrated using frequency division technique to design a multi-bands frequency synthesizer. This technique is also practical for single-band frequency synthesizer design. The chip dimension can be saved without scarifying frequency resolution and phase noise performance by designing oscillator at double or triple frequency. The register design also helps designer to save chip dimension when several chip control bits are needed.

Chapter 3

802.11a Integer-N Frequency Synthesizer

The most popular structures for RF frequency synthesizer are fractional-N frequency synthesizer and integer-N frequency synthesizer. Fractional-N structure can synthesize fractional frequency of reference frequency, thus its frequency resolution is much higher than integer-N structure does. Since fractional frequency can synthesized, the reference frequency of fraction-N frequency synthesizer can be choose higher than required frequency resolution to shorten frequency settling time. Unfortunately, fractional-N structure depends on accumulator carrier to control frequency division number. The carrier signal is periodic produced, causing spur noise close wanted frequency. To suppress the spur noise, a complicated modulator is required which makes fractional-N structure much complicated than integer-N structure. Although the integer-N frequency synthesizer can only synthesize integer multiple of reference frequency, the division number is constant in every reference period. The spur noise of integer-N structure is much minor than fractional-N structure. If frequency resolution is not the main factor of frequency synthesizer (ex: 20MHz for 802.11a/b/g WLANs system), integer-N structure is a good choice since the spectrum purity is much clear than fraction-N structure. The comparison of these two frequency synthesizer structures is listed in Tab.8.

Tab.8 Frequency synthesizer structures performances comparison

Parameter	Fractional-N	Integer-N
Frequency Resolution	Fine	Coarse
Settling Time	Fast	Middle
Spurious Noise	Poor	Good
Complexity	High	Low
Power Consumption	Middle	Low

3.1 Architecture [13]

In this chapter, we will demonstrate an 802.11a pulse-swallow integer-N frequency synthesizer design. Circuit block diagram is shown in Fig.3-1. The reference frequency is 10MHz. A pulse-swallow counter is designed to control the dual-modulus divider (8/9). Except the loop filter, every block is designed on chip.

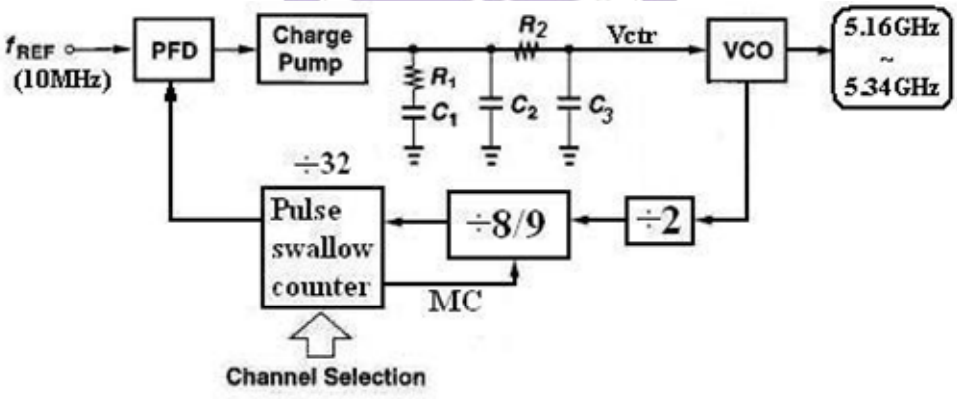


Fig.3-1 802.11a pulse-swallow integer-N frequency synthesizer architecture

3.2 QVCO Design [14][15]

In this chapter we adopt the differentially and complementary cross coupled pairs to generate low phase noise, symmetric and quadrature signal outputs. The

architecture is shown in Fig.3-2. The use of NMOS and PMOS complementary cross coupled pairs offering better rise and fall time symmetry, which results in low up-conversion of 1/f noise and other low frequency noise sources. The complementary structure also provides higher transconductance than all NMOS pairs making circuits much easier to start-up.

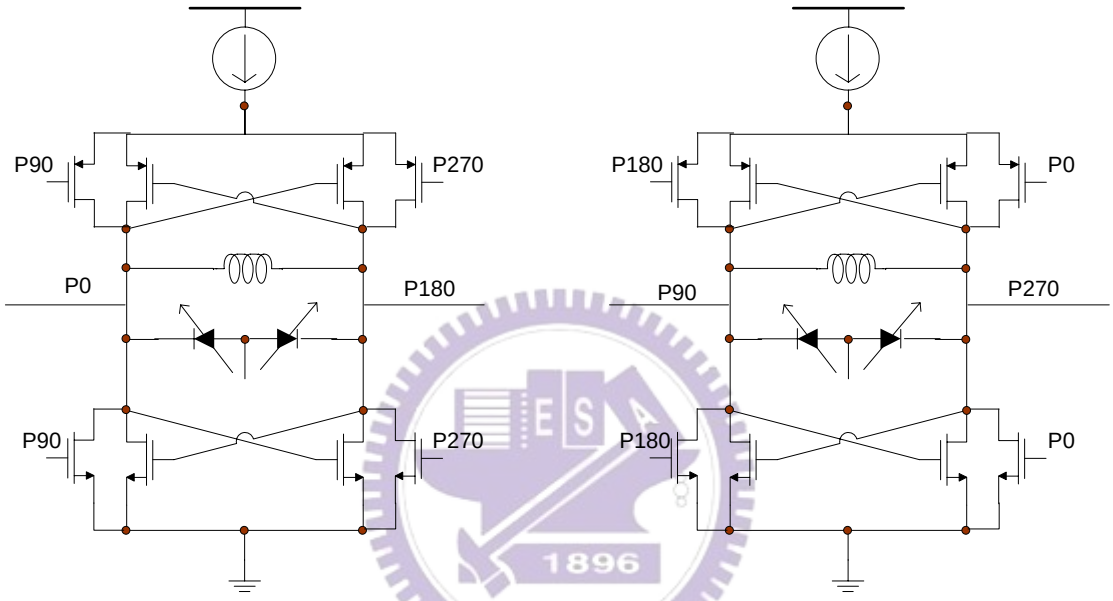
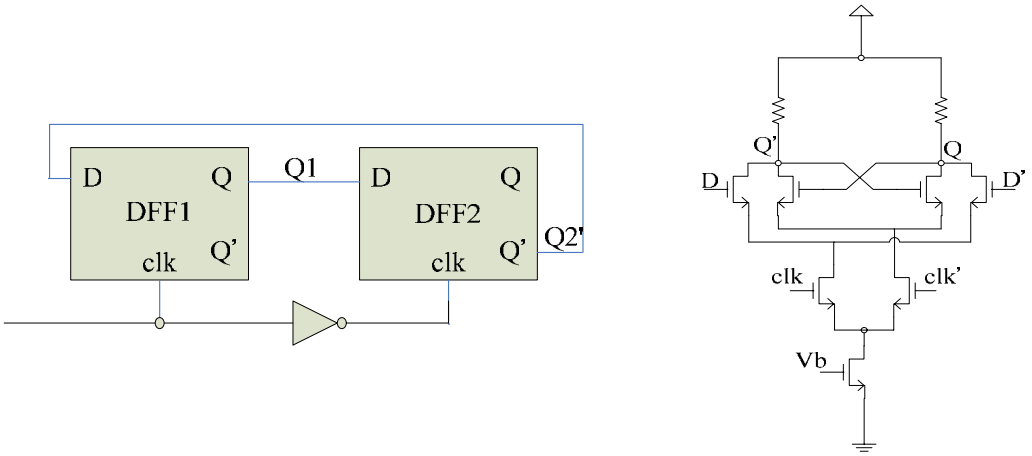


Fig.3-2 Quadrature voltage controlled oscillator architecture

3.3 High speed Frequency Divider [16]

In this design, we adopt DFF operation principle to achieve divide-by-2 circuit. The block diagram is shown in Fig.3-3(a). The DFF2 could be replaced by a delay device used to store Q1 value and flip DFF1 value at next trigger edge. At high frequency, digital logic DFF won't work precisely. Analog DFF must be designed to attain this high frequency divide-by-2 circuit design. The DFF is shown in Fig.3-3(b).



（a） （b）

Fig.3-3（a）Block diagram of divide-by-2 circuit （b）Analog structure of DFF

The cross signal lines in DFF circuit should be layout carefully. Parasitic capacitance and resistance may cause circuit malfunction. We should take these parasitic effect into consider when simulating circuit performance. Fig.3-4 is the transient simulation result of inputting 5.5GHz, 100mV amplitude sine waves to circuit. Circuit will function at 4-6GHz. Minimum acceptable signal amplitude is 80mV.

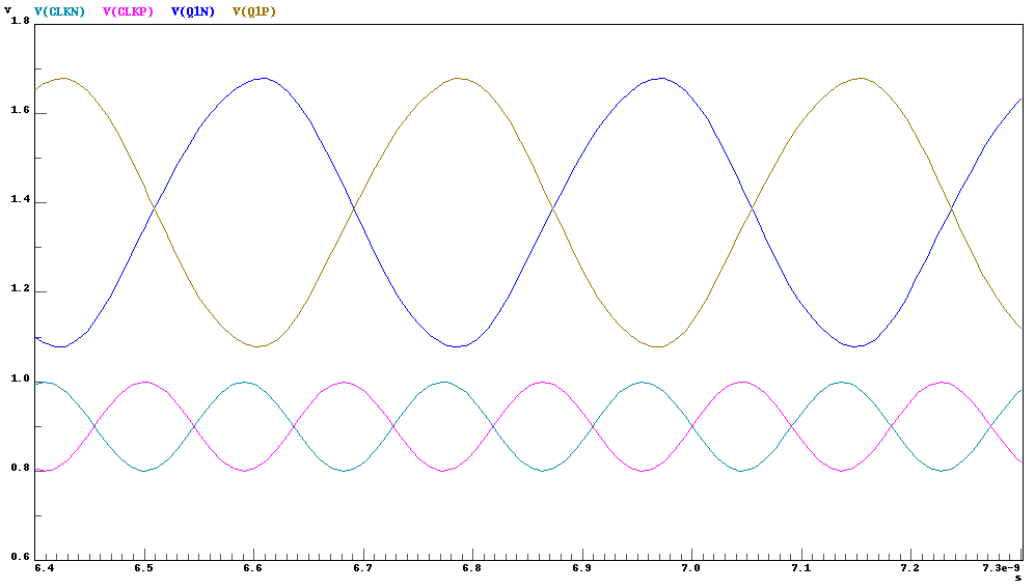
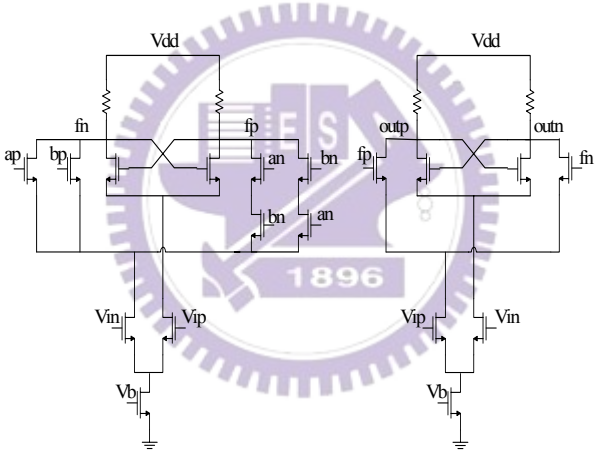


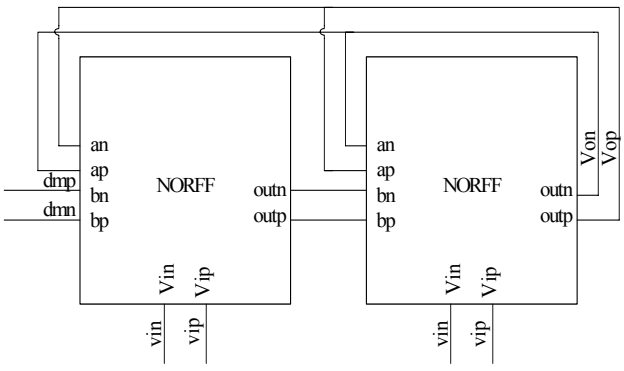
Fig.3-4 Transient simulation result of inputting 5.5GHz, 100mV amplitude sine waves to circuit

3.4 Dual-modulus frequency divider [17][18]

For low power application, the NOR gates of DMFD are combined to D-type flip-flops, circuit shown in Figure.3-5(a). The DMFD architecture is also shown in Figure.3-5(b). Because DMFD uses two D-type flip-flops, it consumes more power than a single divide-by-2 circuit. Since the 4 outputs of these two DFFs are connected to each other, the parasitic capacitance is pretty large. The layout of DMFD should be laid in a high density way. Using Calibre extraction tool, the parasitic capacitance for each DMFD output signal line is about 30fF. The parasitic capacitance should be taken into account at simulation step.



(a)



(b)

Fig.3-5 (a) Architecture combining DFF and NOR gate (b) dual-modulus frequency divider architecture

3.5 Pulse-Swallow Counter [19][20]

The pulse-swallow counter is used to control dual-modulus division (8/9). It is composed of a loading and resetting counter and a channel detection circuit. The counter initially counts up from 0 to the input code (e.g. 6:00110), then counts down from 28 to input code makes a period of 32. The operation principle will be discussed in detail below.

3.5.1 Loading and Resetting Counter

The counter consists of 5 JKFFs with each J and K shorted together individually. UD is a control signal that determines the counting mechanism. As UD=High, counter counts up. As UD=Low, counter counts down. The counter diagram is shown in Fig.3-6.

Initially, UD=High, counter counts up from 0. As A1~A5 equal to channel input codes, UD will change to Low, and counter counts down from 28 (by setting the 3rd to 5th JKFF to High). As A1~A5 equal to channel input codes again, UD will change to High, and counter counts up from 0. Because this counter needs two comparison states (examine whether A1~A5 equal to channel codes or not), one loading state and one resetting state, the loading number is chosen to be 28, not 32! The complete counter structure is shown in Fig.3-7.

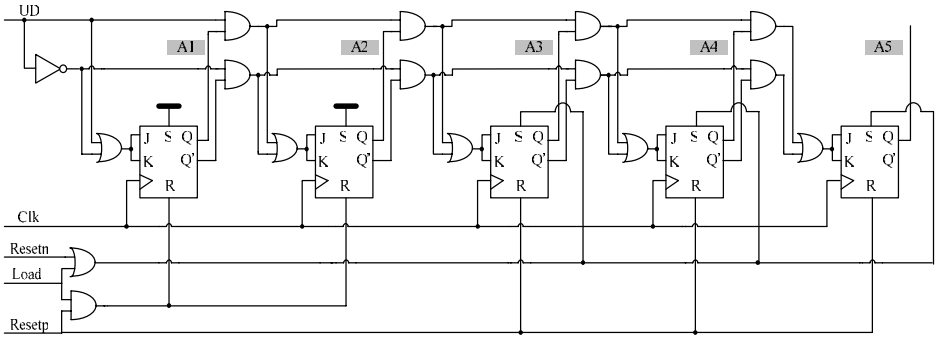


Fig.3-6 Loading and resetting counter

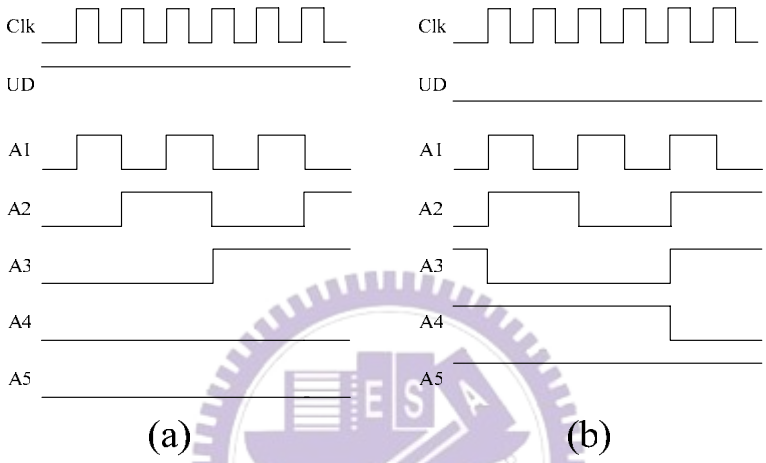


Fig.3-7 Timing diagram of loading and resetting counter

3.5.2 Pulse-Swallow Counter

The complete pulse-swallow counter is shown in Fig.3-8. The 5 counter output bits (A1~A5) are compared to channel input codes (Ch1~Ch5). RL is connected to the JKFF with J, K shorted together. Only when A1~A5 equal Ch1~Ch5, RL will be High. Since RL=High, JKFF will flip its value and change UD state. Notice that UD has a duty circle that is programmed by Ch1~Ch5. For Ch1~Ch5=00100, UD will keep at high for 6 CLK pulses. IF Ch1~Ch5=00110, UD will keep at high for 8 CLK pulses. The UD signal is used modulus control signal since it has a duty circle controlled by the channel input codes. Timing diagram is shown in Fig.3-9.

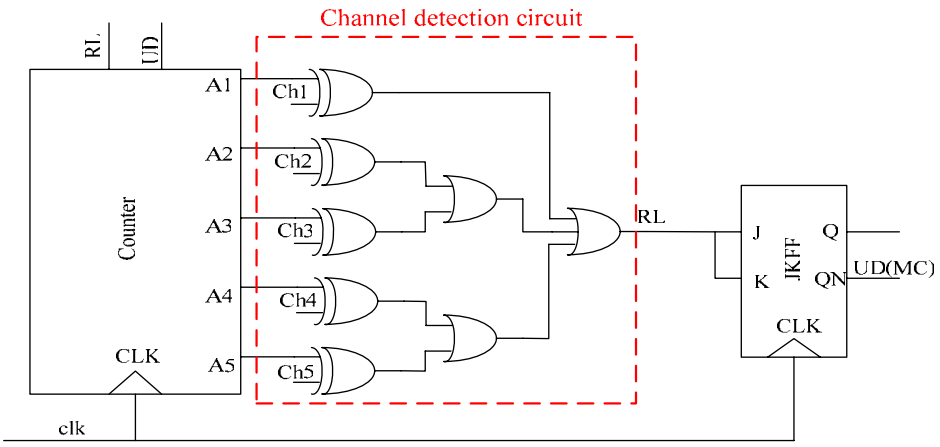


Fig.3-8 Complete pulse-swallow counter architecture

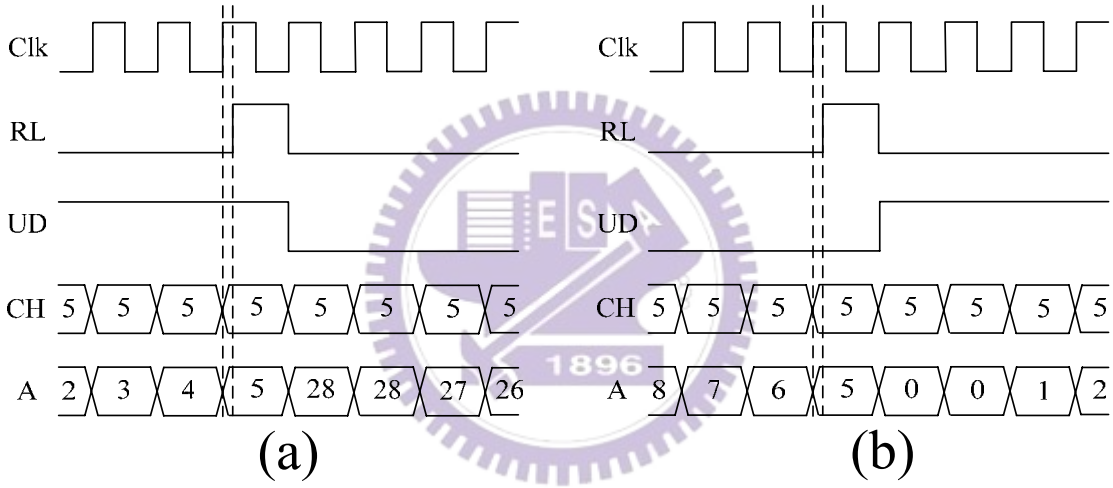


Fig.3-9 Timing diagram of pulse-swallow counter

3.6 PFD and Charge Pump design

The phase frequency detector (PFD) type can be separated to analog and digital. For input signal is at several hundreds MHz order, analog PFD is preferred. In the RF frequency synthesizer, the signal frequency will be scaled down by prescalar and digital frequency divider. Since the divider output frequency is scaled down to only tens MHz, digital PFD is most used in RF frequency synthesizer. The digital PFD is

shown in Fig.3-9. There is one serious problem with this tri-state PFD: dead zone, as depicted in Fig.3-11. This problem results from charging time of charge pump. When reference signal is almost in-phase with divider output signal, the pulse duration produced by PFD isn't long enough to turn on charge pump, causing this small phase mismatch undetectable. To solve this problem, a delay circuit is induced before DFF reset pin to increase PFD pulse duration. The delay time should be long enough to turn on charge pump.

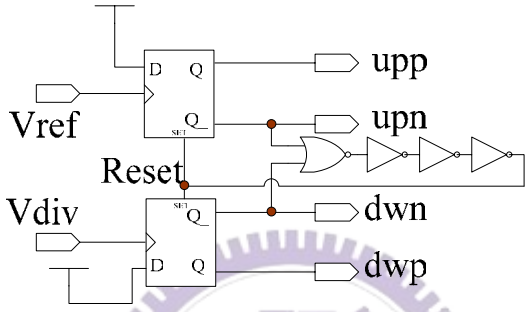


Fig.3-10 Tri-state phase frequency detector (PFD)

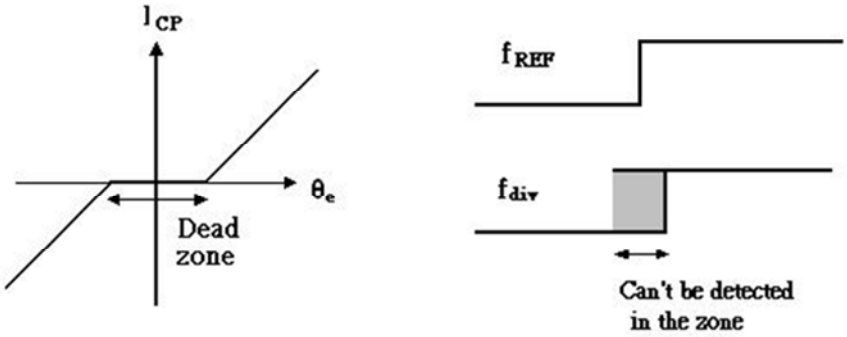


Fig.3-11 Dead zone problem of PFD

The purpose of charge pump is to transform the phase mismatch detected by PFD to a charging current. To achieve a high voltage output range at the charge pump, the transistor size of the current mirror transistors (M_1-M_{11}) must be chosen carefully. Also an accurate layout of the charge pump is important to improve the matching of the positive and negative current to avoid mismatch currents. Mismatch currents produced when the two phase are compared cause reference spur. Reference spur interferes with adjacent channel in RF receiver and produces undesired spectral

emission in RF transmitter. We implement two additional transistors (M_{12}, M_{14}) to guarantee in case of switching the transistors M_{13} and M_{15}, their sources are already precharged. Above reduces current peaks during the switching time and suppressing the spurious tones, too. The charge pump structure is shown in Fig.3-12.

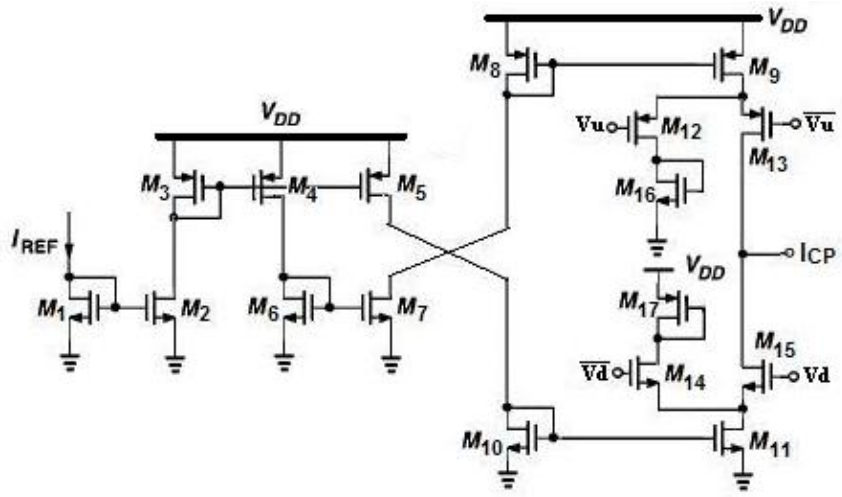


Fig.3-12 Charge pump architecture

3.7 Loop filter design

The loop filter is very important in frequency synthesizer design. We expect the loop bandwidth can be high enough for fast locking behavior. Additionally, loop bandwidth should be low to suppress spurious noise results from PFD and charge pump switching. Since tradeoff exists in the loop filter design, and loop bandwidth should be chosen carefully. For system stability consideration, the phase margin should be designed about 50 degrees.

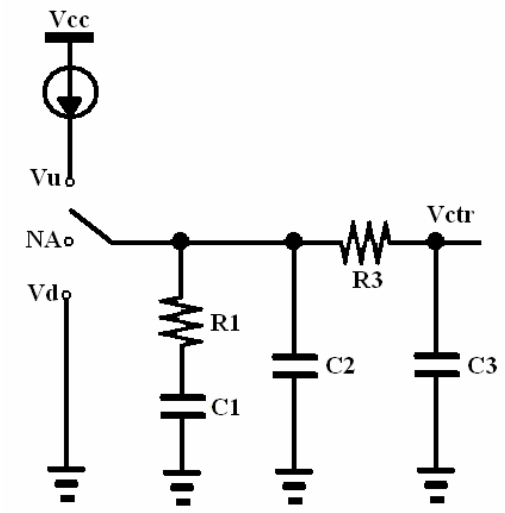


Fig.3-13 4th order Loop filter architecture

Consider all the requirements above; the 4th order loop filter architecture is adopted in this chapter. Fig.3-13 shows the 4th order loop filter architecture. The loop filter transfer function is:

$$H(S) = K_h \frac{S + \omega_z}{S(S + \omega_{p1})(S + \omega_{p2})}$$

$$where\ K_h = \frac{R_1 C_1}{C_1 + C_2},\ \omega_z = \frac{1}{R_1 C_1},\ \omega_{p1} = \frac{C_1 + C_2}{R_1 C_1 C_2},\ \omega_{p2} = \frac{1}{R_3 C_3}$$

Locations of poles, zeros and loop bandwidth determines frequency synthesizer settling time, spurious noise and phase margin. The frequency difference of ω_z to K should equal to the frequency difference of ω_{p1} to K for largest phase margin performance. According to theory and experiment, the poles, zeros, loop bandwidth and reference frequency allocation diagram is depicted in Fig.3-14.

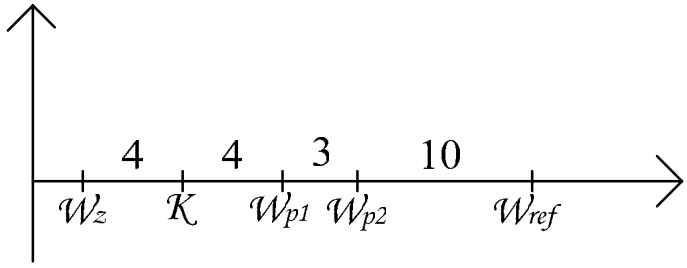


Fig.3-14 Theoretical and experimental poles, zeros, loop bandwidth and reference frequency allocation diagram

After the locations of poles, zeros and loop bandwidth are determined; we derived all the resistance and capacitance values below:

$$R_1 = K_h(1+\frac{1}{x}) = \frac{KN}{K_{vco}K_d}(1+\frac{1}{x}) \ , \ where\ x = \frac{C_1}{C_2} = \frac{\omega_{p1}}{\omega_z} - 1$$

$$C_1 = \frac{1}{\omega_z R_1}$$

$R_3 C_3 = \omega_{p2}$, C_3 should be kept large to bypass spurious noise!

Example:

K_d=9.57μA/rad, K_o=2429.5Mrad/V, ω_{ref}=62.83rad/s, N=520

$\omega_{ref}:\omega_{p2}:\omega_{p1}$:K:$\omega_z$=640:64:16:4:1

$$\frac{C1}{C2} = \frac{\omega_{p1}}{\omega_z} - 1 = \frac{16}{1} - 1 = 15$$

$$R_1 = \frac{KN}{K_{vco}K_d}(1+\frac{1}{x}) = \frac{62.83\times 520}{2426.5\times 9.5738\times 160}(1+\frac{1}{15}) = 9.36\ K\Omega$$

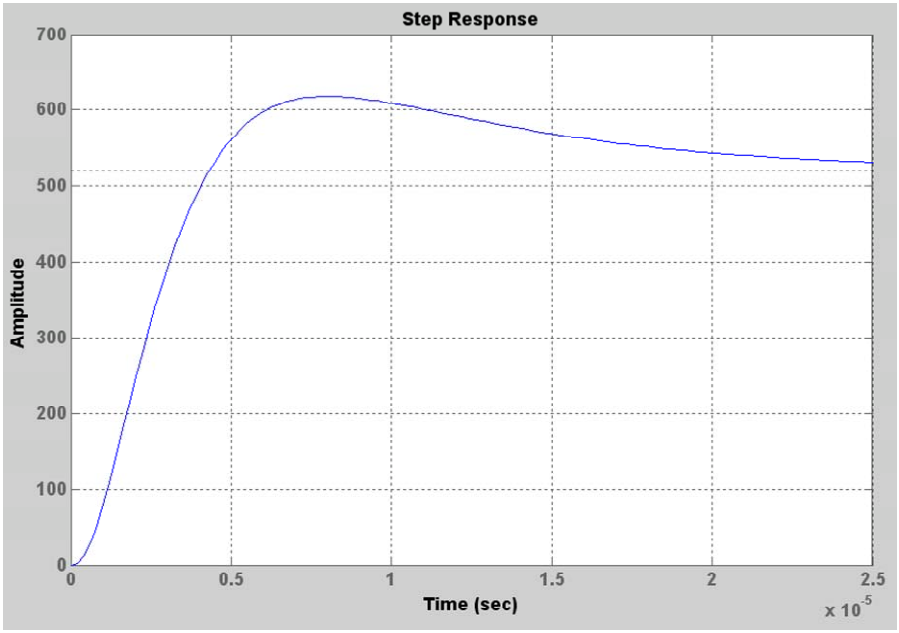
$$C_1 = \frac{640}{9.36\times 62.83} = 1.09\ n\text{F}$$

$$C_2 = \frac{1.09}{15} = 72.7\ p\text{F}$$

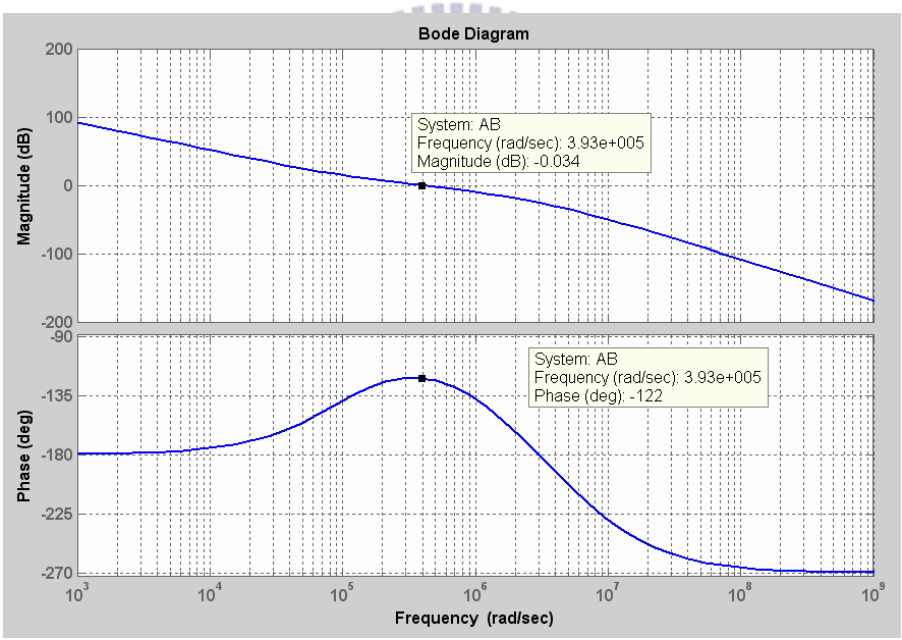
C_3=30 pF

$$R_3 = \frac{10}{30\times 62.83} = 5.3\ K\Omega$$

Compute the resistances and capacitance values according to the above expression and Fig.3-14. Then we apply MATLAB step function and bode plot function to simulate frequency synthesizer close loop transient settling time and open loop phase margin. The MATLAB simulation results are shown in Fig.3-15. Because the resistances and capacitances are quite large comparing to on-chip resistances and capacitances, the loop filter is designed off-chip by microwave devices.



(a)



(b)

Fig.3-15 MALAB simulation results (a) transient analysis (b) bode plot

3.8 Synthesizer simulation results

Fig.3-16 shows frequency synthesizer close loop transient simulation results. From 0 to 50μs, Ch5~CH1=00000, synthesizer locks at 5.14GHz in 40μs. After 50μs,

CH5~CH1=00010, synthesizer locks at 5.18GHz in 40μs. Fig.3-17 shows 5.18GHz spectrum simulation results. Output power is -20.7dBm. The frequency synthesizer performances are summarized in Tab.9.

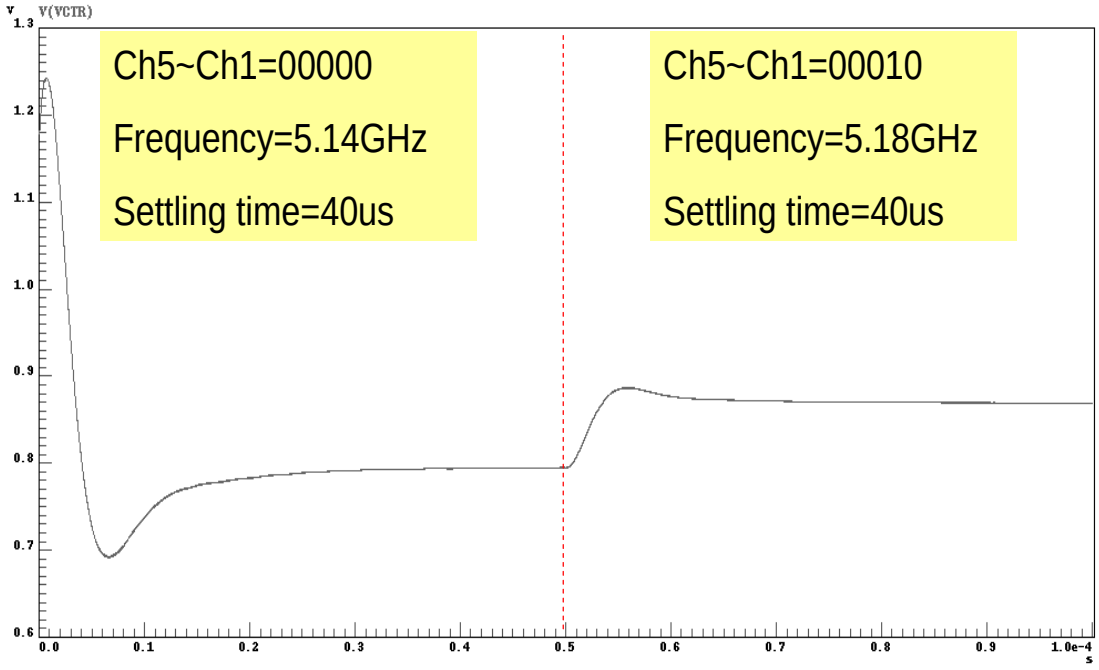


Fig.3-16 Frequency synthesizer transient simulation results

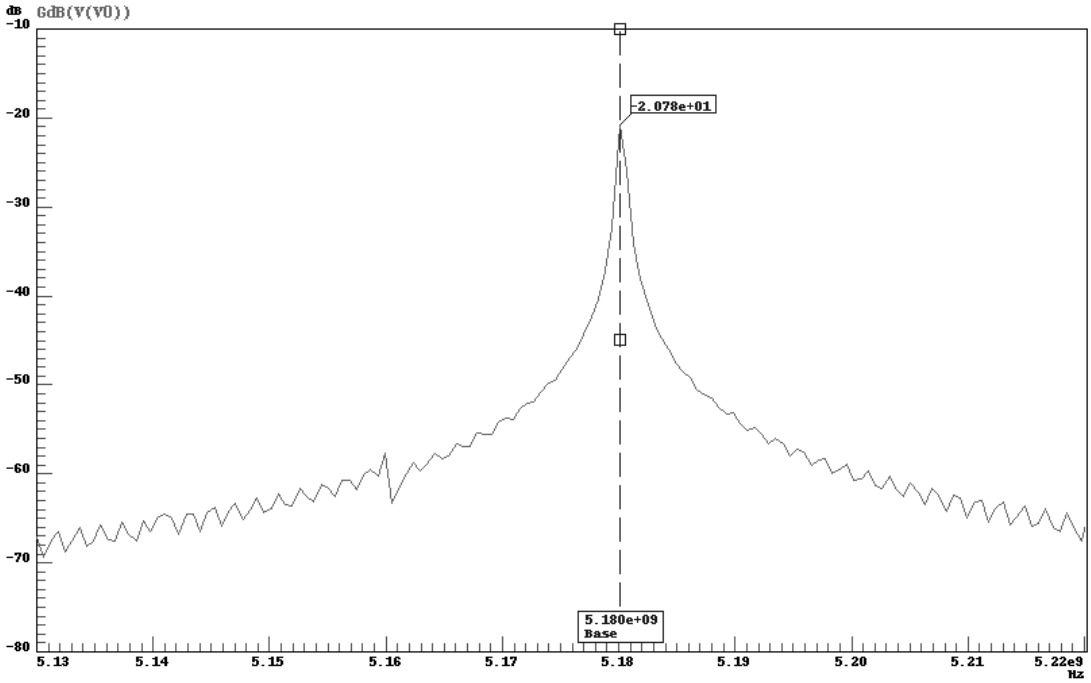


Fig.3-17 5.18GHz spectrum simulation results

Tab.9 802.11a integer-N frequency synthesizer performances summary

Parameter	Simulation Results
Technology	TSMC 0.25μm CMOS
Application	802.11a
Synthesizer Architecture	Integer-N pulse-swallow
Channel Control Bit	5 bits
Phase Noise	-106 dBc/Hz @1MHz
Reference Frequency	10 MHz
Settling Time	40μs
Output Power	-20.7 dBm
Power Consumption	20.44 mW

3.9 Measurement Results

3.9.1 Measurement Consideration

The PCB (printed circuit board) layout and practical FR4 PCB circuit conjunction with SMA connectors for this work are shown in Fig.3-18 and Fig.3-19, respectively. The voltage controlled oscillator signal line width on the PCB must be designed 50Ω for impedance matching. The PCB also preserves additional space for DC blocking and bypassing capacitors. The chip is adhered to PCB and all I/O pads are bonded onto PCB via bond-wires. The die photograph is shown in Fig.3-20.

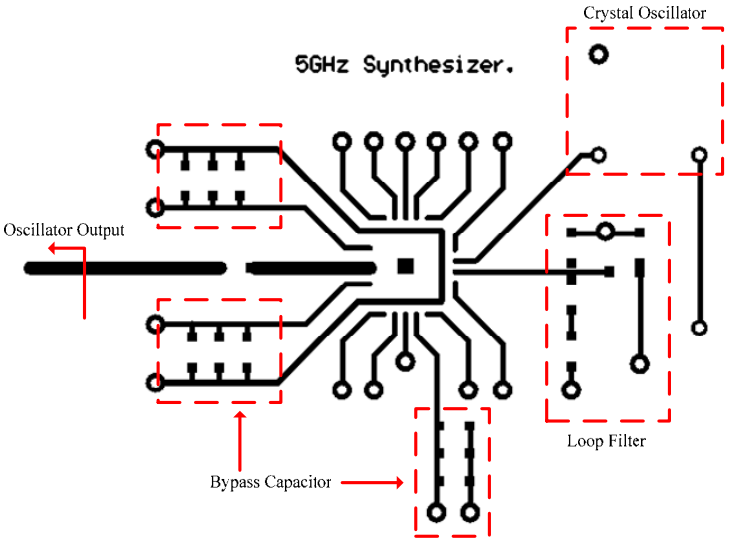


Fig.3-18 PCB layout of 5GHz frequency synthesizer

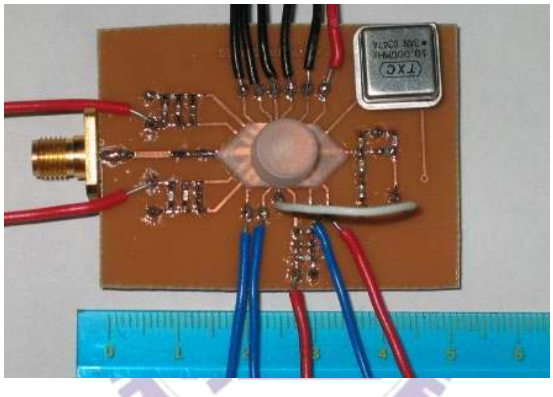


Fig.3-19 5GHz frequency synthesizer practical FR4 PCB measurement circuit

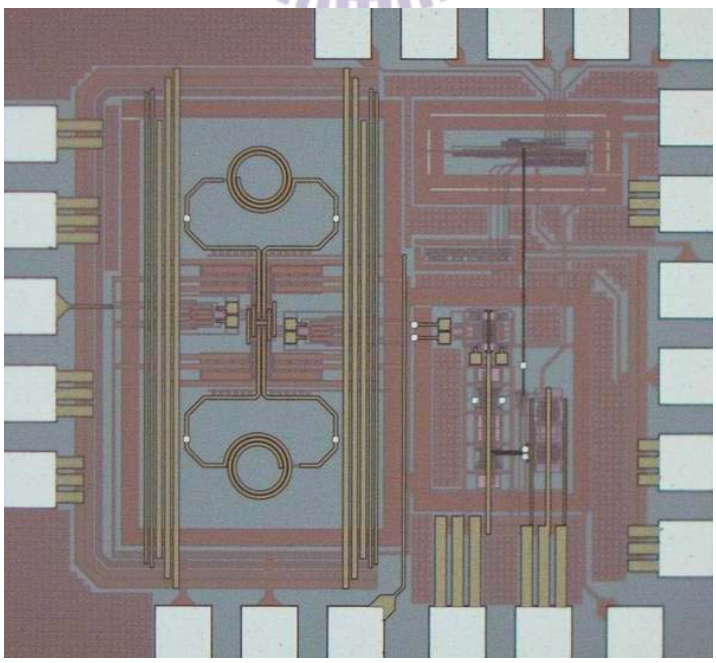


Fig.3-20 Die photo of 5GHz frequency synthesizer

3.9.2 Measurement V.S. Simulation Results

We perform open loop measurement first. The measured DC currents are 13mA for VCO and output buffer, 7mA for frequency divider. Measured DC current fits the simulation FF corner (11.6mA for VCO and buffer, 7mA for divider). Apply spectrum analyzer to measure voltage controlled oscillator output signal power, phase noise and tuning range. The measured output signal power is -26dBm, while the simulation is -20dBm. The measurement result is shown in Fig.3-21. Measured frequency tuning range is 4.6-5.25 GHz, while simulation result of FF corner is 5.23-5.88 GHz. The measured frequency is about 630MHz lower than simulation. The measure result is shown in Fig.3-22. Measured phase noise is -104.33dBc/Hz @1MHz (-54.33 $-10\log10^{5}$=-104.33 dBc/Hz @1MHz), while the simulation result is -105dBc/Hz @1MHz. The phase noise performance is quite close to simulation results and shown in Fig.3-23.

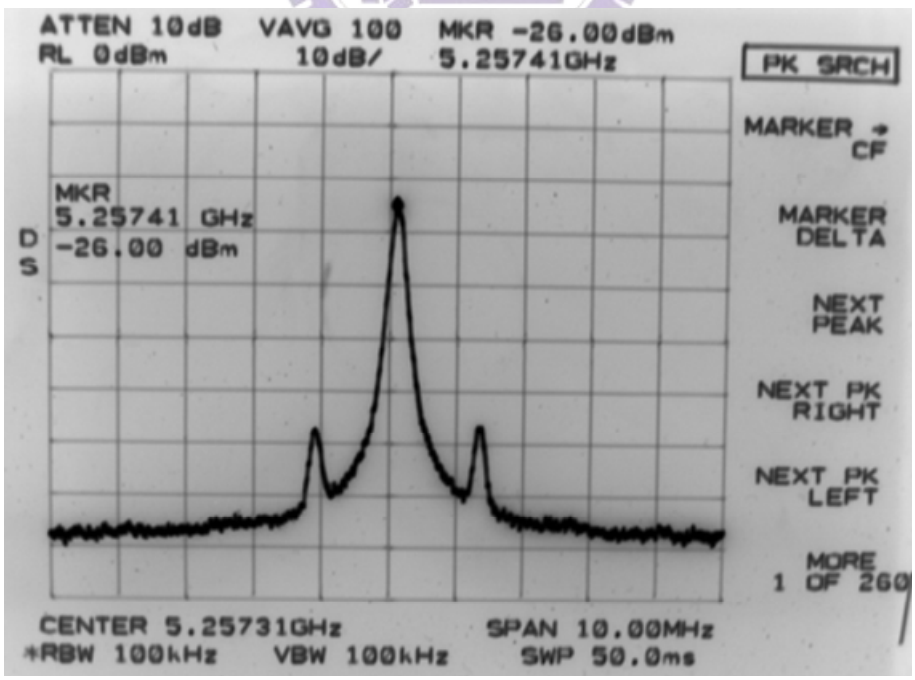


Fig.3-21 Voltage controlled oscillator output power measurement

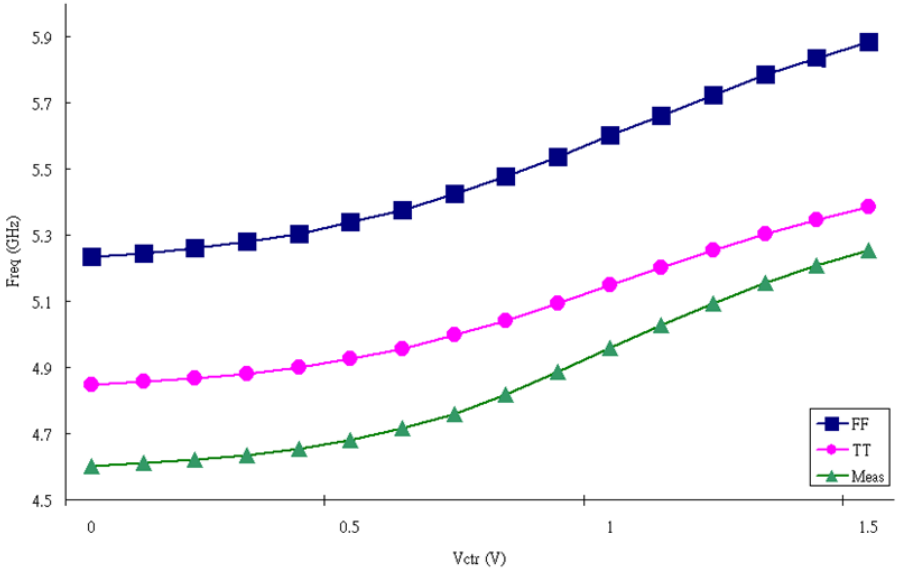


Fig.3-22 Tuning range measurement

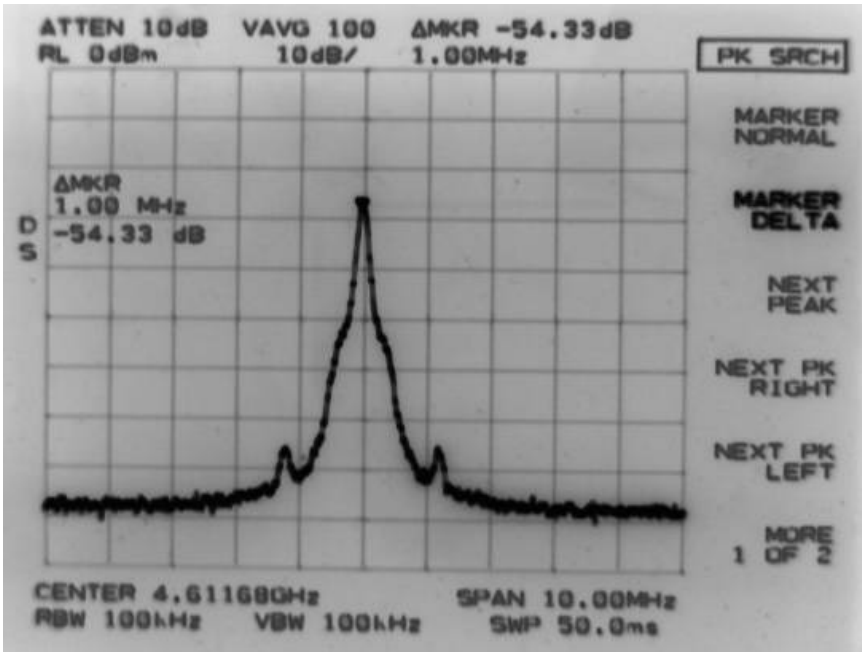


Fig.3-23 Phase noise measurement

The frequency synthesizer didn't lock to the wanted frequency. The problem may results from 2 main reasons. First, the VCO signal swings are not sufficient to push frequency dividers. The measured signal is 6dBm less than simulation. In this design, low power consumption is our design guide. Each circuit is designed to consume fewest DC current. Since low power consumption is of most concern, VCO output

signals were not designed to have large power output. The simulated VCO signal swing is 250mV. The fist divide-by-2 circuit will function if the input signal swing is large than 200mV. 6dB power loss means voltage is degrade by a factor of 2, which means the measured signal swing is only 125mV. Since VCO output signal swing is only 125mV, the divider is unable to function. Second, at the design step of high frequency divide-by-2 circuit, the loading and parasitic effect is very serious. To deal with this problem, we utilized a common drain buffer amplifier. Although the loading and parasitic problems have been solved, the divider output voltage swing is even smaller than VCO output signals. The buffer amplifier consumes DC power and voltage swing, makes system harder to design. To examine the parasitic problem, we use Caliber extraction tools to extract the parasitic capacitances and resistances. The parasitic capacitance of the first divide-bu-2 circuit is 20fF. This parasitic capacitance should be taken into account in the simulation step. By careful consideration, the common buffer amplifier should be eliminated to increase system stability and functionality. This work will be redesigned with no divider buffer amplifier and higher VCO output power.

Chapter 4

An 8-bit AFC Voltage Controlled Oscillator

In this chapter, a high frequency resolution voltage controlled oscillator (VCO) design will be discussed. PMOS varactors are used to achieve 8-bits frequency resolution. This circuit is a step stone to an all-digital complete integration frequency synthesizer design. By designing a high frequency resolution VCO and using a digital coding method to control VCO varactor banks and VCO control voltage, the dream of whole-new all-digital frequency synthesizer architecture will come true. In this new structure, traditional loop filter, used to be implemented off-chip, will be omitted. This new structure will help to increase RF system integration and speed up frequency settling time by several times.

4.1 Proceeding on All-Digital Frequency Synthesizer

4.1.1 Background

Traditionally, the loop filter of frequency synthesizer is an off-chip circuit due to large capacitances and resistances. For SOC application, this will definitely cause problem. In order to integrate loop filter into chip, we propose an all-digital frequency synthesizer architecture.

In the voltage controlled oscillator, each varactor bank code tuning range covers neighboring varactor bank codes by 50%. Therefore, overall tuning range of VCO is:

$BW = \left[1 + \left(2^n - 1\right) * 0.5\right] f$, where f is average tuning range of each varactor bank code. 802.11a application specifies a usable band from 5.15GHz to 5.35GHz. Consider process variation, a 600MHz VCO tuning range is sufficient. Substitute BW=600MHz into above expression, the average varactor tuning range f will be 4.67MHz.

The center frequency tolerance in 802.11a specification is ±20ppm. If center frequency is 5.25GHz, the allowable frequency shifting is ±105KHz. In an 8-bits resolution VCO, average varactor bank code tuning range is 4.67MHz. If we design the control voltage of VCO to have more than 6-bits resolution, the 802.11a specification can be met. We conclude that a 14-bits all-digital frequency synthesizer is practical for 802.11a application. More than that, if we adopt dichotomy logic to design frequency synthesizer comparison mechanism, after 14 decisions system will lock at wanted frequency. Take reference frequency = 10MHz for example, every 0.1μs can determine a bit. Total frequency settling time will be only 14*0.1=1.4μs. Compare to traditional frequency synthesizer settling time of 40μs, this new structure shows a great potential.

4.1.2 Proposed Architecture [21]

The 14 bits should be divided into 2 parts, 8 bits for VCO bank coarse tuning, another 6 bits is left for VCO control voltage fine tuning. Because the VCO is the most important component in frequency synthesizer, it must be proven before been integrated into all-digital frequency synthesizer. The proposed new frequency synthesizer architecture is shown in Fig.4-1. One can find out PFD, charge pump and loop filter circuits do not appear in our proposed architecture. The key component is

the frequency detector that can discriminate which of reference signal or divider signal has higher frequency in a few signal pulses. At first, VCO control voltage is connected to V_{ref}. After first eight comparisons, the 8 VCO varactor banks will be set. Then VCO control voltage is switched to DAC output signal to perform frequency fine tuning. In six more frequency comparisons, the frequency synthesizer will lock at wanted frequency.

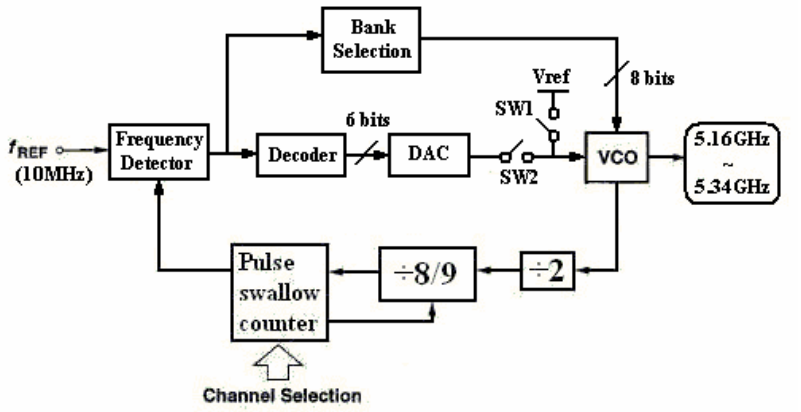


Fig.4-1 Proposed new all-digital frequency synthesizer architecture

4.1.3 Frequency Detector Design [22][23]

The analog frequency detector is shown in Fig.4-2. It is composed of two quadrature mixers and two low pass filters. The circuit principle is as following:

If $\omega_1 > \omega_2$: $V_a = \cos(\omega_1 - \omega_2)t$

$V_b = -\sin(\omega_1 - \omega_2)t = \cos[(\omega_1 - \omega_2)t + \pi/2]$

$\rightarrow$ V_a lags V_b by $\pi/2$

If $\omega_1 < \omega_2$: $V_a = \cos(\omega_1 - \omega_2)t = \cos(\omega_1 - \omega_2)t$

$V_b = -\sin(\omega_1 - \omega_2)t = \sin(\omega_1 - \omega_2)t$

$\rightarrow$ V_a leads V_b by $\pi/2$

By observing Va and Vb, we can tell which of the incoming signal has higher frequency.

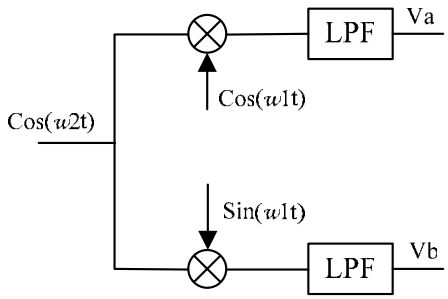


Fig.4-2 Analog frequency detector

Next, we try to form a digital type frequency detector. The two quadrature mixers is replaced by two DFFs. The four ANDs will generates the discrimination signals AB'C, A'BC', AB'C' and A'BC. The discrimination signals conclude all possible combinations about whether Div leads or Ref leads. After JKFF, frequency detector outputs the discrimination results. "H" states Div is slower than Ref, "L" states Div is faster than Ref. "S" means that these two signals have same frequency.

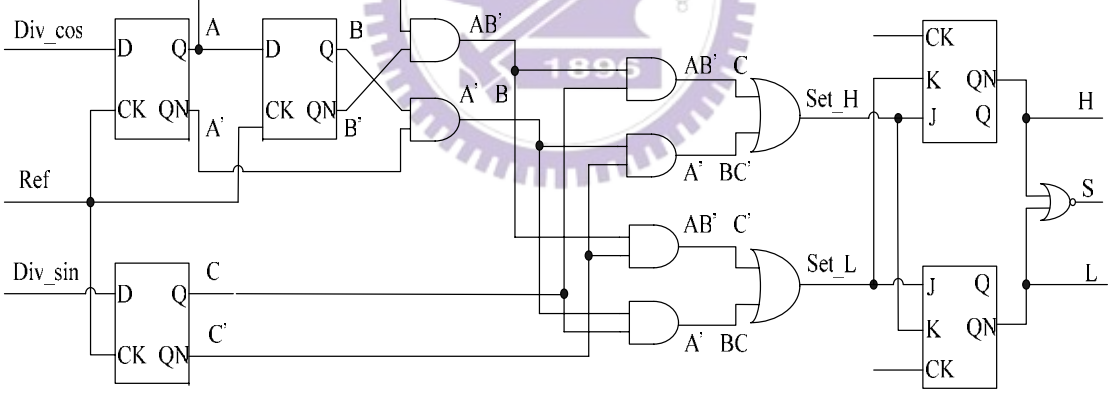


Fig.4-3 Digital frequency detector

Fig.4-3 is further modified to a balanced structure, shown in Fig.4-4, to increase frequency discrimination range.

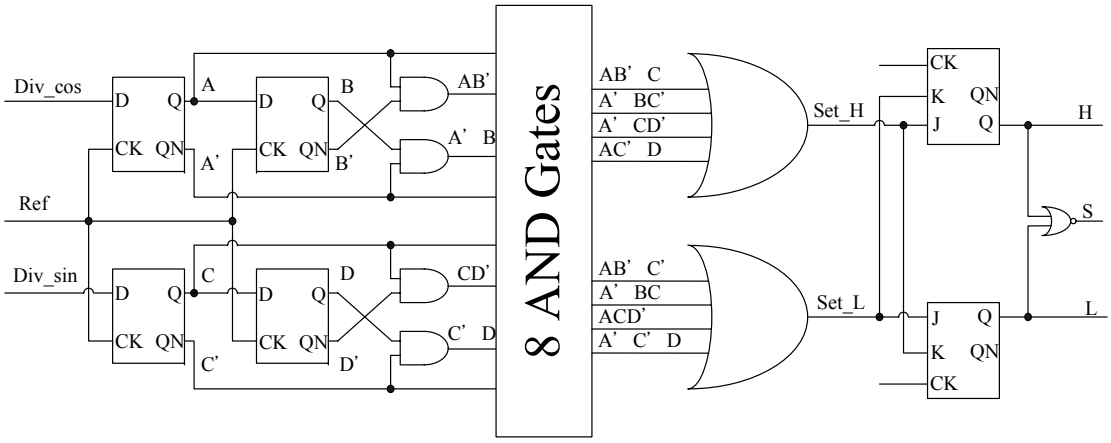


Fig.4-4 Modified balance digital frequency detector

Although this frequency detector can discriminate frequency precisely, the discrimination speed is too slow if the incoming signals don't differ too much in frequency. This problem troubles us a lot, since the all-digital frequency synthesizer depend on this circuit to shorten frequency settling time. A phase synchronizer may be needed to solve this problem. With the help of phase synchronizer, we can discriminate frequency in only one reference clock. Fig.4-5 illustrates the function of a phase equalizer in this frequency detector design.

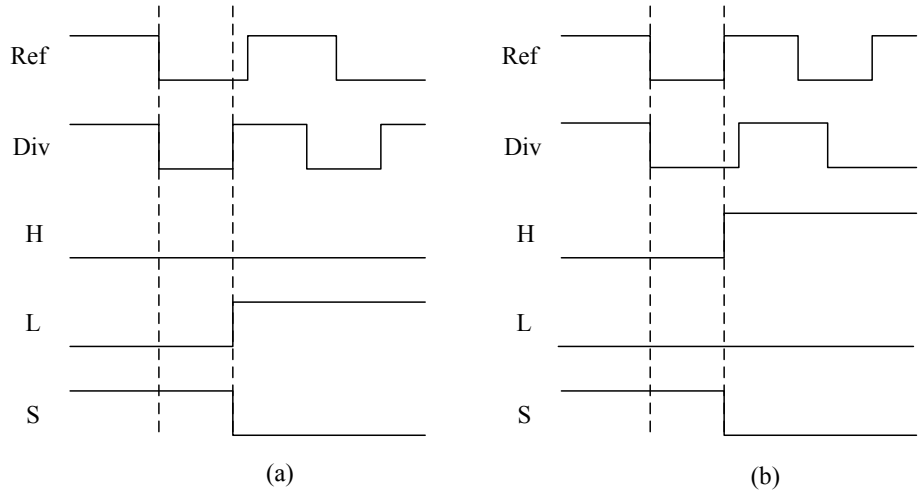


Fig.4-5 Function of phase synchronizer to aid frequency detector design

4.2 8 bits VCO Architecture [24][25][26]

Since the average tuning range of each varactor bank code is only 4.67MHz, the varactor model provided by TSMC is not suitable in this design. In this design, we implement these varactors by PMOS with Drain, Source and Bulk are shorted together. The PMOS varactor layout is shown in Fig.4-6[27]. The tuning characteristic of PMOS varactor is shown in Fig.4-7.

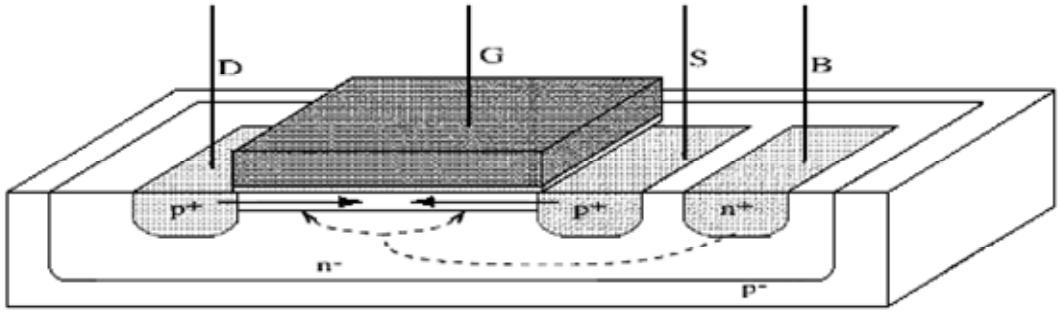


Fig.4-6 PMOS varactor layout

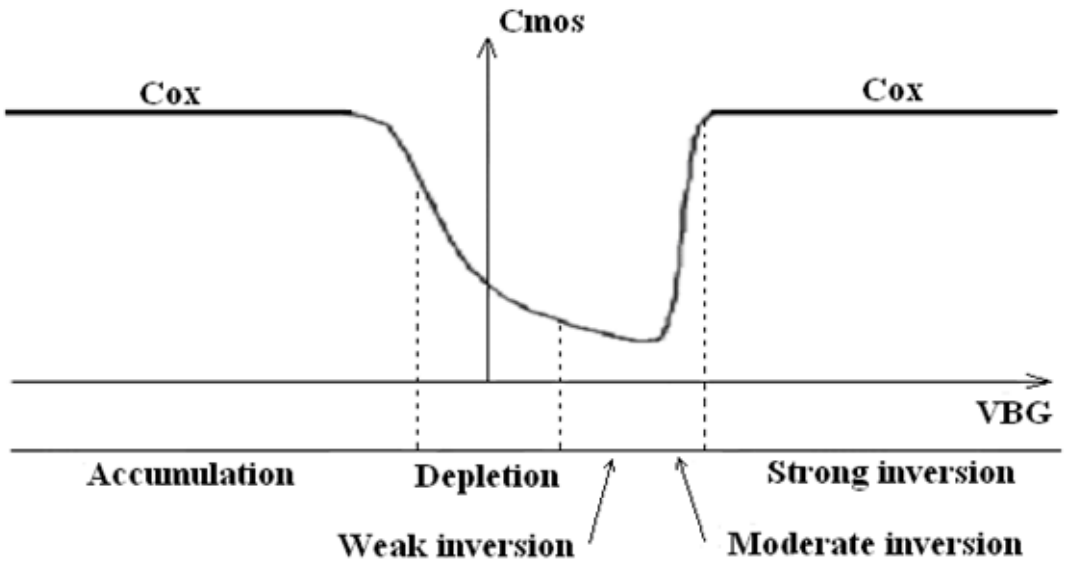


Fig.4-7 Tuning characteristic for the PMOS capacitance with B≡D≡S

VCO is the core circuit in the frequency synthesizer. In most RF design, we use LC-tank oscillator instead of ring oscillator for better phase noise. For image cancellation, we hope VCO can provide quadrature phase output signal. There are three ways to generate quadrature signals: divide-by-two circuit [28]; RC-polyphase network [29]; and two VCOs cross connect with each other [30]. Using divide-by-two circuit needs to design a VCO operate at the double frequency of original frequency. A VCO with RC-polyphase network consumes less power than others, but RC-polyphase is a signal power hungry circuit. For accurate quadrature phase signal and large output signal power reasons, we design two VCOs differentially connect to each other to generate quadrature signal. The whole schematic of the 8-bits frequency resolution quadrature VCO is shown in Fig.4-8. The architecture of cross-coupled pairs adopts both NMOS and PMOS transistors to enhance negative conductance and LC-resonator to include the resonance frequency band.

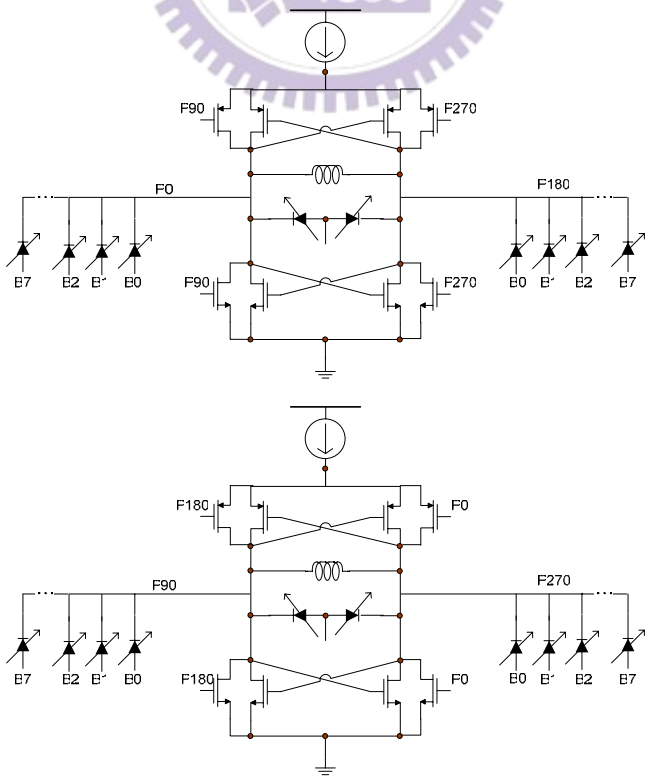


Fig.4-8 8-bits frequency resolution voltage controlled oscillator

4.3 Measurement

4.3.1 Measurement consideration

The PCB (printed circuit board) layout and practical FR4 PCB circuit conjunction with SMA connectors for this work are shown in Fig.4-9 and Fig4.10, respectively. The quadrature voltage controlled oscillator signal line width on the PCB must be designed 50Ω for impedance matching. The PCB also preserves additional space for DC blocking and bypassing capacitors. The chip is adhered to PCB and all I/O pads are bonded onto PCB via bond-wires. The die photograph is shown in Fig.4-11.

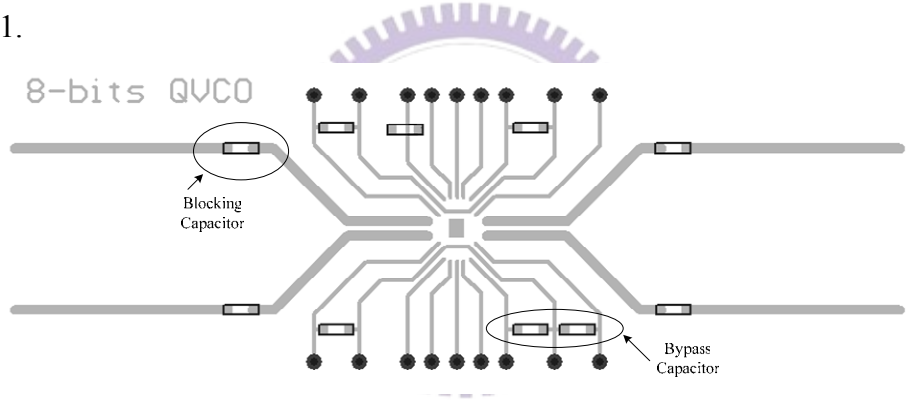


Fig.4-9 PCB layout of 8-bit voltage controlled oscillator

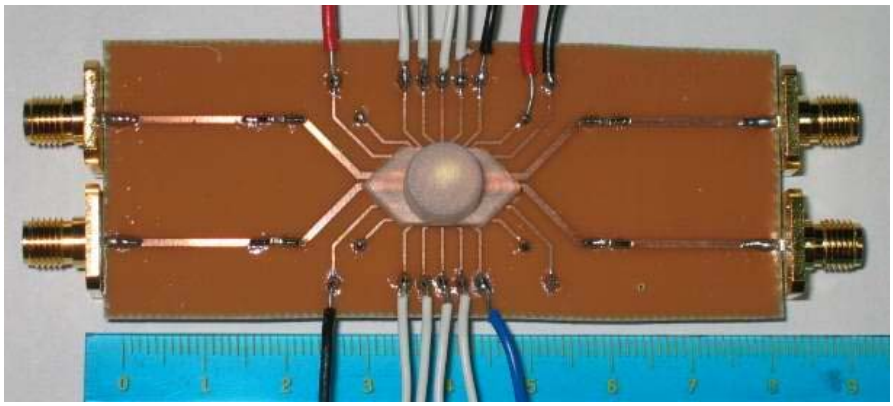


Fig.4-10 8-bit voltage controlled oscillator practical FR4 PCB measurement circuit

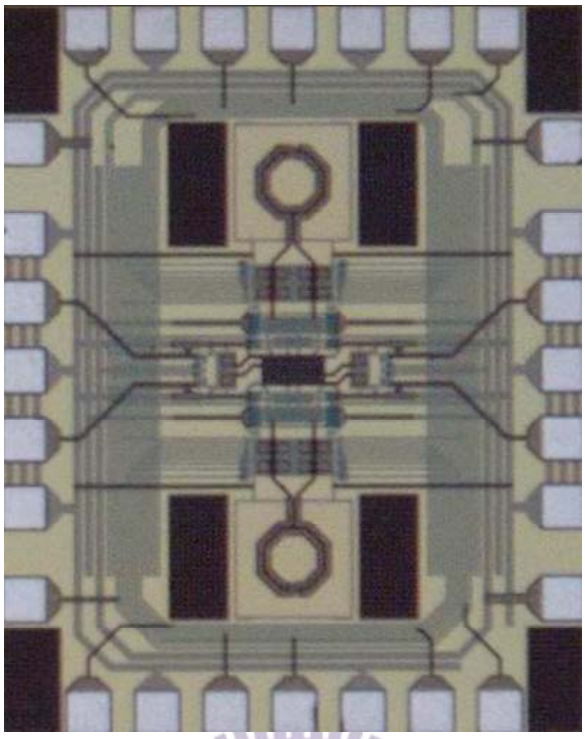


Fig.4-11 Die photo of 8-bits voltage controlled oscillator

4.3.2 Measurement V.S. Simulation Results

To measure the DC current consumption, we sweep the bias voltage of the VCO core current source from 0V to 1V, and measure the consumption current. Fig.4-12 shows the DC current consumption of 8-bits voltage controlled oscillator. The measurement result shows that the chip consumes about 6mA less than TT corner and 2mA less than SS corner. This result tells that chip doesn't feet in the 6 corner cases (FF, FT, FS, TT, TS, SS), and the measurement results would be greatly violated the simulation results.

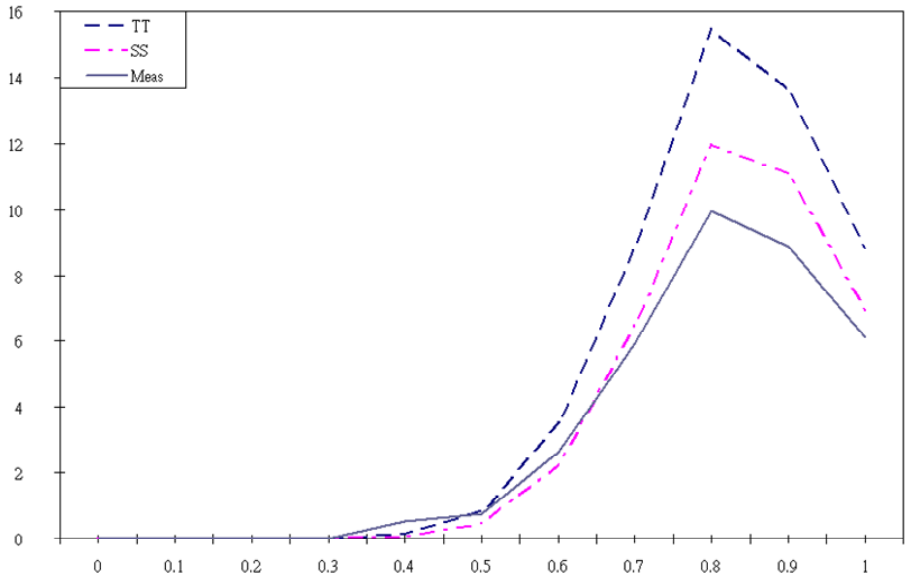


Fig.4-12 Current consumption, simulation V.S. Measurement

The quadrature outputs are connected to the spectrum analyzer to measure signal spectrum, output power, tuning range and phase noise. Setting resolution bandwidth to 100KHz, frequency span to 10MHz, the measured phase noise is -101dBc/Hz @1MHz (-51 -10log10^{5}=-101 dBc/Hz @1MHz).

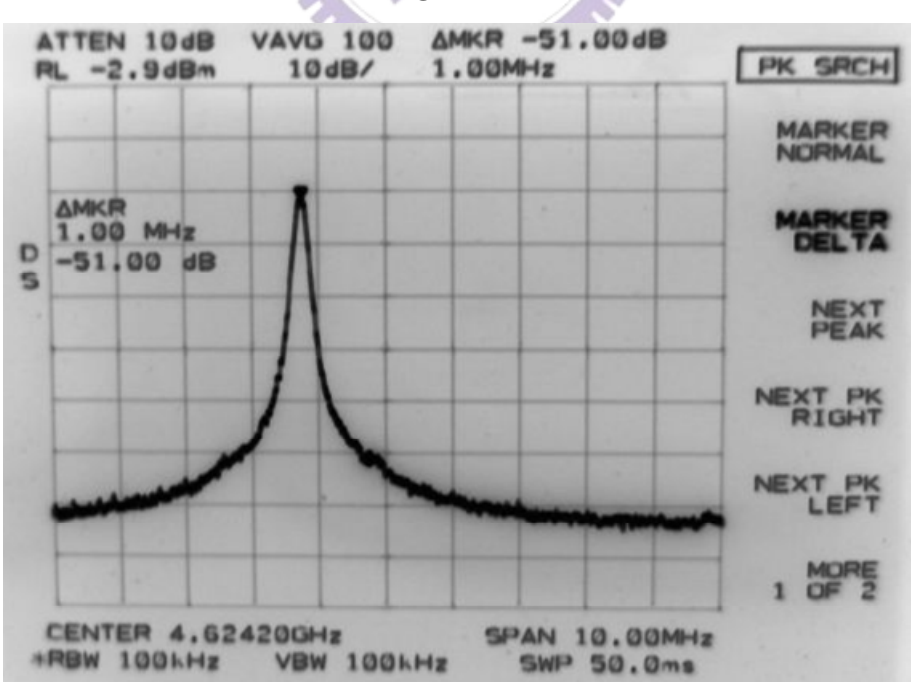


Fig.4-12 8-bits voltage controlled oscillator phase noise measurement result

The tuning range measurement is separated into two parts. First, setting control voltage to 0.9V and measure the VCO tuning range form bank codes 00000000 to 00011111. Fig.4-13 shows the bank code frequency tuning range measurement results V.S. simulation results. In Fig.4-13, the measured frequency tuning curve is down shifted by about 200MHz, since the measured DC current is below SS case. The 8-bits voltage controlled oscillator has linear frequency tuning behavior from 00000000 to 00001000, but breaks down at code 00010000 and 00100000. The nonlinear frequency tuning results from the large size PMOS varactor model isn't correct and process variation.

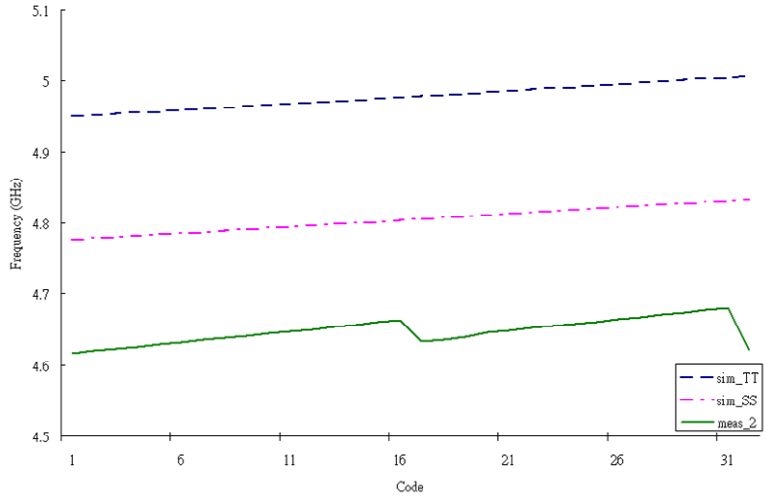


Fig.4-13 Vctr=0.9V, bank code V.S. oscillation frequency

Second part, fix the control voltage to 1.8V, measure the frequency tuning curve of varactor bank code control voltage V.S. oscillation frequency. Fig.4-14 shows the SS corner each bank tuning curve simulation results. The tuning range is binary weighted. Fig.4-15 shows bank 0 to bank 4 tuning range measurement results. Bank 0 to Bank 3 has binary weighted relation. But Bank 4 didn't double Bank 3 tuning range! To examine this problem, we compare the Bank4 to Bank 7 tuning range simulation V.S. measurement results, shown in Fig.4-16 to Fig.4-19, respectively. In Fig.4-17 to Fig.4-19, the measured tuning curve didn't follow the simulation curve anymore.

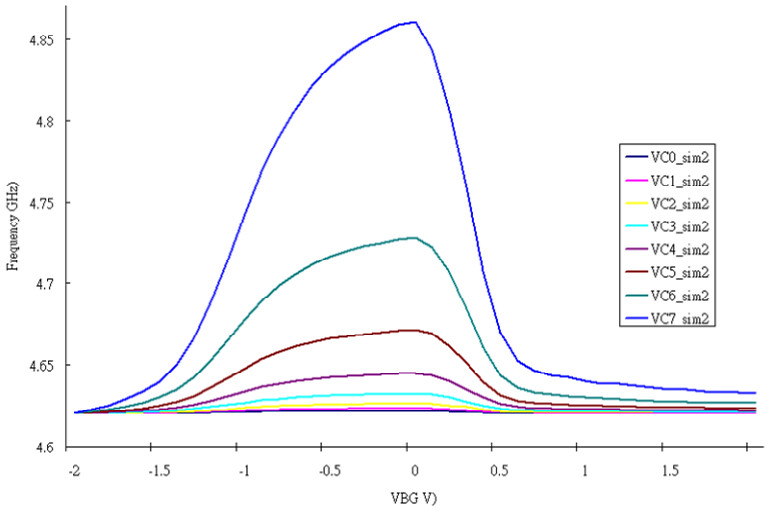


Fig.4-14 Bank tuning range simulation results

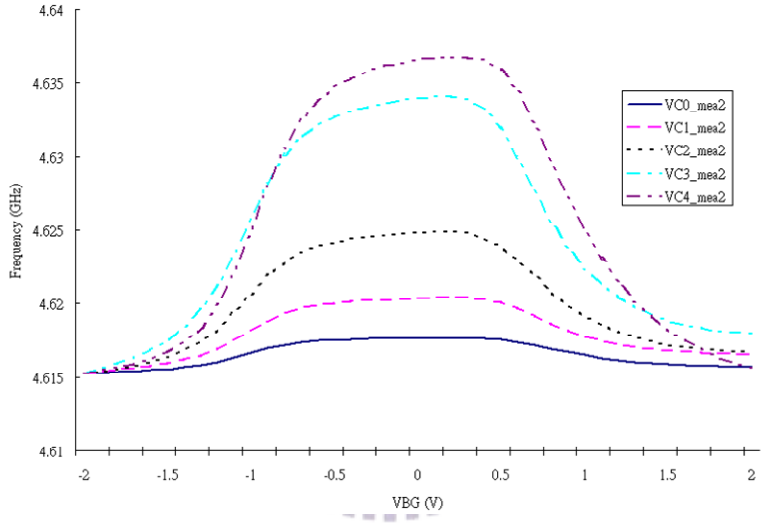


Fig.4-15 Bank tuning range measurement results

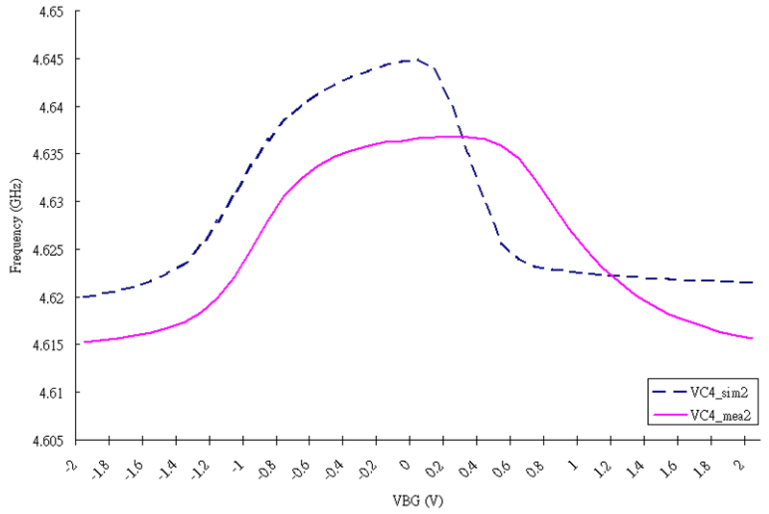


Fig.4-16 Vc4 measured tuning range

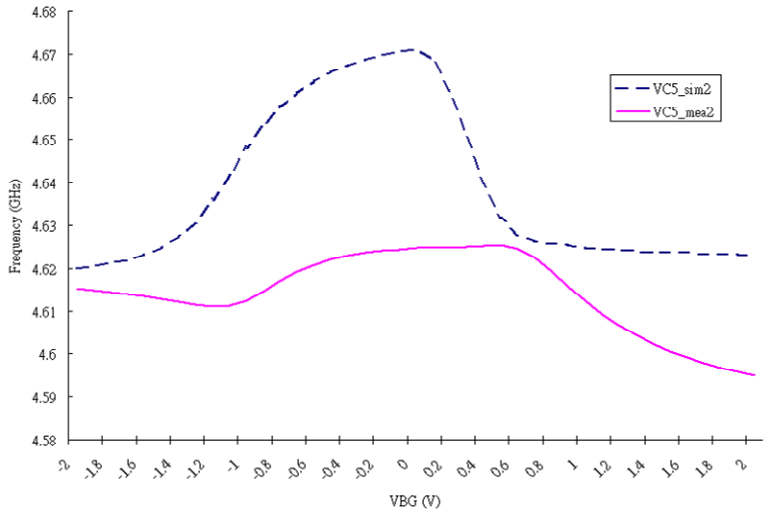


Fig.4-17 Vc5 measured tuning range

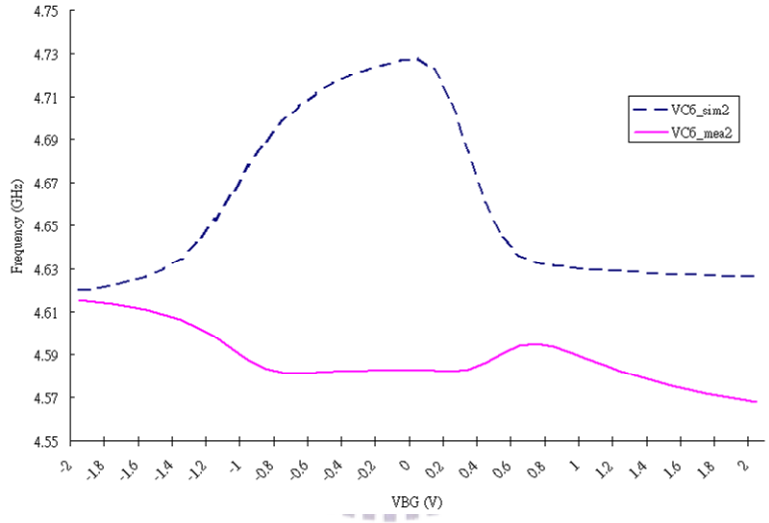


Fig.4-18 Vc6 measured tuning range

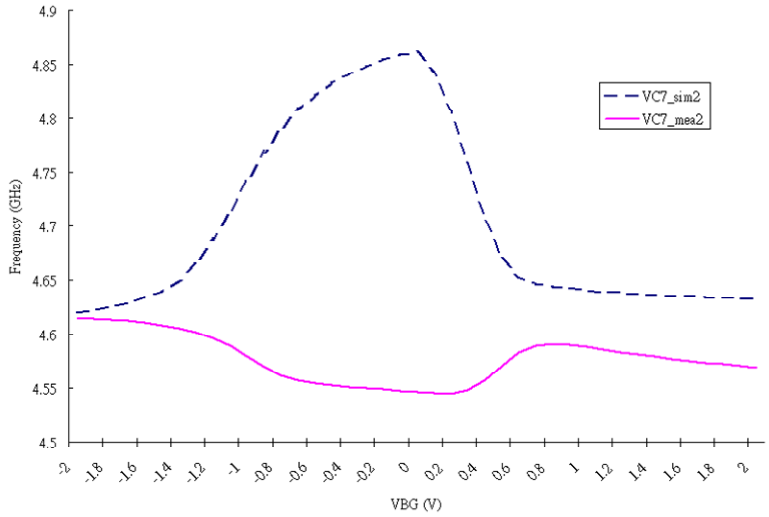
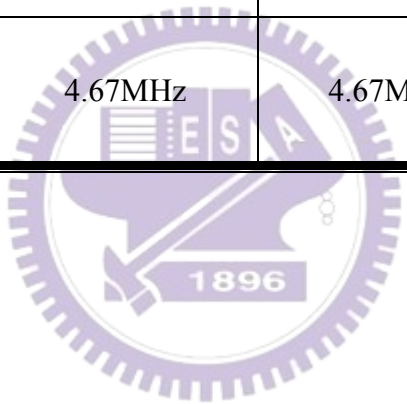


Fig.4-19 Vc7 measured tuning range

We then summary the simulation results in Tab.10.

Tab.10 Measurements summary

Parameter	**TT**	**SS**	**Meas.**
Supply Voltage	1.8V	1.8V	1.8V
DC Current	15.5mA	12mA	9.95mA
Phase Noise @1MHz	-108dBc/Hz	-107dBc/Hz	-101dBc/Hz
Linear Tuning Varactors	8	8	4
Center Frequency	5.24GHz	5.07GHz	4.645GHz
Tuning Range	4.94~5.54GHz	4.77~5.37GHz	4.61~4.68GHz (4 bits)
Average Code Word Tuning Range	4.67MHz	4.67MHz	4.38MHz (4 bits)



4.3.3 Discussion

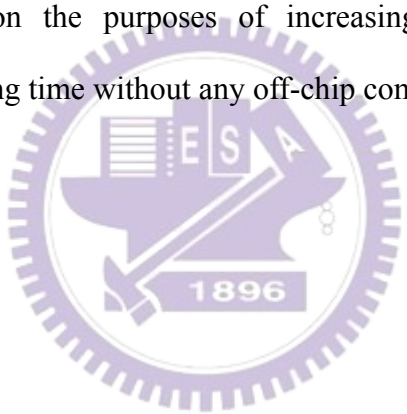
Although this chip is only partial work, some aspects should be noted:

- The process variation is very serious in this work. A DC current 2mA smaller than SS core simulation results makes circuit hardly to oscillate at stable frequency since the -gm value is due to DC current.
- The work shows using varactors to increase frequency resolution is a practical method, since small size varactor tuning is achieved.
- The large size PMOS varactor could be substituted by the MOS_VAR provided by TSMC, since the component is more reliable at high frequency.
- The large size PMOS varactor could be either replaced by MIMCAP switching,

since an On-OFF switching behavior is guaranteed. But the steady oscillation condition should be considered more careful.

4.4 Future Works

The frequency detector reach is still going on. Once a high efficient, accurate frequency detector has been done, this new all-digital frequency synthesizer architecture could be completed. A high speed, high resolution DAC is needed to increase system frequency resolution and settling time. The all-digital frequency synthesizer is designed on the purposes of increasing system integration and shortening frequency settling time without any off-chip comportments.



Chapter 5

Conclusion and Future Work

5.1 Conclusion

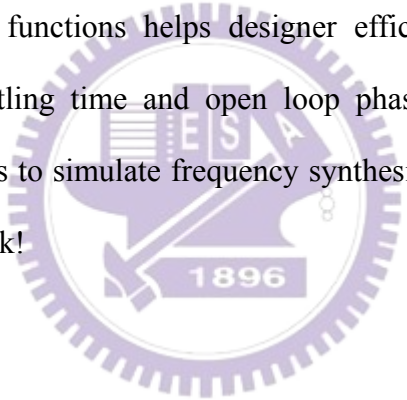
This thesis contents three design works. This first work is high integration multi-bands ΣΔ fraction-N frequency synthesizer in TSMC 0.18μm CMOS. The second work is 802.11a integer-N frequency synthesizer in TSMC 0.25μm CMOS. The third is 8-bit AFC voltage controlled oscillator in TSMC 0.18μm CMOS. All these three circuits have been fabricated through CIC. These circuit design concepts, simulation results, measurement data have been discussed in detail.

5.1.1 High integration quad-bands frequency synthesizer

A novel frequency division technique to integrate multi-band frequency synthesizer circuit design has been discussed in this thesis. This technique reduces chip dimension without scarifying phase noise and frequency resolution performances. The 802.11a/b/g and GSM/DCS1800 quad-bands frequency synthesizers are perfectly combined in single chip. A 12-bit ΣΔ modulator helps increasing frequency resolution to satisfy GSM/DCS1800 200KHz channel bandwidth specification. To further reduce chip area, a register is used to load all digital control bits and voltage controlled oscillator bank control bits. The chip dimension is only 1.61mm2, half the dimension of other compared dual-band frequency synthesizer designs [1][4].

5.1.2 802.11a integer-N frequency synthesizer

In 802.11a application, the integer-N frequency synthesizer architecture is most commonly used. Since the 802.11a channel bandwidth is 20MHz, much higher than other application, the reference can be chosen as high as 10MHz to fasten frequency settling time. In order to lower power consumption, only one dual modulus frequency divider (÷8/9) is used in the work. A pulse-swallow counter is designed to control the dual modulus frequency divider in a period of 32 reference clocks. Reference frequency is 10MHz. Synthesized frequency is from 5.18GHz to 5.34GHz, 20MHz frequency step. Using MATLAB to design loop filter is a practical approach. The MATLAB step and bode functions helps designer efficiently simulate frequency synthesizer close loop settling time and open loop phase margin. The MATLAB program only takes minutes to simulate frequency synthesizer, while ELDO transient analysis takes almost a week!



5.1.3 All-digital frequency synthesizer

We have proposed new all-digital frequency synthesizer architecture. According to the 802.11a frequency tolerance of ±20ppm, at least 14-bit frequency resolution digital frequency resolution can satisfy system specification. The 14-bits are separated in two parts: 8-bit for varactor bank coarse tuning, 6-bit for control voltage fine tuning. Once the designing problem of high efficient frequency detector has been solved, the new frequency synthesizer will promote RF frequency synthesizer integration and frequency settling time. The 8-bit frequency resolution voltage controlled oscillator measurement has been completed. Through this thesis, the research of high frequency

resolution voltage controlled oscillator by using PMOS varactor banks has been proven.

5.2 Future Work

Some aspects need to be improved below:

1. In the quad-bands frequency synthesizer design, the power of quad-bands signals should be increased to above -10dBm for practical telecommunication system. Common drain structure isn't suitable for large output power design, since common drain amplifier is intrinsically a power loss structure. The quad-bands output buffer structure should be modified. Common source output buffer is preferred because it provides power gain rather power loss.
2. The high frequency dividers in quad-bands frequency synthesizer design should be modified to provide more balanced output waveform.
3. In the integer-N frequency synthesizer design, the high frequency divide-by-2 circuit is connected to a buffer. This buffer cause signal voltage swing degradation. This buffer should be removed to increase signal voltage swing.
4. The charge pump in this thesis is a current mismatching circuit. The mismatching current will results in reference spurious noise and distort signal spectrum. A new charge pump structure has been designed and will integrate to frequency synthesizer in future designs.
5. High efficient frequency detector research is going on to complete the new all-digital frequency synthesizer.

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Publication List

1. Kuo-Hua Cheng, Cheng-Hung Chen, Po-Da Chen and Christina F. Jou, “A 20.5-mW, Fast-Switching Integer-N Frequency Synthesizer of 5.2GHz WLANs “, has been accepted by International Symposium on Communications and Information Technologies 2004 (ISCIT 2004), but not published due to economic problem.
2. Cheng-Hung Chen, Wei-Cheng Lien and Christina F. Jou, “A High-Integration, Quad Application Bands ΣΔ Fraction-N Frequency Synthesizer in 0.18-μm Standard CMOS Process”, has been submitted to Asia-Pacific Microwave Conference 2005.