國　立　交　通　大　學

電信工程學系

碩士論文

應用於超寬頻之低雜訊放大器

Low Noise Amplifiers for Ultra-wideband Application

研究生：許志偉

指導教授：張志揚　博士

中華民國　九十四　年　六　月

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摘要

本論文提出適合用於超寬頻的低雜訊放大器。在元件的選擇上，使用由 GCTC 所提供的異質接面雙載子電晶體(heterojunction bipolar transistor, HBT)。電路架構上，則採用達靈頓回授式放大器結構。除了基本架構外，本論文另外提出三種衍生架構：

(1)為節省功率損耗，利用一個基極和集極相接的電晶體取代基本架構中提供偏壓的電阻。

(2)為改善雜訊指數，在輸出級並聯數個電晶體。

(3)為提高增益，直接串接兩個基本架構。

除了理論分析和模擬結果，實際製作出來的電路和量測結果呈現在最後一個章節中。

Low Noise Amplifiers
for Ultra-wideband Application

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Abstract

Low noise amplifiers for ultra-wideband application are presented in this thesis. Darlington feedback topology has been adopted to design a broadband amplifier and demonstrated using heterojunction bipolar transistors (HBT). Except for the basic Darlington feedback topology, three other derivative configurations are introduced in this thesis:

(1) To save the power consumption, a transistor, whose base and collector are connected together, is utilized to substitute the bias resistor.

(2) To improve the noise figure, parallel several transistors at the output stage.

(3) To get higher insertion gain, cascade two basic configurations.

In addition to theoretical analyses and simulation results, the circuits and measurement results are presented in the last chapter.

Acknowledgement

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Chap.1 Introduction

Since Federal Communications Commission (FCC) has approved the ultra-wideband (UWB) radio for commercial applications on February 14, 2002, this relatively new wireless technology, which is originally pursued for military purpose, has been exploited in recent years. Compared to conventional narrow band communication systems, UWB technology spreads the energy of radio signal over a very wide bandwidth, as shown in Fig.1-1.

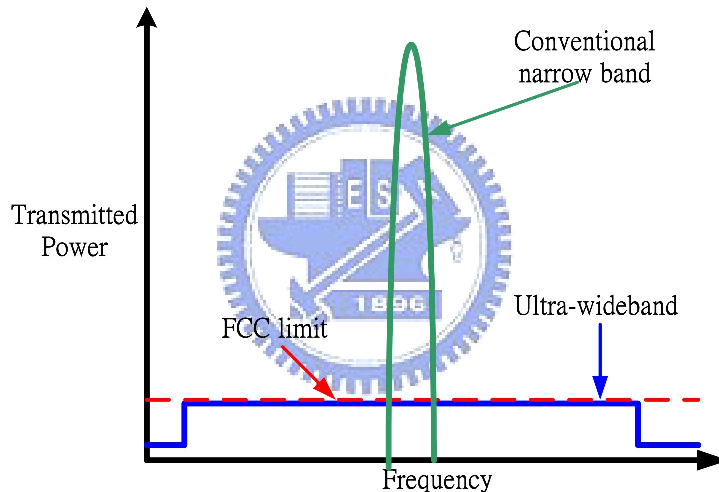

Fig.1-1 Comparison between

Conventional narrow band and Ultra-wideband

According to Shannon's information capacity theorem:

$$\text{data rate} = \text{bandwidth} \times \log_2(SNR) \tag{1.1}$$

Theoretically, data rate increases linearly with the transmission bandwidth. Therefore, UWB technology can provide high data rate at low cost with relatively low power consumption.

The FCC has allocated 7.5GHz of spectrum for unlicensed use of UWB devices

in the 3.1 ~ 10.6 GHz frequency band. Based on this exceptionally large frequency spectrum, UWB technology has attracted a lot of interest from both industries and academia. Since for UWB applications, power spectral density of the transmitted signal is extremely low, it suggests that one of the most critical components in an analog front-end is a broadband amplifier with sufficient gain, low return loss, and as little additional noise as possible. In this thesis, Darlington feedback topology has been adopted to design a broadband amplifier and demonstrated using InGaP/GaAs heterojunction bipolar transistors (HBT).

In the chapter 2, a brief introduction of the HBT devices fabricated by the Global Communication Technology Corporation (GCTC) is presented. In addition, a detailed theoretical analysis of Darlington feedback topology is also described.

The chapter 3 presents the simulation results (by ADS) and layouts. Four types of Darlington feedback amplifier configurations are introduced. The first type is the basic topology using a resistor for biasing, while the second type using a transistor, whose base and collector are connected together, to form an active load. The third type uses several parallel transistors at the output stage of Darlington amplifier to increase insertion gain and lessen noise figure. The fourth type simply cascades two basic topologies to achieve a much higher gain.

The chapter 4 shows the measurement results and conclusions.

Chap.2 Analysis of Darlington feedback amplifiers

2-1 Introduction

The most common approach to design a broadband microwave amplifier in recent years is distributed or traveling-wave amplifier design technique. The basic topology of a distributed amplifier is shown in Fig.2-1.

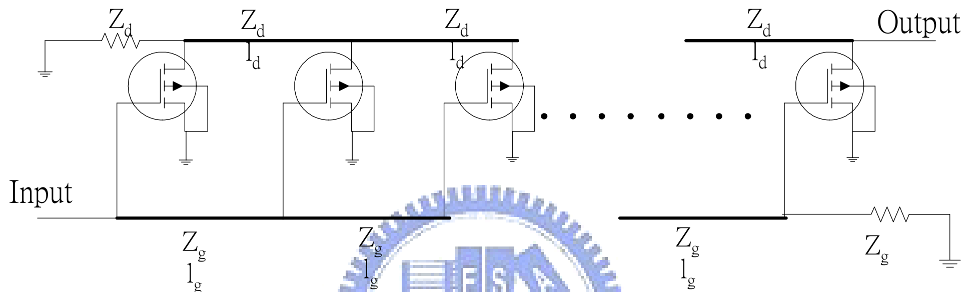

Fig.2-1 Topology of a distributed amplifier

It utilizes several identical transistors having their gates connected to a transmission line of characteristic impedance Z_g, with a spacing of l_g, while their drains connected to a transmission line of characteristic impedance Z_d, with a spacing of l_d. The reason why this configuration can achieve broadband amplification is that these transmission lines can "absorb" parasitic capacitance of devices. However, this method has some drawbacks: large in size, power hungry, and very poor noise figure with a moderate gain.

When HBT devices are designed with distributed amplification technique, there are still some obstacles to overcome because HBT devices have high input capacitance. It mainly comes from the close proximity to the base to the active conducting region. Although high input capacitance leads to high transconductance, it

also limits high frequency performance at the same time. By scaling the device to a small size to get lower input capacitance, the connecting transmission line must incorporate larger unwanted base and emitter resistances, resulting in a very lossy transmission line.

Single-stage direct-coupled configuration reported in the past is well suited for GaAs-based HBT [1], [2]. This topology consists of two Darlington-connected transistors. Negative feedback is achieved by a shunt-shunt resistor connection. This feedback resistor also dominates input and output impedances. As a result, if this resistor is well chosen so that input/output is matched to the system impedance (always 50Ω), excess matching networks are not needed, which eases the complexity of the circuit.

We start with a brief introduction of GCTC HBT devices.

2-2 GCTC HBT devices

HBT technology is an advanced transistor technology for high performance and high frequency applications. The GCTC HBT power process is based on InGaP/GaAs materials. Fig.2-2 illustrates the cross-section of a GCTC HBT.

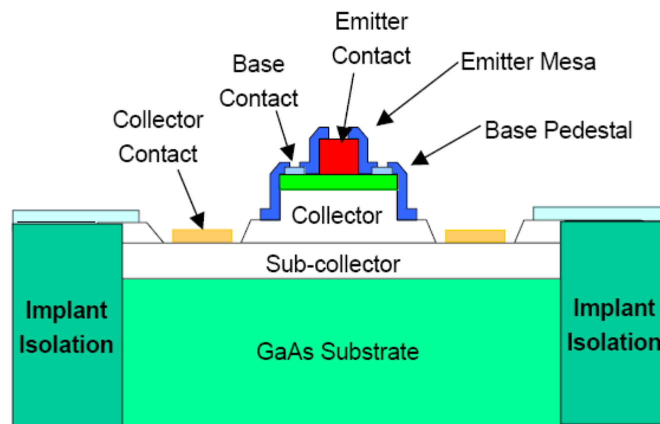

Fig.2-2 Cross-section of HBT

The basic operating physics of GCTC HBT devices is similar to that of silicon BJTs. For NPN type devices, when base-emitter junction is forward biased, electrons are injected from the emitter into the base, thereby allowing charge to flow between the collector and the emitter. The ratio of electron-to-hole injection is called the emitter efficiency, γ, which can be expressed as:

$$\gamma = \frac{n_e v_e}{p_b v_h} \exp(\Delta E_g / kT) \tag{2-1}$$

n_e is the emitter electron doping concentration. v_e is the effective velocity of electrons injected into the base. p_b is the base hole doping concentration. v_h is the corresponding velocity of holes injected into the emitter, and ΔE_g is the difference in bandgaps of emitter and base. The larger value of γ would directly lead to a lager current gain, β.

GaAs-based HBT benefits from a wide bandgap material in the emitter layer, particularly at the emitter-base junction. That means there is some degree of discontinuity in both the conduction and the valence band edges in the junction region, leading to a large value of ΔE_g. According to equation (2-1), this, in turn, allows the base doping to be made quite high without degrading γ. As a result, high base doping concentration makes the GaAs HBT have a very high current gain, a relatively low base resistance, and a high Early voltage.

The high base doping concentration also allows the base region to be made quite thin. This has two important effects: the transit time across the base is very short; and the base transport factor, α_T, is very high, allowing for high operating frequency and increasing the current gain, respectively.

In addition, GCTC power HBT process employs a relatively low collector doping level to further increase the breakdown voltages, BV_{ce} and BV_{cb}.

Some features of a GCTC HBT are listed in Table 2.1 on next page.

Base-emitter turn-on voltage	1.12V
DC current gain (β)	75 (typical)
f_t / f_{max}	35GHz / 55GHz
Breakdown voltage	BV_{ce} > 13V BV_{cb} > 23V

Table 2.1 Performance of GCTC HBT

2-3 Basic Darlington cell

A basic Darlington cell and the corresponding AC currents are shown as Fig.2-3.

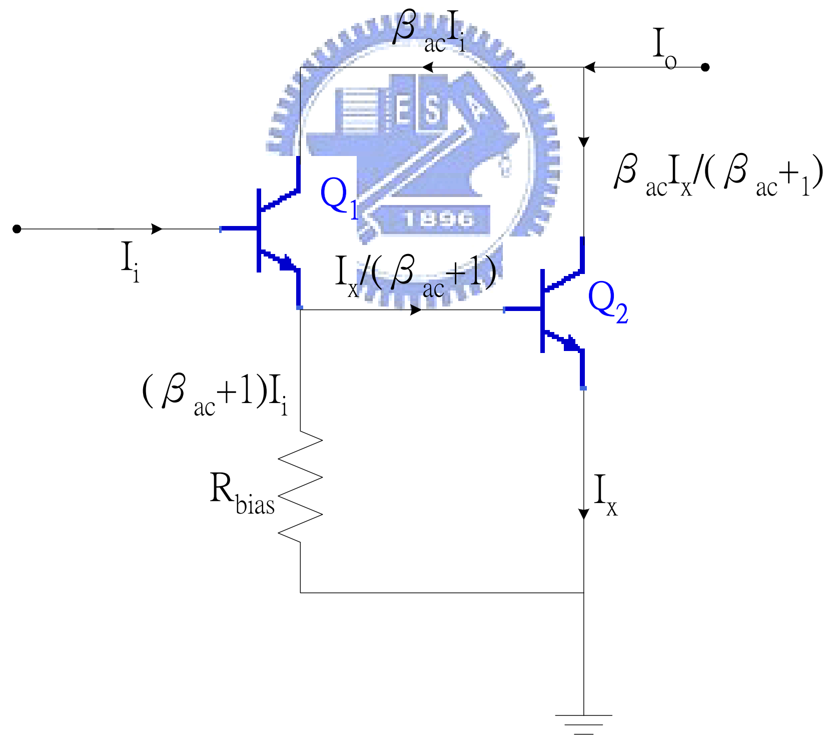

Fig.2-3 Basic Darlington cell

The primary advantage of the Darlington cell is that: an appropriate choice for resistor R_{bias} yields twice the cutoff frequency (f_t) of a single common-emitter configuration. This can be proved as follows.

The low frequency voltage gain of a simple common emitter amplifier is proportional to the ac beta β_{ac} of the transistor. The low frequency ac beta of the transistor can be characterized by a dominant pole approximation given by

$$\beta_{ac}(s) = \frac{\beta_0}{1 + s/\omega_\beta} \tag{2-2}$$

where ω_β is the 3-dB bandwidth of the ac current gain. The cutoff frequency ω_t is related to ω_β,

$$\omega_t = \beta_0 \times \omega_\beta \tag{2-3}$$

From Fig.2-3, the effective ac current gain of the Darlington cell, β_{eff}, can be approximated as

$$\beta_{eff} = \frac{I_o}{I_i} = \beta_{ac} + \beta_{ac}\frac{(\beta_{ac}+1)}{(\beta_{ac}+2)} \approx 2\beta_{ac} \tag{2-4}$$

This equation occurs when the resistor R_{bias} is adjusted so that the ac current through R_{bias} is equal to the ac current in the emitter of Q_2. Under this condition, the Darlington cell can have an effective cutoff frequency of ($2\beta_0 \times \omega_\beta$), which twice that of a single transistor. Therefore, the Darlington cell significantly improves the gain-bandwidth product of the common emitter amplifier topology.

Besides, the Darlington cell also provides larger input impedance. According to the resistance reflection rule, the input impedance looking into the base of Q_1 is

$$R_{in} = (\beta+1)(r_{e1} + R_{bias} \| r_{\pi 2}) \approx (\beta+1)(r_{e1} + R_{bias}) \tag{2-5}$$

Output impedance is approximately ($r_{o1} \| r_{o2}$), where r_{o1} and r_{o2} are the output resistances due to the Early effect. Therefore, both input and output impedances are relatively large compared to 50Ω. How to achieve input and output matching simultaneously will be discussed in next section.

2-4 Input and output matching

Elementary wideband amplifier topologies, such as the common-emitter, always use two methods for input matching: put (1) a shunt input resistor as Fig.2-4 (a) or (2) a common-base transistor at input as Fig.2-4 (b).

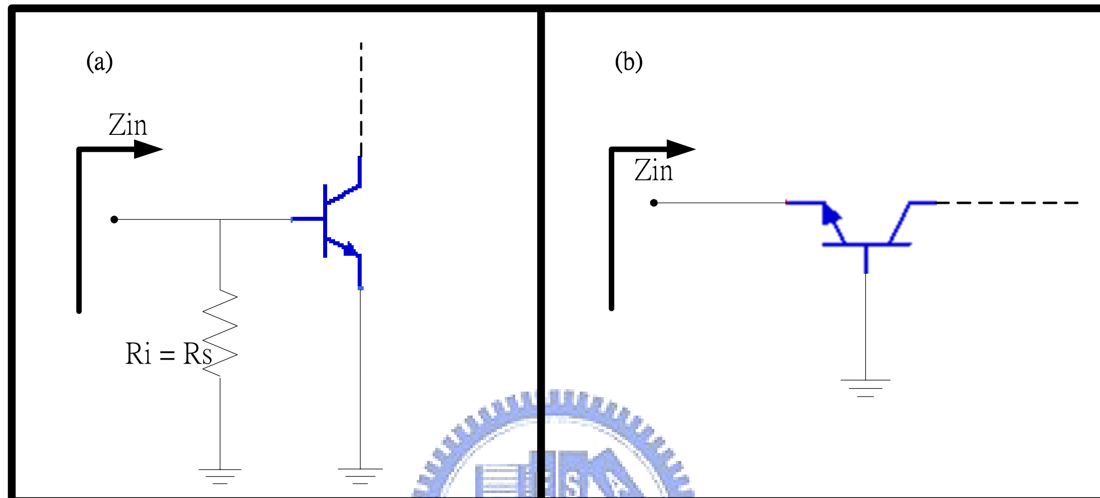

Fig.2-4 (a) A shunt input resistor for input matching

(b) A common-base transistor for input matching

For Fig.2-4 (a), the input impedance looking into the base of a common-emitter transistor is very large compared to 50Ω. It is quite straightforward to put a 50Ω resistor across the input terminals. Unfortunately, this impedance-matching resistor also adds as much equivalent noise as that of the source resistance and produces a very high noise figure.

As for the configuration in Fig.2-4 (b), the resistance looking into the emitter is approximately equal to $1/g_m$, where g_m is the transconductance of the common-base transistor. It follows that a proper choice of the bias current can provide the desired input resistance. However, this bias condition is usually far from the optimum noise figure [3], which means it is also not a suitable approach for input matching.

In contrast with the open-loop architecture, negative feedback can break the trade-off between source impedance match and noise performance. A useful wideband amplifier topology is illustrated as Fig.2-5.

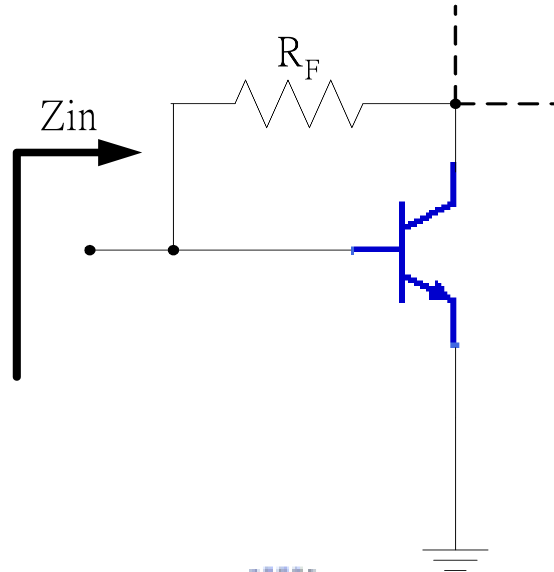

Fig.2-5 A negative feedback resistor for input matching

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A resistor R_F is inserted to provide shunt feedback. The input impedance is given as:

$$R_{in} \approx \frac{R_F}{1 + A\beta} \tag{2-6}$$

where A is the amplifier's open-loop gain and β is the feedback factor. Hence, the feedback resistor R_F becomes the dominant noise source, as well as determines the input impedance. Simple noise analysis shows that the equivalent noise contribution of R_F is (1+Aβ) times smaller than that of source resistance. As a result, theoretically, if the open-looped gain A is sufficient over the operating frequency band, a broadband amplifier with low noise figure and good impedance matching could be achieved.

A Darlington feedback amplifier combines both advantages of a Darlington cell and negative feedback technique. It can be proved the feedback resistor is able to realize both input and output impedance matched to 50Ω.

2-5 Darlington feedback amplifier

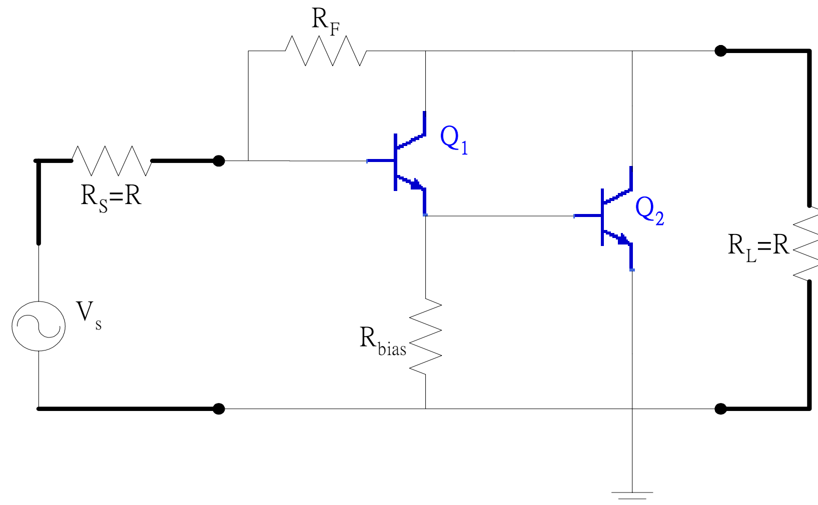

Fig.2-6 Darlington feedback amplifier

A Darlington feedback amplifier with an AC source and terminal impedances is illustrated in Fig.2-6. Some designers also add another resistor at the emitter terminal of Q_2 to introduce negative feedback and improve high frequency response, but also degrade insertion gain at the same time. The following analysis is based on the configuration without this resistor.

At low frequency, Q_1 acts as an emitter follower forcing Q_2 to dominate the effective transconductance of the circuit. Neglect Q_1, the small signal model of Fig.2-6 can be simplified as Fig.2-7.

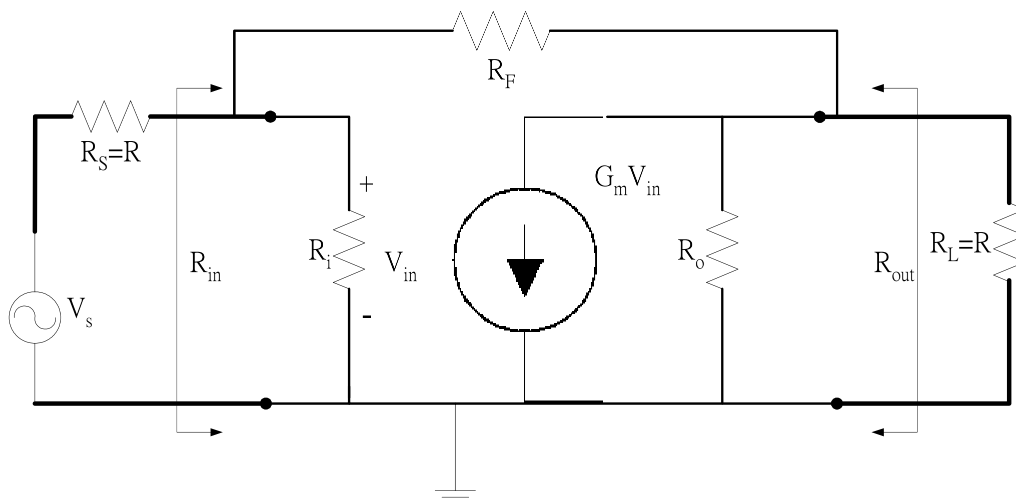

Fig.2-7 Small signal model of Darlington feedback amplifier

System impedances (R_S, R_L) are set to the same value R (always 50Ω). R_i can be obtained from equation (2-5), which is much larger than R. R_o approximates ($r_{o1} \parallel r_{o2}$), which is also a large value with respect to R. G_m is the transconductance of Q_2. Assume the feedback resistor R_F is comparable to R, the input and output impedances (R_{in} and R_{out}) can be expressed as:

$$R_{in} \approx R_{out} \approx \frac{R_F + R}{1 + G_m R} \qquad (2\text{-}7)$$

Setting R_F equal to $\mathbf{G_m R^2}$ will make R_{in} and R_{out} approach system impedance R. Under these matched conditions, the low-frequency voltage gain is the same as the insertion gain S_{21} as:

$$A_v = S_{21} = -(G_m R - 1) \qquad (2\text{-}8)$$

Chap.3 Circuit designs and layouts

3-1 Type I: Basic Darlington amplifier

The design methodology is described in details as follows. We start with an expected insertion gain of **15dB**. According to Equation (2.8) in the previous chapter, the transconductance of Q_2 can be calculated as **132.47mS**. Then, the corresponding bias DC current of Q_2 is about **4 ~ 5mA**. Referring to the design manual provided by GCTC, the best-performance device for this biasing condition is selected. In addition, the feedback resistor is set to G_mR^2, **330Ω**, and the DC bias current of Q_1 is initially set to **1mA.**

The simulation result of this initial guess is shown in Fig.3-1.

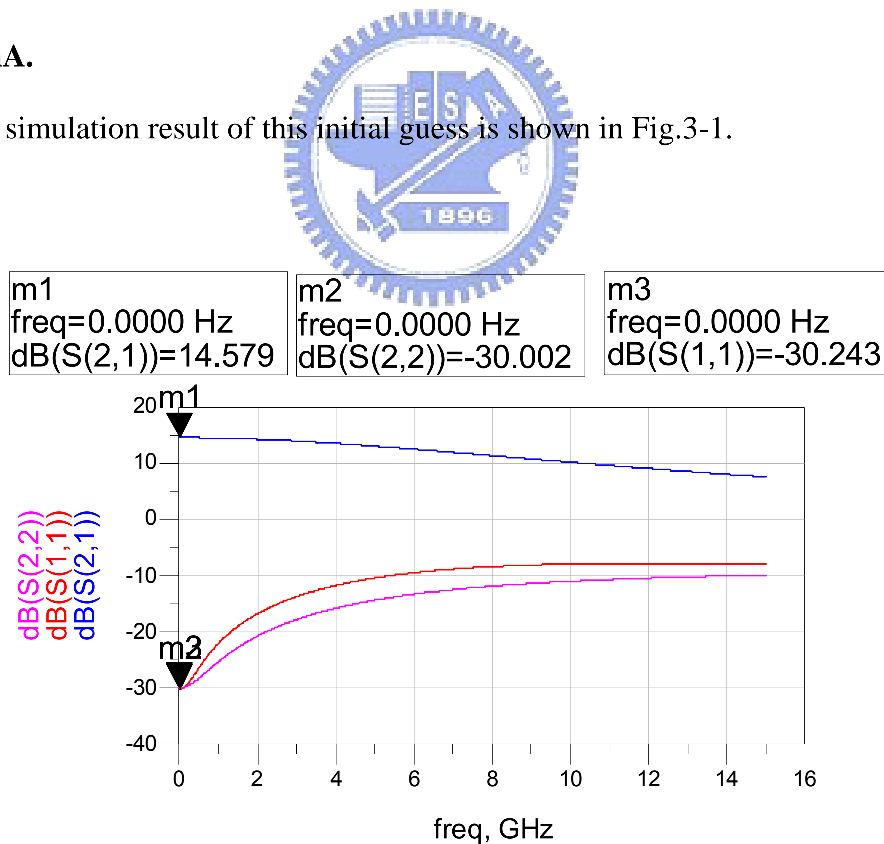

Fig.3-1 Initial guess

In Fig.3-1, at DC condition, the insertion gain is very close to the expected value 15dB. The first emitter follower stage accounts for the slight difference between the expected value (15dB) and the simulation result (14.579dB). Both input and output return losses are about –30dB without matching circuits.

However, since the 3dB-bandwidth is expected to cover 3.1 ~ 10.6GHz (UWB), the values of the bias resistor and the feedback resistor need to be modified. After tuning, the optimal schematic of the circuit is shown in Fig.3-2.

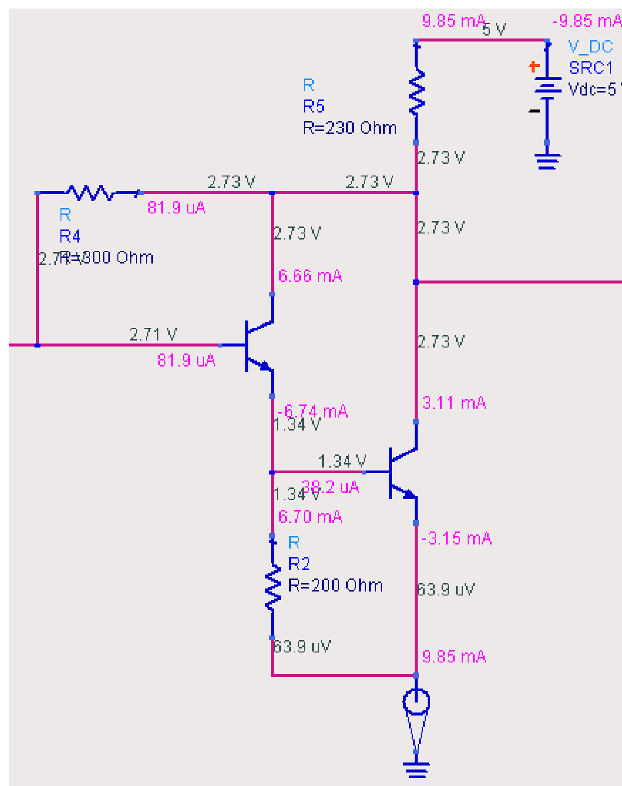

Fig.3-2 Schematic of Type I configuration

In Fig.3-2, the biasing condition is also annotated. The total power consumption is 49.25mW. The DC power supply is set to be a normal value, 5V. A 230Ω resistor, rather than a choke inductor, is used to provide proper biasing conditions for two Darlington connected transistors. It is because: (1) an on-chip inductor will occupy a very large area, and (2) the 230Ω resistor, which introduces much less noise than the 300Ω feedback resistor, has little influence on the noise performance.

The simulation result is illustrated in Fig.3-3.

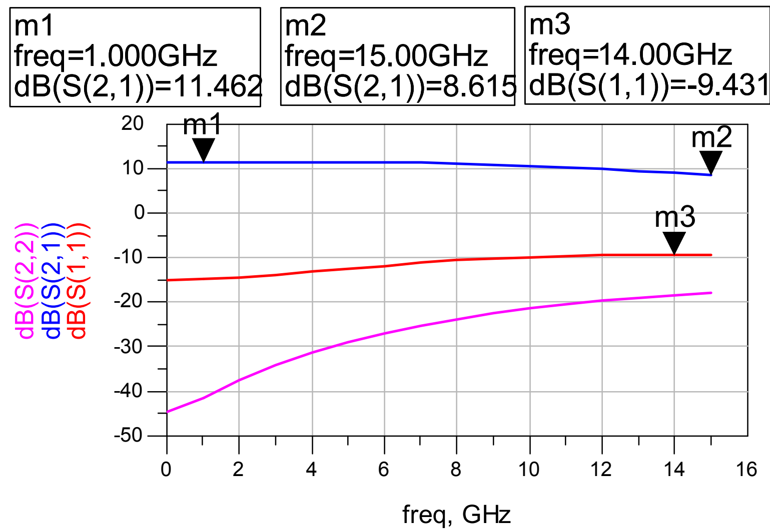

Fig.3-3 Simulation result of Type I configuration

After setting the current through Q_1 to 6.66mA, the insertion gain is much flatter and the 3-dB bandwidth is extended to about 15GHz. The output return loss is less than –15dB, and the input return loss degrades to about –9.5dB in 10 ~ 15GHz.

The noise figure is listed in Fig.3-4.

freq	NFmin	nf(2)
0.0000 Hz	4.769	5.278
1.000GHz	4.797	5.298
2.000GHz	4.881	5.355
3.000GHz	5.014	5.449
4.000GHz	5.188	5.575
5.000GHz	5.393	5.729
6.000GHz	5.620	5.906
7.000GHz	5.863	6.100
8.000GHz	6.113	6.308
9.000GHz	6.366	6.525
10.00GHz	6.619	6.747
11.00GHz	6.868	6.970
12.00GHz	7.112	7.192
13.00GHz	7.348	7.412
14.00GHz	7.577	7.626
15.00GHz	7.797	7.835

Fig.3-4 Noise figure of Type I configuration

According to the simulation results, this configuration has two obvious drawbacks: relatively large power consumption and poor noise figure. The following two sections provide some methods for improving of these drawbacks.

3-2 Type II: Darlington amplifier with an active load

As mentioned in the previous section, the basic configuration consumes a lot of power. In this section, a transistor where its base and collector are connected substitutes the 200Ω resistor. The schematic circuit with corresponding biasing condition is shown in Fig.3-5.

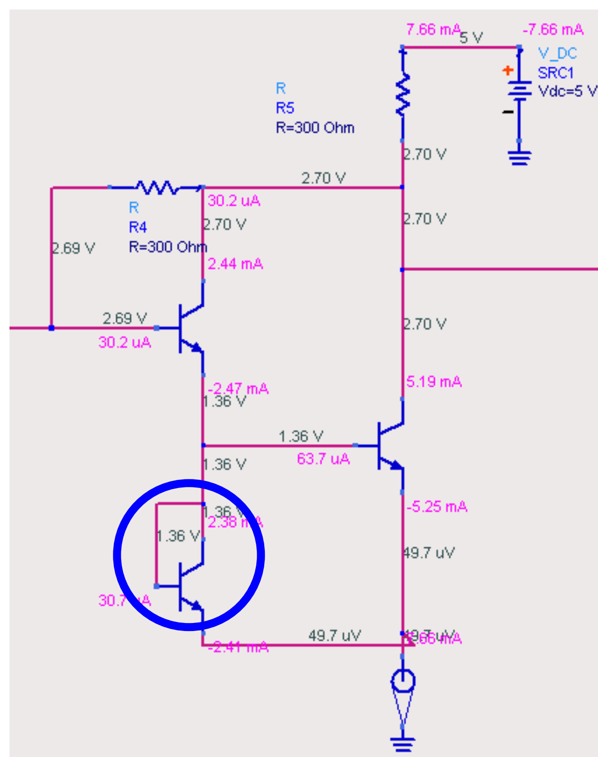

Fig.3-5 Schematic of Type II configuration

The simulation result and noise figure are shown in Fig.3-6 and Fig.3-7, respectively.

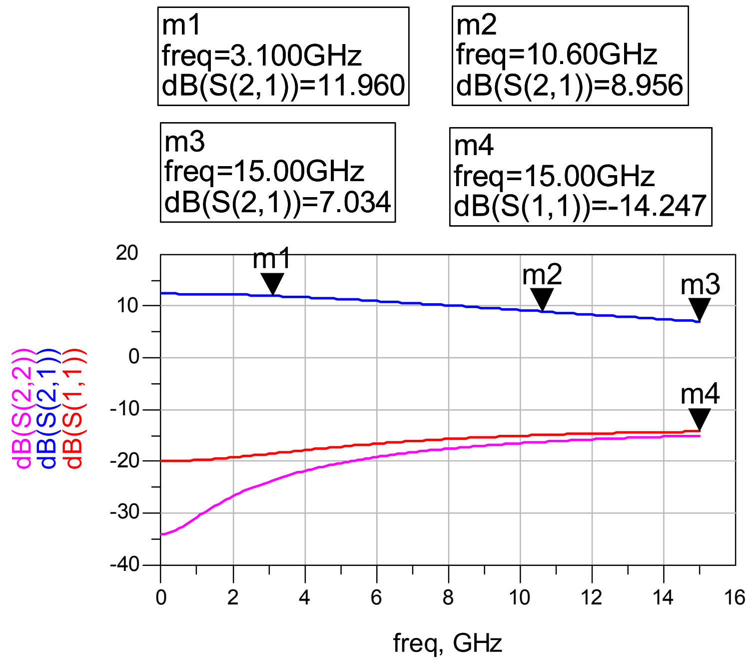

Fig.3-6 Simulation result of Type II configuration

freq	NFmin	nf(2)
0.0000 Hz	5.147	6.014
1.000GHz	5.173	6.028
2.000GHz	5.249	6.069
3.000GHz	5.366	6.135
4.000GHz	5.514	6.220
5.000GHz	5.681	6.322
6.000GHz	5.859	6.435
7.000GHz	6.042	6.556
8.000GHz	6.223	6.683
9.000GHz	6.402	6.813
10.00GHz	6.577	6.944
11.00GHz	6.747	7.077
12.00GHz	6.912	7.211
13.00GHz	7.072	7.345
14.00GHz	7.229	7.478
15.00GHz	7.382	7.612

Fig.3-7 Noise figure of Type II configuration

This configuration consumes 38.3mW, which saves almost 25% power compared with the basic type. Nevertheless, the flatness of insertion gain is heavily influenced, and the 3-dB bandwidth shrinks to about 10GHz. In 3.1 ~ 10.6GHz frequency band,

the average insertion gain is still about 10.5dB, and the noise figure is similarly poor.

3-3 Type III: Darlington amplifier with parallel output stage

As mentioned in the previous sections, the biasing condition of Q_2 (the output stage) dominates the insertion gain while that of Q_1 (the first stage) influences the flatness. In this section, the DC current through Q_2 is equalized to several parallel transistors. Considering the magnitude and the flatness of insertion gain, the number of these parallel transistors should be carefully selected. After the observation, the number is set to be three, and the schematic circuit is shown in Fig.3-8

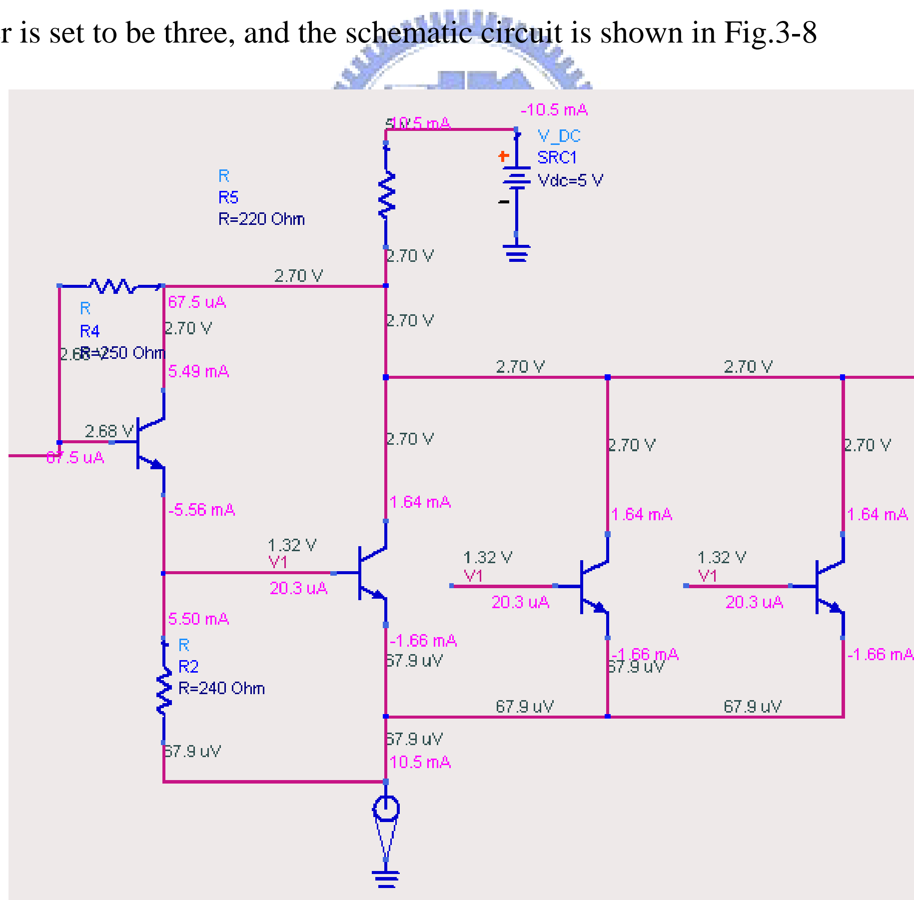

Fig.3-8 Schematic of Type III configuration

The simulation result and noise figure are in Fig.3-9 and Fig.3-10, respectively.

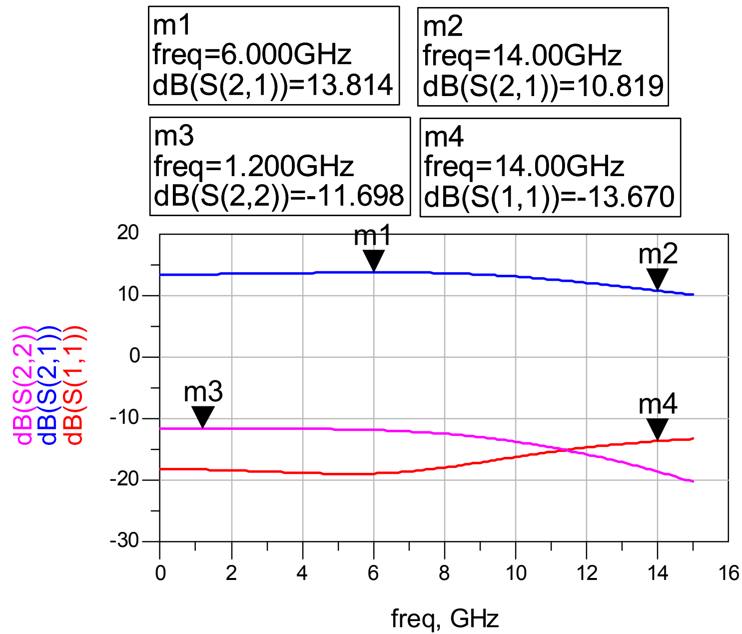

Fig.3-9 Simulation result of Type III configuration

freq	NFmin	nf(2)
0.0000 Hz	4.198	4.441
1.000GHz	4.215	4.454
2.000GHz	4.266	4.494
3.000GHz	4.348	4.559
4.000GHz	4.459	4.649
5.000GHz	4.592	4.759
6.000GHz	4.745	4.889
7.000GHz	4.914	5.035
8.000GHz	5.093	5.195
9.000GHz	5.281	5.366
10.00GHz	5.474	5.546
11.00GHz	5.670	5.731
12.00GHz	5.867	5.921
13.00GHz	6.064	6.113
14.00GHz	6.260	6.305
15.00GHz	6.453	6.498

Fig.3-10 Noise figure of Type III configuration

The insertion gain increases about 2dB with comparable power consumption and

both input and output return loss maintain below –10dB.

The noise figure of Darlington feedback structure is relatively high (reported 5-6dB at 10GHz in [1]), because that feedback resistor unavoidably introduces the input noise to the output. Besides, noises coming from devices also should be considered. In Type III configuration, paralleling these transistors is equivalent to paralleling these corresponding noise sources, leading to a smaller noise source and indirectly improving the noise figure. Compare Fig.3-10 with Fig.3-4, paralleling three transistors at the output stage improves the noise figure of about 1dB.

3-4 Type IV: Cascade Darlington amplifier

This configuration simply cascades two Darlington amplifiers. Since both input and output are well matched to 50Ω, two Darlington feedback amplifiers are connected directly. The schematic is shown in Fig.3-11.

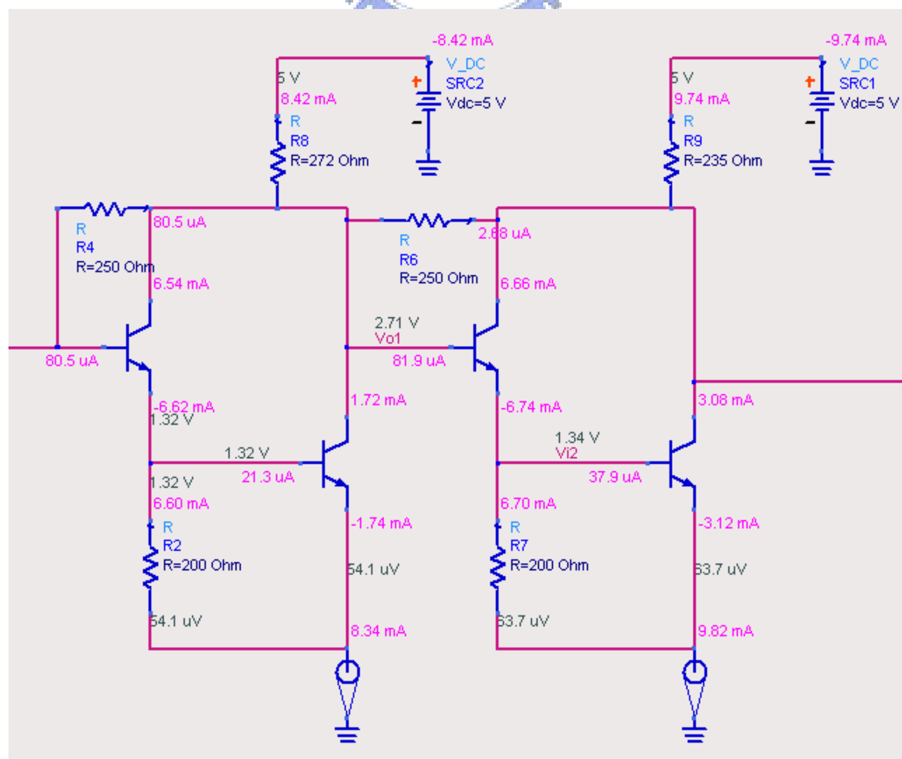

Fig.3-11 Schematic of Type IV configuration

The simulation result and the noise figure are in Fig.3-12 and Fig.3-13, respectively.

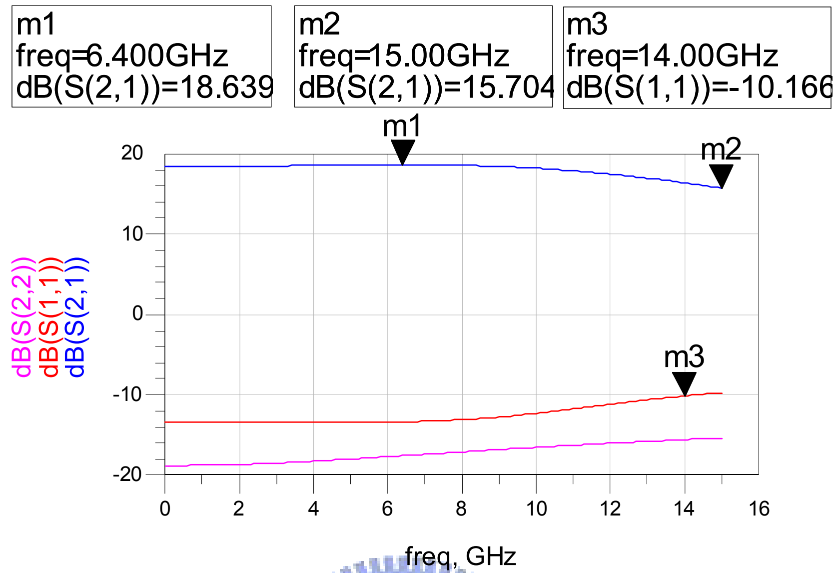

Fig.3-12 Simulation result of Type IV configuration

freq	NFmin	nf(2)
0.0000 Hz	5.975	6.355
1.000GHz	5.999	6.374
2.000GHz	6.069	6.430
3.000GHz	6.182	6.522
4.000GHz	6.331	6.644
5.000GHz	6.509	6.793
6.000GHz	6.710	6.963
7.000GHz	6.926	7.151
8.000GHz	7.153	7.351
9.000GHz	7.386	7.560
10.00GHz	7.623	7.775
11.00GHz	7.861	7.994
12.00GHz	8.098	8.215
13.00GHz	8.334	8.437
14.00GHz	8.568	8.660
15.00GHz	8.800	8.883

Fig.3-13 Noise figure of Type IV configuration

These two feedback resistors are set to be 250Ω as considering of the flatness of the insertion gain. Two biasing resistors are also fine tuned and optimized. The noise

figure degrades about 1dB than that of a single-stage one. Power consumption is almost twice while insertion gain boosts up of about 5dB.

3-5 Layouts

The layout of a HBT device is shown in Fig.3-14.

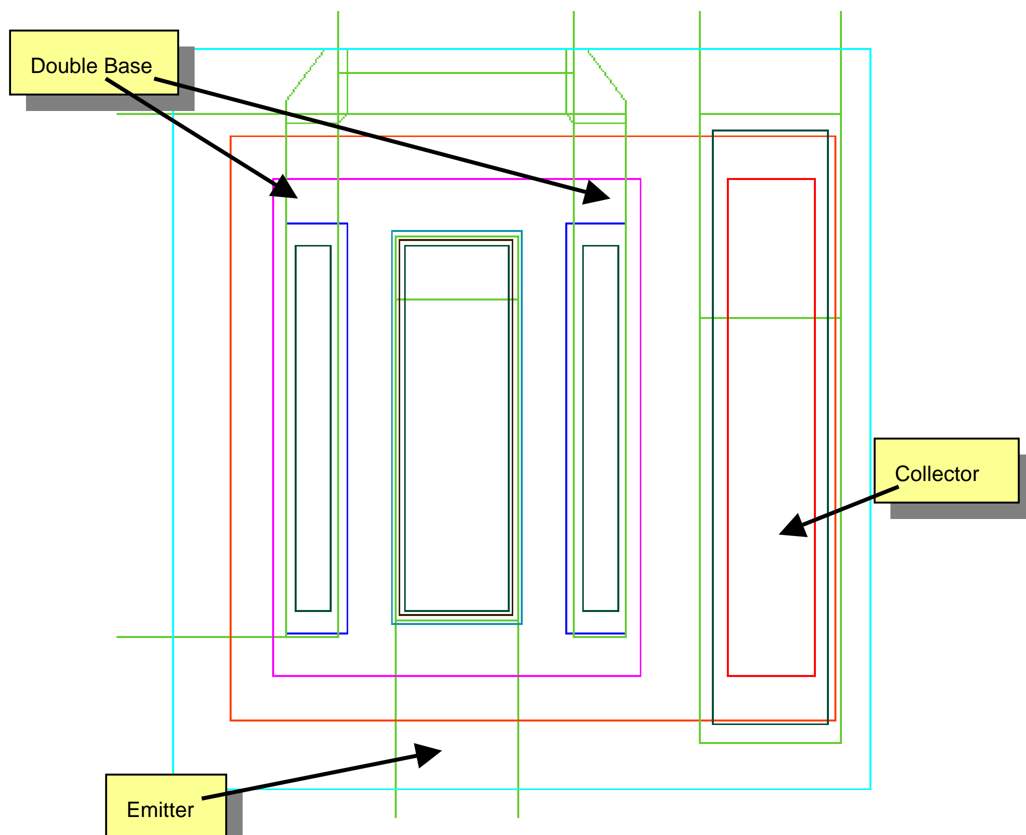

Fig.3-14 Layout of a single HBT device

Metal 1 is used to interconnect the primary circuit elements. A length of metal could be considered as a microstrip line with substrate thickness of 100µm and dielectric constant of 12.9 ($\varepsilon_r = 12.9$ for GaAs). The width of a 50Ω microstrip line is about 73 µm. Since the width of base (about 20 μm) is much smaller than 73 µm, a "stepwise" layout, as shown in Fig.3-15 on next page, is used to feed the RF signals.

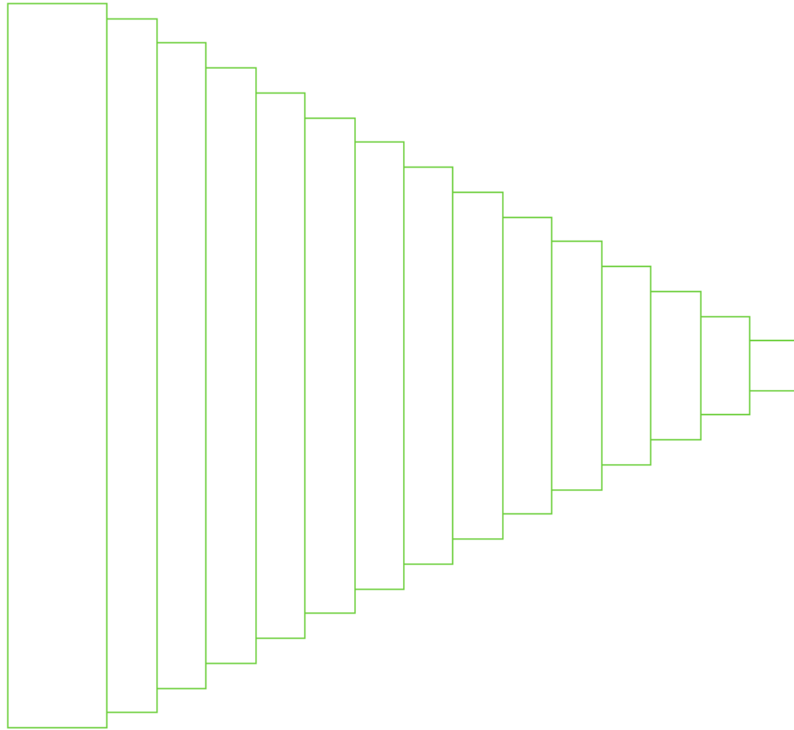

Fig.3-15 Layout of an AC feeding structure

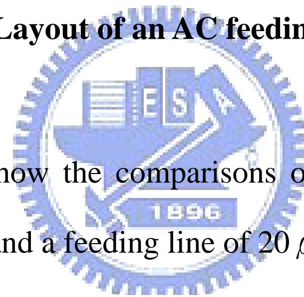

Fig.3-16 and Fig.3-17 show the comparisons of insertion loss and return loss between a stepwise structure and a feeding line of 20 μm in width.

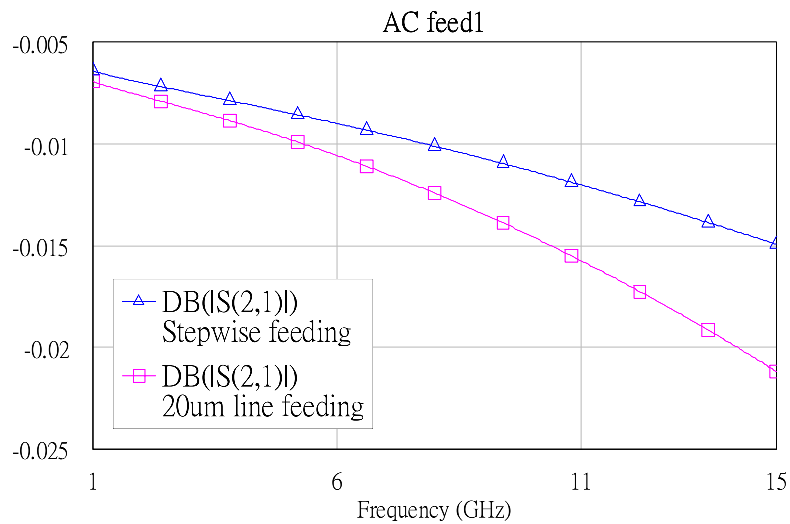

Fig.3-16 Comparison of insertion loss

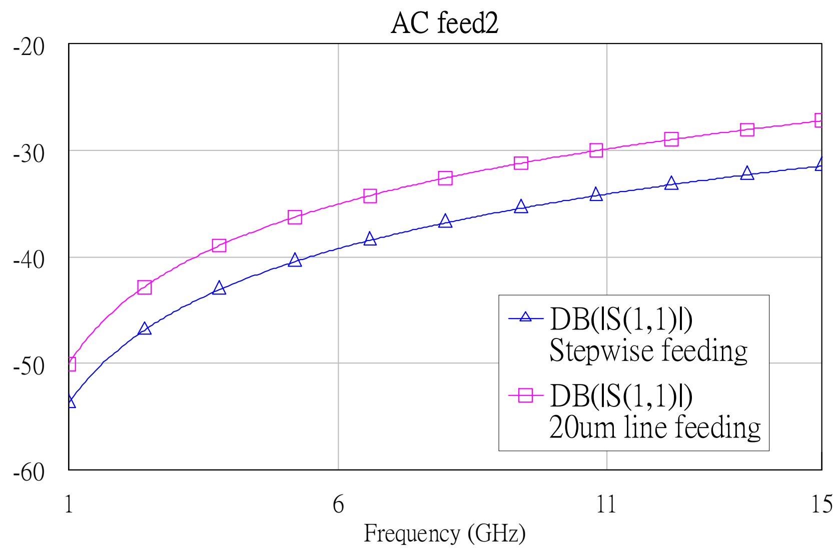

Fig.3-17 Comparison of return loss

It is obvious that a stepwise structure ("△" dots) provides lower insertion loss and better return loss.

There is another important issue: current density. It governs the sizes of interconnecting metals and thin film resistors. The table below lists some relative design rules.

	Metal 1	Metal 2	Thin film resistor
Min. width	2 μm	2 μm	1.4 μm
Min. spacing	2 μm	2 μm	2 μm
Max. current density	3mA/ μm of width	5mA/ μm of width	1mA/ μm of width
Sheet resistance			50Ω/square

Table 3-1 Design rules

According to Table 3-1 and DC currents annotated in the schematics of four configurations, the sizes of resistors and interconnecting metal can be decided. The layout of Type I configuration is shown in Fig.3-18.

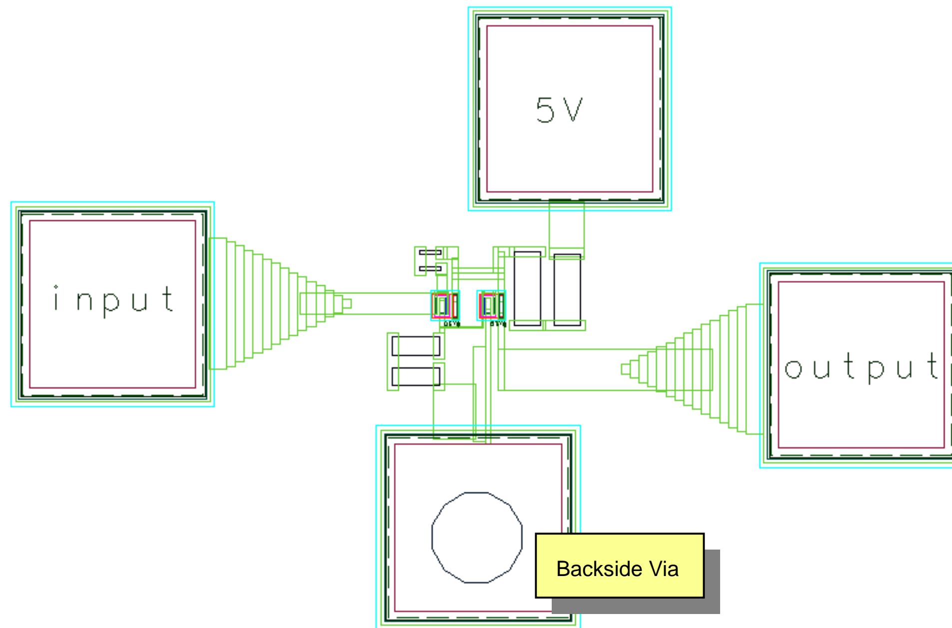

Fig.3-18 Layout of Type I configuration

Fig. 3-19 shows the enlarged view of central part of Fig. 3-18.

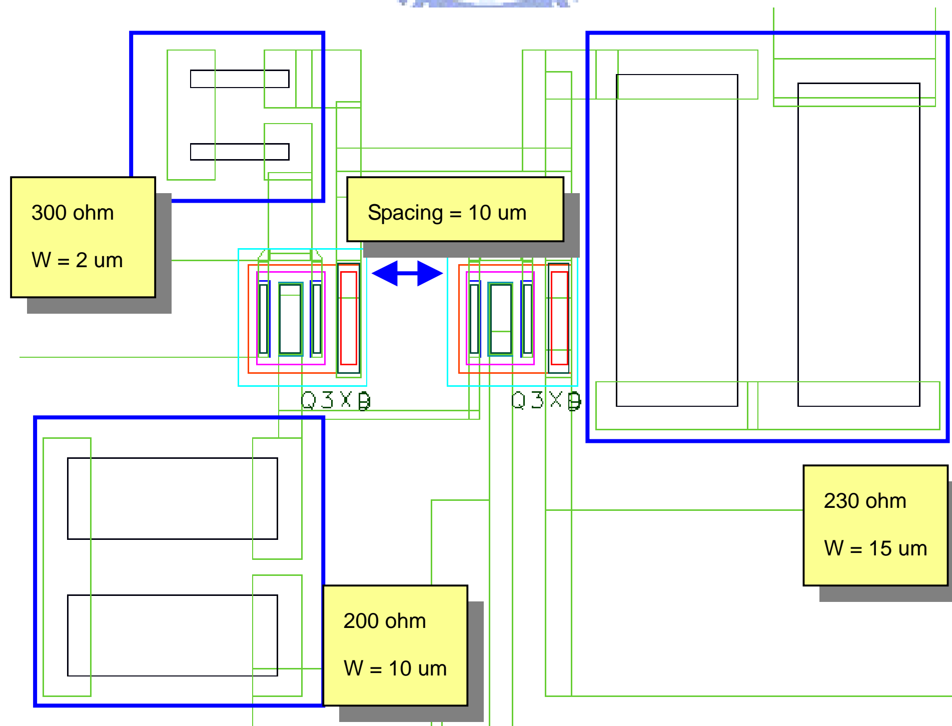

Fig.3-19 Central part of Type I configuration

In Fig.3-18, the backside via provides electrical contact between metals and the ground plane. The distance between the central part and the backside pad is 20 μm, which is a little longer than the minimum space, 15 μm. The spacing between two HBT devices is kept to be 10 μm. The widths (in μm) of thin film resistors are chosen to handle 1.5 times (in mA) of the corresponding DC currents.

The overall layout of Type II configuration is shown in Fig.3-20 and the central part is zoomed in Fig.3-21.

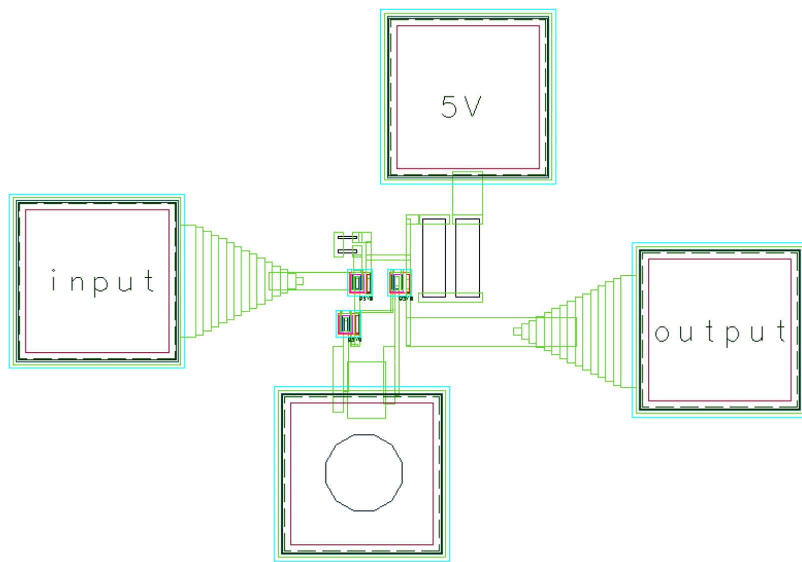

Fig.3-20 Layout of Type II configuration

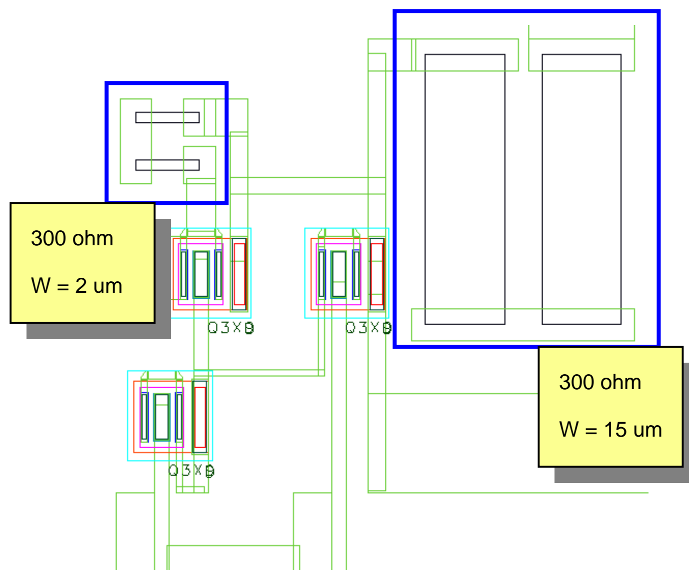

Fig.3-21 Central part of Type II configuration

The overall layout of Type III structure is shown in Fig.3-22 and the central part is zoomed in Fig.3-23.

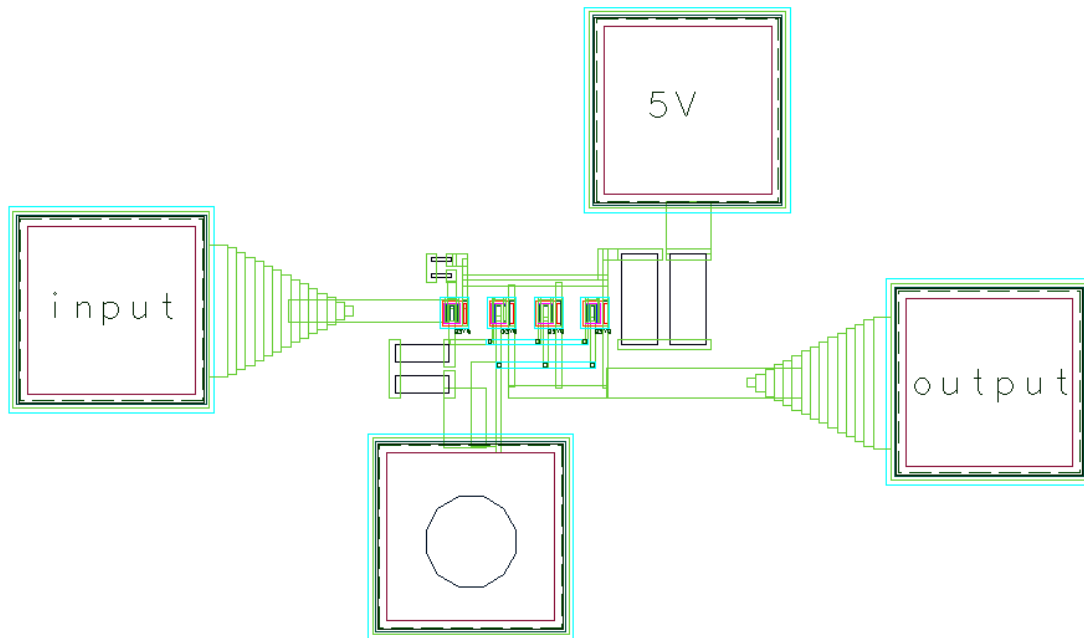

Fig.3-22 Layout of Type III configuration

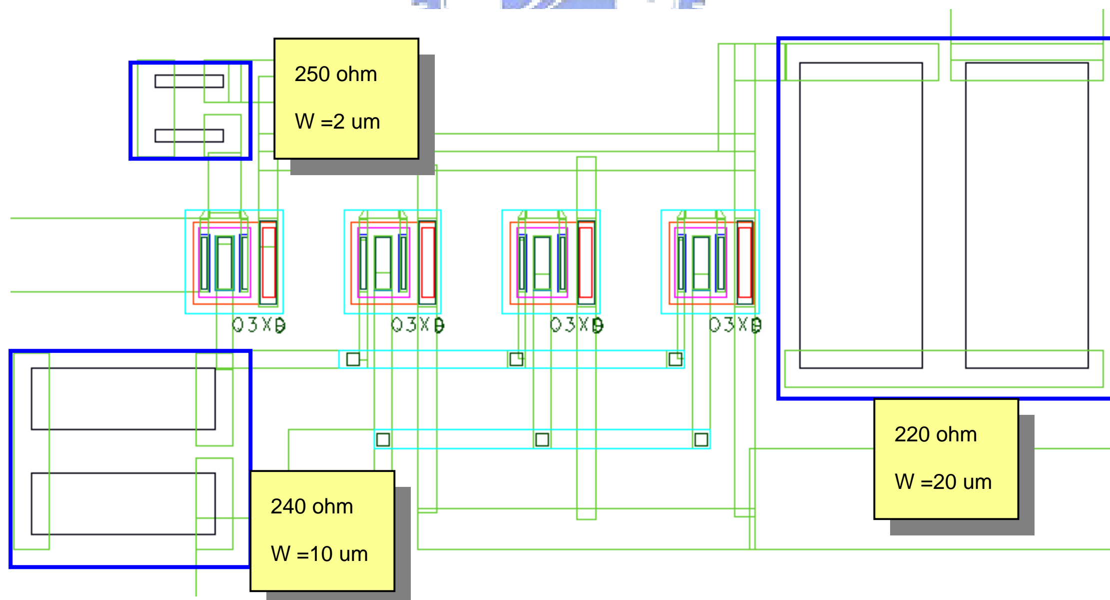

Fig.3-23 Central part of Type III configuration

The bases and emitters of three transistors are connected together through silicon nitride vias between metal 1 and metal 2. A more detailed view is shown in Fig.3-24 on next page.

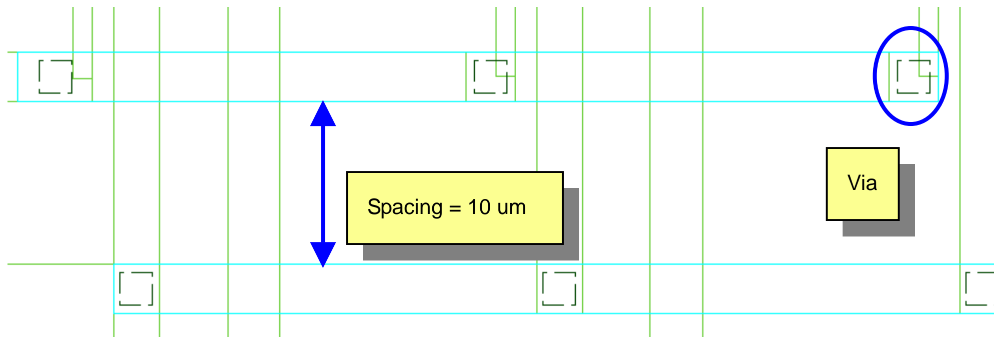

Fig.3-24 Metal 1 and Metal 2

The sizes of vias are set to minimum (1.6 μm × 1.6 μm). The widths of two parallel metal 2 are both 3 μm, and the spacing is 10 μm. The relatively large spacing (compared with line width) can avoid unwanted coupling and feedback effects.

The Type I, II, III configurations occupies no more than **550 μm × 350 μm** of chip area.

The overall layout of Type IV structure is shown in Fig.3-25 and the central part is zoomed in Fig.3-26.

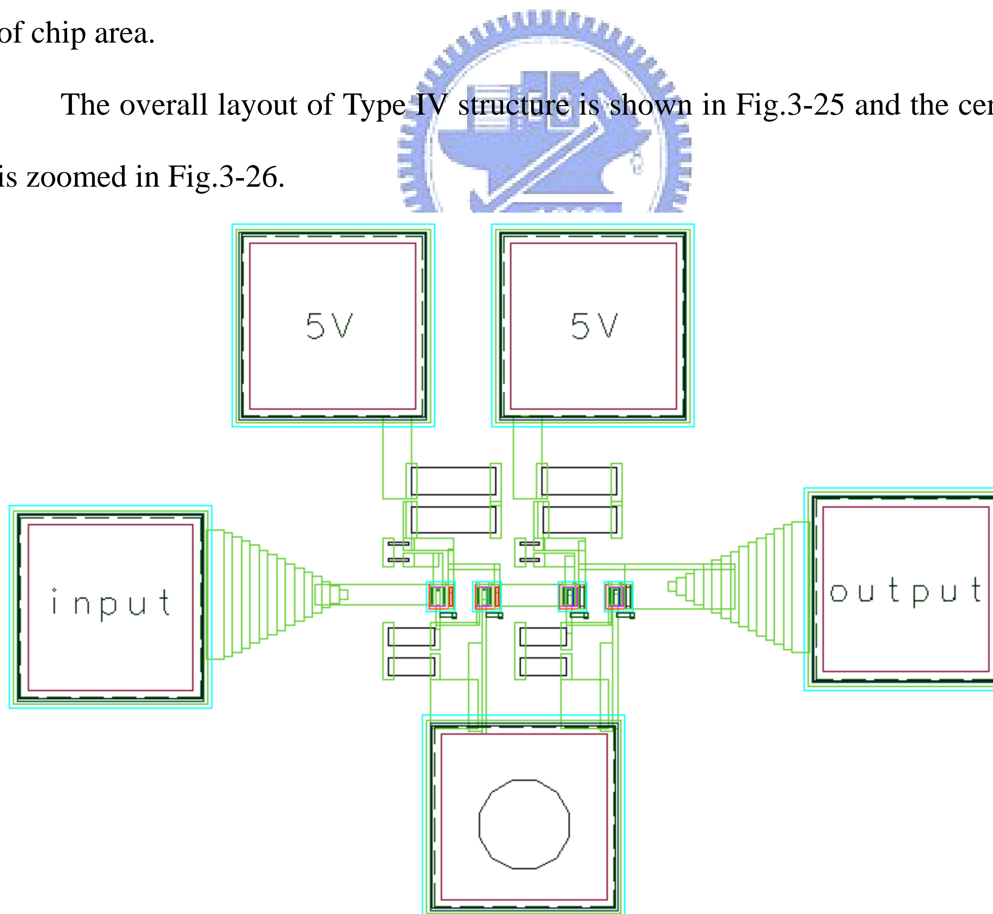

Fig.3-25 Layout of Type IV configuration

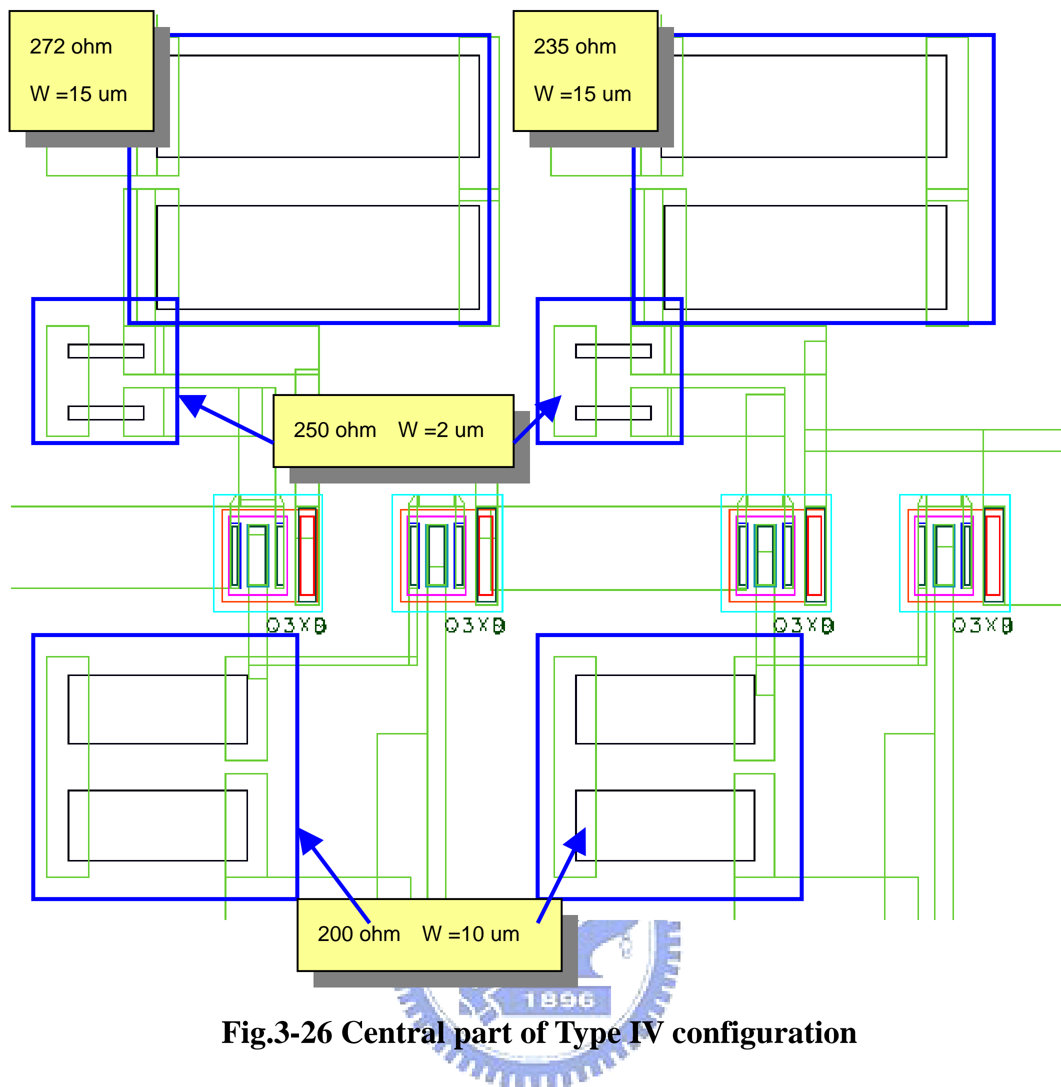

Fig.3-26 Central part of Type IV configuration

3-6 Modified simulation results

The arrangement of layouts will significantly influence measurement results, especially the emitter-to-ground metals. These connecting metals can be approximately equivalent to inductors. It is known that ground inductors definitely have great effects on the stability and high frequency performance. As a result, these metals must be taken into account.

An EM simulator (Sonnet9.52) is utilized to simulate ground metals and then export to a ".sp file". These files are used to modify ordinary simulation results. For example, reconsider Type I configuration. After the layout is fixed, the ground metal

is drawn (by Sonnet9.52) as Fig.3-27.

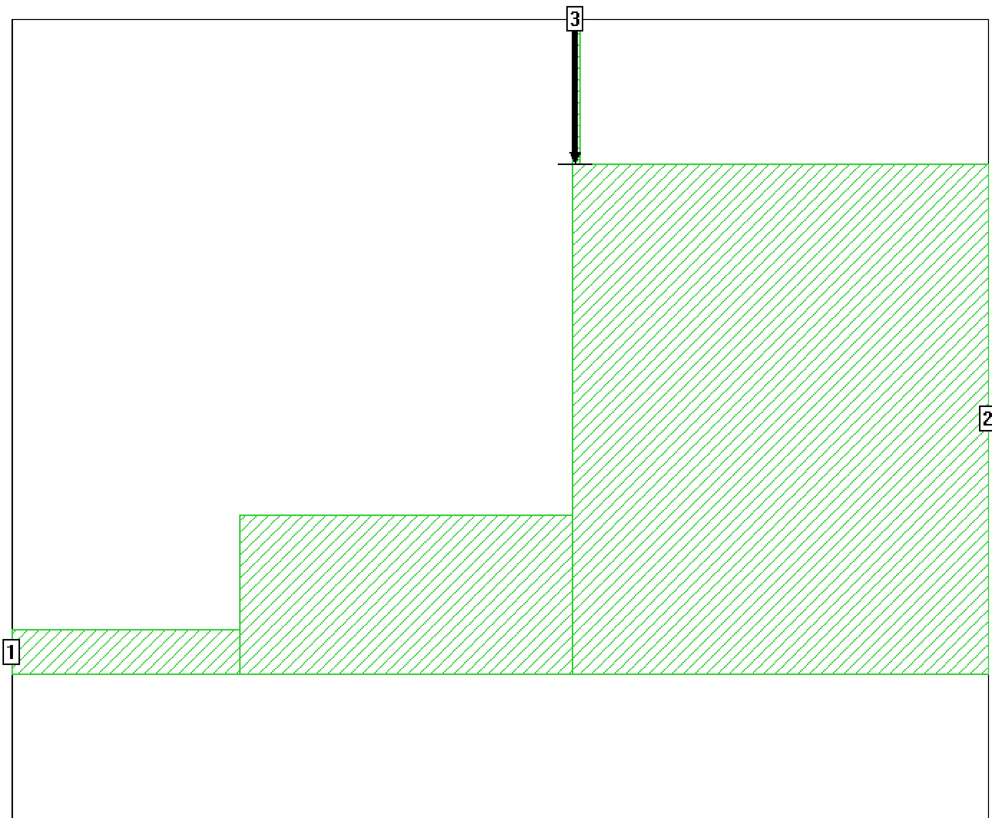

Fig.3-27 Ground metal drawn by Sonnet9.52

The practical ground metal is shown in Fig.3-28.

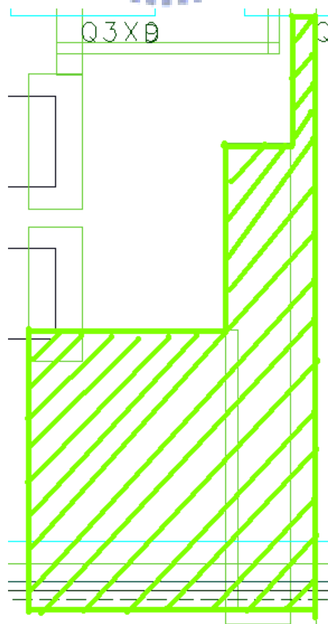

Fig.3-28 Practical ground metal

Compare Fig.3-27 with Fig.3-28, Port 1 connects the emitter of the output stage

transistor. Port 2 corresponds the ground pad, and Port 3 de-embeds to the joint of the biasing resistor. Since the thickness of metal 1 is much greater than the upper dielectric layer (silicon nitride), the "Thick Metal" model provided by Sonnet9.52 is utilized for a more precise simulation results.

After including the ground metal effect (as in Fig.3-29), the modified simulation result of Type I configuration is shown in Fig.3-30.

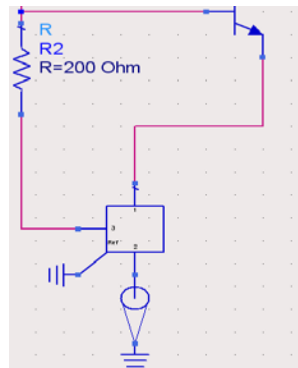

Fig.3-29 Schematic with ground metal model

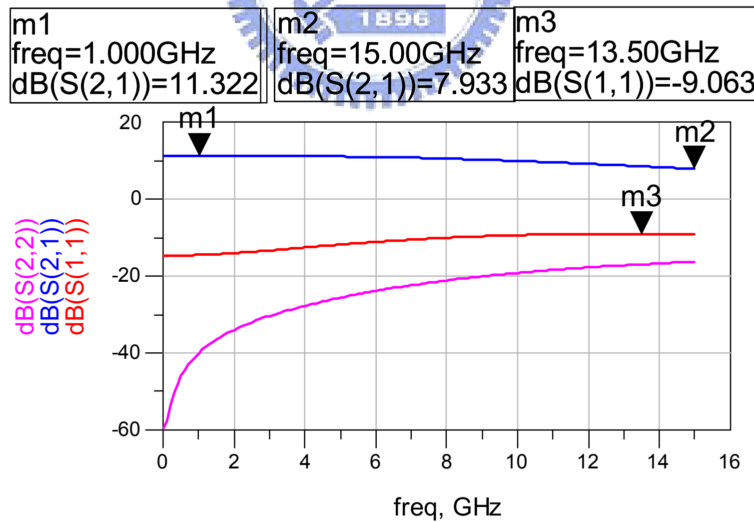

Fig.3-30 Modified simulation result of Type I configuration

Compare Fig.3-30 with Fig.3-3, it is almost the same at low frequency while insertion gain reduces about 0.6dB at high frequency, leading to the shrinkage of 3dB bandwidth.

Similarly, Fig.3-31, Fig.3-32, and Fig.3-33 show the modified simulation results of Type II, Type III, and Type IV configurations.

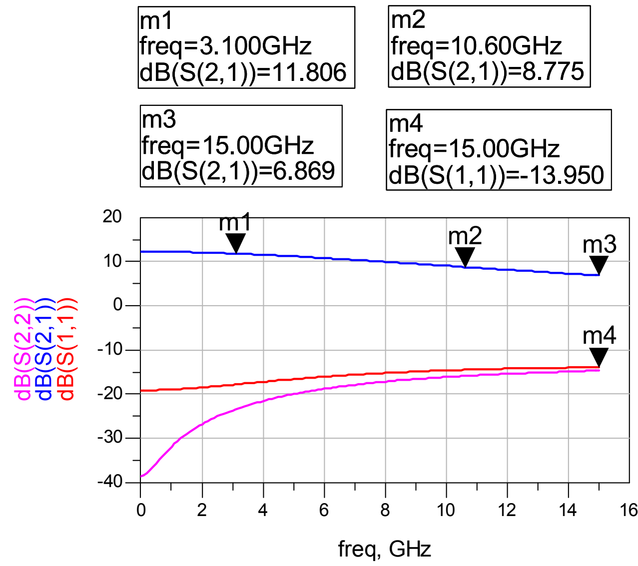

Fig.3-31 Modified simulation result of Type II configuration

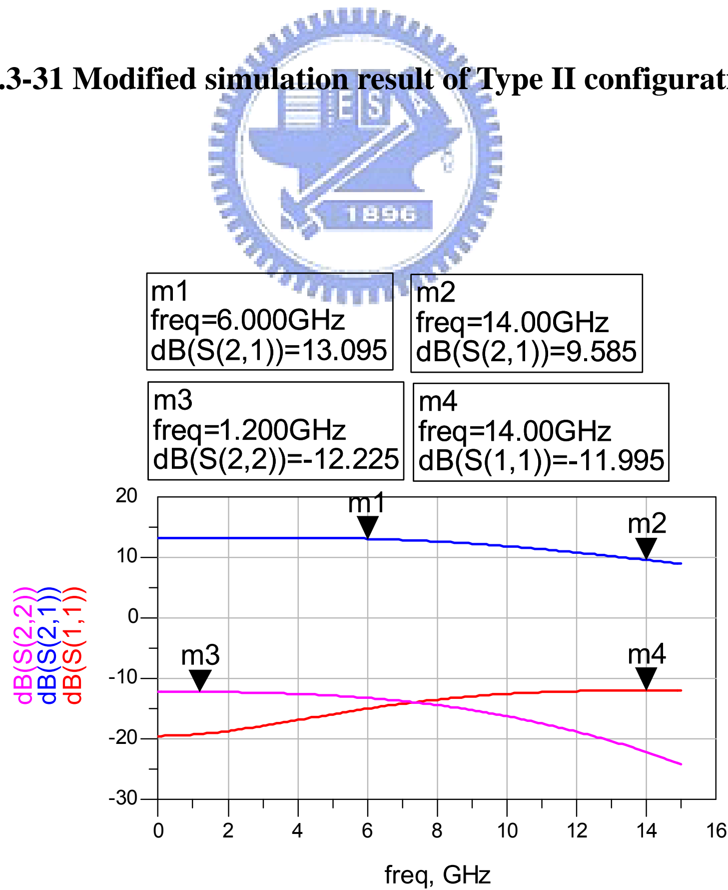

Fig.3-32 Modified simulation result of Type III configuration

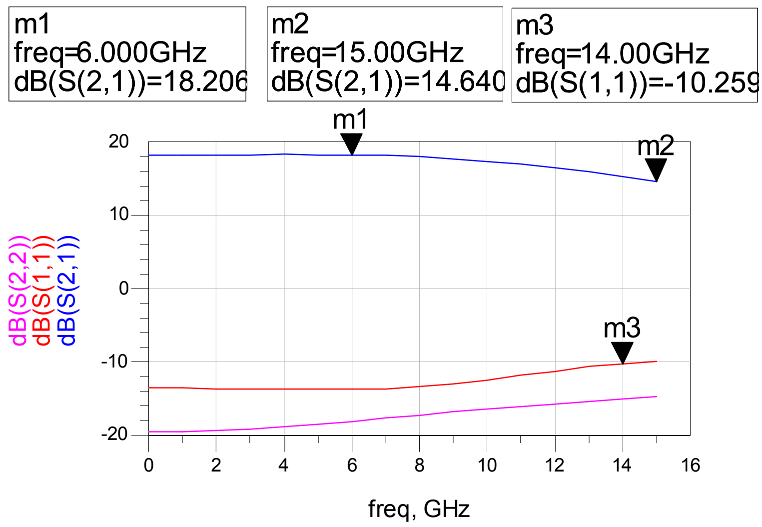

Fig.3-33 Modified simulation result of Type IV configuration

Chap.4 Measurement results and conclusions

A photograph of a circuit is shown in Fig.4-1.

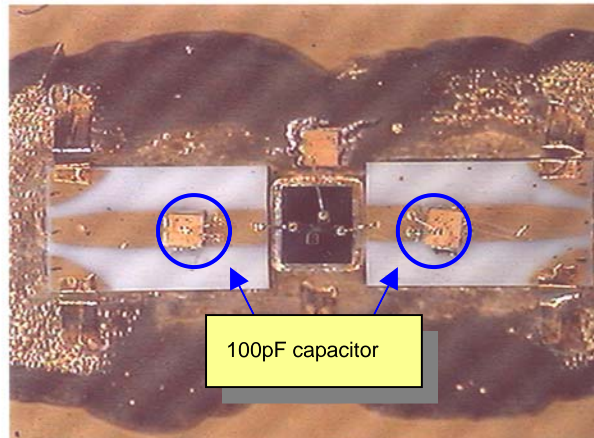

Fig.4-1 Photograph of the circuit

Two 100pF capacitors are added at the input and output feeding lines.

The S-parameters and noise figures of these four configurations are presented in Fig.4-2, Fig.4-3, Fig.4-4 and Fig.4-5, Fig.4-6, respectively.

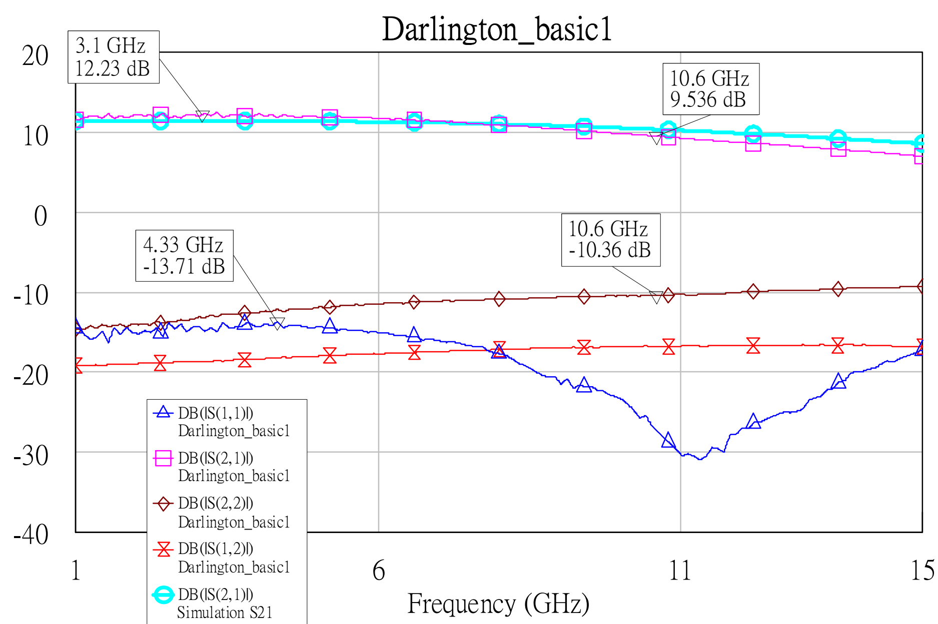

Fig.4-2 S-parameter of Type I configuration

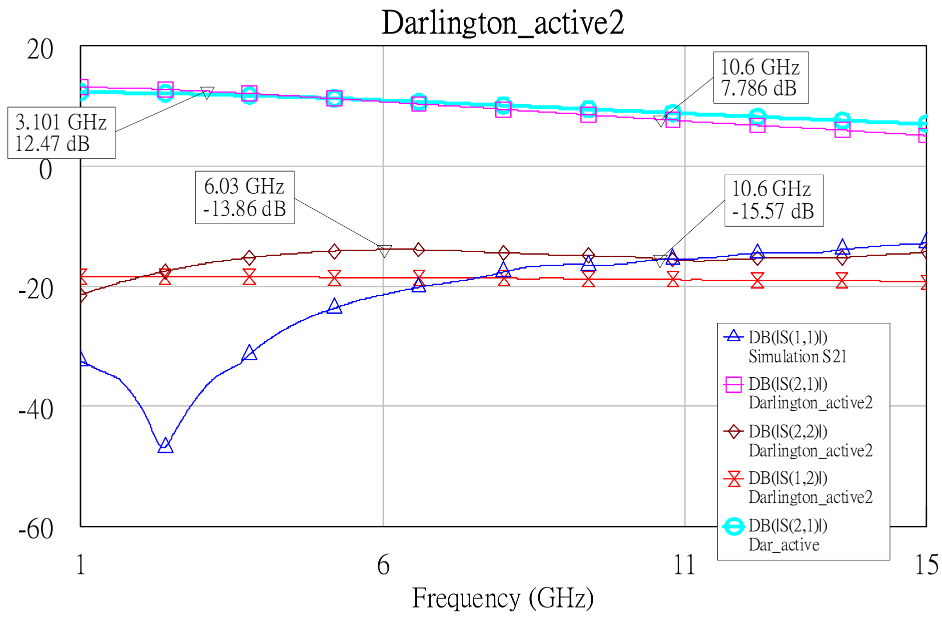

Fig.4-3 S-parameter of Type II configuration

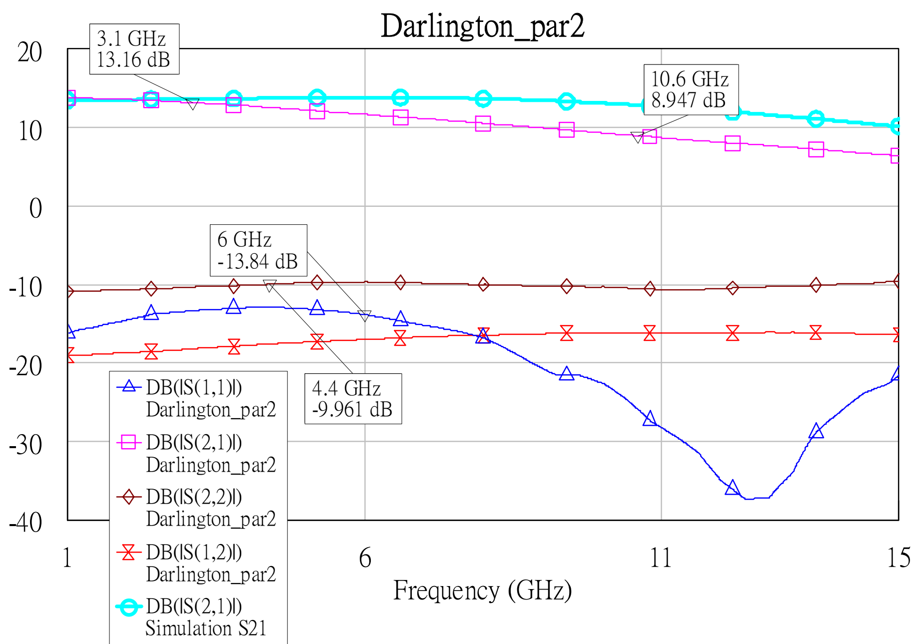

Fig.4-4 S-parameter of Type III configuration

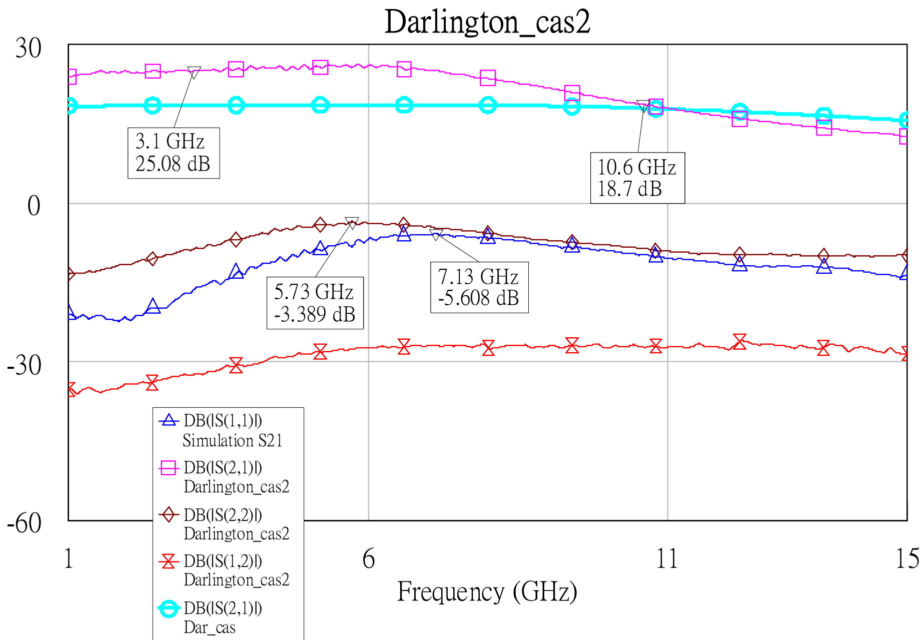

Fig.4-5 S-parameter of Type IV configuration

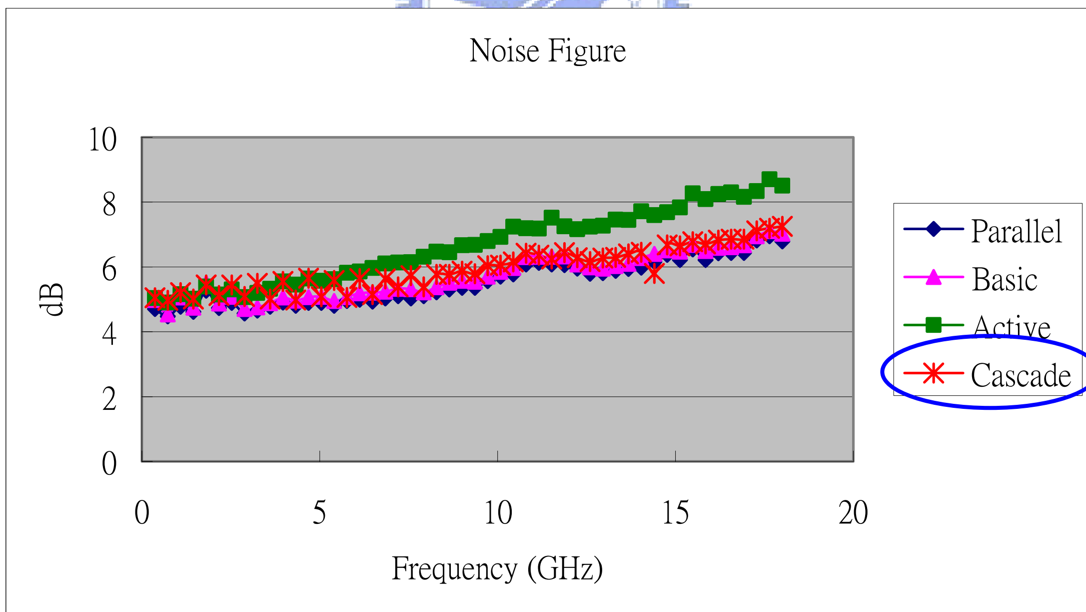

Fig.4-6 Noise figures of four configurations

Generally, except for Type IV configuration, the insertion gains at low frequency are close to simulation results. Type I configuration has a smooth insertion gain. Type

II configuration consumes less power but has a poor noise figure. Type III configuration has larger insertion gain and better noise performance.

Amazingly, the insertion gain and noise figure of Type IV configuration is superior to simulation results, while return loss degrades to about –3.4~-5dB. I think it is because the model provided by GCTC is underestimated.

Reference

[1] K. Kobayashi, R. Esfandiari, A. Oki, D. Umemoto, J. Camou, M. Kim
"GaAs heterojunction bipolar transistor MMIC DC to 10 GHz direct-coupled feedback amplifier"
Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1989. Technical Digest 1989. 11th Annual 22-25 Oct. 1989 Page(s):87 – 90.

[2] K. Kobayashi, D. Umemoto, R. Esfandiari, A. Oki, L. Pawlowicz, M. Hafizi, L. Tran, J. Camou, K. Stolt, D. Streit, M. Kim
"GaAs HBT MMIC broadband amplifiers from DC to 20 GHz"
Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1990. Digest of Papers, IEEE 1990 7-8 May 1990 Page(s):19 – 22.

[3] K. Kobayashi, A. Oki
"A low-noise baseband 5-GHz direct-coupled HBT amplifier with common-base active input match"
Microwave and Guided Wave Letters, IEEE [see also IEEE Microwave and Wireless Components Letters] Volume 4, Issue 11, Nov. 1994 Page(s):373 – 375

[4] K. Kobayashi, R. Esfandiari, M. Hafizi, D. Streit, A. Oki, L. Tran, D. Umemoto, M. Kim
"GaAs HBT wideband matrix distributed and Darlington feedback amplifiers to 24 GHz"
Microwave Theory and Techniques, IEEE Transactions on Volume 39, Issue 12, Dec 1991 Page(s):2001 – 2009

[5] C. Armijo, R. Meyer
"A new wide-band Darlington amplifier"
Solid-State Circuits, IEEE Journal of Volume 24, Issue 4, Aug. 1989 Page(s):1105 - 1109

[6] D. Cui, D. Sawdai, S. Hsu, D. Pavlidis
"Low DC power, high gain-bandwidth product, coplanar Darlington feedback amplifiers using InAlAs/InGaAs heterojunction bipolar transistors"
Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 2000. 22nd

Annual5-8 Nov 2000 Page(s):259 - 262

[7] N. Sheng, W. Ho, N. Wang, R. Pierson, P. Asbeck, W. Edwards
"A 30 GHz bandwidth AlGaAs-GaAs HBT direct-coupled feedback amplifier"
Microwave and Guided Wave Letters, IEEE [see also IEEE Microwave and Wireless Components Letters] Volume 1, Issue 8, Aug. 1991 Page(s):208 – 210

[8] Y. Kuriyama, J. Akagi, T. Sugiyama, S. Hongo, K. Tsuda, N. Iizuka, M. Obara
"DC to 40-GHz broad-band amplifiers using AlGaAs/GaAs HBT's"
Solid-State Circuits, IEEE Journal of Volume 30, Issue 10, Oct. 1995 Page(s):1051 - 1054

[9] Bo Shi, Yan Wah Chia
"Design of a SiGe low-noise amplifier for 3.1-10.6 GHz ultra-wideband radio"
Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on Volume 1, 23-26 May 2004 Page(s):I-101 - I-104 Vol.1

[10] Power HBT Design Manual of GCTC

[11] M.F. Chang
"Current trends in heterojunction bipolar transistors", World Scientific Publishing Co.

[12] D. Pozar
"Microwave engineering", 2nd edition, John Wiley & Sons, N.Y. 1998.