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碩 士 論 文

使用互補金屬氧化半導體製程之超寬頻低雜訊放大器
及使用砷化銦鎵假型高速電子移動電晶體之寬頻開關

UWB CMOS Low-Noise Amplifier
And
Wideband InGaAs pHEMT Switch

研 究 生：邱珮如　　(Pei-Ju Chiu)

指導教授：鍾世忠　　(Dr. Shyh-Jong Chung)

中 華 民 國　九十四 年 六 月

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國立交通大學　電信工程學系碩士班

摘要

本篇論文的第一個部份描述應用在超寬頻系統中的低雜訊放大器之分析與設計。超寬頻的低雜訊放大器需具備有寬頻、低功率、增益平坦的特性，為了達到寬頻的目標，利用多級的概念來設計，並且選擇採用共閘級做為第一級放大，中間兩級選擇共射級組態來提高整體增益，最後再加上一級電壓追隨器達到輸出阻抗匹配。這個寬頻低雜訊放大器的頻寬為 2.6 ~ 8.6 GHz，增益為 16 dB ± 1dB，雜訊指數最低 5.5 dBm，消耗功率為 24 mW。

第二個部份敘述一個寬頻開關的設計與量測。這個單刀雙擲開關的頻寬為 33~60 GHz，中心頻率 46.5 GHz，介入損耗小於 4 dB，與大於 32 dB 的隔絕度。

UWB CMOS Low-Noise Amplifier

And

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Abstract

The first part of the thesis describes the design and analysis of a low-noise amplifier for UWB system. The features of the UWB LNAs are wide bandwidth, low power consumption and flatness of gain. In order to get wide bandwidth, we utilize the concept of multi-stages to design this circuit. The first stage is a common gate topology and two common source amplifiers in the middle stages and the final stage is a voltage follower. The bandwidth of the LNA is ranged from 2.6 GHz to 8.6 GHz. The gain is 16 dB ± 1 dB. The minimum noise figure is 5.5 dBm and the power consumption is 24 mW.

The second part is the design and measurement of a wideband single-pole double-throw switch. The bandwidth of the SPDT switch is ranged from 33 to 60 GHz centered at 46.5 GHz. The insertion loss is less than 4 dB and the isolation is more than 32 dB.

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研究所兩年的生活，除了讓我獲得專業的知識，更讓我在修養方面更上一層樓。首先我要感謝我的指導教授鍾世忠博士，在我的研究過程中提供了充足的研究資源，老師豐富的學識、待人處世的寬厚，讓我受益良多。同時要感謝口試委員陳俊雄教授及郭仁財教授的不吝指導，使這篇論文更爲完善。此外，要特別感謝張志揚教授在 V-band 量測上所給予的協助。

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Chapter 1

Introduction

1.1 Motivation

Ultra-wideband (UWB) radar systems were developed mainly as a military use because they could see through trees and beneath ground surface. Recently, UWB technology has been focused on consumer electronics and communications because of their potential for high-speed wireless communication. UWB is a wireless technology that transmits an extremely low-power signal over a wide spread of radio spectrum which is from 3.1 to 10.6 GHz defined by the Federal Communication Commission (FCC). Ideal goals for UWB systems are low power, low cost, high data rates. The dynamic ranges of the state-of-the-art wideband amplifiers which work well in other applications such as high-speed optical transceivers can not satisfy the UWB system specifications.

Many LNA technologies for narrow-bandwidth systems have been discussed before. Most of the topologies are designed for narrow-bandwidth systems during the last decade. Hence, it is a challenge to find an applicable LNA topology for an UWB system. A low noise amplifier which is applied to UWB systems must be characterized the wide-band input matching to a 50Ω antenna with flat gain over the entire bandwidth, minimum possible noise figure and low power consumption. In order to meet the target of system-on-chip (SOC), the digital and analog sections must be integrated together. Therefore, the CMOS technology will be adopted in this thesis.

A monolithic microwave/millimeter-wave integrated circuit (MMIC) is a microwave or millimeter-wave circuit, in which the active and passive components

are fabricated on the same semiconductor substrate such as gallium arsenide (GaAs) or indium phosphide (InP). The operating frequency is from several to hundred GHz. The GaAs pseudomorphic high electron mobility transistor (pHEMT) is the most commonly available HEMT technology. The term " pseudomorphic" comes from the fact that the device channel is generally formed from InGaAs. Making use of GaAs pHEMT technology is beneficial for performance and is able to reach the requirements of most millimeter-wave wireless applications such as local multipoint distribution system (LMDS), high speed local area networks (LAN' s), satellite communications, astronomy observations, automotive collision avoidance radar system and military use [1]. A broadband switch can be exploited for diverse applications. It controls the signal flow of the integrated circuit and it is also a crucial component to achieve the goal of SOC.

1.2 Organization

This thesis was constructed from six chapters. It was devoted to the design of an UWB CMOS LNA and a new broadband switch using InGaAs pHEMT.

Chapter 1 introduces the motivation of the research and the arrangement of this thesis.

In chapter 2, the topologies in common use of LNA will be introduced. Each of them has different advantages with different design architectures. We will make a description for the four kinds of different topologies and choose the most suitable one for wideband applications. In addition, the survey of recent low-noise amplifiers will also be listed in this chapter.

In chapter 3, a LNA whose bandwidth ranges from 2.6 GHz to 8.6 GHz will be presented. The architecture uses $\frac{1}{g_m}$ termination topology as the first stage. To

achieve wideband performance, we introduce some gain matching components at the third stage. The simulated results will be listed in the end.

In chapter 4, the design methodology of broadband switches and various switching devices will be introduced, and switch configurations will also be presented.

In chapter 5, the design theory and the design flow of a SPDT switch will be introduced here. The bandwidth of the switch is ranged from 33 GHz to 60 GHz. The simulated and measured results will be listed in the last.

In the last chapter, we will make the summary and indicate some suggestions for the future design.

Chapter 2

Design Methodology of Low Noise Amplifier

2.1 Overview

This chapter is composed of three sections; first, simple description of CMOS foundry will be listed. Second, noise sources and four basic topologies of low noise amplifiers will be discussed in detail. Finally, we will discuss the state of the art for UWB LNAs.

2.2 Noise Sources

The output noises are mainly come from thermal noises. Besides the thermal noise of resistances ($i_{n,R}$), there are the thermal noise of the channel current ($i_{n,d}$) and the gate induced current noises ($i_{n,g}$) [2]. They are listed below:

$$\overline{i_{n,R}^2} = 4kT\frac{1}{R}\Delta f \tag{2.1}$$

$$\overline{i_{n,d}^2} = 4kT\gamma g_{d0}\Delta f \tag{2.2}$$

$$\overline{i_{n,g}^2} = 4kT\beta\frac{\omega^2 C_{gs}^2}{g_{d0}}\Delta f \tag{2.3}$$

where g_{d0} is zero bias conductance, γ is the channel noise factor, and β is the gate induced current noise factor.

2.3 The basic topologies of LNAs

For the LNA circuits, a resistive impedance matching between the LNA and the driving source is a critical requirement. It is difficult to provide good impedance

matching to the source without degrading the noise performance because the input of the LNA circuits is connected to a capacitive node. There are various matching methods that have been applied to improve LNA performance. On the basis of these matching methods, the LNA topology can be sorted by four kinds [3]:

Resistive Termination The 50Ω resistance is connected to the input node of a common source amplifier directly and the architecture is shown as Fig. 2.1(a). The connection means that the input source can see only the resistor over reasonable broadband. Nevertheless, the resistance which is connected directly to the input terminal weakens the signal ahead of the transistor and brings thermal noise of its own. This topology is rarely used in the LNA design because of its unacceptable high noise figure.

$1/g_m$ Termination The input impedance is set by the $1/g_m$ of the transistor in the common gate stage shown as Fig 2.1(b). This architecture is very simple and can easily achieve the appropriate impedance matching. This topology seems to be a good choice for a wide bandwidth system because the transistor's g_m is merely affected in the frequency range of UWB system. In order to make $1/g_m$=50Ω, the value of g_m has to be fixed at 20mS. This means that the transistor size has to be fixed and this will affect the noise figure of the single transistor system. The gain of this LNA is also fixed without increasing output resistance. Therefore, there will be more than one stage when using this type topology to enhance the overall gain.

In the common gate configuration, the noise figure and the matching circuits totally depend on the single transistor in the common gate stage. The equation 2.1 shows the noise figure of the single transistor [3].

$$F = 1 + \frac{\gamma}{\alpha} \tag{2.1}$$

where γ is the coefficient of channel thermal noise and α is

$$\alpha = \frac{g_m}{g_{d0}} \tag{2.2}$$

where g_m is the transconductance and g_{d0} is the zero bias drain conductance. For the long channel device, γ equals to 2/3 and α equals to 1. For the short channel case, the value of γ is greater than 2/3. Based on these data, the best noise figure of this $1/g_m$ termination topology tends to be more than 2.2dB. Consequently, this topology can afford quite wide bandwidth impedance matching but bring a large noise figure and is difficult to achieve high gain performance.

Shunt-Series Feedback The architecture is shown as Fig. 2.1(c). With the shunt series feedback architecture, the bias point of the input is fastened with the output voltage. For this reason, the biasing point of this system is not set to the optimal bias point. This will cause an extra power consumption to achieve the desired gain. Moreover, the shunt series feedback architecture has a stability problem.

Usually the shunt series feedback can be analyzed as equation 2.3.

$$[\mathrm{S}] = \frac{1}{\Delta}\begin{bmatrix} \frac{R_f}{Z_0} - \frac{g_m Z_0}{1+g_m R_S} & 2 \\ 2\left(1 - \frac{g_m R_f}{1+g_m R_S}\right) & \frac{R_f}{Z_0} - \frac{g_m Z_0}{1+g_m R_S} \end{bmatrix} \tag{2.3}$$

where $\Delta = 2 + \frac{R_f}{Z_0} + \frac{g_m Z_0}{1+g_m R_S}$. From the S-parameter matrix, the ideal matching condition is $S_{11} = S_{22} = 0$, the series resistance R_S can be calculated as

$$R_S = \frac{Z_0^2}{R_f} - \frac{1}{g_m}. \tag{2.4}$$

Substituting 2.4 in to 2.3 attains S-parameter

$$[\mathrm{S}] = \frac{1}{\Delta}\begin{bmatrix} 0 & \frac{Z_0}{R_f + Z_0} \\ 1 - \frac{R_f}{Z_0} & 0 \end{bmatrix}. \tag{2.5}$$

Form the equation 2.4 and 2.5, we can realize that as long as we control the R_f and

R_S, we can achieve the goal of very wide bandwidth and flat gain. The only restriction of this architecture is that the source resistance R_S must be nonnegative. If R_S becomes negative the system will oscillate. This limitation puts bounds to the value g_m of the transistor with desired gain S_{21}.

$$g_m \geq g_{m\min} = \frac{R_f}{Z_0^2} = \frac{1 - S_{21}}{Z_0} \tag{2.6}$$

Therefore a transistor satisfying the condition of equation 2.6 can be selected in the negative feedback configuration. This analysis is only valid for low frequencies where all reactance components can be neglected. In the case of UWB systems, the parasitic capacitance and inductance can not be neglected. Because of the undesired effects of parasitic, not only the gain degradation but also the noise figure raising will happen at high frequency. Besides, the stability drops to the unstable region because of the feedback effect. This type of configuration must improve its gain and noise figure at high frequency without reducing stability.

With this configuration, it requires very high power consumption to increase the gain because the bias point of the system is fixed at the output voltage, which is not the optimal DC biasing point. However, the architecture gives wide bandwidth characteristic for the UWB system.

Inductive Degeneration The last topology is displayed in the figure 2.2(a). From the small signal model shown as Fig. 2.2(b), the input impedance of this architecture can be calculated as

$$Z_{\text{in}} = s(L_S + L_g) + \frac{1}{sC_{gs}} + (\frac{g_m}{C_{gs}})L_S \tag{2.7}$$

At the resonant frequency, the input impedance is purely real and proportional to L_S. Therefore, this system don't have to add additional any resistive components and it can reach the input impedance matching by choosing appropriate value of the L_S. This leads to a very good noise figure and impedance matching for a narrow

bandwidth system. However, since this topology utilizes resonance at the desired frequency, it can be used only for narrow bandwidth signals and it is not suitable for wide bandwidth applications.

2.4 State-of-the-art LNAs for UWB application

Recently, there are several low-noise amplifiers designed for UWB systems. The general architectures can be sorted for three kinds; one is choosing an inductive degeneration topology which a broadband filter is located in front of. The second is selecting a common gate topology as the first stage in addition to more stages to enhance the power gain and the bandwidth and the third is using a shunt-series feedback configuration. Even though the first kind makes use of inductive degeneration which can afford lowest noise figure, this architecture also utilizes many passive components which will introduce higher noise figure. The second kind utilizes common gate architecture to achieve input matching, but it usually has more than 1 stage and leads to more power consumption. Low noise figure and power consumption are two important features in UWB system. The third kind uses feedback to enhance the bandwidth but this will lead to the problem of stability. In order not to lead the circuit to unstable, the value of resistor must be chosen carefully. The disadvantage of the feedback topology is that the circuit is very sensitive to the process variation of the foundry. If the circuit was designed near the boundary of the stable circle, the circuit will introduce oscillation even with little process errors. It seems that there is no perfect design of low-noise amplifiers for UWB systems so far.

2.4.1 Broadband filter with source inductive degeneration LNA

In September 2001, Pietro Andreani and Henrik Sjoland published a method to optimize noise of inductively degenerated CMOS low-noise amplifier [4]. The

simplified schematic is shown in Fig. 2.3. They mainly discussed the relationship between Q, channel noise and gate induced current noise. When the value of Q is increasing, the channel noise decreases but it also leads the gate induced current noise to increase. The capacitor C_d has the function of decoupling Q from C_{gs}, which allows for an adjustable reduction of Q for any given value of C_{gs}. This architecture is only suitable for narrow band application. In 2004, this circuit was improved for wide-band use. Andrea Bevilacqua and Ali M Niknejad added two inductors (L_1, L_2) and capacitors (C_1, C_2) in front of the previous circuit as shown in Fig. 2.4. These passive components form a three-section band-pass filter to resonate its reactive part over the whole band. In this way, it can achieve the wideband input impedance matching. Its 3 dB bandwidth ranges form 2.4 to 9.5 GHz and power consumption is 9 mW [5].

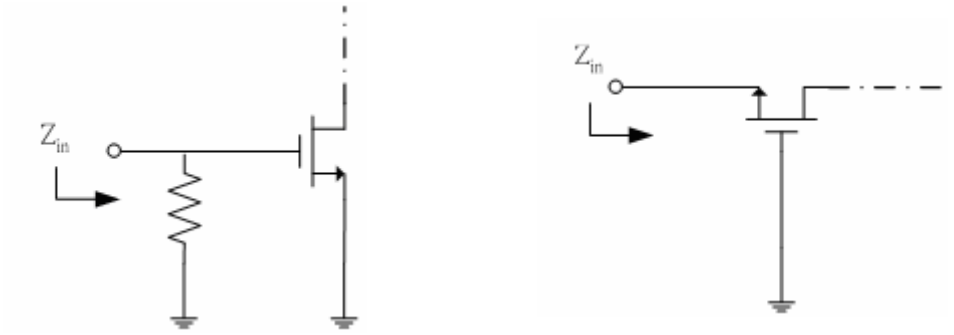
2.4.2 Low noise amplifier with active input matching

This architecture utilizes the characteristic of common-gate topology to achieve the input impedance matching. A circuit presented in 2004 is shown as Fig. 2.5. The resistance looking into the source terminal is $1/g_m$ and proper choice of bias current can get the desired 50Ω. The second stage uses a feedback topology to enhance the bandwidth and increase total gain. The addition of L_f makes more gain and it do not lead the circuit to oscillate. At some frequencies, the phase of output voltage is in-phase with input voltage (positive feedback). L_f can also avoid this situation to happen. The capacitance C_f blocks the DC current that comes from the output node. The bandwidth of this circuit ranges from 3.1 to 6.1 GHz and its gain is around 17 to 15.5 dB [6].

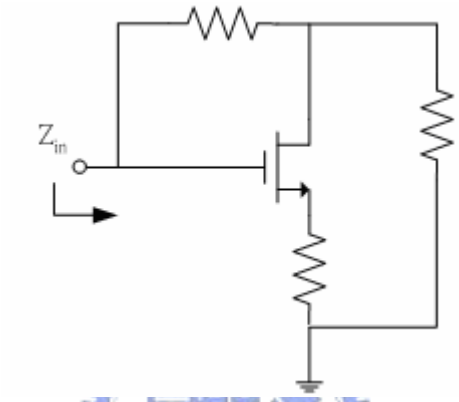
2.4.3 Low noise amplifier with feedback

A shunt-series feedback topology LNA schematic is shown in Fig. 2.6. In the figure, the load inductance L_2 substitutes for the resistive load of the original configuration. The impedance of the inductor increases as the frequency increases and this can compensate for the amplifier degradation at high frequency. The inductor L_1 is added for additional gain boost at high frequency. The C_f is used for DC blocking. This capacitance blocks the DC current that comes from the output node. The transduced gain is 8.5 dB and has a variation of ± 0.2 dB. The noise figure is 3 dB [7].

We make a table to compare some wide-band LNAs shown in Table 4.1. Input 1dB compression point and IP3 are merely concerned in case of UWB LNA because in general the transmit power is limited to be less than -42dBm/Hz.

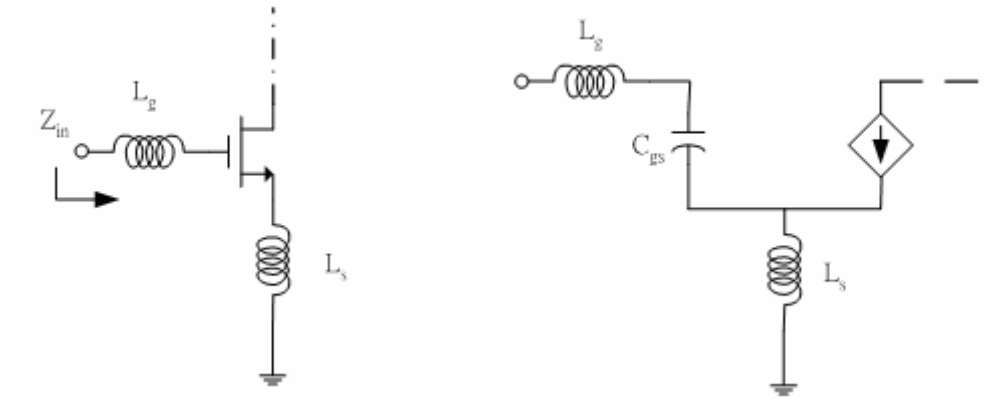


(a) (b)



(c)

Fig. 2.1 LNA topologies: (a) Resistive Termination, (b) $1/g_m$ Termination, (c) Shunt-series Feedback



(a) (b)

Fig. 2.2 Inductive degeneration : (a) topology, (b) small signal model

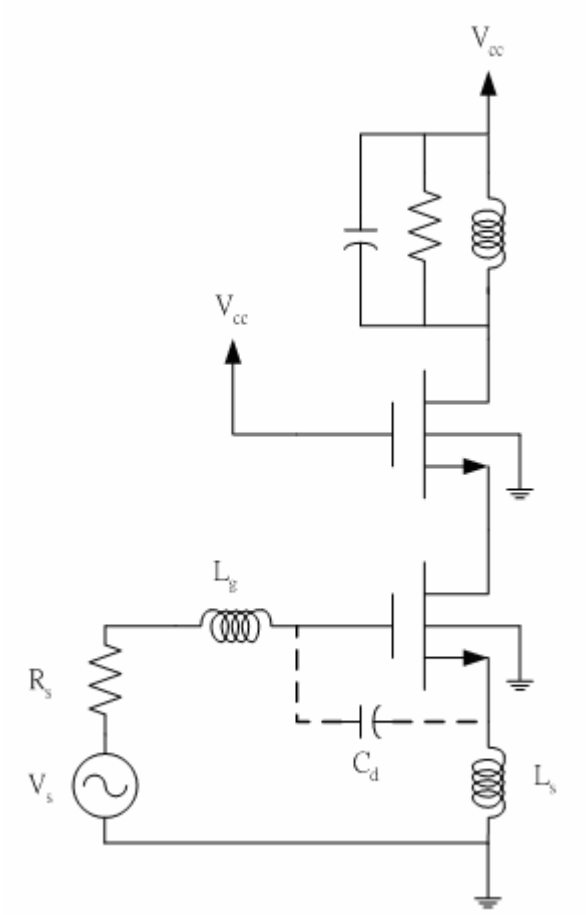


Fig. 2.3 Simplified schematic of a low noise amplifier with inductive source degeneration.

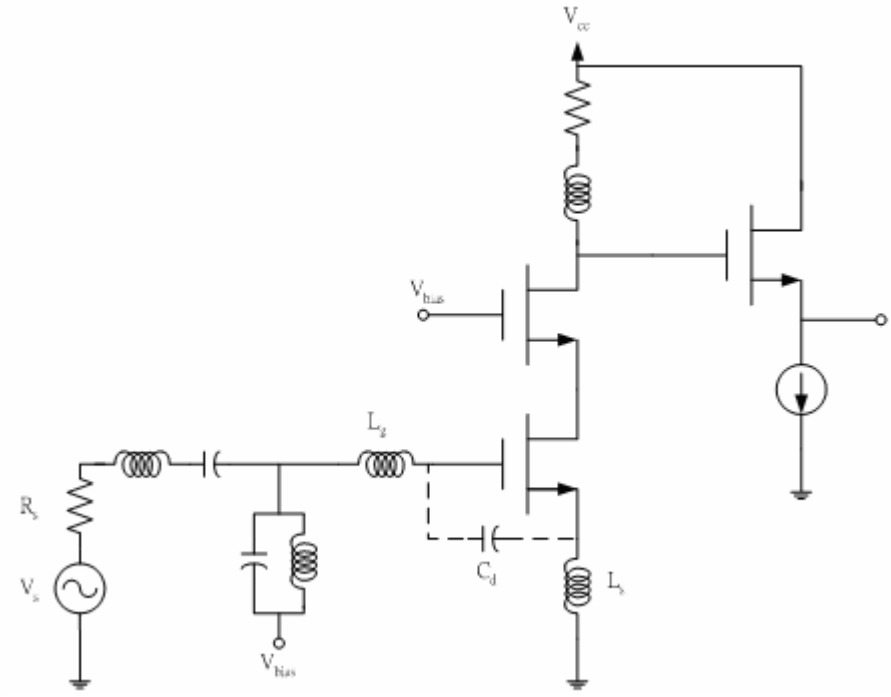


Fig. 2.4 Simplified schematic of wideband low noise amplifier

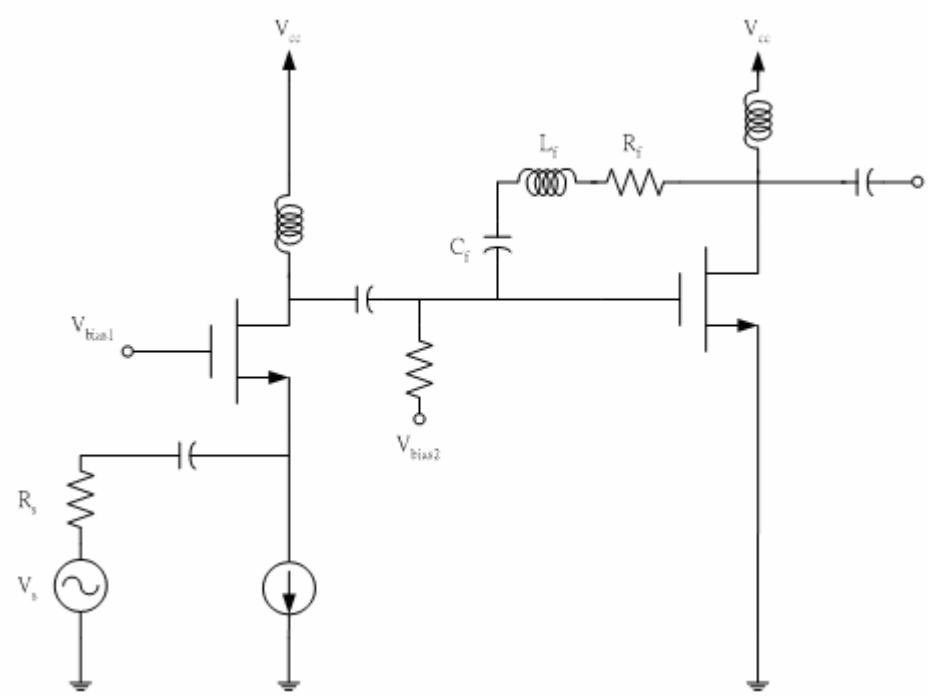


Fig. 2.5 Circuit schematic of wideband LNA with active input matching

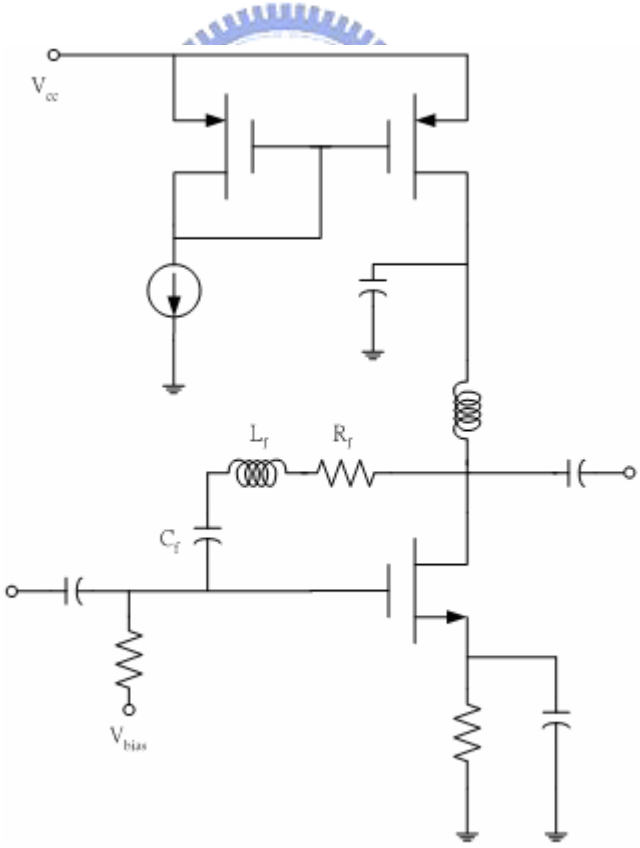


Fig. 2.6 Circuit schematic of wideband LNA with feedback

	[5] measured	[6] Simulated	[7] Simulated	This work Simulated
Technology	0.18 um CMOS	0.18 um CMOS	SiGe 0.5 um	0.18 um CMOS
Band (GHz)	2.4 to 9.5	3.1 to 6.1	0.8 to 1.6	2.6 to 8.6
Bandwidth	7.1 (3dB)	3	0.8	6
S11 (dB)	<-9.4	-12.9 to -18	N/A	<-9.4
S21 (dB)	10.4 (max)	17 to 15.5	8.5 ± 0.2	17.6 to 15.6
S12 (dB)	<-35	<-43	N/A	<-44.5
NF (dB)	4.2 to 8	3.9 to 4.3	about 3	5.58 to 6.6
Power (mW)	9	21	23.1	24
Area(mm^2)	1.1	1.86 x 1.36	N/A	1

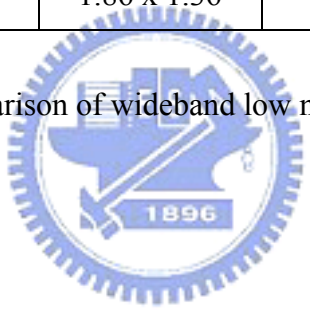


Table 2.1 Comparison of wideband low noise amplifiers

Chapter 3

UWB CMOS Low Noise Amplifier

3.1 Overview

This chapter will present a 2.6-to-8.6 GHz low-noise amplifier using a 0.18 um CMOS process. It is based on the analysis in chapter 2. The foundry description, design and simulation of the circuit will be shown in the following.

3.2 CMOS foundry description

The CMOS device used in this design is fabricated by TSMC Semiconductor Corporation with a deep N-well 0.18-um process, and the Deep N-Well structure is shown as Fig. 3.1. This CMOS process provides academic users only as it is fabricated through TSMC provided shuttle. It possesses 1 poly layer and 6 metal layers with low k inter-metal dielectric. Deep N-well, MiM capacitor, high poly resistor, multi-Vt device and thick top metal are available for 1.8V/3.3V applications. It is suitable for logic, mixed signal, and RF designs [8].

3.2 Circuit Design

In order to achieve the wide-band input impedance matching and flat gain, I utilize the multistage architecture. Using multistage architecture can expand the overall bandwidth [9]. There are 4 stages in this circuit totally, as shown in Fig. 3.2. First stage is a common gate structure in order to achieve the impedance match of 50Ω. The input impedance is close to $1/g_m$ and g_m is not much affected by frequency of the bandwidth range, so it can achieve the wideband input matching. The

second common source structure is for gain boost. The third source inductive degeneration cascade architecture can not only enhance the gain but also reinforce the reverse isolation. Reverse isolation is a crucial factor because LNA is often put in front of mixer. In order to avoid the local oscillator leaking back to the LNA, it's better to choose a LNA with good reverse isolation for systems. The final stage is just used as a buffer to permit the output impedance to be dropped to around 50Ω.

The first and final stages utilize two current sources to bias the circuit, so the current mirrors should be integrated into the circuit. The design of the current mirror is same as tradition except for the capacitor C_{block}, as shown in Fig. 3.3. This capacitor can block the high frequency interference which is leaking from the drain node. If this capacitor was removed, the noise figure of the system will arise significantly.

Because we utilize common gate as the first stage, the thermal noise of channel current has a significant effect on system's noise figure. In order to minimize the effect, we have an analysis for the relationship between ΔV, I_{bias} and $\overline{i_{n,d}^2}$ where $\Delta V = V_{gs} - V_t$.

$$\overline{i_{n,d}^2} = 4kT\gamma g_{d0}\Delta f \tag{3.1}$$

$$g_m^2 \overline{V_{n,in}^2} = \overline{i_{n,d}^2} \tag{3.2}$$

$$\overline{V_{n,i}^2} = \frac{2kT\gamma}{3I_{bias}}\Delta V \tag{3.3}$$

Therefore, we can reduce the noise figure by decreasing ΔV and increasing I_{bias}.

The drain bias voltage is 1.8 V and the gate bias voltage is 0.7 V. The bias voltage of current mirrors is adjustable in the range of 0 to 1.8 V. The layout of this low-noise amplifier is accomplished by the Cadence tools and is depicted in Fig. 3.4. The chip size is 1 x 1 mm^2.

3.3 Simulation Results

The model used in this simulation is BSIM3v3 provided by the foundry. The performance of the low-noise amplifier is simulated with the commercial CAD software Advanced Designed System. The post-simulation are performed via a full-wave EM full-wave simulator SONNET.

The simulated gain and input, output return loss is depicted in Fig. 3.5. The reverse isolation is shown in Fig. 3.6. The minimum noise figure is 5.6 dB, as shown in Fig. 3.7. The total bandwidth is from 2.6 GHz to 8.6 GHz. The gain is 16dB $\pm$1 dB and input/output return loss are better than 10 dB. The reverse isolation is better than 44 dB. The stability factor K and Mu are also simulated, as shown in Fig. 3.8(a) and (b). The sufficient conditions for unconditional stable are K>1 and Mu>1 of two ports network.

The output power versus input power is simulated at 5.5 GHz, as shown in Fig. 3.9. The 1 dB compression point was -27 dBm at 5.5 GHz.

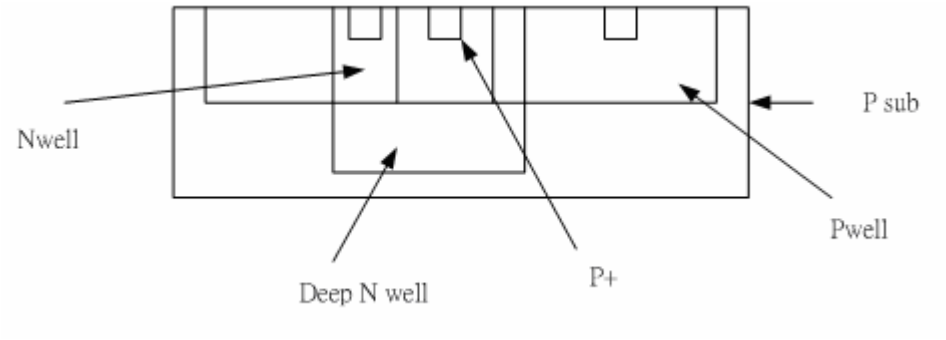


Fig. 3.1 The Deep N-well structure

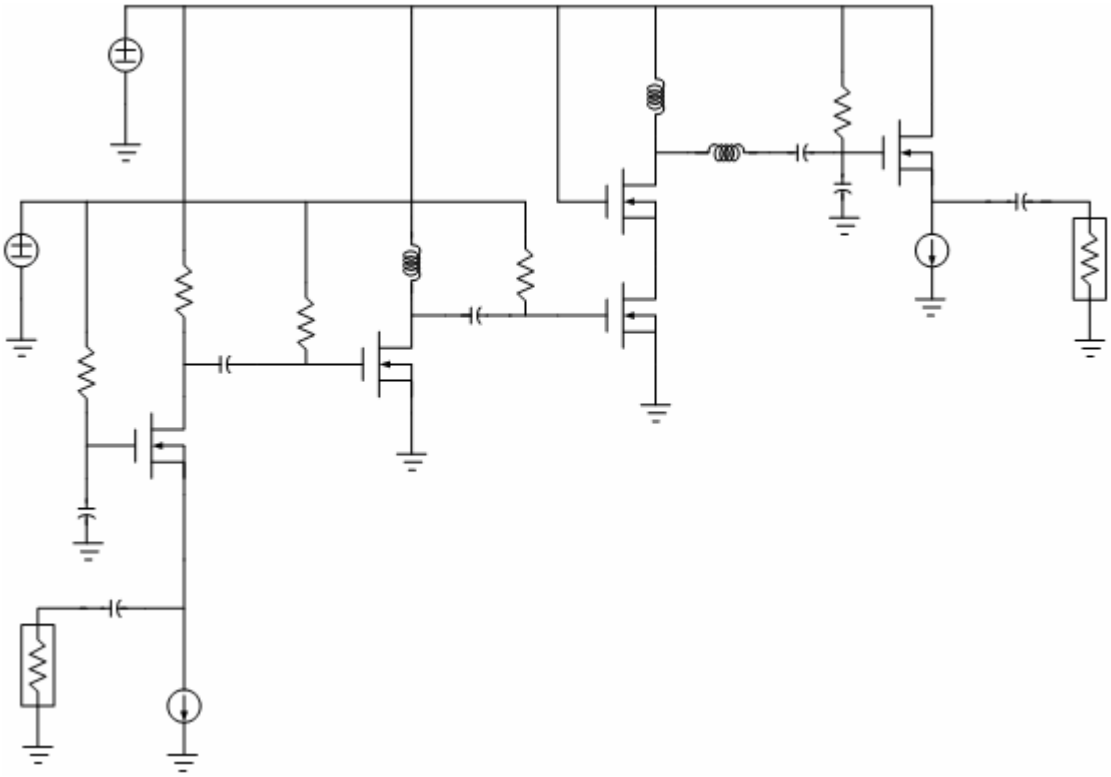


Fig. 3.2 Simplified circuit of low noise amplifier

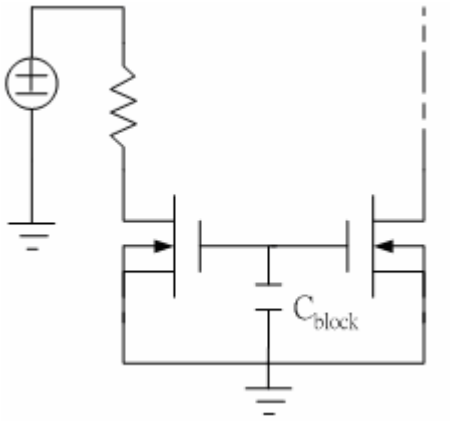


Fig. 3.3 Architecture of the current mirror

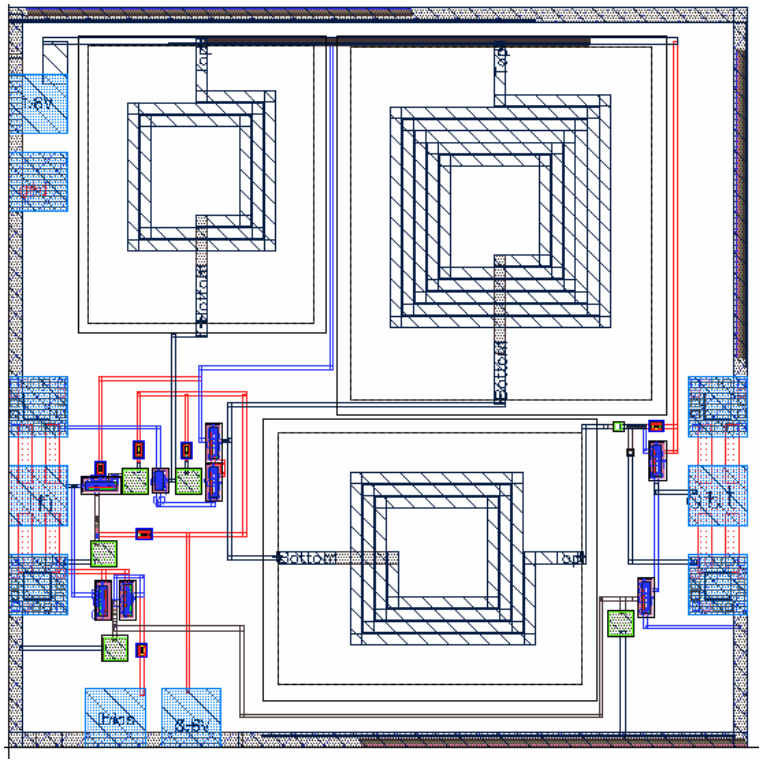


Fig. 3.4 Layout of LNA chip

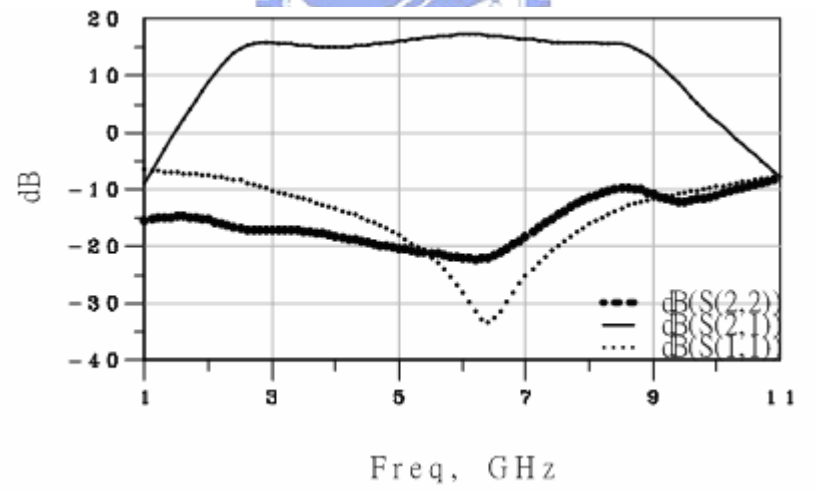


Fig. 3.5 S11, S22 and gain from 1 GHz ~ 11 GHz

Fig. 3.6 Reverse isolation S12 from 1 GHz ~ 11 GHz

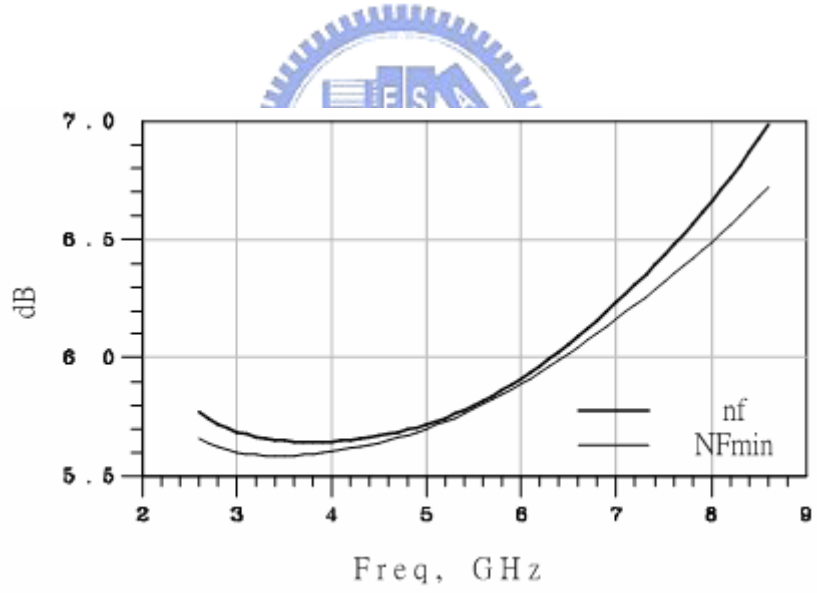
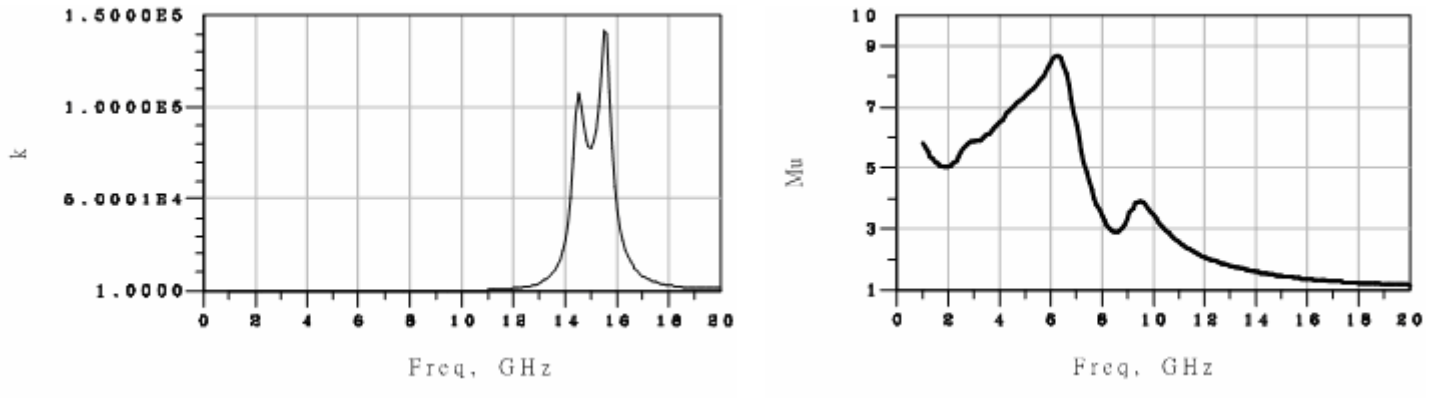


Fig. 3.7 Noise figure of LNA



(a) (b)

Fig. 3.8 Stability Factor, (a) K>1, (b) Mu>1

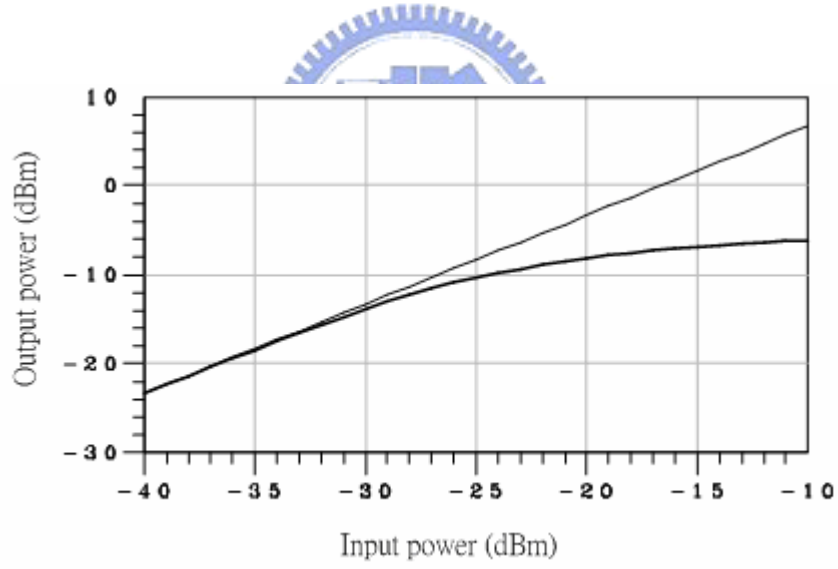


Fig. 3.9 Output power versus input power

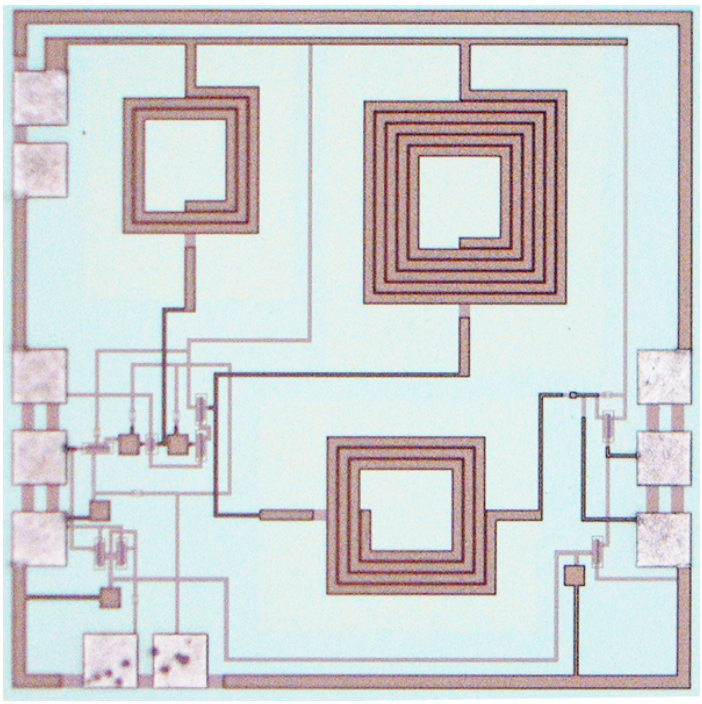


Fig. 3.10 The microphotograph of the UWB LNA

Chapter 4

Design Methodology of Broadband Switch

4.1 Overview

A switch can be applied to execute the multiple accesses, which is widely used and considered as a main choice in communication. It also reduces the duplicate of the circuits with the same functions. In low frequency range, the design of switches neglects the parasitic and transmission-line effects. On the contrary, these effects occur significantly in the millimeter-wave frequency range and must be taken into account in the switch design. This chapter has a full discussion on the design methodology of broadband switches.

4.2 Switching Devices

PIN diodes and FETs are two types of devices used commonly in the control circuits. Here, we discuss the significant properties of these devices.

PIN Diodes A PIN diode is a pn junction device that has a very minimally doped or intrinsic region located between the p-type and n-type contact regions as illustrated in Fig. 4.1(a). The combination of the intrinsic or i-region results in characteristics that is very advantageous for certain device applications. In reverse bias the intrinsic region causes very high value for the diode breakdown voltage, whereas the device capacitance is reduced by the increased separation between the p- and n-region. In forward bias the conductivity of the intrinsic region is controlled by the injection of charge from the end regions. A practical PIN diode consists of a lightly doped p- or n-region between the highly doped p-type and n-type contact

region, as shown in Fig. 4.1(b) and Fig. 4.1(c). To identify very lightly doped p and n material, the Greek letters are used; consequently, lightly doped p material is called π-type and lightly doped n material is called ν-type. The diode is a resistor controlled by bias current with preferable linearity and low distortion. PIN diodes can provide faster switching speed and can handle medium to large RF power levels. They also make excellent RF switches, phase shifters and limiters. Sometimes the Schottky barrier diode (SBD) is applied for faster switching speed.

FETs In recent years PIN diode switches have been increasingly replaced by FETs based monolithic switches, especially for low to medium power applications. The FET switches are three-terminal devices, in which the gate bias V_g controls the states of the switch. The FET acts as a voltage controlled resistor, where the gate bias controls the drain-to source resistance in the channel. The intrinsic gate-to-source and gate-to-drain capacitances and device parasitics limit the performance of the FET switches at higher frequencies. In switching applications, a low-impedance (nearly short) state is obtained by making the gate voltage equal to zero. When the negative gate-source bias is larger than the pinch-off voltage in magnitude, the FET is in a high-impedance (nearly open) state. Fig. 4.2 shows the linear operation regions of a switching FET [10]. The configuration of a switching FET [11] is indicated as Fig. 4.3. A low-impedance state can be adequately modeled by a resistance (R_{on}) which is series connection to a parasitic inductor (L_{on}) between the source and the drain as depicted in Fig. 4.4(a). A complete equivalent circuit in a high-impedance state is illustrated in Fig 4.4(b). The equivalent circuit is based on the device geometry from the reference [10], [12]. The off-state drain-to-source leakage resistance (R_{ds}) is generally large enough to be neglected in circuit modeling. The drain and the source are directly capacitive-coupled and through the gate (C_{ds}, C_{gs} and C_{gd}). All of these

capacitances have series parasitic resistive elements (R_{gs} and R_{gd} for C_{gs} and C_{gd} , R_d for C_{ds}). A simplified FET model can be used without sacrificing accuracy as shown in Fig. 4.5(a) and Fig. 4.5(b). The parasitic inductor was neglected for the on-state equivalent circuit. The off-state equivalent circuit has been reduced to a simple series resistor (R_{off}) and a capacitor (C_{off}). For the simplification, it is assumed that the magnitudes of the reactances of the various capacitances are much greater than the various parasitic resistances. This assumption yields the following relationship:

$$R_{off} = \frac{R_{gs} + R_{gd}}{[1 + \frac{C_{ds}}{C_{gs} + C_{gd}}]^2} + \frac{R_s + R_d}{[1 + \frac{C_{gs} + C_{gd}}{C_{ds}}]^2} \tag{4.1}$$

$$1/C_{off} \approx \frac{1/(C_{gs} + C_{gd})}{[1 + \frac{C_{ds}}{C_{gs} + C_{gd}}]^2} + \frac{1/C_{ds}}{[1 + \frac{C_{gs} + C_{gd}}{C_{ds}}]^2} \tag{4.2}$$

Note that the relationships for R_{off} and C_{off} are frequency independent. The frequency dependent terms have been ignored. It is important to note that no DC power is required by the FET switches in either state. The other advantage of FET switches is that additional bias circuits are unnecessary because of the DC isolation between gate and drain (or source) by constitution. The FET switches are superior to the PIN diode switches because they don't have DC power consumption and DC biasing isolation.

4.3 Basic Switch Configurations

There are two basic configurations [13] that can be used for a simple switch design to control the flow of millimeter-wave signals along a transmission line. One is series-type switch and the other is shunt-type switch. The third configuration that

consists of the series-type and shunt-type switches is called series-shunt switch.

Insertion loss and isolation are two measures of the performance for the switch when it is on-state and off-state. Insertion loss is defined as the ratio of the power delivered to the load in the on-state of the ideal switch to actual power delivered by the practical switch. It is usually expressed in decibels. Isolation is defined as the ratio of the power delivered to the load for an ideal switch in the on-state to the actual power delivered to the load when the switch is in the off-state.

Series-type Switches The equivalent circuit of a series-type switch is shown as Fig. 4.6(a). The low-impedance state of the FET allows the signal to propagate, while in the high-impedance state, the incident power on the switch is mostly reflected back. The low- and high-impedance states of the FET are called on-state and off-state for a series-type switch. The insertion loss may be calculated by considering the equivalent circuit depicted in Fig. 4.6(b). If V_L denotes the actual voltage across the load in the ideal switch, the insertion loss can be written as

$$IL = \left|\frac{V_L}{V_{LD}}\right|^2 = 1 + \frac{R_{low}}{Z_0} + \frac{1}{4}\left(\frac{R_{low}}{Z_0}\right)^2 + \frac{1}{4}\left(\frac{X_{low}}{Z_0}\right)^2, \tag{4.3}$$

where $Z_{low} = R_{low} + jX_{low}$ is the impedance of the switching device in the low-impedance state. Similarly, the isolation is given as

$$ISO = \left|\frac{V_L}{V_{LD}}\right|^2 = 1 + \frac{R_{high}}{Z_0} + \frac{1}{4}\left(\frac{R_{high}}{Z_0}\right)^2 + \frac{1}{4}\left(\frac{X_{high}}{Z_0}\right)^2, \tag{4.4}$$

where $Z_{high} = R_{high} + jX_{high}$ is the impedance of the switching device in the high-impedance state.

Shunt-type Switches Fig. 4.7(a) illustrates the equivalent circuit of a shunt-type switch. The shunt-type switch is complementary to the series-type switch. The low-impedance state of the FET almost reflects the incident power back and the

high-impedance state permits the signal to propagate. Therefore, the low- and high-impedance states of the FET are called off-state and on-state for a shunt-type switch. The insertion loss may also be derived from the equivalent circuit as shown in Fig. 4.7(b). If V_L denotes the actual voltage across the load in the ideal switch, the insertion loss can be written as

$$IL = \left|\frac{V_L}{V_{LD}}\right|^2 = 1 + \frac{G_{high}}{Y_0} + \frac{1}{4}\left(\frac{G_{high}}{Y_0}\right)^2 + \frac{1}{4}\left(\frac{B_{high}}{Y_0}\right)^2, \tag{4.5}$$

where $Y_{high} = G_{high} + jB_{high}$ is the admittance of the switching device in the high-impedance state. Similarly, the isolation is given as

$$ISO = \left|\frac{V_L}{V_{LD}}\right|^2 = 1 + \frac{G_{low}}{Y_0} + \frac{1}{4}\left(\frac{Y_{low}}{Y_0}\right)^2 + \frac{1}{4}\left(\frac{B_{low}}{Y_0}\right)^2, \tag{4.6}$$

where $Y_{low} = G_{low} + jB_{low}$ is the admittance of the switching device in the low-impedance state.

Series-Shunt Switches The simplest series-shunt switching configuration is indicated in Fig. 4.8(a). This switching circuit can be analyzed in terms of the equivalent circuit as shown in Fig. 4.8(b). For on-state, the impedance of the device Z_{se} is denoted by the low impedance Z_{low}, and the impedance Z_{sh} is denoted by the high impedance Z_{high}. From the simple circuit analysis, the insertion loss can be written as

$$IL = \left|\frac{1}{2} + \frac{(Z_0 + Z_{high})(Z_0 + Z_{low})}{2Z_0 Z_{high}}\right|^2. \tag{4.7}$$

Similarly, the isolation is written as

$$ISO = \left|\frac{1}{2} + \frac{(Z_0 + Z_{low})(Z_0 + Z_{high})}{2Z_0 Z_{low}}\right|^2. \tag{4.8}$$

If the non-identical devices are used in the series and the shunt locations, the values of

Z_{high} and Z_{low} in (4.7) will be different from those in (4.8).

In general, the isolation obtained by using the series-shunt configuration is much better than that for either the series-type or the shunt-type switch. The insertion loss for the series-shunt configuration is worse than that for a shunt-type switch but better than that for a series-type switch.

4.4 Broadband Switch Design

4.4.1 Single-Pole Single-Throw Switch

A single-pole single-throw (SPST) switch is used to control the flow of signals along a transmission line. As mentioned previously, three configurations can be applied to design a SPST switch. In the millimeter-wave frequency range, the device paracitics introduce more significant detrimental effects on insertion and isolation performance. Some well-known compensated techniques, such as capacitive [14] or impedance-transformation methods [15], can be exploited to minimize the non-ideal open or short effects. A traveling-wave concept was also applied in SPST switch design.

A traveling-wave switch (TWSW) whose bandwidth is ranged from DC to 110 GHz has been published in May, 2000[16]. The circuit is shown as in Fig. 4.9(a). The TWSW is described as the combination of a distributed shunt FET and a transmission line of drain electrode. The reason that the switch can have a very wide bandwidth is the equivalent circuit, as shown in Fig. 4.9(b), is the same as a lossy transmission line for the on-state of the TWSW. This architecture is only suitable for single-pole single-throw switch design because that when two or more branches combine together, the traveling-wave property, i.e wideband performance, will be destroyed.

4.4.2 Single-Pole Double-Throw Switch

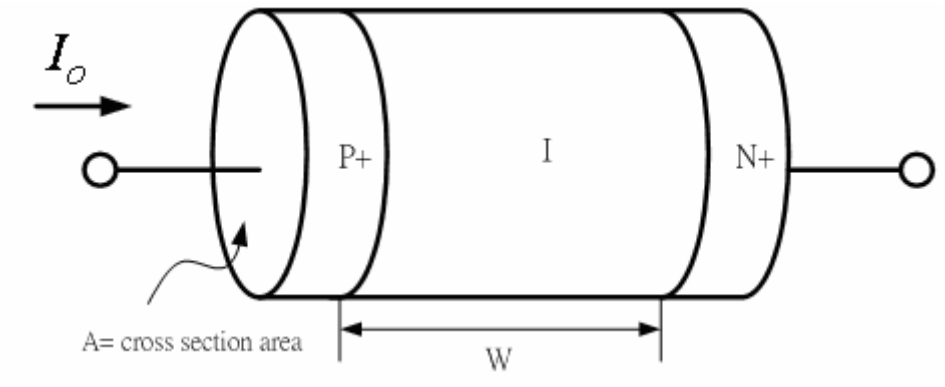
The series-type and shunt-type circuits for single-pole double-throw (SPDT) switch is illustrated in Fig. 4.10(a) and Fig. 4.10(b). The switch requires at least two switching devices. If the branch of the series-type is ON state, the FET is biased in the low-impedance state, and the branch is OFF state while the FET is biased in the high-impedance state. If the branch of the shunt-type is ON state, the FET is bias on the high-impedance state, and vice versa. The input signal flow controls by reversing the FET states. The bandwidth of the shunt-type SPDT switch is limited because of the quarter-wavelength transmission line, which is required between the locations of the two switching devices.

The SPDT circuit, as shown in Fig. 4.11, has the bandwidth of 8 GHz which is ranged from 56 to 64 GHz with insertion loss less than 3.2 dBm [17]. The structure is similar with the circuit illustrated as section 4.4.1. The switch is composed of the quarter-wavelength transformer and the FETs which are spaced by one quarter wavelength between the devices and the common joint. The bandwidth of this SPDT switch is limited by the quarter-wavelength transformer but the transformer can provide high isolation and minimize the loading effect. In spite of the circuit seems like the TWSW, it doesn't have the characteristic of traveling wave so its bandwidth is not wide as the traveling-wave switch.

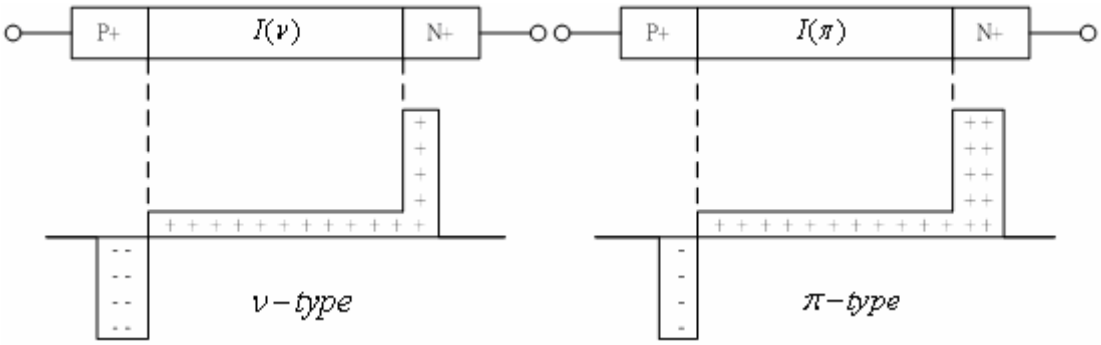
4.4.3 Single Pole m-Throw Switch

The single-pole m-throw (SPmT) switch has a single input, and m arms output and only one arm of them is on state. This kind of switch can be used to control antenna wave beams that the most common application is anti-collision radar used in car. A SPmT shunt-type switch can be realized by using the short-circuited stub filter

which will be introduced in chapter 5. The FETs are spaced by m quarter wavelength transformers whose characteristic admittance is Y_0 between the joint of the input and the m output arms. Each arm has n short-circuited stubs located between FETs and the characteristic admittance of each stub is Y_{TN}. The (m-1) off-arms have a nearly short circuit made by the low-impedance FETs. The equivalent characteristic admittance of these (m-1) arms is (m-1)Y_0. The equivalent circuit of the whole switch, as shown in Fig. 4.12 [18], will be looked like a short-circuited stub whose characteristic admittance is (m-1)Y_0 shunt with the ON output arm. The entire characteristic is still hold with the theory of the short-circuited stub filter. For this reason, the bandwidth is unrestricted by utilizing this design approach.



(a)



(b) (c)

Fig. 4.1 (a) A general structure of the PIN diode; (b) ν-type, (c) π-type

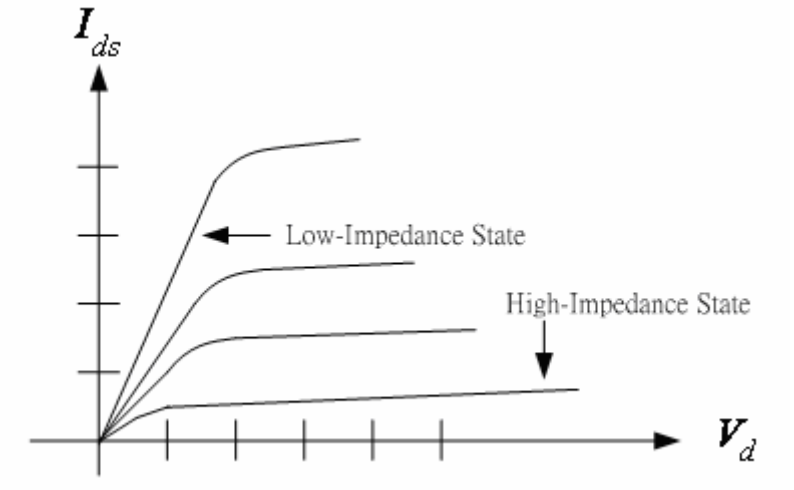


Fig. 4.2 Linear operational regions of a FET switch

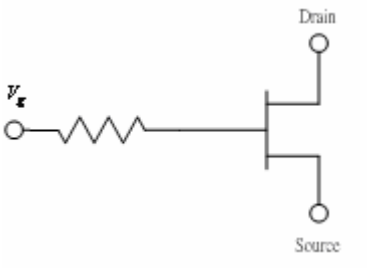
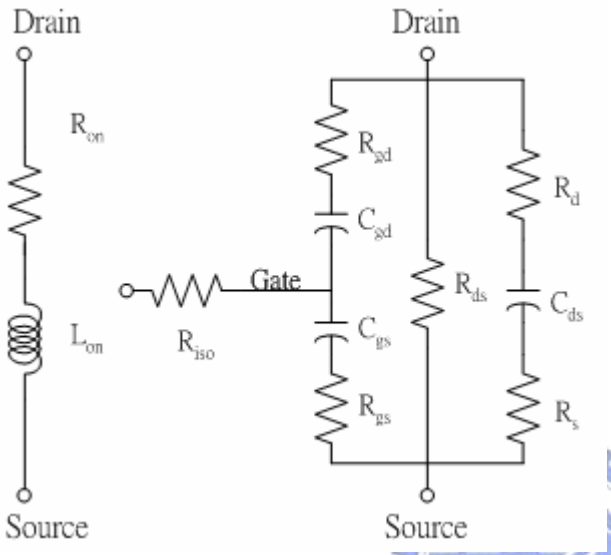
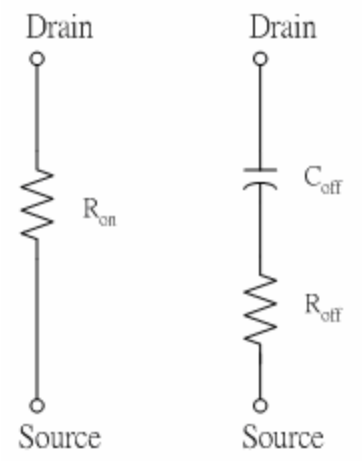


Fig. 4.3 The FET in switching configuration



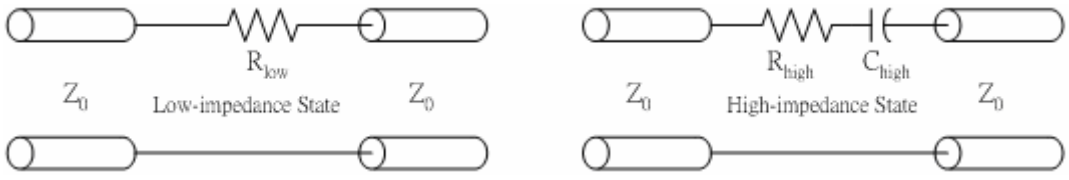
(a) (b)

Fig. 4.4 Complete equivalent circuit for :
(a) low-impedance state
(b) high-impedance state

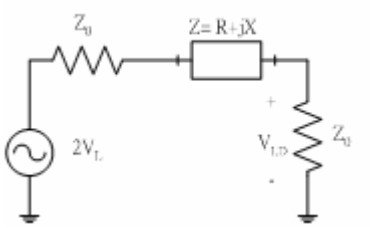


(a) (b)

Fig. 4.5 Simplified equivalent circuit for :
(a) low-impedance state
(b) high-impedance state

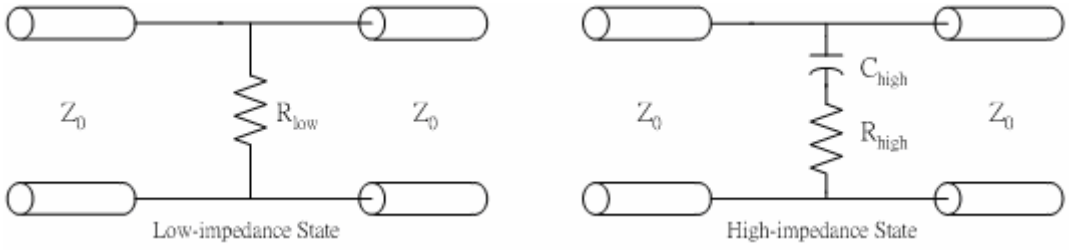


(a)

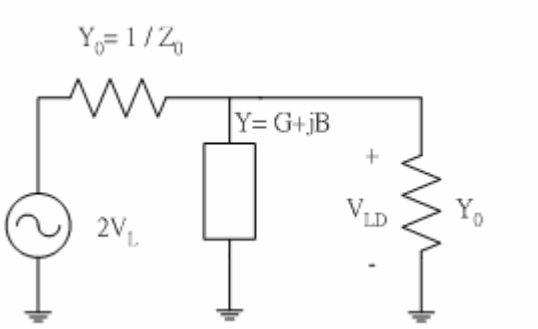


(b)

Fig. 4.6 Series-type switch configuration, (a) transmission line model, (b) equivalent circuit model

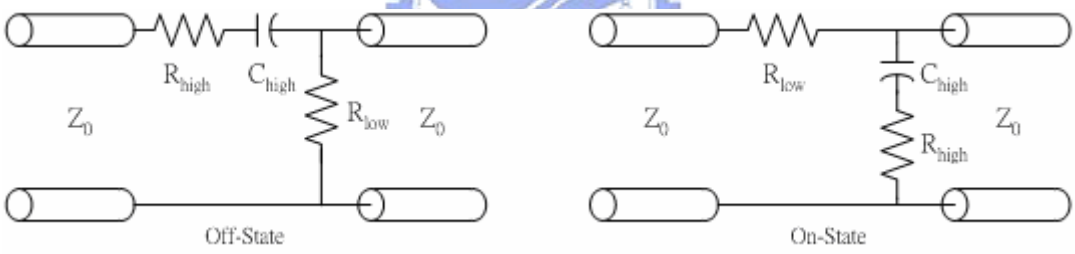


(a)

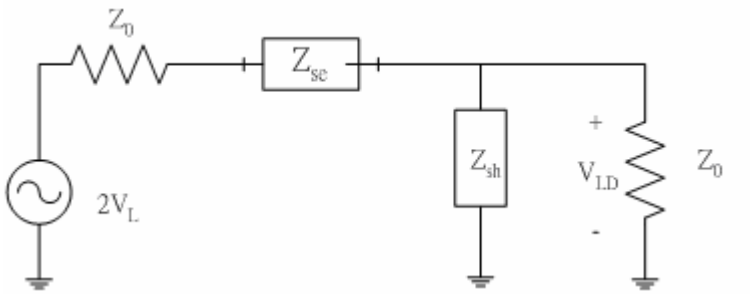


(b)

Fig. 4.7 Shunt-type switch configuration, (a) transmission line model, (b) equivalent circuit model

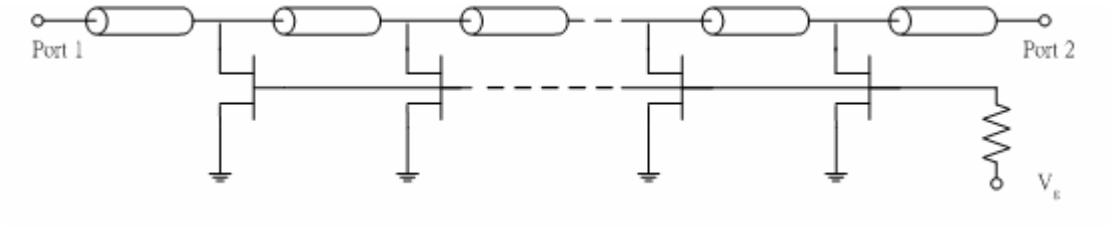


(a)

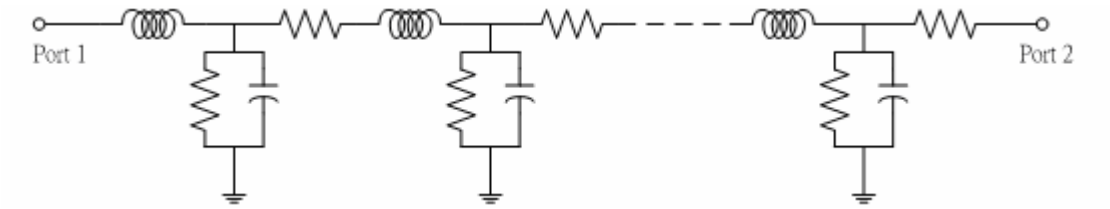


(b)

Fig. 4.8 Series-shunt switch configuration, (a) transmission line model, (b) equivalent circuit model

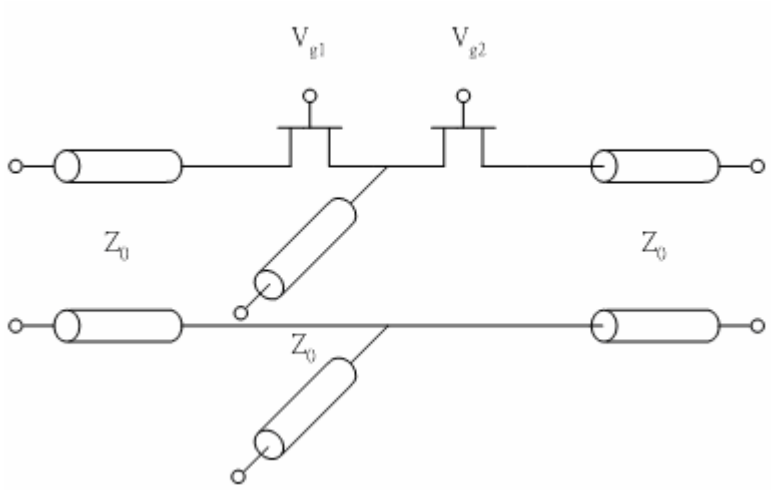


(a)

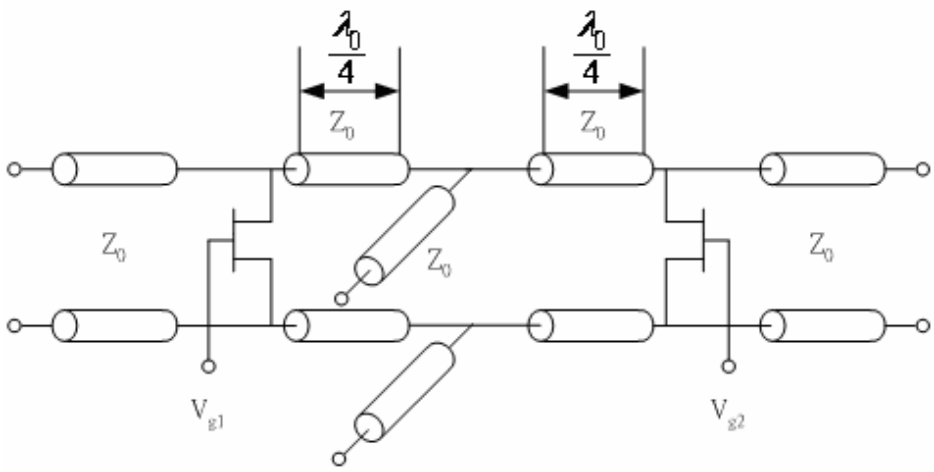


(b)

Fig. 4.9 (a) The circuit of traveling wave switch, (b) Equivalent circuit of TWSW



(a)



(b)

Fig. 4.10 The SPDT switch with, (a) series-type configuration, (b) shunt-type configuration

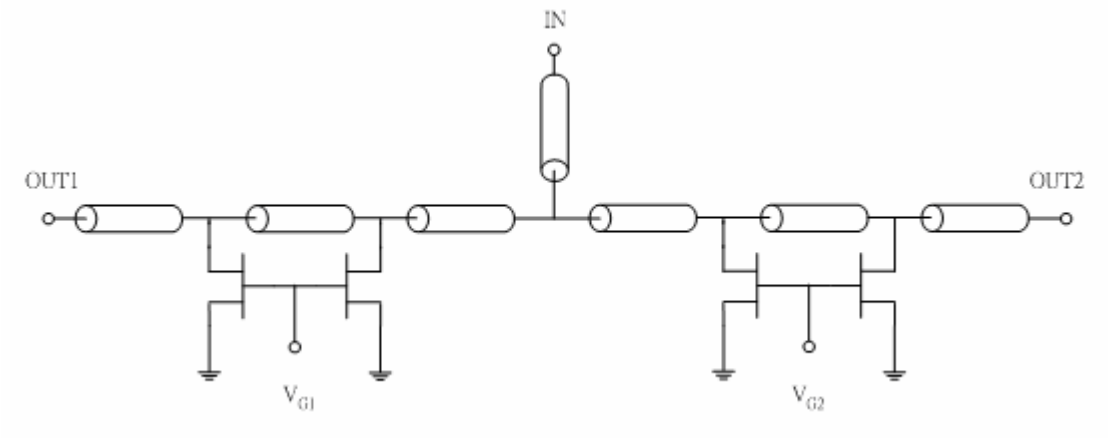


Fig. 4.11 Circuit diagram of the FET T-R switch

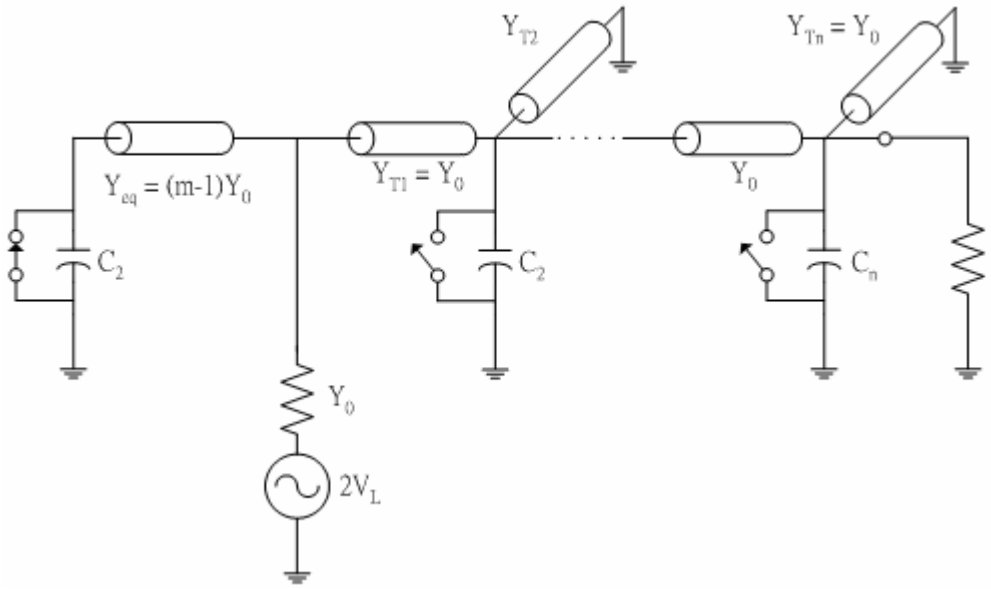


Fig. 4.12 The equivalent circuit of SPmT switch for transmission state

Chapter 5

New Broadband Switches using InGaAs pHEMT

5.1 Overview

In this chapter, a SPDT switch whose bandwidth is ranged from 33 to 60 GHz will be presented. It is based on the Mumford's and Fisher's theory that will be described later. The fabrication, design process and simulated results will be presented in the following. The SPDT is an extended concept of the SPST switch, so these results will be compared with the SPST switch which was designed by Y. Y. Chen [18]. The measurement considerations are also stated in detail. The measured data will be listed in the last.

5.2 MMIC foundry description

This SPDT switch is fabricated by WIN Semiconductor Corporation with a standard 0.15-um high-power InGaAs pHEMT MMIC process. The process uses a hybrid lithographic approach which includes direct-write electron beam (E-beam) lithography for sub-micron T-gate definition and optical lithography for the other process steps. The pHEMT devices are grown using molecular beam epitaxy (MBE) on 6-inch semi-insulating (SI) GaAs substrates. The pHEMT device has a typical unit current gain cutoff frequency (f_t) of 85 GHz and maximum oscillation frequency ($f_{\max}$) of 200 GHz. The peak DC transconductance (G_m) is 495 mS/mm when gate-source voltage is -0.45 V. The gate-drain breakdown voltage is 10 V, and the maximum drain current is 650 mA/mm when gate-source voltage is 0.5 V. This process also contains passive components such as thin-film resistor (TFR),

mesa-resistor (epitaxial layer), metal-insulator-metal (MIM) capacitors, spiral inductors and air bridges. The thickness of the wafer is 100 um for the backside metal plating and reactive ion etching (RIE) via-holes are used for DC grounding.

5.3 Broadband Switches Design

5.3.1 The basic theory of broadband switch

W. W. Mumford [19] published a design approach of a maximally flat filter. The filter, which is illustrated in Fig. 5.1, consists of the quarter-wavelength short-circuited stubs spaced by quarter wave-length distance. The characteristic admittance of each short stub can be examined by the table, is shown in Table 5.1, created by Mumford. The filters are symmetrical and only the normalized admittance are listed.

In 1965, R. E. Fisher [20] has suggested that the diode capacitance and its parallel resonating stub tuner could be analyzed approximately as a simple stub. J. F. White [21] demonstrated the feasibility of Fisher's equivalence for low frequencies from 1 to 2 GHz in 1968. In this thesis, Fisher's equivalence is also adopted except that the switching devices are replaced by the FETs and the frequencies are extended to the millimeter-wave frequency range.

The thesis of Fisher states that when the length of a transmission line whose admittance is Y_E is quarter wavelength, it can be replaced by a diode capacitance C shunted with a transmission line whose admittance is Y_T and phase delay is θ_T. The circuit model used for Fisher's equivalent circuit is shown in Fig. 5.2. The following gives the relationship between Y_E, Y_T, θ_T and the diode capacitance C.

$$Y_E = \frac{2}{\pi}\left\{\omega_0 C + Y_T\left[\cot^{-1}\left(\frac{\omega_0 C}{Y_T}\right)\right]\left[1+\left(\frac{\omega_0 C}{Y_T}\right)^2\right]\right\} \tag{2.9}$$

Fig. 5.3 is the plot for Y_T and θ_T versus $\omega_0 C / Y_E$. For a more accurate estimation, some corresponding variable values for the common steps in the estimation of $\omega_0 C / Y_E$ are listed in Table 5.2. If the diode capacitance C is zero which means the capacitance is not used, in other words the normalized susceptance $\omega_0 C / Y_E$ is zero, the phase delay and normalized admittance Y_T / Y_E of the required tuning stub is $90°$ and 1. The reason is that the phase delay of a quarter wavelength transmission line is $90°$. This thought is instinctive. The largest allowable value of $\omega_0 C / Y_E$ is $\pi / 4$. To look into the curves, Y_T / Y_E and θ_T are both zero when $\omega_0 C / Y_E$ is $\pi / 4$.

Combined the Mumford's and Fisher's theories, we can get the preliminary circuit of the switch. The equivalent circuit is shown in Fig. 5.4. The circuit structure is suitable for the design of the SPST switch, SPDT switch and even SPmT switch because all the off output arms can be simplified as short-circuited stubs with proper characteristic admittances. This speciality leads to keep the structure as the maximally flat filter, so the bandwidth will be unlimited by the quarter wavelength transformer.

5.3.2 Circuit design

The microstrip transmission line is used for the design of the circuit. The switching device is made by InGaAs pHEMT process whose gate width is 2 x 100 um. This SPDT utilizes two SPST switches [18] to shunt together. The SPST switch is composed of four short-circuited stubs and four transistors so it is called 4-order switch. Each of the transistors is shunt with a short-circuited stub and is spaced by quarter wavelength. The gate of each transistor is connected with a thin-film isolation

resistor R_{iso}. For the sake of isolating the noise to come into gate, the value of R_{iso} is chosen as large as possible , here we select it to be 2 KΩ. The gate control voltage (V_g) is set to be -2V for the high-impedance state and 0V for the low-impedance state.

In order to verify the bandwidth of SPDT switch has relation to the 4-order SPST switch, we have to design a 3-order SPDT switch. The reason is that the off arm can be equivalent to a short-circuited stub and this leads the on arm to be looked like a four-order SPST switch. The layout of the SPDT switch is achieved by Cadance tools with chip size 2 x 2 mm^2, as shown in Fig. 5.5.

5.3.3 Simulated results

The switching pHEMT model for this simulation is a HP EEsof scalable nonlinear HEMT model (EE_HEMT model) provided by the foundry. The S-parameters and harmonic balance techniques are simulated by Applied Wave Research (AWR) Microwave Office. The high frequency behavior was confirmed by the commercially available electromagnetic (EM) simulator SONNET.

The simulated insertion loss and return loss of ON-state from 20 GHz to 70 GHz is plotted in Fig. 5.6. The minimum insertion loss is -2.68 dB, and the bandwidth is defined in the range that the insertion loss is less than 4 dB. Therefore, the bandwidth is from 33 GHz to 60 GHz. The return loss is larger than 9.6 dB. The simulated isolation and return loss of OFF-state is illustrated in Fig. 5.7. The isolation is better than 32.7 dB and the output return loss is less than 2.7 dB. The total bandwidth is centered at 46.5GHz for a flat insertion loss.

5.3.4 Measurement considerations

The switch is operated in the frequency range of 33 GHz to 60 GHz which

includes of Q-band, V-band, the parasitic effect of the bonding wire is very significant. Therefore, we have to perform on-wafer measurement. The location of probe can't be arbitrarily placed without concern with the probe station. Each side of the probe station can only put one probe to ensure every probe having space to move. Because the SPDT switch has three ports, one for input and the other two is for out puts, there must be a right angle appeared in the layout. As a result, the calibration process will not be the same as usual. The ideal approach is to measure it via a vector network analyzer (VNA) which has more than three ports. Then, put the probe to a calibration kit which can be used to calibrate three ports and whose size is similar to the DUT. Because there is a 90° bend between three ports, it is hard to have a perfect through line. What mention above is difficult to achieve, so we use another method to measure it. Although this will make some inaccuracy, it is acceptable. The approach to this problem is to complete the 2 ports Through-Reflect-Line (TRL) calibration process. After that, move one probe to the side of input port and the other locates on the original side which is the same direction as output port. The 3rd port (also is output port) is terminated with 50Ω termination. Although this method may induce slightly inaccuracy, it is quite acceptable.

5.3.5 Measured results

The SPDT switch was measured via on-wafer probing. Fig. 5.8 presents the test setup used for the circuit measurement. There are 5 pads in the SPDT layout. Two are connected to control bias and one is for 50Ω termination, the other two are connected to the Vector Network Analyzer. The micro-photograph of the SPDT switch is shown in Fig. 5.9.

The control bias voltage is 0 V for the off-state and -2 V for the on-state. The measured insertion loss, input and output return loss of the on-arm is plotted in Fig.

5.10. The insertion loss is less than 4 dB and input and output return loss is better than 10 dB within 33 GHz to 55 GHz. The off-arm isolation, input and output return loss is illustrated in Fig. 5.11. The isolation is better than 30 dB from 30 to 70 GHz. It has 22 GHz bandwidth centered at 44 GHz for a flat insertion loss.

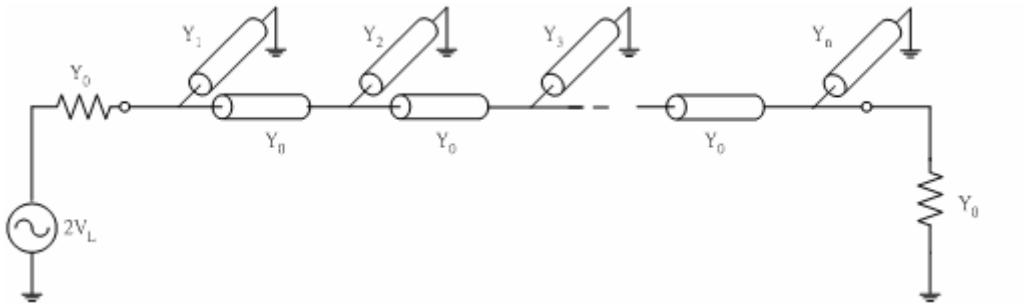


Fig. 5.1 Equivalent circuit for the maximally flat stub filter

	Y_1/Y_0	Y_2/Y_0
Three Stubs	0.100	0.200
	0.300	0.600
	0.500	1.000
	0.700	1.400
	1.000	2.000
	1.400	2.800
	2.000	4.000
	2.500	5.000
	3.000	6.000
Four Stubs	0.100	0.292
	0.200	0.571
	0.400	1.109
	0.800	2.141
	1.300	3.395
	1.900	4.877
	3.000	7.568

	Y_1/Y_0	Y_2/Y_0	Y_3/Y_0
Five Stubs	0.100	0.366	0.532
	0.200	0.694	0.989
	0.300	1.005	1.410
	0.400	1.304	1.808
	0.500	1.596	2.193
	0.700	2.166	2.933
	0.900	2.724	3.648
	1.300	3.819	5.038
	2.000	5.702	7.403
	2.800	7.829	10.058

Table 5.1 Mumford's design tables for the maximally flat stub filters

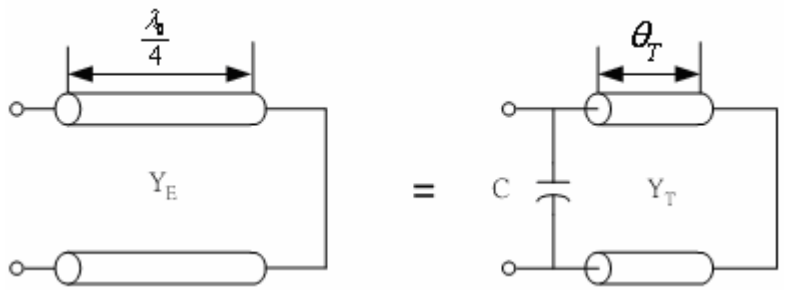


Fig. 5.2 Circuit model used for Fisher's equivalent circuit

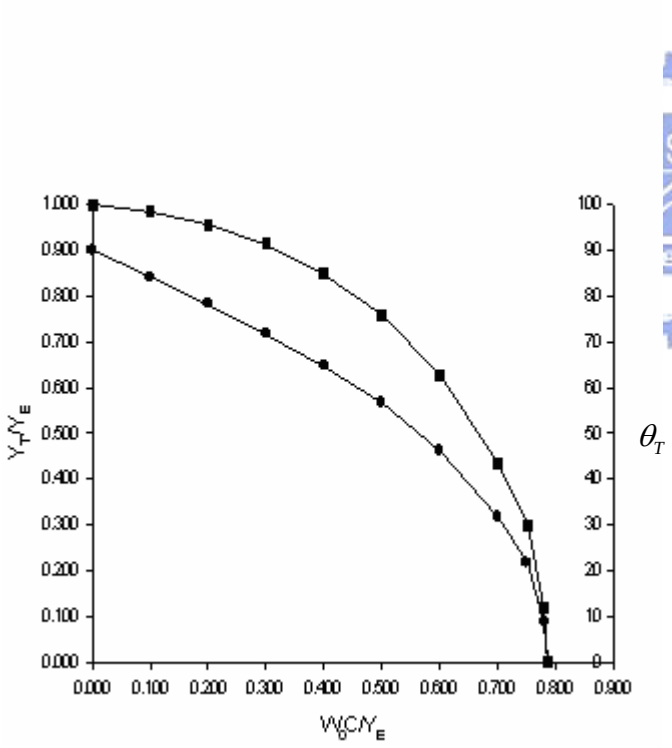


Fig. 5.3 Summary of Fisher's equivalence for simulating a quarter-wavelength stub with a capacitor and its parallel tuner

$\omega_0 C/Y_E$	Y_T/Y_E	θ_T (degree)
0.000	1.000	90.0
0.100	0.985	84.2
0.200	0.956	78.4
0.300	0.915	71.8
0.400	0.850	64.8
0.500	0.760	56.7
0.600	0.627	46.2
0.700	0.436	31.9
0.750	0.300	21.8
0.780	0.120	8.75
0.7854($\pi/4$)	0.000	0.00

Table 5.2 Tuned capacitor values for simulating a quarter-wavelength stub

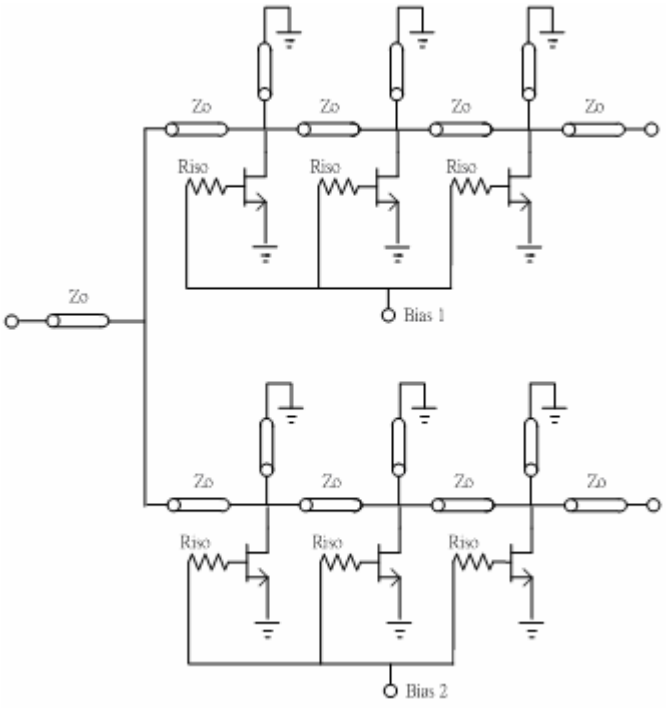


Fig. 5.4 The equivalent circuit of SPDT switch

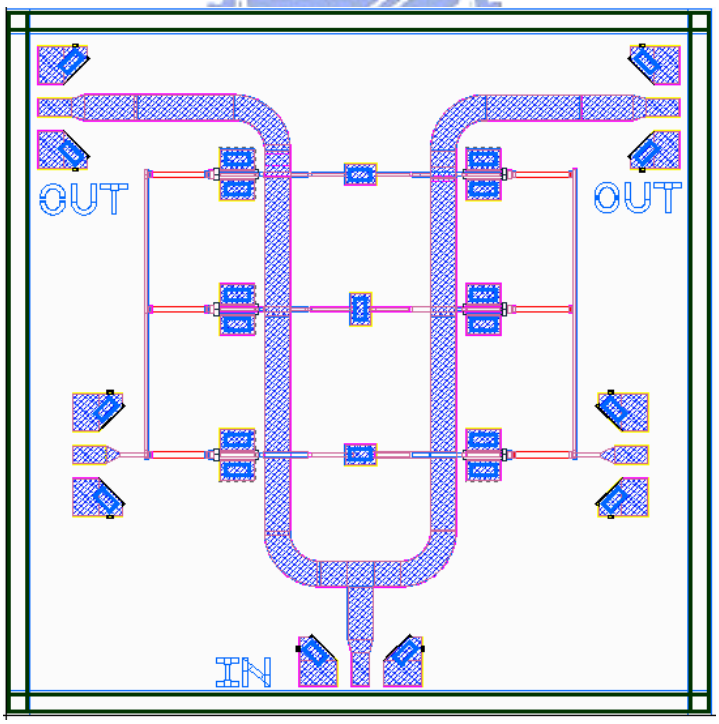


Fig. 5.5 Layout of the SPDT switch

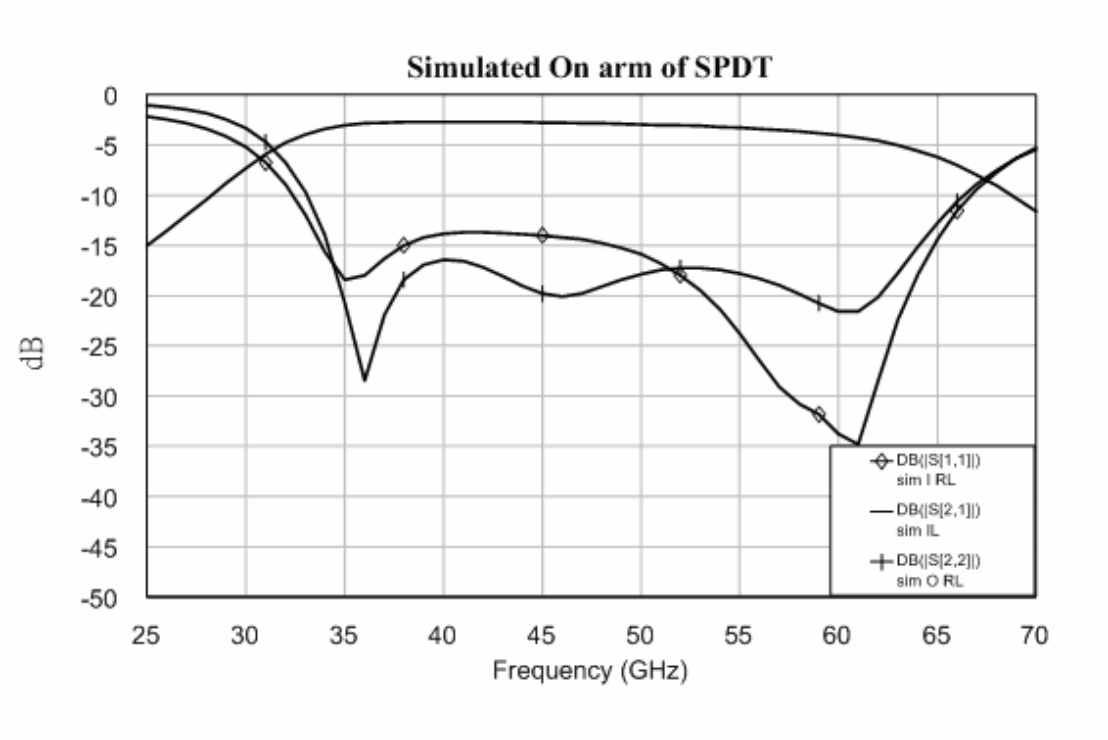


Fig. 5.6 The simulated return loss and insertion loss for the on-arm of the 33-to 60 GHz SPDT Switch

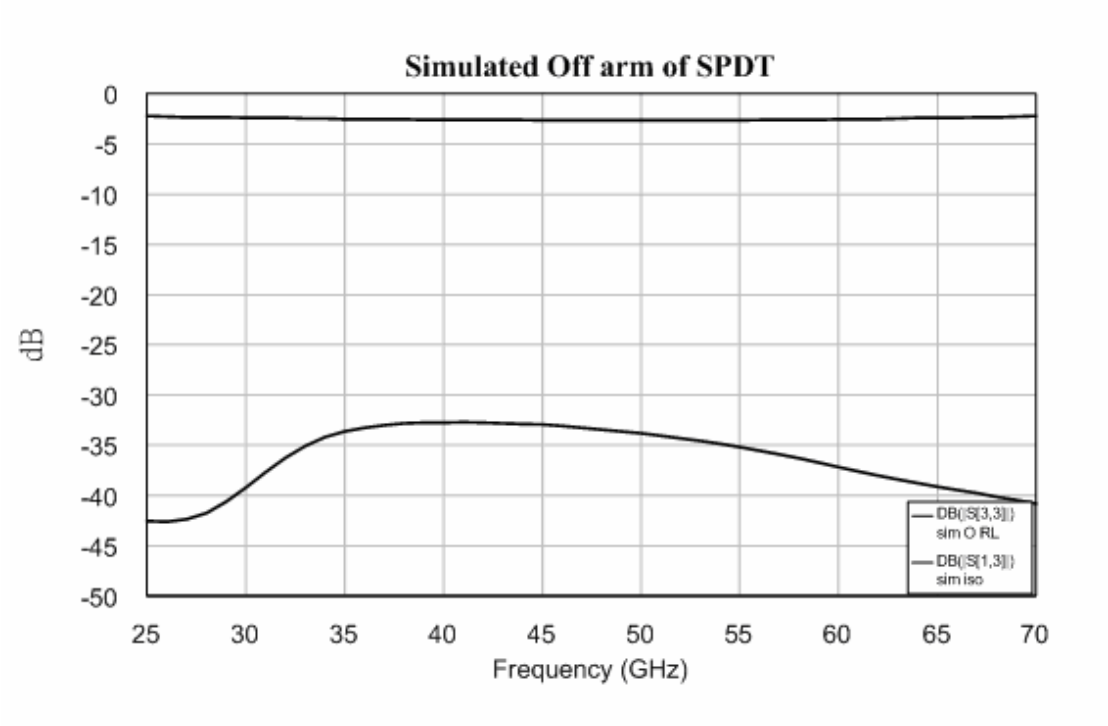


Fig. 5.7 The simulated return loss and isolation for the off-arm of the 33-to 60 GHz SPDT Switch

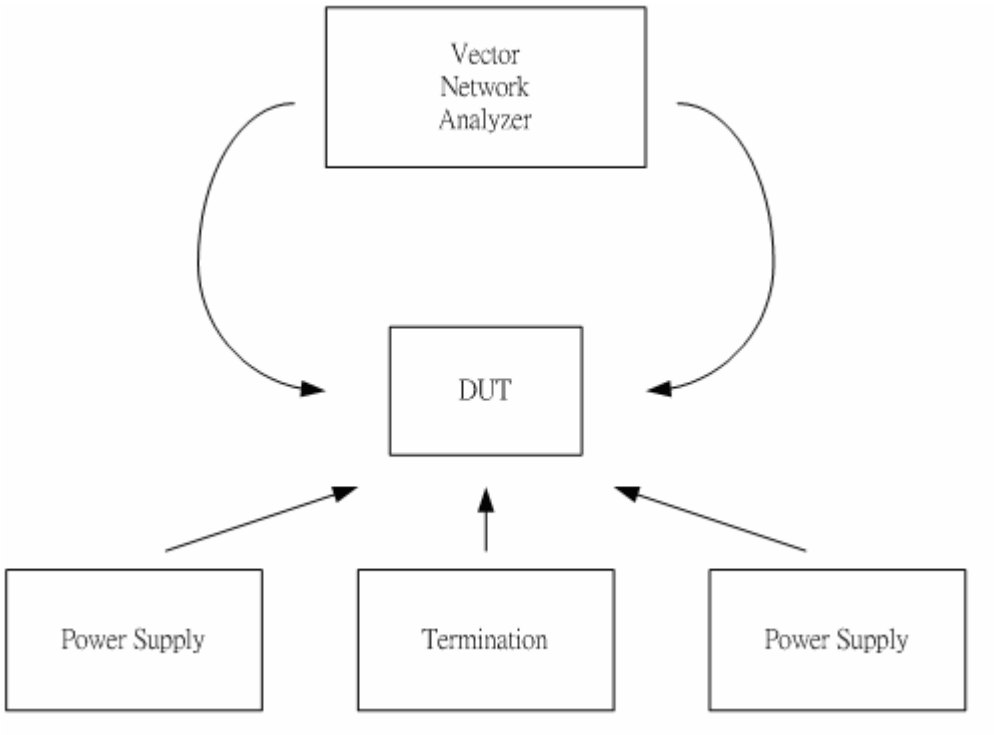


Fig. 5.8 The test setups for the S parameter measurement of the SPDT switch

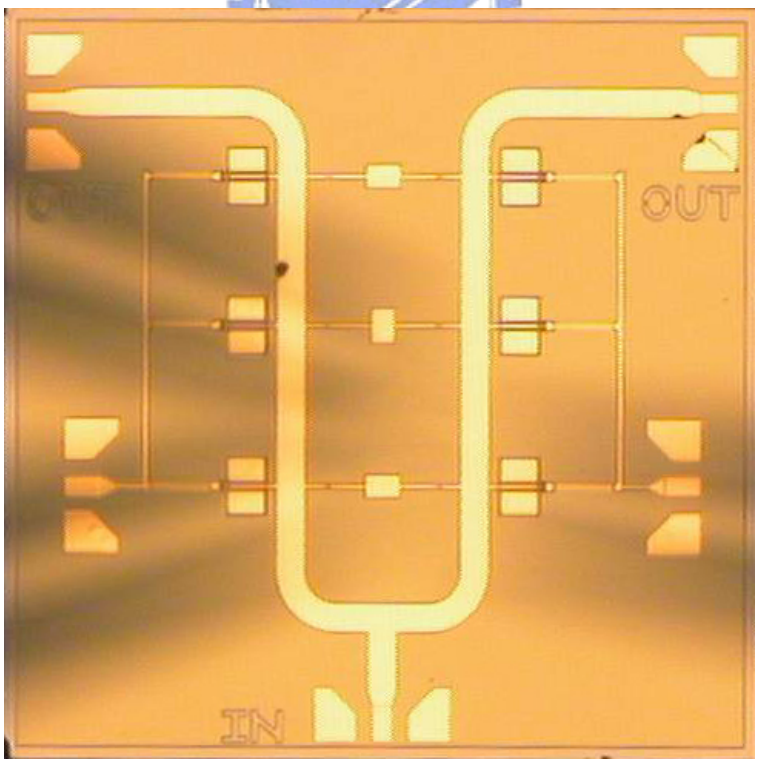


Fig. 5.9 The microphotograph of the SPDT switch

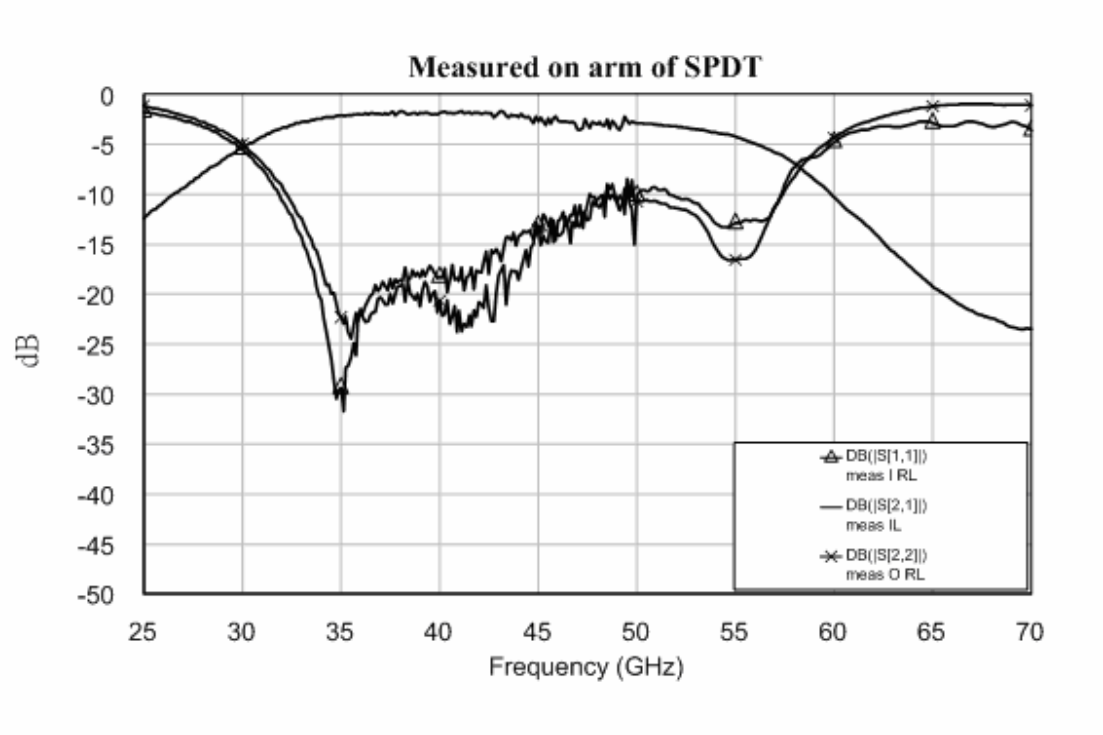


Fig. 5.10 The measured return loss and insertion loss for the on-arm of the 33-to 60 GHz SPDT Switch

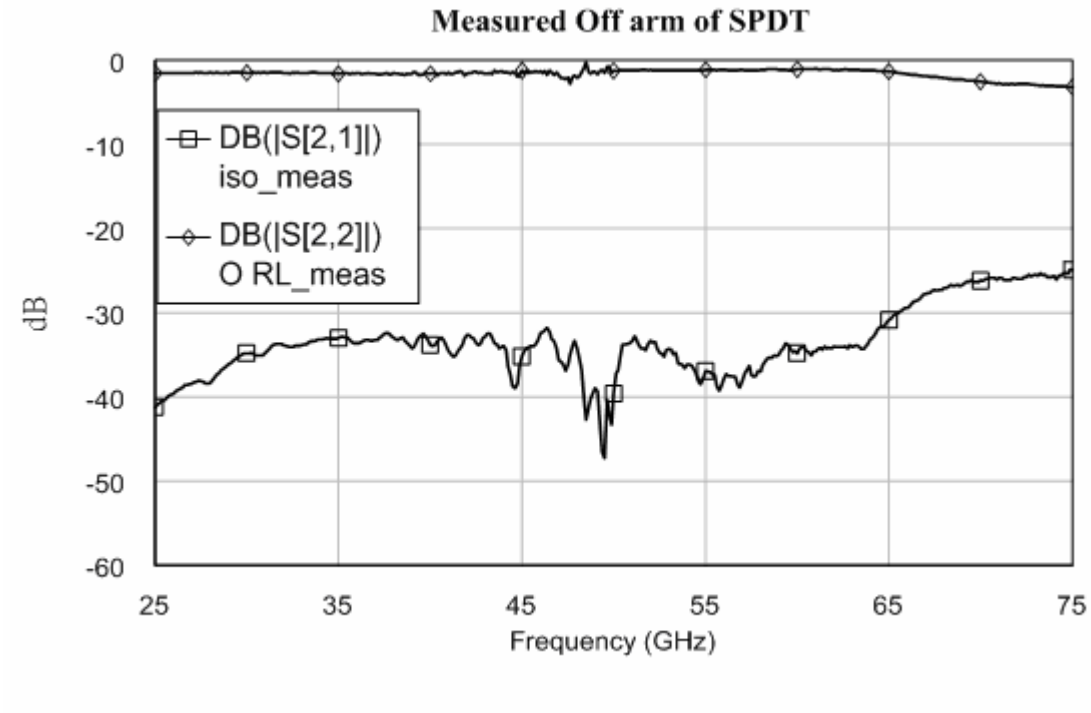


Fig. 5.11 The measured return loss and isolation for the off-arm of the 33-to 60 GHz SPDT Switch

Chapter 6

Conclusions

In this thesis, two integrated circuits are presented. One is using WIN InGaAs pHEMT and the other is using TSMC 0.18 um CMOS process.

A low-noise amplifier whose bandwidth is 2.6 GHz to 8.6 GHz is represented in Chapter 3. The gain of the LNA is 16 dB ± 1dB. The system's minimum noise figure is 5.58 dB at 3.5 GHz. The analysis of the noise figure is based on the existing analytical methods which are suitable for narrow bandwidth systems. Besides, the test methods to examine linearity, such as IIP3, are also developed for narrow bandwidth systems. It is necessary to develop a new analysis method for wideband systems in the future.

A 33 to 60 GHz single-pole double-throw switch is reported in Chapter 5. The insertion loss is less than 4 dB within the bandwidth and the best isolation is -32.6dB at 41 GHz. It has 27 GHz bandwidth centered at 46.5 GHz for a flat insertion loss. The measured result is a little different from the simulated. The measured bandwidth is from 33 to 55 GHz. The bandwidth reduces to 22 GHz and the center frequency is down to 44 GHz. The measured data dropped fast beyond 50 GHz resulting from the un-precise device model which is given by the foundry. Besides, the inaccurate calibration also affects seriously.

Because the circuits are operated at high frequency, the parasitic effects are very significant and the EM simulations should be considered completely. The input/output pads, transmission lines, passive and active devices should be totally included to guarantee the precision of the circuit. Since the design of the wideband switches utilizes the concept of the maximally flat filters, the distance between each

components are fixed. As for the UWB LNA, the distance between two components should be as short as possible in order to reduce the parasitics. The considerations of the layout for these circuits are different. The most important is that the input and output ports should be allocated at first to simplify the measurement setup, especially for the totally on-wafer probing tests. If the locations of ports are not proper, it will lead to increase the difficulty for measurements.

References

[1] I.D Robertson and S. Lucyszyn, RFIC and MMIC Design and Technology 2nd ed, Institution of Electrical Engineers, London, 2001.

[2] A. van der Ziel, Noise in Solid State Devices and Circuits, New York: Wiley, 1986.

[3] Shaeffer, D.K.; Lee, T.H., "A 1.5-V, 1.5-GHz CMOS low noise amplifier", Solid-State Circuits, IEEE Journal of Volume 32, Issue 5, May 1997 Page(s):745 – 759

[4] Andreani, P.; Sjoland, H., "Noise optimization of an inductively degenerated CMOS low noise amplifier", Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on Volume 48, Issue 9, Sept. 2001 Page(s):835 - 841

[5] Bevilacqua, A.; Niknejad, A.M., "An ultra-wideband CMOS LNA for 3.1 to 10.6 GHz wireless receivers", Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International, 15-19 Feb. 2004 Page(s):382 - 533 Vol.1

[6] Vishwakarma, S.; Sungyong Jung; Youngjoong Joo, "Ultra wideband CMOS low noise amplifier with active input matching", Ultra Wideband Systems, 2004. Joint with Conference on Ultrawideband Systems and Technologies. Joint UWBST & IWUWBS. 2004 International Workshop on 18-21 May 2004 Page(s):415 – 419

[7] Sangyoub Lee, "Design and Analysis of Ultra-Wide Bandwidth Impulse Radio Receiver", A dissertation presented to the faculty of southern California in partial fulfillment of the requirements for the degree doctor of philosophy, August 2002.

[8] TSMC 0.18 um mixed signal 1P6M + MIM salicide 1.8V/3.3V design guideline

[9] Wei Meng Lim; Manh Anh Do; Jian Guo Ma; Kiat Seng Yeo, " A broadband CMOS LNA for WLAN applications", Ultra Wideband Systems and Technologies, 2003 IEEE Conference on 16-19 Nov. 2003 Page(s):42 - 46

[10] Y. Ayasli, "Microwave Switching with GaAs FETs", Microwave J., Vol. 25, pp. 61-71, Nov. 1982.

[11] M.J. Schindler and A. Morris, "DC-40 GHz and 20-40 GHz MMIC SPDT switches", IEEE Trans. On Microwave Theory and Techniques, Vol. MTT-35, pp. 1486-1493, Dec. 1987.

[12] A. Gopinath and J. Rankin, "GaAs FET RF Switches", IEEE Trans. On Electron

Devices, Vol. ED-32, pp. 1272-1278, July 1985

[13] I. Bahl and P. Bhartia, Microwave Solid-State Circuit Design, Wiley Interscience, N.Y. 1988

[14] Madihian, M.; Desclos, L.; Maruhashi, K.; Onda, K.; Kuzuhara, M., "A sub-nanosecond resonant-type monolithic T/R switch for millimeter-wave systems applications", Microwave Theory and Techniques, IEEE Transactions on Volume 46, Issue 7, July 1998 Page(s):1016 – 1019

[15] Kun-You Lin; Yu-Jiu Wang; Dow-Chih Niu; Huei Wang, "Millimeter-wave MMIC single-pole-double-throw passive HEMT switches using impedance-transformation networks", Microwave Theory and Techniques, IEEE Transactions on Volume 51, Issue 4, April 2003 Page(s):1076 – 1085

[16] Mizutani, H.; Takayama, Y., "DC-110-GHz MMIC traveling-wave switch", Microwave Theory and Techniques, IEEE Transactions on Volume 48, Issue 5, May 2000 Page(s):840 – 845

[17] G. L. Lan, D. L. Dunn, J. C. Chen, C. K. Pao and D. C. Wang, "A High Performance V-Band Monolithic FET Transmit-Receive Switch", IEEE 1988 Microwave and Millimeter-Wave Monolithic Circuits Symposium

[18] Yang-Yu Chen, "Design of Millimeter-Wave Frequency Doubler and New Broadband Switches using InGaAs pHEMT", A thesis submitted to institute of communication engineering college of electrical engineering and computer science National Chiao Tung University in Partial Fulfillment of the Requirements for the degree of master science in communication engineering, June 2004.

[19] W. W. Mumford, " Tables of Stub Admittances for Maximally Flat Filters Using Shorted Quarter Wave Stubs", IEEE Trans. On Microwave Theory and Techniques, Vol. MIT-13, No. 5, pp. 695-696, Sept. 1965.

[20] R.E Fisher, "Broadbanding Microwave Diode Switches", IEEE Trans. On Microwave Theory and Techniques, Vol. MTT-13, No. 5, pp. 706, Sept. 1965.

[21] J. F. White and K. E. Mortenson, "Diode SPDT Switching at High Power with Octave Microwave Bandwidth", IEEE Trans. On Microwave Theory and Techniques, Vol. MIT-16, No. 1, pp. 30-36, Jan, 1968.