國 立 交 通 大 學

電信工程學系

碩 士 論 文

應用於 Serial ATA II 之 1V 3GHz 展頻時脈產生器

A 1V 3GHz Spread Spectrum Clock Generator for Serial ATA II

研究生：莊誌倫

指導教授：洪崇智 博士

中 華 民 國 95 年 1 月

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摘　　要

高速電子儀器所產生的高頻電磁雜訊干擾(Electro-Magnetic Interference, EMI)常常會影響到其他電路的運作。傳統的解決方法是將電磁雜訊干擾加以屏蔽，或是控制時脈信號的上升速度，但是缺點是昂貴的成本與龐大的體積。現代的解決方法是直接在晶片上降低電磁雜訊干擾，以達到低成本與高彈性空間。

改變時脈信號的中心頻率是最常被採用的方法。這種方法被稱為展頻時脈技術(Spread Spectrum Clocking)，因為時脈信號的頻譜被展開成較寬的頻帶。然而，由於除數上的規律性，造成了頻譜上明顯的突波。因此，在這本論文中，我們使用了高階的 ΣΔ 調變器來打散除法器除數的規律性，並將雜訊移往更高的頻帶。最後，我們可利用鎖相迴路閉迴路的特性將高頻的雜訊濾除。

將互補式金氧半製程的鎖相迴路應用於低電壓，高頻率之系統中是另外一項困難的任務。然而，隨著製程進步，電晶體越做越小，低電壓已經是一項必須面臨的驅勢。對於系統晶片整合(System-On-a-Chip, SOC)而言，類比電路必

須與數位電路整合在同一晶片。因此，將類比電路操作在與數位電路同樣的低電壓下更是重要的。我們也提出了一個應用於第二代 SATA 系統之展頻時脈產生器。經由模擬驗證，可從 3GHz 向下展頻 5000ppm，並且提供超過 14dB 的訊號振幅衰減量。

A 1V 3GHz Spread Spectrum Clock Generator for Serial ATA II

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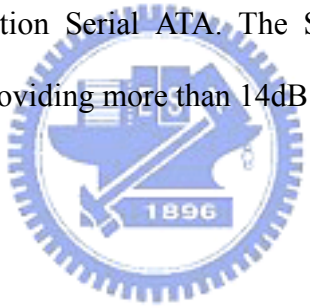
ABSTRACT

Electronic equipments often generate Electric-Magnetic Interference (EMI) that affects the operation of other equipments. In a portable device, the high-speed interfaces between peripheral storages and the other signal processing units are the main noise sources. The conventional techniques to reduce EMI tend to enclose or reduce the amount of the generated radiation, such as shield cables and coaxial wires, but are usually costly and bulky. Modern EMI reduction is done on-chip without using heavy shielding materials to the goal of low-cost and flexibility.

Altering the center frequency of internal clocks is a widely adopted EMI reduction technique. The technique is called Spread Spectrum Clocking (SSC) because the spectrum of the clock is spread over a broader range. Serial ATA (SATA) specification defines an EMI reduction method using SSC. Several papers have discussed the EMI reduction using SSC [1][2]. However, because of the non-random

and regular sequence of the divider modulus, the unwanted spur is obvious in the frequency spectrum of the clock. Therefore, in this thesis, we use a higher-order ΣΔ modulator to randomize the divider modulus and remove the spur to high frequency. In the end, we can also filter out the unwanted noise with the closed loop behavior of the PLL.

The application of CMOS PLL in low voltage and high frequency is crucial. With the reduction of the device feature size, a low supply voltage is a basic requirement. For System-On-a-Chip (SOC) design, analog circuits are necessary to be integrated with digital circuits. Therefore, it is significant for analog circuits to operate at the same low supply voltage as digital circuits. Here, we propose a 1V CMOS SSCG for 2nd generation Serial ATA. The SSCG achieves down spread 5000ppm from 3GHz while providing more than 14dB of power attenuation.



誌　　謝

這兩年的碩士生涯在我的人生道路上，有著不可抹滅的影響。在這兩年中，有著許多的挫折與失望，也有著許多快樂與樂趣。這之中的過程，讓我的心靈成長許多，也讓我的抗壓性越來越強，讓我做好了準備，以面對將來的挑戰。

在這裡我要先謝謝我的指導教授洪崇智博士。老師亦師亦友的關懷，在課業上適時的點出我的問題，並提供正確的方向，讓我更快邁向成功的一步。在生活上也能關心我們的休閒生活，讓我們永遠保持體力的最佳狀態。老師這兩年的指導與關心，點點滴滴令我由衷感激。另承蒙劉萬榮教授，黃淑淑絹教授，陳富強教授對本論文的諸多指導與建議，使其更驅完整與正確，在這裡謝謝每一位老師。

感謝羅天佑學長在這兩年的幫助與指導，讓我在求學路上能夠更順利。感恩我的同學，張家瑋，李三益，邱俊宏，楊峻岳。雖然我們是第一屆，但是由於大家的努力與鼓舞，我們終於還是完成我們的論文，謝謝大家。感謝我的室友，顏欽賢，楊松根， 陳昭霖。因為你們，我的生活充滿了許多歡樂與溫暖。尤其感謝顏欽賢，從你身上學到許多做人處事的道理，謝謝你。還有許多學弟們，為這實驗室帶來許多歡笑與活力，也讓我們在苦樂中研究，歡樂中成長。

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感謝所有曾經幫助過我的人，帶給我成長，帶給我歡笑，感謝我生命中所有的人事物，謝謝你們。

莊誌倫

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Chapter 1

Introduction

1.1 Motivation

With the development of computer systems, the operation speed is becoming more and more rapid. However, this means there are many higher order harmonics in the signal. These signals often generate Electric-Magnetic Interference (EMI) that affects the operation of other equipments. In a portable device, the high-speed interfaces between peripheral storages and the other signal processing units are the main noise sources. When the operation speed is higher, the EMI problem is more severe.

The conventional techniques to reduce EMI tend to enclose or reduce the amount of the generated radiation, such as shield cables and coaxial wires, but are usually costly and bulky. Modern EMI reduction is done on-chip without using heavy shielding materials to the goal of low-cost and flexibility.

Altering the center frequency of internal clocks is a widely adopted EMI reduction technique. The technique is called Spread Spectrum Clocking (SSC) because the spectrum of the clock is spread over a broader range. With spread spectrum modulation, the energy peak of every harmonic component in the spectrum is reduced. Serial ATA (SATA) specification defines an EMI reduction method using

SSC, which limits the peak emission at any given frequency, not the average emission. However, because of the non-random and regular sequence of the divider modulus, the unwanted spur is obvious in the frequency spectrum of the clock. Therefore, in this thesis, we use a fractional-N PLL with a higher-order ΣΔ modulator to randomize the divider modulus and remove the spur to higher frequencies. In the end, we can also filter out the unwanted noise with the closed loop behavior of the PLL. Besides, there are many advantages of fractional-N PLL using ΣΔ modulation, such as arbitrarily small frequency resolution, wide bandwidth, small lock time and fast switching speed.

The application of CMOS PLL in low voltage and high frequency is crucial. With the reduction of the device feature size, a low supply voltage is a basic requirement. For System-On-a-Chip (SOC) design, analog circuits are necessary to be integrated with digital circuits. Therefore, it is significant for analog circuits to operate at the same low supply voltage as digital circuits. Here, we propose a 1V CMOS SSCG for 2nd generation Serial ATA. The SSCG achieves down spread 5000ppm from 3GHz while providing more than 14dB of power attenuation.

1.2 Thesis Organization

This thesis introduces the basics of PLL and the idea of the ΣΔ modulator. Besides, spread spectrum clocking is also explained in detail. The thesis is organized as follows:

Chapter 2 begins with the brief introduction of the charge-pump PLL. The most significant part describes how to analysis PLL in their linear model. We discuss the open loop transfer function as well as closed loop transfer function. Finally, we

describe the phase noise of PLL using Leeson's Model to decide the optima bandwidth.

In Chapter 3, we describe the idea of fractional-N PLL. The most important part is the principles of ΣΔ modulators. We also derive its analytic function to prove the abilities of randomization and noise shaping.

Chapter 4 begins with the introduction to EMI problem and several solutions used for the EMI reduction. The most significant part explains the concept of spread spectrum using frequency modulation technology. Other parameters, like modulation profile and modulation frequency and timing impacts, are also discussed.

In Chapter 5, a 1V 3GHz spread spectrum clock generator using fractional-N PLL is presented. The fractional-N is fabricated in 0.18μm CMOS 1P6M process. We first introduce the architecture of the proposed spread spectrum clock generator and the behavior simulation in MATLAB. The following sections contain the circuit descriptions of each building block. At last, we show the test setup and the experiment results.

Chapter6 gives conclusions to this work, in which fractional-N based SSCG is designed. Suggestions for future works are recommended at the ending of this thesis.

Chapter 2

Principles of Phase-Locked Loop

2.1 Introduction to PLL

Due to the demand for higher performance and lower cost in electronic systems, and the advance of integrated-circuit (IC) technologies in terms of speed and complexity, Phase-locked loop (PLL) become more and more popular in the last twenty years. PLL finds wide application in areas such as communications, wireless systems, and disk drive electronics. A PLL is a circuit that causes a particular system to track with another one. In other words, a PLL is a circuit synchronizing an output signal with a reference in frequency as well as in phase. In the locked state, the phase error between the oscillator's output signal and the reference signal is zero, or remains constant.

If a phase error builds up, the feedback system of PLL will act on the oscillator such that the phase error will be reduced to a minimum. Finally, the phase of the output signal is again locked to the phase of the input signal. That is why we call it as phase-locked loop.

The main functions of PLL are as follows:

1. Jitter reduction. Signals often suffer from random jitter as they are transferred through a communication channel. The PLL can be used to avoid such

jitter by its self feedback system.

2. Skew suppression. A on-chip clock CKs enters a chip from a printed-circuit board (PCB) and is buffered to drive the load capacitance and interconnection capacitance. Thus, the inter-chip clock CKc would exhibit significant delay with respect to CKs, as depicted in Fig. 2.1. The consequent skew makes a limitation in operation speed between on-chip and inter-chip.

3. Frequency synthesizer. With the development of wireless communication, we need to produce any precise step frequency to receive the signal that we want. For example, the 802.11a needs 5180~5320MHz, with steps of 20MHz. By choosing the proper reference frequency and changing the divider modulus, we can synthesize several frequencies that we need.

4. Clock recovery. In the most cases, the transmitter only sent data to the receivers without additional timing reference. However, the receiver must process the data synchronously. So we can use clock and data recovery (CDR) to get the clock information and thus process data correctly. The CDR could be PLL-based or over-sampling-based.

5. Modulation and demodulation. PLL can be used to achieve phase modulation and demodulation. Besides, it also could be used to make frequency demodulation.

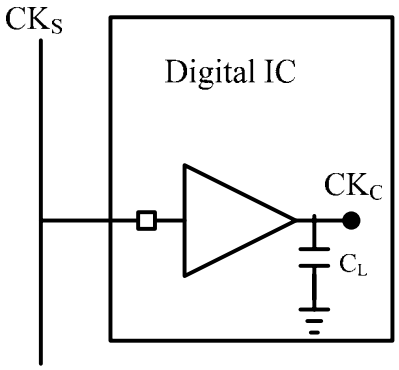


Fig. 2.1 Clock skew in a digital system

2.2 Brief History

The very first phase-locked loops were implemented as early as 1932 by Bellescize; this French engineer is considered the inventor of "coherent communication." However, The PLL found industrial applications only when it became available as an IC. The first PLL ICs appeared around 1965 and were called linear PLL (LPLL), because each block is analog device. An analog multiplier was used as the phase detector; the loop filter was built from a passive or active RC filter. In the following years the very first digital PLL (DPLL) was invented in 1970. It is in effect a hybrid device. The only digital circuit is phase detector, e.g., made from an EXOR gate or a JK-flipflop. But the remaining blocks were still analog. A few years latter, the "all-digital" PLL (ADPLL) was invented. Each block is digital. The loop filter is from Up/Down counter. The VCO is from DCO. Finally, software PLL was presented. The PLL functions are performed by a computer program rather than a piece of specialized hardware.

2.3 Basic Operations in PLL

A typical PLL consist of five parts: phase/frequency detector (PFD), charge pump (CP), loop filter (LF), voltage-controlled oscillator (VCO) and frequency divider.

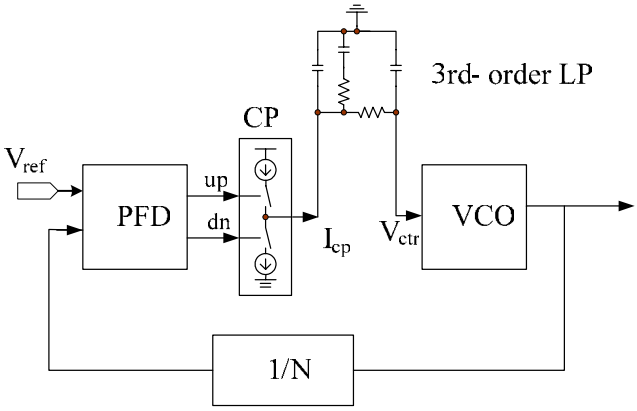


Fig. 2.2 The block diagram of simplest PLL

The principle of the PLL is as follows: the PFD compares the frequency and phase errors between the reference signal and the feedback signal, thus producing digital up or down signals to control the CP. The CP would change the digital signals to the corresponding analog voltage signals. After that, the LP filters out the higher frequencies of the voltage signals and preserve the lower frequencies components. The resulting voltage is used to control the frequency of VCO. The output signal of VCO would pass through the frequency divider and be fed into the PFD again. Therefore the PLL will continuously compare the two signal's frequencies until they are equal. We called that it is locked.

Although the operation of acquisition is nonlinear, the operation close to be locked is almost linear. So we will derive the linear model of each block first.

2.3.1 Phase/Frequency Detector and Charge Pump

The traditional phase detector compares the phases of the reference signal and the feedback signal. But it suffers from a severe problem: the acquisition range is on the order of w_{LPF}. In other words, the loop locks only if the difference between w_{ref} and w_{out} is less than roughly w_{LPF}.

In order to solve the acquisition problem, modern PLL incorporate frequency

detection in addition to phase detection. At the beginning, the FD makes w_{out} toward w_{ref} while the PD remains disable. When w_{out} is closed to the w_{ref}, the PD becomes the dominant part to compare the phases. Such a scheme increases the acquisition range to the tuning range of the VCO.

For periodic signals, we can combine the two loops of Fig. by creating a circuit that can detect both phase and frequency difference. We call it as tri-state phase/frequency detector (PFD), as illustrated in Fig. 2.3. If Q_A=Q_B=0, and REF goes high, Q_A rises. Next, if this event is followed by a rising transition on DIV, Q_B goes high and the AND gate resets both flip-flops and vice versa. Fig. 2.4 shows the timing diagram of tri-state PFD and Fig. 2.5 shows its state diagram.

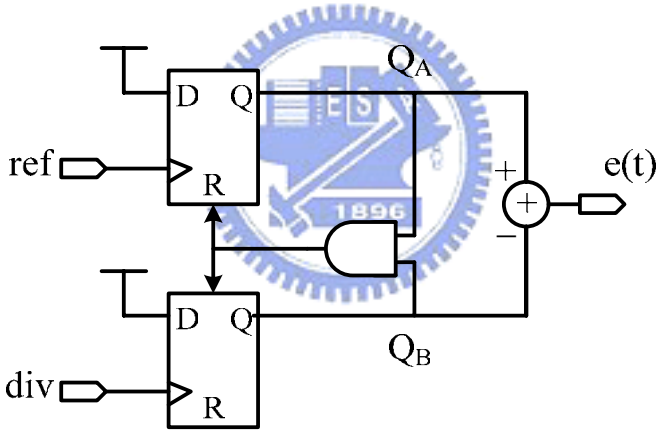


Fig. 2.3 Architecture of tri-state PFD

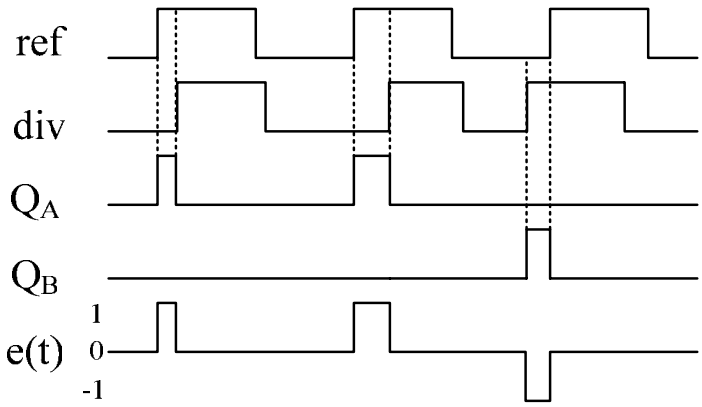


Fig. 2.4 timing diagram of tri-state PFD

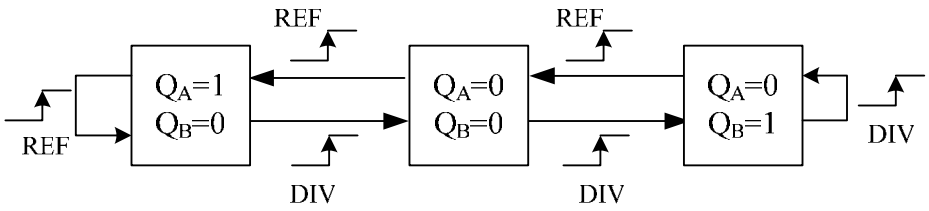


Fig. 2.5 State diagram for PFD

We define the output as the average value of e(t), which is the difference of Q_A and Q_B, and the input as the phase error between REF and DIV. We derive the tri-state PFD characteristic, as shown in Fig. 2.6. In addition to its wide detection range of $\pm 2\pi$, we note that phase error characteristic is asymmetric about zero phase. Such a characteristic allows positive frequency differences to be distinguished from negative frequency differences. So the average value is now positive or negative according to the sign of frequency offset and the PLL will always relock.

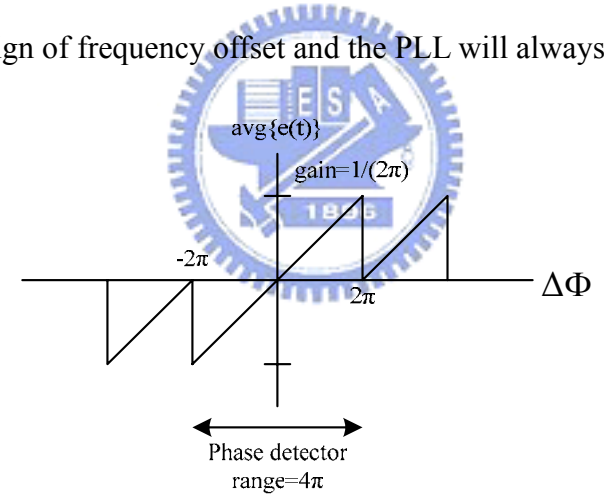


Fig. 2.6 Tri-state PFD characteristic

The Charge Pump (CP) is an analog circuit that converts the Q_A and Q_B signals to the corresponding variation in the control voltage of the VCO. A simple model is as shown in Fig. 2.7. When Q_A is high and Q_B is low, the switch S_1 is on and S_2 is off. Then the I_{UP} charges the output capacitor and the voltage rises. On the contrary, if Q_A is low and Q_B is high, the switch S_1 is off and S_2 is on. Then the I_{DN} discharges the output capacitor and the voltage falls. If both Q_A and Q_B are low, both switches are off and the output voltage is floating. If both Q_A and Q_B are high, the both

switches are on. In the ideal situation, I_{UP} is equal to I_{DN}, so the output voltage remains unchanged.

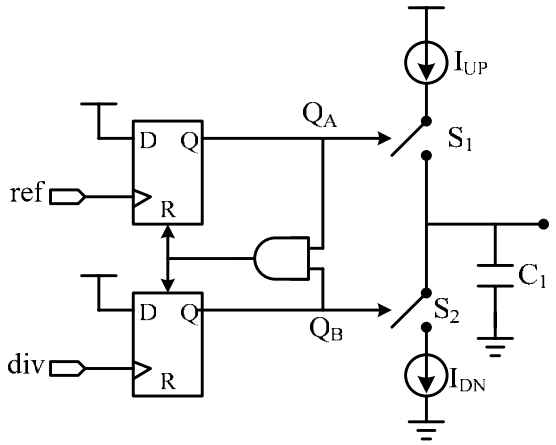


Fig. 2.7 PFD with charge pump

A noticeable problem is the dead zone when we discuss the PFD combined with CP. Due to the parasitic capacitance at the switches, the Q_A or Q_B may not have enough time to reach its logic high value to turn on the switch. That is, if the phase error is below some small value ϕ_0 ., the switch will not be turned on, and the CP will not charge or discharge the control voltage. The control voltage will be floating and no longer a function of $\Delta\phi$. The VCO will accumulate as much random phase error as ϕ_0 to be able to turn on switches. Therefore it will cause jitter in the VCO's output. One way to solve such a problem is to increase the reset time of the PFD. If the pulse is long enough to turn on the switch at $\Delta\phi$=0, it is able to produce the proportional net current with respect to little increment in the phase difference.

If the charge or discharge current of CP is I_P, the phase error between REF and DIV is $\Delta\phi$, the average error current in a cycle is I_e .

$$I_e = \frac{\Delta\phi}{2\pi} I_p \tag{2.1}$$

(2.2)

2.3.2 Voltage Controlled Oscillator

Many applications need that the oscillators be “tunable”. The most popular circuit is the voltage-controlled oscillator, whose frequency is a linear function of its input control voltage. The transfer function is as follows:

$$\omega_{out} = \omega_0 + K_{VCO} V_{cont} \tag{2.3}$$

Here ω_0 is the free running frequency, K_{VCO} is gain or sensitivity of the VCO, (usually in rad/s/V). Next, we want to derive the phase transfer function:

$$\int \omega_{out} = \omega_0 t + K_{VCO} \int V_{cont} dt \tag{2.4}$$

Only the second term of the total phase is of interest. We call $K_{VCO}\int_0^t V_{cont} dt$ as the “excess phase”, denoted by ϕ_{ex}. In fact, in the analysis of PLLs, we respect the VCO as a system whose input as the control voltage and output as the excess phase. If the system is LTI, then we get:

$$\phi_{ex} = K_{VCO} \int V_{cont} dt \tag{2.5}$$

$$\frac{\phi_{ex}}{V_{cont}} = \frac{K_{VCO}}{s} \tag{2.6}$$

Therefore the VCO acts as an ideal integrator, providing a pole at $s = 0$ in the open loop transfer function in the PLL.

2.3.3 Loop Filter

As we discussed earlier, the dc component of the control voltage is proportional to phase error ΔΦ. So we need a low pass filter to avoid unwanted frequency terms, i.e. $2w_{ref}$, $3w_{ref}$, etc. The simplest LPF is to connect a capacitor to the control

voltage. The open-loop transfer function is derived as follows:

$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_p}{2\pi C_p}\frac{1}{s} \tag{2.7}$$

$$\frac{\phi_{out}}{\phi_{out}}(s)\Big|_{open} = \frac{I_p}{2\pi C_p}\frac{K_{vco}}{s^2} \tag{2.8}$$

Since the loop gain has two poles at the origin, this topology is called a “type II” PLL. It is unstable because the loop gain has two poles at the origin. As illustrated in Fig. 2.8(a), each integrator provides constant 90° phase shift. Thus the system will oscillate at the unit-gain frequency. So, we have to add a zero to increase phase margin.

We can thus add a resistor in series with the original capacitor. The open-loop transfer function is derived as follows:

$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_p}{2\pi}\left(R_P + \frac{1}{sC_P}\right) \tag{2.9}$$

$$\frac{\phi_{out}}{\phi_{out}}(s)\Big|_{open} = \frac{I_p}{2\pi}\left(R_P + \frac{1}{sC_P}\right)\frac{K_{vco}}{s} \tag{2.10}$$

As shown in Fig. 2.8(b), the phase margin will increase because of the zero $1/(R_PC_P)$ and the system will not oscillate at the unit-gain frequency. However, a severe problem occurred in such PLLs. Due to the resistor in series with capacitor, each time a current is injected into the loop filter and then produces large voltage jump. It makes ripples of control voltage of VCO and degrades the purity of the output frequency spectrum.

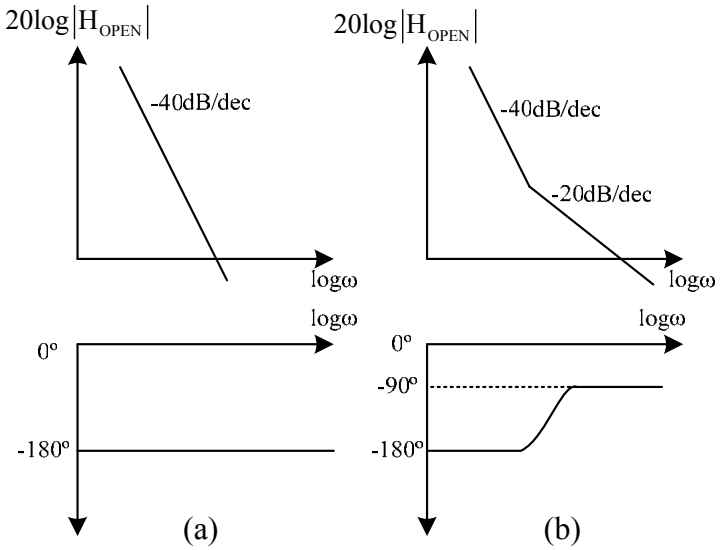


Fig. 2.8 (a) Loop gain of simple PLL (b) addition of zero

We can ease this effect by adding a second capacitor in parallel with R_P and C_P. The loop filter is now of 2nd order and the open loop transfer function of PLL now is of third-order and has stability problem, as shown in Fig. 2.9 (a). But if we make C_2 is about one-fifth to one-tenth of C_P, the open-loop transfer function is near the second-order and would be stable.

$$F(s) = K_h \frac{s + w_2}{s\left(\frac{s}{w_1} + 1\right)} \tag{2.11}$$

where $K_h = \frac{C_P R_p}{C_P + C_2}$, and $\omega_2 = \frac{1}{C_P R_p}$, $\omega_1 = \frac{C_2 + C_P}{C_2 C_P R_p}$

Moreover, current switching in the charge pump at the reference frequency f_{ref} would cause unwanted sidebands at the frequency spectrum of VCO. We can add additional LPF to suppress the spur that is f_{ref} offset from the carrier frequency, as shown in Fig. 2.9 (b). The loop filter transfer function is

$$F(s) = K_h \frac{s + w_2}{s\left(\frac{s}{w_1} + 1\right)\left(\frac{s}{w_3} + 1\right)} \tag{2.12}$$

where $K_h = \frac{C_2 R_2}{C_1 + C_2}$, and $\omega_2 = \frac{1}{C_2 R_2}$, $\omega_1 = \frac{C_1 + C_2}{C_1 C_2 R_2}$

$$\omega_3 = \frac{1}{C_3 R_3}$$

The additional pole must be lower than the reference frequency in order to significantly attenuate the spurs. However, it must be at least five times higher than the loop bandwidth, or the loop will almost assuredly become unstable.

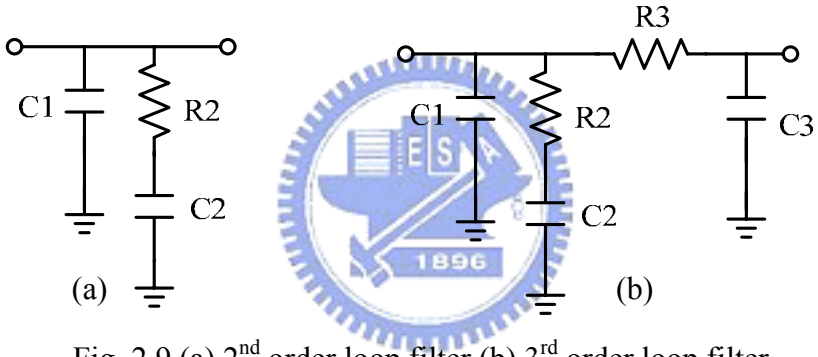


Fig. 2.9 (a) 2nd order loop filter (b) 3rd order loop filter

2.3.4 Divider

If we want to synthesize any high frequency, we need a divider in the feedback path. The only relation between the frequency of VCO ω_{out} and the frequency of the output signal of divider ω_{clkout} is

$$\omega_{clkout} = \frac{1}{N}\omega_{out} \tag{2.13}$$

We integrate both sides of the equation, and thus get the phase relationship:

$$\theta_{clkout} = \frac{1}{N}\theta_{out} \tag{2.14}$$

Generally speaking, the divider modulus is variable and able to synthesize a set of adjacent channels. We call such a divider as Multi-Modulus Divider (MMD).

2.4 Analysis of PLL Linear Model

Because we derive the linear transfer function of each block, we can analysis the open loop transfer function of PLL.

2.4.1 Analysis of open loop transfer function

Because we derive the linear transfer function of each block, we can analysis the open loop transfer function of PLL.

First we calculate the open loop transfer function G(s) with 2nd order loop filter:

$$G(s) = \frac{K_d F(s) K_{vco}}{sN} = -\frac{K_d}{C_1 + C_2} \frac{1 + s/\omega_2}{s(1 + s/\omega_1)} \frac{K_{vco}}{s} \frac{1}{N} \qquad (2.19)$$

For the sake of convenience, we make $\omega_2 = T_2^{-1}$ and $\omega_1 = \omega_2(1 + C_2/C_1) = T_1^{-1}$. The open loop gain is:

$$\left|G(s)\right|_{s=jw} = -\frac{K_d K_{vco}(1 + jw/\omega_2)}{\omega^2 C_1 N (1 + jw/\omega_1)} \frac{T_1}{T_2} \qquad (2.20)$$

And the phase margin is:

$$\phi(\omega) = \tan^{-1}\left(\frac{w}{w_2}\right) - \tan^{-1}\left(\frac{w}{w_1}\right) \qquad (2.21)$$

To insure stability, we want to have the maximum phase margin at the crossover frequency. We differentiate $\phi(\omega)$ being equal to zero to get the frequency

where the phase margin is maximum.

$$\frac{d\phi}{d\omega} = \frac{1}{1+(\omega/\omega_2)^2}\frac{1}{\omega_2} - \frac{1}{1+(\omega/\omega_1)^2}\frac{1}{\omega_1} = 0 \qquad (2.22)$$

$$\omega_p = \sqrt{\omega_1\omega_2} \qquad (2.23)$$

And therefore the maximum phase margin ϕ_c is:

$$\phi_p = \tan^{-1}\left(\frac{\omega_p}{\omega_2}\right) - \tan^{-1}\left(\frac{\omega_p}{\omega_1}\right) \qquad (2.24)$$

From equation 2.20, let $G(j\omega_c)=1$, we can get C_1:

$$C_1 = \frac{K_d K_{vco} T_1}{\omega_p{}^2 N T_2}\left\|\frac{(1+j\omega_p/\omega_2)}{(1+j\omega_p/\omega_1)}\right\| \qquad (2.25)$$

Thus if we decide the loop bandwidth ω_c, and the phase margin ϕ_c, we can derive w_1 and w_2 from the following equations:

$$\omega_1 = \frac{\omega_p}{\sec\phi_p - \tan\phi_p} \qquad (2.26)$$

$$\omega_2 = \frac{\omega_p{}^2}{\omega_1} \qquad (2.27)$$

Therefore, we can get the C_2 and R_2, respectively.

$$C_2 = C_1\left(\frac{\omega_1}{\omega_2} - 1\right) \qquad (2.29)$$

$$R_2 = \frac{1}{C_2\omega_2} \qquad (2.30)$$

If we use the 3rd order filter as the loop filter of PLL, due to the additional LPF, the added attenuation with regard to F_{ref} is

$$ATTEN = 10\log\left[\left(2\pi F_{ref} R_3 C_3\right)^2 + 1\right] \tag{2.31}$$

So if we decide the ATTEN of loop filter, we can get $\omega_3 = \frac{1}{C_3 R_3}$ by

$$T_3 = \frac{1}{\omega_3} = \sqrt{\frac{10^{(ATTEN/10)} - 1}{\left(2\pi F_{ref}\right)^2}} \tag{2.32}$$

As we mentioned above, the ω_3 must be lower than the reference frequency, in order to significantly attenuate the spurs. Because ω_3 will degraded the phase margin, we must recalculated the open loop unit gain ω_c and the relationship between ω_1 , ω_2 , ω_3 and ω_c . Similar to the equation (2.22), we use the same way to derive the relation between ω_1 , ω_2 , ω_3 and ω_c .

$$T_2 = 1\Big/\left[\omega_c^2\left(T1 + T3\right)\right] \tag{2.33}$$

From the ref [3], we can get the new open loop unit gain ω_c as

$$\begin{aligned}\omega_c &= \frac{\tan\phi\cdot\left(T_1 + T_3\right)}{\left[\left(T_1 + T_3\right)^2 + T_1 T_3\right]} \\ &\times\left[\sqrt{1 + \frac{\left(T_1 + T_3\right)^2 + T_1 T_3}{\left[\tan\phi\cdot\left(T_1 + T_3\right)\right]^2}} - 1\right]\end{aligned} \tag{2.34}$$

From equation (2.20), let $G\left(j\omega_c\right) = 1$, we can get C_1:

$$C_1 = \frac{T_1}{T_2}\frac{K_{pd}K_{vco}}{\omega_c^2 N}\left[\frac{\left(1 + \omega_c^2 T_2^2\right)}{\left(1 + \omega_c^2 T_1^2\right)\left(1 + \omega_c^2 T_3^2\right)}\right]^{1/2} \tag{2.35}$$

Similar to the 2nd order filter, we can get

$$C_2 = C_1\left(\frac{\omega_1}{\omega_2} - 1\right) \tag{2.36}$$

$$R_2 = \frac{1}{C_2\omega_2} \tag{2.37}$$

The only variable components are R_3 and C_3. The single condition is equation (2.32). A rule of thumb choose $C_3 \le C_1/10$, otherwise T_3 will interact with the primary poles of the filter. Similarly, choose R_3 at least twice the value of R_2. With the aid of simulation, we can get satisfactory results by using above analysis.

2.4.2 Analysis of closed loop transfer function

In the following, we will discuss the closed loop transfer function of using 2nd order loop filter. From the equation (2.19), let $K = \frac{K_c K_h K_{vco}}{N}$, which equals the loop bandwidth ω_c, and we obtain another expression of $G(s)$:

$$G(s) = \frac{K(s+\omega_2)}{s^2\left(1+\frac{s}{\omega_1}\right)} \tag{2.38}$$

Thus the closed loop transfer function $H(s)$ is:

$$H(s) = \frac{NG(s)}{1+G(s)} \tag{2.39}$$

$$= \frac{NK(s+\omega_2)}{s^2(1+s/\omega_1)+KS+K\omega_2} \tag{2.40}$$

Because $H(s)$ is of 3rd order system, we cannot use the control theorem to analyze it. However, in the lower frequency, we can treat the CP-PLL with 2nd order

loop filter as the 2nd open-loop system. Then the equation (2.40) can be written as

$$H(s) = \frac{NK(s + \omega_2)}{s^2 + KS + K\omega_2} \tag{2.41}$$

Compared $H(s)$ with the normalized form for a 2nd order control system:

$$H(S) = \frac{2\zeta\omega_n S + \omega_n^2}{S^2 + 2\zeta\omega_n S + \omega_n^2} \tag{2.42}$$

where ζ = Damping factor , ω_n = Natural frequency

We can get the following relationships:

$$\zeta = 0.5\sqrt{K/\omega_2}, \quad \omega_n = \sqrt{K\omega_2} \tag{2.43}$$

If ζ is larger, the step response will oscillate and rapidly damp to the final value. However, it would have large overshoot. On the contrary, if ζ is too small, the step response will converge slowly and need more time to stable. ω_n means the oscillatory frequency of the system in the transient response. Fig. (2.10) shows the step response under various ζ . We can observe that the damping ratio among the range of $0.8 \le \zeta \le 1$ is a good choice if we want proper settling time and acceptable overshoot. Besides, we calculate the phase margin under various K/ω_2 , which is proportional to ζ . We can find that if the K/ω_2 is larger, the phase margin is larger. By choosing $0.8 \le \zeta \le 1$, we thus get $46.4° \le PM \le 62°$.

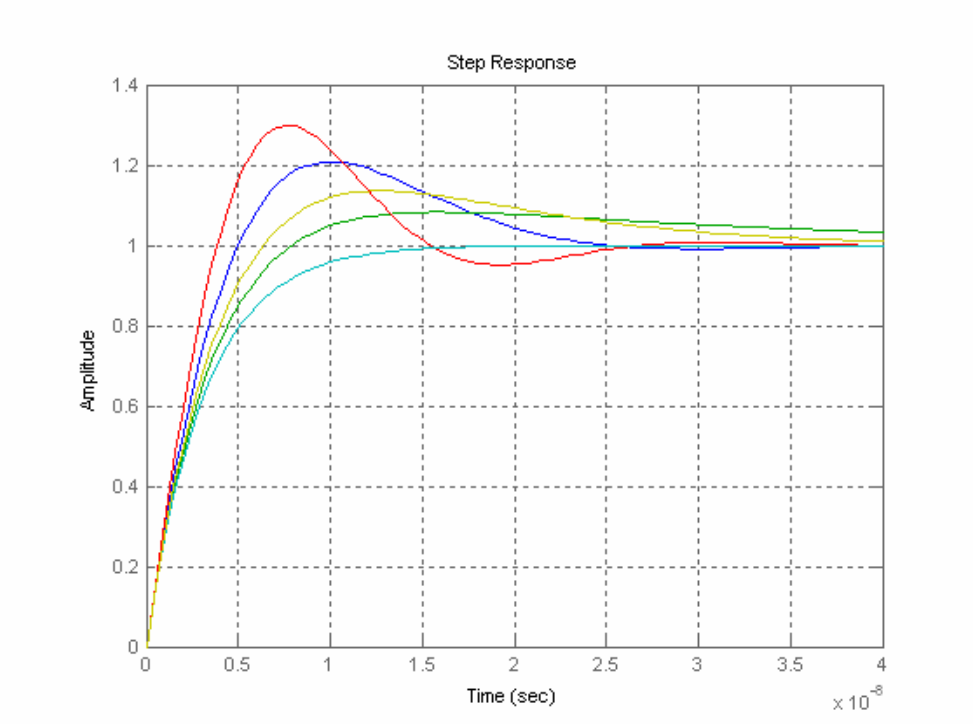


Fig. 2.10 step response under various ζ

TABLE I. phase margin under various K/ω_2

K/ω_2	2.5	3	3.5	4	4.5	5
PM	46.4°	53.1°	58.1°	61.9°	64.9°	67.4°

2.4.3 Steady State Phase Error

The steady state phase error can be derived in the following:

$$\theta_e = \theta_{ref} - \theta_{out} / N \tag{2.44}$$

$$\theta_e = \frac{\theta_{ref}}{1 + K_d F(s) K_o / sN} \tag{2.45}$$

$$\lim_{t \to \infty} \theta_e(t) = \lim_{s \to 0} s\theta_e(s) = \frac{s^2 \theta_{ref} N}{K_d F(s) K_o} \tag{2.46}$$

So if we apply the 2nd order filter to the above $F(s)$, and

let $K = \frac{K_c K_h K_{vco}}{N}$, we can get

$$\lim_{s \to 0} s\theta_e(s) = \frac{s^3\left(1 + s/\omega_1\right)\theta_{ref}}{K\left(s + \omega_2\right)} \tag{2.47}$$

Therefore, whether $\lim_{t \to \infty} \theta_e(t) = 0$ or not depends on the type of input signal θ_{ref}. There are three kinds of input signals we may apple to the PLL. They are phase step, frequency step or frequency ramp and Laplace representations are respectively $\frac{\phi}{s}$, $\frac{f_o}{s^2}$, and $\frac{a}{s^3}$, a is the derivative of the frequency ramp. We apply the three signals to the equation and derive the following conclusion shown in table II.

TABLE II. Steady state phase error under various input signals

Input signal	Steady state phase error
phase step $\theta_{ref} = \frac{\phi}{s}$	$\lim_{t \to \infty} \theta_e(t) = 0$
frequency step $\theta_{ref} = \frac{f_o}{s^2}$	$\lim_{t \to \infty} \theta_e(t) = 0$
Frequency ramp $\theta_{ref} = \frac{a}{s^3}$	$\lim_{t \to \infty} \theta_e(t) = \frac{aN}{K\omega_2}$

Therefore the phase error will be zero finally for phase step and frequency step and the loop will be locked. However, the phase error of frequency ramp is a fixed value $\frac{aN}{K\omega_2}$. If “a” is small, the loop will still be locked. What if “a” is large? We know if input signal is large, the model is no longer linear, but proportional to sine of the phase error. We can rewrite it as:

$$\lim_{t \to \infty} \sin\theta_e(t) = \frac{aN}{K\omega_2} \tag{2.48}$$

Because $\sin\theta_e(t)$ has its maximum value, which equals unity, and the

frequency ramp has the limitation as equation (2.49)

$$a \leq \frac{K \omega_2}{N} \tag{2.49}$$

So if the frequency ramp is larger than $\frac{K\omega_2}{N}$, the loop will be unlocked. Fortunately, in our application, such a situation won't be happened because it is not used in the frequency hopping.

2.5 Phase Noise

There are two parameters to make us know how purity of the output spectrum is: phase noise and spur. In the beginning, we will explain how these two effects are produced. Let us consider the following signal as the output of VCO:

$$x(t) = A\cos\left[\omega_c t + \phi_n(t)\right] \tag{2.50}$$

$\phi_n(t)$ is the random phase of output signal. It will cause jitter in the time domain. For convenience, we divide $\phi_n(t)$ into two parts, periodic and non-periodic signals. First, we suppose $\phi_n(t) = \phi_m \sin\omega_m t$

$$\begin{aligned} x(t) &= A\cos\left[\omega_c t + \phi_m \sin\omega_m t\right] \\ &= A\cos\omega_c t\cos\left(\phi_m \sin\omega_m t\right) \\ &\quad - A\sin\omega_c t\sin\left(\phi_m \sin\omega_m t\right) \end{aligned} \tag{2.51}$$

If $\phi_m \ll 1$, then equation (2.51) can be simplified as

$$\begin{aligned} x(t) &\approx A\cos\omega_c - \left(A\sin\omega_c t\right)\left(\phi_m \sin\omega_m t\right) \\ &= A\cos\omega_c - \frac{A\phi_m}{2} \\ &\quad \times\left[\cos\left(\omega_c + \omega_m\right)t - \cos\left(\omega_c - \omega_m\right)t\right] \end{aligned} \tag{2.52}$$

Therefore, the spectrum of the output signal has the strong component

at $\omega = \omega_c$, and two small sidebands at $\omega = \omega_c \pm \omega_m$. The sidebands are so-called spurs, as shown in Fig. 11(a). Spurs are the deterministic components and can be predicted. It is different from the harmonics of the output signal because it is more closed to the carrier and usually has harmful effect in the applications. Second, we suppose $\phi_n(t)$ is a stationary Gaussian random noise with a low-pass power spectral density:

$$P_\phi(\omega) = \frac{1}{1 + (\omega/\omega_0)^2} \tag{2.53}$$

In a similar manner, if $|\phi_n(t)| \ll 1$, we can get

$$\begin{aligned} x(t) &= A\cos[\omega_c t + \phi_n] \\ &= A\cos\omega_c t\cos\phi_n - A\sin\omega_c t\sin\phi_n \\ &= A\cos\omega_c t - A\phi_n\sin\omega_c t \end{aligned} \tag{2.54}$$

The resulting spectrum shows noise skirts around the center frequency. In contrast to spurs, phase noise results from the random phases, as shown in Fig. 2.11(b). To quantify phase noise, we consider a unit bandwidth at a frequency offset $\Delta\omega$ with respect to ω_c, calculate the total noise power in this bandwidth, and divide the result by the power of the carrier, as shown in Fig. 2.12. The unit of phase noise is dBc/Hz, the letter "c" denotes the normalization of the noise power to the carrier power, and the unit Hz signifying the unit bandwidth used for the noise power.

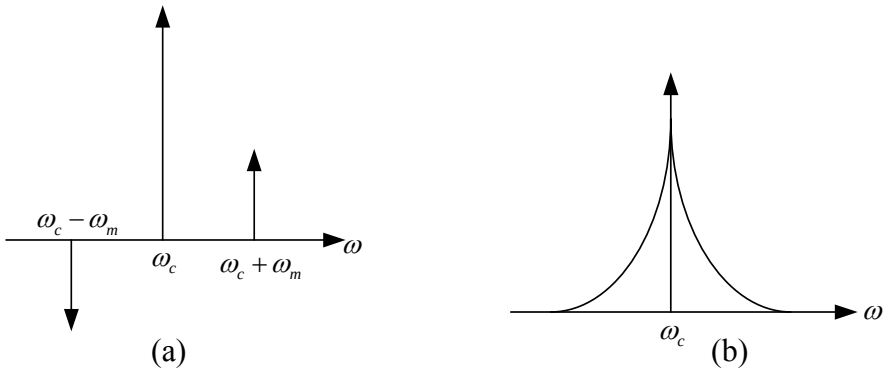


Fig. 2.11 (a) Sidebands and (b) noise skirts resulting from phase modulation

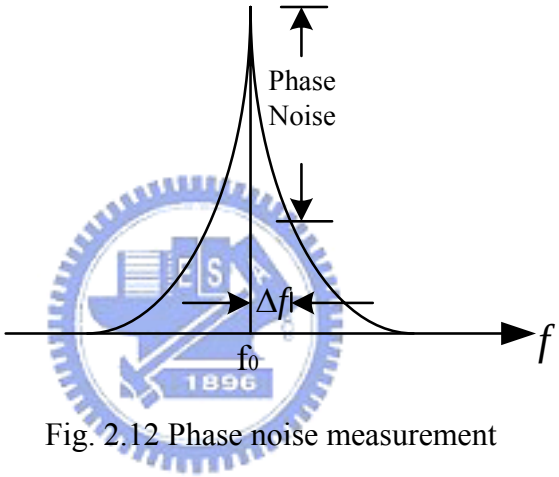


Fig. 2.12 Phase noise measurement

2.5.1 Leeson's Model

In the beginning, we consider the phase noise of the oscillator. Because oscillators usually have the function of BPF, just like LC-tank VCO or crystal oscillator, we must know how the BPF influence the input white noise to the oscillator's output. Fig. is a simple Leeson's model [4][5]. We suppose the gain of amplifier is unity, and the BPF is in the feedback path.

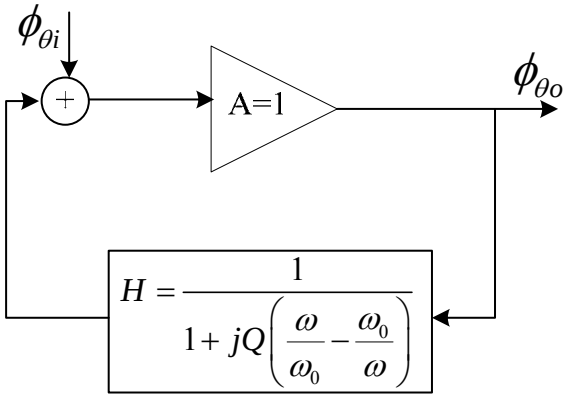


Fig. 2.13 Leeson's Model

The function of BPF is given as

$$H(j\omega) = \frac{1}{1 + jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)} \tag{2.55}$$

Let us consider the frequency which is closed to the center frequency of BPF ω_0. If $\omega \to \omega_0$

$$H(j\omega) = \frac{1}{1 + jQ\left(\frac{\omega^2 - \omega_0^2}{\omega\,\omega_0}\right)} \approx \frac{1}{1 + \frac{2Q}{\omega_0}} \tag{2.56}$$

Since we are only interested in the frequencies closed to the carrier, we would like to transform the frequencies to the offset frequencies from the carrier frequency. Therefore, let $\Delta\omega = \omega - \omega_0 \equiv \omega_m$=Offset frequency , we get

$$H_L(j\omega_m) \approx \frac{1}{1 + j\frac{\omega_m}{\omega_L}}, \omega_L \triangleq \frac{\omega_0}{2Q} = 3dB \text{ BW} \tag{2.57}$$

Thus, we have successfully transformed the viewpoint from the BPF to the LPF, where the BW is half the one of the BPF. Finally, the output phase noise can be expressed as

$$\phi_{\theta 0} = \phi_{\theta i} \bullet \left| \frac{1}{1 - H_L} \right| = \phi_{\theta i} \bullet \left(1 + \frac{\omega_L^2}{\omega_m^2} \right) \tag{2.58}$$

If $\omega_m \ll \omega_L$

$$\phi_{\theta 0} = \phi_{\theta i} \bullet \left(1 + \frac{\omega_L^2}{\omega_m^2} \right) \approx \frac{\omega_L^2}{\omega_m^2} \phi_{\theta i} \tag{2.59}$$

If $\omega_m \gg \omega_L$

$$\phi_{\theta 0} = \phi_{\theta i} \bullet \left(1 + \frac{\omega_L^2}{\omega_m^2} \right) \approx \phi_{\theta i} \tag{2.60}$$

The resulting spectrum is shown in Fig. 2.14(a). Besides, another noise source called flicker noise appears in the oscillator's output. By measurement, if frequencies below some frequency ω_c, flicker noise would dominate and be proportional to $1/\omega_m$. Otherwise, thermal noise would dominate, as shown in Fig. 2.14(b).

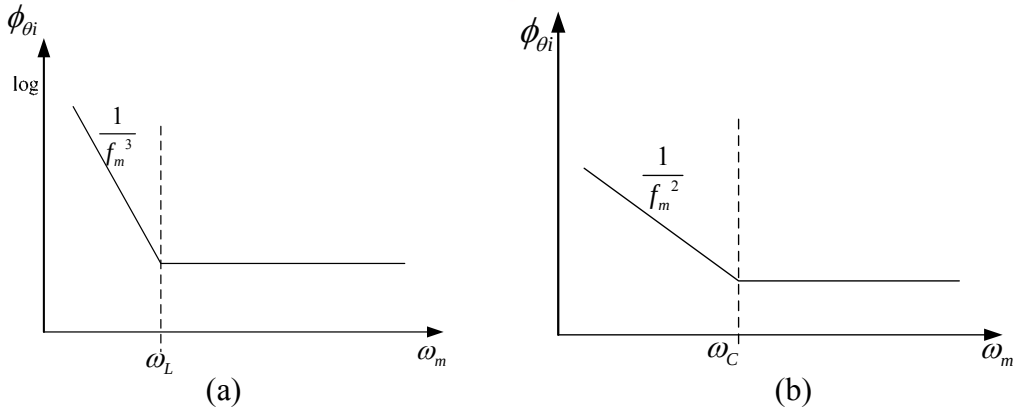


Fig. 2.14 (a) Output phase noise due to BPF (b) flicker noise in the output signal

In the case of LC-tank VCO, ω_c is usually smaller than ω_L. So the phase noise of VCO is shown in Fig. 2.14(a). On the other hand, in the case of crystal oscillator, ω_c is usually larger than ω_L and phase noise is shown in Fig. 2.14(b).

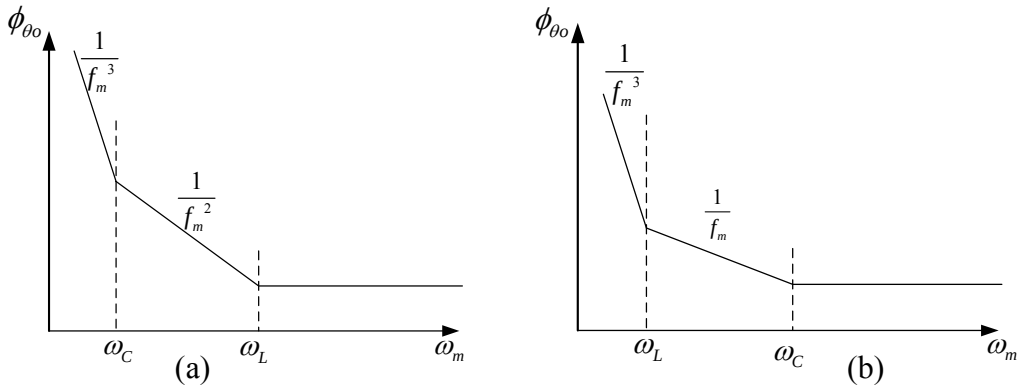


Fig. 2.14 (c) Phase noise of VCO (low Q) (d) phase noise of crystal oscillator (high Q)

We now discuss the phase noise of the output signal of the PLL. As shown in Fig. 2.15, the noise ϕ_{NO} of VCO is added after the VCO block. The noise transfer function can be derived as follows:

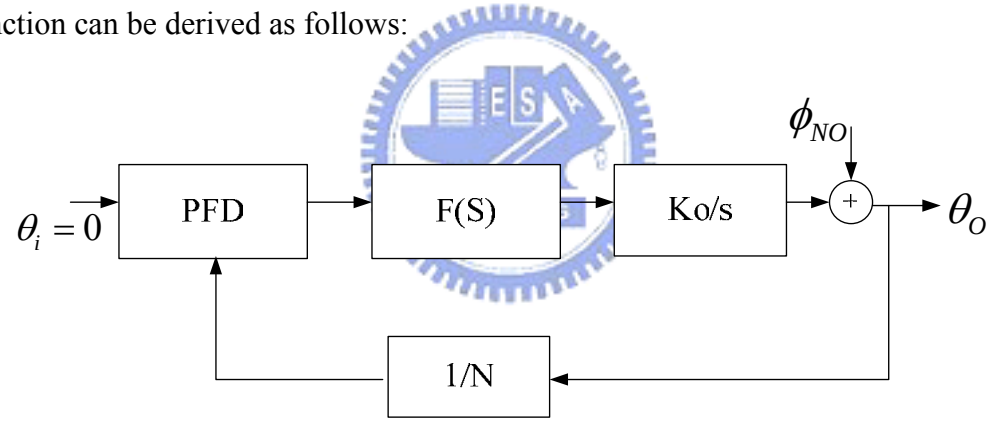


Fig. 2.15 PLL noise model from VCO

$$\left(0 - \frac{\theta_0}{N} \right) K_d \cdot F(s) \cdot \frac{K_o}{s} + \phi_{NO} = \theta_0 \tag{2.61}$$

$$\Rightarrow \frac{\theta_0}{\phi_{NO}} = \frac{1}{1 + \frac{K_d K_o F(s)}{N s}} \tag{2.62}$$

As we discuss earlier, the transfer function of PLL is given in equation (2.39), and we modify it as

$$\frac{\theta_0}{\theta_i} = H(s) = \frac{N K_d K_o \frac{F(s)}{sN}}{1 + K_d K_o \frac{F(s)}{Ns}} \tag{2.63}$$

$$\frac{H}{N} = \frac{K_d K_o \frac{F(s)}{sN}}{1 + K_d K_o \frac{F(s)}{Ns}} \tag{2.64}$$

Thus we can derive the relation between noise transfer function and system function

$$H_e = \frac{\theta_o}{\phi_{NO}} = 1 - \frac{H}{N} \tag{2.65}$$

Because $H(s)$ is a LPF, the noise transfer function H_e is a HPF. If the bandwidth (BW) of $H(s)$ is K, the H_e will be unity at high frequency, and below K, it will decay from K at the rate of 20dB/decade.

Now we can apply the above equations to calculate the output phase noise due to reference signal (REF) and VCO. Fig. 2.16 shows the phase noise model of REF, $|H(s)|^2$ and the output phase noise due to REF.

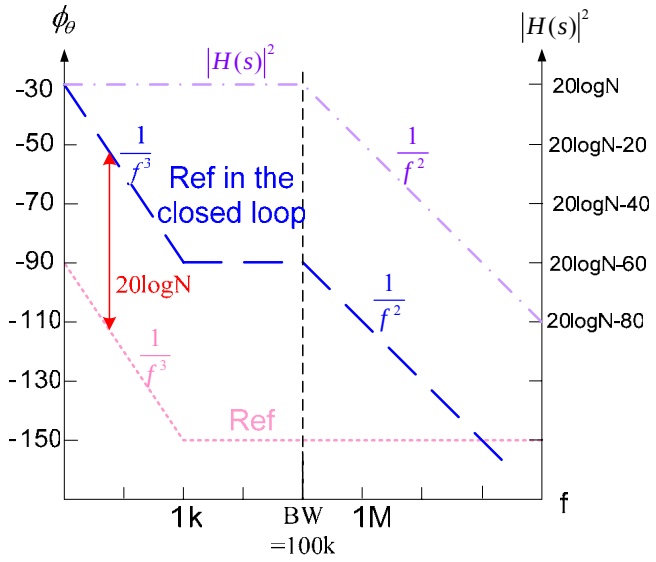


Fig. 2.16 Output phase noise from REF

In the closed loop, the phase noise of REF will increase N^2 times and decay at the rate of 20dB/decade from frequencies above BW. Here we make $N = 1000$ and $BW = 100k$. It is important to note that the smaller BW is and the more decay we make.

In the same way, Fig. 2.17 shows the phase noise model of VCO, $|H_e|^2$ and the output phase noise due to VCO. When $f \geq BW$, $|H_e|^2 = 0dB$. So the phase noise of VCO is unchanged. When $f \leq BW$, $|H_e|^2$ will decay at the rate of 20dB/decade from frequencies below BW. Thus, the phase noise will become constant at $1k \leq f \leq BW$ and rise at the rate of 10dB/decade at $f \leq 1k$. In addition, due to the property of HPF, the larger BW is and the more decay it does.

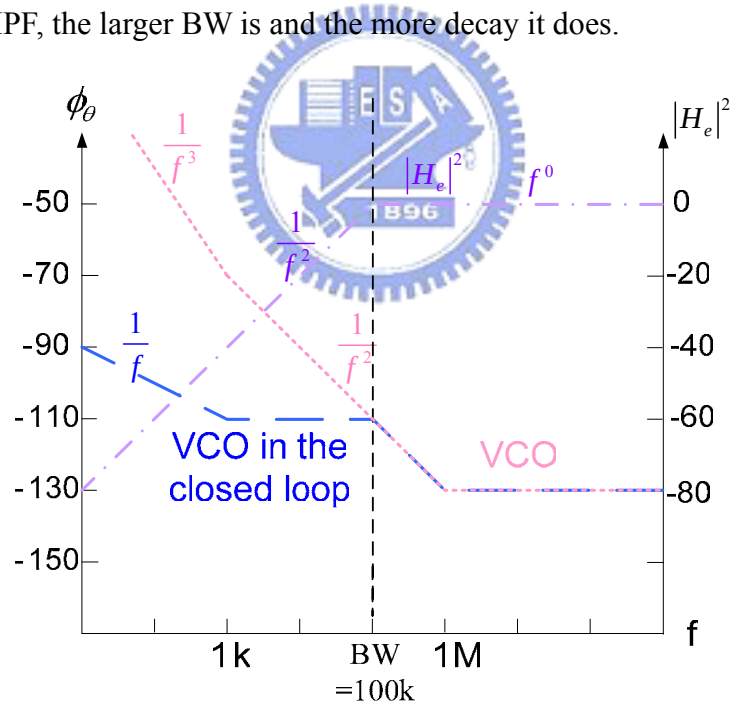


Fig. 2.17 Output phase noise from VCO

The total phase noise can be derived by adding the above two eventual phase noises, as shown in Fig. 2.18. It is obviously that when the frequencies nears carrier, the REF in the closed loop dominate the total phase noise. Otherwise, the VCO dominates. If we want to suppress the phase noise of REF, we can decrease the BW.

However, it will raise the phase noise of VCO. On the contrary, increasing the BW will suppress the phase noise of VCO but raise the phase noise of REF. It is a trade off. How we decide the best BW is important.

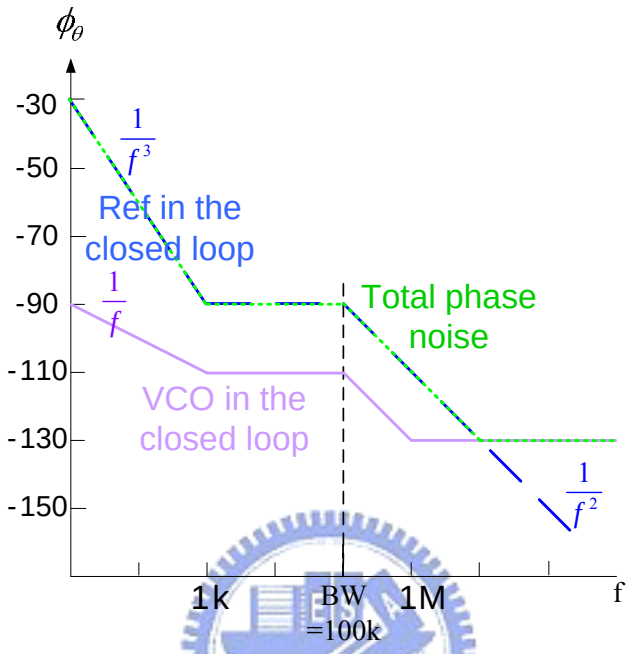


Fig. 2.18 Total output phase noise

Fig. 2.19 shows the resolution to decide the BW. First, raise the phase noise of REF by $20\log N$. Second, find the intersection of above line and the phase noise of VCO. The frequency of the intersection is the optimal BW. Fig. 2.20 shows the comparison between the optimal BW (10k) and another BW (100k). Finding the optimal bandwidth results in the least phase noise appeared in the output.

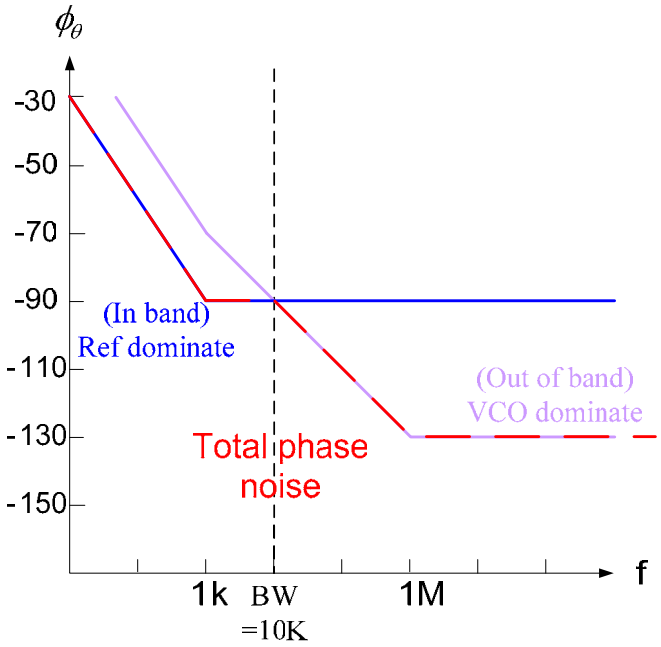


Fig. 2.19 Illustration of finding the best BW

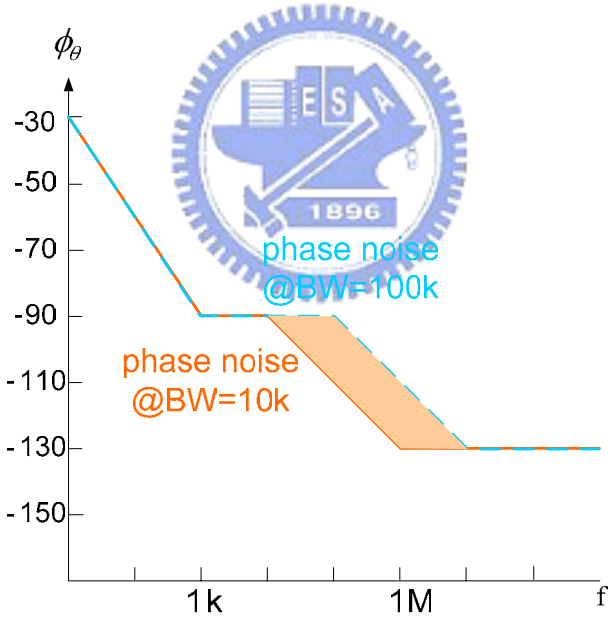


Fig. 2.20 Phase noise comparison between optima BW and another BW

Chapter 3

Principles of Fractional-N PLL

3.1 Concept of Fractional-N PLL

The conventional frequency synthesizer consists of integer-N PLL and fractional-N PLL. The advantage of PLL over integer-N PLL is to provide finer frequency resolution while owning wide loop bandwidth. Thus the fractional-N PLL has smaller lock-time and fast switch-speed. The only drawback of it is the fractional spur. Because of the regular sequence of divider modulus, it would cause spurs in the spectrum. The modern solution is to use the ΣΔ modulator to solve it. It can cause randomization and noise shaping. In the following, we will introduce the fractional-N mechanism and the principle of ΣΔ modulator.

3.2 The Fractional-N mechanism

Before introducing the architecture of fraction-N divider, let us observe the pulse removal phenomenon, as shown in Fig. 3.1. If a pulse is removed every T_P seconds from a periodic sequence that has the frequency F_P, the resulting sequence then has the $F_P T_P - 1$ pulses in the T_P. That is, the subsequent sequence has the average frequency of $F_P - 1/T_P$. This method can be used to vary the average frequency of the signal by small steps.

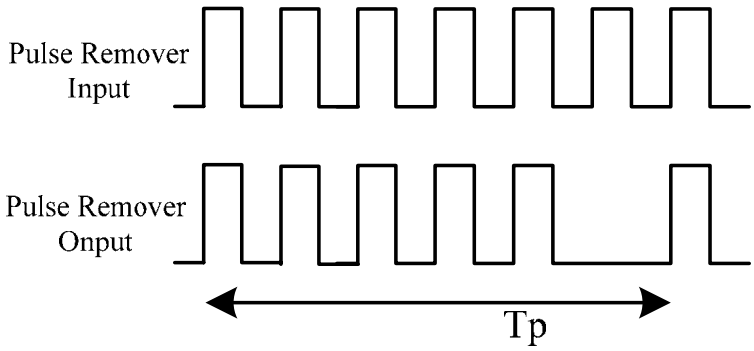


Fig. 3.1 Periodic removal of pulse from a periodic waveform

Fig. 3.2 shows the basic architecture of fraction-N PLL. We incorporate the pulse remover into the feedback path. In the locked state, f_{REF} is equal to pulse remover output. So f_{OUT} would finally equal $F_P + 1/T_P$. We can further replace the pulse remover with dual-mode divider as shown in Fig. 3.2. If the divider divides by N+1 for A output pulses (of the VCO) and by N for the remaining M-A output pulses, then the output frequency can be derived as follows:

$$\left[(N+1) \cdot A + (M-A) \cdot N \right] \cdot 1/f_{vco} = M \cdot 1/f_{ref} \tag{3.1}$$

$$\begin{aligned} \therefore \quad f_{vco} &= f_{ref} \cdot \frac{(N+1) \cdot A + (M-A) \cdot N}{M} \\ &= f_{ref} \cdot \left(N + A/M \right) \quad , M > A \end{aligned} \tag{3.2}$$

Thus the equivalent division ratio is $N + A/M$. This value can vary between N and N+1 in fine steps by proper choice of A and M. It is worthy to note that the counter M must be larger than the counter A, otherwise, the analytic function would no more exist.

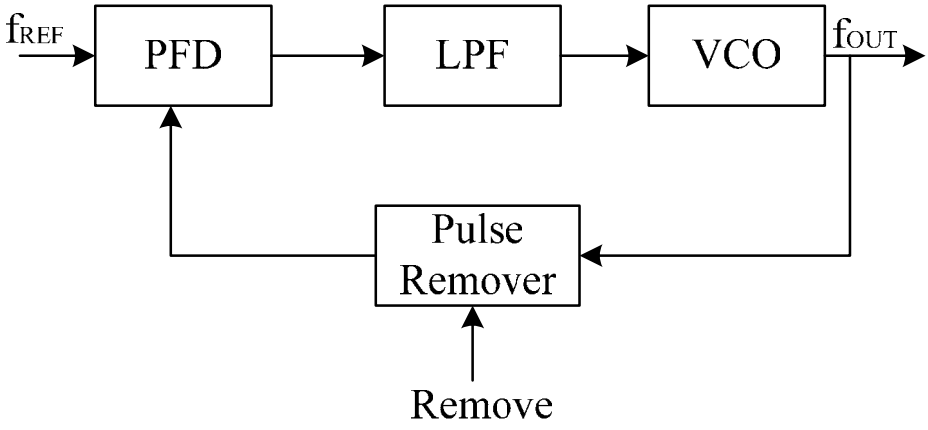


Fig. 3.2 Simple fraction-N PLL

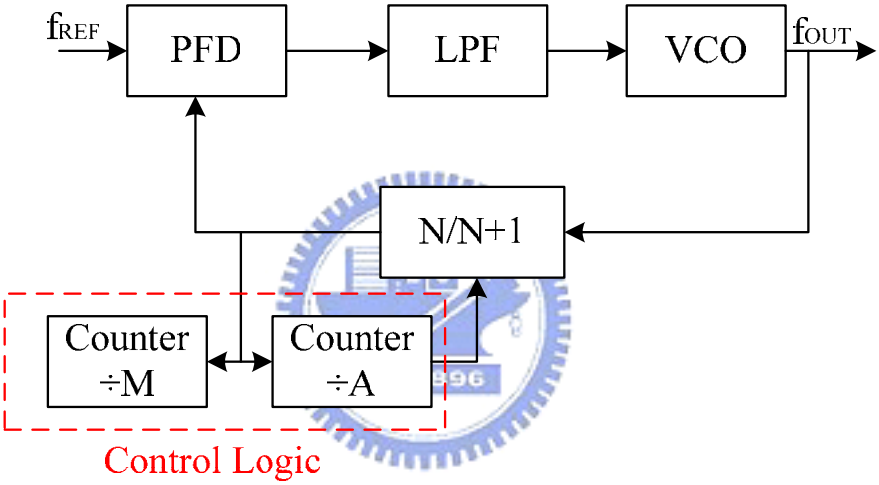


Fig. 3.3 Fraction-N PLL using a dual-modulus divider

There is a severe problem we will meet when we use the fractional-N PLL. When we use counters to control the modulus of the divider, there is a periodic accumulation error, as given by Fig. 3.3. In the first A output pulses of the VCO, the divider divides by N+1 cycles and the phase error accumulates. Then the phase error is gradually compensated after divider is changed to N. Since the phase error grows to significant values, the amplitude of the LPF output waveform is quite large, yielding fractional spurs f_{ref}/M offset from the carrier frequency. Because fractional spurs will decrease the quality of communication, we should reduce it as much as possible. The most popular method is using ΣΔ modulator. We will explain

it in detail in the next section.

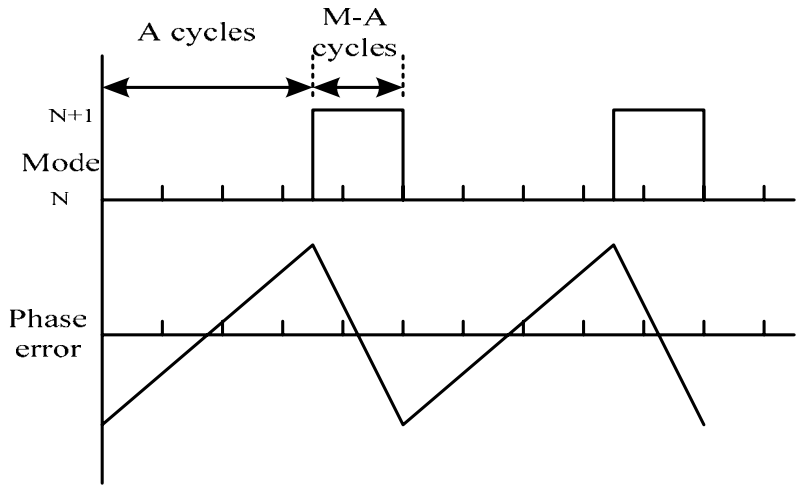


Fig. 3.4 periodic accumulation error phenomenon

3.3 Principles of ΣΔ modulator

Because the fractional spurs originate from the regular sequence of the divider modulus, we can eliminate spurs by randomize it. By randomization the choice of the modulus such that the average division factor is still given by $N+\alpha$, which means individual division factors occur for only short periods of time, the systematic fractional sideband would be converted to random noise. Besides, we can shape the resulting noise spectrum such that most of its energy appears at large frequency offsets. Therefore, the noise in the vicinity of the divided carrier is sufficiently small and the noise at high offsets is suppressed by the LPF of the PLL, as shown in Fig. 3.4. With the ΣΔ modulator [6][7][8], the divider modulus is near pseudo-random sequence and the quantization noise is differentiated in the signal band. The quantization noise comes from the reason that the divider only can divide by N or N+1, not N.α, where the dot denotes a decimal point and N and α represent the integer and fractional parts. Therefore, we can consider that the ideal divider

modulus N.α is quantized to N or N+1. Fig. 3.5 shows that the average of $b(t)$, α, is always quantized to 0 or 1.

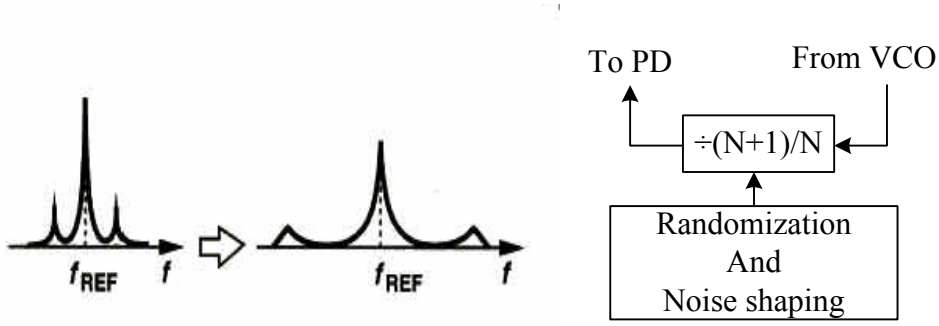


Fig. 3.5 Randomization and Noise shaping to eliminate unwanted spurs

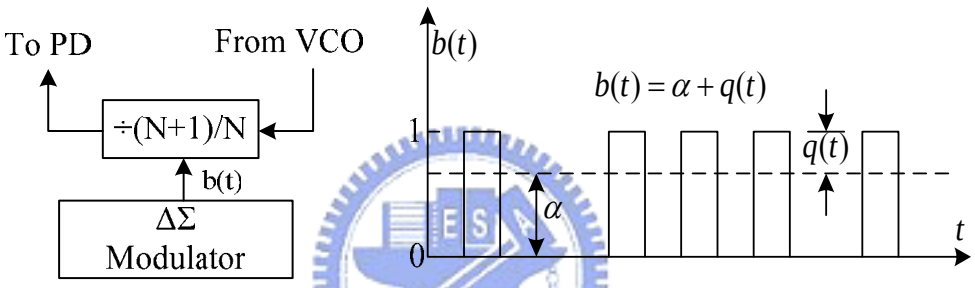


Fig. 3.6 the source of quantization noise

The idea of ΣΔ modulator is to use an integrator and a differentiator, as shown in Fig. 3.6. The input signal passes the both blocks and don't decay at all. However, the quantization just passes the differentiator and its power is lowered at signal band.

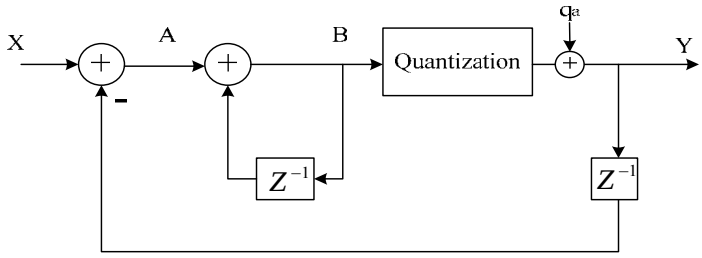


Fig. 3.7 ΣΔ modulator block diagram

We can get the transfer function as follows:

$$Y = X + \left(1 + Z^{-1}\right) q_a \qquad (3.3)$$

The implementation of ΣΔ modulator can be achieved by the accumulator. Fig.

3.7(a) shows the architecture of the accumulator and Fig. 3.7(b) shows its block diagram. In the same way, we can derive its transfer function in equation (3.4), which is the same as equation (3.3).

$$\begin{aligned} N[Z] &= .f[Z] + \left(1 + Z^{-1}\right) q_a[Z] \\ &= .f[Z] + qe[Z] \end{aligned} \tag{3.4}$$

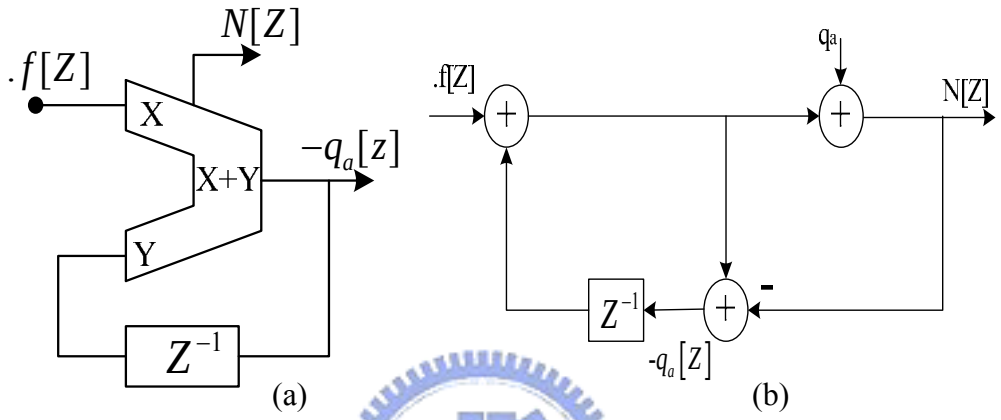


Fig. 3.8 (a) Implementation and (b) block diagram of ΣΔ modulator

As shown in Fig. 3.8, we can incorporate the ΣΔ modulator in the PLL to control the divider modulus.

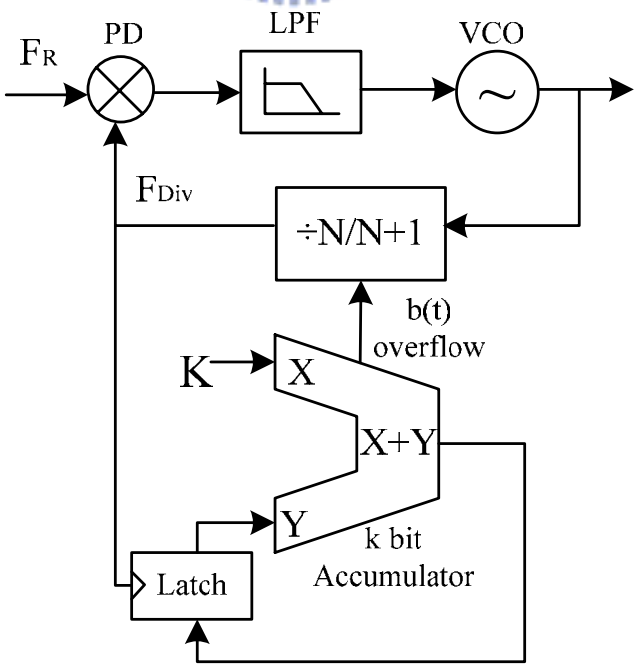


Fig. 3.9 Realization of ΣΔ modulator

It can be seen that, for a k-bit accumulator, the accumulator will produce an overflow on average $K/2^k$ every cycle of the F_{Div} clock. Thus the average division ratio is

$$N_{avg} = \frac{K \cdot (N+1) + (2^k - K) \cdot N}{2^k} = N + \frac{K}{2^k} \tag{3.5}$$

To get more insight into ΣΔ modulator, we should analyze it in analytic function. The optimal output signal of divider is in equation:

$$f_{div} = f_{ref} = \frac{f_{out}}{N + K/2^k} = \frac{f_{out}}{N'} \tag{3.6}$$

And the instantaneous frequency of divider is

$$\begin{aligned} f_{inst} &= \frac{f_{out}}{N + b(t)} = \frac{f_{out}}{N + K/2^k + qe(t)} \\ &= \frac{f_{out}}{N' + qe(t)} \end{aligned} \tag{3.7}$$

The quantization phase noise is

$$\theta_e(t) = 2\pi \cdot \int (f_{div} - f_{inst})dt = 2\pi \cdot \frac{f_{ref}}{N'} \cdot \int qe(t)dt \tag{3.8}$$

So the power spectral density of $\theta_e(t)$ is

$$S_{\theta_e}(f) = \frac{1}{(2\pi f)^2} \cdot S_{\theta_e'}(f) = \left(\frac{f_{ref}}{f \cdot N'}\right)^2 S_{qe}(f) \tag{3.9}$$

Now we recall that

$$qe[Z] = (1 + Z^{-1}) q_a[Z], \quad q_a[Z] = \frac{1}{12 f_{ref}} \text{ [9]} \tag{3.10}$$

The noise transfer function in the discrete time domain can be converted into the continuous time domain by the following method.

$$\left|H\ (f)\right| = \sqrt{\left|\left(1 - Z^{-1}\right)\right|^2}\Bigg|_{z=e^{\frac{-j2\pi f}{f_{ref}}}} = 2\sin\left(\frac{\pi f}{f_{ref}}\right) \tag{3.11}$$

From equation (3.9), we can get the final power spectral density of quantization noise is

$$S_{\theta_e}(f) = \frac{f_{ref}}{3(f \cdot N')^2} \cdot \sin^2\left(\frac{\pi f}{f_{ref}}\right) \propto f^0 \tag{3.12}$$

From the power spectral density of the 1st order ΣΔ modulator, we know that the noise in the output of VCO is flat, not the differential as we thought. That is because when we change the function from the frequency error to the phase error, we add a pole $s = 0$ on the total transfer function, degrading the advantage of high pass filtering in accumulator. In order to obtain effectively the noise shaping toward the high frequency end, the higher order ΣΔ modulator is required.

Fig. 3.9(a) shows the common 3rd order ΣΔ modulator: Multi-Stage Noise Shaping 1-1-1 (MASH 1-1-1) [10][11]. The block diagram is shown in Fig. 3.9(b). Thus we can thus get its transfer function

$$N1[z] = K[z] + \left(1 - z^{-1}\right) qa1 \tag{3.13}$$

$$N2[z] = -qa1 + \left(1 - z^{-1}\right) qa2 \tag{3.14}$$

$$N3[z] = -qa2 + \left(1 - z^{-1}\right) qa3 \tag{3.15}$$

$$\begin{aligned} N[z] &= N1[z] + \left(1 - z^{-1}\right) N2[z] + \left(1 - z^{-1}\right)^2 N3[z] \\ &= K[z] + \left(1 - z^{-1}\right)^3 qa3[z] \end{aligned} \tag{3.16}$$

Similarly, we can also change the noise transfer function to $H(f) = \left(1 - Z^{-1}\right)^3$ and get the final power spectral density of output noise.

$$S_{\theta_e}(f) = \frac{16 f_{ref}}{3(f \cdot N')^2} \cdot \sin^6\left(\frac{\pi f}{f_{ref}}\right) \propto f^4 \qquad (3.17)$$

The output PSD is now proportional to f^4, revealing that the quantization noise is suppressed in the signal band. As in general formula, if we use the i[th] order ΣΔ modulator, the PSD of the phase noise is [12]

$$S_{\theta_e}(f) = \frac{f_{ref}}{12(f \cdot N')^2} \cdot \left[2 \sin\left(\frac{\pi f}{f_{ref}}\right)\right]^{2i} rad^2/Hz \qquad (3.18)$$

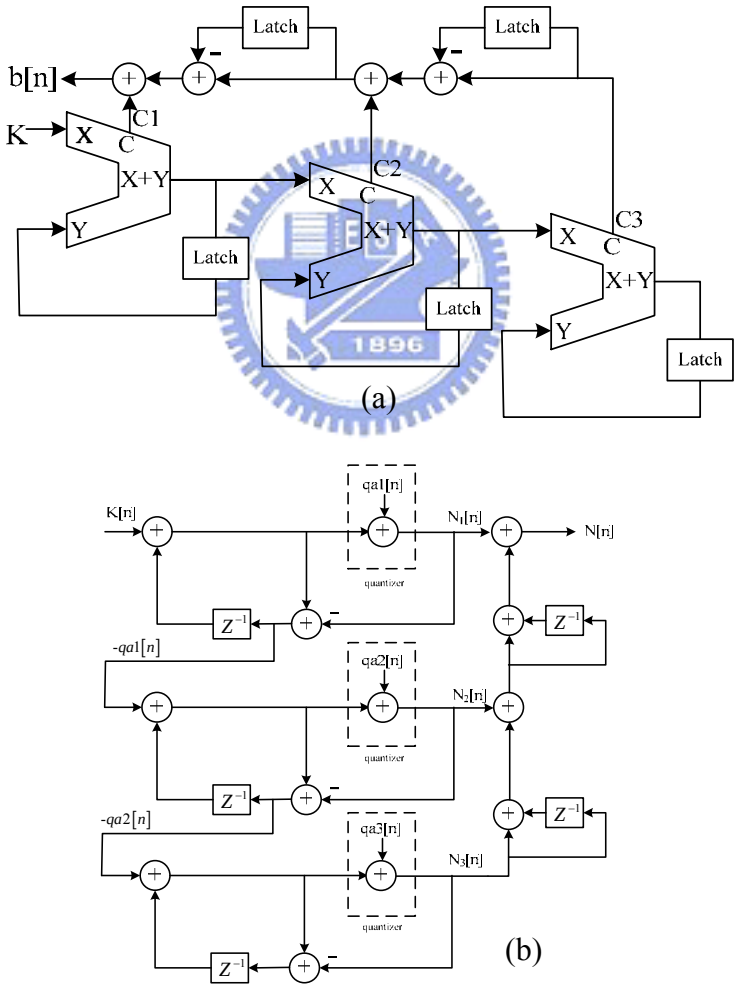


Fig. 3.10 (a) Implementation and (b) block diagram of 3[rd] order ΣΔ modulator

Chapter 4

Basic of Spread Spectrum Clock Generator

4.1 Background: EMI problem

Electro-Magnetic Interference (EMI) emission is always of great concern for power electronic circuit designers. Due to rapid switching of high current and high voltage, interference emission is a serious problem in switching power circuits because it pollutes carefully managed radio spectrum. In the USA, the Federal Communications Commission (FCC) has stringent rules about the maximum amount of EMI that a system may emit. These regulations address peak emissions (rather than average emissions) at a particular frequency. Many products fail to make it to the market because of their failure to comply with the government EMI regulations. Numerous companies have cited EMI problems as the major cause in the delay of their product introduction.

EMI noise reduction is generally accomplished by several means: metal shielding, pulse shaping, slew-rate control, layout technique, multi-layer printed circuit boards, special casing, and the spread spectrum clocking.

“Metal shielding” is to add more power and ground lines layers to lower EMI effects. It only encloses EMI rather than eliminating it. Thus, it is bulky and unpractical for portable systems due to the heavy weight.

"Pulse shaping" is to smooth the transition edges and remove the high frequency parts of the signal. This method only works when one can control portion of the waveform near the switching threshold. The drawback of this method is too much rounding may make digital signals look like analog signals, degrading the signal quality.

"Slew rate control" is similar to pulse shaping. A current-controlled output is to control the rising-edge or falling edge slope. As the speed of the system rises, timing budgets become more limited. Altering the edge rate too excessively is not recommended.

In these methods, they can be classified into two types: one is enclosing the EMI and the other is to reduce EMI at the source. Spread spectrum belongs to the second and thus provides a more efficient solution. Besides, it offers the best immunity with respect to manufacturing process variations.

4.2 Concept of Spread Spectrum

Spread spectrum clocking techniques is a special case of frequency modulation (FM) [13]. The basic concept is to slightly modulate the frequency of the clock signal and the energy of the signal will be spread over a wider range. Thus, the energy peak of every harmonic component is reduced. Furthermore, the higher order harmonic terms suffer from larger spread amounts and the attenuations are more obvious. This effect makes it easier for the resultant emission spectrum to pass EMI regulations. Consequently, spread spectrum clocking offer low EMI signal.

To get an insight of how frequency modulation related to spread spectrum, we now discuss the frequency modulation in analytic equations. Consider a sinusoidal modulating signal defined by:

$$m(t) = A_m \cos(2\pi f_m t) \tag{4.1}$$

The instantaneous frequency of the FM signal is

$$\begin{aligned} f_{FM}(t) &= f_c + k_f A_m \cos(2\pi f_m t) \\ &= f_c + \Delta f \cos(2\pi f_m t) \end{aligned} \tag{4.2}$$

$$where \quad \Delta f = k_f A_m \tag{4.3}$$

The Δf is called the frequency deviation, representing the maximum deviation of FM signal from the carrier frequency f_c. The angle of FM signal is obtained as:

$$\begin{aligned} \theta_{FM}(t) &= 2\pi f_c t + \frac{\Delta f}{f_m} \sin(2\pi f_m t) \\ &= 2\pi f_c t + \beta \sin(2\pi f_m t) \end{aligned} \tag{4.4}$$

$$where \quad \beta = \Delta f / f_m \tag{4.5}$$

The β is called the modulation index, representing the maximum phase deviation of FM signal. Depending on the value of the modulation index β, FM can be divided into two cases. When β is small compared to one radian, we call it narrow-band FM. On the contrary, when β is large compared to one radian, we call it wide-band FM. Generally speaking, the spread spectrum clocking belongs to the wide-band FM. The spectrum of FM signal is spread and can be represented by the Bessel function, i.e.

$$\begin{aligned} s(t) &= A_c \cos(2\pi f_c + \beta \sin 2\pi f_m t) \\ &= A_c \sum_{n=-\infty}^{\infty} J_n(\beta) \cos\left[2\pi (f_c + n f_m) t\right] \end{aligned} \tag{4.6}$$

Fig. 4.1 shows the Bessel function under various modulation indexes β and Fig. 4.2 shows the effect of frequency modulation on the frequency spectrum [14]. According to the Carson's rule, there are two important characteristics of an FM signal.

I. The total power of the signal is unaffected by the frequency modulation, i.e., $\sum_{n=-\infty}^{\infty} J_n^{\,2}(\beta) = 1$. Thus, referring to Fig. 4.2(b), the $A^2 = A_1^{\,2} + 2\left(A_2^{\,2} + A_3^{\,2} + \cdots\right)$.

II. Second, the 98% of the total power of a FM signal is within the bandwidth B_T, where $B_T = 2(\beta + 1) f_m$. Practically speaking, that represents the sideband harmonic frequency ranges from $(f_c - B_T/2)$ to $(f_c + B_T/2)$. If $\beta \gg 1$, then $B_T = 2\beta f_m = 2\Delta f$.

Therefore, from Fig. 4.1 , it looks as if the bar in $\beta = 0$ is broken and scatted around the sideband frequencies shown in $\beta = 1, 2, 3, ...$, according to the value of β. Besides, the frequency difference between every two adjacent side-band harmonics is f_m.

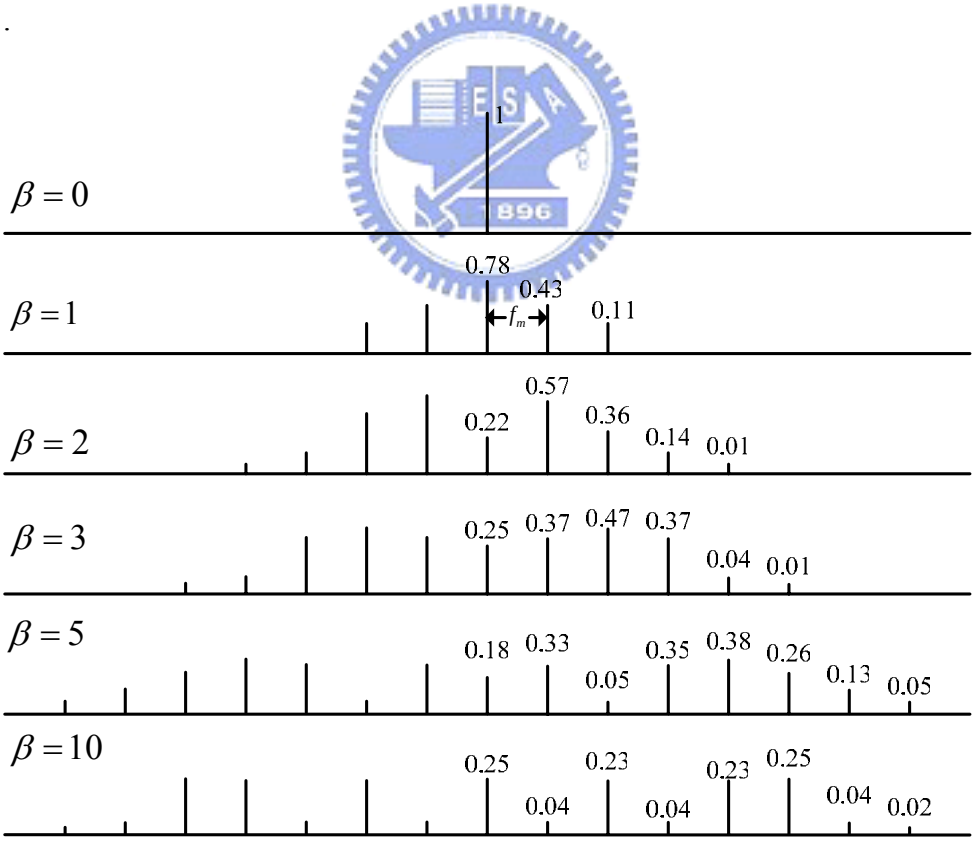


Fig. 4.1 Spectra of frequency-modulated sinewave under various modulation indexes

(a)

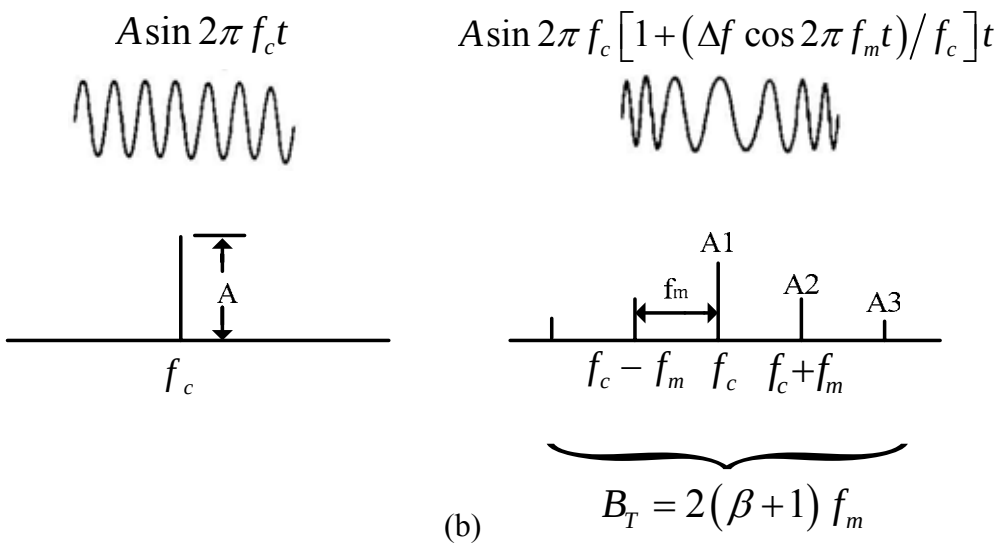


Fig. 4.2 Spectra of (a) sinusoidal waveform and (b) frequency-modulated sinusoidal waveform

If the un-modulated signal is a pulse train, it is composed of infinite sinusoidal components. Frequency modulation of the pulse train distributes each of harmonic into many side-band frequencies as shown in Fig. 4.3. The frequency difference between each two adjacent side-band frequencies is still f_m. However, the modulation index of each harmonic is different. If the maximum frequency of the pulse train is $f_c+\Delta f$, then the maximum frequency of nth harmonics is $n\left(f_c+\Delta f\right)$. Thus, from $\beta=\Delta f/f_m$, $\beta_n=n\Delta f/f_m$, we derive $\beta_n=n\beta$. Because the modulation index changes with each harmonic, the scattering effect of each harmonic is different, i.e. $B_{nT}=2\left(n\beta+1\right)f_m$. If $\beta\gg 1$, then $B_{nT}=nB_T$. Thus the higher the harmonic number, the more even is the spread-out power.

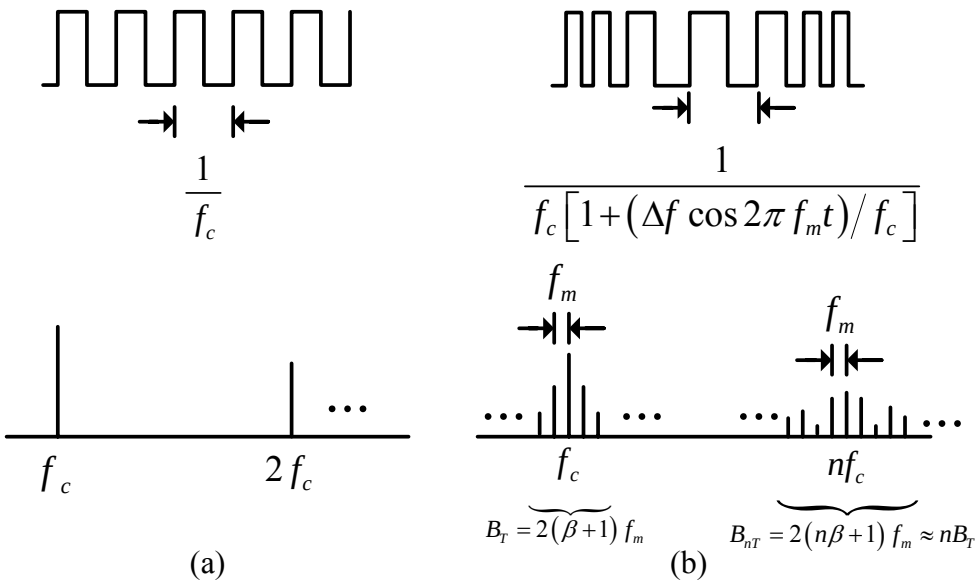


Fig. 4.3 Spectra of (a) square waveform and (b) frequency-modulated square waveform

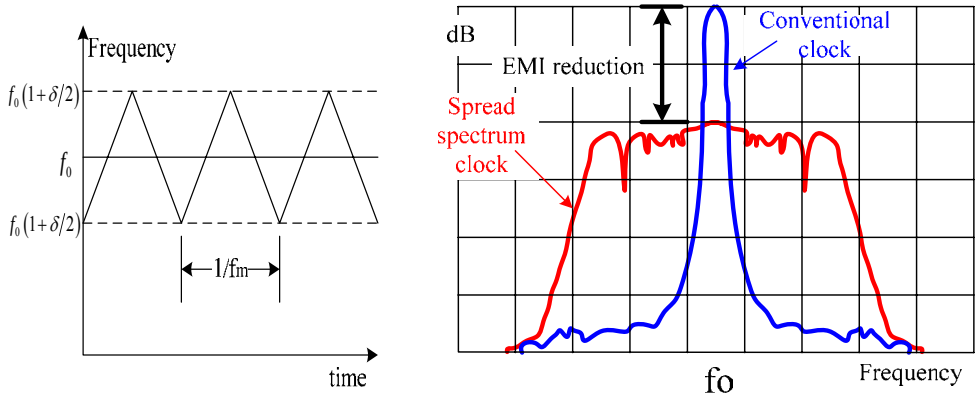
4.3 Spread Spectrum parameter

Based on the frequency ranges of modulated signal, the spread spectrum modes can be divided into three groups: center-spread, down spread, and up-spread.

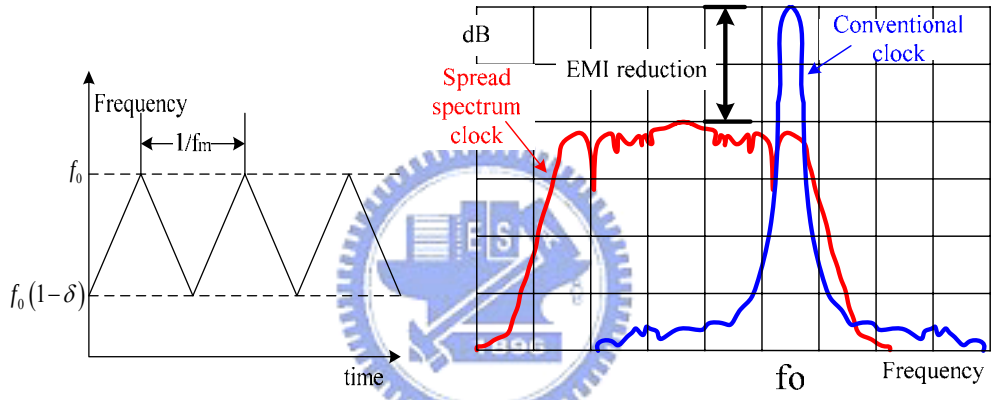
In center-spread (Fig. 4.4(a)), f_m is the modulation frequency and δ is the total amount relative to the nominal frequency f_0 in spreading spectrum. The modulated frequency is centered at the nominal frequency f_0, and varies between $f_0(1+\delta/2)$ and $f_0(1-\delta/2)$. This makes the average frequency of the modulated signal is still f_0. For example, a 1% center-spread modulation means that a 1GHz clock is modulated between 1005MHz and 995MHz.

In down spread (Fig. 4.4(b)), the modulated frequency varies between f_0 and $f_0(1-\delta)$. Thus it has the average frequency $f_0(1-\delta/2)$. Besides, the down spread can be thought as the center-spread with nominal frequency $f_0(1-\delta/2)$ and modulation amount $\delta/2$. For example, a 1% down-spread modulation means that a

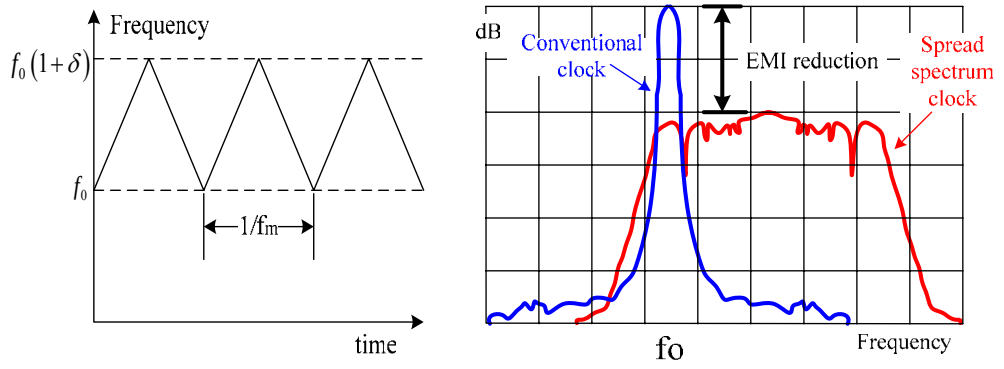
1GHz clock is modulated between 1000MHz and 990MHz.



(a)



(b)



(c)

Fig. 4.4 Modulation profiles and spectrums of (a) center-spread (b) down-spread (c) up-spread

In up-spread (Fig. 4.4(c)), the modulated frequency varies between

f_0 and $f_0(1+\delta)$. Thus it has the average frequency $f_0(1+\delta/2)$. However, some system cannot tolerate over-clocking (operation at higher than nominal frequency). So the up-spread mode is seldom adopted. Besides, there is a period of time that the center-spread will be running between $f_0(1+\delta/2)$ and f_0, which may erode the system timing margin. Using down-spread will avoid this problem with small sacrifice of a slightly slower clock rate.

4.3.1Modulation profile

The key to maximize the attenuation of a clock signal and its harmonics is the modulating waveform. While the modulation frequency is higher, from the Carson's rule, the attenuation is more obvious. However, the modulation frequency should be slow enough to make the stability problem not happened when cooperating with other PLLs. Furthermore, the spread spectrum modulation frequency must be slow compared with the nominal frequency to ensure that the change in the clock rate is transparent to the system.

The modulation profile determines the shape of spectral energy distribution. There are three type modulation profiles we will introduce, that is, sinusoidal signal, triangular signal and saw-tooth signal. Although sinusoidal modulation is easier to analyze and implement, it doesn't provide the ideal attenuation. Triangular modulation, sometimes called linear modulation, provide better EMI attenuation. From ref [15], the energies in the spectrum of the modulated waveform will tent to concentrate at those frequencies corresponding to points in the modulating waveform where the time derivatives are small. We compare modulation profiles and their corresponding spectrums of sinusoidal, triangular and saw-tooth, as shown

in Fig. 4.5. The spectrum of the sinusoidal modulation displays a peaking of the amplitude at the corners. Because the time derivative of the triangular wave at its zero crossing is less than that of sine wave, the amplitude at the center of the spectrum is increased and thus the amplitudes at the corners are reduced. Finally, by decreasing the time derivative at the zero crossing and increase the time derivative at the peaks of the modulation waveform, the optimized modulation profile offers the best-modulated spectrum.

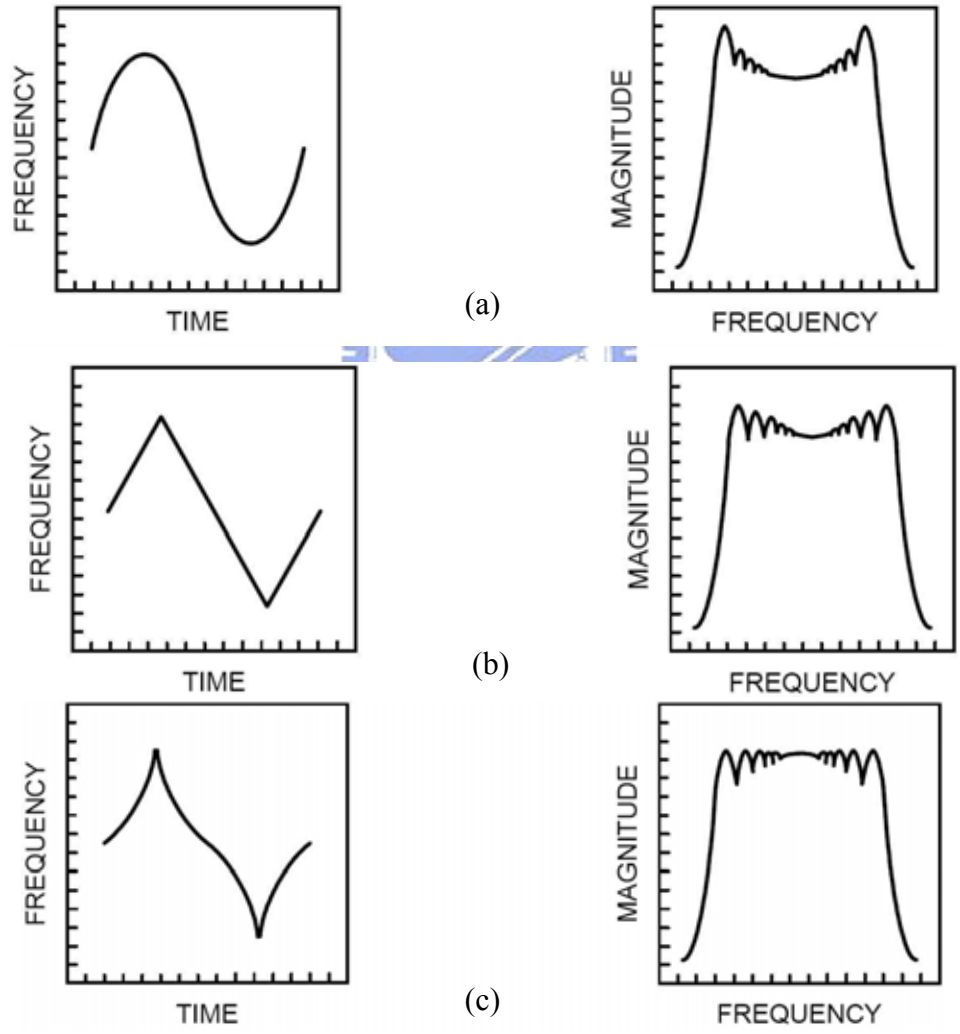


Fig. 4.5 (a) Sinusoidal modulation signal and the resulting spectrum (b) triangular modulation signal and the resulting spectrum (c) saw-tooth modulation signal and the resulting spectrum

4.3.2 Timing Impacts

Since the frequency changes with the modulation profile in the spread spectrum clock system, the period also changes with time. In spite of the modulation profiles, the waveform is approximately as in Fig. 4.6. In fact, we are concerned about the cycle-to-cycle jitter and long-term jitter in time domain. To make sure the jitter would not cause the system work improperly is important.

(a) (b)

Fig. 4.6 Waveforms of (a) un-modulated pulse and (b) frequency-modulated pulse

I. Cycle-to-Cycle Jitter

Cycle-to-cycle jitter is the change in a clock's output transition form its corresponding position in the previous cycle. Let us take the down spread spectrum as an example. The period difference between the maximum and the minimum frequencies is

$$\Delta T_{total} = \frac{1}{(1-\delta) f_{nom}} - \frac{1}{f_{nom}} \approx \frac{\delta}{f_{nom}} \tag{4.8}$$

The number of clocks that exist in the time interval that the modulated clock moves from f_{nom} to $(1-\delta) f_{nom}$ is

$$N = \frac{f_{avg}}{2 f_m} \tag{4.9}$$

The f_{avg} is the average frequency of the spread spectrum clock. From triangular modulation profile, we can derive the average frequency is

$$f_{avg} = (1 - 0.5\delta) f_{nom} \tag{4.10}$$

Therefore, the cycle-to-cycle jitter due to spread spectrum clock can be expressed as

$$\begin{aligned} \Delta T_{c-c} &= \frac{\Delta T_{total}}{N} = \frac{\delta}{f_{nom}} \cdot \frac{2 f_m}{(1 - 0.5\delta) f_{nom}} \\ &= \frac{2 f_m \delta}{(1 - 0.5\delta) {f_{nom}}^2} \end{aligned} \tag{4.11}$$

For a 3GHz spread spectrum clock with 0.5% triangular modulation and 33 KHz modulation frequency, the increase in cycle-to-cycle jitter is

$$\Delta T_{c-c} = \frac{2 \times 33 \times 10^3 \times 0.5\%}{(1 - 0.5 \times 0.5\%)(3 \times 10^9)^2} = 3.676 \times 10^{-17} \tag{4.12}$$

II. Long-Term Jitter

Long-term jitter measures the maximum change in a clock's output transition form its ideal position. Therefore, equation (4.8) can be viewed as the long-term jitter of a down-spreading clock signal. Similarly, for a 3GHz spread spectrum clock with 0.5% triangular modulation and 33 KHz modulation frequency, the increase in long-term jitter is

$$\Delta T_{total} = \frac{\delta}{f_{nom}} = \frac{0.5\%}{3 \times 10^9} = 1.67 \times 10^{12} \tag{4.13}$$

Thus, the increase of cycle-to-cycle jitter of the spread spectrum clock is in a considerably small compared with non-spread clock signal. However, the long-term jitter of spread spectrum signal is enormous.

Chapter 5

SSCG based on the fractional-N PLL

5.1 Introduction

As we know, the fractional-N phase-locked loop is capable of synthesizing frequencies at channel spacing at less than the reference frequency. Thus we can increase the reference frequency and reduce the lock time of PLL. However, a major disadvantage of fraction-N PLL is the generation of fractional spurs. Using ΣΔ modulator can eliminate such spurs by randomization and noise shaping. Therefore, we choose fractional-N based on ΣΔ modulator as our basic architecture to achieve the clock generator.

With the operation speed is higher and higher, currents and voltages present in the circuits and the signal traces lead to greater electro-magnetic interference (EMI). We choose the spread spectrum clocking technique to reduce EMI, because it is simplest and the most efficient. There are three types of spread spectrum clock generators in the literature. The first type controls the divider modulus of the divider in the PLL [1][2][16][17]. The second type modulates the voltage-controlled oscillator [18]. The third type combines the multiphase circuits and switches among them to achieve the spread spectrum clock [19]. Our circuit belongs to the fist type.

5.2 System architecture

Spread spectrum clock generator based on the fractional-N frequency synthesizer is achieved by modulating the input of the ΣΔ modulator with a periodic waveform. Thus the average divider modulus would be changed by a small amount and the output frequency would also be modulated by a small deviation. The EMI reduction is mainly determined by the frequency deviation and the modulation waveform.

As shown in Fig. 5.1, the fractional-N PLL consists of Phase Frequency Detector (PFD), Charge Pump (CP), Voltage Controlled Oscillator (VCO), Loop Filter (LP), Multi-Modulus Divider (MMD), ΣΔ modulator. The up and down counter performs the purpose of frequency modulation. The input of the ΣΔ modulator is controlled by an up and down counter with slow modulation frequency compared to the frequency of the input clock. The modulation frequency is set to 30~33 KHz. The smoothing effect of the PLL loop results in continuous frequency modulation from a discrete staircase input and thus it seems to be modulated by triangle waves. When the output of the ΣΔ modulator is -1, 0, 1, and 2, we select the modulus of the divider as N+1, N, N-1, and N-2 respectively, where $N=f_{nonspread}/f_{ref}$, $f_{nonspread}$ is the non-spread spectrum output frequency (3GHz), and f_{ref} is the reference signal frequency (30MHz). Therefore, if the input of the ΣΔ modulator is m, the average frequency of the output will be equal to:

$$f_{spread} = f_{ref}\left(N - \frac{m}{2^k}\right) = f_{nonspread}\left(1 - \frac{m}{N \times 2^k}\right) \qquad (4.13)$$

The m runs periodically as 0, 1, 2… M….2, 1, 0, 1, 2… We use 6-bits accumulators to construct the modulator, so M is chosen to be 32 to achieve -5000

ppm spread spectrum frequency range.

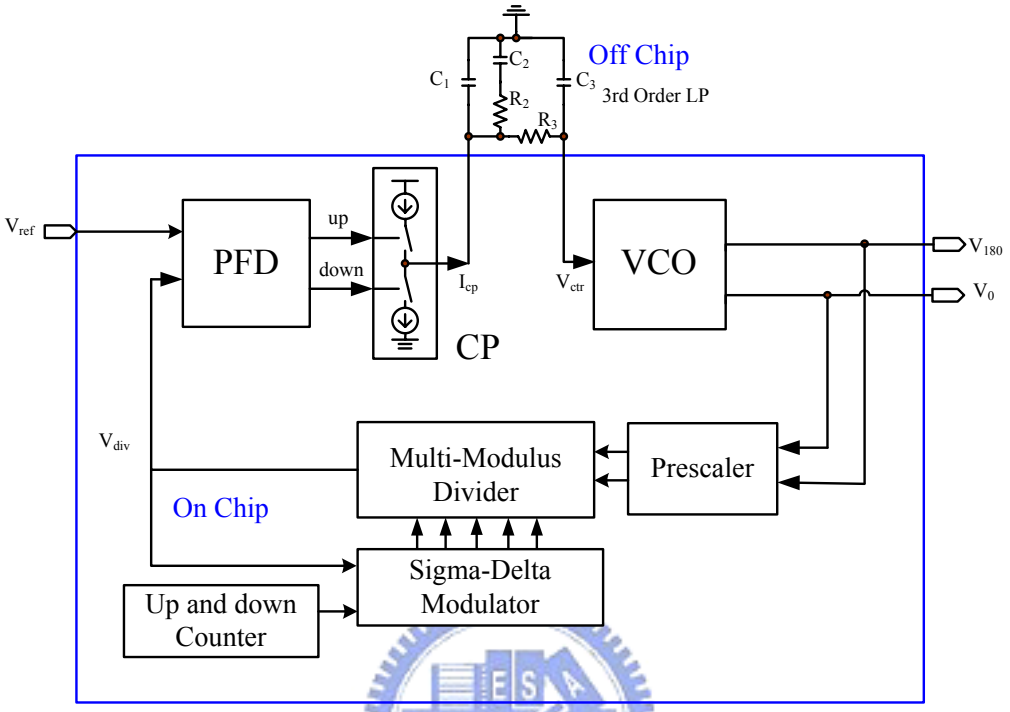
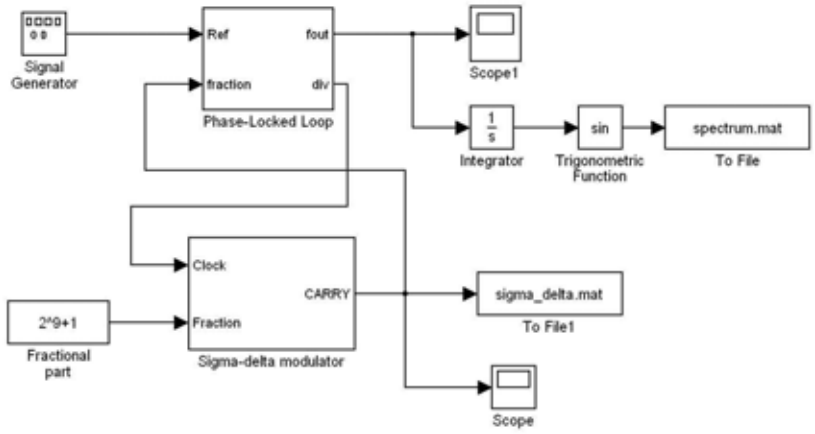


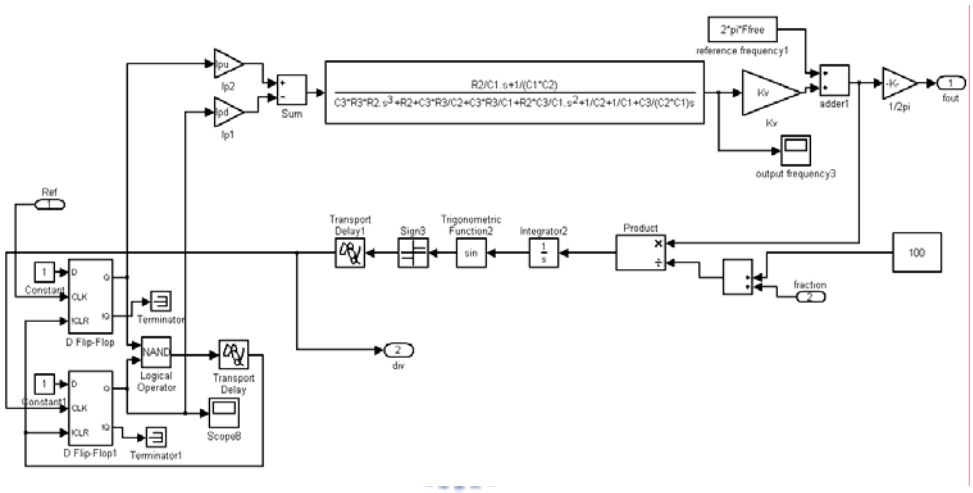
Fig. 5.1 the architecture of SSCG based on ΣΔ modulator

5.3 Behavior simulation

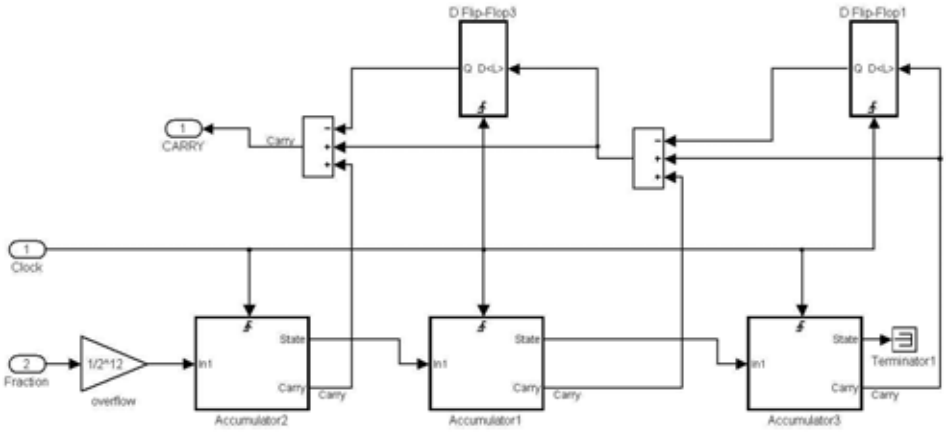
Because of the great amount of gates counts in the phase-locked loop, the closed-loop simulation with HSPICE will take a lot of time. In order to rapidly and approximately know the behavior of PLL, we use SIMULINK to test and verify system parameters and transient response. Fig. 5.2 shows the behavioral model built with SIMULINK [20].



(a)



(b)



(c)

Fig. 5.2 SIMULINK model of the fractional-N frequency synthesizer (a) Fractional-N frequency synthesizer (b) Phase-locked loop (c) 3rd order ΣΔ modulator

The behavior simulation of fractional-N frequency synthesizer is shown in Fig. 5.3.

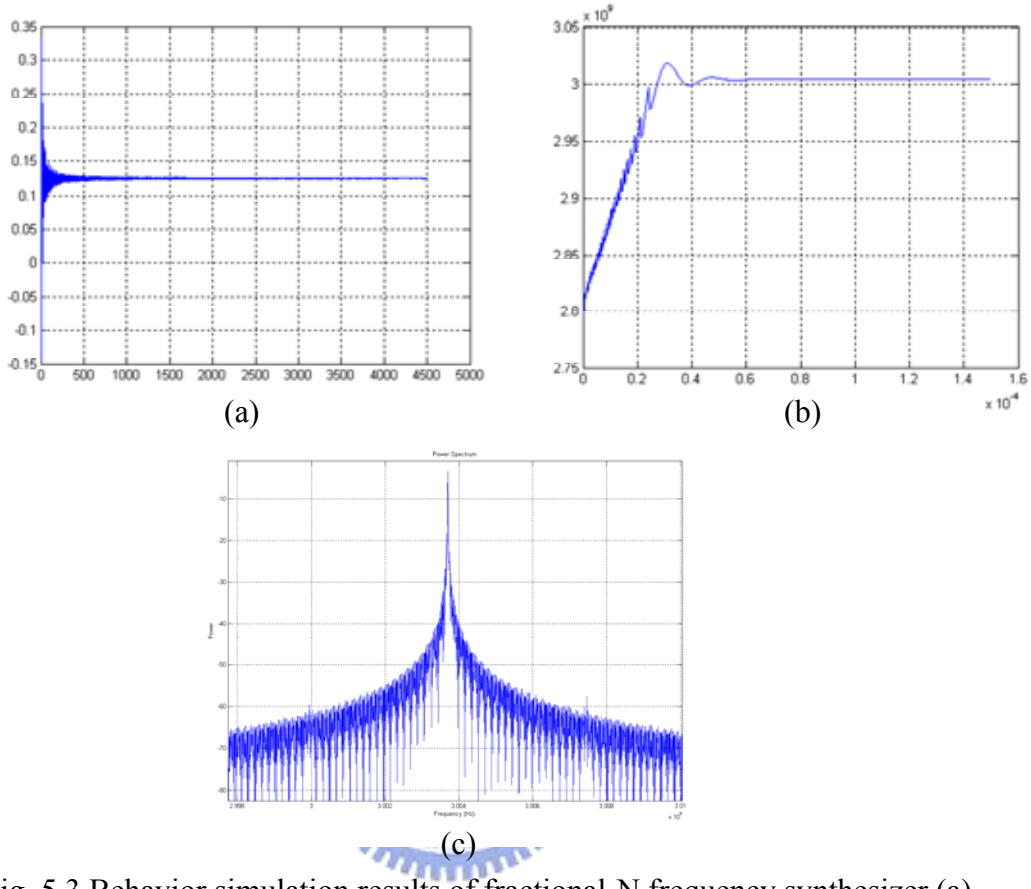


Fig. 5.3 Behavior simulation results of fractional-N frequency synthesizer (a) average output of ΣΔ modulator (b) transient response (c) frequency response

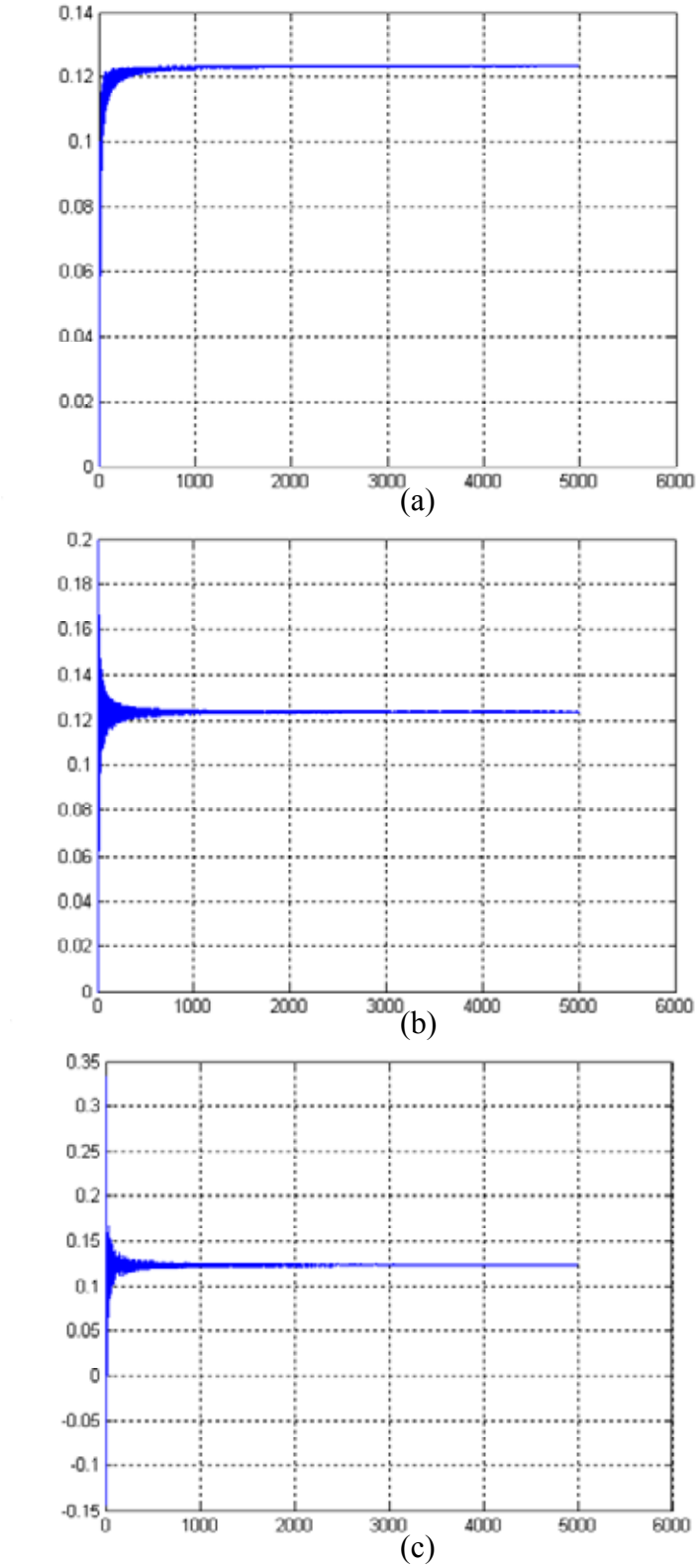


Fig. 5.4 Average output of ΣΔ modulator (a) 1st order (b) 2nd order (c) 3rd order

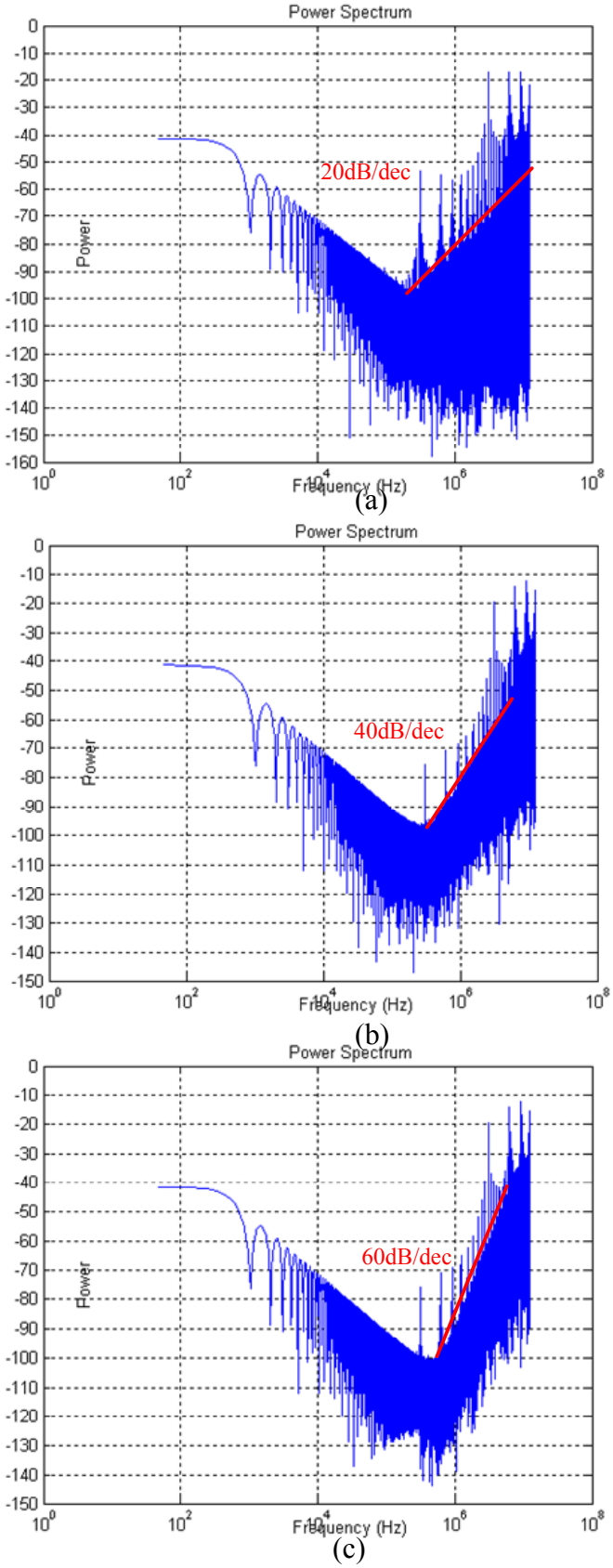
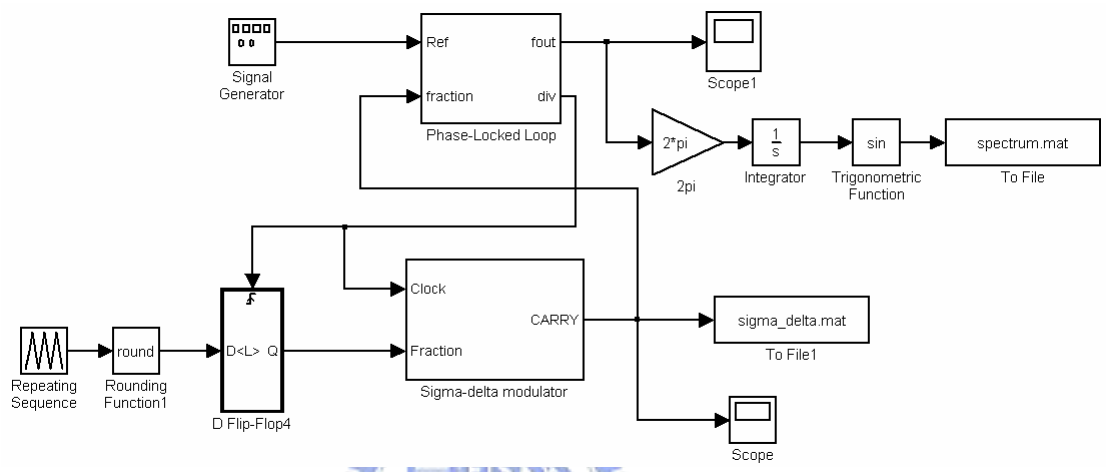


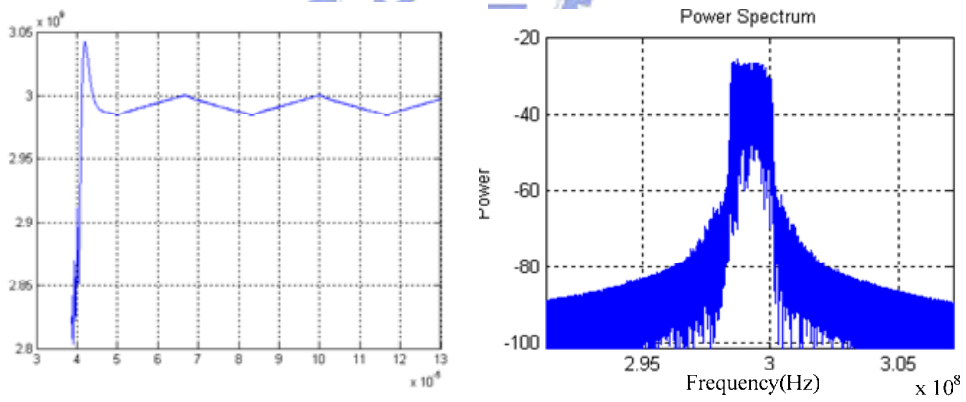
Fig. 5.5 PSD of ΣΔ modulator (a) 1st order (b) 2nd order (c) 3rd order

Fig. 5.4 shows the comparison of the convergence speed of various orders of ΣΔ modulator and Fig. 5.5 shows their corresponding power spectrum density.

Fig. 5.6 shows the SIMULINK model of spread spectrum clock generator. We use other blocks to construct the triangular waveform to control the input of ΣΔ modulator.



(a)



(b) (c)

Fig. 5.6 Behavior simulation results of spread spectrum clock generator (a) SIMULINK model of SSCG (b) transient response (c) frequency response

5.4 Circuit Implementation

5.4.1Phase / Frequency Detector

Fig. shows the modified version of sequential phase frequency detector (PFD) proposed in [21]. It only uses 12 transistors and thus possesses little small parasitic inherently. Compared with conventional PFD, the dynamic PFD overcome the speed limitation and reduce the dead zone. Due to the input inverters, the dynamic PFD changes from negative-edge trigger to positive-edge trigger. Fig. 5.8 shows the timing diagram. If the REF leads the FB, the UP pulse will be high for a while and then the DN pulses changes to high. The width difference between UP and DOWN pulses will be proportional to the phase difference of the inputs.

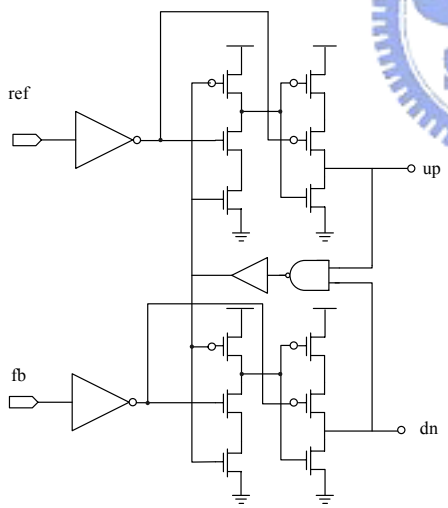


Fig. 5.7 Circuit of PFD

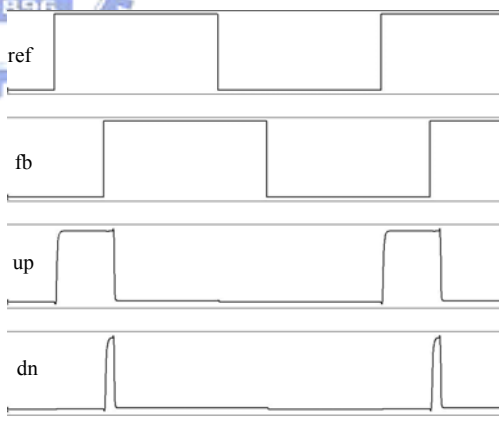


Fig. 5.8 the timing diagram of PFD

5.4.2Charge Pump

The charge pump (CP) that converts digital outputs from PFD into analog control signals for local oscillators is an essential component of phase-locked loop. The implementation of integrated PLL charge pump faces many challenges.

Decreasing clock feedthrough from the charge pump to the VCO is a crucial issue. Obtaining a large output voltage range, while operation from a low power supply, is another issue that remains to be addressed.

Single-ended charge pumps are popular since they don't need an additional loop filter and offer low-power consumption with tri-state operation. Fig. 5.9(a) shows the conventional charge pump with switches at the drain of the current source. However, it has many problems. For example, when the switches are OFF, the voltage at output capacitor C is floating, while the voltages at the sources of S_1 and S_2 are rapidly pulled to VDD and ground respectively. Due to the non-ideal characteristics of the MOS switch, such as charge injection and clock feedthrough, this rapid change in the source voltages creates glitches in the capacitor current, which results in a jump in the stored voltage V_C. Any jump in V_C adds undesirable spurious tones and phase noise to the output signal of the VCO. Besides, when the switches are OFF, the voltage at node X and Y are V_{dd} and gnd, respectively and the output voltage V_C is floating. When the switches are turned ON, the voltage at node X will decrease and that on node Y will increase, resulting in charge sharing between C_L, C_X and C_Y, and a consequent deviation in the output voltage V_C. A possible approach is to add a unity gain amplifier as shown in Fig. 5.9(b) [22]. The voltage at the X and Y is set to the voltage at the output node when the switches are turned off to reduce the charge sharing effect when the switch is turned on. However, the enhancing performance comes at the expense of extra complexity, area, and power consumption.

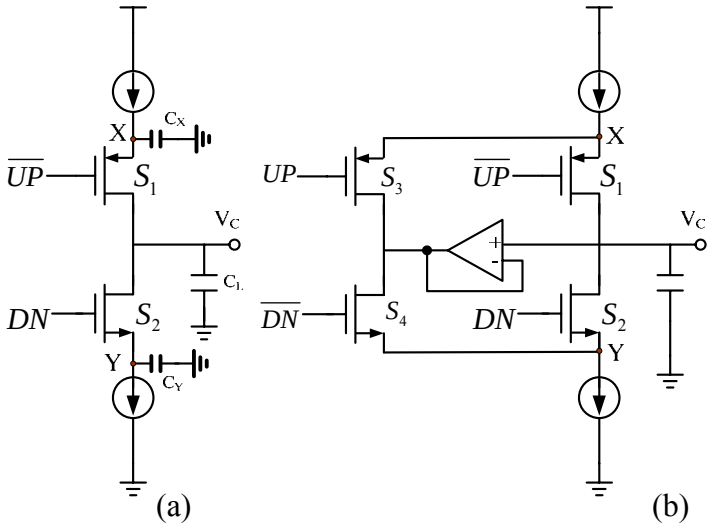


Fig. 5.9 Single-ended charge pumps (a) switch in drain (b) with active amplifier

Another one is the charge pump with the current steering switch as shown in Fig. 5.10(a). The performance is similar to the one shown in Fig. 5.9(b) but the charge injection error is reduced and the switch time is improved by using the current switch. In Fig. 5.10(b), the inherent mismatch of PMOS and NMOS is avoided by using only NMOS switches [23]. However, this charge pump suffers from a slow-path node at the gate of M6, which is the point A. when M4 is ON, M3 is OFF, but M6 still conducts current until the parasitic capacitance at the slow-node is fully discharged. Moreover, when M3 is OFF, current is wasted in the M4-I_{CP} branch.

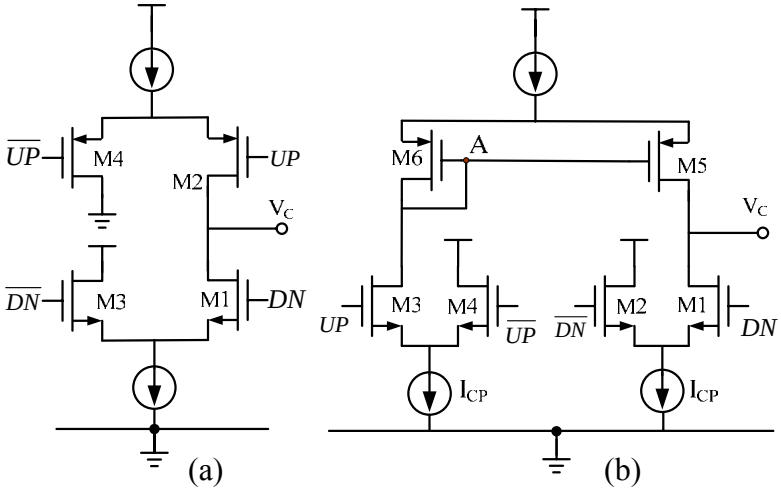


Fig. 5.10 (a) Conventional current-steering CP (b) NMOS switches only CP

In order to solve the slow-path problem, Chang proposed a current-steering CP with a pull-up mirror as shown in Fig. 5.11(a) [24]. The pull-up circuit is used to increase the charge speed of node A. However, when the current of the input pair is steered to M1, M3 still conducts a temporal current, which modulates the VCO, introducing phase noise. The time constant associated with node A is not a well-defined parameter and makes a slow path. Other drawback of this circuit is that in order to increase charging speed at A, I_S must be increased. However, increasing I_S will decrease the net charging/discharging current of CP finally and the speed of the circuit. In order to maintain speed, one would have to increase I_B and consequently the power consumption. Finally, when the current source I_B is steered through M1, this current is wasted since it's not any more utilized, thus wasting power.

Sanchez [25] modified Chang's CP by removing the current-source I_S and connected the drain of M6 directly to that of M1, as shown is Fig. 5.11(b). Since I_B is greater than the injection current I_S in the previous structure, M4 is turned off faster. Besides, the current waste problem is resolved. However, the problem of a slow path on node B still exists. To solve this problem, pull-up transistor M7 is added. The final configuration is a simple positive feedback amplifier with gain enhancement, where the switching speed is increased, as shown in Fig. 5.11 (c). Nevertheless, positive feedback puts a restriction on the input signal $\overline{UP}$, for M1 to stay in saturation, $\overline{UP}$ must be less than VDD; this requires additional circuitry [26].

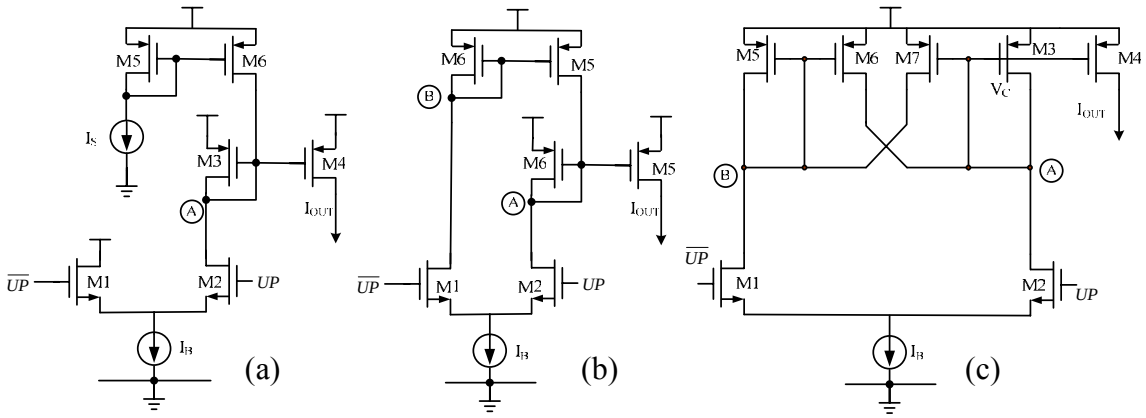


Fig. 5.11 (a) Chang's CP (b) Current reuse (c) Current reuse and positive feedback

To implement a very low voltage charge pump, the above configurations are not suitable because they cascode at least three MOS transistors. Sharma [27] included a low-voltage switched push-current source. We adopt it and make some modification, as illustrated in Fig. 5.12. The switch-at-gate charge pump uses an inter-locked structure and has more stable output voltage than the switch-at-drain charge pump because it eliminates charge sharing. We should note that any jump in V_{OUT} adds an undesirable spurious tones and phase noise to the output signal of the VCO. Besides, since the structure is composed of one PMOS and one NMOS, it is suitable for the low voltage supply. Although it may suffer from reduced switching speed due to the large parasitic capacitance at the gates, we can compensate for speed by using larger bias current.

The charge pump operates form a 1V power supply as follow:

1. <u>When the signal UP is at logic zero:</u>

✧ Transistor P3 is ON, and the current of P3 is steered into transistors N3 and P5. Since the power supply is 1V, when transistor P5 is ON, transistor P4 will not have enough voltage headroom between its gate and source to be ON.

✧ The transistor P6 is therefore OFF and the current in P6 can be negligible. The voltage at the output capacitor will remain stable.

2. When the signal UP is at logic high:

✧ Transistor P3 is OFF and the current of N3 is steered to transistor P4. Similarly, because of not enough headroom, the transistor P5 is OFF.

✧ Due to the current mirror formed by transistors P4 and P6, the current in P5 will be mirrored and be pushed into the capacitor C, raising the voltage V_{OUT}.

For the proposed structure, the current driving capability of transistor P3 must be larger than that of transistor N5, or the circuit would operate incorrectly. The above circuit performs pull-up function. For pull-down, a similar circuit is used and shown in Fig. 5.12.

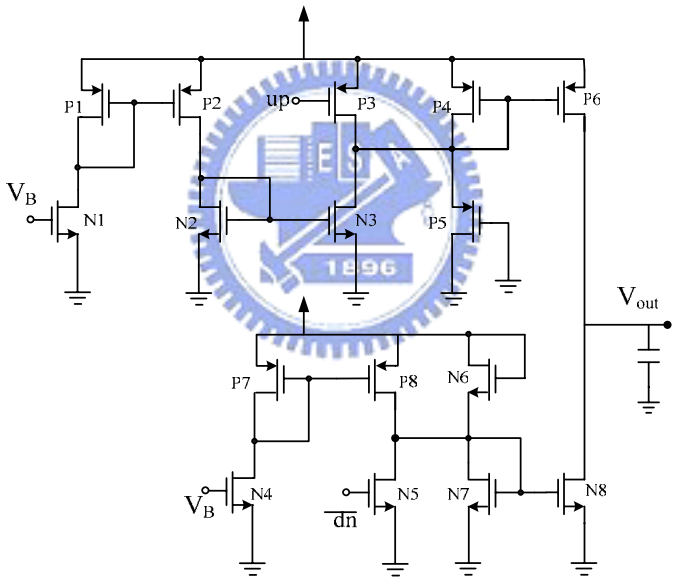


Fig. 5.12 1-volt Charge Pump

As shown in Fig. 5.13, when there is a phase error, the pulse of UP is longer than $\overline{DN}$, causing there is net current charging the output capacitor.

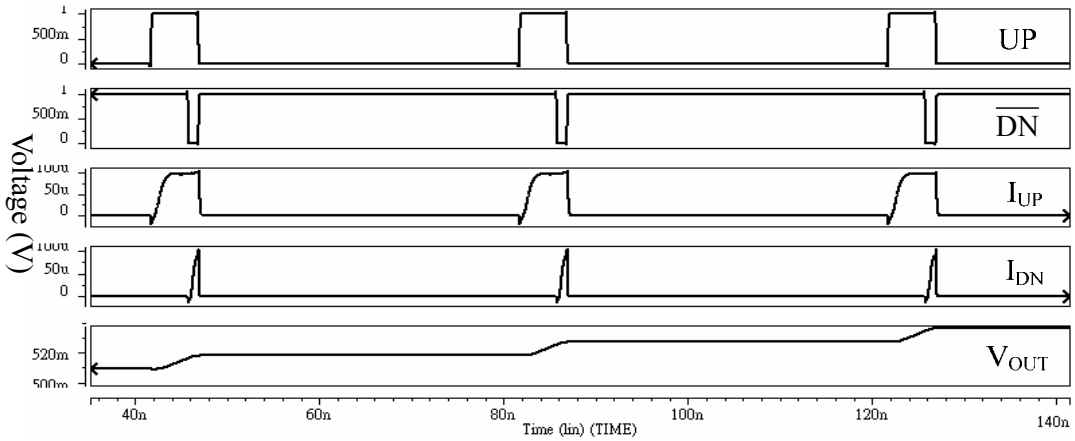


Fig. 5.13 Simulation results of charge pump (with capacitor only)

Fig. 5.14 shows the dead zone simulation. By increasing the reset time of PFD, we can decrease the dead zone as much as possible. Fig. 5.15 compares the charging current and discharging current under various output voltages. It is obviously they are only the same in a specific voltage because of the channel length modulation. We can ease the phenomenon by increase the length of transistors P6 and N8. Other method has been proposed by forcing the current of PMOS to be the same as that of NMOS [28].

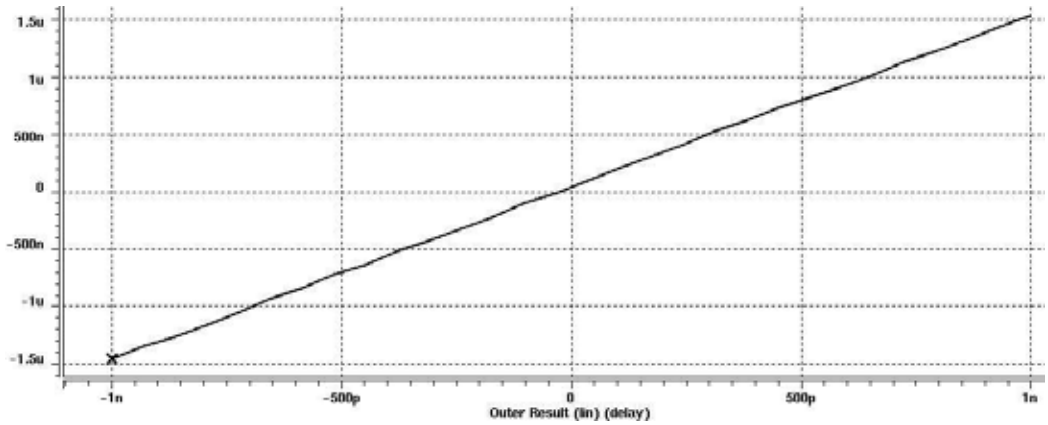


Fig. 5.14 Dead zone simulation of PFD with CP

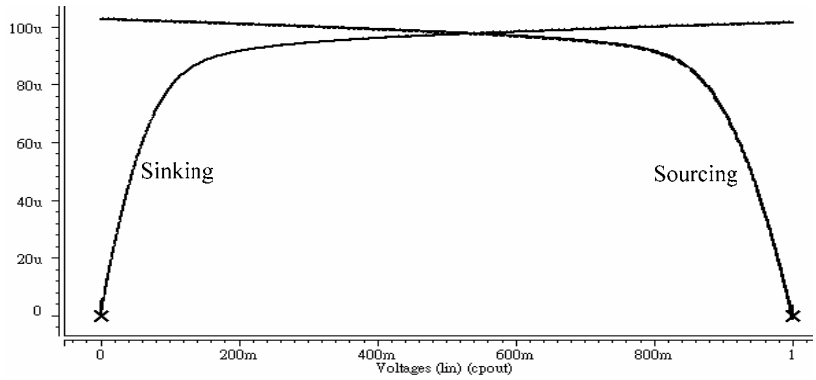


Fig. 5.15 Charge pump current matching characteristic

5.4.3Loop Filter

As we know, the loop filter mainly determines the noise and dynamic performance of the PLL. In order to effectively attenuate the reference spur, we adopt the 3rd order loop filter. To decide the proper values of each element, the basic steps are as follows [3]:

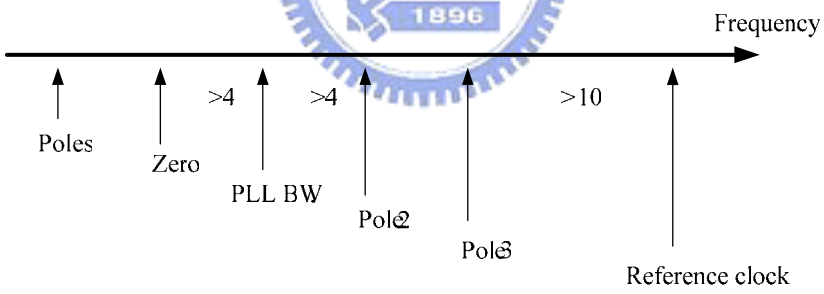


Fig. 5.16 Relationship between zero, poles, reference and loop bandwidth

1. As a rule, the relationship between zero, poles, and reference and loop bandwidth are shown in Fig. 5.16. Deciding the proper values of open-loop unity-gain bandwidth ω_P, phase margin ϕ and the added attenuation from the third pole.
2. Calculate the time constant T_1 and T_3. Then we can get the new unity-gain bandwidth ω_C due to the added third pole.

$$T_1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} \tag{5.1}$$

$$T_3 = \frac{1}{\omega_3} = \sqrt{\frac{10^{(ATTEN/10)} - 1}{(2\pi F_{ref})^2}} \tag{5.2}$$

$$\omega_c = \frac{\tan\phi \cdot (T_1 + T_3)}{\left[(T_1 + T_3)^2 + T_1 T_3\right]} \times \left[\sqrt{1 + \frac{(T_1 + T_3)^2 + T_1 T_3}{\left[\tan\phi \cdot (T_1 + T_3)\right]^2}} - 1\right] \tag{5.3}$$

3. Calculate the time constant T_2.

$$T_2 = 1 \Big/ \left[\omega_c^2 (T1 + T3)\right] \tag{5.4}$$

4. Thus we can derive the value of each element.

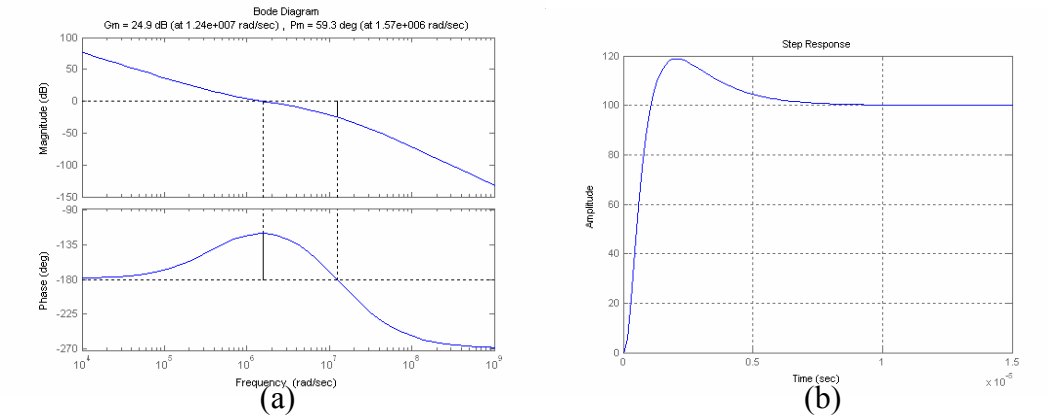
$$C_1 = \frac{T_1}{T_2} \frac{K_{pd} K_{vco}}{\omega_c^2 N} \left[\frac{(1 + \omega_c^2 T_2^2)}{(1 + \omega_c^2 T_1^2)(1 + \omega_c^2 T_3^2)}\right]^{1/2} \tag{5.5}$$

$$C_2 = C_1 \left(\frac{\omega_1}{\omega_2} - 1\right), \quad R_2 = \frac{1}{C_2 \omega_2} \tag{5.6}$$

5. As rule of thumb chooses $C_3 \le C_1/10$, otherwise T_3 will interact with the primary poles of the filter.

$$C_3 = C_1/10, \quad R_3 = T_3/C_3 \tag{5.7}$$

Fig. 5.17(a) shows bode plot of the open loop transfer function of PLL and Fig. 5.17(b) shows the step response. The result is as we expect. It proves the above equations are precise enough to estimate PLL parameters.



(a) (b)

Fig. 5.17 (a) Bode plot of open loop PLL (b) step response of closed loop PLL

5.4.4Voltage Controlled Oscillator

Voltage-Controlled Oscillators (VCO) is one of the key elements in frequency synthesizer and most critically determines the performance of a frequency synthesizer. Recently, because of the increasing demand for lower cost and higher integration, CMOS VCO's have been continuously studied and enhanced. The big challenges for the CMOS VCO's are the low phase noise, sufficient tuning range and acceptable power consumption. There are mainly two implementations of VCO design: LC tank and ring oscillator. LC-tank oscillators with an on-chip spiral inductor are widely adopted in the wireless communication applications due to their ease of achieving high frequency with low phase noise and power consumption [29]. However, it still has several barriers to overcome before becoming a reliable VCO. Implementing a high-quality inductor in a standard CMOS process is limited by parasitic effects and often requires nonstandard processing steps [30][31]. Besides, the tuning range of integrated LC-tank oscillator is generally small, so that the performance of the frequency synthesizer is sensitive to the process variations.

The schematic shown in Fig. 5.18 is a top-biased differential LC-tank VCO. Because the current source is placed in the N-well, rather than in the substrate, the top-biased oscillator has better immunity to the substrate noise than the tail-biased oscillator. Furthermore, due to the use of cross-coupled NMOS transistor pair and PMOS transistor pair, we have several advantages, such as double $G_{m,}$ current reuse, saving power and symmetrical waveform.

We use the common drain amplifier as the output buffer because of its high driving capability. Besides, due to the small output resistance, it is much easier to match the input resistance of spectrum analyzer. The level shift behind the source

follower is to adjust the dc bias of the output signal, making the prescaler work properly. The simulation result of VCO is shown in Fig. 5.19

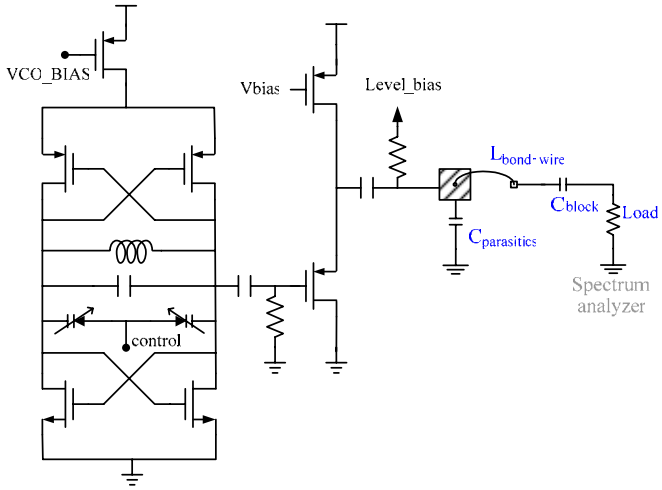


Fig. 5.18 VCO with common drain amplifier as output buffer

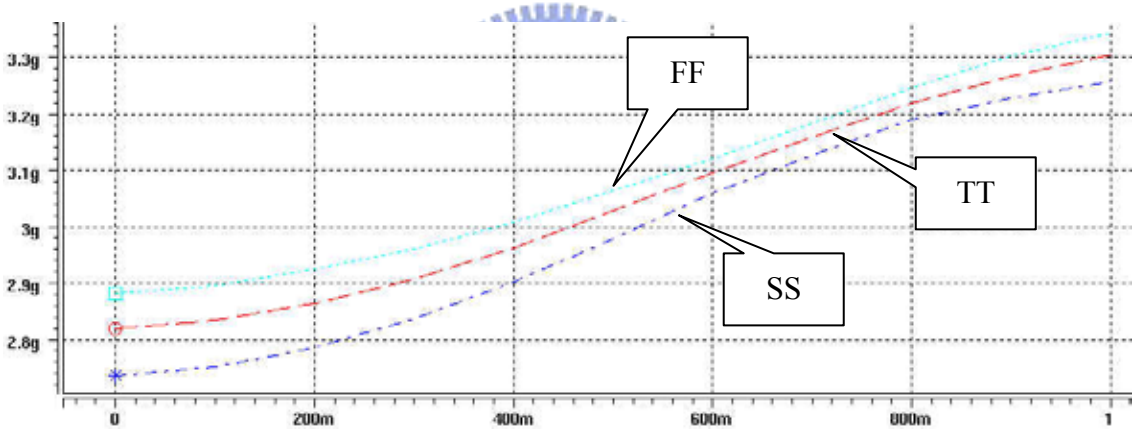


Fig. 5.19 Simulation results of the voltage-controlled oscillator

Fig. 5.20 shows another type of output buffer, that is Bias Tee. It uses an off-chip inductor as the load of the common source amplifier. Here we have considered the effect of bonding wire, which contains two parasitic capacitors and one inductor. Before connecting to the spectrum analyzer, dc blocking capacitor must be put in order not to influence the bias of the amplifier.

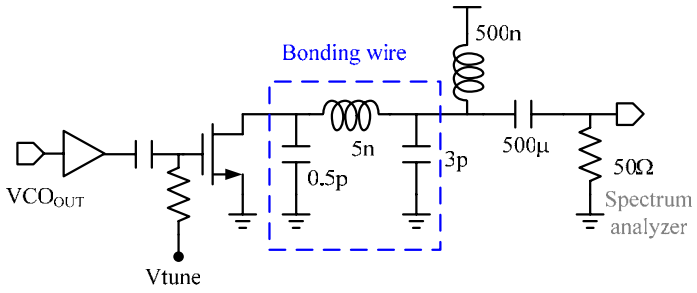


Fig. 5.20 Bias Tee as output buffer of VCO

A modified Bias Tee is shown in Fig. 5.21. It doesn't need any off-chip inductor and capacitor as its load impedance. However, it cleverly uses the input resistor of spectrum analyzer as its load impedance. To be sure that the gain of amplifier is enough, the simulation must be more careful.

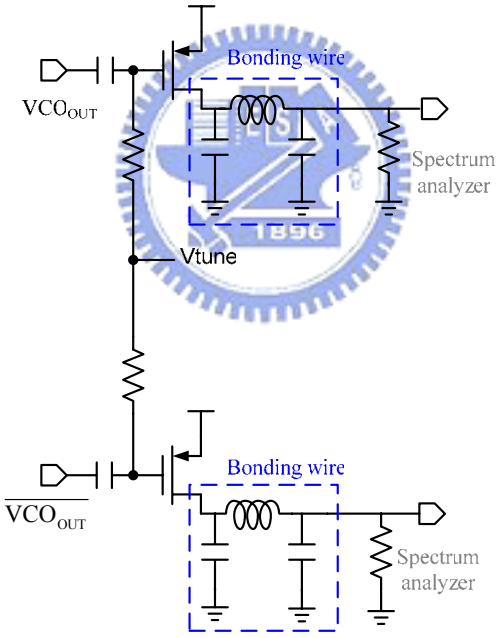


Fig. 5.21 Modified Bias Tee as output buffer of VCO

Generally speaking, a ring oscillator is much easier to be integrated in a standard CMOS process without extra processing steps, because it doesn't need any passive resonant element. It also owns wide tuning range and occupies smaller area than the LC tank oscillators. However, the ring oscillator usually shows poorer phase-noise performance, because it contains many noisy active and passive devices

in the signal path [32]. Another limitation of ring oscillator is its achievable highest frequency. With the advance of process, a 10-GHz CMOS ring oscillators is proposed in [33]. A low power dissipation and low phase noise has also been achieved.

Fig. 5.22 shows the ring oscillator with dual-delay path which can reduce the smallest delay per stage [34][35]. The basic idea of dual-delay path oscillators is to add another secondary feedforward path into the loop to make the delay per stage smaller than that of the single-loop oscillators. The bold lines in Fig. represent the primary loop and the colored lines represent secondary loop. Therefore, we can see that the secondary inputs are turned on earlier than the primary inputs, so the outputs of the delay cell will start to change and thus the delay time is reduced.

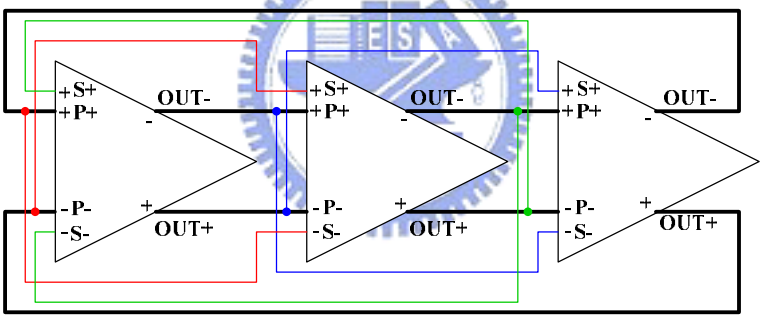


Fig. 5.22 Block diagram of ring oscillator with dual-delay paths

In Fig.5.23, the design evolution of the proposed ring oscillator is illustrated. Fig. 5.22(a) shows the basic differential delay cell structure with the dual-delay path. The NMOS transistors M1 and M2 form the input pair for the primary loop, while PMOS transistors M5 and M6 serve as the input pair of the secondary loop. The oscillatory frequency is control by the gate voltage of M4 and M5. Here we eliminate the tail current source in order to reduce the 1/f noise and increase the output voltage swing. Besides, the structure can be operated properly in the low voltage.

However, because there is no balancing between the two outputs, the ring oscillator will produce irregular waveforms or even no more oscillate. Some self-balancing mechanism must be adopted to prevent the differential outputs from settling to the same voltages. Hence, the positive feedback composed of cross-coupled NMOS pair is added to differential oscillator, as shown in Fig. 5.23(b).

When the control voltage is larger than $Vdd-|V_{thp}|$, the PMOS transistors M3 and M4 will be cut off and consequently the circuit will fail to oscillate. In order not to make the oscillator fail, another PMOS transistor pair is added to the load. Their gate voltages are connected to a fixed voltage, e.g., V_{dd}, so the circuit will still oscillate at very high voltage, as shown in Fig. 5.23(c). Besides, the added load yields a smaller tuning range, and thus reduces the gain and makes the circuit less sensitive to noise, as illustrate in Fig. 5.24.

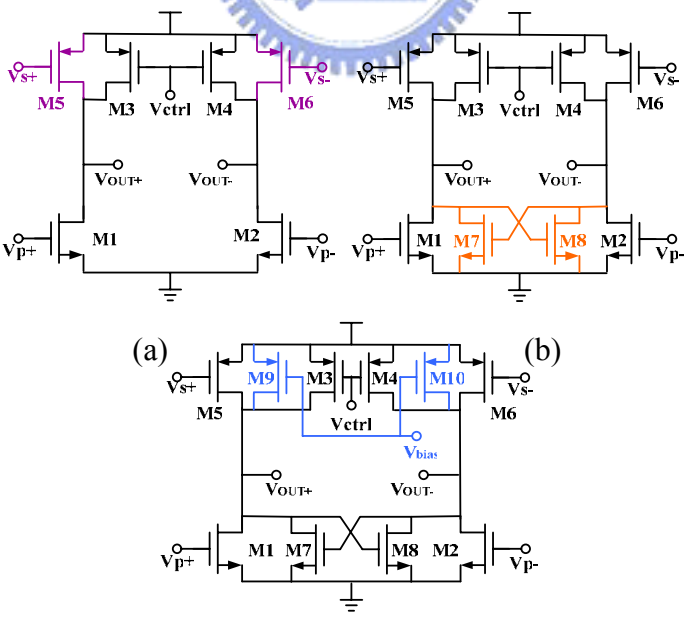


Fig. 5.23 Design evolution of the proposed ring oscillator differential delay cell: (a) basic structure with dual-delay paths, (b) delay cell with cross-coupled NMOS pair for oscillation sustaining, (c) additional PMOS biased to avoid oscillation failure in

extreme case of frequency tuning

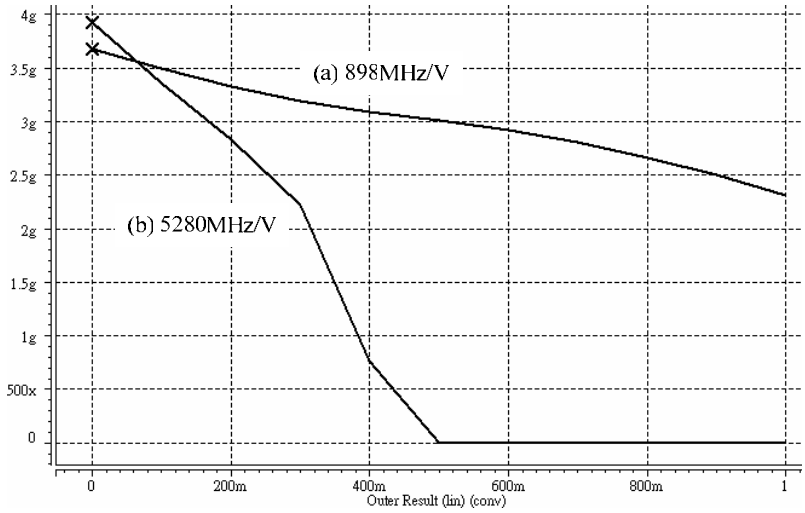


Fig. 5.24 Characteristics of VCO (a) with additional PMOS load (b) without additional PMOS load

5.4.5 Prescaler

Because of the oscillatory frequency of the VCO is very high, we first employ a prescaler to decrease the input clock frequency of the following multi-modulus divider. Fig. 5.25(a) shows the block diagram of common 1/2 frequency divider using two D-latches in a master-slave configuration with negative feedback. In high speed operation, it's usual practice to design the slave as the "dual of the master", such that they can be driven by a single clock [36]. Nevertheless, duality will make one of the latches uses PMOS devices in the signal path, lowering the maximum operation speed. Razavi proposed a divider utilizing two identical D-latches, driving by complementary clocks [37], as illustrated in Fig. 5.25(b). The transmission gate in the non-inverted phase is to minimize the skew between CK and $\overline{CK}$.

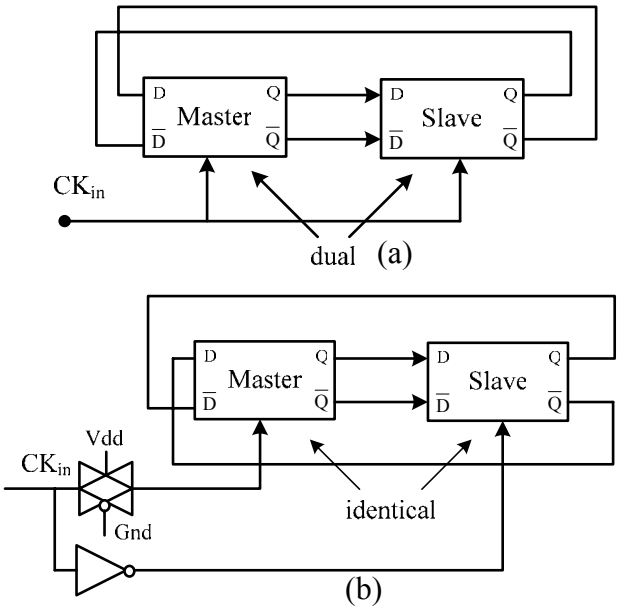


Fig. 5.25 Master-slave divider with (a) single clock (b) complementary clocks

Fig. 5.26 shows the high speed divider circuit [37]. Each latch comprises two sense devices (M1, M2, M7, M8), a regenerative loop (M3, M4, M9, M10), and two pull-up devices (M5, M6, M11, M12). When the CK is high, M5 and M6 are off, and the master is in the sense mode. In the same time, M11 and M12 are on, and the slave is in the store mode. When CK changes to low, the reverse occurs.

Especially, this circuit is different from the conventional latch topologies. The D-latch does not disable its input devices when it goes from the sense mode to the store mode. However, it does not make the divider work improperly. When the master is in the sense mode, and the slave is in the store mode, the master's outputs can only change from high to low and hence cannot override the state stored in the slave. Fig. 5.27 shows the measured waveforms between input and output of the divider at f_{in}=3GHz. In this measurement, the supply voltage is 1V, and the input amplitude is about 700mV. It is worthy to note that due to no stacked or pass transistors in the circuit; it can work excellently in the low voltage supply. Besides, the swing of CK can be as low as 200mV, saving power of output buffer of VCO.

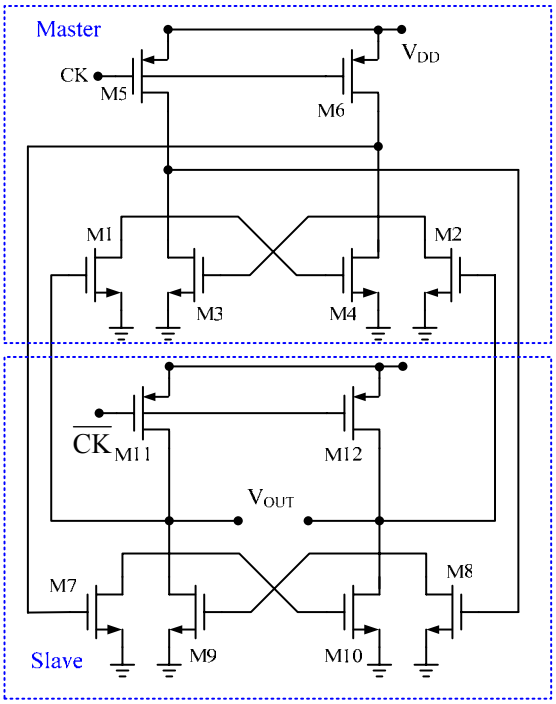


Fig. 5.26 High speed, low voltage frequency divider

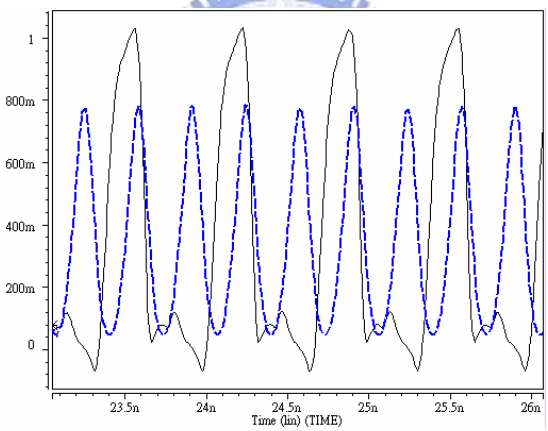


Fig. 5.27 Measured divider input/output waveforms for f_{in}=3GHz

5.4.6 Multi-Modulus Divider (MMD)

The fractional divider ratio is made from a MMD working in an appropriate ratio. Therefore, a programmable MMD is necessary in our design. Fig. 5.28 shows the MMD and Fig. 5.29 shows the circuit of the ÷2/3 divider [38]. This design cascades five ÷2/3 dividers to achieve the divider ratio of 2^5 to 2^6-1. Differing from the traditional MMD, this structure fulfills control qualification by synchronizing within each stage before passing to the previous stage, and therefore avoids jitter

accumulation. Besides, the ÷2/3 divider has similar complexity compared to the traditional MMD [39], two registers and accompanying logic gates. That is, no extra cost has to be paid. The implementation of the ÷2/3 divider can use CML or standard rail-to-rail CMOS logic. The CML can operate in higher frequency under small voltage swing. Therefore, the first two ÷2/3 dividers are implemented with the CML structure, as illustrated in Fig. 5.30 [37]. Although CML usually consumes larger power than CMOS digital logic, it is comparable with CMOS digital logic when operating in high frequencies.

Fig. 5.30 shows CML combing the AND gate logic. It is used to form the three latches and three AND gates in the ÷2/3 divider. The latch without AND gate is composed of normal CML latch. After two ÷2/3 dividers, the signal swing is larger and the frequency is reduced, so we select rail-to-rail CMOS logic to achieve the remaining blocks. We propose a low voltage latch shown in Fig. 5.31. It can operate properly in low voltage (1V) and at frequencies up to 1GHz.

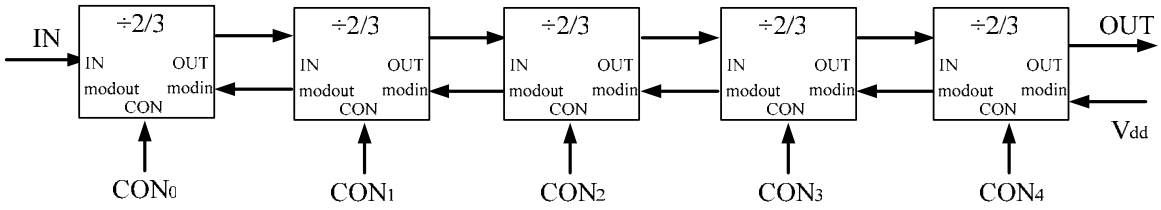


Fig. 5.28 Multi-Modulus Divider

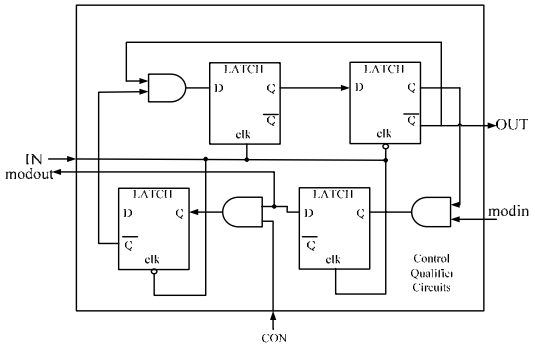


Fig. 5.29 ÷2/3 divider

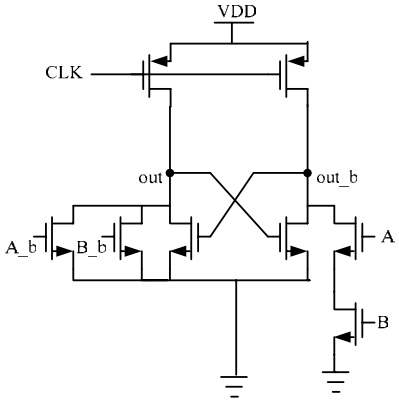


Fig. 5.30 Current Mode Logic embedded AND gate

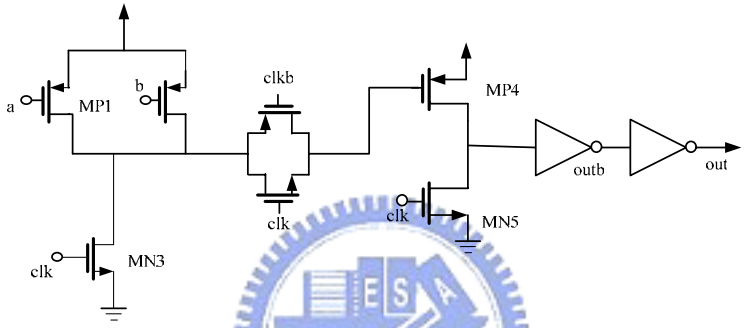


Fig. 5.31 Low voltage latch embedded AND gate

5.4.7 ΣΔ Modulator

In the traditional fractional-N synthesizer, the divider is controlled by counters. Such divider modulus is usually deterministic and will cause unwanted spurs in spectrum. In this design, we use a 2^{nd} order ΣΔ modulator to solve these problems [10]. Fig. 5.32 shows the pipelined 2^{nd} order ΣΔ modulator. The ΣΔ modulator can randomize the divider modulus and cause noise shaping. Besides, the pipelining technique causes the ΣΔ modulator to eliminate spur in output and thus can operate in higher speed. The positive to negative converter performs the effect of down spread spectrum.

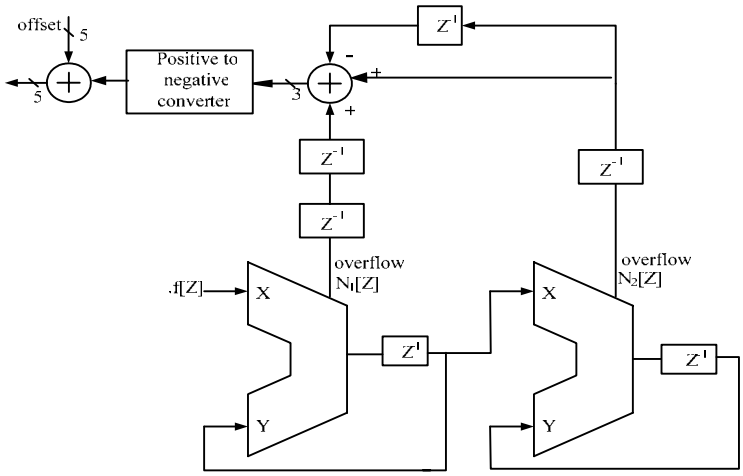


Fig. 5.32 2nd order ΣΔ modulator with control logic

5.4.8 Up/down counter

Because we add a prescaler behind VCO, the maximum input of ΣΔ modulator is set to 16. For simplicity, we use four DFFs to construct the up and down counter, as shown in Fig. 5.33. When the select becomes zero, it acts like an up counter, otherwise a down counter. The simulation result is shown in Fig. 5.34.

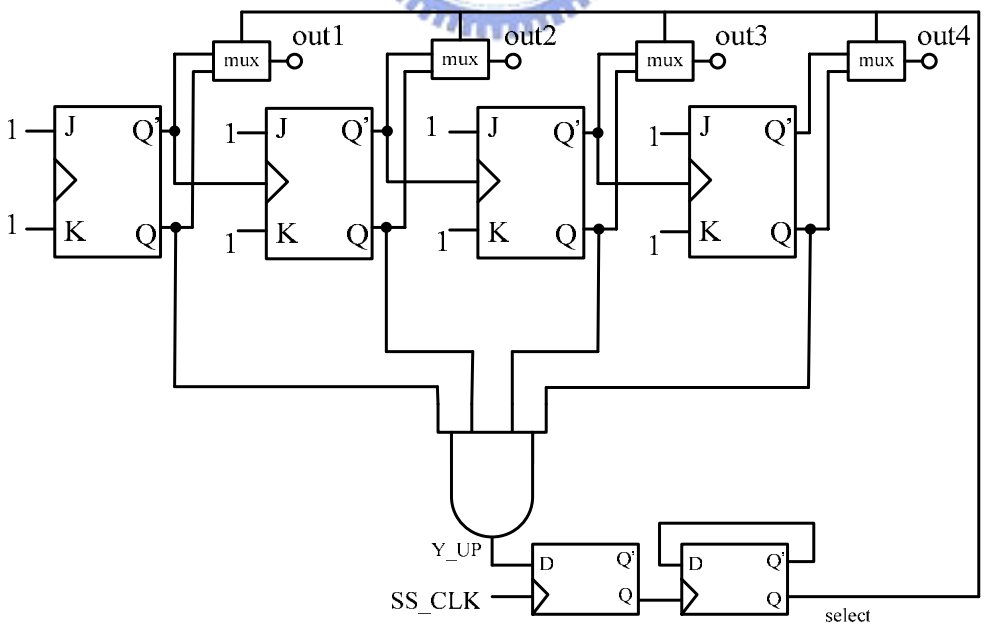


Fig. 5.33 Circuit of up/down counter

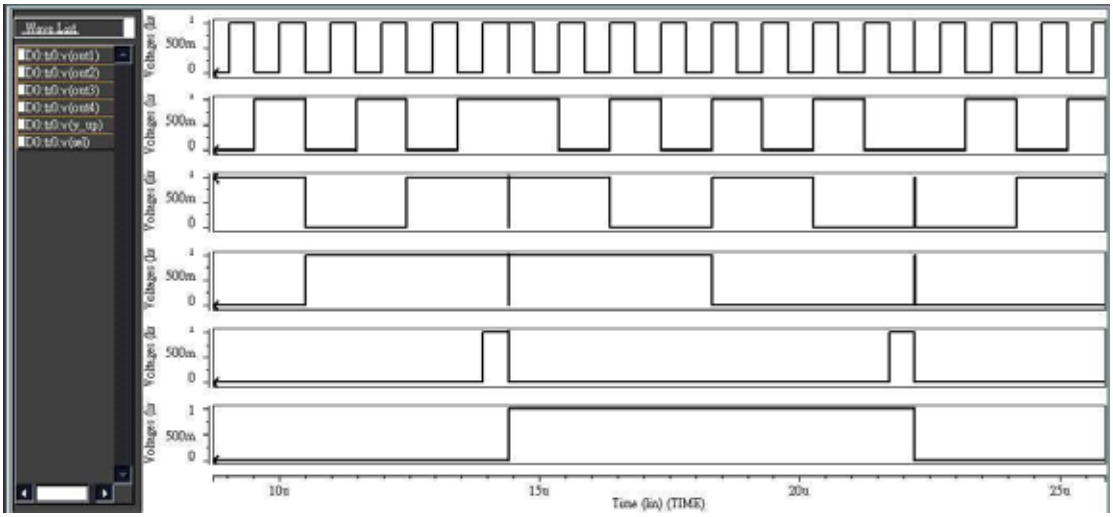


Fig. 5.34 Timing diagram of up/down counter

5.4.9 SSCG System

Fig. 5.35 shows the VCO control voltage of the spread spectrum clock. We can obviously find that the control voltage is similar to triangular wave.

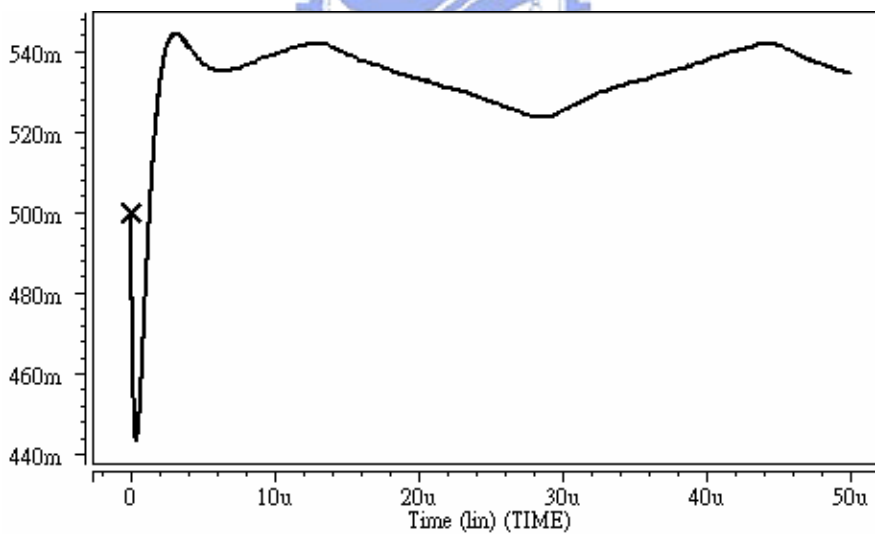


Fig. 5.35 transient response of the control voltage of the VCO

Fig. 5.36 shows the carrier spectra without spread spectrum. Fig. 5.37 is the carrier spectra with spread spectrum. The spectrum is spread over a wider bandwidth, and therefore reduces the peak amplitude. Here the reduction of carrier amplitude is about 14dB.

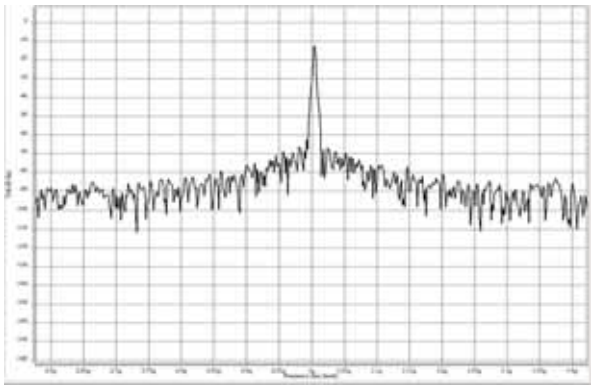


Fig. 5.36 Carrier Spectra without spread spectrum(-12dBV @ 3GHz)

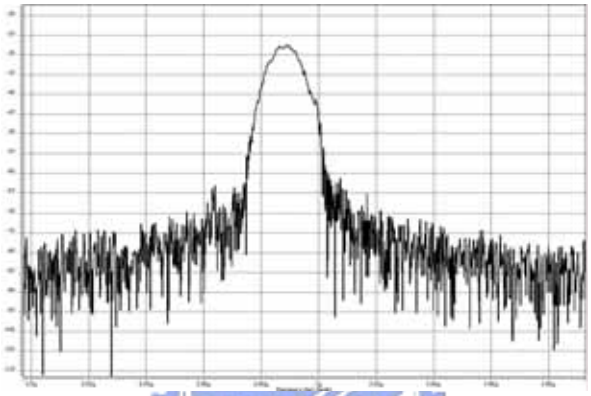


Fig. 5.37 Carrier Spectra with spread spectrum(-26dBV @ 3GHz)

The simulated performance of the proposed SSCG is summarized in Table 5.1.

Table 5.1 SSCG performance summaries

PLL Spec.	Operation frequency	3GHz
	Open-Loop Bandwidth	375KHz
	Kvco	300MHz/V
	Charge Pump Current	100uA
	VCO Frequency Range	2.82GHz ~3.3GHz
	Phase Margin	50º
SSCG Spec.	Spread Amount	-0.5%
	Modulation Frequency	30KHz
Power consumption		50mW
Supply Voltage		1V
Technology		TSMC 0.18 um 1P6M CMOS
Chip Area		1.1×1.08 mm^2

5.5 Experimental Results

The proposed spread spectrum clock generator has been integrated in a 0.18-μm 1P6M CMOS process. In this section, we introduce the testing environment and the experimental results of the chip. The loop filter is left off-chip to facilitate measurements. Fig. 5.38 shows the microphotograph of the SSCG. The total area of the chip is $1.1\times1.08\ mm^2$.

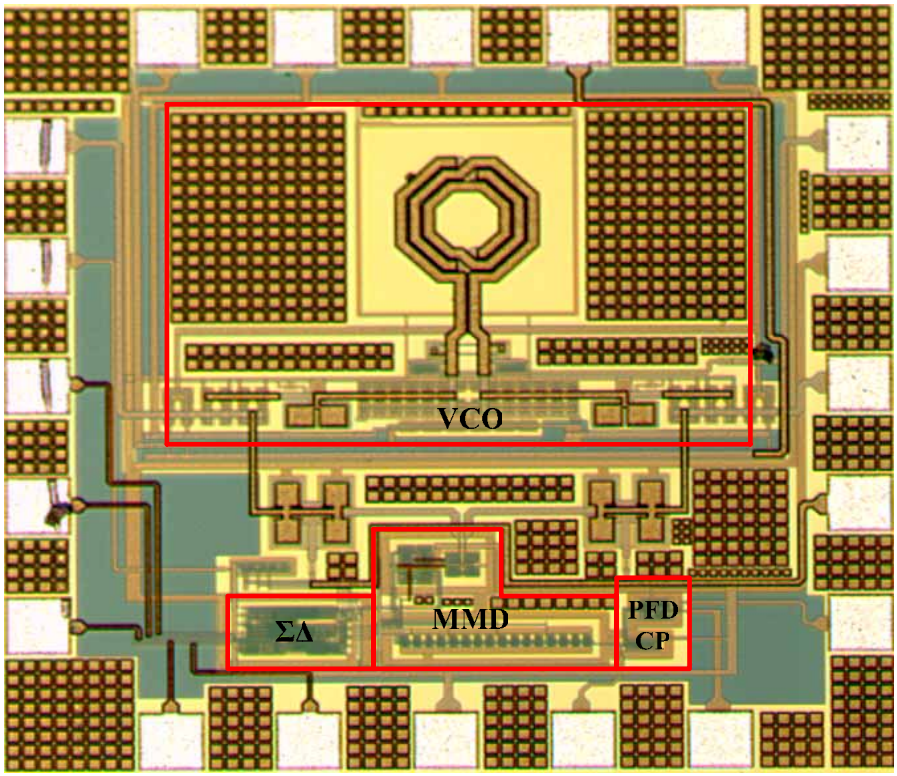


Fig. 5.38 Die microphotograph

5.5.1 Test Setup

Since the SSCG is a mixed-mode system, the powers and grounds of digital and analog parts should be separated. We can connect the ground of digital part and that of analog part with an inductor. This inductor can shot the DC voltage of their grounds, and avoid the high frequency noise coupling from digital part to analog

part.

The analog and digital powers are generated by a single commercial voltage regulator (LM317), because it generates more stable voltage than general power supply. The regulator only needs two resistors to set the output voltage. The output voltage can be predicted by equation (5.8)

$$V_{OUT} = 1.25\left(1 + R_1 / R_2\right) + I_{ADJ} \cdot R_2 \qquad (5.8)$$

The I_{ADJ} is the DC current that flows out of the ADJ terminal of the regulator. Besides, the capacitors C_1 and C_2 are the bypass capacitors.

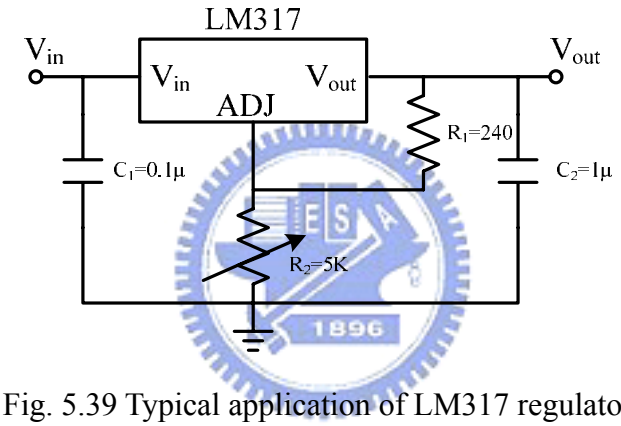


Fig. 5.39 Typical application of LM317 regulator

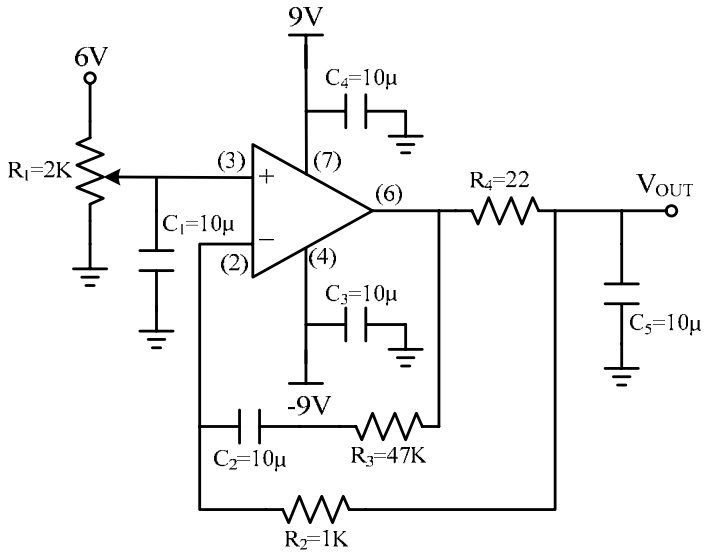


Fig. 5.40 Schematic of generation supply below 1.25V

However, the minimum output voltage of the regulator is about 1.25V. In our

chip, all the supply voltages are 1V, and the bias voltages are all below 1V. So we combine an adjustable low noise dc voltage source with OP27 operational amplifier, as shown in Fig. 5.40. The OP27 performs a unity gain amplifier with the input voltage set by the 2KΩ potentiometer [40].

The bypass filter network is combined by 10μF, 1μF, 0.1μ and 0.01μF capacitors, as shown in Fig. 5.41. The large capacitors can supply more charge than the smaller ones but have a lower self resonant frequency. Therefore, Fig. 5.41 provides decoupling of both low-frequency noise with large amplitudes and high-frequency noise with small amplitudes.

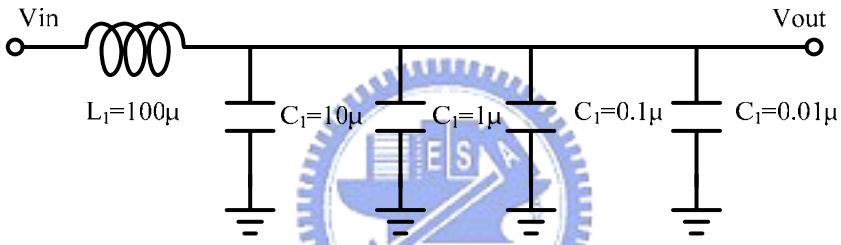


Fig. 5.41 Bypass filter at the regulator output

For impedance matching, a 50 Ω termination is employed. As shown in Fig. 5.42 (a), the width of PCB wire is also designed to be 50Ω impedance. We use SMA connectors with 50 Ω impedance cable (RG223/U) to deliver signals from PCB to oscilloscope or from generator to PCB. Fig. 5.42 (b) shows the regulator with LM317 and OP27.

The input clock of the SSCG and the counter clock are produced from the signal generator (Agilent 33250A). The output spectrum is observed by a Spectrum Analyzer (Agilent E4440A) and the time domain waveform of VCO is derived from the oscilloscope (Tektronix TDS6124C).

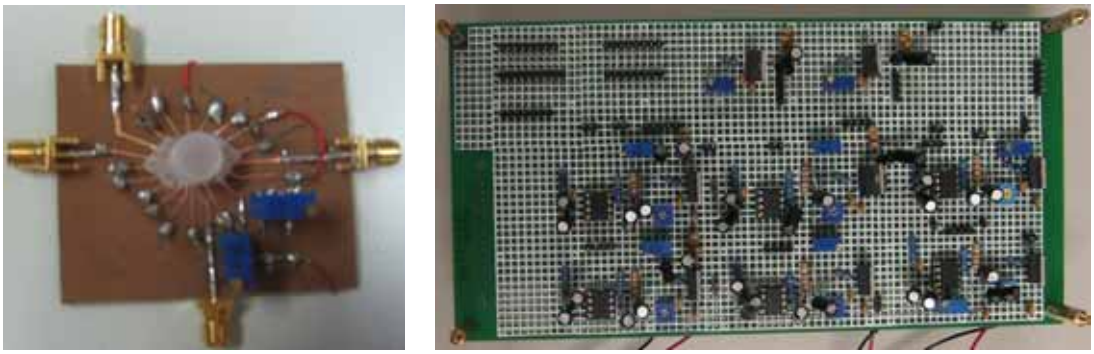


Fig. 5.42 Photograph of (a) PCB and (b) voltage regulator

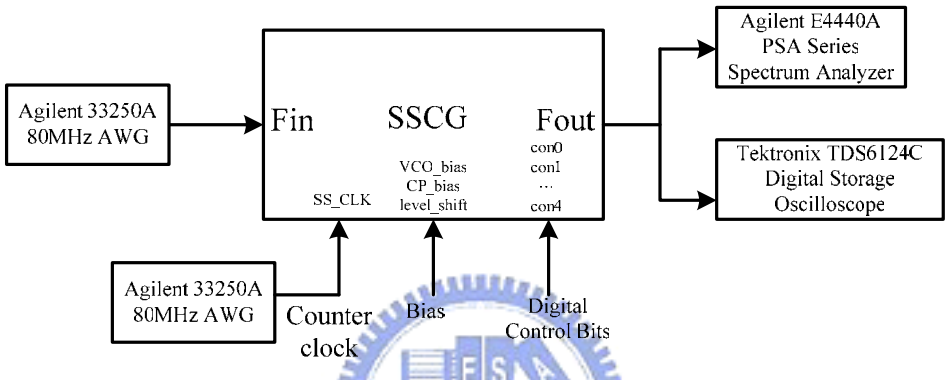


Fig. 5.43 Measurement setup of the SSCG

5.5.2 Measured Spectrum and Waveform

Fig. 5.44 and Fig. 5.45 show that the reduction of carrier amplitude is only about 0.5dBm at the carrier frequency (3GHz). However, the reduction of the reference spur amplitude is about 6dBm, as shown in Fig. 5.46 and Fig. 5.47. It is observed that when the frequency is higher, the reduction is much more. Fig. 5.48 shows the measured waveform of VCO is about 160mv. The measurement results are shown in Table 5.2.

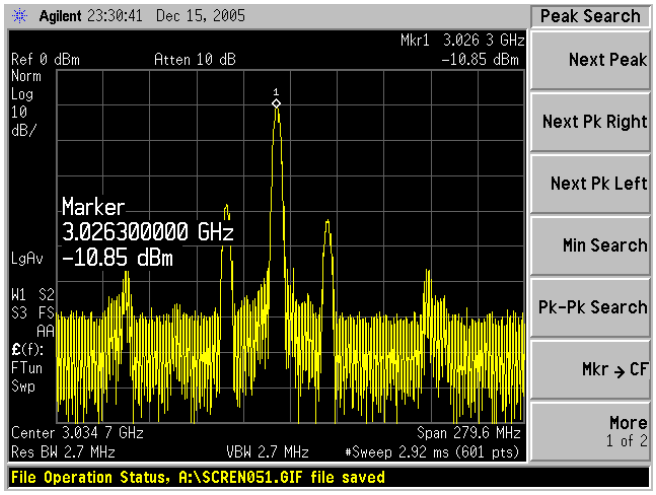


Fig. 5.44 Carrier Spectra without spread spectrum

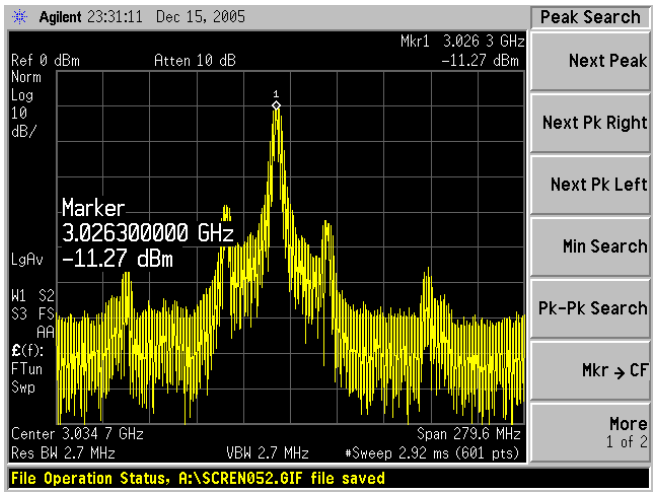


Fig. 5.45 Carrier Spectra with spread spectrum

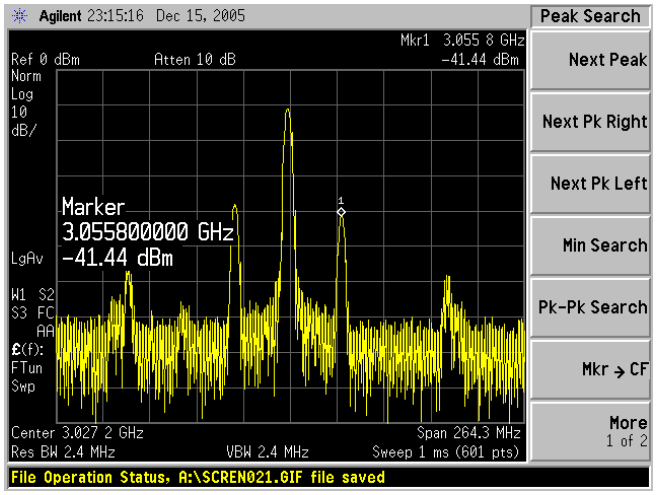


Fig. 5.46 Reference spurs Spectra without spread spectrum

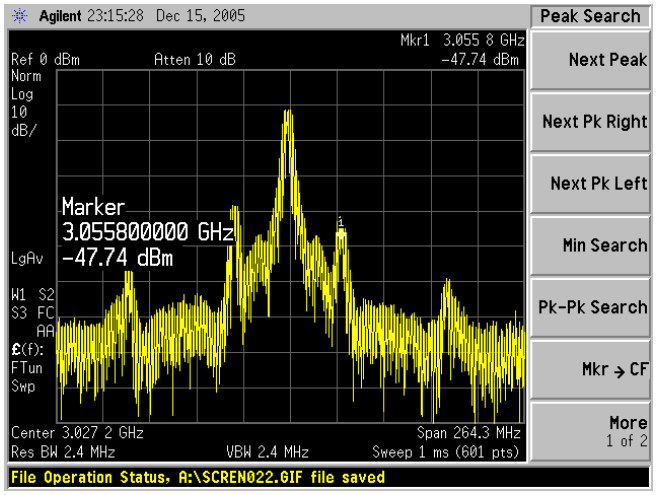


Fig. 5.47 Reference spurs Spectra with spread spectrum

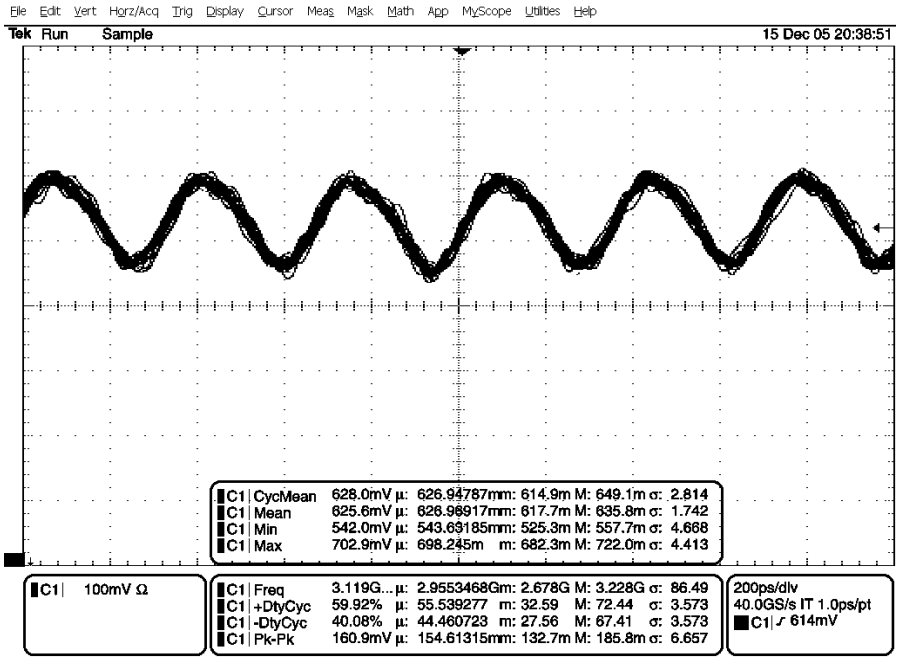
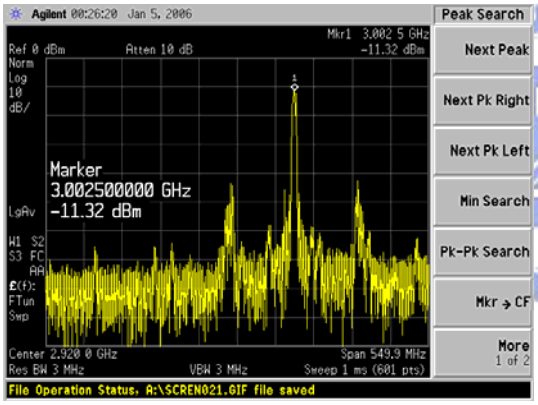


Fig. 5.48 Measure waveform of VCO

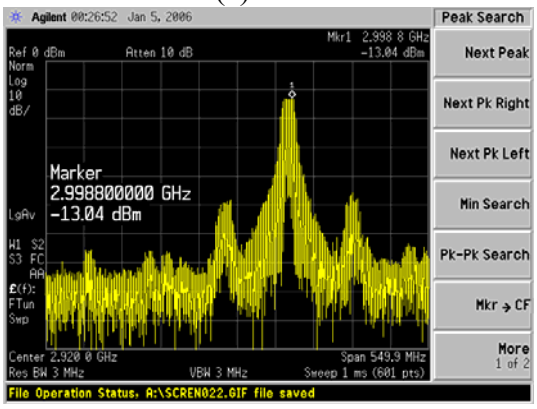
TABLE III. Measure results

Parameters	Unit	Performance
Frequency deviation	%	**0/-0.5**
EMI reduction (carrier)	dB	**0.5**
EMI reduction (reference spur)	dB	**6**

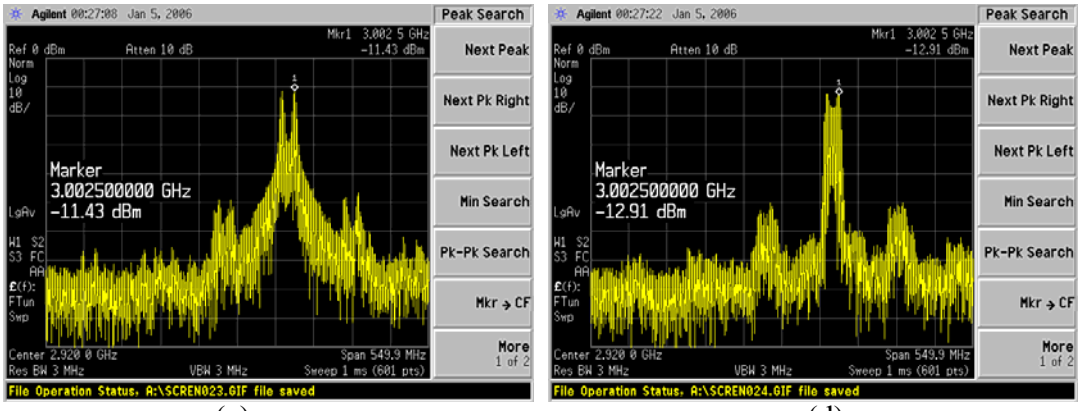
To get more insight into the spreading spectrum caused by the frequency-modulated, we directly connect the control voltage of VCO with the signal generator (Agilent 33250A). Fig. 5.49(a) is the carrier spectrum with a fixed control voltage. Fig. 5.49(b) is the carrier spectrum with triangular modulation. The peak attenuation is about 1.5dBm. Fig. 5.49(c) shows the carrier spectrum with rectangular modulation. It is obviously that the energy is concentrated at two sides and thus the effect is worse than the triangular modulation. The peak attenuation is only 0.1dBm. Fig. 5.49(d) is the sinusoidal modulation. The spreading spectrum effect is worse than the triangular modulation and better than rectangular modulation. The peak attenuation is about 1.6dBm.



(a)



(b)



(c) (d)

Fig. 5.49 Carrier Spectrum with (a) no modulation (b) triangular modulation (c) rectangular modulation (d) sinusoidal modulation

5.5.3Conclusion and Discussion

From the measurement, the amplitude reduction is not as we expect. The performance degradation probably comes from the process variation and un-perfect layout skill. Although the carrier doesn't decay so much, the phase noise of the carrier rise greatly after spreading spectrum. We guess that the phenomenon results from the improper function of the divider. Therefore, the divider modulus is not the same as we expect. Therefore, according to this experience, we should get more insight into the layout skill and process variation.

Chapter 6

Conclusions and Future Work

Electronic equipments often generate Electric-Magnetic Interference (EMI) that affects the operation of other equipments, like printers, CD-ROM drivers and LCD displays. The conventional techniques to reduce EMI tend to enclose or reduce the amount of the generated radiation, such as shield cables and coaxial wires, but are usually costly and bulky. Modern EMI reduction is done on-chip without using heavy shielding materials to the goal of low-cost and flexibility.

Altering the center frequency of internal clocks is a widely adopted EMI reduction technique. The technique is called Spread Spectrum Clocking (SSC) because the spectrum of the clock is spread over a broader range. It is also not sensitive to the process variation. Besides, because of the non-random and regular sequence of the divider modulus, the unwanted spur is obvious in the frequency spectrum of the clock. Therefore, in this thesis, we use a higher-order ΣΔ modulator to randomize the divider modulus and remove the spur to high frequency.

The application of CMOS PLL in low voltage and high frequency is crucial. With the reduction of the device feature size, a low supply voltage is a basic requirement. For System-On-a-Chip (SOC) design, it is significant for analog circuits to operate at the same low supply voltage as digital circuits. This thesis proposes a 1V CMOS SSCG for 2nd generation Serial ATA. The SSCG achieves

down spread 5000ppm from 3GHz while providing more than 14dB of power attenuation.

Chapter 2 begins with the brief introduction of the charge-pump PLL. The most significant part discusses the open loop transfer function as well as closed loop transfer function. Finally, we describe the phase noise of PLL using Leeson's Model to decide the optima bandwidth.

In Chapter 3, we describe the idea of fractional-N PLL. The most important part is the principles of ΣΔ modulators. We also derive its analytic function to prove the abilities of randomization and noise shaping.

Chapter 4 begins with the introduction to EMI problem and several solutions used for the EMI reduction. The most significant part explains the concept of spread spectrum using frequency modulation technology. Other properties, like modulation profile and modulation frequency and timing impacts, are also discussed.

In Chapter 5, a 1V 3GHz spread spectrum clock generator using fractional-N PLL for Serial ATA II is presented. The proposed circuit is fabricated in 0.18μm CMOS 1P6M process and the active area occupies 1.1 × 1.08 mm^2. Besides, the loop filter is designed off-chip in order to offer a variable bandwidth and get more accurate control on the spread amounts. The SSCG is fed with triangular modulation profile. Simulation shows at least 14dB of power attenuation while achieving down spread 5000ppm from 3GHz.

The low voltage spread spectrum clock generator proposed in this thesis is successfully achieved. To get more flexibility and lower power dissipation, more effort and considerations must be paid. How to operate in the higher frequency is also another challenge. Besides, how to reduce jitter while providing more attenuation is also an interesting topic.

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