國 立 交 通 大 學

電信工程學系

碩 士 論 文

10 位元 80 百萬赫茲導管式類比數位轉換器
和 CMOS 能階參考電路

10-Bit 80MHz Pipelined
Analog-to-Digital Converter and
CMOS Bandgap Reference Circuit

研究生：張 家 瑋

指導教授：洪 崇 智 教授

中 華 民 國 九十五 年 一 月

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研 究 生：張家瑋　　Student：Chia-Wei Chang

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摘要

高速類比數位轉換器是目前高效能系統，例如光纖通訊的前端接收器和資料通訊連結系統中不可獲缺的主要電路。高速類比數位轉換器在設計上，需要考慮如何將電路不匹配所造成的靜態(static)或動態(dynamic)的誤差如 DNL，INL 等誤差降低，以增加電路的解析度(resolutions)。此高速類比數位轉換器亦將採用低電壓操作，已達到低功率消耗的標準。在設計上如何將高速，高解析度和低功率消耗的優點集中在此類比數位轉換器，將是研究的重點之一。

一般而言，類比數位轉換器取樣頻率大於 1 GS/s 時，大多採用 Flash 架構的轉換器。當解析度每增加 1 位元(Bit)時，電晶體的數目將增加 4~8 倍，造成晶片面積和功率消耗增加，因此一般而言採用 Flash 架構的轉換器，其解析度普遍都不會大於 6 位元。為了提高轉換器的解析度，可採用導管式(Pipeline)架構的轉換器，此導管式轉換器主要是犧牲整體速度達到解析度的提升，因此可在速度、解析度和晶片面積之間取得最佳化。解析度 10 位元、取樣頻率 80 MS/s 的導管式類比數位轉換器(Pipelined ADC)將會在此研究中實現。

在此研究中，轉換器採用每一級 1.5 位元，串接八級，最後加上一級 2 位元的子轉換器，實現 10 位元的解析度。一個 10 位元每秒取樣 80 百萬次操作電壓 1.8 伏特的導管式類比數位轉換器，在晶片中心(CIC)提供的台積電(tsmc)標準 0.18 微米製程中被設計與實現。

論文中，低功率消耗的互補式金氧半能階參考電路(CMOS Bandgap Reference)，將以晶片中心(CIC)提供的台積電(tsmc)標準 0.18 微米製程設計與實現。此電路將電晶體偏壓在弱反轉層(weak-inversion region)，使其產生取代傳統雙載子(BJT)元件的電壓-電流關係式。此電路利用偏壓在弱反轉層電晶體閘源極(V_{GS})間的壓差，產生正溫度係數的電壓，再加上負溫度係數的電壓，藉此達到穩壓的效果。此電路以標準的CMOS製程實現，不需而外的製程輔助。

10-Bit 80MHz Pipelined Analog-to-Digital Converter and CMOS Bandgap Reference Circuit

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Abstract

High speed analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) are very significant blocks of nowadays high-performance systems such as data communication links using multilevel signaling (e.g., PAM and QAM). The main issues in the design of high-speed ADCs include static and dynamic offset reduction, low supply-voltage operation, gain, and speed optimization. Design tradeoffs between power, speed, and chip area further tighten the design requirements.

For analog to digital conversion at sampling rates above 1 GS/s, typically flash converters are used. The resolution of these converters is limited because each extra bit would require 4 to 8 times more gate areas resulting in excessive power consumption. Generally speaking, flash converters are practically limited to 6 bits of accuracy. For lower speed, alternative architectures are widely available, such as pipelined converters which enable higher resolution and higher efficiency. In this research, a 10-bit 80 MS/s pipelined ADC will be presented.

The converter uses the 1.5 bit/stage architecture that cascodes eight stages. A 2 bit flash sub-converter in the last stage is utilized to achieve the 10-bit resolution. A 10 bits、80 MS/s and 1.8 V Pipelined ADC was designed and implemented by tsmc 0.18um process supported by CIC.

Also, a low power CMOS Bandgap Reference Circuit was designed and implemented by tsmc 0.18um process supported by CIC. The BJTs are replaced by the MOSFETs which operate in the weak-inversion region because the MOSFETs operating in the weak-inversion region have similar voltage-current relationship to the BJTs. The bandgap reference circuit uses the different V_{GS} voltage between two MOSFETs operated in weak-inversion region to generate the voltage of positive temperature coefficient. We could get the stable reference voltage by combine the voltage of positive temperature coefficient with voltage of negative temperature coefficient. This circuit was designed in standard CMOS process without any other process.

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Chapter 1

Introduction

1.1 Motivation

In the last few years, there is a tendency to move the signal processing functions from the analog domain to the digital domain. Because circuits in the digital domain have some advantages, such as a high level accuracy, saving power consumptions and silicon areas, and programmability of functions. In the nature, signals transmit almost in the analog way, thus a conversion between analog and digital is needed at the interface. In mixed-mode analog-to-digital interfaces, there are many applications such as video-image systems, DVD players, portable personal communication devices, mobile phones, camcorders, and etc. With the growth of wireless communication systems and portable devices, low power consumption and longer battery-lifetime have become a major problem. Therefore minimum power dissipation in integrated circuits is necessary with limited energy of batteries.

A pipelined A/D converter is inherently a multi-step-quantification architecture in which the digitization is performed by a cascade of many identical stages of low-resolution analog-to-digital converters. Pipelining enables high conversion throughput by inserting sample-and-hold amplifiers (SHAs) between stages that allow a concurrent operation of all stages. In analog-to-digital converters, Pipeline ADC architecture becomes more and more attractive because it can offer the best performance in terms of low power, high speed and small area.

In this research, the 85mW, 10-bit, 80MS/s pipelined A/D converter with the 1.8V supply voltage has been designed and implemented with the standard TSMC 0.18μm CMOS 1P6M process. By the way, no special process or multiplied voltage is needed in this research.

Expect for pipelined ADC, we propose a low power CMOS bandgap reference circuit. This bandgap reference circuit is designed by using MOSFETs operated in weak-inversion region instead of BJTs to reduce power consumption. Basically the bandgap reference circuit could provide stable reference voltages and bias voltages to our pipelined ADC. The relationship of bandgap reference circuit and pipelined ADC is shown in Figure 1.1.

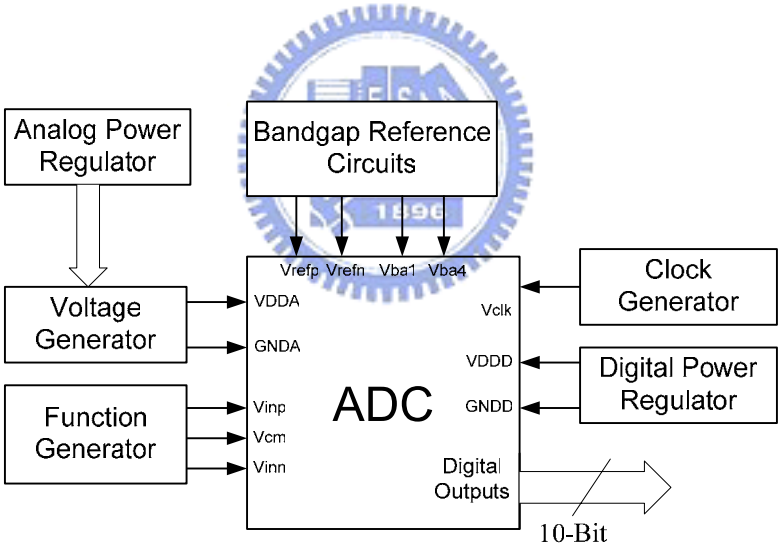


Figure 1.1 The relationship of bandgap reference circuit and pipelined ADC

1.2 Thesis Organization

This thesis is organized into six chapters.

In Chapter 1, this thesis is briefly introduced.

Chapter 2 describes the concepts of analog-to-digital conversion and performance parameters used to characterize ADCs. Then, several ADC architectures are introduced and the evolution of the pipelined ADC is presented. Then, the digital error correction technique and the 1.5-bit architecture are described. Finally, the timing of the pipelined ADC is analyzed.

Chapter 3 describes the key circuit blocks used in pipelined ADC. Among them are the operational amplifier, the common mode feedback, the comparator, the bootstrapped switch, the sample-and-hold amplifier (SHA), the 1.5-bit architecture, and the 2-bit flash converter. Then, the transistor level simulated results of each circuit are presented. Finally, the simulation of the whole pipelined ADC and its layout and floor plan are presented.

Chapter 4 presents the testing environment, including the component circuits on the DUT (device under test) board and the instruments. Then, the pipelined ADC described in Chapter 3 is fabricated in a standard TSMC 0.18μm CMOS Mixed-Signal process and the measured results of this chip are summarized.

Chapter 5 described the principle of the new low-power CMOS bandgap reference circuit. Finally, the simulated results of this CMOS bandgap reference circuit are presented with the standard TSMC 0.18μm CMOS Mixed-Signal process.

Finally, the conclusions of this thesis are summarized in Chapter 6.

Chapter 2

General Design Consideration in Pipelined A/D Converters

2.1 Introduction

Many practical integrated circuit realizations of pipelined A/D converters have been successfully implemented over past decade. This Chapter first presents the main performance parameters used to access the static and dynamic behaviors of Nyquist A/D converters and then introduces some of the prominent ADC architectures.

2.2 Performance Parameters In Nyquist A/D Converters

In conventional Nyquist A/D converter the accuracy can be defined by comparing every input sample and the corresponding output sample. Figure 2.1 illustrates the ideal conversion characteristic of a 3-bit ADC. The transition voltage can be written as

$$V_{tn} = \frac{V_{ref}}{2^N} \cdot n, \quad n \in \{0,1,2,...,2^N - 1\}, \tag{2.1}$$

where N and V_{ref} represent the bit numbers and the applied reference voltage respectively. The quantization step (V_{LSB}) is the difference of two transition voltages and it can be written as

$$V_{LSB} = \frac{V_{ref}}{2^N}. \tag{2.2}$$

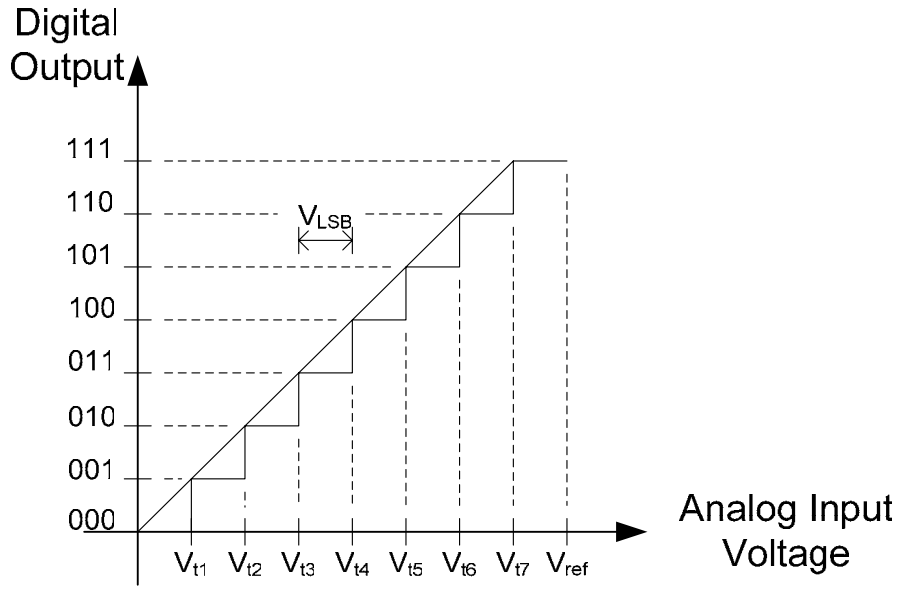


Figure 2.1 Ideal conversion characteristic of a 3-bit ADC

2.2.1 Offset and Gain Error

The error of an A/D converter is the difference between the theoretical and the actual input voltage required to produce a particular output code. In most applications the user can calibrate the offset and gain errors by subtracting the offset and dividing by the gain.

Offset error is the difference between the theoretical transition voltage and the actual transition voltage relatively to the quantization step. Gain error indicates the slope difference between the lines connecting the theoretical and actual transitions of the full scale extremes.

Figure 2.2 illustrates Offset and Gain Error. [01]

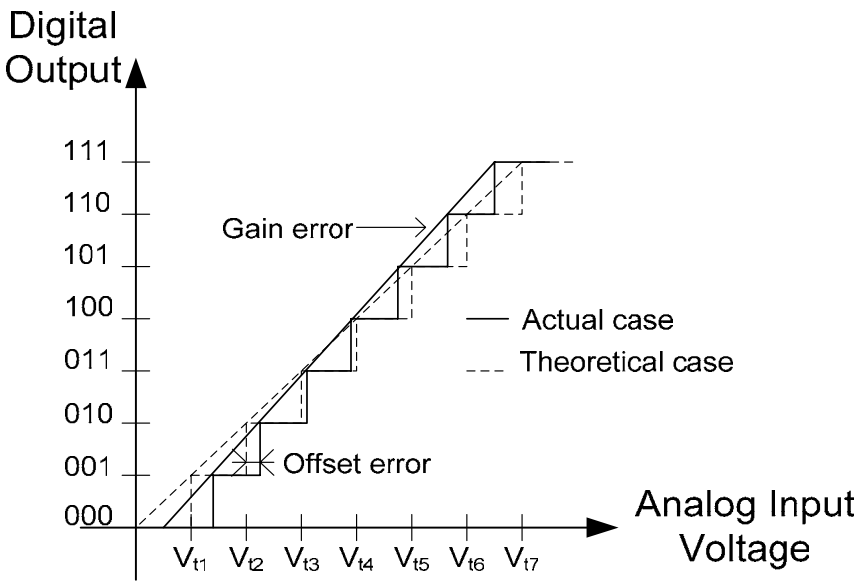


Figure 2.2 Illustrates Offset and Gain Error

2.2.2 Differential Non-Linearity Error (DNL)

DNL error is defined as the difference between an actual step width and the ideal voltage of 1LSB ($1LSB = \frac{V_{ref}}{2^N}$). For an ideal ADC, in which the differential nonlinearity coincides with DNL = 0LSB, each analog step equals 1LSB and the transition voltages are spaced exactly 1LSB apart. A DNL error specification of less than or equal to 1LSB guarantees a monotonic transfer function with no missing codes. DNL is specified after the static gain error has been removed. It is defined as follows:

$$DNL(n) = \frac{V_{t(n+1),actual} - V_{t(n),actual}}{1LSB} - 1 . \qquad (2.3)$$

If the maximum DNL error is larger than -1 LSB at N-bit level, it is guaranteed that the ADC is monotonic, which means that the digital output always increases or is kept constant as the input increases. [01] [02]

2.2.3 Integral Non-Linearity Error (INL)

INL error is defined as the deviation of each transition voltage of each code from the ideal transition voltage. INL is the difference between the actual finite resolution characteristic and the ideal finite resolution characteristic. INL is also specified after the static gain error has been removed. It is defined as follows:

$$INL(n) = \frac{V_{t(n),actual} - V_{t(n),ideal}}{1LSB}. \quad (2.4)$$

Figure 2.3 displays examples of DNL and INL errors for different codes. [01] [02]

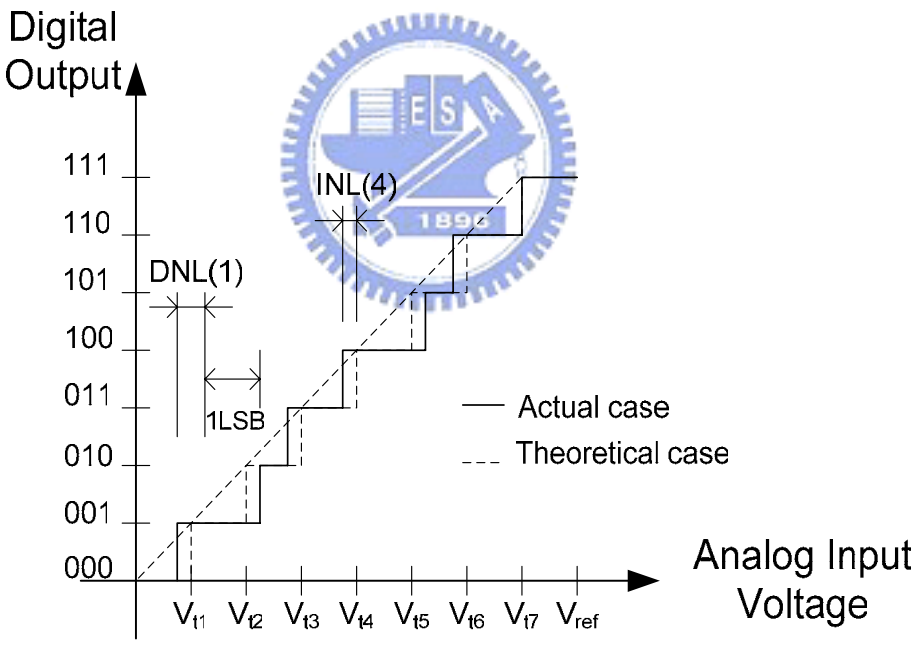


Figure 2.3 Example of DNL and INL errors in a 3-bit ADC

2.2.4 Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio of the signal power to noise power at

the ADC's output. It is well known that the theoretical SNR for an N-bit ADC is given by

$$SNR = 6.02 \cdot N + 1.76 \quad dB. \tag{2.5}$$

2.2.5 Spurious Free Dynamic Range (SFDR)

The spurious free dynamic range is defined as the ratio of rms amplitude of the fundamental (the maximum signal amplitude) to the rms value of the largest distortion component in a specified frequency range. SFDR is important because noise and harmonics restrict converters' dynamic range.

2.2.6 Signal-to-Noise and Distortion Ratio (SNDR)

For sinusoidal input signals, the signal to noise and distortion ratio is defined as the ratio of the signal power (maximum amplitude of the signal component) to the noise and harmonic distortion power at the ADC's output.

2.2.7 Effective Number of Bits (ENOB)

For actual ADCs, a specification often used in place of the SNR or SNDR is ENOB, which is a global indication of ADC accuracy at a specific input frequency and sampling rate. ENOB can be defined as follows:

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad bits. \tag{2.6}$$

2.3 Review of ADC Architectures

Analog-to-digital conversion can be separated into two distinct operations: sampling and quantization. Sampling transforms a continuous time signal into a corresponding discrete time signal. Quantization converts the continuous amplitude distribution into a set of discrete levels, which can be expressed with digital codes. Figure 2.4 illustrates the principle of A/D conversion.

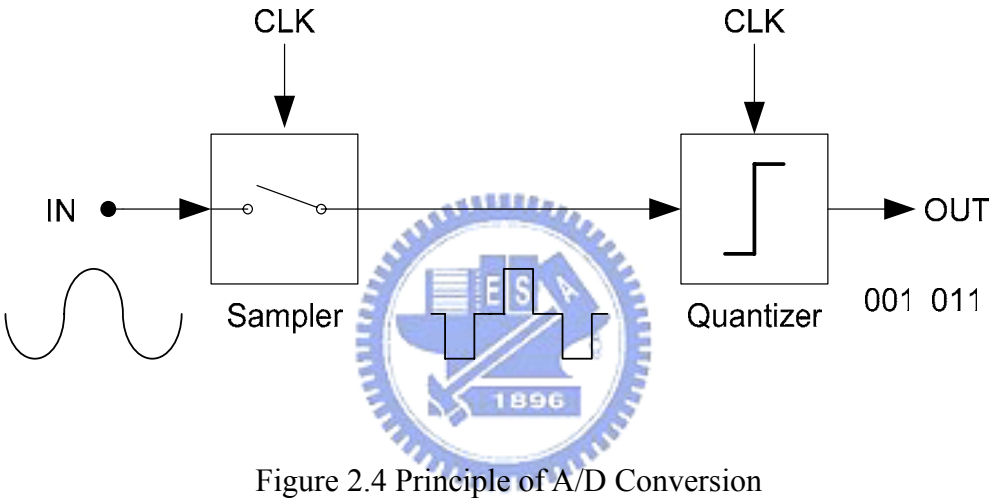


Figure 2.4 Principle of A/D Conversion

Some A/D converter architectures, such as flash converter, can perform sampling and quantization simultaneously. In high performance ADCs, sampling and quantization are usually separated to make it possible to optimize the circuitry for both tasks without compromises. [02] [03]

2.3.1 Flash ADC

Flash ADC which is the fastest and one of the simplest ADC architecture is shown in Figure 2.5. It consists of 2^N-1 comparators and performs 2^N-1 level quantization.

The reference voltages of the comparators are generated by using a resistor ladder which is connected between the positive and the negative reference voltage: +Vref and –Vref respectively. The set of 2^N-1 comparator outputs is often referred to as thermometer code and is converted to N-bit binary word with a logic circuit. The input signal of the flash ADC is directly connected to the inputs of the comparators thus the speed of the flash ADC is very fast and the speed is only limited by the speed of the comparators. Therefore the flash ADC is capable of high speed.

The drawback of the flash ADC is the fact that the number of the comparators grows exponentially with the number of bits. As the number of comparators increases the chip area and power consumption will also increase. Therefore the flash ADC is not suitable for high resolution application; typical resolutions are seven bits or below. Another drawback of the flash ADC is that the converter is sensitivity to comparator offset however the offset voltage can be solved by using auto-zeroing comparators.

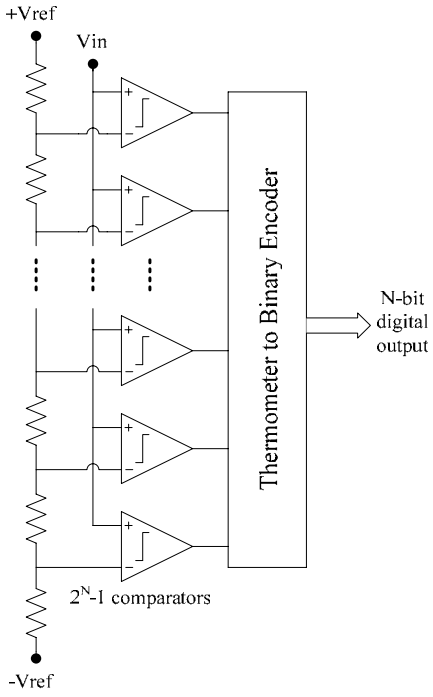


Figure 2.5 N-bit Flash ADC

2.3.2 Two-Step ADC (or Subranging ADC)

One way to reduce the number of comparators in flash ADC is to perform the quantization in two steps [04]. Therefore, the number of comparators can be reduced form 2^N-1 to $2\times2^{N/2}$. The block diagram of this two-step converter is shown in Figure 2.6. The operation of this converter is described as follows. The fine flash ADC determines the most significant bits then these bits are converted back to an analog signal through the DAC to be subtracted from the input signal. This residual signal is then sent to the coarse flash ADC to determine the least significant bits.

The two-step converter has a longer latency delay than the flash converter but it can allow for higher resolutions than the flash converter because of reducing the number of comparators.

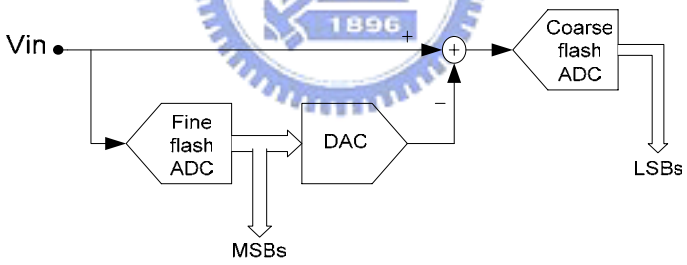


Figure 2.6 Two-step ADC

2.3.3 Pipelined ADC

The block diagram of the pipelined ADC is shown in Figure 2.7. It consists of a cascade of M identical stages in which each stage produce k bits and the last pipelined stage is followed by a flash ADC providing p bits. As a result, the final resolution N is M×k+p.

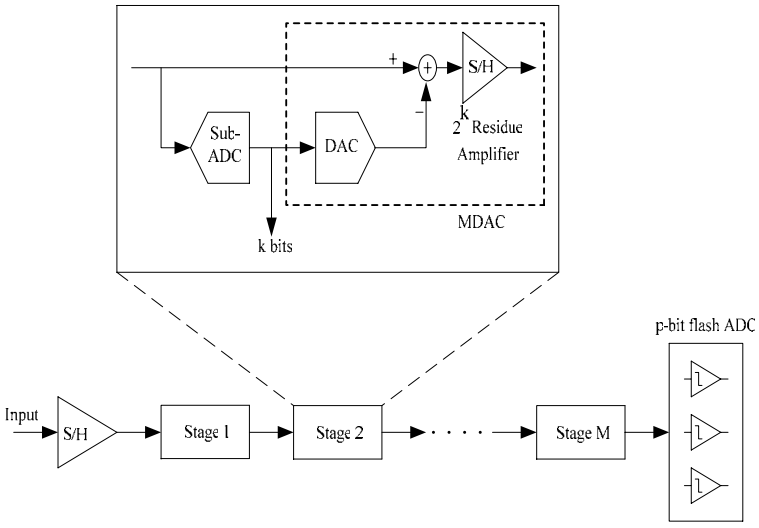


Figure 2.7 m-bit/stage pipelined ADC

A function block diagram of one stage is shown in the inset of Figure 2.7. The incoming voltage is sampled by the S/H circuit and simultaneously digitized by the sub-ADC. The output signals of the sub-ADC are then converted back to analog forms and will be subtracted form the output signals of the S/H circuit. The resulting residue voltage is amplified by 2^k. The S/H circuit, the D/A converter, the subtraction, and the amplification are all performed by a single circuit block which called multiplying analog-to-digital converter (MDAC). The MDAC circuit consists of an opamp and a set of switched capacitors. The sub-ADC is usually performed in fresh architecture and consists of a few comparators and logic gates.

When the input signal is a rapidly-changing signal, the relative timing of the first stage S/H circuit and the sub-ADC is critical but it can be relaxed with a front-end circuit. If the input signal is not a rapidly-changing signal a front-end S/H circuit is not needed, since the pipelined stage already contains an S/H circuit. [05]

2.3.4 Cyclic ADC

A cyclic ADC consisted of a single pipeline stage with the output fed back to the input is shown in Figure 2.8. The operation of a cyclic ADC is the same as a pipelined ADC except that one stage does all the processing. The cyclic ADC completes N bits by reusing the stage multiple times thus it uses very little chip area and dissipates very low power. [06]

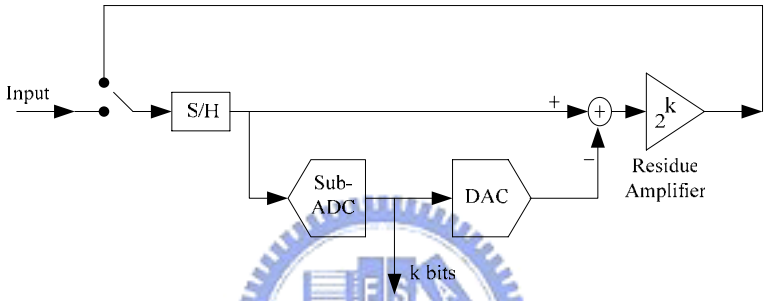


Figure 2.8 Cyclic ADC

2.3.5 Time-Interleaved ADC

Figure 2.9 shows the block diagram of an architecture in which four ADCs are used on parallel to achieve four times the sampling rate of a single converter. This method is often known as time-interleaved architecture [07]. The sample-and-hold circuits consecutively sample and apply the input analog signal to their respective ADCs. The digital outputs of the channels are combined with a multiplexer to a single bit-stream. [02]

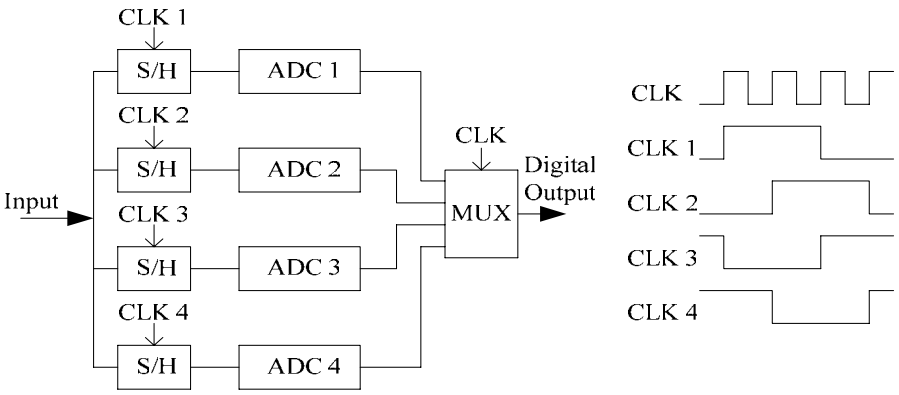
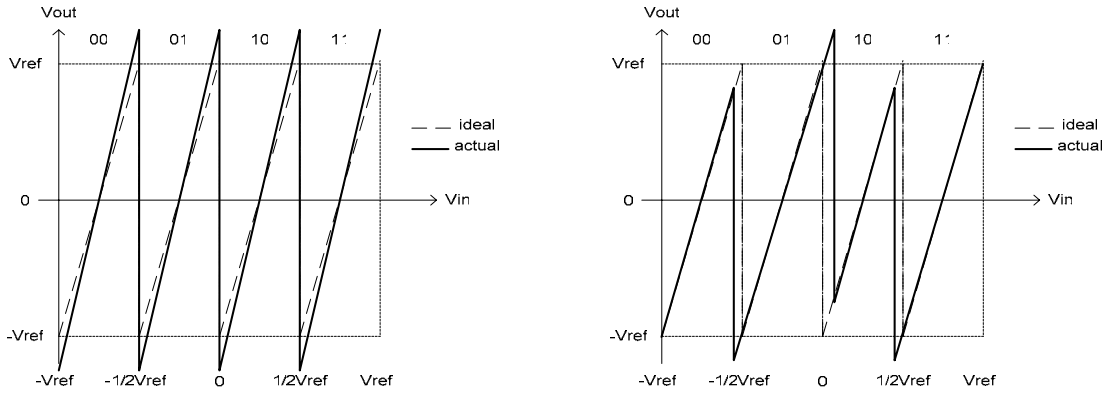


Figure 2.9 Four-channel time-interleaved ADC and its clock signals

2.4 Digital Error Correction Technique

In the pipelined ADC, the input signal range is the same with the output signal range for each stage. This is done by the gain amplifier which amplifies the residue subtracted from the input signal. The amplified residue must still within the conversion range for the next stage. If there is a deviation such as the amplified residue exceeds the conversion range of the next stage, it may have wrong codes. As illustrated in Figure 2.10, the gain error and comparator offset may lead to over conversion range problems. Digital error correction is the name of the calibration technique that reduces the gain error, keeps the conversion range constant with modified coding and tolerates greater comparator offset.

For example, in a 2-bit pipelined stage there is only a contribution of less than two bits to final output word of the A/D converter and the residue amplification gain used is usually smaller than 4. This will keep the residue within certain boundaries and therefore the extra redundancy can be used to correct in the digital domain the referred non-ideal effects in the Flash Quantizers. Figure 2.11 shows the modified coding transfer curve with digital error correction.



(a) Gain error (b) Comparator offset

Figure 2.10 Residue amplification characteristic of a 2-bit/stage with

(a) Gain error (b) Comparator offset

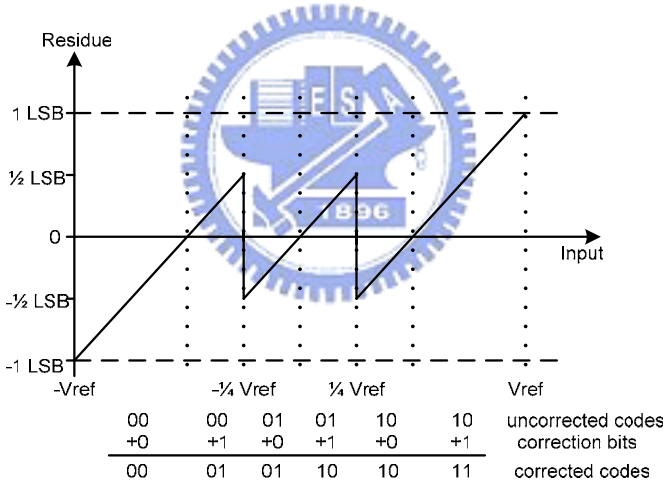


Figure 2.11 Analog residue with digital error correction

In the digital domain the correction is a simple addition, as illustrated in Figure 2.12. On the left is shown how the bits of the final result are obtained by summing the output bits of the stages with one-bit overlap. On the right the same bits are rearranged to show how the correction can be performed with a single adder. [05] [08]

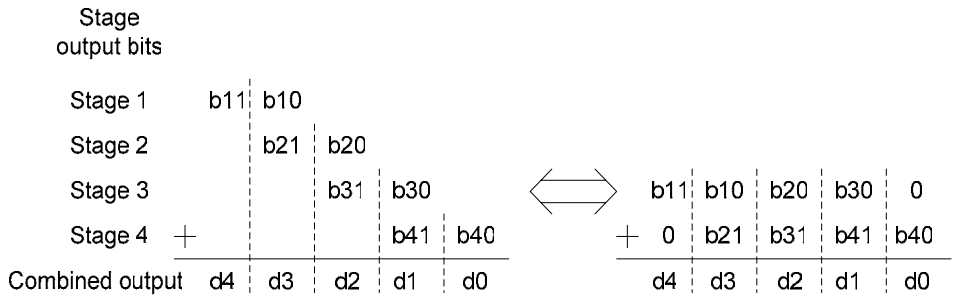


Figure 2.12 RSD correction in digital domain

2.5 1.5-Bit / Stage Architecture

The pipelined ADC uses a pipelined 1.5-bit/stage architecture with 9 stages as shown in Figure 2.13. Each stage resolves 2 bits with a sub-ADC, and subtracts this value form its input and amplifies the resulting residue by a gain of two. The input signal range of the pipelined ADC is from –Vref to +Vref. In the 1.5-bit/stage, we set the threshold voltages of the sub-ADC at –Vref/4 and +Vref/4, therefore the residue transfer function is given as follows

$$V_{out} = \begin{cases} 2V_{in} + V_{ref}, if\ -V_{ref} < V_{in} < \dfrac{-V_{ref}}{4} \Leftrightarrow D = (00)_2 \\ 2V_{in}\quad\quad , if\ \dfrac{-V_{ref}}{4} < V_{in} < \dfrac{+V_{ref}}{4} \Leftrightarrow D = (01)_2 \\ 2V_{in} - V_{ref}, if\ \dfrac{+V_{ref}}{4} < V_{in} < +V_{ref} \Leftrightarrow D = (10)_2 \end{cases} \quad (2.7)$$

where D is the binary output code for each stage. The transfer function of 1.5-bit/stage is shown in Figure 2.11. Because of using the digital error correction technology, the 1.5-bit/stage has lower (2 instead of 4) inter-stage gain than the 2-bit/stage, but it requires more stages (9 stages instead of 5 stages for 10bits ADC) than the 2-bit/stage. By reducing the inter-stage gain, the accuracy requirements on the sub-ADCs are

greatly reduced. In this research, a maximum offset voltage of Vref/4 can be tolerated before the bit errors occur.

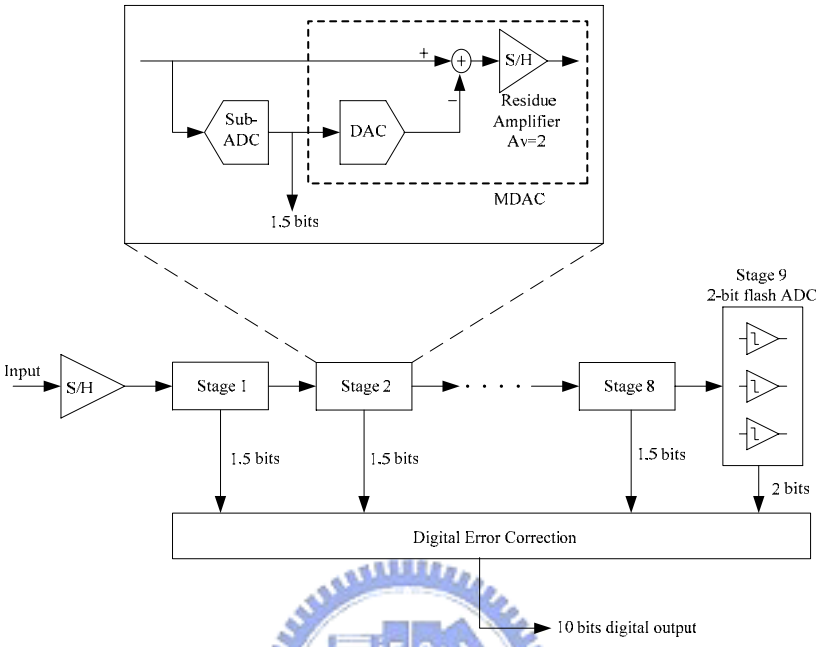


Figure 2.13 Pipelined ADC with 1.5-bit/stage architecture

The number of bits per stage has a serious impact on the power, speed, and accuracy requirements of each stage. Therefore, the best choice of bit/stage is decided on the overall ADC specifications. For example, for fewer numbers of bits per stage, the comparator requirement is more relaxed, and the inherent speed of each stage is faster. The higher speed gain is because the inter-stage gain is lower allowing higher speed due to the fundamental gain bandwidth tradeoff of amplifiers. If fewer bits per stage are used, more stages are required. Therefore, the noise and gain errors of the later stages would make more inaccuracy to the overall converter because of the low inter-stage gain. Thus, low speed, high resolution specifications tend to favor higher number of bits per stage, where high speed, low resolution specifications favor a lower number of bits per stage.

This 1.5-bit/stage architecture has been shown to be effective in achieving high throughput at low power consumption. The low number of bits per stage combined with digital error correction technology relaxes the limits on the comparator offset voltage and DC gain of op-amp. [08]

2.6 Timing Analysis of The Pipelined ADC

The operation of the pipelined ADC is best understood with a timing diagram. Figure 2.14 illustrates the timing of the pipelined ADC. The 1.5-bit sub-ADC in each stage is composed of two comparators and performs comparison to get digital output of A/D converter, and then the digital outputs of the 1.5-bit sub-ADC are delivered into registers to store. The register number in stage 1 is 9 and decreases in turn in the following stages. The register array is shown in Figure 2.15.

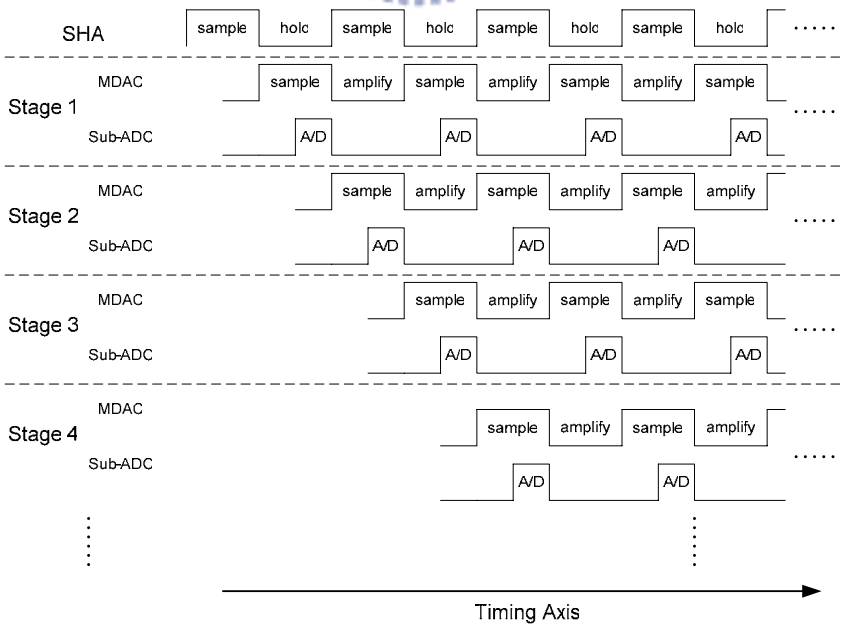


Figure 2.14 Timing diagram of the pipelined ADC

Figure 2.15 Register array of the pipelined ADC

In Figure 2.15, ø1 and ø2 are two non-overlapping signals, and by passing register array, digital outputs from 9 stages can enter digital error correction block concurrently. The ten registers after digital error correction block make 10 digital outputs come out at the same time.

Chapter 3

Design of Pipelined Analog-to-Digital Converter

3.1 Introduction

Traditional designs of high-speed CMOS analog-to-digital converters have used flash architectures. While flash architectures usually yield the highest throughput rate, they trend to require large silicon area because of the large numbers of comparators required. An important purpose is that the realization of high-speed ADC in smaller area than that required in flash converters so that the A/D interface function can be integrated on the same chip with associated image-processing functions. Multistage conversion architectures reduce the area by reducing the number of comparators. Using a pipelined architecture allows the stages to operate concurrently and produces the maximum throughput rate. Also, digital error correction technology significantly reduces the sensitivity of the architecture to certain component non-idealities.

The pipelined ADC architecture has been adopted into many high-speed applications such as high-performance digital communication systems and high-quality video systems. The rapid growth in these applications is driven the design of ADCs toward higher sampling rate, lower power consumption, and smaller chip area. The continued scaling of submicron CMOS technology couples with lower power supply voltage. This trend gives a challenge to conventional pipelined ADC designs which rely on high-gain and large-bandwidth operational amplifiers (op-amp)

to produce high-accuracy and high-speed data converters. At low power supply voltage, large open-loop operational amplifier gain is difficult to realize without sacrificing bandwidth or power consumption. As a result, the finite operational amplifier gain is becoming a major problem in achieving both high speed and high accuracy. One way to get a high op-amp gain is usually realized by multistage op-amp structure, gain-boosting technique, and long channel devices.

3.2 Operational Amplifier

Speed and accuracy are two of the most important properties of analog circuits, however optimizing circuits for both aspects lead to contradictory demands. In a wide variety of CMOS analog circuits such as switched-capacitor (SC) circuits, sample-and-hold amplifiers, and pipelined ADC, speed and accuracy are determined by the settling behavior of operational amplifiers. Fast settling requires a high unity-gain frequency, whereas accurate settling requires a high dc gain.

The realization of a CMOS operational amplifier that combines high dc gain with high unity-gain frequency has been a difficult problem. The high-gain requirement leads to multistage designs with long-channel devices, whereas the high unity-gain frequency requirement needs a single-stage design with short-channel devices. One way to overcome this problem is using the cascoding technique. Cascoding technique can enhance the dc gain of an op-amp without degrading the high frequency performance. The dc gain of the op-amp is proportional to the square of the intrinsic MOS transistor gain $g_m \times r_o$.

The op-amp used in this pipelined ADC is made in the fully-differential

architecture. The advantages of the fully-differential circuit are that it can reduce even-order harmonic distortion, substrate noise, and common-mode disturbances. It also improves the power supply rejection ratio (PSRR) and the common-mode rejection ratio (CMRR). One drawback in the fully-differential circuit is that it needs the common-mode feedback circuit and it will be illustrated in the following sections.

3.2.1 Folded Cascode Operational Amplifier

The op-amp is the most important element in every stage of the pipelined ADC. If we increase the frequency bandwidth of the op-amp, the converting speed of the pipelined ADC can be increased. However, if we increase the dc gain of the op-amp, the resolutions of the pipelined ADC can be increased. In this project, the operational amplifier is made in folded cascode architecture. The folded cascode op-amp is shown in Figure 3.1. However, the dc gain of the folded cascode op-amp is limited by the short-channel devices and the effective gate-driving voltage. For this reason, it is necessary to use the op-amp open-loop gain enhancement technique to increase the dc gain of the op-amp. This method is called gain-boosting, and the theory will be illustrated as follows.

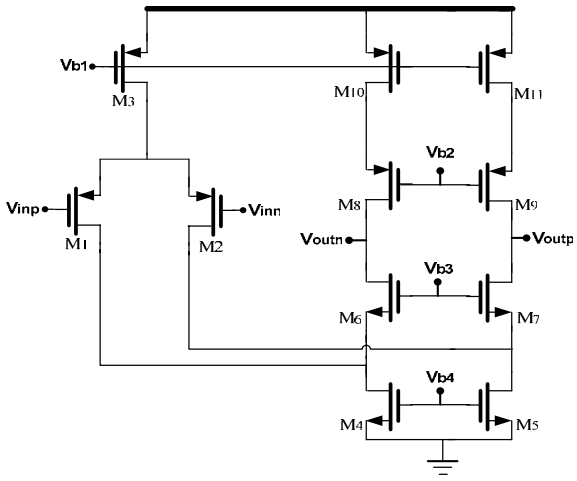


Figure 3.1 Fully-differential folded cascode op-amp

The dc gain of the fully-differential folded cascode op-amp of Figure 3.1 can be written as

$$|A_v| = G_m \times R_{out} . \tag{3.1}$$

The output impedance R_{out} is expressed as $R_{out} = R_{op} \| R_{on}$. Where R_{op} can be written to $R_{op} \approx (g_{m9} + g_{mb9}) r_{o11} r_{o9}$, and R_{on} can be written to $R_{on} \approx (g_{m7} + g_{mb7}) r_{o7} (r_{o2} \| r_{o5})$. Thus the output impedance R_{out} is shown as

$$R_{out} = \left[(g_{m9} + g_{mb9}) r_{o11} r_{o9} \right] \| \left[(g_{m7} + g_{mb7}) r_{o7} (r_{o2} \| r_{o5}) \right]. \tag{3.2}$$

The transconductance G_m is approximately equal to g_{m2}. Substituting equation (3.2) into equation (3.1), we obtain

$$|A_v| = g_{m2} \left\{ \left[(g_{m9} + g_{mb9}) r_{o11} r_{o9} \right] \| \left[(g_{m7} + g_{mb7}) r_{o7} (r_{o2} \| r_{o5}) \right] \right\}. \tag{3.3}$$

Op-amps used in feedback circuits indicate a large signal behavior called "slewing". The slewing behavior of the folded cascode op-amp is shown in Figure 3.2. Figure 3.2(a) and (b) illustrate the equivalent circuit for positive and negative step inputs respectively. The NMOS current sources supply currents of I_n, however the current that discharges or charges the load capacitor C_L is equal to I_{SS}. So the slew rate of the folded cascode op-amp can be expressed as $\pm I_{SS}/C_L$. Note that the slew rate is independent of I_n if $I_n > I_{SS}$.

In Figure 3.2(b), if $I_{SS} > I_n$ and the op-amp is slewing, M_7 turns off such that M_1 and the tail current source will enter the liner region. After M_2 turns on, the circuit returns to the equilibrium state, at the same time the drain voltage of M_5 will experience a large swing and this phenomenon will slow down the settling behavior. [10]

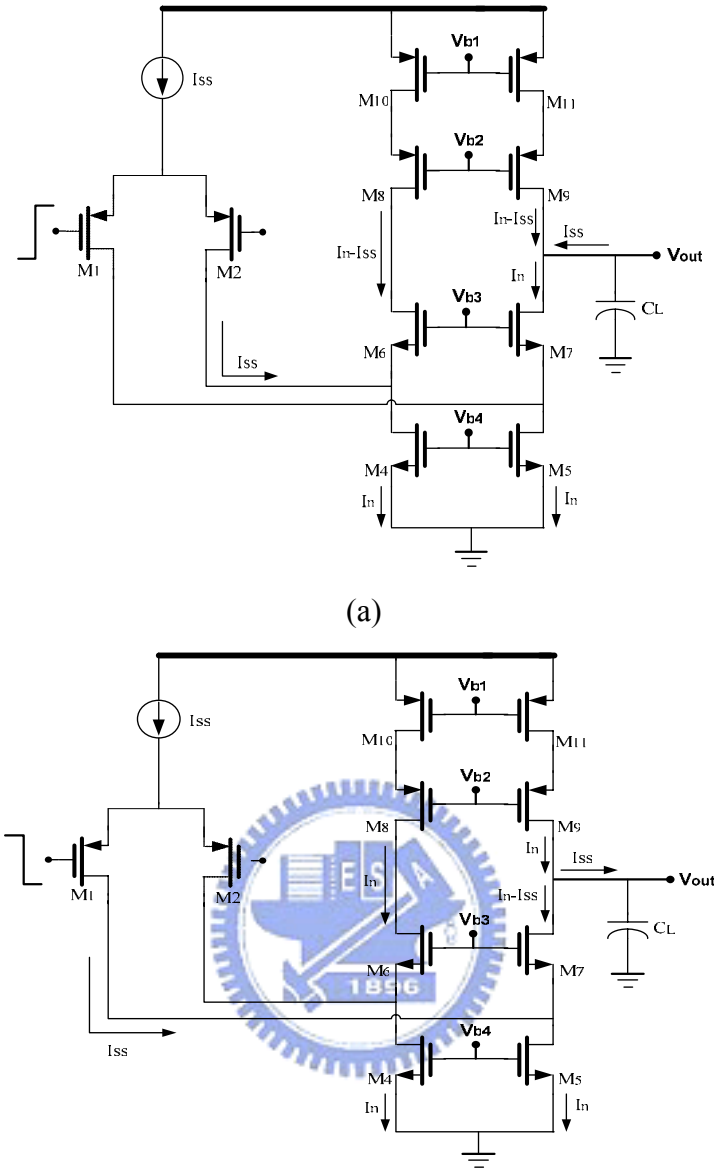


Figure 3.2 Slewing behavior of the folded cascode op-amp

3.2.2 Gain-Boosting Technique

A very widely-used technique to enhance the op-amp dc gain without going into multistage architectures is based on improving the cascoding effect of a single MOS transistor by using local negative feedback [11]. The resultant circuit, often referred to as regulated cascode, is shown in Figure 3.3. The auxiliary amplifier encloses the

cascode transistor M_2 in a feedback loop, making the voltage on its source node almost constant. As a result, the output impedance is given by

$$R_{out} \approx A_1 g_{m2} r_{o2} r_{o1}. \tag{3.4}$$

Thus the regulation improves the impedance by the gain of the auxiliary amplifier A_1 and the dc gain of the op-amp is increased by the same amount. [10]

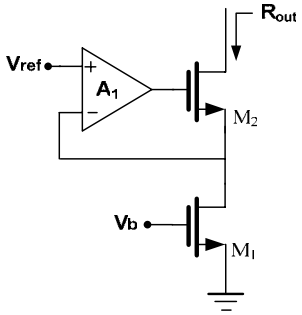


Figure 3.3 Increasing the output impedance by feedback

Shown in Figure 3.4 is a folded cascode op-amp with gain-boosting technique used in this project, the output impedance of such a boosts of the PMOS current sources as well, thereby getting a very high gain.

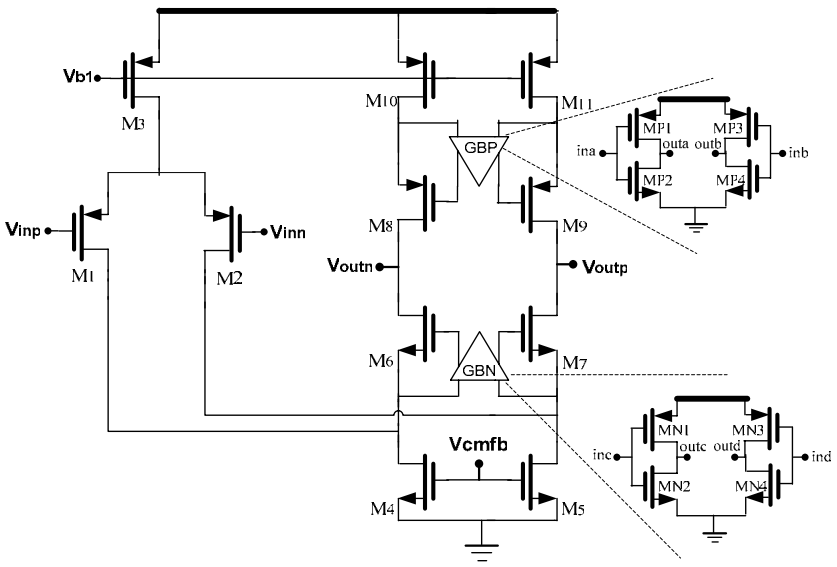


Figure 3.4 Folded cascode op-amp with gain-boosting technique

3.2.3 The Common-Mode Feedback (CMFB) of Switched Capacitor

In the previous section, we have discussed the advantages about the fully-differential op-amp. As we know, fully-differential circuits provide better rejection of common-mode (CM) noise and high-frequency power-supply variations compared to their single-ended circuits. However, since the CM loop gain from the external feedback loop around the fully-differential op-amp is small, the CM voltage in fully-differential circuits is not precisely defined. Without proper control, the output CM voltage tends to drift to the supply rails due to power-supply variations, process variations, offsets, etc. Hence, an additional CM feedback loop is usually necessary. The circuit comprising this CM feedback loop is called the CM feedback (CMFB) circuit.

The CMFB circuit performed in switched-capacitor (SC) is shown in Figure 3.5. The main advantages of SC-CMFB are that they impose no limits on the maximum allowable differential input signals, have no additional parasitic poles in the CM loop, and are highly linear. However, SC-CMFB injects nonlinear clock-feedthrough noise into the op-amp output nodes and increases the load capacitance that needs to be driven by the op-amp. Hence, SC-CMFB is typically only used in switched-capacitor applications such as sample-and-hold amplifier and SC-filter.

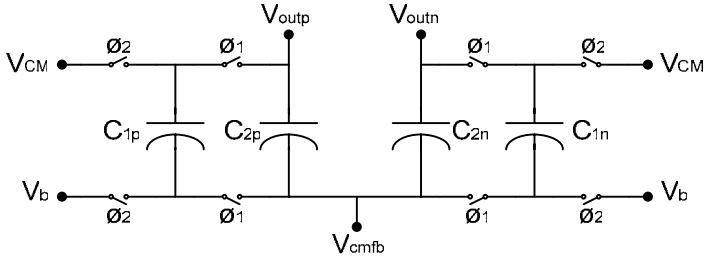


Figure 3.5 Switched-capacitor CMFB circuit

During clock phase $ø_1$, C_{1p} and C_{1n} are connected to C_{2p} and C_{2n}, respectively. The dc voltage across C_{2p} and C_{2n} is determined by C_{1p} and C_{1n}, respectively, and is refreshed every $ø_1$ clock phase. During clock phase $ø_2$, C_{1p} and C_{1n} are charged to V_{CM}-V_b and capacitors C_{2p} and C_{2n} generate the control voltage V_{cmfb} and the output voltage of V_{outp} and V_{outn}. [12]

3.2.4 Simulation Result of The Folded-Cascode Op-Amp

Figure 3.6 shows the AC simulation results including the gain and phase margin of five process corners (TT, FF, FS, SF, SS). The simulated slew rate response of the op-amp is shown in Figure 3.7. The simulated performance of the fully-differential folded cascode op-amp is summarized in Table 3.1.

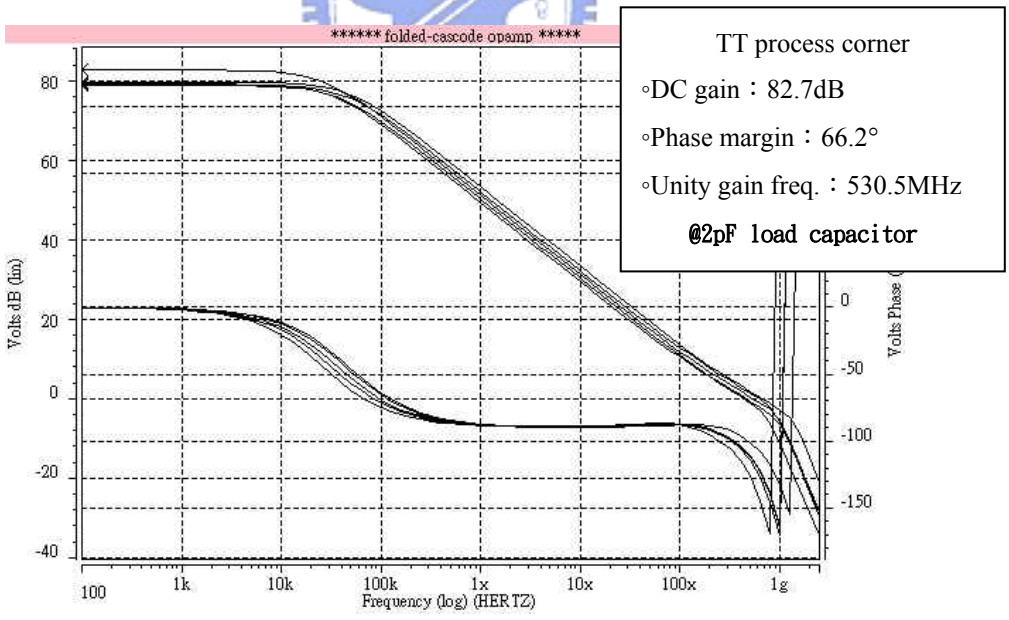


Figure 3.6 Simulated AC results of the op-amp

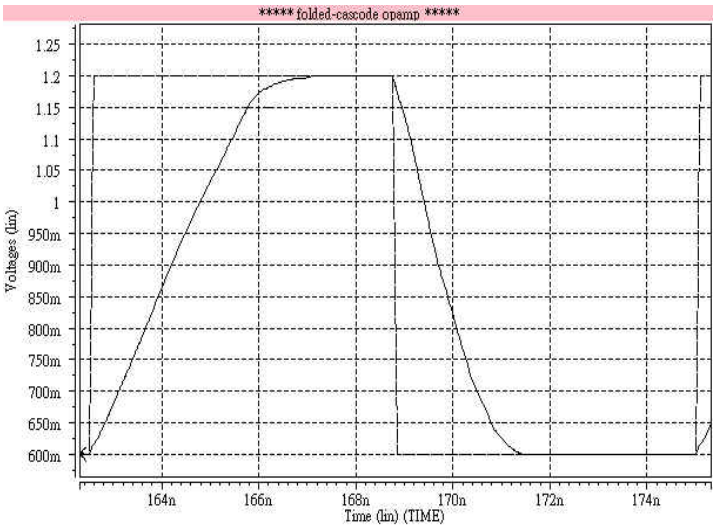


Figure 3.7 Simulated slew rate result of the op-amp

Table 3.1 Summary of the simulation results of the op-amp

Folded-Cascode Op-amp		
DC Gain		82.7dB
Phase Margin		66.2°
Unity Gain Bandwidth		530.5MHz
Load Capacitor		2pF
Common Mode Input Range		0.3V~1.4V
Output Swing		0.35V~1.45V
Slew Rate	Rise	202V/μs
	Fall	311V/μs
Settling Time		4.56ns
Power Dissipation		5.34mW
Process		TSMC 0.18μm 1P6M Process

3.3 Comparator

A fully-differential CMOS dynamic comparator topology suitable for pipelined ADC with a low stage resolution is used in this project and shown in Figure 3.8. The comparator, based on two cross coupled differential pairs and switchable current sources, has a small power and area dissipation and it is shown to be very insensitive to transistor mismatch. In order to make the comparator insensitive to mismatch and process variations, all transistors should be operated in saturation region after the latching signal applied.

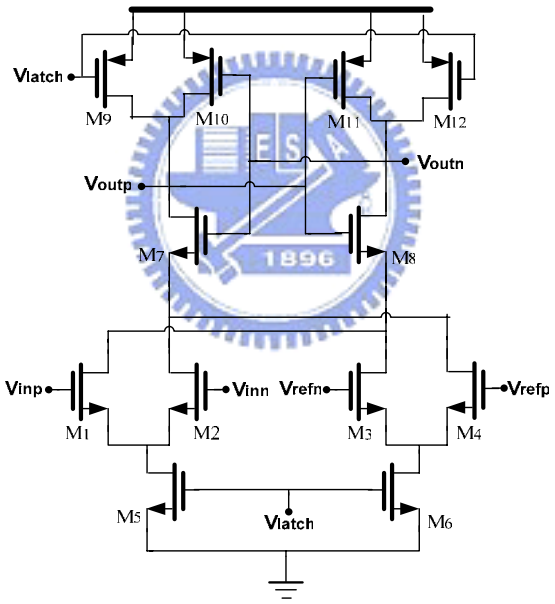


Figure 3.8 Schematic diagram of comparator circuit

The operation of the comparator is described as followed. Where transistors M_1~M_4 are the two cross coupled differential pairs, M_5 and M_6 are the current source transistors, and M_7~M_{12} forms the latches. When the comparator is inactive the latch signal V_{latch} is at 0V, which means that the current source transistors M_5 and M_6 are switched off and no current path between the supply voltages exists. Simultaneously

the switch transistors M_9 and M_{12} reset the outputs by shorting them to V_{dd}. The transistors M_7 and M_8 of the latch conduct and force the drains of all the input transistors M_1~M_4 to V_{dd}. When the V_{latch} is risen to V_{dd} the outputs are disconnected from the positive supply and the switching current sources M_5 and M_6 enter saturation regions and begin to conduct. These two transistors determine the bias currents of the two differential pairs M_1 - M_2 and M_3 - M_4, respectively. Therefore, the threshold voltage of the comparator is determined by the current division in the differential pairs and between the cross coupled branches. [13] [14]

Figure 3.9 shows the simulation result of the output signal when applying the sine-wave input into the comparator.

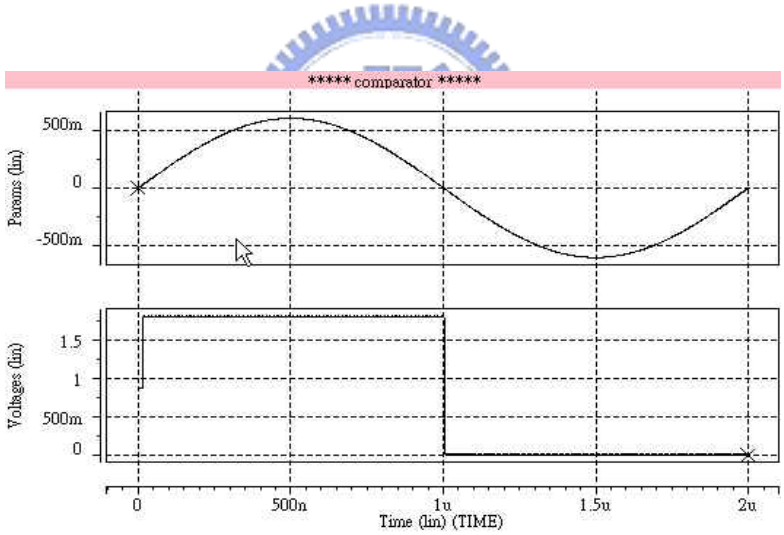


Figure 3.9 Simulated result of the comparator

3.4 Bootstrapped Switches

Figure 3.10 shows the well known gate-source bootstrapping technique. It shows the signal switch MNSW together with five additional switches (S1~S5) and an additional capacitor C. Switches S3 and S4 charge the capacitor during $ø_2$ to V_{DD}.

During $ø_1$, switches S1 and S2 connect the pre-charged capacitor in series with the input voltage V_{in} such that the gate-source voltage of transistor MNSW is equal to the voltage V_C ($\cong V_{DD}$) across the capacitor. This guarantees maximum switch conductance independent of V_{in}. This advantage is that the constant R_{ON} due to the fixed V_{GS} makes the time constant $\tau=R_{ON}\times C$ independent of the input signal. This will decrease the harmonic distortion. The fixed V_{GS} also eliminates the high gate oxide voltage when the input signal is low. Switch S5 fixes the gate voltage of MNSW to V_{SS} during $ø_2$ to make sure that the transistor is in the OFF state.

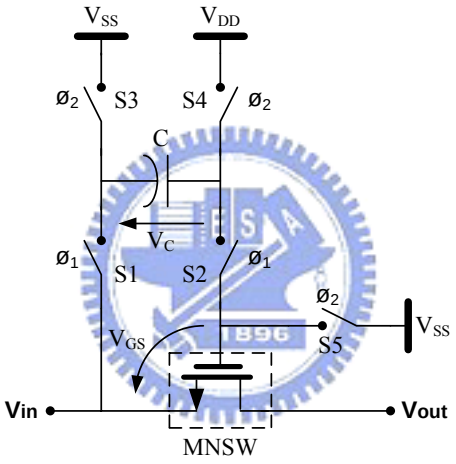


Figure 3.10 Basic circuit of the bootstrapped switch

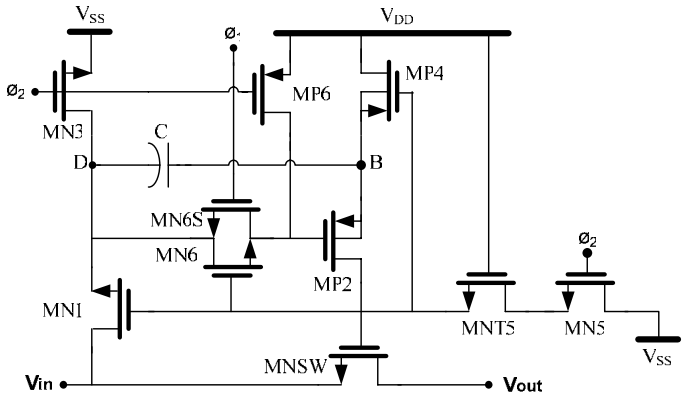


Figure 3.11 Transistor-level implementation of the bootstrapped switch

Figure 3.11 shows the transistor-level implementation of the bootstrapped-switch circuit shown in Figure 3.10. Transistors MN1, MP2, MN3, MP4, and MN5 correspond to the five ideal switches S1~S5 respectively. The transistor MN6S triggers MP2 on at the beginning of $ø_1$ while transistor MN6 keeps it on as the voltage on node D rising to the input voltage V_{in}. Gate connections of transistors MN1 and MN6 allow them to be turned on similar to the main switch MNSW. Furthermore, transistor MNT5 has been added to prevent the gate–drain voltage of MN5 from exceeding V_{DD} during $ø_1$ while it is off. During $ø_1$ when MNT5 is off, its drain-bulk diode junction voltage reaches a reverse bias voltage of $2V_{DD}$. This must be compatible with the technology limits. It should be also noted that the bulk of transistors MP2 and MP4 must be tied to the highest potential, i.e., node B, and not to V_{DD}.

However, the voltage at the drain side of the main switch MNSW must be always higher than that at the source side at the switching moment to prevent the drain–gate voltage from exceeding V_{DD} during the turn-on transient. In spite of the fact that the gate–source potential of the bootstrapped switch is held constant, the conductance drops with the source voltage due to the source-bulk potential which increases the threshold voltage. [16] [17]

3.5 Sample and Hold Amplifier

The front-end sample-and-hold amplifier (SHA) is shown in Figure 3.12. Figure 3.13 shows the non-overlapping clock phases used in this project. During the sampling phase (phase $ø_1$), capacitors C_S are connected to the differential inputs V_{in} ($V_{in}=V_{inp}-V_{inn}$) and the inputs of the op-amp. At the same time, the inputs and the

outputs of the op-amp are connected together in a negative feedback configuration. This makes the differential voltages at these nodes to be equal to the input offset voltage of the op-amp, V_{offset}. Therefore, the capacitors C_S are charged to V_{in}-V_{offset}. During the holding phase (phase $ø_2$), the capacitors C_S are connected between the inputs and the outputs of the op-amp. This will make the differential output voltages to be equal to V_{in} without regard to the input offset voltage of the op-amp. It means that the SHA reduces the offset error of the op-amp by storing the error during one clock phase and subtracting this error from the signal during the next phase. At the end of the holding phase, the differential output voltage is given by

$$V_{out} = \frac{V_{in} + \frac{V_{offset}}{A}}{1 + \frac{1}{A}}, \tag{3.5}$$

where A is the dc gain of the op-amp. For very large A, the equation 3.5 can be approximated as

$$V_{out} \cong V_{in}. \tag{3.6}$$

Since the sampling and the holding capacitors use the same capacitors, this SHA has no gain-error due to the capacitor mismatch. However, the SHA is not suitable for processing single-ended signals because this circuit lack the inherent single-ended to fully-differential conversion capability. However, the single-ended signals will not be used in this project.

Since this SHA is supposed to be used in the front-end of the pipelined ADC, the size of the capacitors should be chosen in order to reduce the sampled thermal noise (kT/C) to an acceptable level. [15]

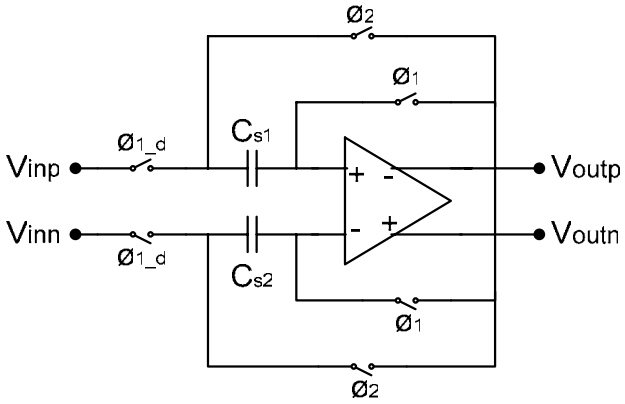


Figure 3.12 Schematic diagram of sample-and-hold amplifier circuit

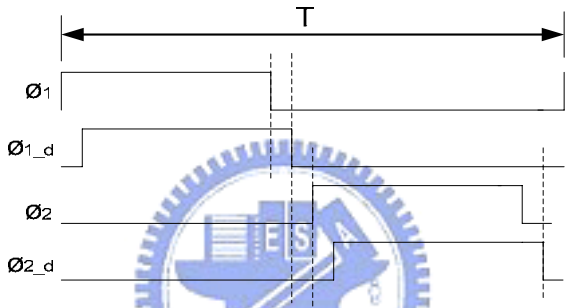
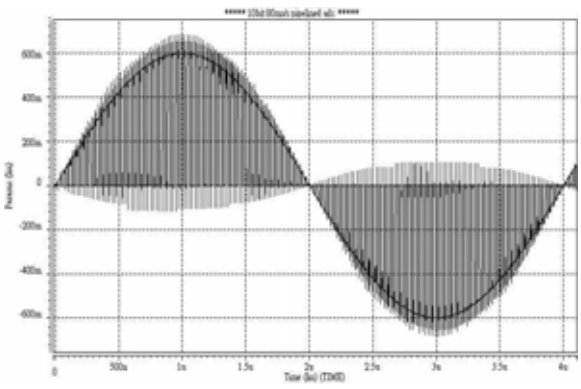
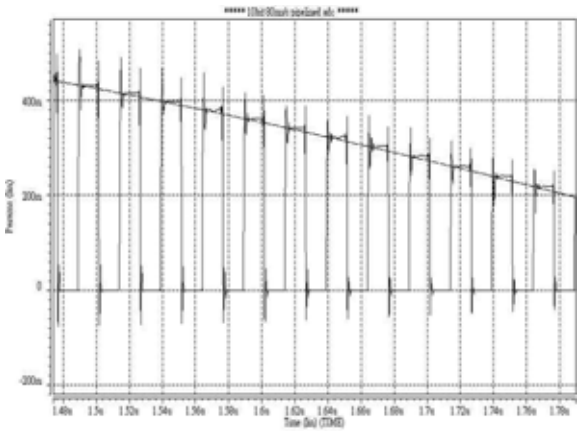


Figure 3.13 Non-overlapping clock phases

Figure 3.14 shows the simulation result of the SHA when applying the sine-wave input of 0.25MHz (frequency) with the amplitude of ±600mV. Figure 3.14(b) is the zoom-in result of Figure 3.14(a).



(a)



(b)

Figure 3.14 Simulated result of the SHA sampling the input sine-wave

3.6 The 1.5-Bit Sub-ADC (Flash Quantizer)

As previously mentioned in section 2.5, in a pipelined ADC, the function of the sub-ADC is to convert the held input of the previous stage into low resolution digital codes. Traditional N-bit flash converters employ a resistor-string for the division of the reference voltage for defining the decision levels combined with 2^N-1 comparators. In this project, the 1.5-bit sub-ADC uses only 2 comparators in its implementation.

For a 1.5-bit sub-ADC, a comparator offset voltage up to ±Vref/4 can be tolerated through digital error correction technology. The comparator structure employed in the 1.5-bit sub-ADC is shown in Figure 3.8, and the 1.5-bit sub-ADC is shown in Figure 3.15. Where the MSB and LSB are the digital output codes of the 1.5-bit sub-ADC, and the X, Y, and Z are the controlled signals which will be applied to the MDAC. Table 3.2 summaries the digital output codes of MSB and LSB and the controlled signals of X, Y, and Z for different values of the differential input voltage. Figure 3.16 shows the simulated result of the 1.5-bit sub-ADC, where the ±Vref are set equal to ±600mV.

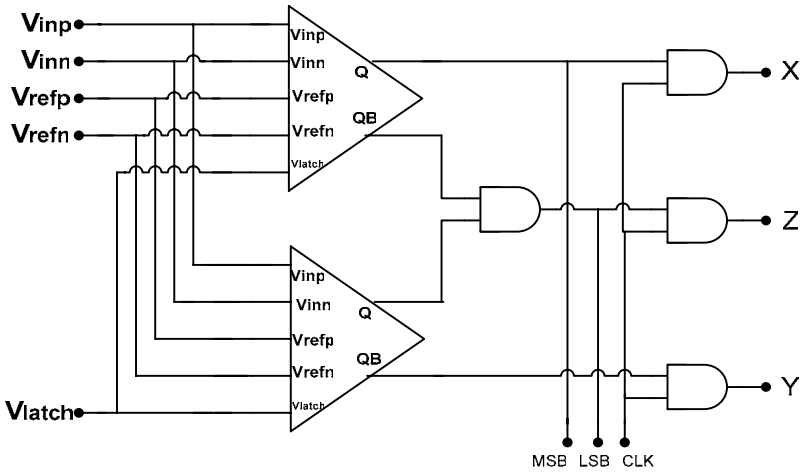


Figure 3.15 Schematic of the 1.5-bit Sub-ADC

Table 3.2 Digital output codes and controlled signals of 1.5-bit sub-ADC

Differential Input Voltage (V_{in})	Digital Output Codes (MSB, LSB)	Controlled Signals (X, Y, Z)
$-V_{ref} < V_{in} < \frac{-V_{ref}}{4}$	00	010
$\frac{-V_{ref}}{4} < V_{in} < \frac{+V_{ref}}{4}$	01	001
$\frac{+V_{ref}}{4} < V_{in} < +V_{ref}$	10	100

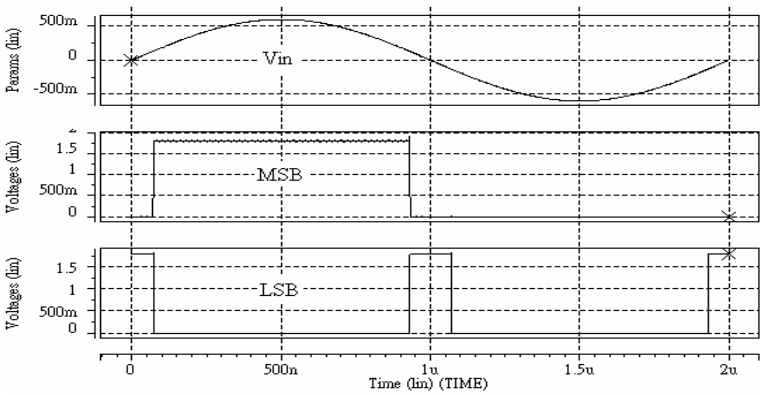


Figure 3.16 Simulated result of the 1.5-bit Sub-ADC

3.7 The 1.5-Bit MDAC

Figure 3.17 shows the schematic of the 1.5-bit MDAC circuit, which consists of an op-amp, four equal sized capacitors and 13 switches. In a pipeline stage the function of the MDAC is twofold. First, it provides the sample-and-hold operation required for the pipelining, second, it performs the analogue reconstruction of the digital code resulting from the sub-ADC, subtracts it from the analogue sampled voltage, Vin, and multiplies the resulting residue by 2. Phase $ø_1$ and phase $ø_2$ are two non-overlapping signals and phase $ø_{1\_d}$ is a delayed version of phase $ø_1$ but still non-overlapping with phase $ø_2$. During phase $ø_1$ (sampling phase), the two pairs of capacitors Cs and Cf sample the differential input Vinp and Vinn. Next, during phase $ø_2$ (residue amplification phase), the integrating capacitors, Cf, form the feedback loop of the op-amp while the bottom plates of the sampling capacitors are connected to each other, to the positive reference (Vrefp), or to the negative reference (Vrefn) depending on the state of controlled signals X, Y, and Z. Assuming Cs=Cf=C and the a non-ideal op-amp with finite DC gain, A, and offset voltage V_{offset}, at the end of phase $ø_2$, the value of the amplified residue to be processed by the next stage of the pipeline is given approximately by

$$V_{out} = \begin{cases} \dfrac{2V_{in} + V_{ref} + \dfrac{2V_{offset}}{A}}{1+\dfrac{2}{A}}, if\ -V_{ref} < V_{in} < \dfrac{-V_{ref}}{4} \Leftrightarrow Y = 1 \\ \dfrac{2V_{in} + \dfrac{2V_{offset}}{A}}{1+\dfrac{2}{A}}, if\ \dfrac{-V_{ref}}{4} < V_{in} < \dfrac{+V_{ref}}{4} \Leftrightarrow Z = 1 \\ \dfrac{2V_{in} - V_{ref} + \dfrac{2V_{offset}}{A}}{1+\dfrac{2}{A}}, if\ \dfrac{+V_{ref}}{4} < V_{in} < +V_{ref} \Leftrightarrow X = 1 \end{cases}, \quad (3.7)$$

yielding for very large A

$$V_{out} \cong 2 \cdot V_{in} - X \cdot V_{ref} + Y \cdot V_{ref} , \tag{3.8}$$

where X, Y, and Z are the encoded digital outputs provided by the 1.5-bit sub-ADC.

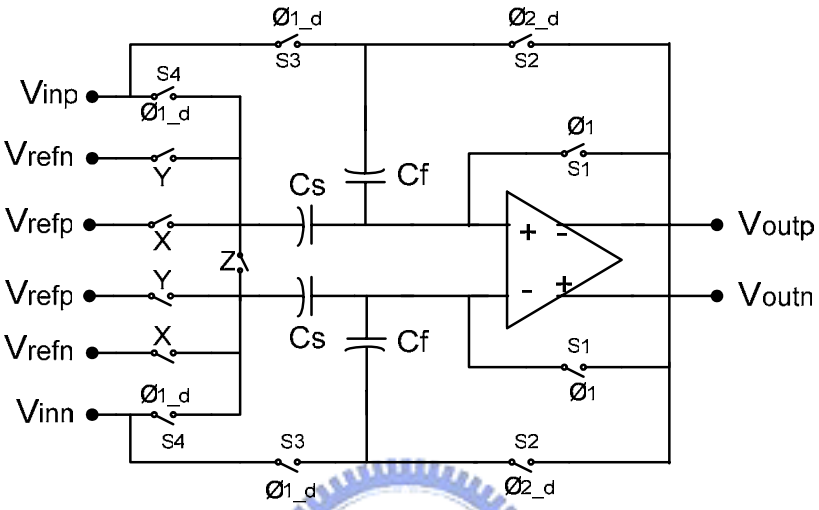


Figure 3.17 Schematic of the 1.5-bit MDAC

Figure 3.18 shows the simulation output waveform of the MDAC circuits. The input signal Vin is first applied to front-end SHA, then the output signal of the SHA is applied to the 1.5-bit MDAC and the 1.5-bit sub-ADC.

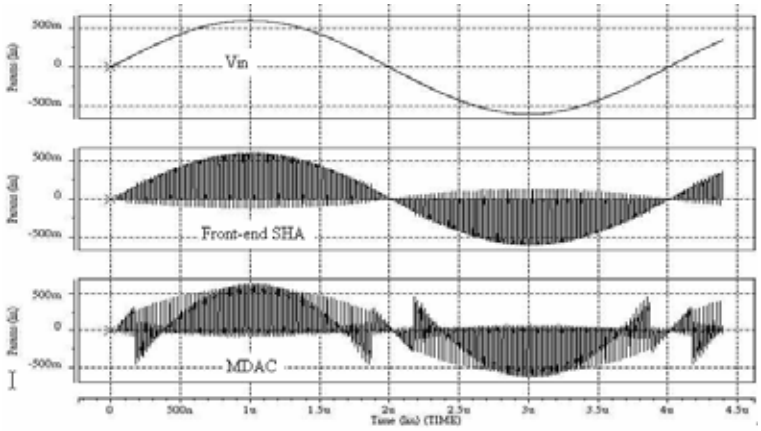


Figure 3.18 Simulated result of the 1.5-bit MDAC

3.8 The 2-Bit Flash ADC

The final stage of 2-bit flash ADC is shown Figure 3.19. A typical architecture of a 2-bit flash quantizer requires a bank of 3 comparators to achieve 2 bits of resolution. Figure 3.20 shows the simulation result of the 2-bit flash ADC

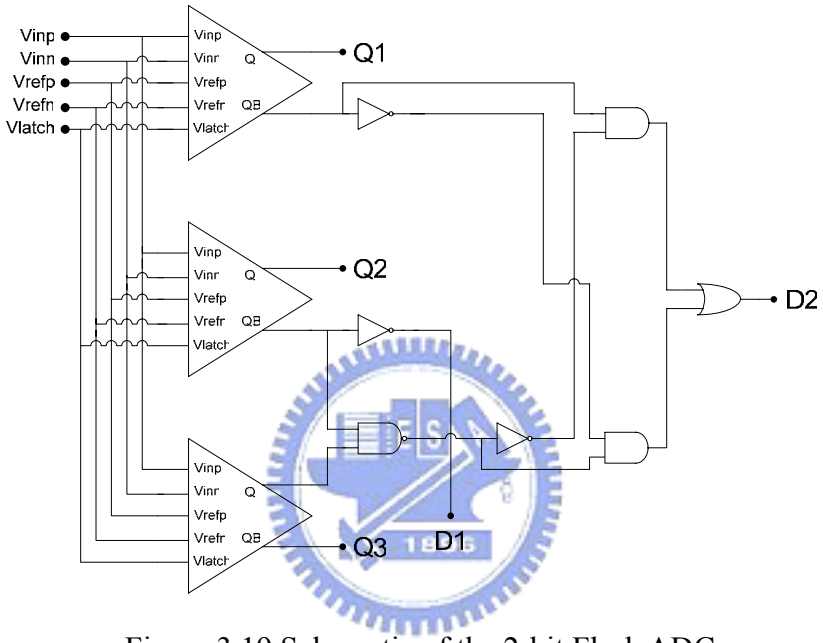


Figure 3.19 Schematic of the 2-bit Flash ADC

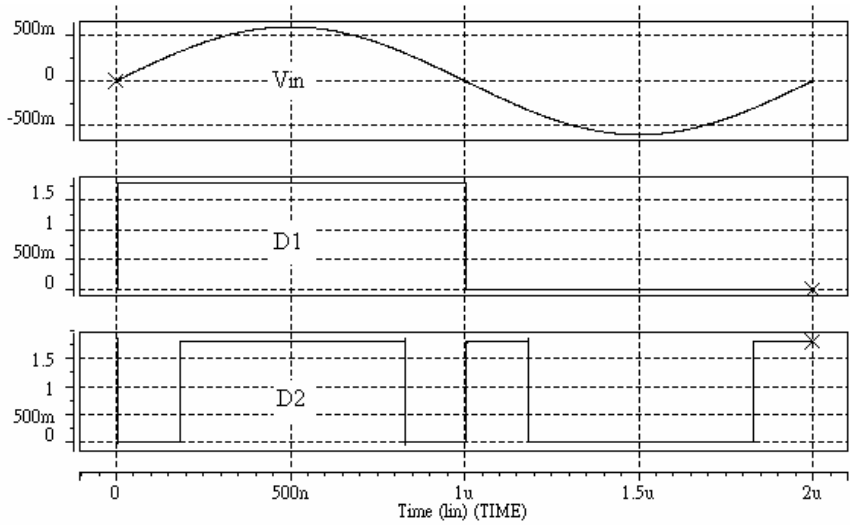


Figure 3.20 Simulated result of the 2-bit Flash ADC

3.9 Simulated Results of Pipelined ADC

The architecture of the 10-bit, 80MS/s pipelined A/D converter with the 1.8V supply voltage shown in Figure 3.21 had simulated with eight identical 1.5-bit stages and one 2-bit flash converter. In the simulation, we use the ideal DAC to convert digital outputs of the pipelined ADC to analog signal. Figure 3.22 shows the simulated result of the pipelined ADC when applying the 1 MHz sine-wave to the inputs.

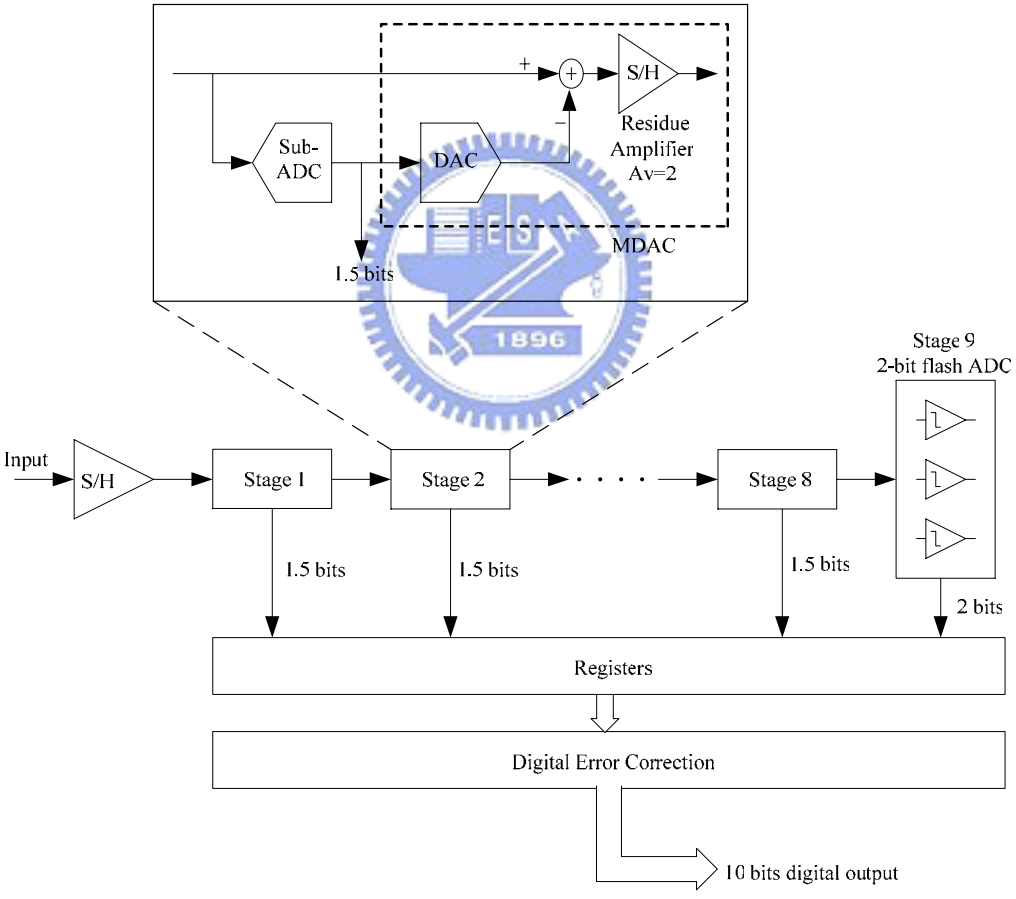


Figure 3.21 All schematic block of pipelined ADC

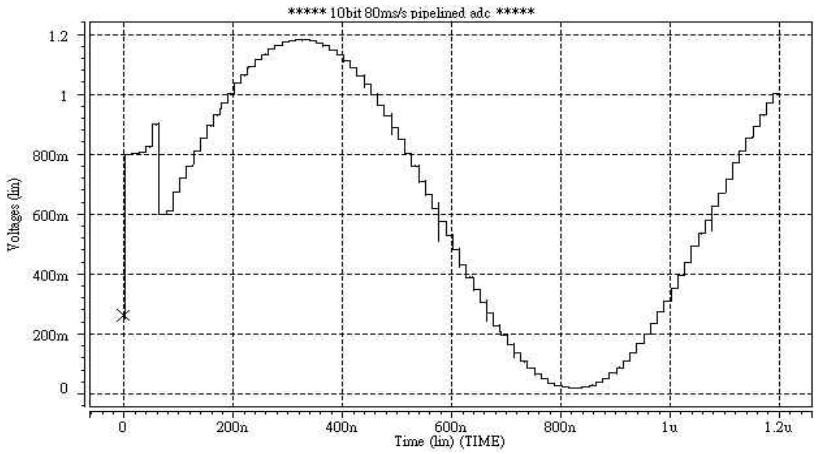


Figure 3.22 Simulated result of the pipelined ADC with the sine-wave input signal

Figure 3.23 shows the simulated results through the ideal DAC when applying the ramp signal to input. Then the results are analyzed for characterizing the linearity of the ADC. However, the linearity of the ADC could be realized by analyzing the parameters of the DNL and INL. The simulated results of the DNL and INL of the pipelined ADC are shown in Figure 3.24. The maximum DNL and INL are ±0.7 LSB and ±1.0 LSB respectively.

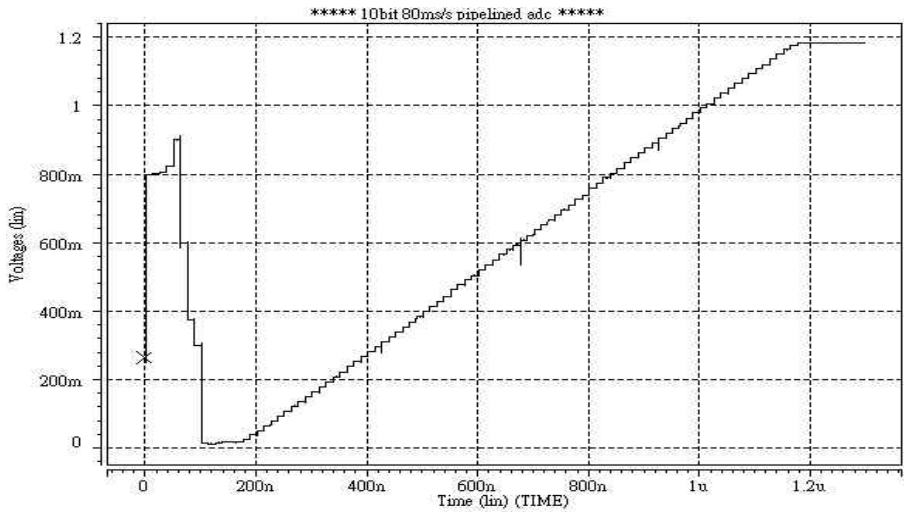
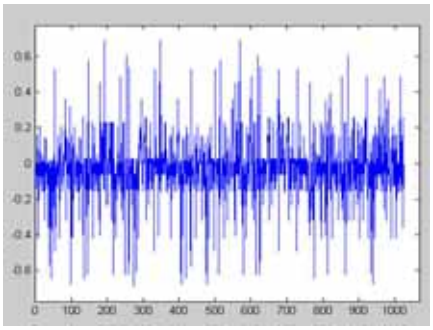
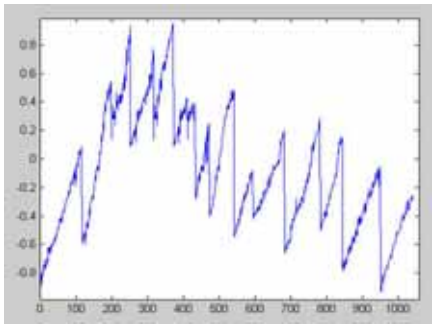


Figure 3.23 Simulated result of the pipelined ADC with the ramp input signal



(a) DNL



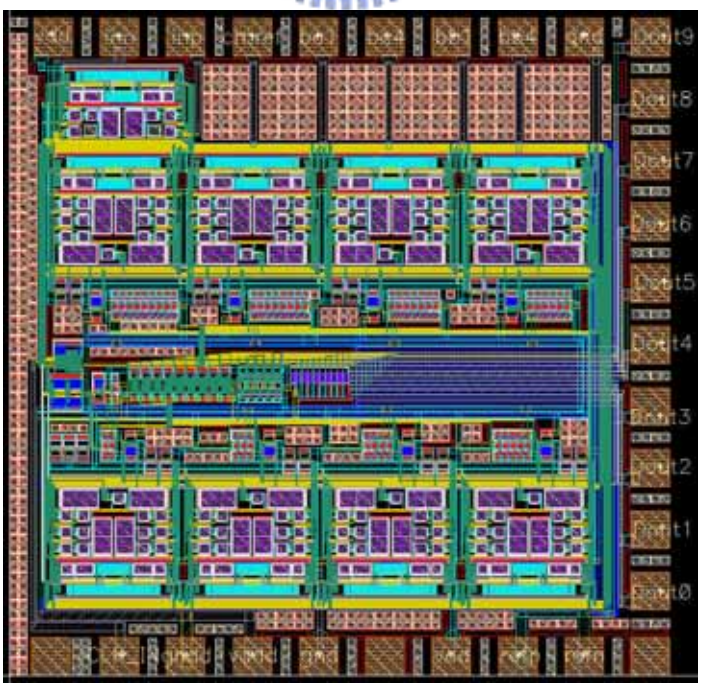
(b) INL

Figure 3.24 Simulated results of DNL and INL

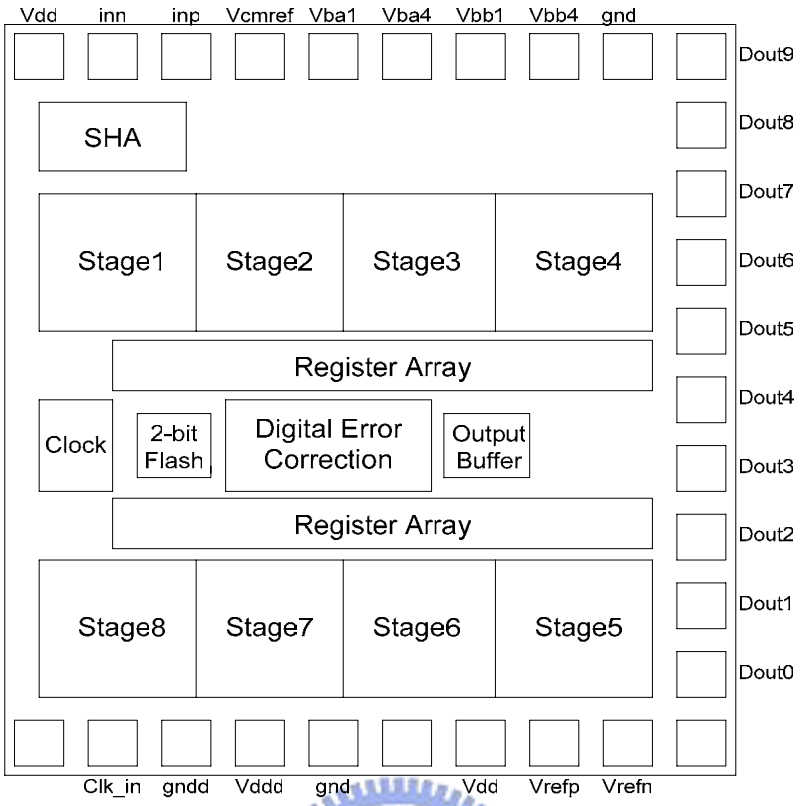
Table 3.3 summaries the simulated results of the pipelined ADC. Layout and floor plan of the experimental prototype chip are shown in Figure 3.25. This pipelined ADC was laid out on a 1.388×1.392 mm^2 die that including digital circuits and the pad frame. In the layout, we use the mirror symmetry to enhance the rejection of common mode noises in the fully differential circuits. In this research, the analog circuit is separated from the digital circuit and is powered from a separated power supply.

Table 3.3 Summary of simulated results of the pipelined ADC

Parameters	Simulated Results
Process	TSMC 0.18μm CMOS Mixed-Signal
Supply Voltage	1.8 V
Input Range	±0.6V Fully differential
Resolution	10 bits
Operation Frequency	80 MHz
DNL	±0.7 LSB
INL	±1.0 LSB
SFDR (Fin=1MHz)	58 dB
Power Dissipation	85 mW
Chip Size	1.388mm×1.392mm



(a) Layout



(b) Floor plan

Figure 3.25 Layout and floor plan of the pipelined ADC

Chapter 4

Test Setup and Experimental Results

4.1 Introduction

This pipelined ADC has been designed and laid out by using the TSMC 0.18μm CMOS Mixed-Signal process with one poly and six mental. In this chapter, we present the testing environment, including the component circuits on the DUT (device under test) board and the instruments. The measured results are presented in this chapter, too.

4.2 Test Circuits

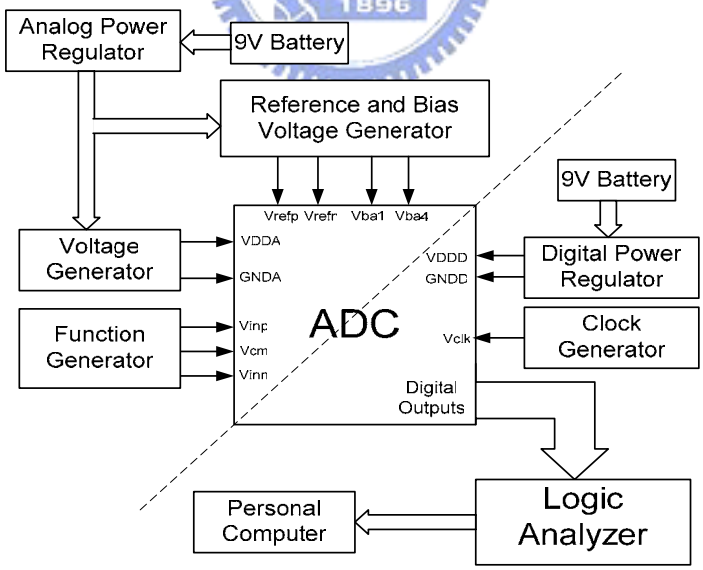


Figure 4.1 Testing setup

Figure 4.1 shows the testing setup used to measure the performance of the experimental pipelined ADC described in this project. It contains analog power

regulator, digital power regulator, clock generator, function generator, logic analyzer, and etc. The supply voltages for analog and digital power regulators are supplied by the 9V batteries. In order to present the digital noise coupling to the analog circuits, the analog ground and digital ground are isolated to each other.

The input signal to the DUT is provided by the signal generator, Agilent E4438C. The photograph of the signal generator is shown in Figure 4.2. The output bit streams of the DUT are sent to the logic analyzer, HP 16702B which is shown in Figure 4.3. The clock signal of the system is generated with a signal generator, HP 8648C, where its output signal is fed to the pulse generator, HP 8133A, to generate the clock signal. The photograph of the clock generators are shown in Figure 4.4.

Figure 4.2 Signal Generator Agilent E4438C

Figure 4.3 Logic analyzer HP 16702B

Figure 4.4 Clock generator, the top instrument is signal generator HP 8648C, and the bottom instrument is pulse generator HP 8133A

4.2.1 Power Supply Regulators

The analog and digital power supplies are generated by the application of the LM317 adjustable regulators shown in Figure 4.5. The diodes D1 and D2 are the protection diodes. The capacitor C1 is used to improve the ripple rejection and capacitor C2 is the input bypass capacitor. The resistor R1 is the fixed resistor and resistor R2 is the precise variable resistor. The output voltage of the Figure 4.2 can be expressed as

$$V_{out} = 1.25 \cdot \left(1 + \frac{R2}{R1}\right) \cdot I_{ADJ} \cdot R2 , \qquad (4.1)$$

where I_{ADJ} is the DC current that flows out of the adjustment terminal ADJ of the regulator. By the way, the resistor R1 can use the low temperature coefficient of the metal film resistor to get the stable output voltage. [23]

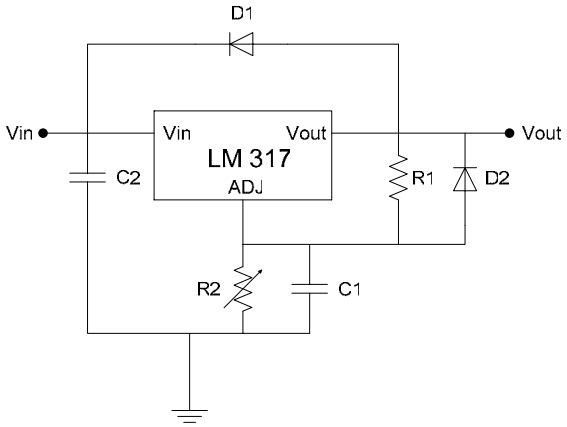


Figure 4.5 Power supply regulator

The outputs of the regulators are bypassed on the PCB with the filter tank. The bypassed filter network is combined by 10uF, 1uF, 0.1uF, and 0.01uF capacitors as shown in Figure 4.6. The capacitor arrangement in Figure 4.6 provides decoupling of both low frequency noise with large amplitude and high frequency noise with small amplitude. [24] [25]

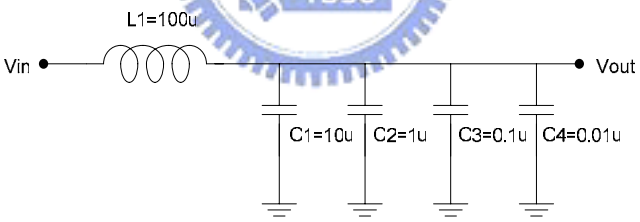


Figure 4.6 Bypass filter at the output of the regulator

4.2.2 Reference and Bias Voltage Generators

Figure 4.7 shows the schematic of the reference and bias voltage generators. The function of this circuit is to generate the low noise dc voltage source implemented with OP27 operational amplifier. The operational amplifier acts as a unity gain buffer for the voltage set by the potentiometer R1 at its input. The terminal Vdd_in is connected from the LM317 voltage regulator described in section 4.2.1. The voltage

of both +9V and -9V are supplied by the power supply instrument. [24]

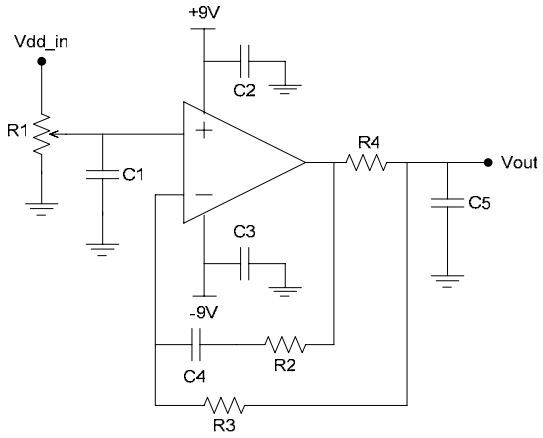


Figure 4.7 Reference and bias voltage generator

4.3 The Package and Pin Configuration

Figure 4.8 shows the die photomicrograph of the experimental pipelined ADC and Figure 4.9 shows the photograph of the testing DUT board. Figure 4.10 presents the pin configuration and lists the pin assignments of the experimental pipelined ADC.

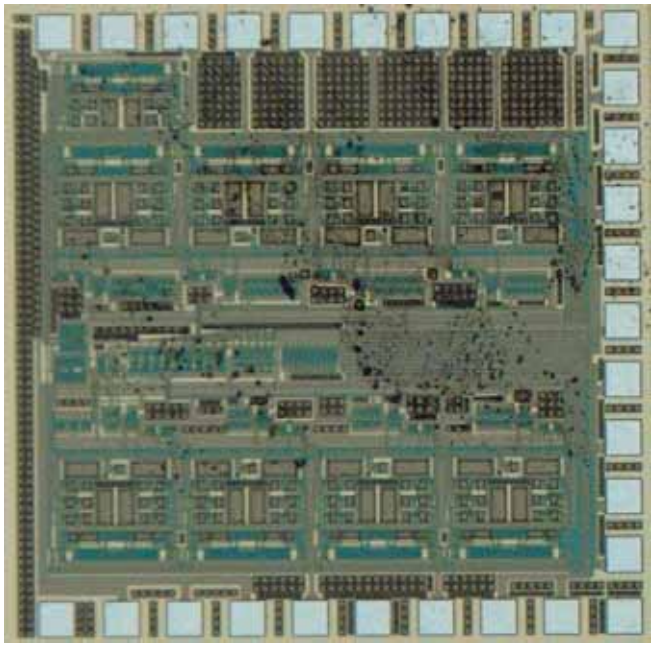
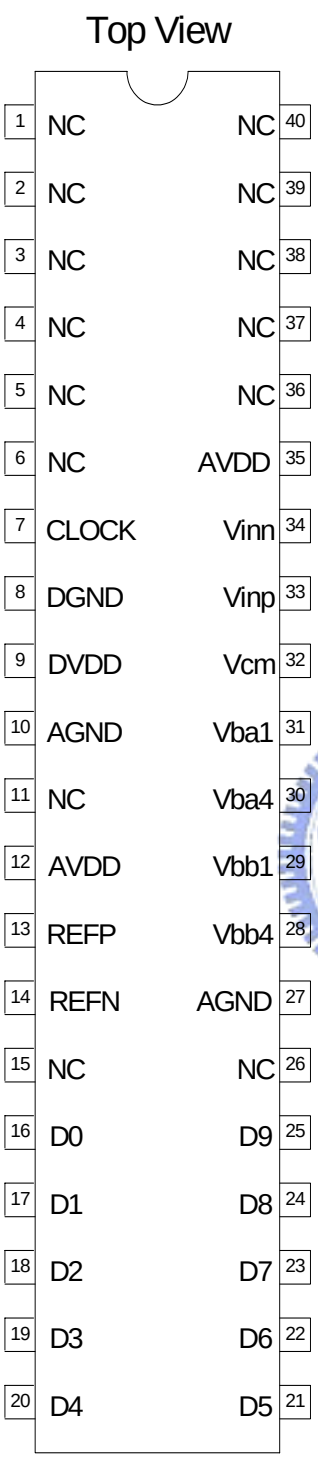


Figure 4.8 Die photomicrograph of the pipelined ADC

Figure 4.9 The photograph of the experimental pipelined ADC DUT board

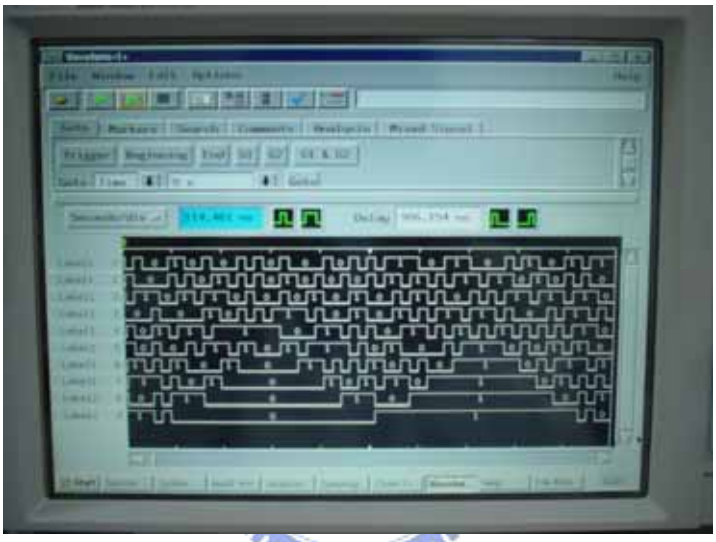


Pin	Name	I/O	Describe
1	NC	-	No connection
2	NC	-	No connection
3	NC	-	No connection
4	NC	-	No connection
5	NC	-	No connection
6	NC	-	No connection
7	CLOCK	In	System clock input
8	DGND	In	Digital ground
9	DVDD	In	Digital power supply
10	AGND	In	Analog ground
11	NC	-	No connection
12	AVDD	In	Analog power supply
13	REFP	In	Reference voltage＞Vcm
14	REFN	In	Reference voltage＜Vcm
15	NC	-	No connection
16	D0	Out	Digital data output
17	D1	Out	Digital data output
18	D2	Out	Digital data output
19	D3	Out	Digital data output
20	D4	Out	Digital data output
21	D5	Out	Digital data output
22	D6	Out	Digital data output
23	D7	Out	Digital data output
24	D8	Out	Digital data output
25	D9	Out	Digital data output
26	NC	-	No connection
27	AGND	In	Analog ground
28	Vbb4	In	Bias voltage
29	Vbb1	In	Bias voltage
30	Vba4	In	Bias voltage
31	Vba1	In	Bias voltage
32	Vcm	In	Common mode voltage
33	Vinp	In	Input signal (0°)
34	Vinn	In	Input signal (180°)
35	AVDD	In	Analog power supply
36	NC	-	No connection
37	NC	-	No connection
38	NC	-	No connection
39	NC	-	No connection
40	NC	-	No connection

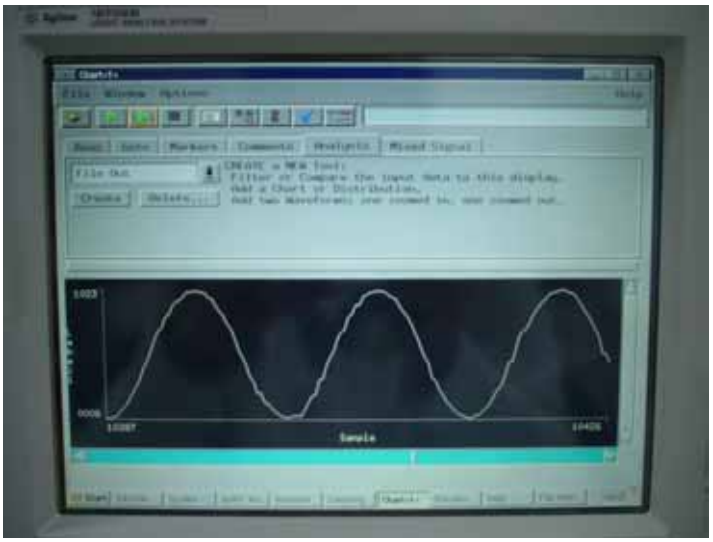
Figure 4.10 (a) Pin configuration diagram and (b) Pin assignment

4.4 Experiment Results of Pipelined ADC

The pipelined ADC has fabricated in 0.18μm CMOS process. The chip was powered by the 1.8 V analog and digital circuits supply. A 1 MHz sine wave is applied to the ADC and operates at the 65 Msample/s conversion rate. The output 10-bit streams of the DUT collected by the logic analyzer and the plot chart are shown in Figure 4.11.



(a) Output bit streams



(b) Plot chart

Figure 4.11 Measured results

From the measured results shown in Figure 4.11, the signal to noise ratio is calculated by collecting 16384 samples of the input signal and performing a 16384 point fast Fourier transform shown in Figure 4.12. This result shows that SNR is about 37.2 dB, and the SNDR is about 31.8 dB due to severe harmonic distortions. The SFDR shown in Figure 4.12 is about 38.1 dB.

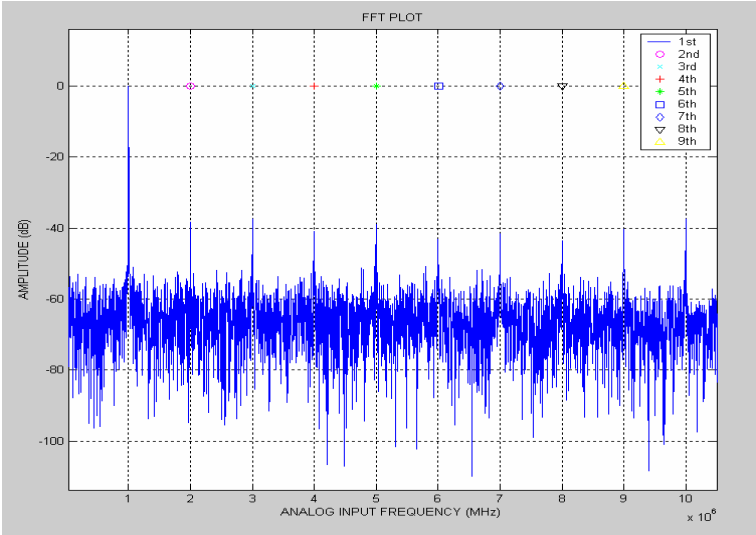


Figure 4.12 16384 points FFT at 1MHz input frequency and 65 MHz sampling frequency

These harmonic distortions are caused by the nonlinear of the op-amp and mismatch of the output pairs. The worst reason is that the DC gain of the op-amp at the highest output swing is no longer large enough to meet the required specification. Furthermore, the charge injection and common mode drift issues both are the possible reasons. In addition, when the sampling rate is large than 65 Msample/s, the plot chart of the ADC doesn't show the similar sine-wave. Probably the input signal and the sampling rate are coupled each other, thus the input signal is influenced and doesn't like sine-wave anymore. Figure 4.13 shows the SNDR for different sampling rate. Table 4.1 summaries the measured results of the pipelined ADC.

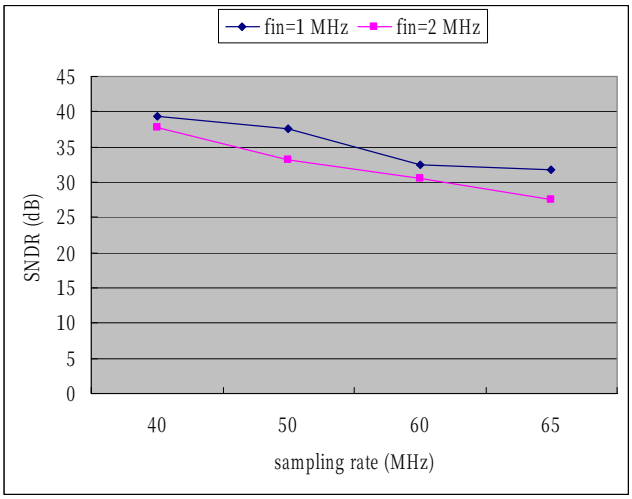


Figure 4.13 The SNDR against the sampling rate

Table 4.1 Summary of measured results of the pipelined ADC

Parameters	Measured Results
Process	TSMC 0.18μm CMOS Mixed-Signal
Supply Voltage	1.8 V
Input Range	±0.6V Fully differential
Operation Frequency	65 MHz
SNR for a 1 MHz input	37.2 dB
SNDR for a 1 MHz input	31.8 dB
SFDR for a 1 MHz input	38.1 dB
ENOB	5 bits
Power Dissipation	79 mW
Chip Size	1.388mm×1.392mm

Chapter 5

Design of Low-Power CMOS Bandgap Reference Circuit

5.1 Introduction

In most analog integrated circuits, bandgap reference voltage generators become the indispensable circuits in operation amplifiers, digital-to-analog converters, and analog-to-digital converters. The reason bandgap reference circuit becomes so important is that it can generate the stable reference voltage which is insensitive to the variation of the temperature and the supply voltage. With the growth of wireless communication systems and portable devices, low-power consumption and low supply voltage operation have become a popular research.

Recently, research on generating a low-power and low supply voltage reference circuit was based on discussing the properties of MOSFETs operated in the weak inversion. In the traditional bandgap reference, the BJTs can be replaced by the MOSFETs which operated in the weak inversion and these MOSFETs can generate the current which has direct proportion to temperature. With the MOSFETs operated in the weak inversion, the reference circuit consumes less current and further reduces the power consumption. The proposed bandgap reference circuit will be illustrated in the next section.

5.2 Bandgap Reference Circuit Configuration

The proposed bandgap reference circuit is shown in Figure 5.1. The elements M1 and M2 connect in a current mirror and serve for realizing the function of self-biasing. The MOSFETs M3 and M4 are designed to operate in the weak inversion such that the low-power reference circuit can be achieved. The current mirror of M1 and M2 is designed to make the drain currents of M3 and M4 operate in the weak inversion, then the voltage across R1 is proportional to the absolute temperature (PTAT). Hence, the resistor ratio R2/R1 can be used to compensate for the variation of the gate-source voltage of M4 with respect to the temperature. The detail circuit analysis will be illustrated in the next section. [18] [19] [20]

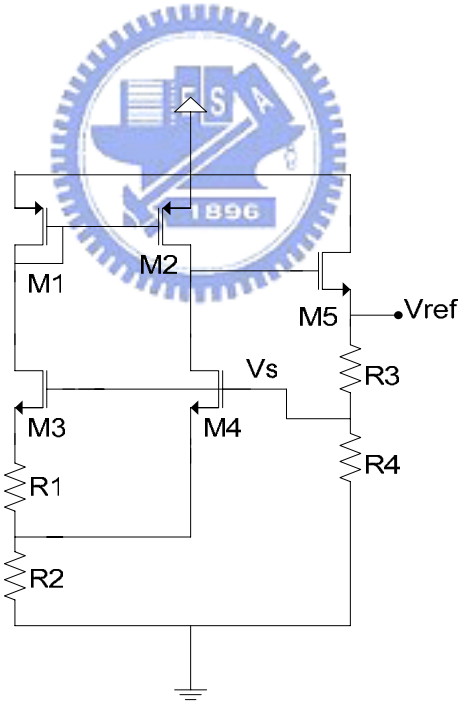


Figure 5.1 Schematic diagram of bandgap reference circuit

5.3 Bandgap Reference Circuit Analysis

For an n-MOSFET operate in the weak inversion region, its drain current is similar to the current of BJTs and it can be given as follows:

$$I_D = \frac{W}{L} I_t \exp\left(\frac{V_{GS}}{nV_T}\right), \tag{5.1}$$

where $I_t = qXD_n n_{q0} \exp\left(\frac{C}{V_T}\right)$, $V_T = \frac{kT}{q}$ the thermal voltage, n and C are the constant, and satisfied $V_{DS} \geq 3V_T$.

The drain currents of M3 and M4 can be expressed as

$$I_{D3} = K_3 I_t \exp\left(\frac{V_{GS3}}{nV_T}\right), \; I_{D4} = K_4 I_t \exp\left(\frac{V_{GS4}}{nV_T}\right), \text{ where } K_3 = NK_4. \tag{5.2}$$

Using equation (5.2) and assuming that the ratio of K_1 and K_2 is unity which meant that the currents go through M3 and M4 are equal, we can obtain

$$V_{GS4} - V_{GS3} = nV_T \ln(N). \tag{5.3}$$

From figure 5.1, we can get a relationship between two gate-source voltages of M3 and M4 and it is given by:

$$V_{GS4} = V_{GS3} + I_{D3} R_1. \tag{5.4}$$

Substitute equation (5.3) into equation (5.4), we obtain

$$I_{D3} = \frac{V_{GS4} - V_{GS3}}{R_1} = \frac{nV_T \ln(N)}{R_1}. \tag{5.5}$$

Equation (5.5) shows that the drain current of M3 is PTAT.

The gate voltage V_S of M3 and M4 is given as:

$$V_S = V_{GS4} + 2I_{D3}R_2 . \tag{5.6}$$

For an n-MOSFET with a PTAT drain current, the voltage V_{GS4} with respect to the temperature can be given by

$$V_{GS4} = A_0 + A_1 T + A_2 T \ln T , \tag{5.7}$$

where A_0, A_1 and A_2 are the constants and dependent on the process technology. Substitute equation (5.5) and equation (5.7) into equation (5.6), thus the voltage V_S can be expressed as

$$V_S = \left(A_0 + A_1 T + A_2 T \ln T\right) + 2\frac{nV_T \ln\left(N\right)}{R_1} R_2 . \tag{5.8}$$

Hence, the resistor ratio R_2/R_1 and the transistor size ratio N of M3 and M4 can be designed to make the temperature coefficient of V_S equal to zero at a selected temperature. Therefore the final output reference voltage V_{ref} can be expressed as

$$V_{ref} = \left(1 + \frac{R_3}{R_4}\right) V_S . \tag{5.9}$$

Figure 5.2 shows the schematic diagram of bandgap reference and startup circuit. The startup circuit is composed of several transistors including Ms1, Ms2 and Ms3, where Ms1 and Ms2 form a CMOS inverter. If the circuit is in the undesired zero-current state, the gate-source voltage V_S of M4 would be less than a threshold voltage. As a result, Ms1 is turned off and Ms2 operates in the triode region, pulling the gate-source voltage of Ms3 up to Vdd. Therefore Ms3 is turned on and pulls down the voltages on the gates of M1 and M2, and this action causes current to flow in M1 and M2 to avoid the zero-current state.

When the circuit is in the steady state, the voltage of V_S is designed to be in the high voltage for the inverter to turn on Ms1. Therefore the gate-source voltage of Ms3 pulls down and Ms3 would be turned off to avoid the current of core circuit flowing into Ms3. Since the startup circuit should not interfere with normal operation of the reference circuit in the steady state, the inverter output should fall low enough to turn Ms3 off in steady state. Therefore this startup circuit can solve the problem of the degeneration and make sure this reference circuit could work normally in the steady state. [20] [21] [22]

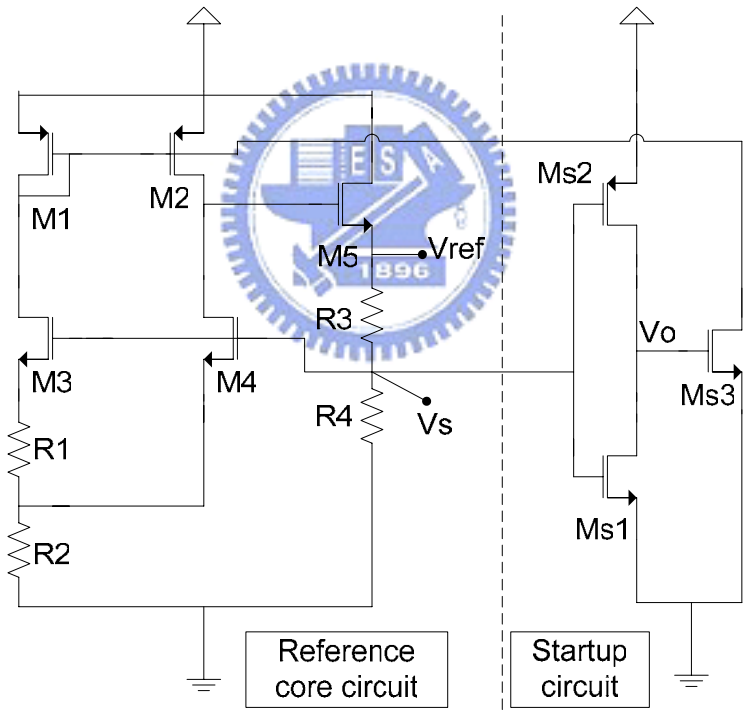


Figure 5.2 Schematic diagrams of Bandgap reference and Startup circuit

5.4 Simulation Results

The simulation results of the low-power CMOS bandgap reference will be shown as follows. Figure 5.3 shows the simulation result of the reference voltage V_{ref} against supply voltage at the 60℃. When the supply voltage is larger than 1.5V, the stability of the reference circuit does not have a lot influence.

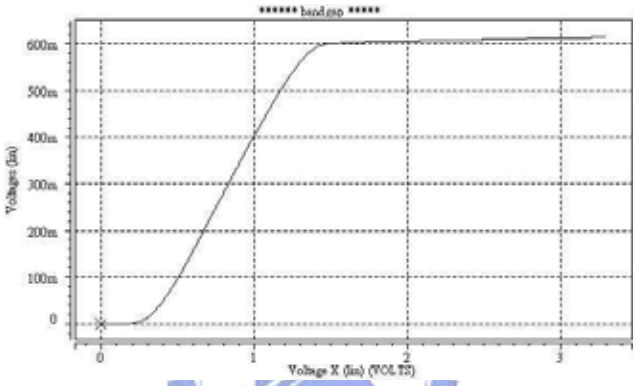


Figure 5.3 Reference voltage against supply voltage

Figure 5.4 shows the simulation result of reference voltage V_{ref} against temperature T at various supply voltages. Table 5.1 shows the temperature coefficient of reference voltage V_{ref} against temperature T at various supply voltages.

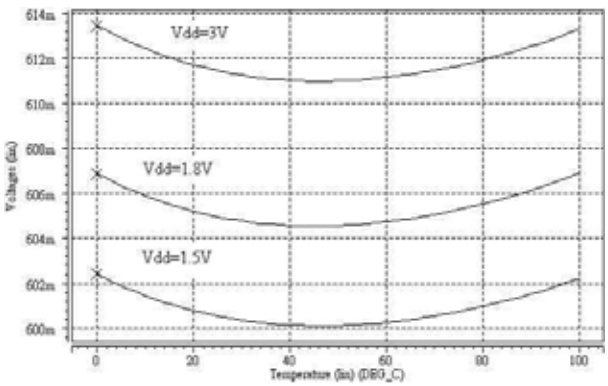


Figure 5.4 Reference voltage against temperature at various supply voltages

Table 5.1 Temperature coefficient of different supply voltages

Supply voltage	Reference voltage	Temperature coefficient
1.5V	601mV	37.8 ppm/℃(2.28mV)
1.8V	605mV	38.4 ppm/℃(2.33mV)
3V	612mV	40.3 ppm/℃(2.47mV)

Figure 5.5 shows the simulation result of the reference voltage against temperature at 1.8V supply voltage of five process corners (TT, FF, FS, SF, SS). Table 5.2 shows the temperature coefficient of reference voltage V_{ref} against temperature T at five process corners.

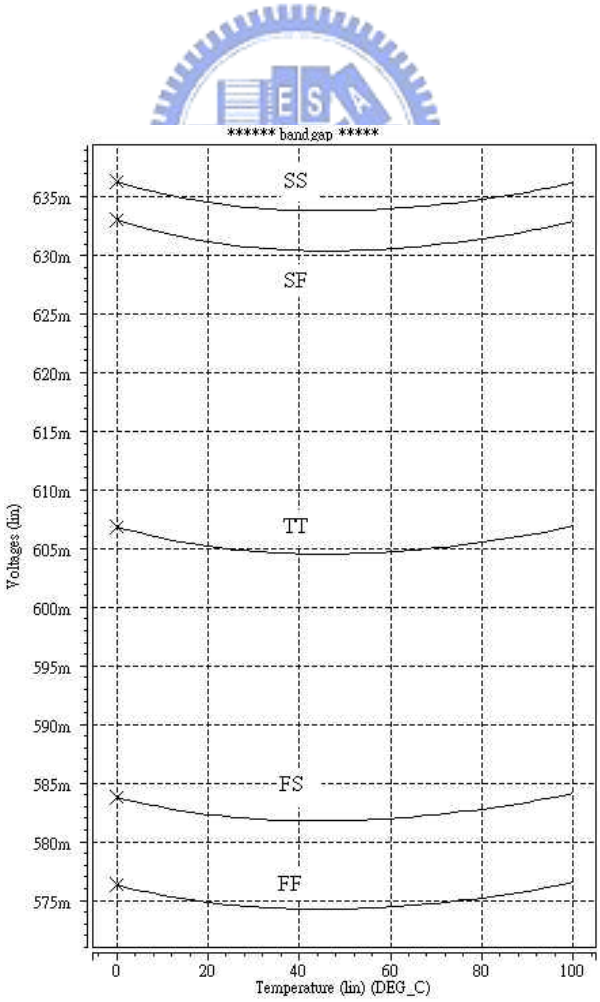


Figure 5.5 Reference voltages against temperature at five process corners

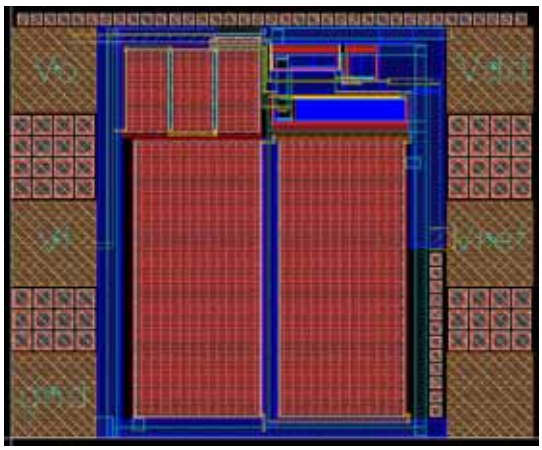
Table 5.2 Temperature coefficient of different process corners

Process Corner	Reference voltage	Temperature coefficient
TT	605mV	38.4ppm/℃(2.33mV)
FF	575 mV	39.7ppm/℃(2.28mV)
FS	583mV	40.4ppm/℃(2.35mV)
SF	633mV	41.2ppm/℃(2.60mV)
SS	635mV	39.8ppm/℃(2.54mV)

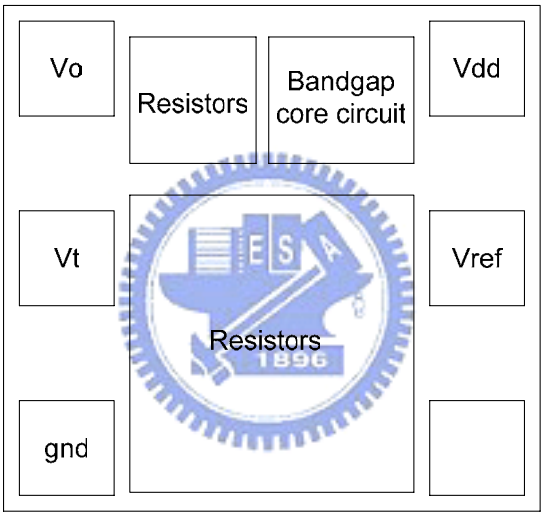
Table 5.3 summaries the simulation results of the low-power CMOS bandgap reference. Layout and floor plan of the experimental prototype chip are shown in Figure 5.6. This low-power CMOS bandgap reference circuit was laid out on a $0.400\times0.490mm^2$ die that including the pad frame.

Table 5.3 Summary of the simulated results of the CMOS bandgap reference

Parameters	Simulated Results
Process	TSMC 0.18μm CMOS Mixed-Signal
Supply Voltage	1.5V
Reference Voltage	600.8mV
Temperature Coefficient (0℃~100℃)	37.8 ppm/℃(2.28mV)
PSRR	-41dB at 1kHz
Supply current	6.75μA
Chip Size	0.400mm×0.490mm



(a) Layout



(b) Floor plan

Figure 5.6 Layout and floor plan of the CMOS bandgap reference

5.5 Conclusion

A low-power reference circuit with MOSFETs operated in the weak inversion region is described. The reference output voltage is around 600 mV, and the minimum supply voltage is 1.5V. This circuit is easy to design, and suitable for use in low-voltage, low-power applications.

Chapter 6

Conclusions

6.1 Conclusion

Among many types of CMOS ADC architectures, the pipelined ADC is the most popular approach for high speed and medium accuracy. This popularity is due to the fact that pipelined ADC can achieve high sampling rate as flash ADCs as a result of an S/H circuit in each stage of the pipeline. Also, the pipelined ADC require less silicon area, dissipate less power, and the voltages of the comparators in the sub-converter need to resolve are less stringent than the flash equivalents. In this research, the 10-bit、80 MS/s pipelined ADC has been designed and simulated by the program of Hspice using the standard tsmc 0.18μm CMOS process.

The thesis also has designed the low-power CMOS bandgap reference using the tsmc 0.18μm CMOS process. The bandgap reference uses the MOSFETs operated in the weak inversion to generate the proportional to absolute temperature current instead of using BJTs in CMOS process. Thus the power and silicon are could be reduced. The simulated results show that the temperature coefficient is 37.8ppm/℃ (2.28mV) when the output voltage is 600.8mV at supply voltage of 1.5V.

6.2 Future Work

In order to achieve the higher performance of the pipelined ADC, designing an op-amp with both larger signal swing and larger bandwidth for high dynamic range

and high speed respectively will be a challenging. If we continue to research on the same topic, we will try to use the correlated double-sampling architecture to get the higher operating speed. Also, using correlated double-sampling architecture could reduce gain errors and gain sensitivities. In the other hand, low voltage low-power circuit is the popular research for the future work. Thus scaling down the supply voltage without degrading the performance of the op-amp will be a difficult challenging. Thus, the design of high speed and high resolution of ultra low voltage pipelined ADCs will be the most important area for the future work.

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