Wideband LNA Compatible for Differential and Single-Ended Inputs

Ming-Ching Kuo, *Member, IEEE*, Chien-Nan Kuo, *Member, IEEE*, and Tzu-Chan Chueh

***Abstract*—This letter presents a wideband low-noise amplifier (LNA) that supports both differential and single-ended inputs, while providing differential output. The LNA is implemented in 0.13 μm CMOS technology. For sub-1 GHz wideband applications, this LNA achieves 22.5 dB voltage gain, $+1$ dBm IIP3, and 2.5 dB NF in the differential receiving mode, while achieving 23 dB voltage gain, -0.5 dBm IIP3, and 2.65 dB NF in the single-ended receiving mode. The LNA core circuit draws 2.5 mA from 1.2 V supply voltage, and occupies a small chip area of 0.06 mm^2.**

***Index Terms*—Balun, capacitor cross-coupling (CCC), low-noise amplifier (LNA), noise-canceling, reconfigurable, wideband.**

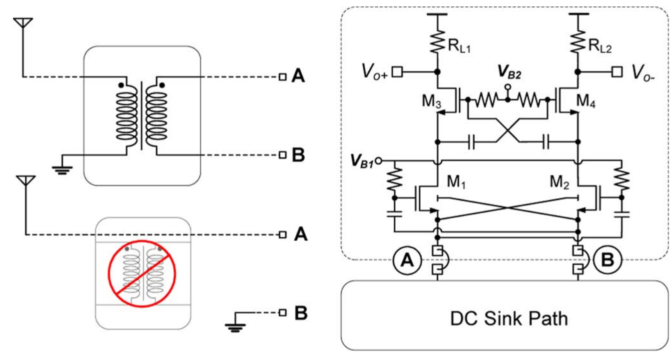

Fig. 1. Single LNA circuit driven from a differential or from a single- ended input signal source.

I. Introduction

DIFFERENTIAL low-noise amplifiers (LNAs) are widely used for their advantages of common-mode disturbance immunity and high dynamic range. However, they usually require external balanced-to-unbalanced (balun) converters, which inevitably raise the bill-of-material (BOM), introduce loss, and degrade gain flatness. On the contrary single-ended (SE) LNAs avoid these issues and consequently benefit in low cost and small area. Nevertheless, they suffer from sensitivity degradation due to the troublesome substrate noise and spurious leakages, especially in a system-on-a-chip (SoC) environment. Furthermore, single-to- differential converters (SDC) following the LNAs are normally needed to provide differential signal to the subsequent mixer. This issue is alleviated by combining the SDC with the SE LNA into a single-stage balun LNA [1]. For the concern of the LNA input, an attractive solution is a single LNA circuit capable of handling both single-ended and differential input configurations flexibly to fulfill the requirements among different standards.

Typically LNAs in RF chips are designed to receive either differential or single-ended inputs, but not both. Supporting both differential and single-ended inputs in LNAs is not common in literature. The difficulty lies in the requirement that in both operation modes circuit design must achieve impedance match, approximately constant gain, low NF, and balanced differential output. One scheme was demonstrated in a 65 nm CMOS tuner [[2], Fig. 4(a)], while requiring an area-consuming on-chip transformer. This letter proposes an LNA topology that accepts differential and single-ended inputs and provides differential output. The LNA presents appropriate input impedance match and maintains substantially constant gain, irrespective of differential or single-ended operation. In particular, the LNA carries out the balun function in the single-ended operation mode so that it needs no bulky transformer and occupies small chip area.

Manuscript received December 22, 2008; revised March 23, 2009. First published June 23, 2009; current version published July 09, 2009. This work was supported by the SoC Technology Center (STC), Industrial Technology Research Institute (ITRI), Taiwan, and by the National Science Council of Taiwan.

M.-C. Kuo is with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan and also with ITRI/STC, Hsinchu, Taiwan (e-mail:mckuo.tw@gmail.com).

C.-N. Kuo is with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan. (e-mail: cnkuo@mail.nctu.edu.tw).

T.-C. Chueh is with the ITRI/STC, Hsinchu, Taiwan (e-mail: zzchuih@itri.org.tw).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LMWC.2009.2022142

II. Proposed LNA Circuit Topology

The integrated circuit schematic of the proposed LNA core is shown within the dashed box in Fig. 1. The core circuit has a symmetric design with identical device dimensions and the same bias condition in the two branches. The LNA core connects to the external input source and DC current sink at nodes A and B. Depending on the type of the sources, the core circuit can either operate in the differential or single-ended receiving mode.

A. Differential Receiving Mode

When the LNA is selected to operate in the differential receiving mode, the circuit presents a balanced response. Both M_1 and M_2 are configured as common-gate (CG) amplifiers. The differential signal from the off-chip balun is AC-coupled to the source nodes of M_1 and M_2, which are connected to the ground through two external large inductors for DC current sink.

The topology is similar to G_m-boosted CG LNAs [3], except the bulk cross-coupling (BCC) connection between M_1 and M_2, as well as the capacitor cross-coupling (CCC) network between M_3 and M_4. In the conventional G_m-boosted CG LNA, gm-boosting is realized by a CCC network between M_1 and

M_2. The input transconductance is doubled without consuming extra DC current due to the fully differential structure with the feed-forward amplification of -1. In the proposed LNA scheme, the input transconductance is further intensified by cascading the effect of BCC and CCC. The BCC configuration successfully turns the transistors M_1 and M_2 into dual-gate operation. This effectively boosts the input transconductance from g_{m1} to $g_{m1} + g_{mb1}$, where g_{mb1} denotes the body transconductance. Consequently, the input transconductance G_{m1} is effectively boosted to $2 \cdot (g_{m_1} + g_{mb_1})$. In this design, g_{mb1} is nearly 0.22 times of g_{m1}, leading to a transconductance boost by 44%. This advantage significantly improves the noise figure and reduces the power consumption as well as the voltage headroom.

Assume an ideal wideband balun of 1:1 is applied. The differential input impedance is transform into single-ended one approximately as

$$Z_{in} \approx \left(\frac{1}{G_{m1}} + \frac{1}{G_{m2}}\right) = \frac{1}{g_{m1} + g_{mb1}}. \tag{1}$$

The differential output voltage gain is derived as

$$A_v = 2 \cdot \kappa_1 \cdot (g_{m1} + g_{mb1}) R_L \tag{2}$$

where the factor $\kappa_1 = 2 \cdot Z_{in}/(R_s + Z_{in})$, equal to unity under the perfect input match condition.

Because the effective input transconductance is further boosted by BCC, the noise factor contributed by M_1 and M_2 is thus reduced by a factor of (g_m/G_m), or 18% if compared with that of the conventional Gm-boosted LNA. The noise factor is derived as

$$F = 1 + \frac{2}{G_m R_s} \cdot \frac{g_m}{G_m} \cdot \frac{\gamma}{\alpha} + \left(\frac{1}{G_m R_s} + \frac{1}{2}\right)^2 \cdot \frac{2R_s}{R_L}. \tag{3}$$

The higher the G_m is, the lower the NF is. However, this might cause significant input impedance mismatch if the G_m is too high. In this work $(g_{m1} + g_{mb1})$ of 25 mS is chosen to trade-off the NF and input return loss.

B. Single-Ended Receiving Mode

When the LNA is selected to operate in the single-ended receiving mode, the circuit appears as a balun LNA. As shown in Fig. 2(b), M_1 constructs a CG amplifier by connecting its source node to the ground via an external inductor (choke), while M_2 constructs a common-source (CS) amplifier by shorting its source node to ground. The circuit topology is similar to the noise-canceling LNA [1], regardless of the BCC and CCC configuration.

The input impedance is dominated by M_1 in the CG branch, approximated as $1/(g_{m1}+g_{mb1})$, and matched to 50 ohm source resistance. As the parallel CS branch provides the same signal amplification with an inverted phase at the output, this LNA configuration naturally achieves wideband single-to- differential conversion under symmetric design. The differential output voltage gain is thus as $A_v = 2 \cdot k_1 \cdot (g_{m1} + g_{mb1}) \cdot R_L$. Note that the LNA achieves the same voltage gain as well as input impedance match in both single-ended and differential modes.

Design consideration for noise performance takes into account contributions from M_1 and M_2. In this balun-configured LNA, M_1 noise can be cancelled at the differential output by the CS amplifier following the design in the noise-canceling LNAs. Nevertheless, the CS transistor still contributes significantly to the overall noise factor, leading to an NF as high as 4 dB. To alleviate this problem, one commonly used scheme in previously published work is transconductance boosting of the CS amplifier. In [1], g_{m2} is chosen 5 times higher than g_{m1} to decrease the noise contribution of M_2. However, this method results in unbalanced circuit branches, inappropriate for differential operation mode.

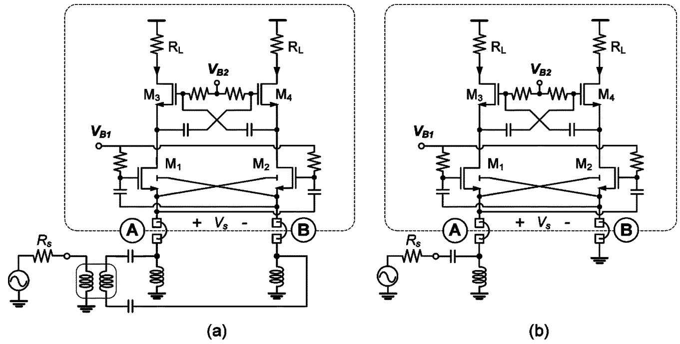

Fig. 2. Proposed LNA operated in (a) the differential receiving mode, and (b) the single-ended receiving mode.

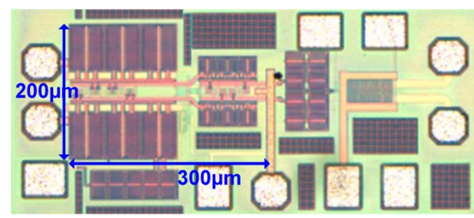

Fig. 3. Die micrograph of the fabricated LNA.

In this proposed LNA, M_2 noise reduction makes use of the CCC network between M_3 and M_4. Circuit balance is therefore sustained. The noise factor contributed by M_2 is effectively reduced by a factor of 0.41 due to this feed-forward configuration [4]. As a result, an NF less than 2.5 dB becomes feasible, even though g_{m2} is the same as g_{m1}.

III. Measured Results

The LNA is fabricated in a 0.13 μm CMOS technology. The die micrograph is shown in Fig. 3. The testkey occupies an area of 300×700 μm^2, while the LNA core is only 200×300 μm^2 excluding the test buffer and pads.

The measurement of the LNA chip is performed by bonding the chip on board. On-chip test buffers, implemented by source followers, are included at the differential output for measurement purpose. All measured performance includes this buffer effect except the item of voltage gain. Table I summarizes the performance of the proposed LNA and some recently published works [5], [6].

The S-parameters are measured using a 4-port network analyzer. The same test setup with single-ended input to differential output is applied to both LNA configurations, i.e., the external balun is included in the differential mode measurement.

TABLE I
PERFORMANCE COMPARISON

Ref.	This Work		[1]	[5]	[3]	[6]
Architecture	Balun	Diff.	Balun	SE	Diff.	Diff.
Freq. [GHz]	0.15-1	0.15-1	0.2-5.2	0.2-2	6	0.1-0.93
A_v Gain [dB]	22-24	22-23.5	13-15.6	10-14	N/A	N/A
S21 [dB]	14.3	14.5	6.6	10-14	7.1	13
NF [dB]	2.5-2.9	2.2-2.9	2.8-3.5	1.9-2.4	3	3.6-4.8
IIP3 [dBm]	-0.5	+1	0	0	+11.4	-10.2
IIP2 [dBm]	+10	+20	+20	+12	N/A	N/A
S11 [dB]	<-10	<-8	<-10	-8	-10	<-8
Supply [V]	1.2	1.2	1.2	2.5	1.8	1.2
Power [mW]	3	3	14	35	6.5	0.72
Technology	0.13µm	0.13µm	65nm	0.25µm	0.18µm	0.13µm
Area [mm²]	0.06	0.06	0.009	0.075	0.95*	0.27

*Including the test pads.

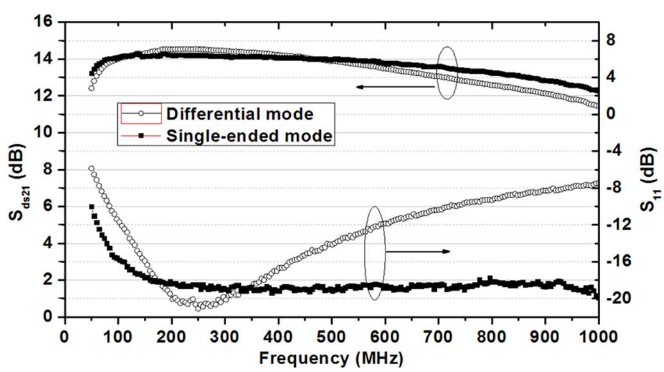

Fig. 4. The measured S-parameters in both operation modes.

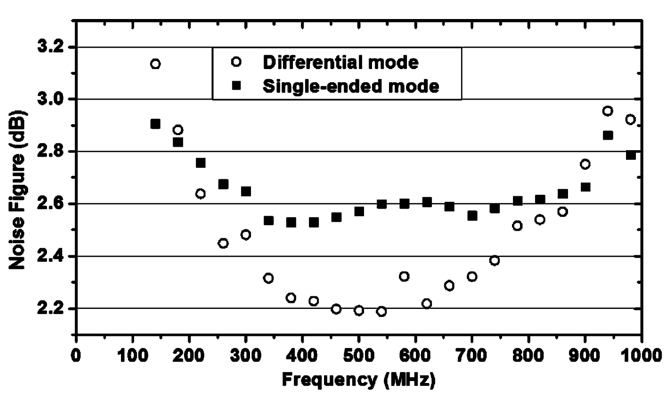

Fig. 5. The measured NF in both operation modes.

As shown in Fig. 4, the S_{11} is below -16 dB from 100 MHz to 1 GHz in SE configuration, while -8 dB in the differential mode due to the effect of the non-ideal external balun. The measured single-ended input to differential output S-parameter gain S_{ds21} is 14.3–12.3 dB in SE mode, while 14.5–11.5 dB in the differential mode after subtracting the balun loss. These results are translated into voltage gain of 23 ± 1 dB and 22.5 ± 1.5 dB in SE and the differential mode, respectively, after de-embedding the effect of the test buffers.

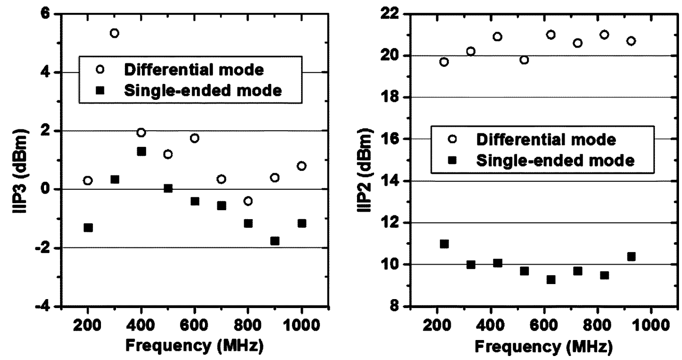

Fig. 6. Measured IIP3 and IIP2 in both operation modes.

Fig. 5 illustrates the measured NF, which is 2.5–2.9 dB with an average value of 2.65 dB in SE mode, while 2.2–2.9 dB with an average 2.5 dB in the differential mode. Fig. 6 depicts the measured IIP2 and IIP3 versus frequency. The IIP3 is measured by applying two tones with 2 MHz spacing, while the IIP2 is measured by two tones with 210 MHz spacing. Across the frequency band of interest, the proposed LNA achieves an average IIP3 of -0.5dBm and $+1$ dBm, and IIP2 of $+10$ dBm and $+20$ dBm in SE and differential mode, respectively.

IV. CONCLUSION

A wideband LNA for sub-1 GHz applications is introduced. The proposed LNA provides great flexibility for the differential and single-ended operation. In both operation modes, the LNA achieves wideband impedance match, high voltage gain, and low NF with low power consumption.

REFERENCES

[1] S. C. Blaakmeer, E. A. M. Klumperink, B. Nauta, and D. M. W. Leenaerts, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, pp. 1341–1350, Jun. 2008.

[2] I. Vassiliou, K. Vavelidis, N. Haralabidis, A. Kyranas, Y. Kokolakis, S. Bouras, G. Kamoulakos, C. Kapnistis, S. Kavadias, N. Kanakaris, E. Metaxakis, C. Kokozidis, and H. Peyravi, "A 65 nm CMOS multistandard, multiband TV tuner for mobile and multimedia applications," *IEEE J. Solid-State Circuits*, vol. 43, pp. 1522–1533, Jul. 2008.

[3] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. P. de Gyvez, D. J. Allstot, and E. Sánchez-Sinencio, "A capacitor cross-coupled common-gate low noise amplifier," *IEEE Trans. Circuits Syst. II: Expr. Briefs*, vol. 52, no. 12, pp. 875–879, Dec. 2005.

[4] M.-C. Kuo, S.-W. Kao, C.-H. Chen, T.-S. Hung, Y.-S. Shih, T.-Y. Yang, and C.-N. Kuo, "A 1.2V 114 mW dual-band direct-conversion dvb-H tuner in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, pp. 950–961, Mar. 2009.

[5] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise cancelling," *IEEE J. Solid-State Circuits*, vol. 39, pp. 275–282, Feb. 2004.

[6] S. B. T. Wang, A. M. Niknejad, and R. W. Brodersen, "Design of a sub-mW 960-MHz UWB CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 41, pp. 2449–2456, Nov. 2006.