Optimization on MOS-Triggered SCR Structures for On-Chip ESD Protection

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***Abstract*—MOS-triggered silicon-controlled rectifier (SCR) devices have been reported to achieve efficient on-chip electrostatic discharge (ESD) protection in deep-submicrometer CMOS technology. The channel length of the embedded MOS transistor in the MOS-triggered SCR device dominates the trigger mechanism and current distribution to govern the trigger voltage, holding voltage, on resistance, second breakdown current, and ESD robustness of the MOS-triggered SCR device. The embedded MOS transistor in the MOS-triggered SCR device should be optimized to achieve the most efficient ESD protection in advanced CMOS technology. In addition, the layout style of the embedded MOS transistor can be adjusted to improve the MOS-triggered SCR device for ESD protection.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection, silicon-controlled rectifiers (SCRs).**

I. Introduction

DUE TO THE lower breakdown voltage of the thinner gate oxide, electrostatic discharge (ESD) threat has become a major reliability concern for CMOS IC products fabricated in the advanced nanoscale CMOS processes [1], [2]. Silicon-controlled rectifiers (SCRs) have been used as on-chip ESD protection devices because of their superior area-efficient ESD robustness [1], [2]. However, SCR has some drawbacks, such as higher trigger voltage (V_{t1}), lower turn-on speed, and latchup concern. Therefore, the low-voltage-triggered SCR was invented to reduce the trigger voltage of SCR device [3]. Moreover, some advanced circuit techniques (the gate-coupled [4], diode-triggered [5], substrate-triggered [6], and GGNMOS-triggered [7] techniques) were also reported to enhance the turn-on efficiency of SCR devices for ESD protection. In addition, the lower holding voltages may suffer latchup failure (if lower than VDD operation voltage) due to external noise triggering under normal circuit operation conditions. Several previous studies had been presented to increase the holding voltage or the trigger current against latchup concern, such as dynamic holding voltage SCR [8], SCR with stacked diode string [6], stacked SCR devices [9], high-current-triggered SCR devices [10], and high-holding low-voltage trigger SCR [11]. Recently, an initial-on ESD protection concept realized with PMOS-triggered SCR device in general CMOS processes was reported [12]. In this paper, further optimizations on the MOS-triggered SCR devices for ESD protection are studied. The modified PMOS-triggered SCR device with merged layout style is proposed to further enhance its ESD protection capability. In addition, NMOS transistors are also embedded into the SCR structures to implement NMOS-triggered SCR devices for ESD protection. These two different MOS-triggered SCR devices are compared to optimize on-chip ESD protection design in CMOS ICs.

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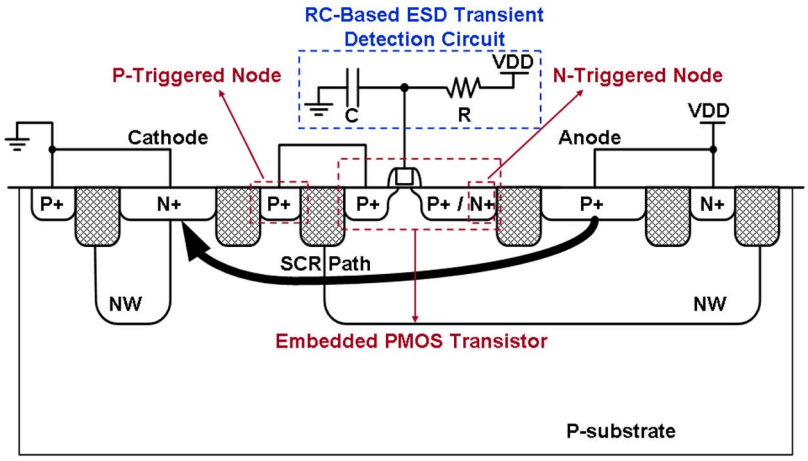
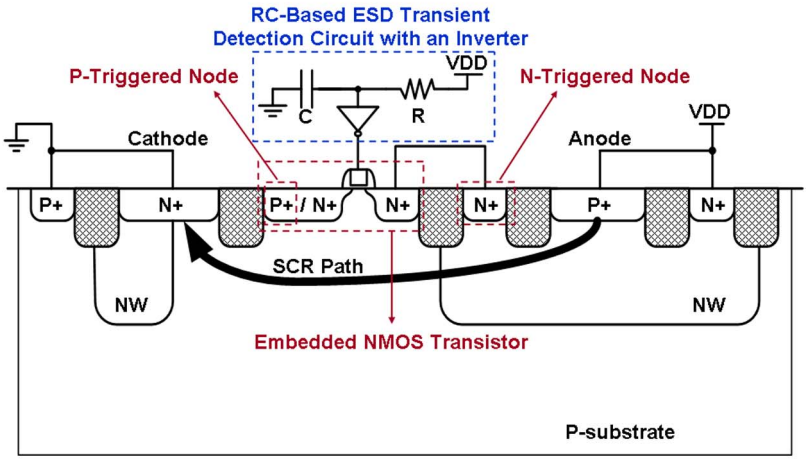
II. SCR Devices With Embedded MOS Transistors

The PMOS-triggered SCR device with embedded PMOS transistor and RC-based ESD transient detection circuit is shown in Fig. 1(a) [12]. A similar SCR structure with embedded MOS transistor had been reported in the previous study [11]. The source and drain terminals of embedded PMOS transistors are, respectively, connected to the n-triggered and p-triggered nodes to synchronously generate double trigger currents into n-well and p-well of the SCR structure. The gate terminal of the embedded PMOS transistor is tied to an RC-based ESD transient detection circuit. Compared to the PMOS-triggered SCR device, the NMOS-triggered SCR device is implemented with an embedded NMOS transistor, as shown in Fig. 1(b). The source and drain terminals of the embedded NMOS transistor are, respectively, connected to the p-triggered and n-triggered nodes. The gate terminal of the embedded NMOS transistor is tied to an RC-based ESD transient detection circuit with an inverter. Due to the difference in the rise times between the ESD pulse and the VDD power-on voltage, the RC time constant in the ESD transient detection circuit is traditionally designed about 0.1–1 μs to distinguish the ESD stress condition from the normal circuit operation condition [13]. To achieve the desirable operation, the RC time constant of the ESD transient detection circuit is designed as 0.4 μs in this paper.

The layout top views of the MOS-triggered SCR devices are shown in Fig. 2(a) and (b). With the three different channel lengths (L) in the embedded MOS transistors, the anode-to-cathode spacings are therefore different in the MOS-triggered SCR devices. They are 6.8, 7.0, and 7.25 μm in the MOS-triggered SCR devices with channel lengths of 0.3, 0.5, and 0.75 μm in the embedded MOS transistors, respectively. The MOS-triggered SCR device with merged layout style is



(a)



(b)

Fig. 1. Cross-sectional views of (a) the PMOS-triggered SCR device with RC-based ESD transient detection circuit and (b) the NMOS-triggered SCR device with RC-based ESD transient detection circuit and an inverter.

also implemented in this paper. The p-triggered node (or the n-triggered node) was directly merged into the drain side of the embedded PMOS transistor (or the embedded NMOS transistor) and located across the junction between n-well and p-well. The layout top views of the MOS-triggered SCR devices with shorter anode-to-cathode spacing are shown in Fig. 3(a) and (b). This shorter anode-to-cathode spacing is only 5.1 μm when the embedded MOS transistor has a channel length of 0.3 μm. The device widths of all MOS-triggered SCR devices are kept the same at 50 μm, which have been fabricated in a 0.18-μm fully silicide CMOS process.

III. Experimental Results

A. DC Characteristics

During the normal circuit operation condition with VDD (1.8 V) and VSS (0 V) biases, the gate terminals of embedded PMOS and NMOS transistors were biased at VDD and VSS, respectively, to keep themselves off. In this paper, the dc I–V characteristics of all SCR devices are measured by Curve Tracer (Tek 370A) with the dc mode. According to the measured dc I–V curves of the MOS-triggered SCR devices with different channel lengths in the embedded MOS transistors (original layout style), the dc trigger voltage (V_{t1}) and holding voltage (V_h) of PMOS-triggered SCR devices with 0.3-μm (0.5- and 0.75-μm) channel length are 7.30 V (7.61 and 7.83 V) and 2.82 V (3.00 and 3.12 V), respectively. On the other hand, the NMOS-triggered SCR devices with 0.3-, 0.5-, and 0.75-μm channel lengths have the V_h of 3.28, 3.63, and 3.75 V, respectively, with the corresponding V_{t1} of 6.50, 7.17, and 7.19 V. The V_{t1} and V_h are increased by increasing the channel length of the embedded MOS transistor. Moreover, the V_{t1} of the MOS-triggered SCR device with merged layout style is similar to that with original layout style. The merged layout style can slightly reduce the V_h of MOS-triggered SCR devices due to the shorter anode-to-cathode spacing in the layout. The dc V_{t1} and V_h of PMOS-triggered and NMOS-triggered SCR devices were listed in Table I. The difference in V_{t1} between the NMOS-triggered and PMOS-triggered SCR devices can be attributed to the different drain breakdown voltages of NMOS and PMOS transistors. The influence of the embedded PMOS and NMOS transistors on V_h of SCR devices will be further discussed in the next section.

B. Turn-On Verifications

In order to observe the turn-on efficiency of MOS-triggered SCR devices with different channel lengths in the embedded

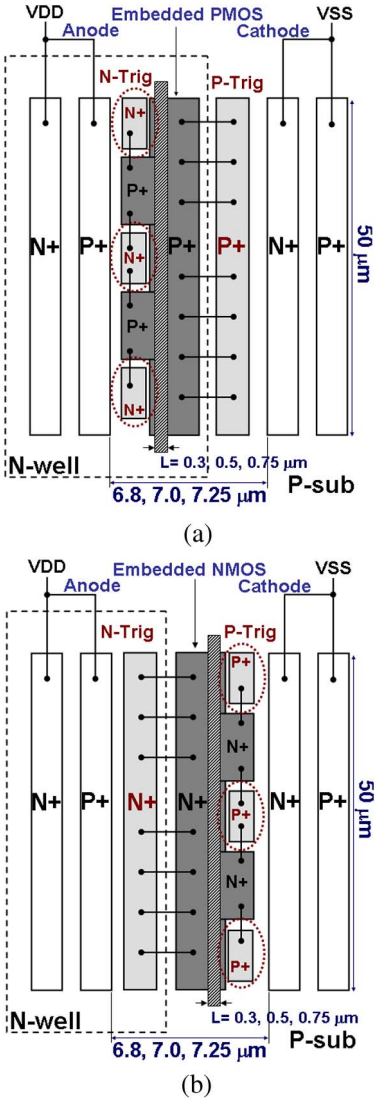


Fig. 2. Top views of (a) the PMOS-triggered and (b) the NMOS-triggered SCR devices with three different channel lengths of 0.3, 0.5, and 0.75 μm in the embedded MOS transistor (original layout style).

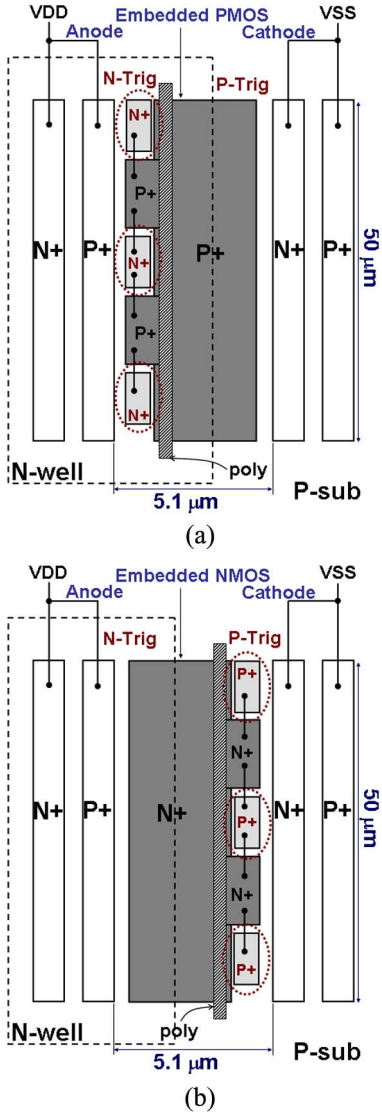


Fig. 3. Top views of (a) the PMOS-triggered SCR device and (b) NMOS-triggered SCR device with merged layout style. Both anode-to-cathode spacings of PMOS-triggered and NMOS-triggered SCR devices are only 5.1 μm.

PMOS and NMOS transistors, a 5-V ESD-like voltage pulse with a fast rise time of 2 ns was applied to each VDD node (anode) of the MOS-triggered SCR device with its VSS node (cathode) grounded. The rise time of Human-Body-Model (HBM) ESD event is about 2–10 ns [14]. The voltage pulse with a rise time of 2 ns generated from a pulse generator is used to simulate the fast-rising edge of the HBM ESD event. The sharp-rising edge of the ESD-like voltage pulse will be detected by the RC-based ESD transient detection circuit to trigger on the MOS-triggered SCR devices. When the MOS-triggered SCR device is turned on, the voltage waveform on VDD node will be clamped down as the measured waveforms shown in Fig. 4(a) and (b). The PMOS-triggered SCR device (original layout style) with 0.3-μm channel length in the embedded PMOS transistor can efficiently clamp the overshooting ESD voltage pulse to a lower voltage level, as shown in Fig. 4(a). However, all of the NMOS-triggered SCR devices (original layout style) with 0.3-, 0.5-, and 0.75-μm channel lengths present better turn-on efficiency to clamp the overshooting pulse to a much lower voltage level. Due to the larger driving capability in the embedded NMOS transistor, the NMOS-triggered SCR devices exhibit better turn-on efficiency, as shown in Fig. 4(b).

C. TLP I–V Characteristics and ESD Robustness

The TLP [15] I–V curves of the MOS-triggered SCR devices with different channel lengths and layout styles in the embedded PMOS or NMOS transistors were measured in Figs. 5(a) and (b) and 6(a) and (b), respectively. The trigger voltages (V_{t1}) of PMOS-triggered SCR devices are decreased from $\sim$5.12 to $\sim$3.50 V when the embedded PMOS transistors are drawn with reduced channel lengths from 0.75 to 0.3 μm, whereas those of the NMOS-triggered SCR devices are also decreased from $\sim$2.98 to $\sim$2.47 V by decreasing the channel lengths from 0.75 to 0.3 μm. The shorter channel lengths in the embedded MOS transistors can generate the higher trigger currents to reduce the V_{t1} of the MOS-triggered SCR devices. The holding voltages (V_h) are decreased from $\sim$3.38 to $\sim$2.81 V by decreasing the channel lengths from 0.75 to 0.3 μm in the embedded PMOS transistors, and those are similarly decreased

TABLE I
DEVICE CHARACTERISTICS OF PMOS-TRIGGERED AND NMOS-TRIGGERED SCR DEVICES WITH THREE DIFFERENT CHANNEL LENGTHS IN EMBEDDED MOS TRANSISTORS AND TWO DIFFERENT LAYOUT STYLES

Device Characteristics		Original Layout Style						Merged Layout Style	
		L= 0.3 μm		L= 0.5 μm		L= 0.75 μm		L= 0.3 μm	
		PMOS-Triggered	NMOS-Triggered	PMOS-Triggered	NMOS-Triggered	PMOS-Triggered	NMOS-Triggered	PMOS-Triggered	NMOS-Triggered
DC	Vt1	7.30 V	6.50 V	7.61 V	7.17 V	7.83 V	7.19 V	7.30 V	6.48 V
	Vh	2.82 V	3.28 V	3.00 V	3.63 V	3.12 V	3.75 V	2.35 V	2.88 V
TLP	Vt1	3.50 V	2.47 V	4.41 V	2.72 V	5.12 V	2.98 V	3.40 V	2.44 V
	Vh	2.81 V	2.36 V	3.10 V	2.56 V	3.38 V	2.68 V	2.40 V	2.28 V
	Ron	2.71 Ω	2.60 Ω	3.28 Ω	2.81 Ω	3.31 Ω	2.78 Ω	2.40 Ω	2.13 Ω
	It2	3.05 A	2.67 A	3.51 A	2.71 A	3.92 A	2.78 A	4.17 A	4.22 A
ESD Level	HBM	5.0 kV	4.0 kV	6.5 kV	4.5 kV	6.5 kV	4.5 kV	7.0 kV	7.0 kV
	MM	200 V	150 V	250 V	200 V	300 V	200 V	350 V	350 V

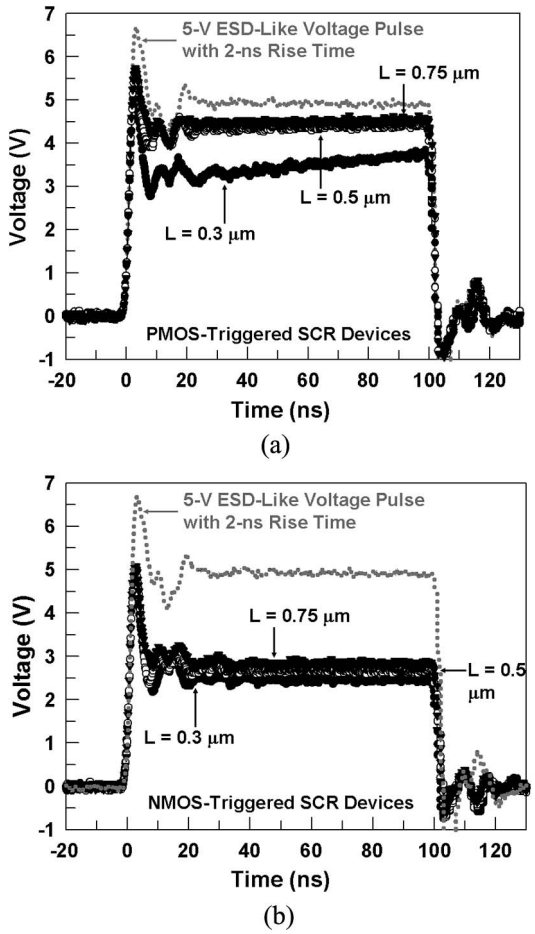


Fig. 4. Under 5-V ESD-like voltage pulses with 2-ns rise time, the clamped voltage waveforms by (a) the PMOS-triggered SCR devices and (b) the NMOS-triggered SCR devices, under three different channel lengths in the embedded MOS transistors (original layout style).

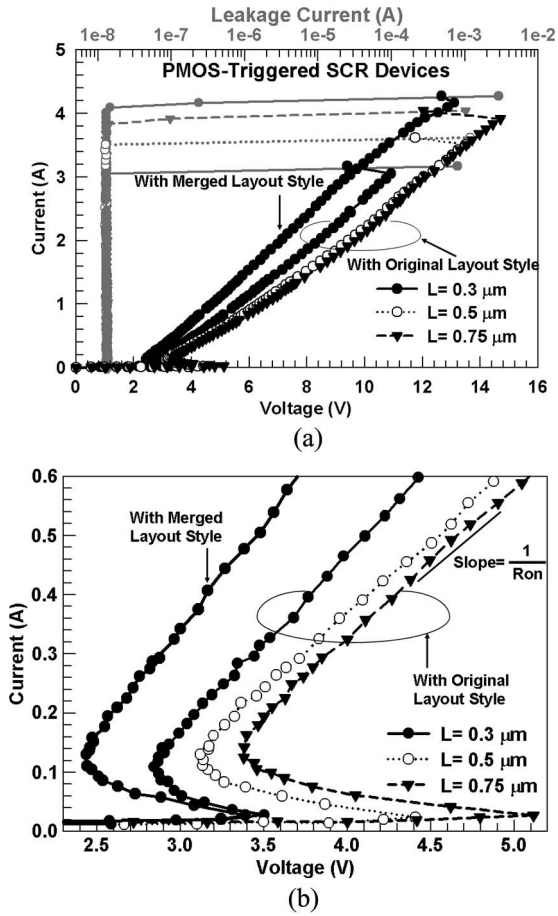


Fig. 5. (a) TLP-measured I–V curves of the PMOS-triggered SCR devices with different channel lengths and different layout styles in the embedded PMOS transistors. (b) Zoomed-in view of (a) around the low-current range.

from ∼2.68 to ∼2.36 V by decreasing the channel lengths in the embedded NMOS transistors. The on resistances ($R_{\rm on}$), which are extracted from the TLP-measured I–V curves, of the PMOS-triggered (NMOS-triggered) SCR devices with 0.3-, 0.5-, and 0.75-μm channel lengths in the embedded PMOS transistors (NMOS transistors) are 2.71, 3.28, and 3.31 Ω (2.60, 2.81, and 2.78 Ω), respectively, as listed in Table I.

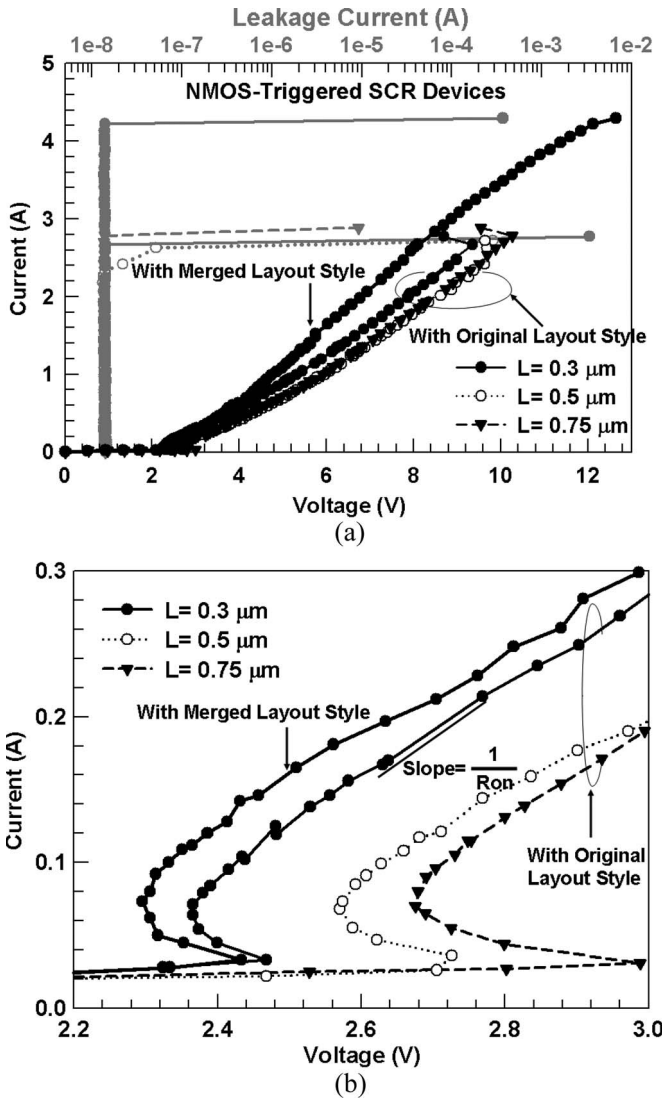


Fig. 6. (a) TLP-measured I–V curves of the NMOS-triggered SCR devices with different channel lengths and different layout styles in the embedded NMOS transistors. (b) Zoomed-in view of (a) around the low-current range.

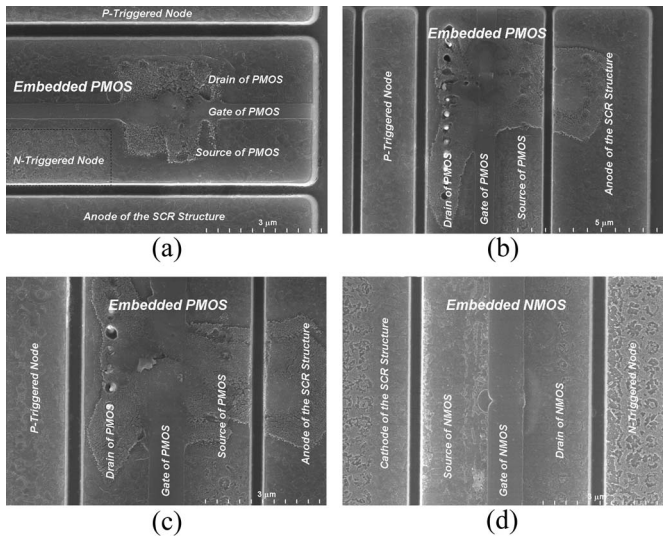


Fig. 7. (a) Failure spot is located at the embedded PMOS transistor in the PMOS-triggered SCR device with 0.3-μm channel length. [(b) and (c)] Failure spots are located at the anode to embedded PMOS transistors in the PMOS-triggered SCR devices with 0.5- and 0.75-μm channel lengths. (d) Failure spot is located at the embedded NMOS transistor in the NMOS-triggered SCR device with 0.75-μm channel length.

In Figs. 5(a) and (b) and 6(a) and (b), each leakage current is measured under the bias of 1.8-V VDD. The second breakdown currents (I_{t2}'s) are increased from ~3.05 to ~3.92 A (from ~2.67 to ~2.78 A) by increasing the channel lengths from 0.3 to 0.75 μm in the PMOS-triggered (NMOS-triggered) SCR devices. In addition, the HBM (Machine Model, MM [16]) ESD robustness of the PMOS-triggered SCR devices with 0.3-, 0.5-, and 0.75-μm channel lengths are 5.0 kV (200 V), 6.5 kV (250 V), and 6.5 kV (300 V), respectively. They are 4.0 kV (150 V), 4.5 kV (200 V), and 4.5 kV (200 V) in NMOS-triggered SCR devices, as listed in Table I. Although the NMOS-triggered SCR devices have lower V_h and $R_{\rm on}$, all of the PMOS-triggered SCR devices have higher ESD robustness and I_{t2}. The reasons will be attributed to the different failure mechanisms in PMOS-triggered and NMOS-triggered SCR devices. Overall, the MOS-triggered SCR device with merged layout style has a lower V_h, a smaller $R_{\rm on}$, and a higher I_{t2} due to a shorter anode-to-cathode spacing and higher turn-on efficiency. The I_{t2} of PMOS-triggered (NMOS-triggered) SCR device with merged layout style achieves 4.17 A (4.22 A), which is over 1 A higher than that with the original layout style, as shown in Figs. 5(a) and 6(a). The HBM (MM) ESD robustness of the PMOS-triggered and NMOS-triggered SCR devices with merged layout styles are 7.0 kV (350 V) and 7.0 kV (350 V), respectively, in Table I.

IV. Failure Analysis and Discussion

A. Failure Analysis

The failure spot investigated by SEM image is located at the embedded PMOS transistor in the PMOS-triggered SCR device with 0.3-μm channel length, as shown in Fig. 7(a). However, the failure spots are located at the anode diffusions of PMOS-triggered SCR devices with 0.5- and 0.75-μm channel lengths, as shown in Fig. 7(b) and (c). The embedded PMOS transistor with shorter channel length of 0.3 μm causes the crowding ESD currents nearby the embedded PMOS transistor and generates the huge local joule heat to destroy the embedded PMOS transistor. In addition, the embedded PMOS transistor with shorter channel length has the lower channel resistance to conduct the huge ESD current through the surface channel of the PMOS transistor to burn out itself. On the other hand, since the driving capability of the NMOS transistor is higher than that of the PMOS transistor, the failure spots on all NMOS-triggered SCR devices are located in the embedded NMOS transistors after 5-kV HBM ESD stresses, as shown in Fig. 7(d). The embedded NMOS transistors conduct huge ESD currents, and the local joule heat is produced to damage the embedded NMOS transistor from drain to source. Such a failure mechanism can explain that the ESD robustness of NMOS-triggered SCR devices was not increased by increasing the channel lengths of embedded NMOS transistors.

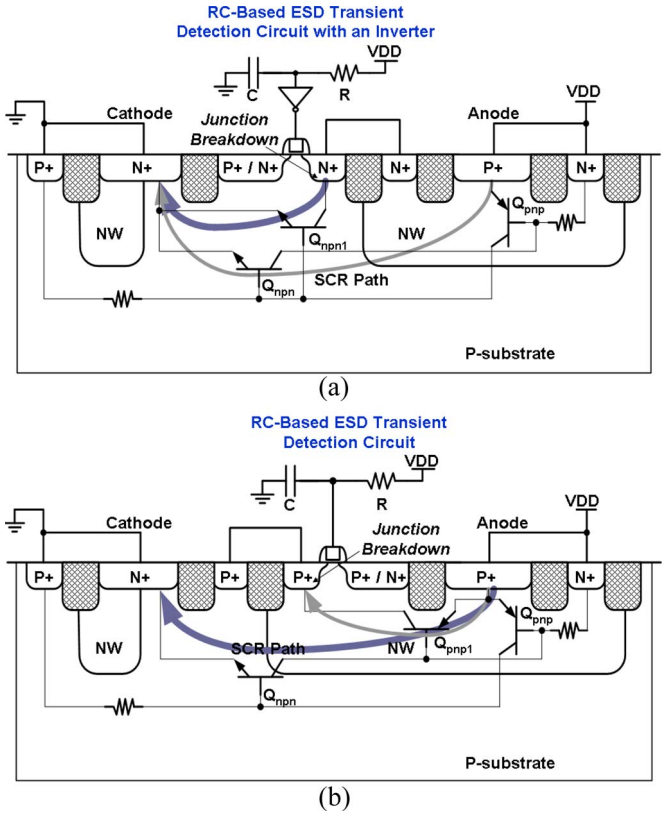


Fig. 8. Turn-on mechanisms of (a) NMOS-triggered SCR device and (b) PMOS-triggered SCR device under dc measurement with the embedded MOS transistors in OFF state.

B. Discussion

According to the previous work [17], the holding voltage (V_h) of the SCR device under dc measurement was much lower than that of the same SCR device under TLP measurement. However, a different measured result has been observed in the NMOS-triggered SCR devices in this paper. The V_h of the NMOS-triggered SCR device under dc measurement is obviously higher than that under TLP measurement. However, the V_h of the PMOS-triggered SCR device under dc measurement is slightly lower than that under TLP measurement. The major mechanism of this abnormal phenomenon can be attributed to the different parasitic structures in these two MOS-triggered SCR devices, as shown in Fig. 8(a) and (b). When the gate terminal of the embedded NMOS transistor was biased at VSS, the drain-bulk junction breakdown of the embedded NMOS transistor in the NMOS-triggered SCR device would be induced under dc measurements with overstress voltage. The additional parasitic n-p-n bipolar transistor $(Q_{\rm npn1})$, which is formed by the drain-side N^+ diffusion, p-substrate, and the cathode of the NMOS-triggered SCR device, will be triggered on to conduct main currents under dc measurement, as shown in Fig. 8(a). The V_h of the NMOS-triggered SCR devices was dominated by the parasitic n-p-n bipolar transistor under dc measurement. However, such parasitic n-p-n bipolar transistor does not exist in the PMOS-triggered SCR devices. The anode of the PMOS-triggered SCR device, the n-well, and the drain-side P^+ diffusion also construct another additional parasitic p-n-p bipolar transistor $(Q_{\rm pnp1})$, as shown in Fig. 8(b). Since the beta gain (β) of this parasitic lateral $Q_{\rm pnp1}$ is very small, the V_h of the PMOS-triggered SCR devices is still determined by the SCR path. In addition, no junction breakdown occurs in the MOS-triggered SCR devices under TLP measurements. The embedded MOS transistors can be turned on to produce the triggering currents into n-well and p-substrate; therefore, the SCR devices will be rapidly triggered on during TLP measurement. The V_h of the MOS-triggered SCR devices are ruled by the SCR paths under TLP measurement.

V. Conclusion

The device characteristics of SCR devices with different embedded PMOS and NMOS transistors have been compared and investigated in this paper. The turn-on efficiency, such as V_{t1}, V_h, and $R_{\rm on}$, of the MOS-triggered SCR devices is enhanced by decreasing the channel lengths in the embedded MOS transistors. However, the I_{t2} and ESD robustness of the MOS-triggered SCR devices are increased by increasing the channel lengths, particularly in the PMOS-triggered SCR devices. In addition, the embedded MOS transistor with merged layout style can obviously improve I_{t2} and ESD robustness of the MOS-triggered SCR devices without any sacrifice of the turn-on efficiency, which will be more suitable for ESD protection in nanoscale CMOS technology. Moreover, the obvious differences on the V_h of NMOS-triggered SCR devices under dc and TLP measurements have been attributed to the current distributions through the additional parasitic n-p-n bipolar transistor in the SCR device structure.

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