國立交通大學

電信工程學系碩士班

碩 士 論 文

應用於藍芽系統之超低電壓(0.7V)

可調增益低雜訊放大器及混頻器設計

Design of Ultra Low Voltage (0.7V) Variable-Gain LNA and Mixer for Bluetooth Application

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指導教授：周復芳　博士

中 華 民 國 九 十 四 年 六 月

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中文摘要

在此篇論文研究中，主要探討兩個主題：第一個主題是設計一個偏壓於 0.7 伏特的完全積體化 CMOS 低雜訊放大器，為了偏壓於 0.7 伏特且減少面積的消耗，電路的架構選擇 P 型的折疊式組態。由於電路的偏壓十分的低，電晶體能電壓擺幅有限，故電路在輸出級加入一個源極隨耦器以提升整體電路的線性度。電路採用 on-wafer 量測方式，量測結果不如預期，在 7.28mW 的功率損耗下只有 2.2dB 的增益以及 6.2dB 的雜訊指數，其原因主要來自於輸入端的匹配發生嚴重頻率漂移，此原因將於論文中做討論。第二個主題是設計一個偏壓於 0.7 伏特的完全差動型態 CMOS 雙平衡式混頻器，由於混頻器的中頻選擇 2MHz，電路選擇 P 型的折疊式組態減少 1/f 對電路的影響，也由於使用折疊式組態，混頻器的轉導級電流以及開關級電流能夠彼此獨立以達到更佳的電路特性，此電路在 LC tank 部份做了一些改進，將兩組獨立的 tank 改為一組相關的 tank 以減少所需的電感值以減少面積的損耗。我們採用電路板量測方式而其中的差異將於論文中探討。以上兩組晶片皆以台積電 CMOS 0.18um 的製程實現並完成量測和模擬比較。

Design of Ultra Low Voltage (0.7V) Variable-Gain LNA and Mixer for Bluetooth Application

Student: Po-Da Chen Advisor: Dr. Christina F. Jou

Institute of Communication Engineering

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Abstract

This thesis contents two works. First, we design a 0.7V fully integrated CMOS LNA. We choose the PMOS type folded cascode configuration for such low voltage application and to reduce the chip size at the same time. Because the operating voltage is very low, the voltage swing for the transistors is quite small. Thus, we add a source follower before the output port to increase the linearity. The circuit is designed for on-wafer testing, and the measurement results are not as expected. The forward gain is 2.2dB, the noise figure is 6.2dB and the power consumption is 7.27mw. The major reason is due to the frequency shifting of the S_{11} parameter, which will be discussed in the thesis. The second work is the design of a 0.7V fully differential double-balanced mixer. The IF of the mixer is chosen as 2MHz that is close to the corner of the flicker noise. Therefore, the use of the PMOS type folded cascode configuration can reduce the noise contribution of the switching stage that improves the performance of the mixer. Another advantage is the circuit of the transconductance stage and switching stage is independent that we can achieve better circuit performance. In this circuit, we do a modification on the LC tank. We design a

dependent LC tank instead of two independent LC tanks. This modification could make the inductor smaller than before. The circuit is designed for on-board testing and the difference between measurement and simulation results will be discussed. The two IC have been fabricated by the TSMC 0.18um CMOS process technology.

Acknowledgement

首先，我要感謝我的指導教授周復芳老師當年願意收我為他的研究生，讓我有這機會在 919 這充滿人情味的實驗室裡學習成長，並謝謝她這兩年來的細心且開通指導和不曾間斷過的關心，提供我們非常良好的學習環境和實驗室設備，讓我的學習及研究能更加順利。

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Chapter 1
Introduction

1.1 Background and Motivation

The Bluetooth standard defines short-range wireless connection between mobile phone, mobile PCs and other portable devices. The radio band used by Bluetooth is the Industrial, Scientific and Medical (ISM) band ranging from 2.4GHz to 2.483GHz. It specifies a 2.4 GHz frequency-hopped spread-spectrum system that enables the users to easily connect to a wide range of computing and telecommunication devices without the need for wires or cabling of any kind. The modulation scheme employed is Gaussian frequency shift keying (GFSK) with an instantaneous bit rate of 1Mb/s [1].

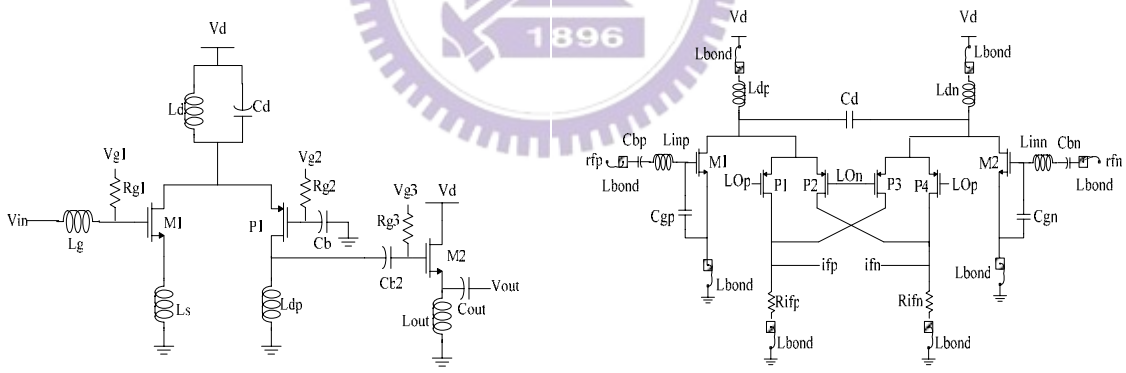
In the recent years, the low-power, low-cost and high integration have become the trend for the communication ICs. Since the base band digital signal processor (DSP) is typically implemented within a CMOS technology, we should put effort toward implementing the high-frequency analog front-end components within the CMOS environment. With great development in CMOS process, modern CMOS technology has accommodated for applications at high frequency. The threshold voltage of the modern $0.18\,um$ CMOS transistors is down to 0.5V and its cut-off frequency is higher than 50GHz. Thus, CMOS technology can offer a higher level of integration that the cost could be cut down and has the ability of operating at relatively low supply voltages [2].

Low power is influenced by the chosen architecture. Three different architectures are commonly used in receiver design: high-IF, low-IF and direct-conversion architectures [3]. A high-IF receiver improves the demodulator performance, but it requires off-chip components and complex IF band circuits that cause more power consumption. Meanwhile, the direct-conversion architecture has the problems such as dc offset, I/Q mismatch, self-mixing, power amplifier pull, flicker noise, etc., have been compromised to achieve acceptable system performance. Thus, the low-IF architecture is more appropriate for low power design, especially when considering the relaxed image rejection requirement in the Bluetooth standard [4]. The choice of the IF is involved in many design tradeoffs. The IF with 1 MHz [5], 2 MHz [6-8], and 3 MHz [9] were implemented. The high IF (3 MHz or above) raises the power dissipation of the IF blocks. While an IF of 1 MHz is difficult to remove the dc offset and image signal since they are closer to the desired channel [7]. Therefore, an IF of two times the channel bandwidth is chosen,i.e., 2 MHz, that the desired signal will well beyond the flicker noise corner.

Lowering the supply voltage is another effective way of reducing the power consumption of mobile communication applications. However, the supply voltages of some RF CMOS receivers have been reported between 0.8V-3V [4-12]. For the next generation of wireless systems, the RF CMOS receiver will have to operate at a supply voltage below 1V. As a result, we try to implement a low-IF Bluetooth receiver with supply voltage of 0.7V. So this thesis contains two major works, including a fully integrated low voltage variable-gain LNA and a modified low voltage mixer. All of them are fabricated using TSMC $0.18um$ CMOS technology process and can be easily integrated with other blocks like synthesizer and filters in the future. In the subsequent sections, we will introduce our circuits and organization of this thesis.

1.2 Designed Circuits Introduction

In this thesis, we design a low voltage variable-gain LNA and a low voltage mixer for 2.45 GHz application. Both of them are designed in the PMOS type folded cascode topology to reduce the supply voltage and chip size. The LNA is one of the most critical building blocks in the modern integrated RF receiver. The main function of the LNA is to provide enough gain to overcome the noise of subsequent stages while maintain low noise. And the function of gain variation is added to prevent the receiver get saturated. The low voltage variable-gain LNA is shown in Fig.1.1(a). The mixer dominated the overall dynamic range of the receiver. Thus, the main function of the mixer is the frequency down (up) conversion and obtains high linearity. The modified low voltage mixer is shown in Fig.1.1(b).



(a) (b)

Fig.1.1 The schematic of (a) Low voltage variable-gain LNA

(b) Low voltage mixer

All the simulation and measurement results of the two circuits are shown in Table 1.1 (low voltage variable-gain LNA) and Table 1.2 (low voltage mixer), respectively. Comparison between this work and recent papers are listed in the table,

too. The difference between simulation and measurement and performance comparison with other papers would be discussed in detail in section 2.5 and in section 3.5.

REF	[16] 2002	[22] 2003	[23] 2003	[24] 2003	[25] 2004	This work 2005.06	
Supply voltage (V)	1	1	1	1.8	1.8	0.7	0.7
S21(dB)	15	23.0	11.6	23.1	15	2.21	17.5
S11(dB)	-51.4	-16.8	-5.1	-5.8	-14	-4.35	-15.0
S22(dB)	-34	-10.2	NA	NA	NA	-10.14	-21.3
S12(dB)	-37.5	-51.7	NA	-25.9	NA	-39.16	-38.6
NF(dB)	3.23	3.8	2.3	4.5	2.2	6.22	1.90
P1dB(dBm)	NA	NA	-7.9	-20.8	NA	-3	-21.5
IIP3(dBm)	-1	-9.1	NA	-15	3	8	-11
Power(mw)	9.85	13	14.2	36	7.2	7.27	7.27
Condition	Sim.	Meas.	Meas.	Meas.	Sim.	Meas.	Sim.

Table 1.1 Comparison of resent LNA papers

REF	[28] 2004	[34] 2004	[35] 2003	[36] 2003	[37] 2004	This work 2005.06	
Supply voltage (V)	1.5	1	1	1.8	1.8	0.7	0.7
IF (MHz)	100	1	2	1	20	2	2
Voltage gain (dB)	3.3	11.9	3.5	13.3	9.33	0.91	6.83
IIP3(dBm)	5.5	-3	-1	-1	1	10	8
NF (dB)	15	14	14	16	8.53	NA	9.13
Power(mw)	5.6	3.2	1.4	36	2.88	2.11	1.84
Condition	Sim.	Meas.	Sim.	Meas.	Meas.	Meas.	Sim.

Table 1.2 Comparison of recent mixer papers

The front-end circuit is simulated by the harmonic balance tools Eldo-RF. These two IC have been fabricated using TSMC 0.18um CMOS technology process through Chip Implementation Center (CIC). The on-wafer testing measurement results and PCB on-board measurement results have been also accomplished at CIC.

1.3 Thesis Organization

This work discusses about the front-end circuit design and implementation for Bluetooth applications. The contents consist of two major topics: “0.7V 2.45GHz Variable-Gain Low-Noise Amplifier” and “0.7V 2.45GHz mixer”, respectively in Chapter 2 and Chapter 3. We will present the design flow and experimental results. Moreover, we will discuss the reasons of differences between simulation and measurement results.

In Chapter 2, we will present the design and implementation of a low voltage variable-gain LNA. The LNA is the main block determined the noise performance of the whole receiver front-end circuit. We will discuss the configuration, variable gain mechanism, input/output matching, noise, and linearity of the LNA in this chapter.

In Chapter 3, we will present the design and implementation of a low voltage mixer. The mixer is the main block determined the dynamic range of the whole receiver front-end circuit. We will discuss the configuration, gain, linearity, and noise of the low voltage mixer in this chapter.

In chapter 4, we will make a conclusion and discuss the future work.

Finally, the appendix presents a concurrent dual-band receiver (LNA plus mixer). Because the circuit does not tape out, we only show the simulation results. And this circuit will be implemented by our lab’s juniors.

Chapter 2
0.7V 2.45GHz Variable-Gain Low-Noise Amplifier

This chapter presents a 0.7V variable-gain LNA designed and fabricated in TSMC 0.18 μm CMOS process. We will discuss the topology selection, design of input matching network, analysis of noise figure and linearity, and the variable gain mechanism in the low voltage LNA. The measurement results show that the LNA only provide a gain of 2.2dB, noise figure of 6.2dB, and IIP3 of 8dBm at the high gain mode. The gain and linearity release can achieve to 6.5dB and 7dBm. Then, the discussion of the difference between simulation and measurement results and the comparisons of other low voltage LNA papers will be in the last section.

2.1 Introduction

The low-noise amplifier (LNA) is the first stage in the receiver shown in Fig. 2.1. Usually, it directly follows the filter inserted between the antenna and the LNA, and its output drive the mixer (or the image reject filter between the LNA and the mixer). When the gain of the first stage is larger, the noise of the subsequent stage is reduced more. As a result, the noise performance is mainly determined by the first stage. Therefore, the main function of the LNA is to provide enough gain to overcome the noise of subsequent stages while maintain low noise. Providing a 50 Ω input impedance to terminate an unknown length of transmission line which delivers signal from the antenna to the amplifier is another important character. Finally, to prevent saturation of the receiver when the input signal is too large, the function of variable

gain is necessary. Thus, as so many considerations should be take into account, the design of LNA must be very carefully and completely.

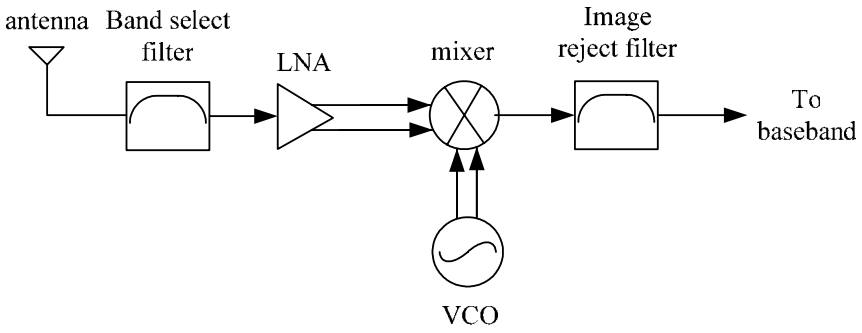


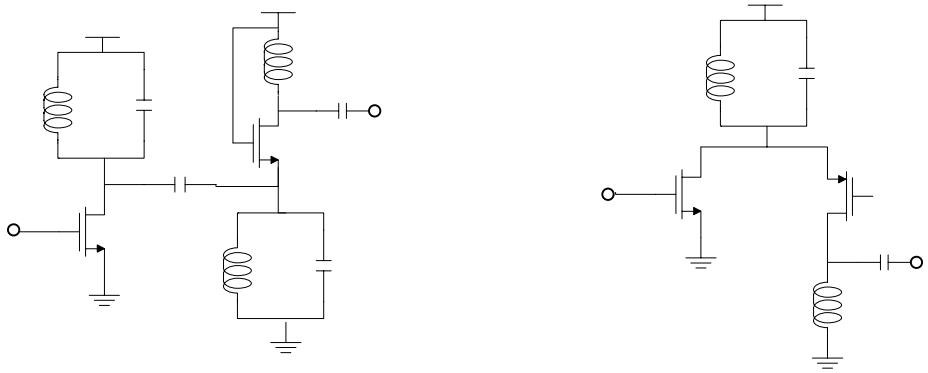
Fig.2.1 Block diagram of RF receiver

2.2 LNA Design

At first sight, the LNA might be simple to design due to the relatively few components used in its implementation. However, LNA design is full of tradeoffs between optimum gain, low noise figure, input and output matching, linearity and power consumption. Generally, the LNA offers the highest gain and lowest NF in the high gain mode for the weak signal. But under strong received signal conditions, the LNA and the whole receiver may get saturated, thereby the LNA has to operate in the low gain mode to prevent saturation. Gain reduction in LNA can also reduce the dynamic range of the Automatic Gain Control (AGC), which is implemented in the IF after the down-conversion mixer. With the reduced dynamic range of the AGC, the SNR performance can be improved [13].

Conventional cascode configuration for LNA have many advantages such as enhance the gain, port to port isolation, stability and reduced Miller effect. But it is not suitable for low voltage design because two transistors stacked between the supply

rails. In order to be able to operate from a very low voltage supply and retain the advantages of the conventional cascode configuration, a folded cascode configuration is used as shown in Fig.2.2. The folding of the common gate stage helps to extend the cutoff frequency of the common source stage. Since it eliminates one level of transistor stacking, the supply voltage is only needed to bias a single transistor in the saturation region. Therefore, the supply voltage of the LNA can be reduced under 1V for the transistors to be biased in the saturation region. Folded cascode configuration have two types, PMOS type [12,14-16] and NMOS [17-18]type. It is obvious that NMOS type needs two LC tank networks, one more than PMOS type. Because the common gate stage acts as an current buffer and does not provide power gain for LNA, PMOS can achieve almost the same performance as NMOS. In order to save the die area, PMOS type is the common choice in recent research. And folded cascode configuration has another advantage that two transistors can be biased independently. The first stage can be biased to provide low noise figure and the second stage can be biased at different dc current to minimize the Miller effect.



(a) NMOS type (b) PMOS type

Fig.2.2 Two types of the folded cascode configuration

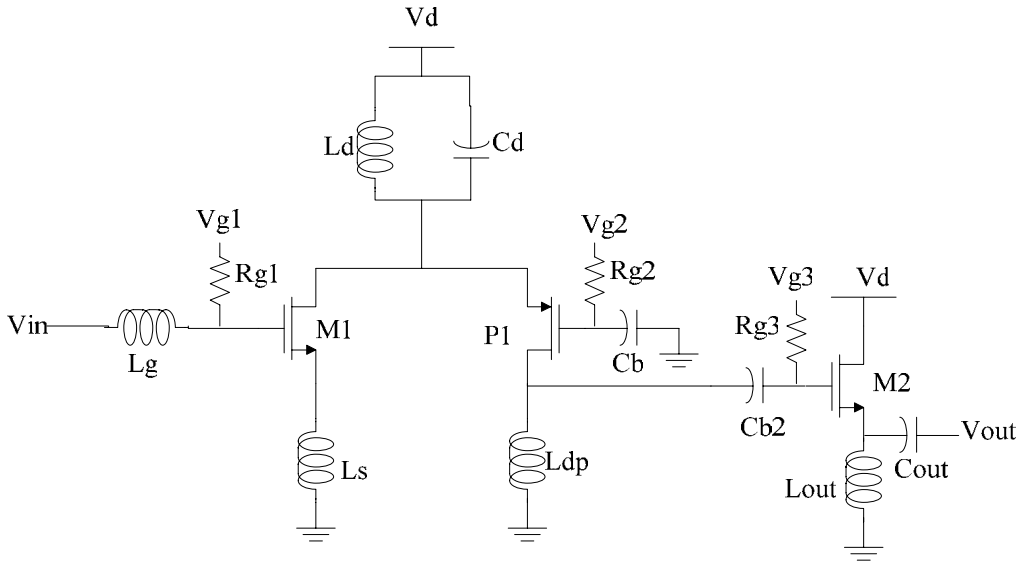


Fig.2.3 Architecture of ultra low voltage variable-gain LNA

The proposed 0.7V LNA is shown in Fig.2.3. In this circuit, the RF signal is amplified by the NMOS device and the common gate current buffer is implemented by PMOS device to minimize Miller effect and to improve the response at high frequency. Then, use C_{b2} to ac couple the RF signal to the last NMOS buffer. In the low voltage design, we use an LC tank network (L_d , C_d), acting as a high impedance current source to decrease headroom dissipation. The resonant frequency of this LC tank is designed at the RF frequency of 2.45GHz. At resonant frequency, it provides a high impedance branch to force the RF signal to flow into the source of M2 and bypass other undesired signal to ground at other frequencies. Notice that the parasitic capacitance and C_{gs2} have to be considered when determining the value of C_d .

$$w_o \approx \sqrt{\frac{1}{L_d\left(C_d + C_{gs2}\right)}} \tag{2.1}$$

Because C_{gs2} is eliminated or reduced at resonant frequency, it helps to suppress the noise contribution of the common gate stage at the output. Thus, the noise performance of the folded cascode configuration can be lower than conventional cascode configuration.

In order for this operation to be true, it is necessary to have the impedance of the LC tank at resonance much higher than the input resistance seen at the source of M2. Fig.2.4 shows the characteristic of the LC tank, where R_s and Q are the resistance and the quality factor of the L_d. At the resonant frequency, the impedance of the LC tank attains the peak value of $R_s(1+Q^2) \approx R_s Q^2$. It can shown that this is satisfied by choosing $g_{m2} \gg \frac{1}{R_s Q^2}$. Since P1 only acts as a common gate unity gain current buffer, it does not need an f_T much higher than the RF frequency. An f_T of approximately twice of the RF is sufficient to achieve the desired performance and this requirement can be easily satisfied with modern submicron PMOS devices [14].

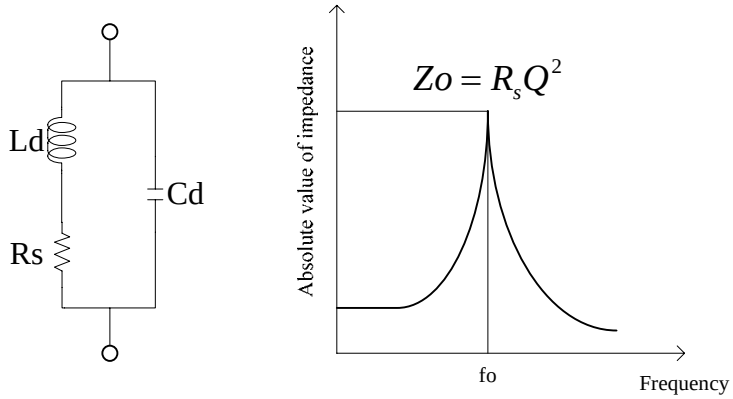


Fig.2.4 Characteristic of LC tank

2.2.1 Input Matching

To design a LNA, the minimum noise figure and maximum power gain are the most important considerations. In fact, the noise behavior will depend on the LNA experimental results and appropriate architecture. Several architectures of the LNA for these design goals had been developed and inductive source degeneration used in the first stage of LNA is the most prevalent method for CMOS amplifiers [19]. This architecture applies a source inductor and a gate inductor to generate real impedance of the input port. This topology also has the possibility of reaching the best noise performance and is most practical for high frequency applications. A simple analysis of the input impedance of the source inductive degeneration architecture is shown blow.

$$Z_{in} = R_l + R_g + \frac{g_m L_s}{C_{gs}} + j\left[w(L_g + L_s) - \frac{1}{wC_{gs}} \right]$$

$$= R_l + R_g + w_T L_s \quad \text{(at resonance)} \qquad (2.2)$$

where R_l is the series resistance of the gate inductor L_g and R_g is the gate resistance of the MOS. For noise purposes, the effective gate resistance is given by $R_g = \frac{R_{\square} W}{3n^2 L}$, where $R_{\square}$ is the sheet resistance of the poly silicon, W is the total gate width of the device, and n is the number of gate fingers used to layout the device. By interdigitating the device, R_g can be reduced to insignificant level. For high Q inductor, R_l may be negligible. If so, the real term in the input impedance is determined by L_s and typically is 50Ω. At the central frequency, the imaginary

term of Z_{in} will be zero, which gives

$$w(L_g + L_s) - \frac{1}{wC_{gs}} = 0 \tag{2.3}$$

From the above equation, we can solve L_g .

2.2.2 Noise Figure and MOS Width Selection

In CMOS process, drain current noise and gate noise are main noise sources in LNA design. The noise figure is related to SNR (signal to noise ratio) as

$$NF \equiv \frac{SNR_{in}}{SNR_{out}} = \frac{\text{Tatol noise power at output}}{\text{Noise power at output due to source only}}$$

$$= 1 + \frac{N_{add}}{N_i} \tag{2.4}$$

If we, only consider the drain current noise of the M1 and P1, the noise figure of the LNA can be presented as [20]

$$NF \approx 1 + \gamma_1 g_{d0n1} R_s \left(\frac{w_o}{w_T}\right)^2 \left[1 + \left(\frac{w_o C_t}{g_{mp1}}\right)^2 \left(\frac{\gamma_{p1} g_{d0p1}}{\gamma_{n1} g_{d0n1}}\right)\left(1 + \frac{w_T L_s}{R_s}\right)^2\right] \tag{2.5}$$

where C_t represents the overall capacitance at M1 drain, including the parasitic capacitance at M1 drain and the gate to source capacitance of P1, g_{do} is the drain-source conductance at zero $V_{DS,}$ the parameter γ has a value of unity at zero V_{DS} and, in long device, decreases toward a value of 2/3 in saturation. And the noise

contribution of the P1 is

$$NF_{p1} \approx \gamma_{p1} g_{d0\,p1} R_s \left(\frac{w_o}{w_T}\right)^2 \left(\frac{w_o C_t}{g_{mp1}}\right)^2 \left(1+\frac{w_T L_s}{R_s}\right)^2 \tag{2.6}$$

It indicates that the noise contribution of P1 decrease with C_t, which can be decreased by the LC tank and layout skill. In general, C_t is in the same order of the gate to source capacitor, thus

$$\left(\frac{w_o C_t}{g_{mp1}}\right)^2 = \left(\frac{w_o}{w_T}\right)^2 \tag{2.7}$$

and the noise contribution of P1 becomes

$$NF_{p1} = \gamma_{p1} g_{dop1} R_s \left(\frac{w_o}{w_T}\right)^2 \left(1+\frac{w_T L_s}{R_s}\right)^2 \left(\frac{w_o}{w_T}\right)^2$$

$$\approx NF_{M1} \left(1+\frac{w_T L_s}{R_s}\right)^2 \left(\frac{w_o}{w_T}\right)^2 \tag{2.8}$$

where NF_{M1} is the noise contribution of M1. In practice, $w_0 \ll w_T$, so the noise contribution of P1 is much less than M1, in other word, M1 dominates the noise figure of the LNA. Thus, the first stage of LNA should choose appropriate width size to minimize the noise figure. The optimum M1 size can be calculated by the

$$W_{opt} = \frac{3}{2} \frac{1}{wLC_{ox}R_s Q_{L,opt}} \approx \frac{1}{3wLC_{ox}R_s} \tag{2.9}$$

which is about 280um if minimum channel length of $0.18\,um$ is chosen. And the width of the PMOS is selected as twice of the M1 because the transconductance of PMOS is twice smaller than that of NMOS.

2.2.3 Linearity and Variable Gain Mechanism

In the cascade architecture, the later stage plays a more important role than the former stage. Thus, a buffer stage M2 is added to increase the linearity of LNA. The transfer function for a short channel MOSFET can be expressed as [20]

$$i_d = K\frac{\left(V_{GS}+v(t)\right)^2}{1+\theta\left(V_{GS}+v(t)\right)} \tag{2.10}$$

where $v(t)$ is the input voltage and θ is the normal field mobility degradation factor has a typical value in the range of 0.1-1V^{-1}. Expanding Eq.(2.10) in Taylor series and neglecting the DC component and harmonics higher than the third-order, we get the coefficients of the transfer function as

$$\beta_1 = \frac{KV_{GS}\left(2+\theta V_{GS}\right)}{\left(1+\theta V_{GS}\right)^2} \tag{2.11}$$

$$\beta_3 = \frac{-\theta K}{\left(1+\theta V_{GS}\right)^4} \tag{2.12}$$

The input referred third order intercept point of M2 is

$$IIP3^2_{M2} = \frac{4}{3}\left|\frac{\beta_1}{\beta_3}\right| = \frac{4}{3}\left|\frac{V_{GS}\left(2+\theta V_{GS}\right)\left(1+\theta V_{GS}\right)^2}{\theta}\right| \tag{2.13}$$

As shown in Eq.(2.13), the input referred third order intercept point of M2 increases with the gate to source voltage. But increase the gate to source voltage will lead to a rise in power consumption at the same time. So, M2 is designed quarter of the M1 to save power consumption and then to provide suitable output matching and increase the linearity.

The gain control is achieve by adjusting the gate voltage of the PMOS without affecting the bias condition and input matching which are determined by M1. Hence, the NF is not affected seriously when controlling the overall gain of the LNA. Conventional cascode LNA do not have this flexibility in gain control. Gain control could only be achieved by altering the bias current of M1 and affecting the whole input noise and input matching that we do not desire.

There are two useful formulas presented in [21]

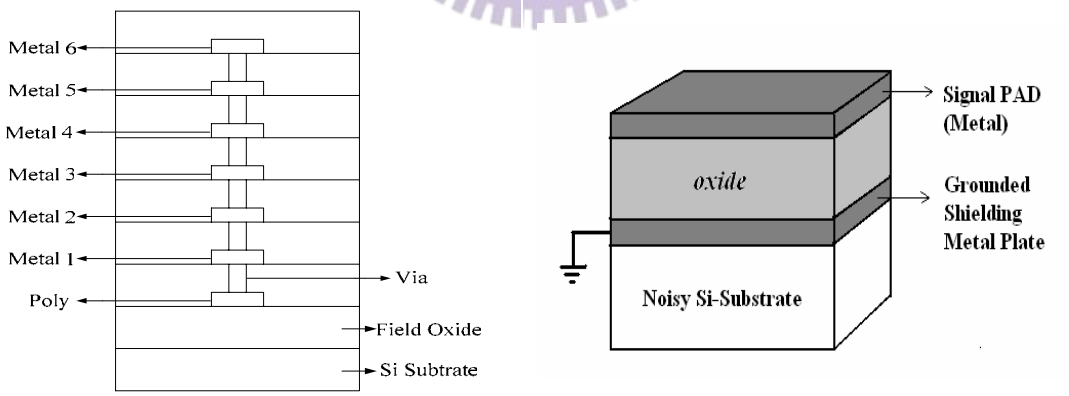
$$NF \approx 1 + \frac{2}{3}\frac{L_s}{L_g} \tag{2.14}$$

$$P \propto \frac{L^2}{\mu}\left(\frac{R_s}{w_c}\right)^2 \frac{1}{L_s^3\left(1+\frac{L_g}{L_s}\right)} \tag{2.15}$$

It reveals that NF decrease as L_s decreases and L_g increases, but the power will increase as L_s decrease. There is a trade-off between noise figure and power consumption. This is a very valuable design guideline.

2.3 Layout Consideration

Layout is the heart of the RFICs. The layout affects the performance significantly for RF circuit due to the parasitic components at high frequencies. We should not only take all of these parasitic into simulation but minimize these effects as low as possible. There are several essential common senses should keep in our mind. First, wide metal connection is avoided because this cause large parasitic capacitance to ground that may induce AC signal leakage. Second, transistor with a large width is split into several small transistors that reduce both the S/D junction area and the gate resistance. Third, due to the lowest parasitic resistance, metal 6 is the best layer for RF signal. Fourth, the spiral inductors are as far as possible to the other device (at least 50um). Fifth, the active devices are protected by the guard ring to minimize the noise coupling from substrate. Finally, to reduce noise coupling from the noisy silicon substrate, the shield signal PAD shown in Fig.2.5 (b) is used.



(a) (b)

Fig.2.5 (a) Cross section of 0.18um CMOS technology (b) The shielded signal PAD

The low voltage LNA is implemented in TSMC 0.18um process. The final layout is shown in Fig2.6 that all elements are fully integrated on a chip including RFMOS, spiral inductor, metal-insulator-metal (MIM) capacitor and poly-resistance. Since LNA is designed for on wafer measurement, layout is set in uni-directional mode. The RF input and output are placed on opposite sides of the layout to avoid the high frequency signal coupling. And GSG (Ground-Signal-Ground) pad structures are used in both RF input and output ports. The total chip size is 1.1mm*1.0mm.

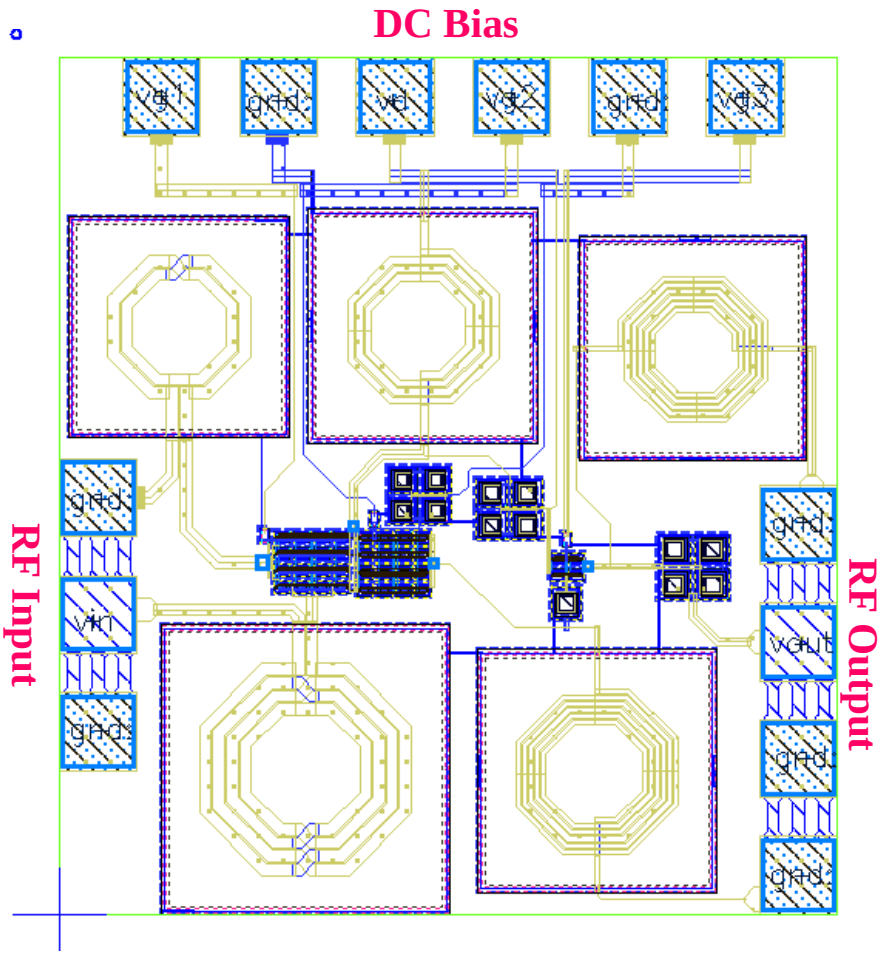


Fig.2.6 Layout of the low voltage LNA

2.4 Measurement Consideration

The LNA is designed for on-wafer testing, so the layout allocation must fit the requirement of the CIC's probe station testing rules as shown in Fig.2.7. We use one 6-pin dc probe card and two GSG RF probes on CIC. The measurement arrangement for our design of the LNA is represented in Fig.2.8. The measurement setup is show in Fig.2.9, which includes high frequency S-parameters, noise figure, P1dB and two-tone IIP3 linearity testing. The circuit is designed a frond-end in 50Ω system for the measurement system. All of the matching devices are on-chip components and then we can easily integrate the other frond-end circuit such as mixer and synthesizer in future work. Since we have finished the measurements from CIC, we will discuss and compare the simulation and measurement results in the next section.

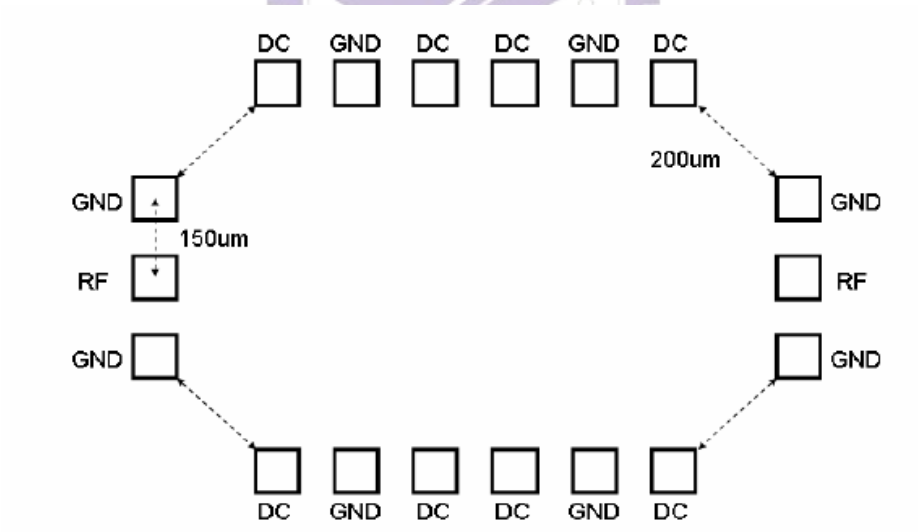


Fig.2.7 CIC probe station layout rule

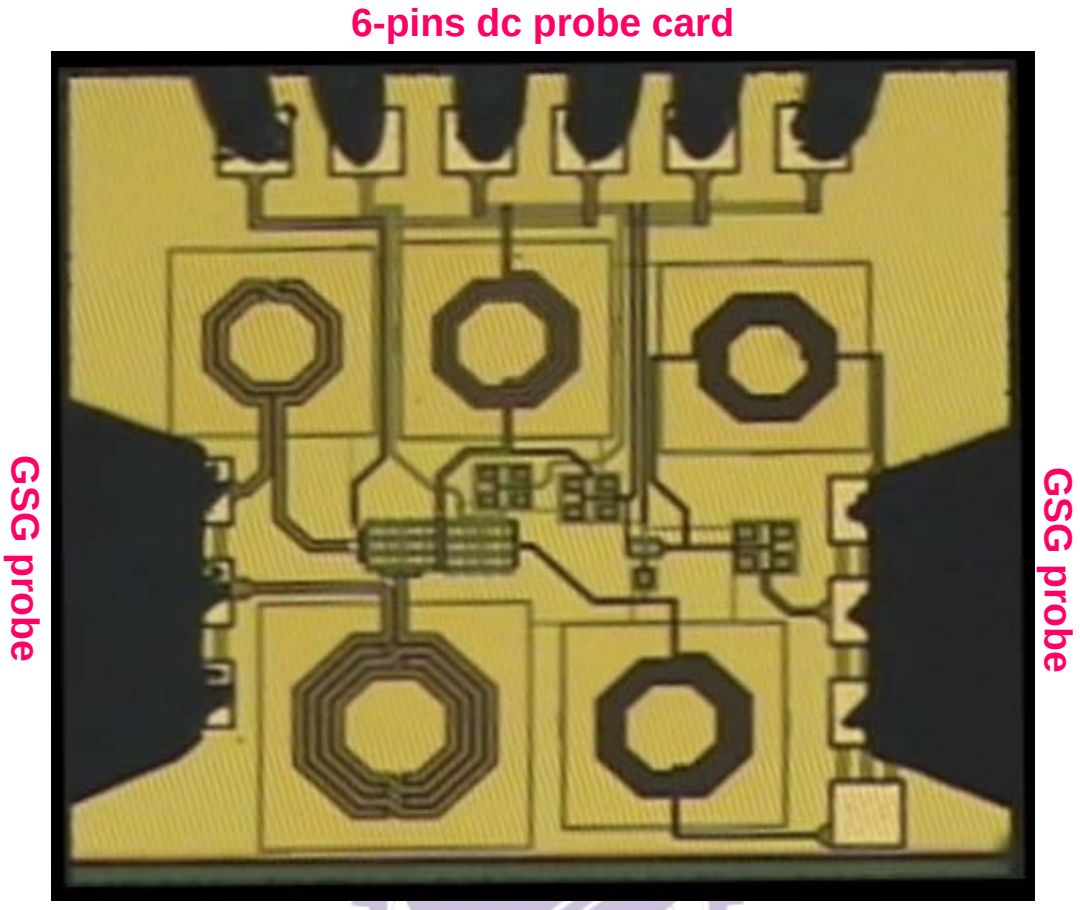
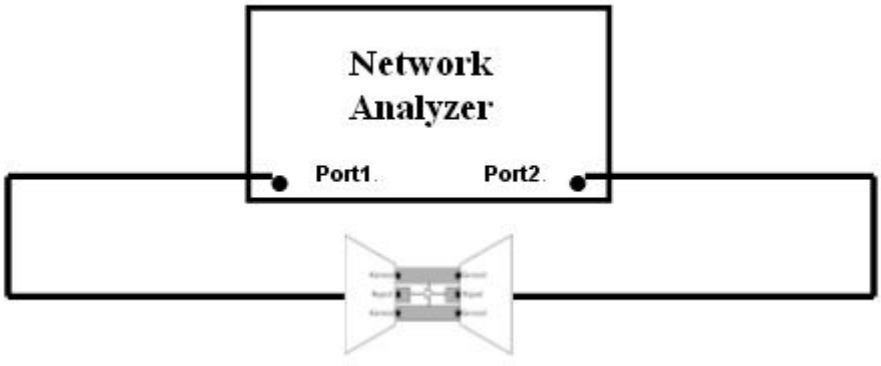
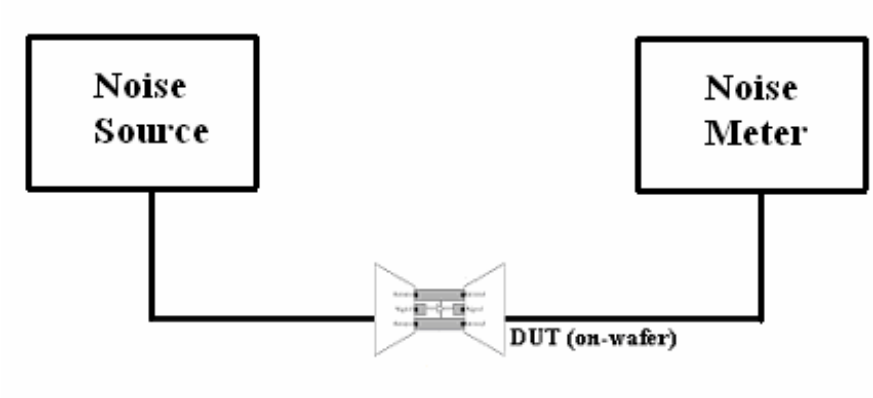


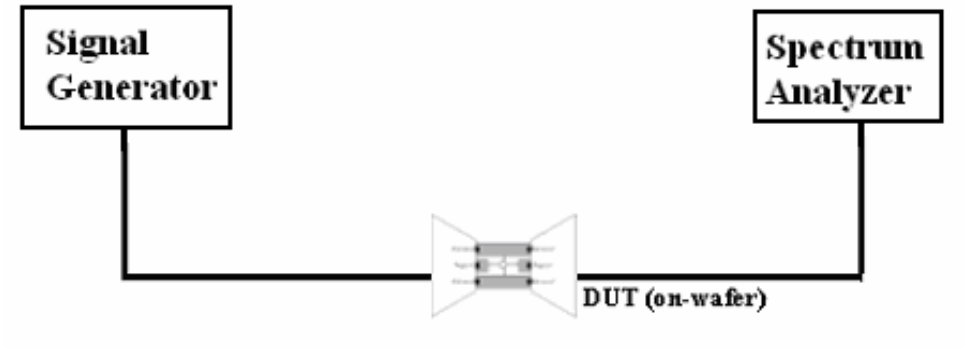
Fig.2.8 LNA measurement arrangement



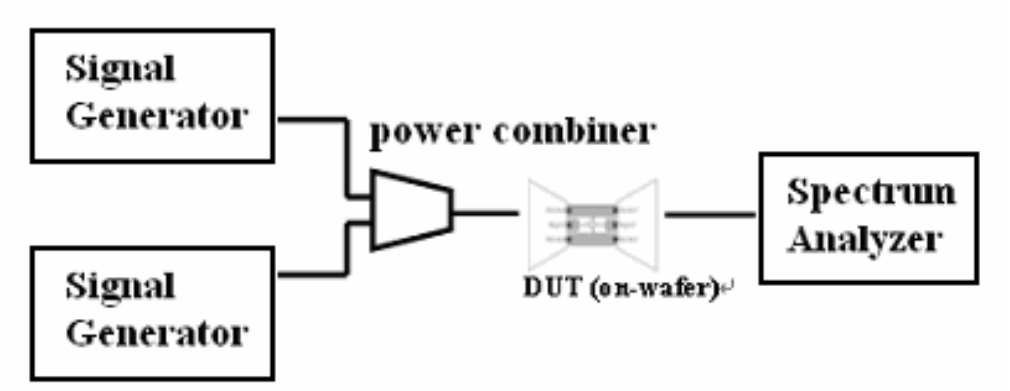
(a) S-parameter



(b) Noise figure



(c) P1dB

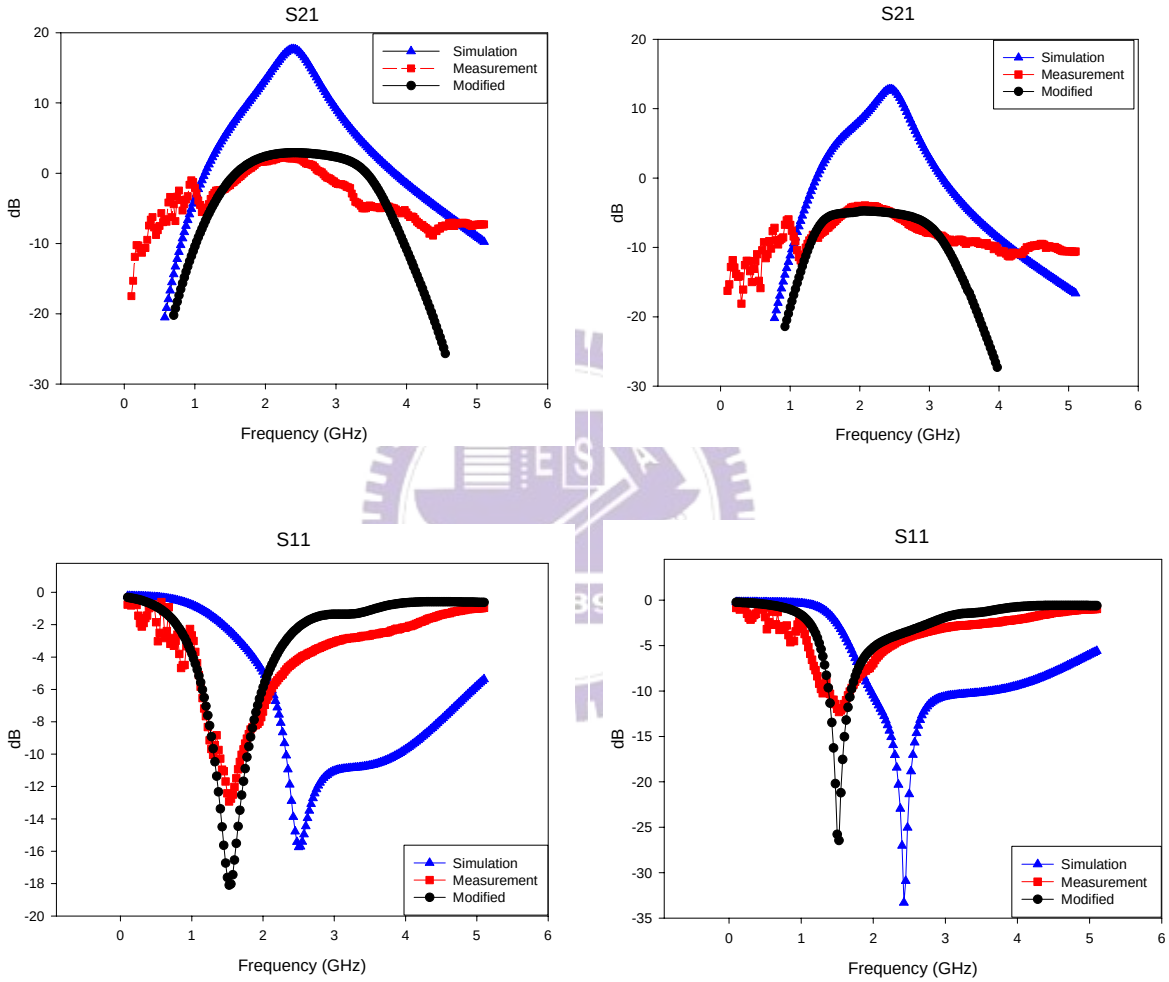


(d) IIP3

Fig.2.9 Measurement setups for LNA

2.5 Simulation and Measurement Results Comparison

Fig.2.10 shows the simulation, measurement and modified simulation results of S21 and S11



(a) High gain mode (b) Low gain mode

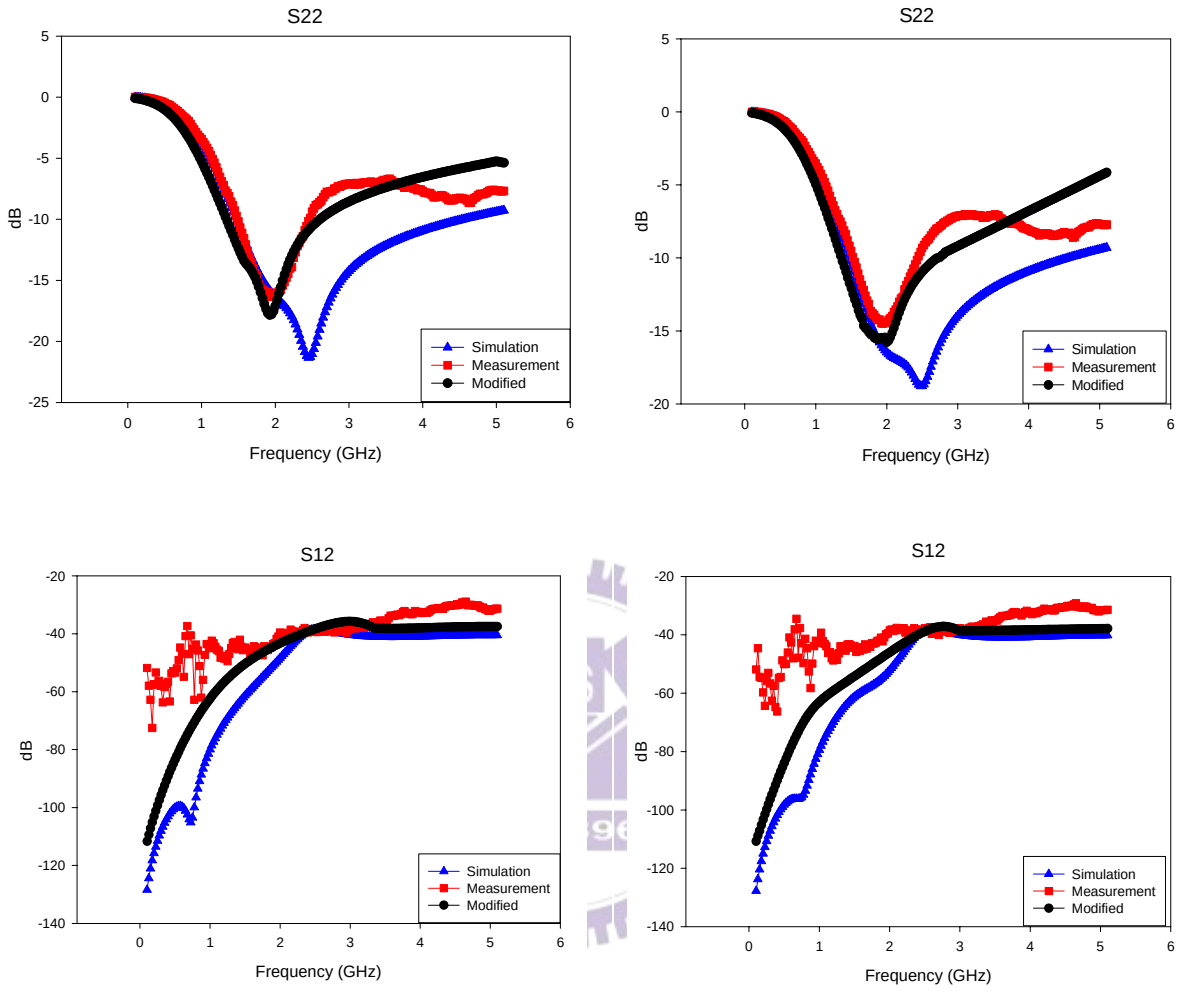
Fig.2.10 Comparison between simulation and measurement of S21 and S11

We find that the S21 is appeared closely at the center frequency, but S11 is shifted down to the 1.7GHz. The simulation and measurement results are not meeting

the same way. Thus, we modify circuit parameters to fit the measurement results. By the Eq.(2.3), the larger inductor and gate to source capacitor the lower resonant frequency. Thus, a larger inductor and capacitor on the input matching network make the optimum matching peak of S11 shift down to the low frequency. We try to increase the inductors of M1 to fit the measurement results. Fortunately, the modified simulation results can achieve closed results as measurement. Therefore, we can prove the larger inductance appears in the input matching network make the frequency shifting. This may come from the incorrect model of the on chip inductor and the large parasitic inductor from the long RF line in the input matching network. Although through the layout parasitic extraction (LPE), we still can not accurately predict the parasitic effects in the high frequency region. The larger parasitic inductor and capacitor can be avoided by advanced layout skill that is a worthy goal for designer to learn. Because of the resonant frequency of the LC tank is closed to 2.45GHz, the S21 parameter closely falls on desired band. And there are three possible reasons make the value be -15dB lower than simulation. First and the major reason is the frequency shifting of S11. Second, the inductance of L_{dp} and L_{out} is smaller than we expected. Third, the Q value of the LC tank is not good enough with the LNA layout design, that making the RF signal loss to ground.

Fig.2.11 shows the simulation, measurement and modified simulation results of S22 and S12. The peak of the output matching S22 is shifted down to 2GHz and is -10dB at 2.45GHz. By the modified simulation, we can find the smaller inductor and capacitor on the output matching network make a -10dB reduction. Although -10dB is achieved, it is enough for applications. From above discussion, the correct model for the on chip inductor is the most important in the LNA design. The S12 is as good as simulation results that prove the folded cascode configuration can provide good

isolation as the conventional cascode configuration.

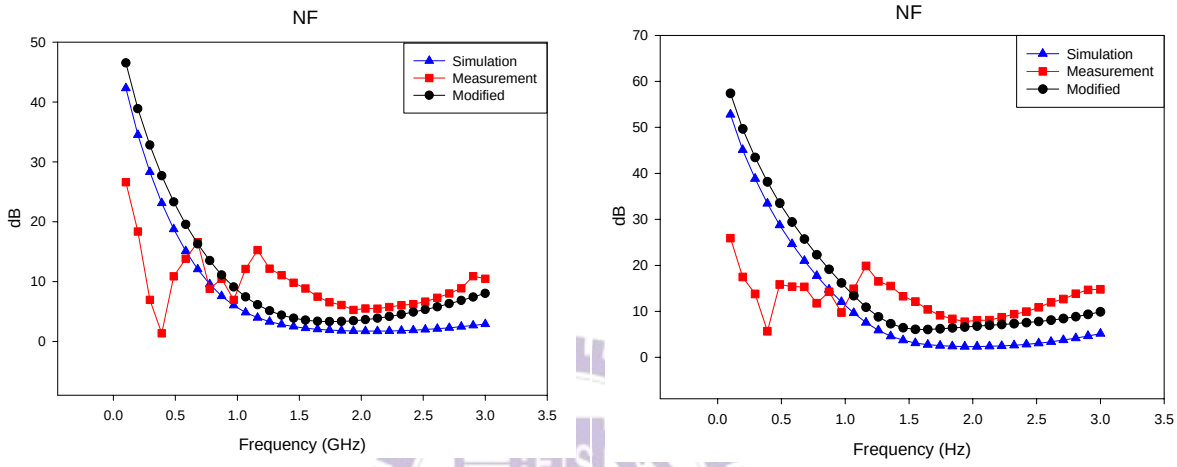


(a) High gain mode (b) Low gain mode

Fig.2.11 Comparison between simulation and measurement of S22 and S12

The noise figure is measured from 100MHz to 3GHz as shown in Fig.2.12. The noise performance is not good, rising to 6.22dB at high gain mode. The major reason is the gain of the LNA is only 2.21dB that can not suppress the noise contribution. And the measurement result is a little higher than modified simulation results. This is because the transistor model is not accurate enough which only

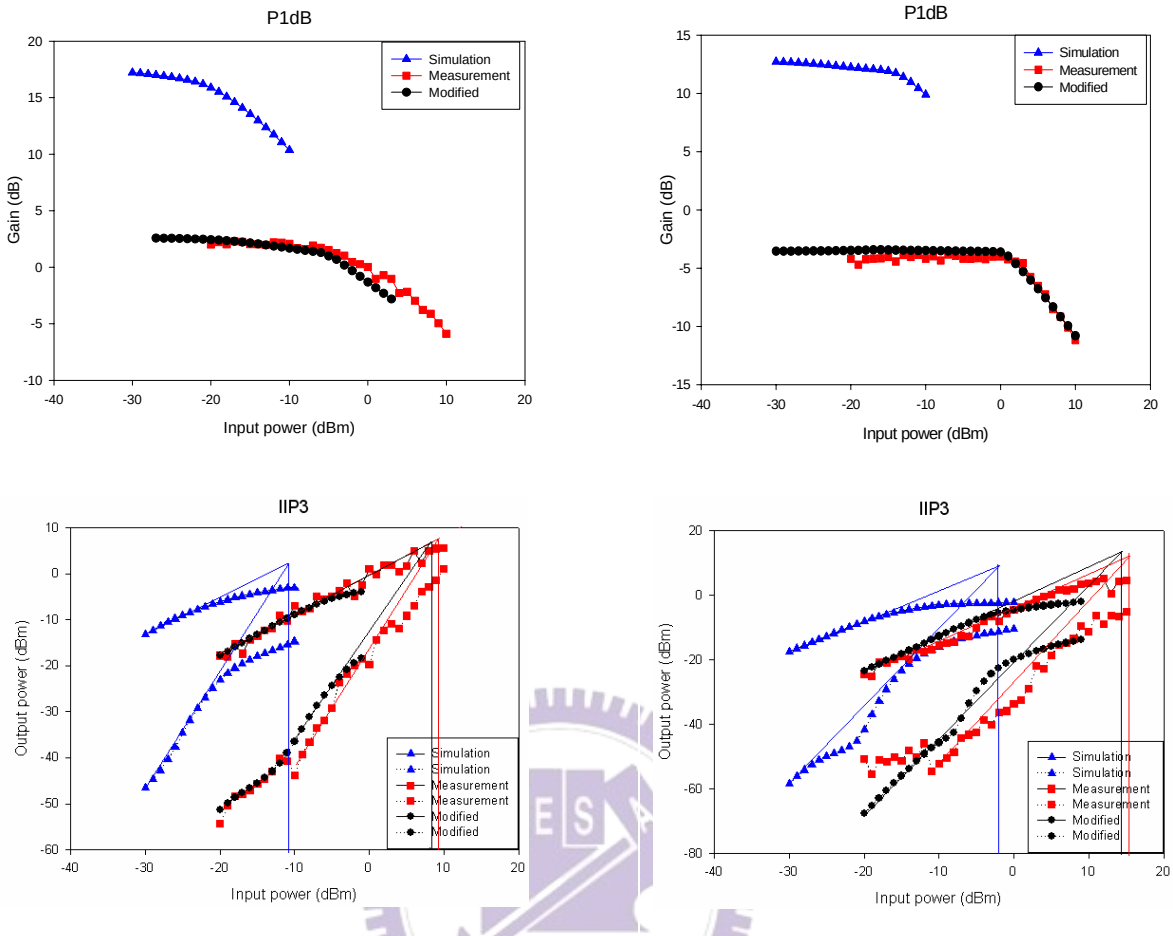
consider the thermal noise and gate induced noise is not included. But the peak value of noise figure is almost appeared at the center frequency. That is because the peak value of S21 is close to the center frequency. Thus, if we can achieve enough gain, the noise figure may go down to anticipated value below 2.5dB.



(a) High gain mode (b) Low gain mode

Fig.2.12 Comparison between simulation and measurement of NF

The LNA design can achieve better dynamic range and linearity of P1dB and IIP3 parameters in measurement than those in simulation. As shown in Fig.2.13, the modified simulation and the measurement results are almost the same, the IIP3 is 8dBm at the high gain mode and 15dBm at the low gain mode. Of course, that is due to the lower gain performance cause the high linearity. The difference of linearity between high and low gain mode is 7dB, being almost the same as simulation. Thus, the function of the linearity release is work. And the performance of the simulation and measurement is summarized in the Table 2.1. The total power consumption is 7.27mw at the high gain mode and 5.06mw at the low gain mode.



(a) High gain mode (b) Low gain mode

Fig.2.13 Comparison between simulation and measurement of P1dB and IIP3

Table 2.2 shows the comparison of this work and recent LNA papers. Because the difference between simulation and measurement results, both data are showed. According to the simulation results, power consumption and the noise figure is the lowest one. The forward gain, input matching, output matching are designed at a suitable value above 15dB. And the most important performance, noise figure, is designed to a lowest value. Although linearity is not good enough, it is in the specification for Bluetooth and 802.11b applications. Because of the linearity of the receiver is dominated by the later stage as mixer, our goal is to design a LNA with low noise figure, appropriate forward gain and low power consumption.

Specification	Simulation		Measurement	
	High gain mode (Vg2=0V)	Low gain mode (Vg2=0.16V)	High gain mode (Vg2=0V)	Low gain mode (Vg2=0.16V)
Center frequency(GHz)	2.45	2.45	2.45	2.45
S21 (dB)	17.5	12.8	2.21	-4.38
S11 (dB)	-15.0	-30.4	-4.35	-4.17
S22 (dB)	-21.3	-18.6	-10.14	-9.88
S12 (dB)	-38.6	-38.5	-39.16	-38.46
NF (dB)	1.90	2.90	6.22	9.55
P1dB (dBm)	-21.5	-14.1	-3	4
IIP3 (dBm)	-11	-3	8	15
Power (mw)	7.27	5.06	7.27	5.06

Table 2.1 Measurement and Simulation results Summary

REF	[16] 2002	[22] 2003	[23] 2003	[24] 2003	[25] 2004	This work 2005.06	
Supply voltage (V)	1	1	1	1.8	1.8	0.7	0.7
S21(dB)	15	23.0	11.6	23.1	15	2.21	17.5
S11(dB)	-51.4	-16.8	-5.1	-5.8	-14	-4.35	15.0
S22(dB)	-34	-10.2	NA	NA	NA	-10.14	-21.3
S12(dB)	-37.5	-51.7	NA	-25.9	NA	-39.16	-38.6
NF(dB)	3.23	3.8	2.3	4.5	2.2	6.22	1.90
P1dB(dBm)	NA	NA	-7.9	-20.8	NA	-3	-21.5
IIP3(dBm)	-1	-9.1	NA	-15	3	8	-11
Power(mw)	9.85	13	14.2	36	7.2	7.27	7.27
Condition	Sim.	Meas.	Meas.	Meas.	Sim.	Meas.	Sim.

Table 2.2 Comparison of recent LNA papers

Chapter 3
0.7V 2.45GHz Mixer

In this chapter, we will present a 0.7V mixer designed and fabricated in TSMC 0.18 μm CMOS process. Like the design method applied in low voltage LNA, the differential PMOS type folded cascode configuration is used. We will analysis the conversion gain, noise and linearity of the low voltage mixer. The measurement results show that the mixer provides a voltage gain of 0.91dB, power gain of -9.68dB, P1dB of 0dBm, and IIP3 of 10dBm with the 2.11mW power consumption. The discussion of the difference between simulation results and measurement results and the comparison of other low voltage mixer papers will be in the last section.

3.1 Introduction

An essential element in modern transmitters and receiver is the mixer, being responsible for frequency up-conversion and down conversion. Modern wireless communication systems demand stringent dynamic range requirement that is often dominated by the mixer. Thus, mixer design focuses on balancing the tradeoff between gain, linearity, matching, port to port isolation, LO power, noise figure and power consumption. The noise performance of the mixer is not too stern because it is located after the LNA that will suppress the noise contributed from mixer. Therefore, a good mixer design is focused on the high linearity. The mixer would handle larger signal than LNA, and its non-linearity must be lower by at least a factor of the LNA gain if it is not to become the bottleneck to receiver dynamic range. And, integrated mixers become more desirable than discrete ones for higher system integration for cost and space saving.

Passive and active mixers are two common topologies in recent research. The name “passive” mixer comes from the characteristic that it does not provide any gain. Since double balanced active mixer designs are more desirable for today’s integrated receiver designs due to its low spurious outputs, high common mode noise rejection, high port to port isolation and the most important, gain. Thus, our low voltage mixer is basically a double balanced active mixer configuration.

3.2 Mixer Design

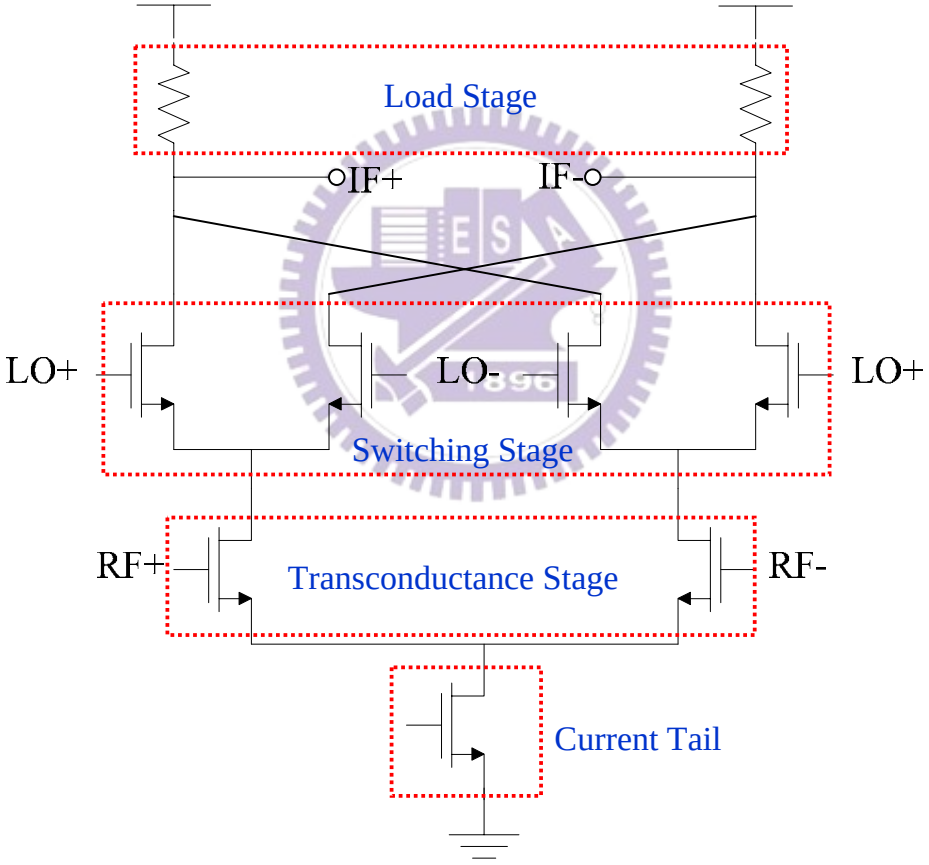
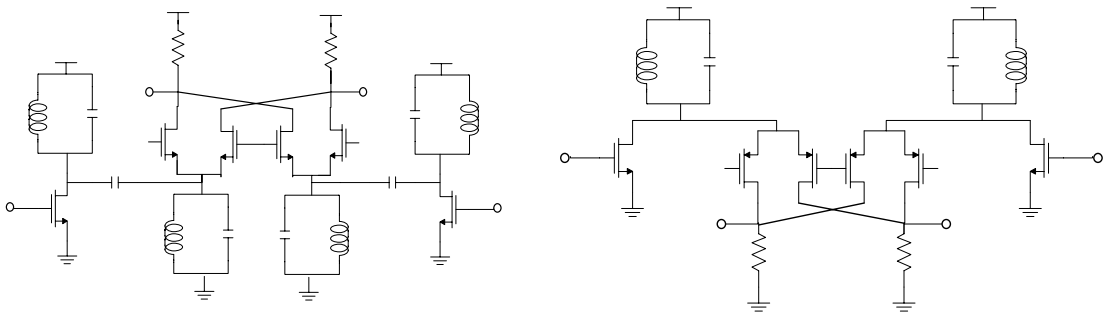


Fig.3.1 Gilbert type double balanced mixer architecture

Fig.3.1 shows a most common seen topology for mixer called Gilbert-type double balanced mixer. It has the virtue of moderate gain, good RF-LO isolation, and linearity than other topologies. The mixer can roughly be divided into three stages, the

transconductanc stage, the switching stage and the load stage. Outputs are located between the switching stage and the load. The transconductance transistors first amplify the input voltage signal and convert the signal into a current signal. Then the switching stage performs the frequency translation, and the load converts the current signal back to voltage signal.

Because the above double balanced mixer has a stack of three transistors and a load resistor between the voltage rails. It is not suitable while the supply voltage decreases to 0.7V. Thus, folded cascode configuration is used to reduce the stack of the transistors. As described in Chapter 2, there are two topologies for folded cascode, PMOS type [16, 26-27] and NMOS type [17, 28] as shown in Fig.3.2. In the differential circuits like mixer, NMOS type will need four LC tanks that the chip area is much larger than PMOS type. And on the low IF receiver, flicker noise of the switching stage is the most important noise source for the mixer. It is know that PMOS has less flicker noise than NMOS, and the low voltage mixer is basically a PMOS type configuration to achieve better noise performance.



(a) NMOS type (b) PMOS type

Fig.3.2 Two types of the differential folded cascode configuration

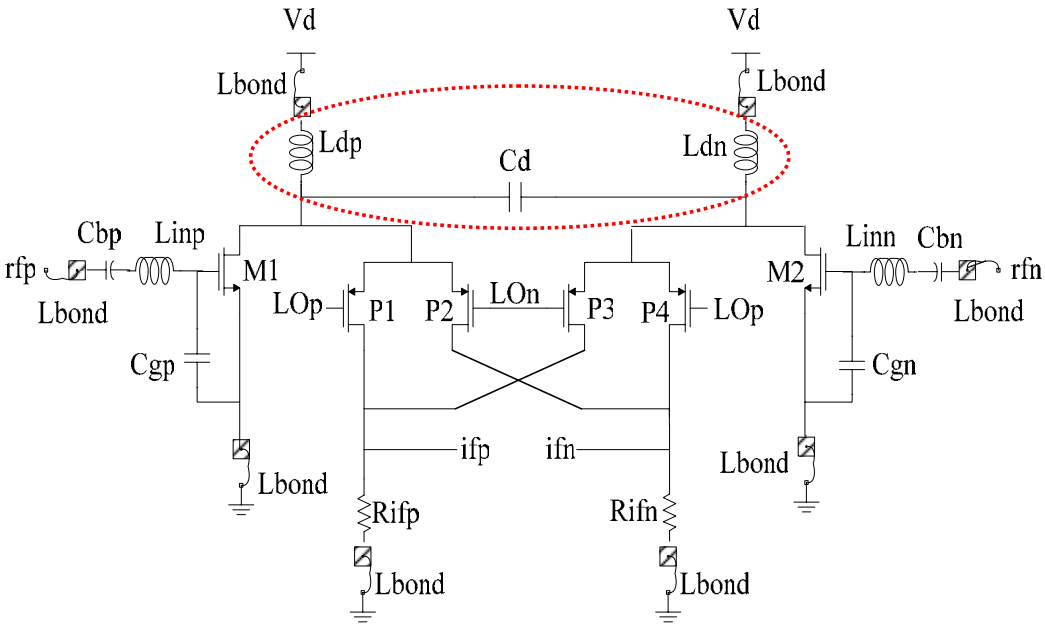


Fig.3.3 Architecture of modified very low voltage mixer

Fig.3.3 shows the proposed low voltage mixer. As the typical double balanced mixer, NMOS M1 and M2 acts as transconductance stage, PMOS P1-P4 act as the switching stage and using two resistors as load stage. The current tail is not used because it will cost the voltage headroom and decrease the linearity. The high impedance LC tank is made by L_{dp}, L_{dn} and C_d unlike using two separated LC tanks in general design. The resonant frequency is designed at center frequency-2.45GHz. Here, the bond wires, the parasitic capacitances and the C_{gs} of PMOS must be considered.

$$w_o \approx \sqrt{\frac{1}{2\left(L_{bond}+L_{dp}\right)\left(C_d+C_{gsp}\right)}} \tag{3.1}$$

It is obviously that the inductors are half of the two separate LC tanks design so we can save more chip size. The input matching network is made by L_{inp} (L_{inn}),

$C_{bp}(C_{bn})$, $C_{gp}(C_{gn}), C_{gsp}(C_{gsn})$ and the bond wires on RF input and on the source of M1 (M2). Using the Eq.(2.2) and assuming each bond wire be 3nH, we design the input matching network. Here, the resistor load $R_{ifp}(R_{ifn})$ is used instead of the active load to decrease the flicker noise contributed from load stage. Since the load is resistive, the need of a common-mode feedback (CMFB) circuit is avoided. In order to realize an on-chip band pass filter (BPF), the IF frequency should be lower, <3MHz, because a low-Q BPF is easy to design and the current consumption must be reduced. Thus, an IF of 2MHz is chosen

3.2.1 Conversion Gain

In Fig.3.2, we assume that the mixer under large LO driver and the mixer commutates the RF transconductance current with a square wave. Suppose a unit sinusoidal input voltage of frequency w_{RF} is linearity converted to a current, and commutated by the switches at w_{LO}, which amounts to multiplying the sinusoidal current by a square wave, $sq(w_{LO}t)$, alternating between +1 and -1. Then the differential current of R_{ifp} and R_{ifn} is [30]

$$I_{IF,dif} = g_{m,RF}v_{RF}\sin(w_{RF}t)\times sq(w_{LO}t)$$

$$= g_{m,RF}v_{RF}\sin(w_{RF}t)\times(\frac{4}{\pi})\left(\sin(w_{LO}t)+\frac{1}{3}\sin(w_{LO}t)+\cdots\right)$$

$$= (\frac{2}{\pi})g_{m,RF}v_{RF}\cos\left(w_{RF}-w_{LO}\right)t \qquad (3.2)$$

where the square wave is expanded as a Fourier series, and the term containing the downconverted frequency at $w_{RF} - w_{LO}$ is retained. Eq.(3.2) shows a current conversion loss of at least $\frac{\pi}{2}$ through the mixer. The overall mixer voltage gain is

$$Gain = \frac{4}{\pi} g_{m,RF} R_{ifp} \tag{3.3}$$

If we consider the switching time of switching stage P1-P4, we can re-express Eq.(3.3) as

$$Gain \approx \frac{4}{\pi} g_{m,RF} R_{ifp} \left(1 - \frac{\sqrt{2}\left(V_{GS} - V_t\right)_{sw}}{\pi V_{LO}} \right) \tag{3.4}$$

where $\left(V_{gs} - V_t\right)_{sw}$ denotes the overdrive voltage of switching stage [31]. From Eq.(3.4) we can understand that the conversion gain is proportional to the input device transconductance, the IF load, the overdrive voltage of switching stage and the amplitude of the input LO signal. If we increase conversion gain by increasing $g_{m,RF}$ and V_{LO}, the power consumption of the mixer and the VCO will rise simultaneously. Therefore the conversion gain forms a tradeoff with the circuit power consumption. In general, voltage and power conversion gain are not equal. The contrast between these two gains can be seen by expressing as

$$A_P = A_V^2 \frac{R_s}{R_L} \tag{3.5}$$

It indicates that the voltage and power conversion gain is equal only in the case where the differential load resistance is equal to the source resistance.

3.2.2 Noise

In the low IF receiver, flicker noise is the most important noise source of mixer. And the double balanced mixer is composed of transconductance stage, switching stage, and load stage. Noise is present in all the transistors making up these functions. First, the flicker noise contributed by the load stage can be reduced. It is know that the flicker noise only appears in the MOS transistors. Thus, the mixer loaded with polysilicon resistors instead of MOS transistors which are free of flicker noise from load stage. Then we discuss the flicker noise in the switching stage and transconductance stage. In [32], the signal to noise ratio of the switching stage is

$$SNR_{sw} = \frac{2A_{LO}}{(V_{GS} - V_t)_{trans}} \cdot \frac{V_{in}}{V_n} \tag{3.6}$$

The relationship shows that SNR of switching stage can be improved by rising the amplitude of LO signal; by increasing the gate area of the switch transistor to lower the flicker noise V_n; and by lowering the transconductance transistor overdrive voltage. However, increasing switching transistor gate area is usually degraded the mixer bandwidth and lowering transconductance transistor overdrive voltage will reduce the conversion gain. Then, the signal to noise ratio due to the transconductance stage flicker noise leaking to the output is

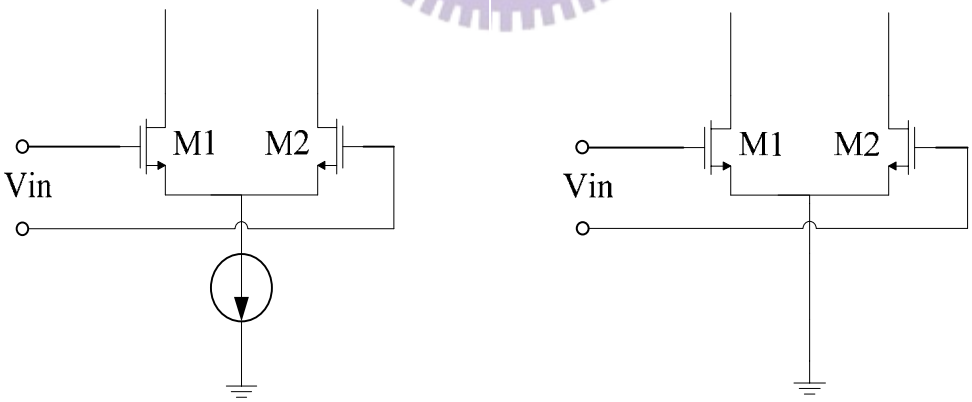
$$SNR_{trans} = \frac{2A_{LO}}{V_{os}} \cdot \frac{V_{in}}{V_n} \tag{3.7}$$

where V_{os} is the gate offset voltage due to the mismatch between switching stage.

As $V_{os} \ll V_{GS} - V_t$, the switching stage induced much larger noise than the transconductance stage. Thus, we can reduce the noise by using PMOS transistor as switching stage. This is another reason why we choose folded PMOS type instead of NMOS type. Here, the width of the transconductance stage is chosen a little larger than that of Eq.(2.9) in order to lower the threshold voltage required to bias the transistors in the saturation region. The width of the switching stage is chosen one-third of the transconductance stage and is biased near threshold to minimize their switching time that reducing in the same time the output noise..

3.2.3 Linearity

Linearity is the most important parameter in mixer design. The constant current tail and the grounded sources circuits in Fig.3.4 demonstrate differential behavior in linearity.



(a) (b)

Fig.3.4 Transconductance stage with (a) constant current tail (b) grounded sources

In Fig.3.4(a)

$$I_{out} = I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{in} \cdot \sqrt{\frac{2I_{SS}}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)} - V_{in}^2} \tag{3.8}$$

In Fig.3.4(b)

$$I_{out} = I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{in} \cdot \left(V_{GS1} + V_{GS2} - 2V_t\right) \tag{3.9}$$

The grounded source pair output contains no third order intermodulation products. Thus, we note that the transconductance stage with a constant current tail exhibits higher third order nonlinearity than the grounded source pair biased at the same current and device dimensions. In practice, short channel effects such as nonlinear channel length modulation and mobility degradation with the vertical field in the channel give rise to the third order distortion, but this calculation points to the potentially higher linearity of the grounded source pair [33].

Assuming the distortion performance to be mostly constrained by the transconductance stage, we can derive a estimation on the IIP3 performance expressed as [31]

$$IIP3 \approx 4\sqrt{\frac{2}{3}}\left(V_{GS} - V_t\right)_{trans} \tag{3.10}$$

Therefore, as the quality $\left(V_{GS} - V_t\right)_{trans}$ increases, the mixer is less likely to output distorted waveforms. Besides the voltage drop from the gate to the source of the input

device, the mismatches at the input stage also degrade the linearity performance.

As discuss above, the PMOS type folded cascode has many advantages. First, the reduction of the stack transistors let the supply voltage fall to 0.7V. Second, we use PMOS transistor as switching stage to decrease the flicker noise. Third and the most important one, the current in the transconductance stage and switching stage can be set independently to simultaneously optimize noise figure, linearity, and conversion gain. The high bias current in the transconductance stage can provide high conversion gain and better linearity performance. While minimize the flicker noise by choosing low bias current , wide device size and low gate to source overdrive voltage (most approach zero) using in the switching stage. The size of the transconductance stage is the same as the first stage of the LNA that can decrease some thermal noise to enhance the noise performance. The input network is like the source degeneration configuration and can design by the formula in Chapter 2. Here we assume each bond wire has a 3nH inductance. The LO port matching is realized by using the off chip element as shown in Fig.3.5.

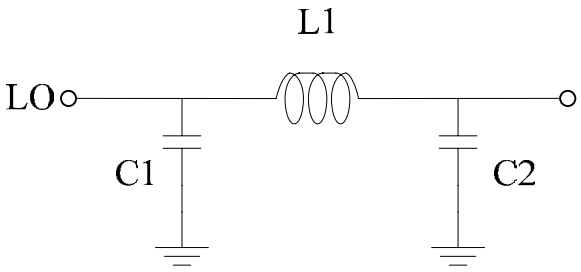


Fig.3.5 LO matching network

3.3 Layout Consideration

The most important layout guidelines are described in the Chapter 2. There is an additional guideline would be considered. The layout of the mixer should be as symmetrical as we can to avoid the phase difference and ensuring CMRR. The layout of the low voltage mixer is shown in Fig.3.6. Because the mixer is usually measured on PCB rather than on wafer, the order of pads does not need to follow the GSG (RF pad) or SGS (DC pad) rules. The RF and IF ports are on the bottom and top of the chip, and the LO port is on the right and left sides. Here, the circuit ground and substrate ground are separated to avoid the noise coupling. Then, the total chip size is 1.0mm*1.0mm.

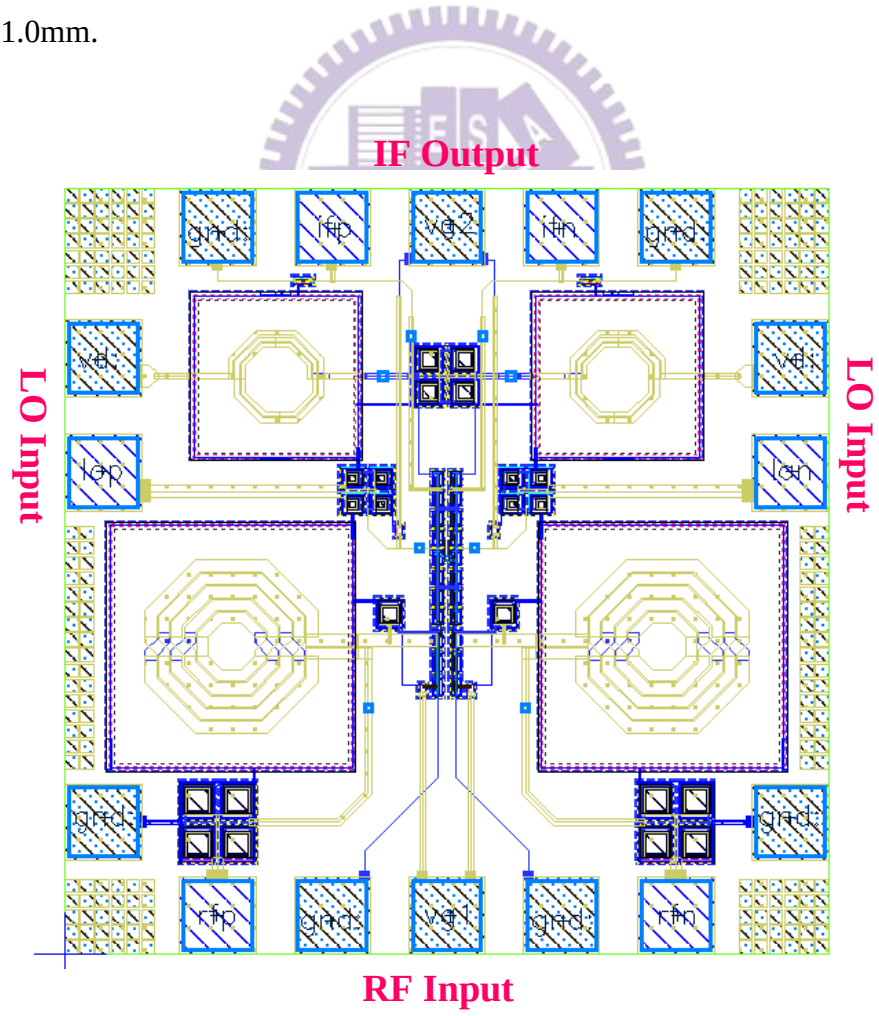


Fig.3.6 Layout of the low voltage mixer

3.4 Measurement consideration

Because the mixer is designed for PCB on-board testing, the parasitic effects of bond wires and bond-pads will greatly affect the impedance matching of all ports. For all outside 50Ω instruments, only input power of generators can be delivered into the chip or circuit output power can be received by measurement instruments more efficiently with good input or output impedance matching. Therefore, these parasitic effects must be included and considered throughout all simulation procedure very carefully. Typically, the inductance of the bond wire is about 1nH per 1mm and the parasitic capacitance of a 100um x 100um bond pad is approximate 150fF to the ground.

Because of fully differential configuration of the mixer, two Balun are required to transform single input to differential inputs. Here, we used a rat race shown in Fig3.7 to act as such Balun and the real S-parameter is as follow.

$$\begin{bmatrix} 0.046\angle 85.71° & 0.678\angle 155.1° & 0.675\angle 152.7° & 0.032\angle -25.9° \\ 0.676\angle 154.2° & 0.055\angle 55.93° & 0.035\angle -20.5° & 0.671\angle -22.7° \\ 0.675\angle 152.3° & 0.035\angle -21.3° & 0.017\angle 139.9° & 0.676\angle 155.7° \\ 0.032\angle -26.1° & 0.671\angle -22.9° & 0.675\angle 154.6° & 0.065\angle -45.1° \end{bmatrix}$$

Although this experimental result still has little error, it is very close to that of ideal case and satisfies for our requirement.

Layout of PCB and practical FR4 PCB circuit with SMA connectors are shown in Fig.3.8 and Fig.3.9, respectively. The RF, IF and LO signal path are drawn as 50Ω line width for impedance matching. Several on board decoupling capacitances are added on the DC path to filter the noise from the power supply.

The measurement setup is shown in Fig.3.10. The measured parameters are conversion gain, P1dB, IIP3 and high frequency input return loss of RF and LO ports. We use RFIC measurement system in CIC to complete our measurement. And the wide band Balun block used in the RF port is also provided by CIC. The loss of cable, Balun, SMA connector and board must be taken into account.

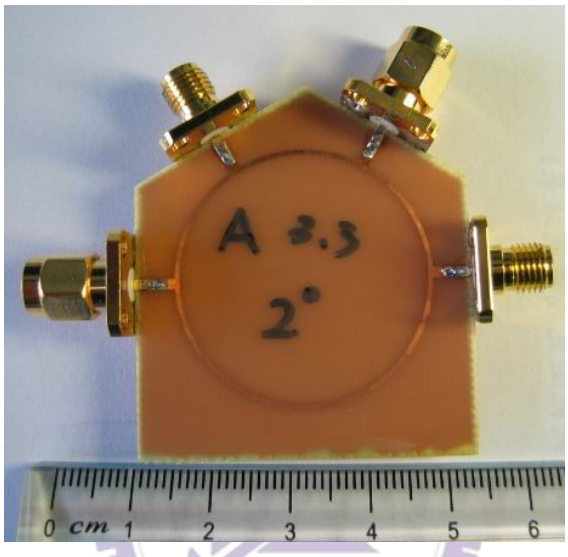


Fig.3.7 Photograph of LO port Rat-race

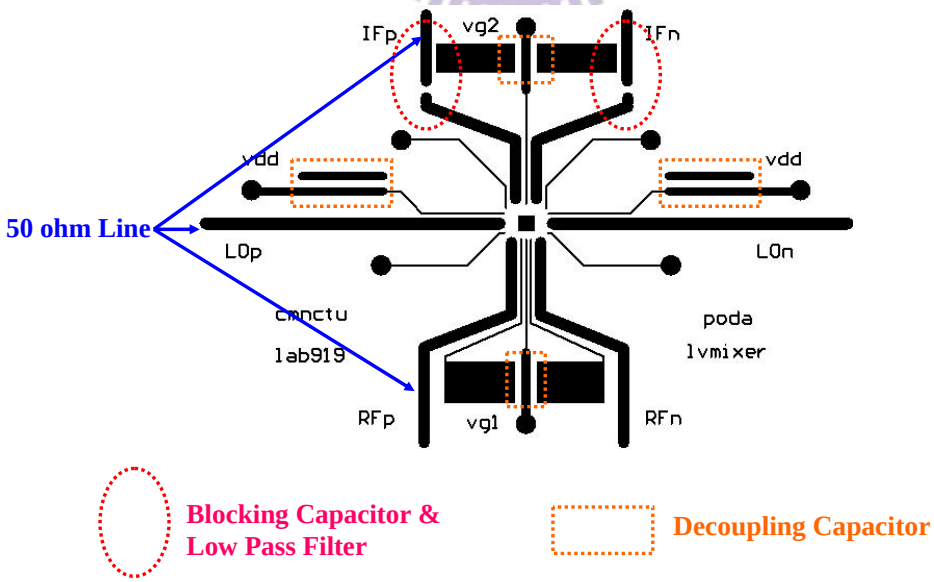


Fig.3.8 PCB layout

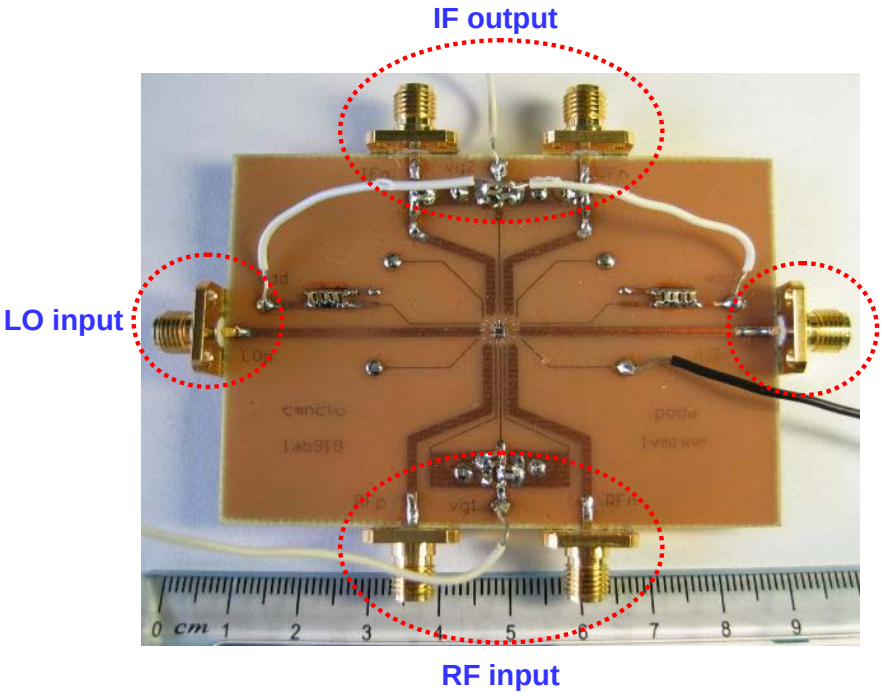


Fig.3.9 Practical FR4 PCB circuit

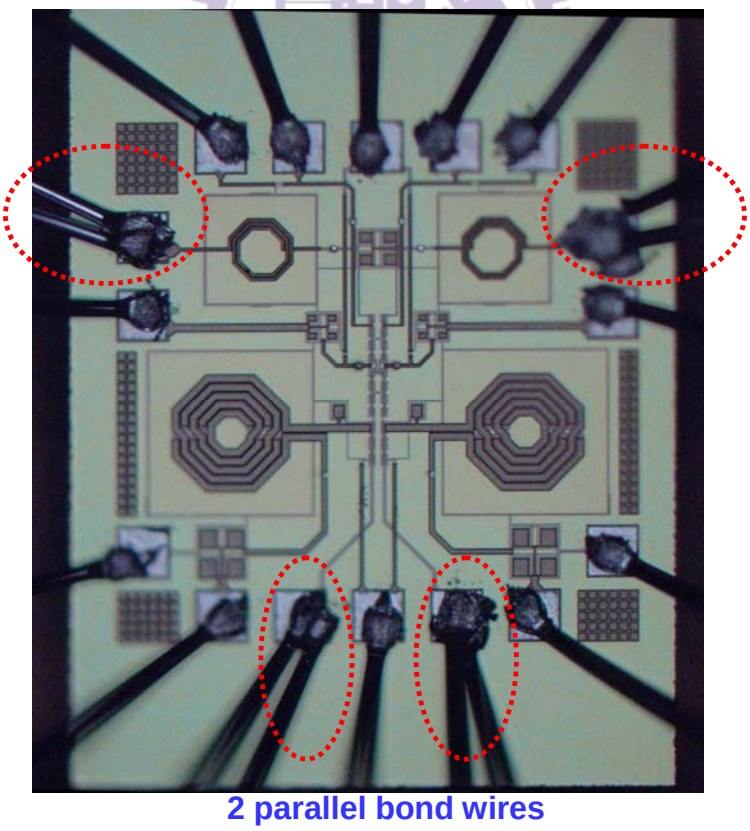
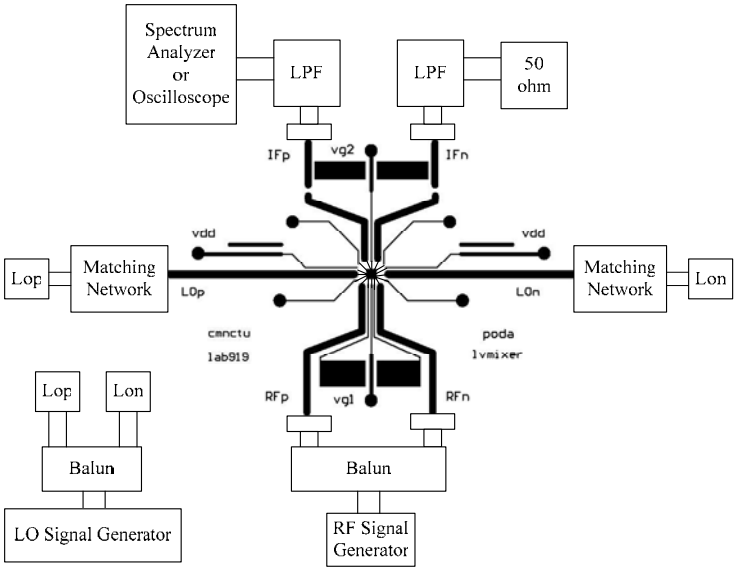
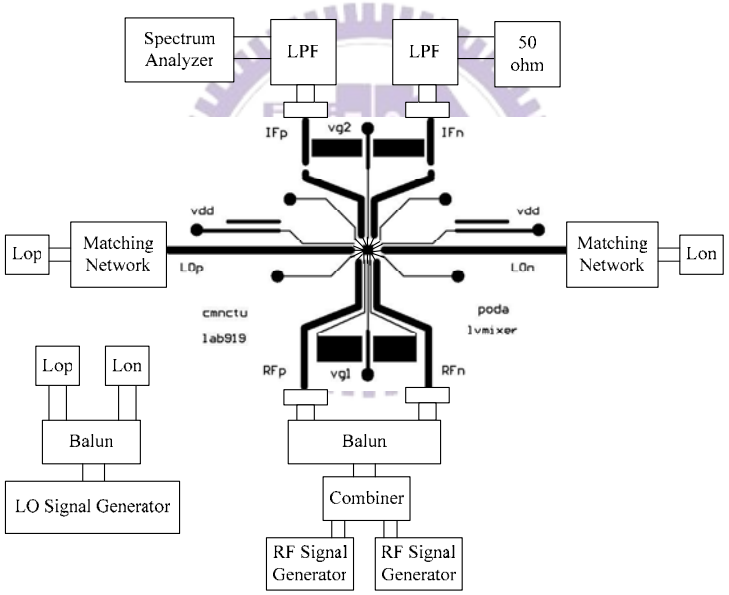


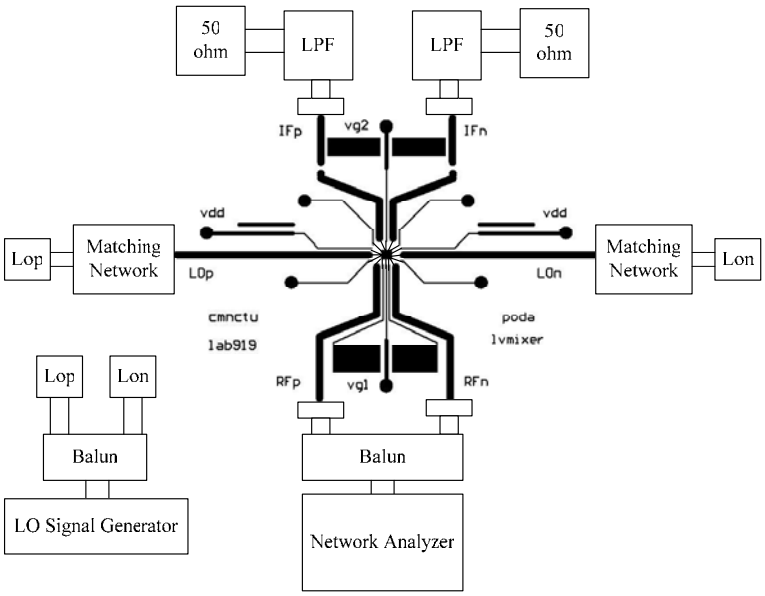
Fig.3.10 Photograph of low voltage mixer


Spectrum Analyzer or Oscilloscope
LPF
LPF
50 ohm
IFp
vg2
IFn
vdd
vdd
Lop
Matching Network
LOp
LOn
Matching Network
Lon
cmnctu
lab919
poda
lvmixer
Lop
Lon
RFp
vg1
RFn
Balun
Balun
LO Signal Generator
RF Signal Generator

(a)


Spectrum Analyzer
LPF
LPF
50 ohm
IFp
vg2
IFn
vdd
vdd
Lop
Matching Network
LOp
LOn
Matching Network
Lon
cmnctu
lab919
poda
lvmixer
Lop
Lon
RFp
vg1
RFn
Balun
Balun
LO Signal Generator
Combiner
RF Signal Generator
RF Signal Generator

(b)



(c)

Fig.3.11 Measurement setup of (a) Conversion gain (b) IIP3 (c) Input return loss

The practical measurement picture is shown in Fig.3.11 which include of the mixer, PCB board, Balun and cables.

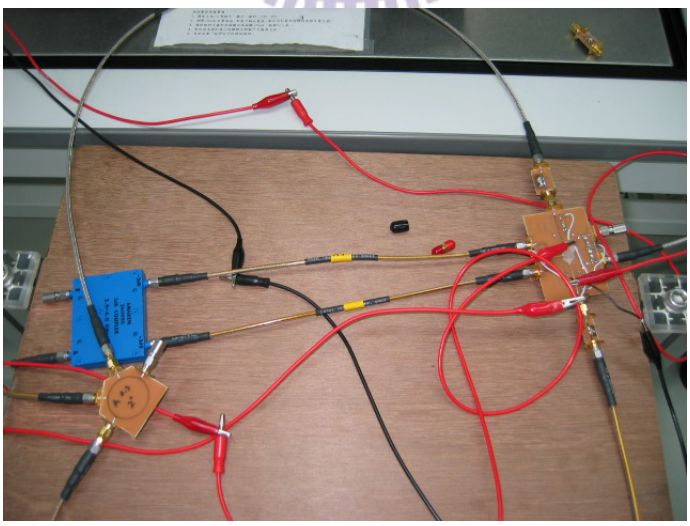


Fig.3.12 Measurement picture

To find out the loss of RF port to IF port, and confirm if the loss would affect the circuit performance, we utilize the 50Ω line testing board for the loss testing. The loss of board and SMA connectors are about 0.4dB. The practical picture and measurement result are shown in Fig.3.11 and Fig.3.12. Furthermore, the loss of cable and Balun is calculated and compensated in CIC RFIC measurement system.

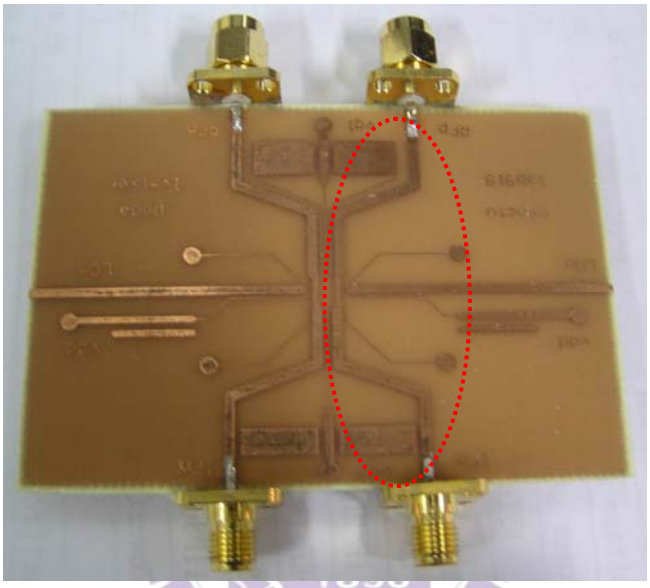


Fig.3.13 Loss testing board

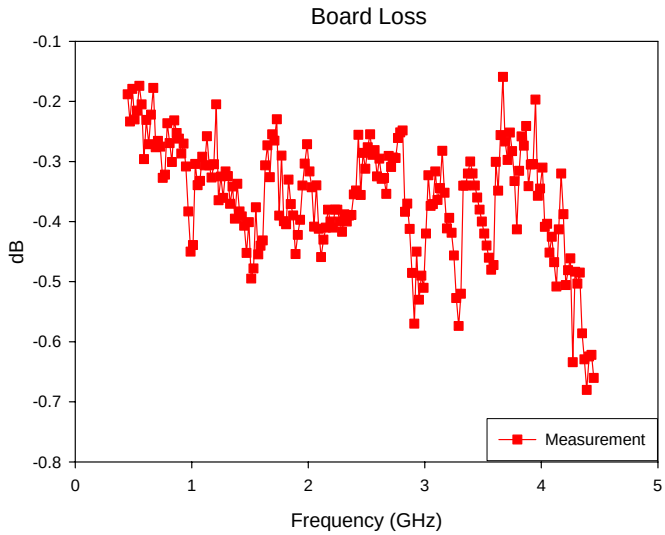


Fig.3.14 Measurement results of the board loss

3.5 Simulation and Measurement Results Comparison

Upon previous measurement considerations and arrangement, we have made all PCB on-board testing for our design in CIC and our laboratory. It is found that the current in each transconductance stage is 0.2mA, a little larger but close to the simulation result in TT-core. On the other hand, the current in the switching stage is twice than that in simulation. Therefore, we can determine the PMOS transistors in the FF-core. Fortunately, the PMOS transistors act as a switched do not seriously affect the circuit performance. Therefore, we try to increase the bias of the PMOS transistors to decrease their current and make the PMOS transistors more close to the saturation and threshold region. With the supply voltage of 0.7V, the power consumption of the mixer is 2.11mw which is a little larger than the simulation results in the TT corner.

From 0.45GHz to 4.45GHz, the RF port input return loss at 2.45GHz in 50Ω measurement system is -8.9dB as shown in Fig.3.15. The peak value about -14dB is shifting down to 2.35GHz that may come from the larger bond wires inductance in the input network. Although two parallel bond wires are used in the ground pad to decrease the bond wire inductance, the inductance remains larger than we expected. Here, we also add a modified simulation without changing the bias and power to find out the problems caused by frequency shifting. The LO input return loss include additional effect of π-matching circuit is about -12.5dB at 2.448GHz as shown in Fig.3.16. Even though it is 7dB less than the simulation result, -12.5dB must be satisfied for our specification.

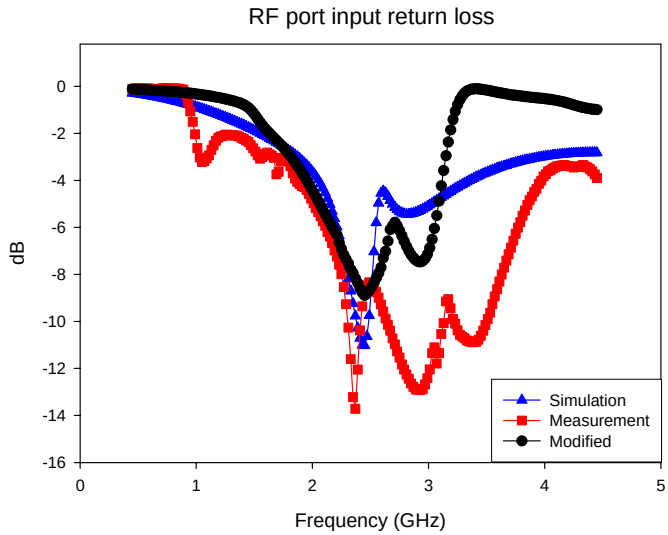


Fig.3.15 Measurement RF port input return loss

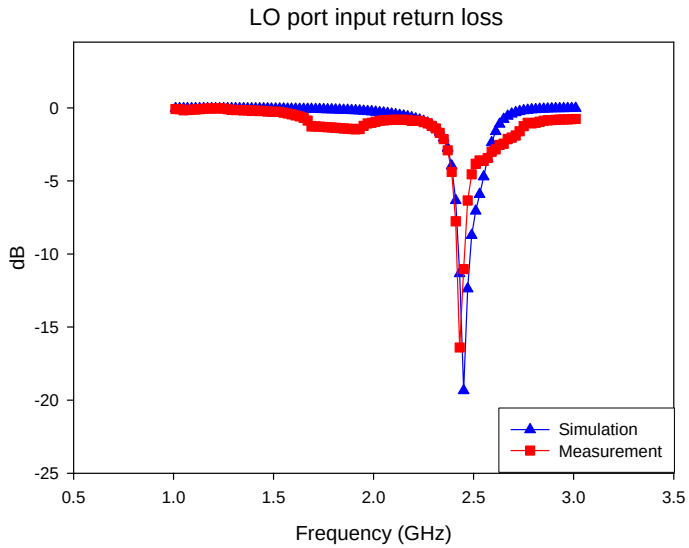


Fig.3.16 Measurement LO port input return loss

When the RF input power is -30dBm and LO power is -3dBm, the measurement output power is only -9.48dB as shown in Fig.3.17. Deduct from the loss of the PCB board, the power gain is -9.08dB. By the modified simulation results shows the frequency shifting in the RF port and the bond wire variation in the LC tank will affect the performance seriously. Although we try to use several length of the bond wire to find the optimum performance of the mixer, we do not successful find this optimum length. Of course, no buffer added in the output so that the mixer could not push the 50Ω load may be another reason.

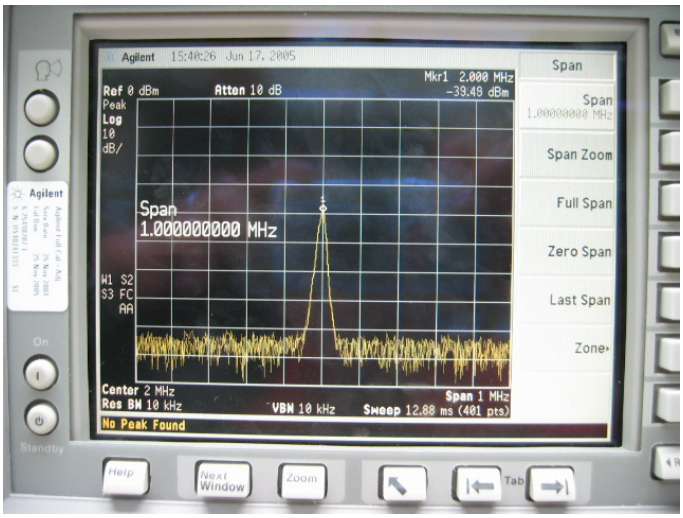


Fig.3.17 Power Gain (RF power =-30dBm, LO power = -4dBm, IF=-39.48dBm)

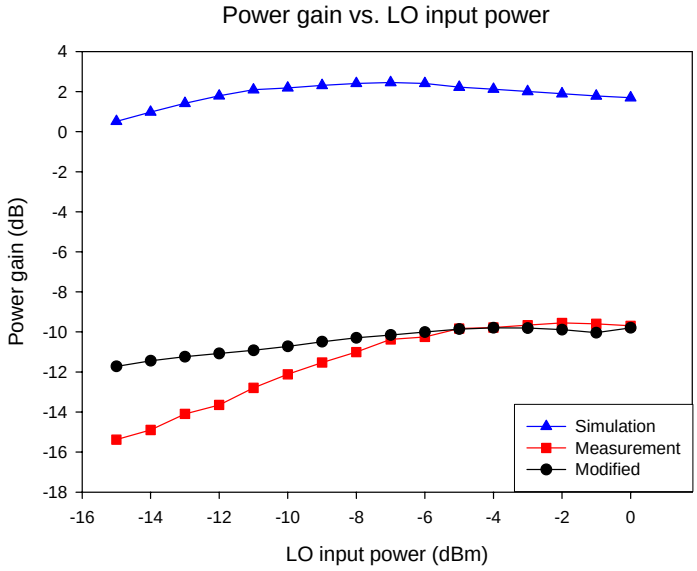


Fig.3.18 Power gain vs. LO power

The linearity is better than simulation due to the low conversion gain. The P1dB is 0dBm and IIP3 is 10dBm as shown in Fig.3.19 and Fig.3.20, respectively. These two measurement results are also close to the modified simulation results. Finally, the IF output waveform is also measured by oscilloscope (1MegΩload), instead of spectrum analyzer (50 Ωload). Fig.3.21 shows that the peak-to-peak voltage of IF output waveform is 22.19mV while the RF input power is -30dBm. By the simple mathematics transform, the mixer exhibits 0.91dB of voltage gain. Because the gain of 50 Ωload and 1MegΩload are measured, we can do a simple calculation to find

out the output impedance of the mixer. After calculation, the output impedance is about 125Ω. This value is smaller than our resistive load of 200Ω. As a result, we can say the smaller load resistor is another reason causes the conversion gain degradation.

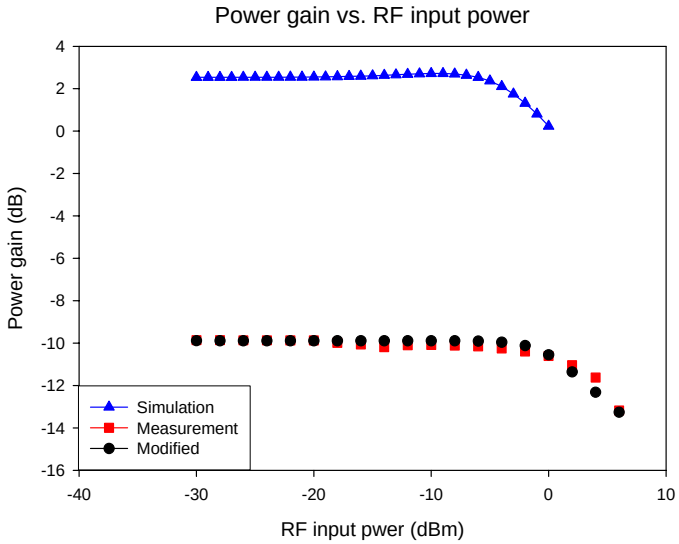


Fig.3.19 Power gain vs. RF power

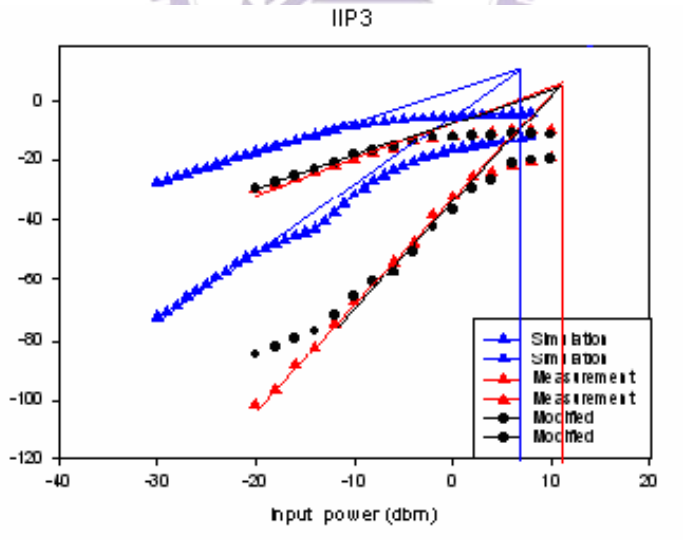


Fig.3.20 Measurement result of IIP3

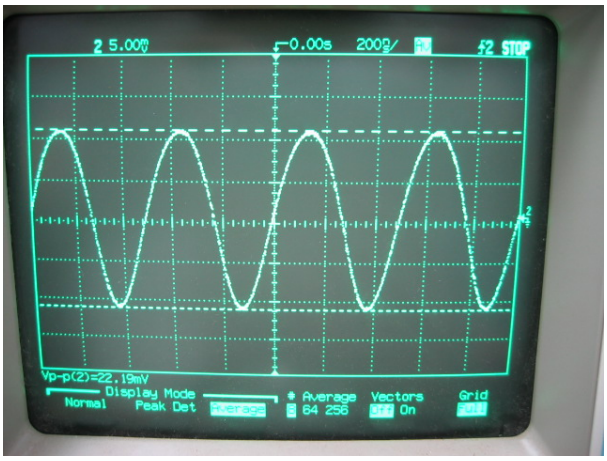


Fig.3.21 IF output waveform

Although the current in the transconductance stage is larger than simulation, the gain is not larger than modified simulation result. This is because of the Gm in the transconductance stage is almost the same as simulation. As shown in Fig.3.22, the Gm value is the slope of the two curves. It is obviously that the slopes of the two curves are almost the same, so Gm of them is almost the same. As a result, the power gain and voltage gain do not increase with the more power consumption of the mixer. There are two main reasons leading to the decrease of power gain and voltage gain. The first is the bond wire in the Vd pad. As described in Sec.3.1, the resonant frequency of the LC tank is dependent with the bond wires. The simulation shows the difference of the two bond wires makes the resonant frequency offset that makes the voltage gain decrease. Second, the frequency shifting in the RF port also affects the performance of the mixer. Last, the smaller load resistor is a factor causes the conversion gain degradation.

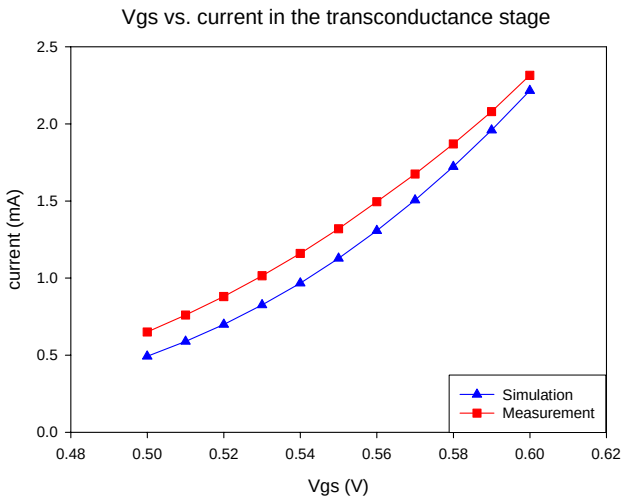


Fig.3.22 The characteristic of Vgs versus current in the transconductance stage

Table 3.2 shows the comparison of this work and recent mixer papers. As we described in Chapter 2, the simulation and measurement data are shown. Although the conversion gain of the mixer is not as high as other design, it is known that an active mixer has a gain of 5dB is enough. The reason why we do not design a high gain mixer is that we try to design a high linearity mixer to compensate the worse linearity performance in our LNA design. Therefore we should decrease the conversion gain to attain better linearity performance. Although the measurement power gain is only -9.08dB, it is obviously that our mixer has the best linearity performance than others. And in the view of the integrated receiver, the load of the mixer is the high impedance of the VGA or IF filter instead of the 50Ω load. Thus, the gain will be increased. Even under a low IF configuration, the noise performance is still better than others. This is because we choose the PMOS type folded cascode configuration that depresses the flicker noise in the switching stage. It is a pity that the noise figure could not be measured in this work. This is because the noise meter in CIC can't operate in the frequency lower than 10MHz. Therefore, we can verify our noise performance. The measurement results show that the power consumption is only 2.11mw with the 0.7V supply voltage that is still lower than the greater part.

Specification	Simulation	Measurement
IF (MHz)	2	2
RF Input RL (dB)	-11.1	-8.9
LO Input RL (dB)	-19.3	-12.5
Voltage Gain (dB)	6.83	0.91
Power Gain (dB)	2.50	-9.08
P1dB (dBm)	-2.5	0
IIP3 (dBm)	8	11
NF (dB)	9.13	NA
LO-to-RF Isolation (dB)	-72.3	-36
Power (mw)	1.84	2.11

Table 3.1 Simulation and Measurement results summary

REF	[28] 2004	[34] 2004	[35] 2003	[36] 2003	[37] 2004	This work 2005.06	
Supply voltage (V)	1.5	1	1	1.8	1.8	0.7	0.7
IF (MHz)	100	1	2	1	20	2	2
Voltage gain (dB)	3.3	11.9	3.5	13.3	9.33	0.91	6.83
IIP3(dBm)	5.5	-3	-1	-1	1	10	8
NF (dB)	15	14	14	16	8.53	NA	9.13
Power (mw)	5.6	3.2	1.4	36	2.88	2.11	1.84
Condition	Sim.	Meas.	Sim.	Meas.	Meas.	Meas.	Sim.

Table 3.2 Comparison of recent mixer papers

Chapter 4
Conclusion and Future Work

4.1 Conclusion

This thesis contains two works：low voltage LNA and mixer. All of the simulation results are finished through Eldo-RF simulator. These two circuits are fabricated in TSMC 0.18 μm CMOS process through CIC. In this thesis, we have presented the design concepts and simulation versus measurement results.

4.1.1 Low Voltage Variable-Gain LNA

The fully integrated 0.7V variable-gain LNA has been designed and presented in this thesis. All measurements were finished through on-wafer measurement at CIC. The power consumption is 7.27mw, being almost the same as the simulation. But, the measurement results show that the LNA only provide a gain of 2.2dB, noise figure of 6.2dB, and IIP3 of 8dBm at the high gain mode. The gain and linearity release can be 6.5dB and 7dBm. The major reason causing the low gain is the frequency shifting of the S11, which only achieves -4.35dB at 2.45G. This may come from the incorrect on-chip model or the large parasitic inductance on the input matching network. However, the low gain performance led to the better linearity performance; IIP3 is 8dBm at high gain mode and 15dBm at low gain mode. Although the measurement results such as S-parameter and noise figure do not meet our expectation, the function of the linearity release is work.

4.1.2 Low Voltage Mixer

The modified 0.7V PMOS type folded cascode double-balanced mixer has been designed and presented in this thesis. All measurement results were finished through PCB on-board testing at CIC. With the 0.7V supply voltage, the mixer exhibits 0.91dB of voltage gain, -9.48dB of power gain, 0dBm of P1dB, 10dB of IIP3, and 2.11mW of power consumption. Although the power gain is not as expected, the high linearity is achieved in this work. These differences may come from the practical rat-race circuit generating deviations of non-equal power and non-180o phase difference, non optimum bond wires in the LC tank and the frequency shifting in the RF port. The measurement results show that the modified low voltage mixer exhibits a low power, high linearity than the conventional Gilbert type mixer architecture.

4.2 Future Work

Fig.4.1 shows the diagram of the purposed ultra low voltage receiver. In this thesis, we have finished the design and measurement of the low voltage LNA and mixer. And there are many important blocks need to be implemented; Synthesizer, VGA, Gm-C filter, demodulator and A/D converter. Because our LNA is not design in the full differential configuration, an on-chip balun should be added to integrate with our differential mixer. Of course, the LNA can be redesigned in the differential topology. But the chip size and the power consumption will increase. Another solution is to design a low voltage micromixer. The RF input stage of micromixer is single-ended and can provide almost the same performance as the Gilbert double-balanced mixer. Therefore, the LNA and mixer can be integrated easily.

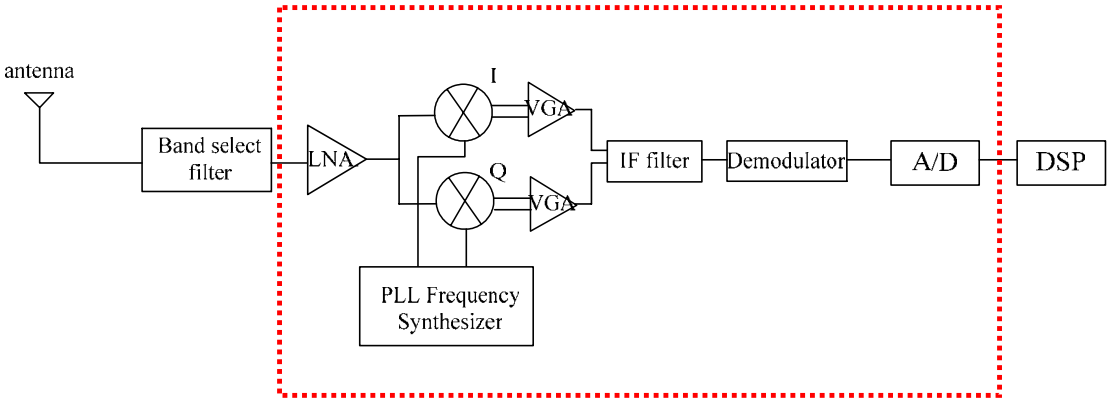


Fig.4.1 The diagram of the purposed ultra low voltage receiver

There are some other future works need to be implemented. First, the accurate RFMOS model and inductor model should be built. Second, the on-chip bias circuit should be designed to reduce the large numbers of DC pads. Final, the ESD protection must be designed within the thinner gate oxide process like modern 0.18 μm CMOS process.

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Appendix
Concurrent Dual-Band Receiver

A.1 Introduction

With the increase demand of wireless communication with low cost and low power, recent research has been focusing on single chip solution. While it is already common to use the CMOS technology to develop base-band circuits, it is gaining popularity to use the CMOS technology to develop RF front-end circuits. As a result, a fully integrated dual-band receiver intended for GPS and Bluetooth is designed in CMOS technology in this work.

Conventional dual-band receiver architectures are achieved by building two individual receiving paths that increase the cost and power consumption [33]. The way to modify these disadvantages is using the concurrent architecture that is capable of simultaneous operation at two different frequencies without dissipating twice power and increase cost. This concurrent architecture can provide simultaneous narrow-band input matching and high gain at two frequency band while maintaining low noise figure.

A.2 Receiver Architecture

Most conventional receivers use individual receiving paths that need large hardware area. If the dual-band receiver uses concurrent architecture, its hardware cost will be high. As a result, the concurrent architecture should be taken into account.

The concurrent dual-band receiver is shown in Fig.A.1. It consists of a dual-band LNA, a dual-band sub-harmonic mixer, a dual-band Voltage-Controlled Oscillator (VCO) and a tunable Gm-C filter. Due to the modulation of the GPS is BPSK, it is either suitable for low IF architecture design [38-39]. Thus, our concurrent dual-band receiver is chosen low IF architecture (2MHZ) to reduce cost and power consumption. In this work, we try to integrate the dual-band LNA and sub-harmonic mixer.

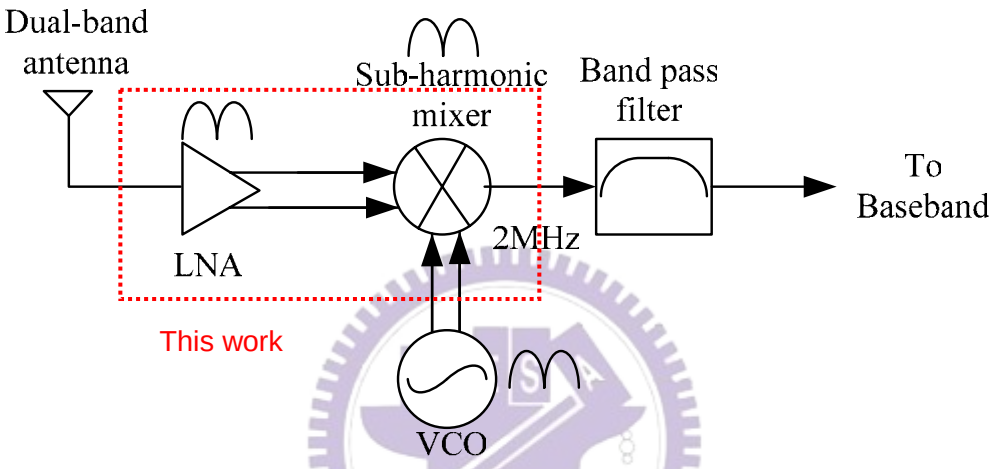
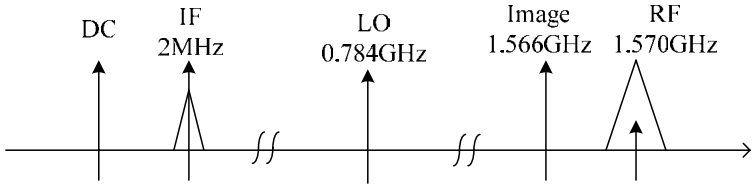
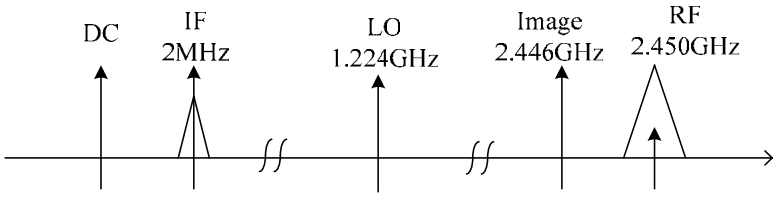


Fig.A.1 Dual-band receiver block diagram

The architecture and frequency plan of the RF transceiver play a critical role and complexity and performance of the overall system. The receiver frequency plan is shown in the Fig.2. The receiver uses a local oscillator (LO) frequency of 0.784GHz and 1.224GHz, translating the input signal from 1.57GHz and 2.45GHz to IF of 2MHz. Because the LO frequency of the sub-harmonic mixer is half of the Gilbert type double balanced mixer, the two LO signals provided by VCO are at close range. Therefore, the dual-band VCO can easily be designed and implemented. Then, the image frequency occurs at 1.566GHz and 2.446GHz and will be cancelled by the tunable Gm-C filter.



(a)



(b)

Fig.A.2 Receiver frequency plan (a) 1.57GHz for GPS (b) 2.45GHz for Bluetooth

A.3 Main Block Description

A.3.1 Concurrent Dual-Band LNA

The concurrent dual-band LNA is shown in Fig.A.3. The low noise and high linearity performance can be achieved by the optimization of M1 and M2, with almost no trade-offs. The optimum width of M1and M2 can be found using Eq.(2.9), where the center frequency is chosen the average of the two desired frequency. After calculation, the optimum width is approach 500μm. The input and output matching network are adding a LC tank and LC branch, respectively. The LC tank in the input is used in order to resonate the gate impedance and to provide the additional lower band gain transfer function [40-41]. The LC branch introduces a zero in the transfer function of the LNA and performs a notch between 1.57GHz and 2.45GHz to improve

receiver's image rejection. To improve the sensitivity of the gate-induced current noise, we add a capacitor Cgs placed in parallel to the intrinsic gate to source capacitor of the input transistor. The insertion of this capacitor adds a degree of freedom to play with to achieve a better compromise between thermal and gate-inducted noise. Therefore, a new optimum condition with a lower noise figure can be achieved. But, this is paid by a slight lower forward gain.

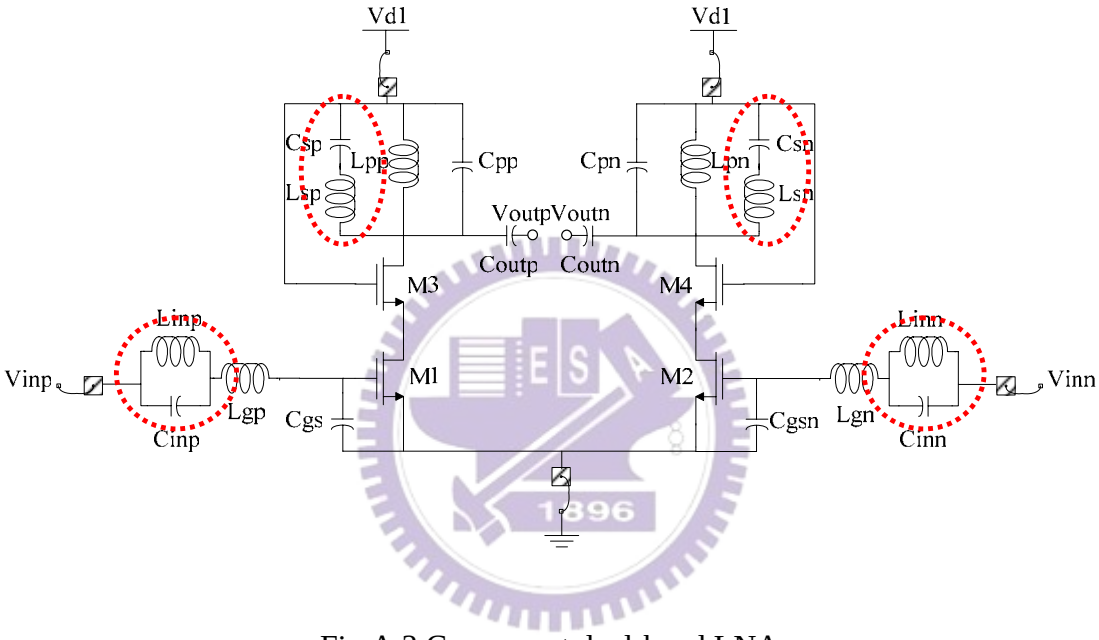


Fig.A.3 Concurrent dual-band LNA

With a 1.8V supply, the LNA achieves power gain of 12.6dB, voltage gain of 20.9dB, S_{11} of -12.7dB, noise figure of 2.98dBm and IIP3 of -1.40dBm at 1.57GHz. And at 2.45GHz, LNA provides power gain of 11.9dB, voltage gain of 20.0dB, S_{11} of -18.7dB, noise figure of 3.35dBm and IIP3 of 1.14dBm at 2.45GHz.The power consumption of the LNA is 18.96mW.

A.3.2 Sub-Harmonic Mixer

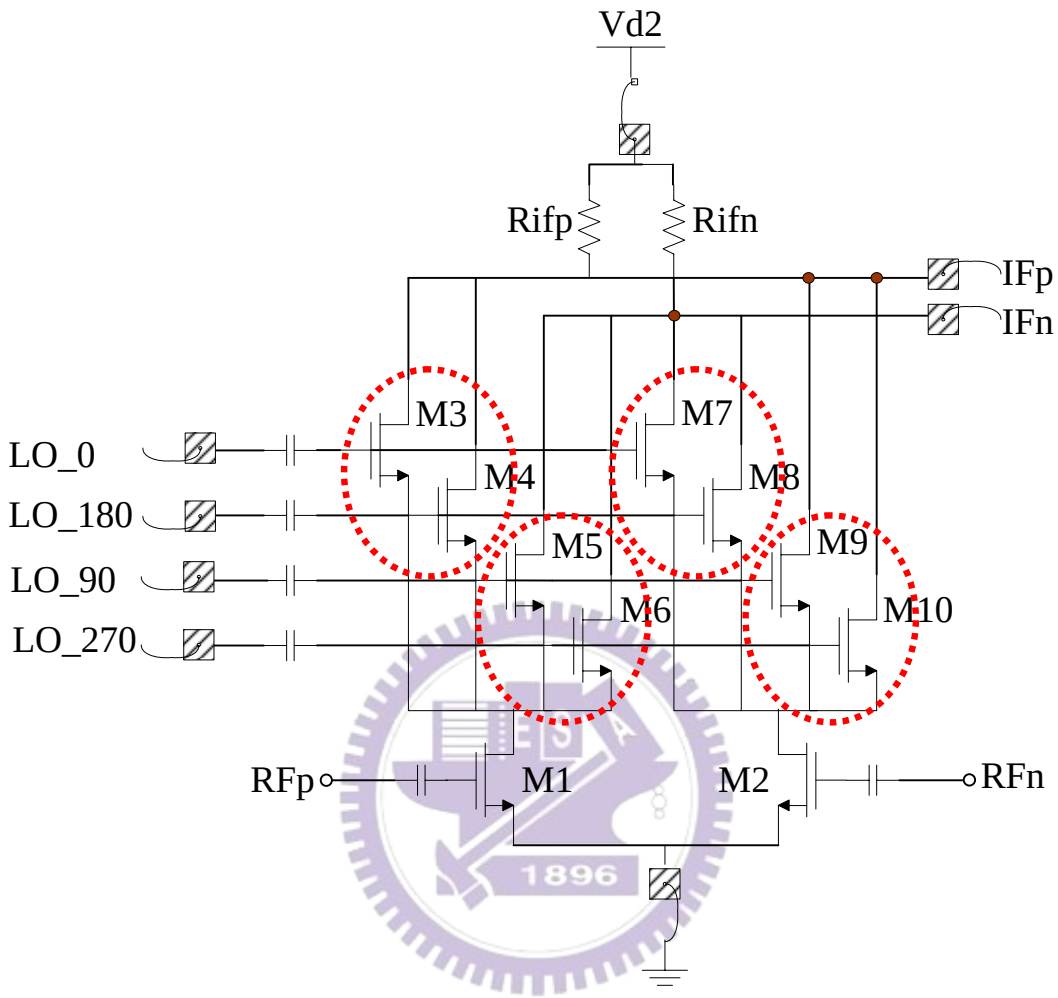


Fig.A.4 Sub-harmonic mixer

Fig.5 shows the schematic of the sub-harmonic mixer. The core of sub-harmonic mixer is the differential pair M1, M2 at RF ports and eight transistors M3 to M10 at LO port, where the LO is applied at roughly half the RF frequency. When operating with LO signals with large amplitude, the LO core acts as a mixer by commutating the load across the drains of the input transconductance stage at twice the LO input frequency. However, the sub-harmonic mixer topology relies on the phase relationship of the LO signals to provide a region where the $0/180^{o}$ and $90/270^{o}$ devices are both off to create the effective twice LO switching frequency. The

quadrature ~F_{RF}/2 signal applied to the LO inputs allows the RF signal to be switched on every quarter cycle of the LO drive waveform, creating an effective $2F_{LO}$ signal [42]. There is no inductor used in the mixer for the small chip size purpose. And, the dual-band LO port matching is realized by using the off-chip element as shown in Fig.A.5.

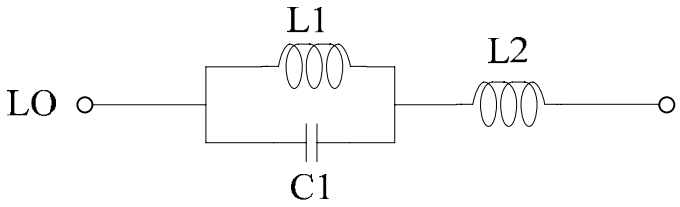


Fig.A.5 Dual-band LO matching network

With a 1.8V supply, the sub-harmonic mixer achieves conversion gain of 2.39dB, noise figure of 8.12dBm, and IIP3 of -5.8dBm at 1.57GHz. On other hand, the mixer provides conversion gain of 1.44dB, noise figure of 9.89dbm, and IIP3 of -5.8dBm. The power consumption is 3.24mW and IF is chosen at 2MHz.

A.4 Layout and Simulation Results

The layout of the dual-band receiver is shown in Fig.A.6. Because the receiver is measured on PCB rather than on wafer, the bond wire and pad parasitic capacitance should be considered. The RF input ports of the receiver are on the left side. The bias of the LNA and the LO input ports are on the top and bottom of the chip. The bias of the mixer and the IF output ports are on the right side. Here, the two circuits are surrounding by a guard ring to avoid the noise coupling. Then, the total chip size is 1.4mm*1.3mm.

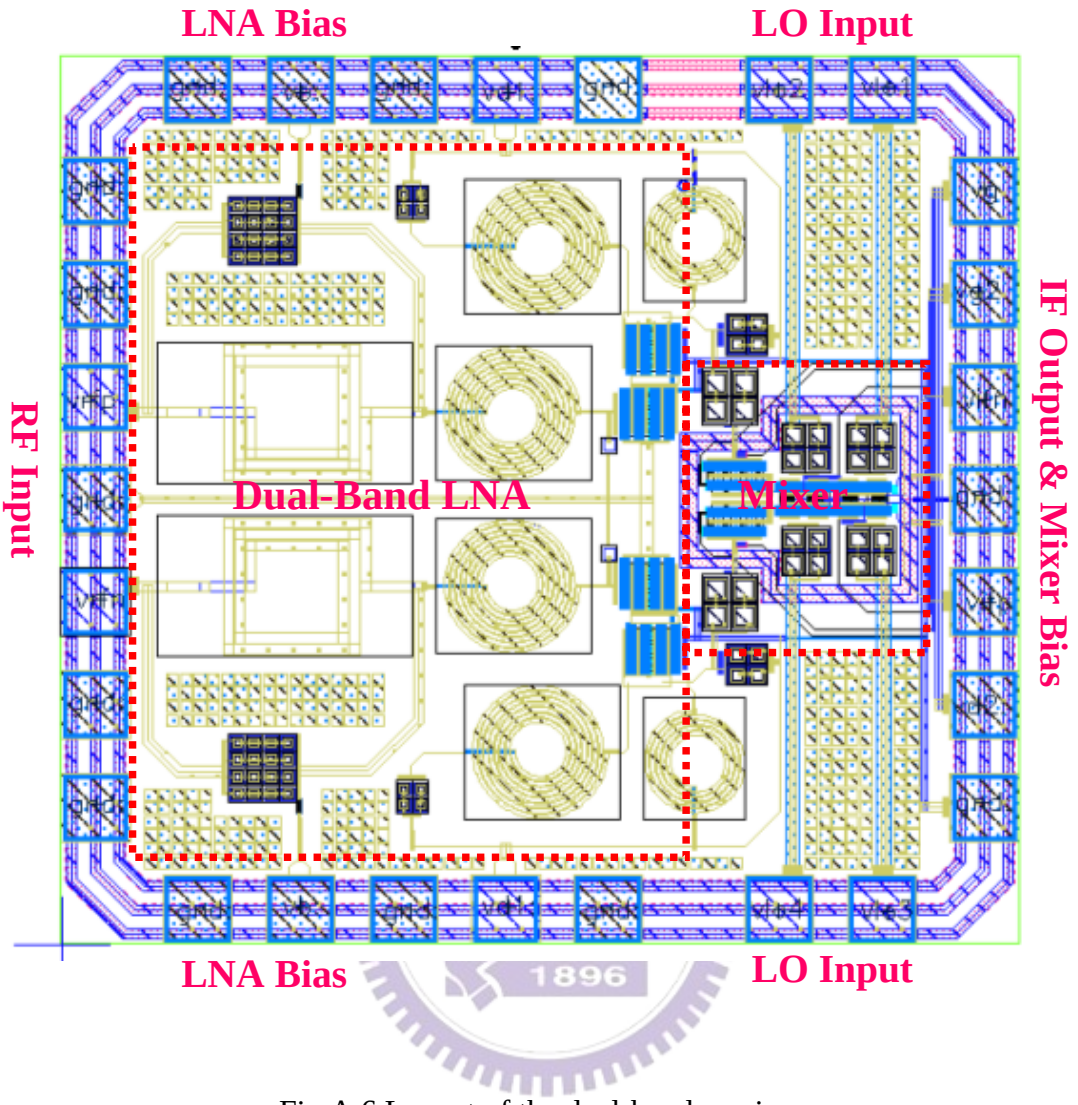
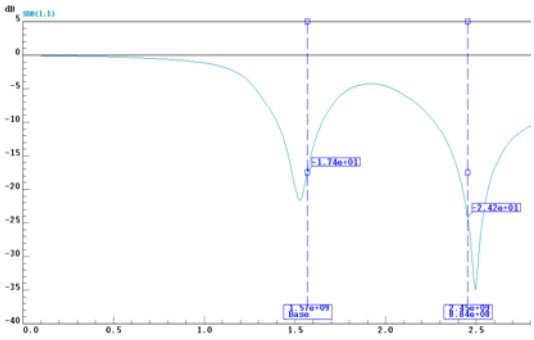
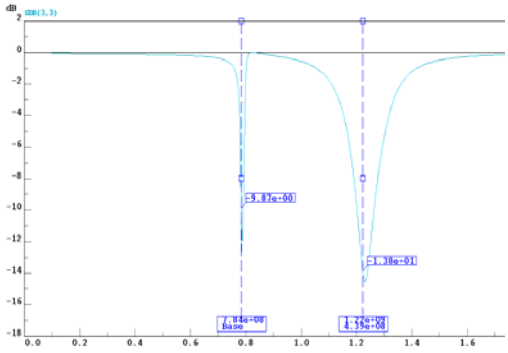


Fig.A.6 Layout of the dual-band receiver

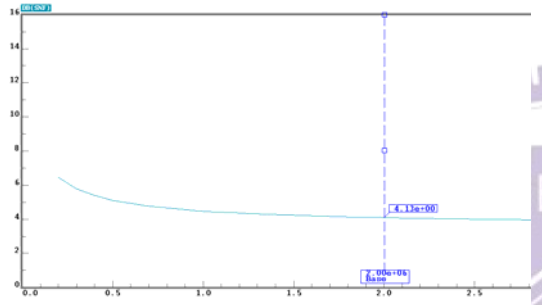
The simulation results are shown in Fig.A.7. The voltage gain of the receiver is 27.7dB at 1.57GHz and 24.2dB at 2.45GHz. The noise figure is 4.13dB and 6.84dB, the p1dB is -29.9dBm and -24.4dBm, IIP3 is -19dBm and -16dBm, and the total power dissipation is 22.2mw. And the summary of the simulation results are in the Table A.1.



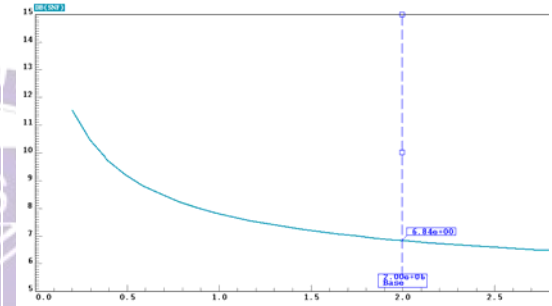
(a) RF input RL



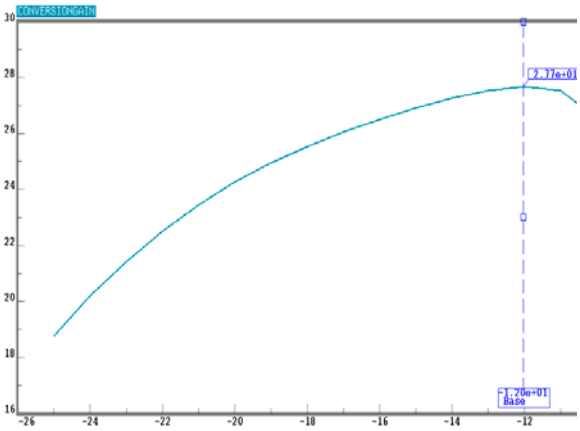
(b) LO input RL



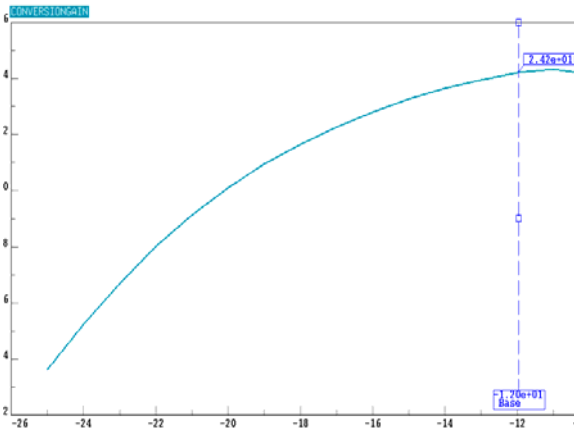
(c) NF @ 1.57GHz



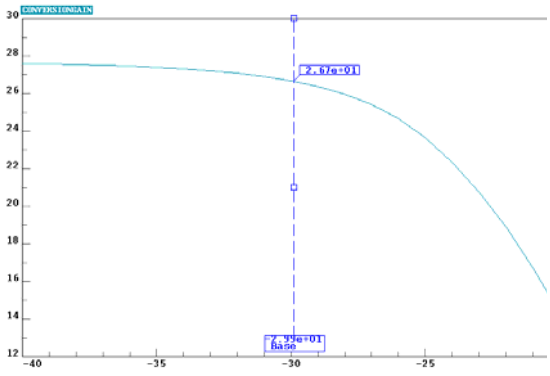
(d) NF @ 2.45GHz



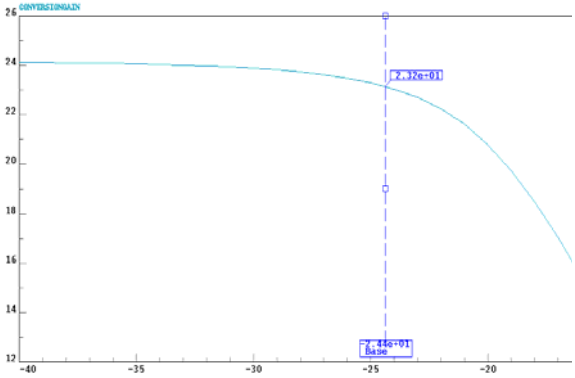
(e) Gain vs. LO power @ 1.57GHz



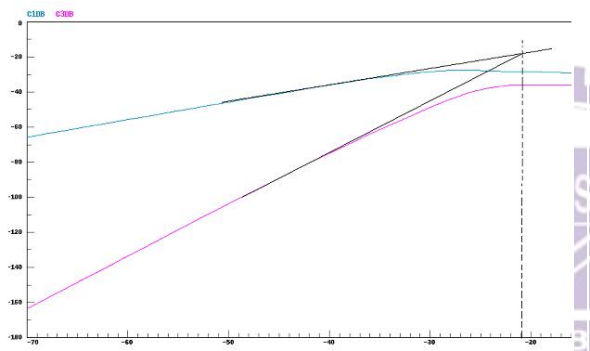
(f) Gain vs. LO power @ 2.45GHz



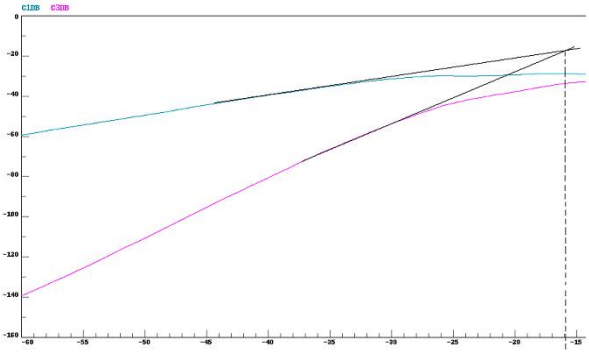
(g) Gain vs. RF power @ 1.57GHz



(h) Gain vs. RF power @ 2.45GHz



(i) IIP3 @ 1.57GHz



(j) IIP3 @ 2.45GHz

Fig.A.7 Simulation results

Specification	@ 1.57 GHz	@ 2.45 GHz
RF Input RL (dB)	-17.4	-24.2
LO Input RL (dB)	-9.87	-13.8
NF (dB)	4.13	6.84
Voltage Gain (dB)	27.7	24.2
P1dB (dBm)	-29.9	-24.4
IIP3 (dBm)	-19	-16
Power (mw)	22.2mw	

Table A.1 Concurrent dual-band receiver simulation results summary

The specification of the GPS is conversion gain>85dB, NF<5dB, IIP3>-20dBm. And the specification of Bluetooth is conversion gain>50dB, NF<8dB, IIIP3>-16.5dBm. By the simulation results, the NF is in the specification of the two applications. The conversion gain would be amplified by the IF amplifier or the variable gain amplifier (VGA). In general, the gain of the IF amplifier or VGA can be higher than 60dB. Therefore, performance of the conversion gain would be in specification too. But the linearity of the GPS is 1dBm lower than the specification and closely to the boundary of the specification. The main reason is the linearity of the mixer is not good enough that decrease the overall linearity. This could be modified by decreasing the gain of the LNA or mixer to increase the linearity. But consider the bad noise performance; we do not do this correction. Another solution is modified the topology of the mixer- adding an inductor between the drains of the

transconductance stage (M1, M2) to enhance the linearity. Because this modify will increase the chip area, we do not choose this change. We do the modification on the other way; do more strictly on the linearity of the VGA that would modify the linearity of receiver