國立交通大學

電機工程學系 電信工程研究所

博士論文

具立體通道之矽奈米級金氧半場效應電晶體本質參數擾動之研究

Intrinsic Parameter Fluctuation in Nanoscale MOSFET with Vertical Silicon Channels

研 究 生：黃至鴻

指導教授：李義明　教授

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摘要

延續摩爾定律而獲得高性能矽晶片以及高密度元件之觀點，新材料、新製程與新結構的開發是半導體製造上繼續微縮元件的尺寸最有效的策略方案；其中，16 奈米之後電晶體結構的改變儼然已成為非常前瞻與重要的趨勢，因此研究隨機摻雜問題與製程變異在多重閘極場效電晶體特性之影響已為重要且急迫之課題之一。因此本論文發展了三維度元件電路模擬技術使用等效原子層級離散摻雜暨量子傳輸方程的大尺度統計運算方法，並成功地分析 16 奈米立體矽場效應電晶體特性之擾動由單閘極、雙閘極、三閘極至全閘極電晶體。此研究方法之準確度已成功地以次 20 奈米矽場效應電晶體特性之實驗驗證。相較於單閘極電晶體，臨界電壓擾動在雙閘極、三閘極至全閘極分別被壓抑 2.2、3.3 與 4 倍，壓抑的原理及物理特性均有探討。此外，近來金屬閘極與高介電係數材料的使用已成為奈米電晶體元件開發之重要課題，但金屬閘極的使用將因金屬材料本身結晶顆粒的大小與方向帶來另外的擾動來源，因此本論文發展蒙地卡羅方法廣泛的分析閘極功函數擾動、離散摻雜擾動與製程變異在多重閘極場效電晶體特性暨其電路之影響，發現閘極功函數擾動對於金屬閘電晶體尤其是 p-type 元件之重大影響，此論文結果對於電晶體擾動壓抑之推估以及下世代電晶體特性擾動分析極有助益。

Abstract

Gate-length scaling is still the most effective way to continue Moore's Law for transistor density increase and chip performance enhancement. Accompanied with complementary metal-oxide-semiconductor (CMOS) technology advanced to 32-nm node in production, further scaling down to sub-20 nm and even beyond has been widely noticed encountering much more challenges at short channel control than previous generations. The worsened short channel control of nanoscale transistor not only increases standby power dissipation, but also enlarges electrical characteristic fluctuations, such as the deviation of threshold voltage, drive current, mismatch, and so on. The fluctuation budget has to be controlled even tighter due to doubly increased transistor number along with technology node moving ahead. Moreover, the fluctuation is intrinsically increased with the scaling of transistor feature size, even not considering worsened short channel control. This thesis describes the intrinsic parameter fluctuations in vertical-channel devices from planar transistor to

double gate, tri-gate, omega fin-type field effect transistors (FinFETs) and nanowire FinFETs through experimental validated three-dimension device simulation and characterization. The implication of device variability in nanoscale transistor circuits are advanced. The extensive study assesses the fluctuations on device and circuit reliability, which can in turn be used to optimize nanoscale MOSFET and circuits. Full realization of the benefit of nanoscale transistor therefore requires development and optimization of new device materials, structures, and technologies to keep transistor performance and reliability.

誌謝

六年前的夏天，回憶的片段像口試時撥放的投影片，一頁頁略過我的腦海。當初那個羞澀中帶有點稚氣的年輕人又映入我的眼簾，背景的圖案從工程四館、電資大樓、校門口的土地公廟到交大的校園的每一處不停的變換，中間閃過了日本、希臘、法國、美國等充滿異國風情的背景，最後回到了一張多人的大合照。曾幾何時，那笨拙稚氣的年輕人已穿上了西裝露出微笑，眼角泛著淚光，曾幾何時，那本來瘦弱的臂膀已變得強壯而結實，這一切的一切都要感謝照片中所有人的陪伴、支持與鼓勵。

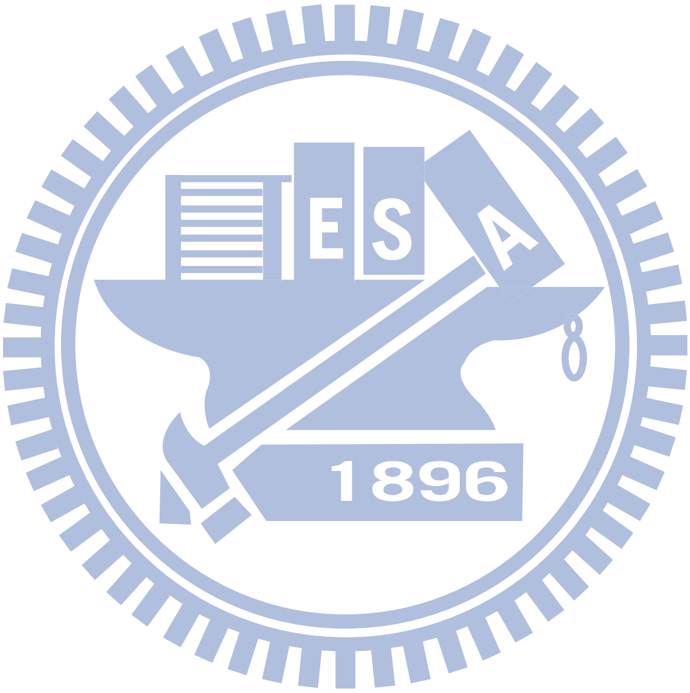
年輕人右手邊的是他的指導教授　李義明老師，他是帶給照片那位年輕人影響最多的人。多年的悉心指導、專業知識的傳授、研究方法的推敲、用字遣辭之斟酌以及為學處世待人接物謹慎積極的態度，讓那位年輕人在治學方法及處世態度上受益良多，尤其是在論文發表時常退居幕後，讓學生站在國際的舞台上發光發熱，更是年輕一輩學子日後之表率。值得一提的是李老師右手邊的 周復芳老師與　李育民老師，兩位老師在修業期間提供的教誨與最大的自由度與支持讓學生得以進行感興趣的研究。在幾位老師身旁的是論文口試期間提供寶貴意見與殷切指正讓論文更臻完備的成大電機工程學系 王水進老師、清華大學電機工程學系 白田里一郎老師、清華大學工程與系統科學系 張廖貴術老師與交通大學電子工程學系 陳明哲老師。師恩細長，深切銘心，學生在此謹獻上最誠摯的感謝與敬意。

年輕人的左手邊是他平行科學計算實驗室的好伙伴：正凱、紹銘、素雲、惠文、益廷、大慶、宣銘、典燁、毓翔、英傑、國輔、銘鴻、紀寰、忠誠及俊諺，正凱學長神人般留傳的程式庫、紹銘學長的熱情教學與呵呵微笑、同窗好友的互相砥礪，如繞樑之音盤旋在腦海。年輕人身後還有他一群共患難的朋友：金玲、逸宏、闡哥、酷桑、阿琅、小宇、培育、哲宇、獻哲，謝謝你們，尤其是金玲，與妳在一起的六個年頭，有苦有笑點滴在心頭，謝謝妳一路的陪伴。感謝這群陪伴我渡過許多困難的好友，學業的路上沒有你們，再美好的風景都覺得索然無味。畫面轉回到身後的家人，感謝之詞溢於言表，謝謝你們在背後默默的支持與忍耐，你們是我最大的力量來源，讓我在疲憊的時候給我最大的鼓勵與支持，請讓我用行動表達心中的感謝。

投影片到了最後的一頁，感謝行政院國家科學委員(計畫編號：NSC-96-2221-E-009- 210、NSC- 95-2221-E-009-336、NSC-95-2752-E-009-003-PAE、 NSC-97-2221-E-009-154- MY2)、卓越延續計畫(計畫編號：NSC-95-2752-E-009-003-PAE、NSC-96-2752-E-009-003-PAE)、五年五百億計畫、群創光電股份有限公司、台灣積體電路製造股份有限公司產學研究計畫之經費補助。感謝台積電楊副處長富量博士（現國家奈米元件實驗室主任）與黃經理俊仁博士提供研究上的協助。能順利完成博士學業，全靠父母、家人及諸位朋友、同學的支持與忍耐，對此由衷感謝，謹在此將本論文獻給關心我的人。

黃至鴻　謹誌

中華民國九十八年十月　于交通大學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Chapter 1

Introduction

This chapter presents an introduction of this thesis. It begins with an introduction of nanoscale transistors, and its structure evolution from planar device to vertical channel, such as double-gate, triple-gate, and surrounding-gate transistors. The literature review of current research status and motivation are then introduced.

1.1 Toward Nanoscale Transistor Era

Evolution of complementary metal-oxide-semiconductor (CMOS) technology in the past 40 years has followed the path of device scaling for achieving density, speed and power improvements. The 2007 International Roadmap for Semiconductors (ITRS) projected that sub-l0-nm-gate length will be launched before 2015[l]. The most critical issues for continuing the device scaling will be performance enhancement (short channel effect, leakage current, power consumption, and so on) and yield (intrinsic parameter fluctuations). In the past several decades, planar metal-oxide-semiconductor FETs (MOSFETs) have been the core of very-large-scale integration (VLSI) circuits and memories [2,3]; however, as gate length scales, they started to suffer from undesirable short-channel effects (SCEs) in scaled dimensions. The significant SCEs not only increases standby power dissipation, but also enlarges electrical characteristic fluctuations, such as the deviation of threshold voltage, drive current, mismatch, and so on. Various technologies, such as, mobility enhancement [4,5], metal-gate with high-κ dielectrics [6-8], optimal doping profile design [9-11], lithography [12-14], vertical channel transistor [15-39], have been proposed to enhance the transistor performance.

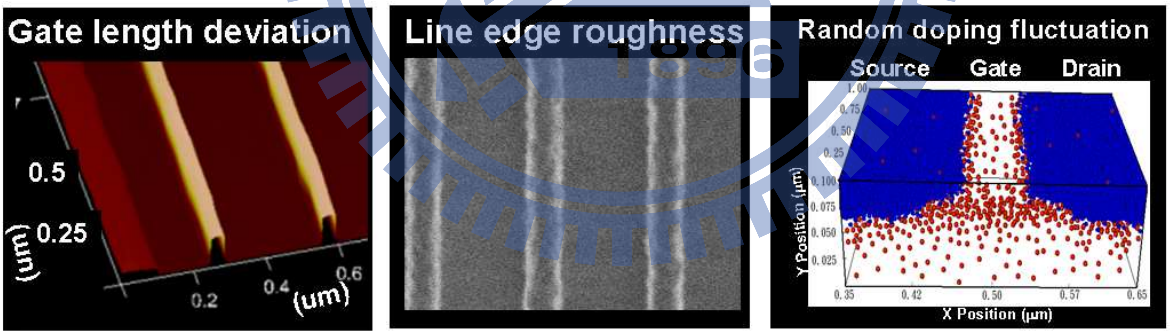


Figure 1.1: The major sources of intrinsic parameter fluctuations: the gate length deviation, line edge roughness, and random dopant fluctuation [15].

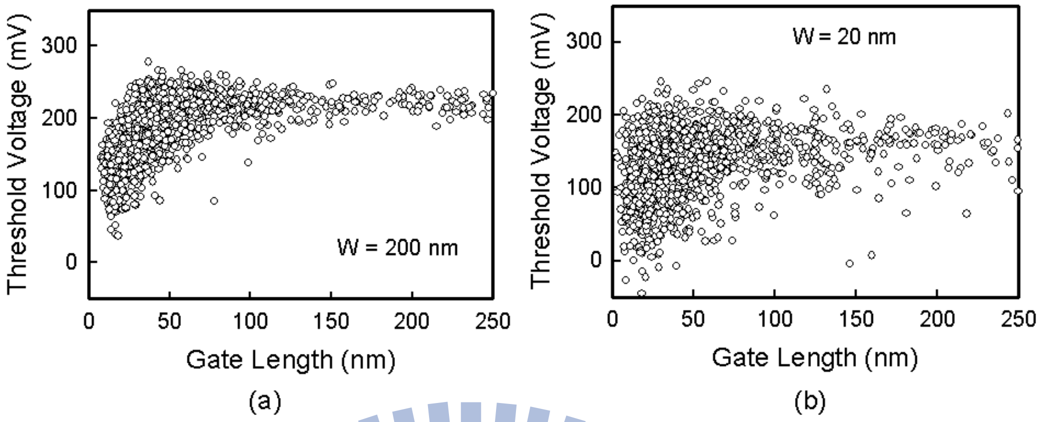


Figure 1.2: Experimental saturation threshold voltage of NMOSFETs with L_g down to 20 nm for the (a) width = 200 nm and (b) width = 20 nm at V_D = 1.0 V.

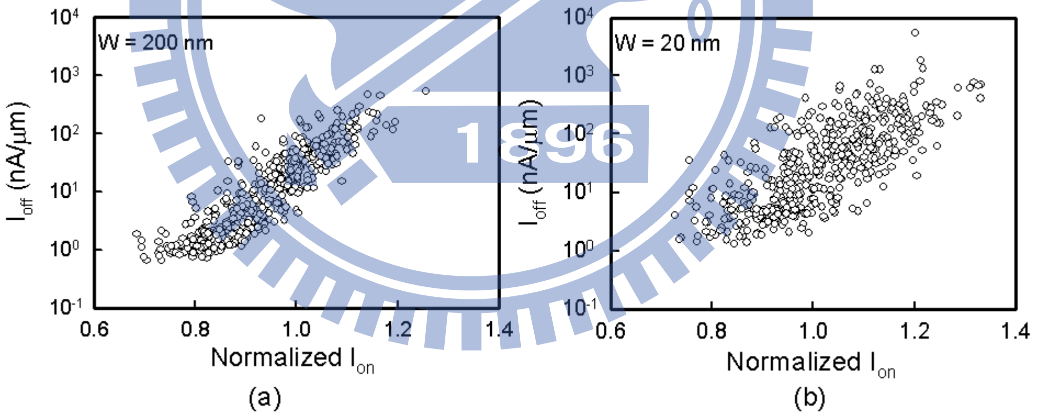


Figure 1.3: Experimental I_{on}-I_{off} characteristics of NMOSFETs with L_g down to 20 nm for the (a) width = 200 nm and (b) width = 20 nm at V_D = 1.0 V. The I_{on} was normalized against the on-current of nominal L_g case, i.e. the 20 nm L_g case.

Gate lengths of scaled MOSFETs are now under 30 nm in 45-nm node high-performance circuits [5,40-43]. Transistor scaling down to sub-20 nm and even beyond has been widely noticed encountering much more challenges at short channel control than previous generations. The worsened short channel control enlarges electrical characteristic fluctuations, such as the deviation of threshold voltage, drive current, mis-match, and so on. Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, variations in the process parameters, etc., are known as indispensable components of the circuit design methodology [44-48]. Additionally, the fluctuation is intrinsically increased with the scaling of transistor feature size, even not considering worsened short channel control [15,20-27]. Figure 1.1 shows the major sources of intrinsic parameter fluctuations, including the gate length deviation [15, 27, 36, 57-61], line edge roughness [15, 27, 36, 57-61], and random dopant fluctuation [21-27,62-89]. The fluctuation caused by granularity of the poly-silicon gate [90-93], silicon film thickness variation [94,95], and random telegraph signal [96,97] are also important factors in device intrinsic fluctuation, which dependents on the device structure. Figures 1.2 and 1.3 show the experimental V_{th} fluctuation and the on- and off-state currents (I_{on}-I_{off}) characteristics of the n-typed MOSFETs (NMOSFETs) down to 20 nm gates. The gate length L_g values in Fig. 1.2 are estimated from the gate capacitances in analysis data, and we presume the widths of all samples in Figs. 1.2(a) and 1.2(b) are 200 nm and 20 nm, respectively. As expected, the

σV_{th} roll-off characteristics of 20-nm-wide devices are much more scattered than that of 200 nm-wide devices. Notably, in Fig. 1.2, the maximum V_{th} difference for 20-nm-gate length device has approached 150 mV, which is larger than the desired V_{th}, 140 mV. The I_{on}-I_{off} characteristic fluctuation becomes even worsened in Fig. 1.3. The maximum V_{th} difference for 20-nm-gate length device is over 250 mV; moreover, in some cases, their V_{th} are zero and can not be used in circuits and systems.

1.2 Vertical Channel Transistor Architecture

As the gate lengths of MOSFETs scales below sub-30 nm, the Field effect transistors (FETs) with multiple-gate structures, such as fin-type FETs (FinFETs) have been of great interest due to the excellent controlling ability of carriers in the device's channel, which suppressed the short-channel effect [15-17]. The succession of device structure from planar to vertical channel transistors has become the main trend in VLSI technologies. Figure 1.4 plots an evolution of transistor architecture from planar MOSFETS to ultra-thin-body silicon-on-insulator (UTB SOI), double-gate, omega gate, and nanowire FinFETs. The transistors with vertical channel are with large gate-to-channel coverage ratio and have very thin body to control short-channel-effect.

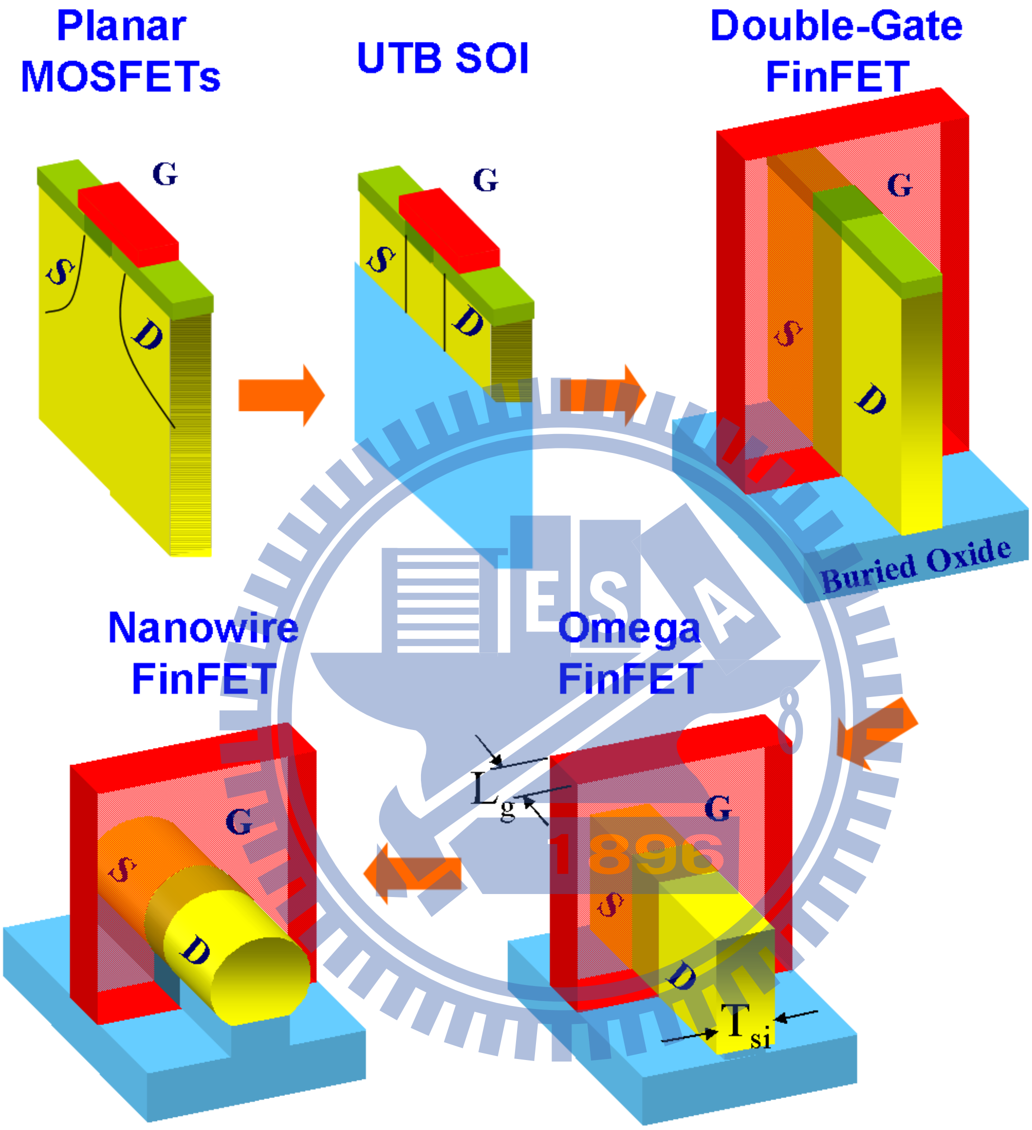


Figure 1.4: The evolution of transistor architecture from planar MOSFETs to ultra-thin-body silicon-on-insulator, double-gate, omega gate, and nanowire FinFETs.

1.2.1 FinFET Process Steps

This section presents the manufacturing process of 25-nm-gate FinFETs. The process result is exhibited. The process simulation is similar to the sub-10-nm-gate nanowire FinFETs in [15-17,20], which is the state-of-art nanowire FinFETs transistor. The process flow used in this work is summarized:

1. Si fin and STI patterning, T_{si} trimmed down upon STI etching;
2. Well and threshold voltage implantation;
3. Gate oxide growth (physical thickness 1.4 nm);
4. Gate deposition (in-situ doped N^+ poly silicon);
5. Poly Si chemical mechanical polishing;
6. Gate hard mask deposited and patterning (Hard mask trimmed down upon etching);
7. Poly gate etching;
8. Pocket and lightly doped drain (LDD) implantation;
9. Oxide/Nitride combo spacer formation;
10. Source/Drain implant;
11. Low-thermal-budget activation process;
12. Contact formation; and
13. Copper interconnect.

After Si fin patterning and shallow-trench isolation (STI) formation, the device width is trimmed down upon STI etching. Well and threshold voltage implantation are performed to adjust threshold voltage (V_{th}) of transistor. Then, to relieve the etch damage, a sacrificial oxide is removed before gate oxidation. Thermal oxide is grown and in-situ heavily doped N^+ poly-silicon is deposited. After the deposition and trimmed down of gate hard mask, the pocket and lightly doped drain (LDD) implantation techniques are used for the suppression of the short channel effect and hot carrier effect. Composite spacer of silicon oxide and nitride is deposited and etched anisotropically. After the gate and spacer formation, heavily doped N^+ junction are made with Phosphorous implantation. Low-thermal-budget activation process is used for dopant activation and control of doping profile. After inter-layer-dielectric deposition, wolfram is used for metal contact plugging and copper is used for interconnection. Finally, alloying anneal is performed. We notice that the narrow width device trimmed down upon STI etching and low-thermal-budget activation process are the critical steps in fabrication of nanoscale FinFET transistor.

1.2.2 Process Simulation Using TCAD

The process simulation of FinFET is presented by using TCAD simulator [134]. Figure 1.5 presents the simulation result. After the Si fin patterning, STI patterning, and trimming, a silicon fin with substrate are formed, as displayed in Fig. 1.5(a”). The dark brown region in Fig. 1.5(a) and white region in Fig. 1.5(a’) are SiO_2. The doping concentration in this step is background doping with 1.0×10^{15} cm^{-3} boron concentration. Figures 1.5(b)- 1.5(b”)

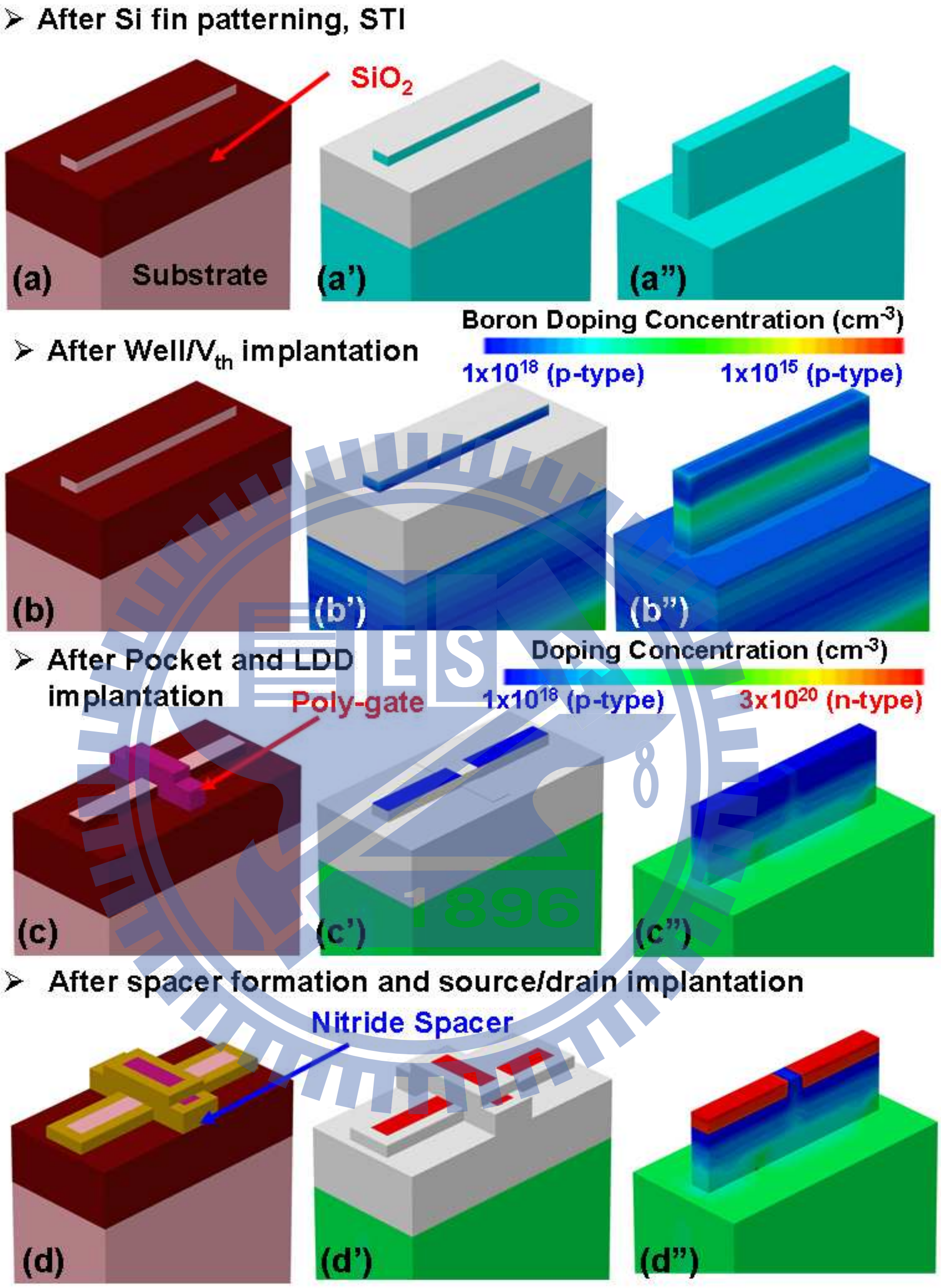


Figure 1.5: The process simulation result for FinFETs. ((a)-(a"))The device structure after Si fin patterning, STI. The doping concentration in this step is background doping with 1.0×10^{15} cm^{-3} boron concentration.((b)-(b"))After Well/V$_{th}$ implantation and annealing, the dopants are activated after thermal annealing. The fabrication process then goes to gate formulation, pocket and LDD implantation. The gate oxide is formulated after the gate oxide growth ((c)-(c")). ((d)-(d"))After spacer formation and source/drain implantation, the final device structure is shown.

shows the doping concentration after the well and threshold voltage implantation. The dopants are activated after thermal annealing. The fabrication process then goes to gate formulation, pocket and LDD implantation. The gate oxide is formulated after the gate oxide growth, as shown in Fig. 1.5(c'). The structure of heavily doped poly-silicon gate is then constructed and displayed in Fig. 1.5(c). The results of spacer and final source/drain implantation are presented in Fig. 1.5(d)- 1.5(d").

1.3 Current Research Status and Motivation

This section reviews the current status of research and problem. Then the motivation of this thesis is drawn. The problems is first addressed as below.

1. There have been many studies of the intrinsic parameter fluctuations, including the process variation [15,27,36,57-61], random dopant fluctuation [21-27,62-89], and poly-silicon gate [90-93] on planar MOSFETs. However, the studies of FinFETs fluctuation is not enough [15,23,27,55,84]. Moreover, the extensive exploration of multi-gate channel transistor as well as comparison with planar MOSFETs are lacked.
2. The use thin gate oxide becomes an important alternative research object [63] to further suppress the impact of fluctuation. Figure 1.6 shows the gate length deviation, line edge roughness, and random dopant fluctuation induced V_{th} fluctuation versus

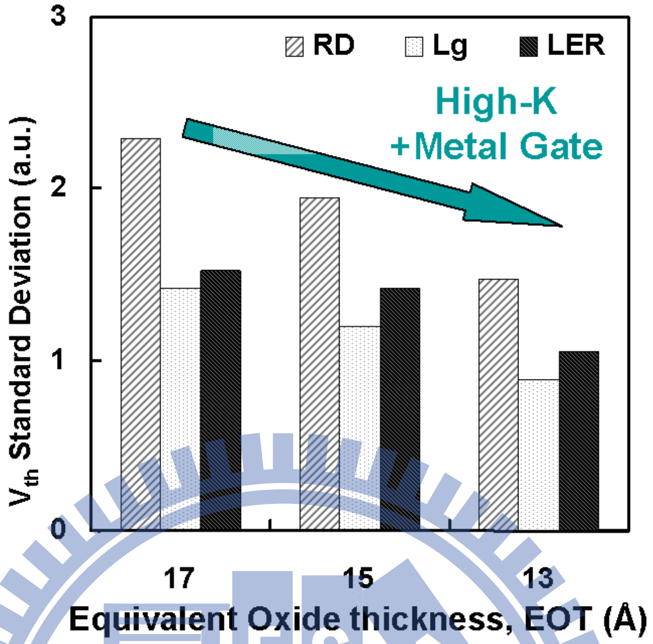


Figure 1.6: The gate length deviation, line edge roughness, and random dopant fluctuation induced V_{th} fluctuation versus equivalent oxide thickness (EOT).

equivalent oxide thickness (EOT). The EOT reduction can be achieved by the introduction of metal-gate and high-κ dielectric for low standby power devices. All of the comparisons are based on the same off-sate (leakage) current. In principal, the standard deviation of V_{th} induced by the three aforementioned sources can all be reduced with decreased gate dielectric thickness, due to less surface potential perturbation under the enhanced gate controllability. This improvement will depend on implementation of reliable high-κ gate dielectrics and well work-function modulated metal gate.

3. High-κ/metal-gate technology has been recently recognized as the key to sub-45 nm transistor fabrication due to the small gate leakage current with an increased gate capacitance. Moreover, the sheet resistance is reduced with the use of metal as gate material. Comparing to the poly-gate technology, the metal-gate material will not react with high-κ material and therefore there existing less interface charge and V_{th} pinning effect. The gate depletion in poly-gate material is no longer existed. Additionally, the phono scattering effect is significantly reduced due to the less quantum resonance effect. However, the use of metal as a gate material introduces a new source of random variation due to the dependency of workfunction on the orientation of metal grains [121,122]. The grain orientation of metal is uncontrollable during growth period.
4. The use of vertical channel transistor to suppress the intrinsic parameter fluctuation is crucial. Figure 1.7 reviews the threshold voltage (V_{th}) fluctuation versus technology node [15]. At 32-nm node, the thinner gate dielectric thickness could be achieved by the introduction of metal gate (for eliminating poly depletion) and high-κ (for thinner equivalent-oxide thickness but not increasing gate leakage) materials. Another opportunity is not scaling gate dielectric thickness but enhancing short channel control with SOI substrate. Special attention will be paid to thin-buried-oxide SOI [49]. At sub-22 nm node, planar SOI will no more be a good device option, because

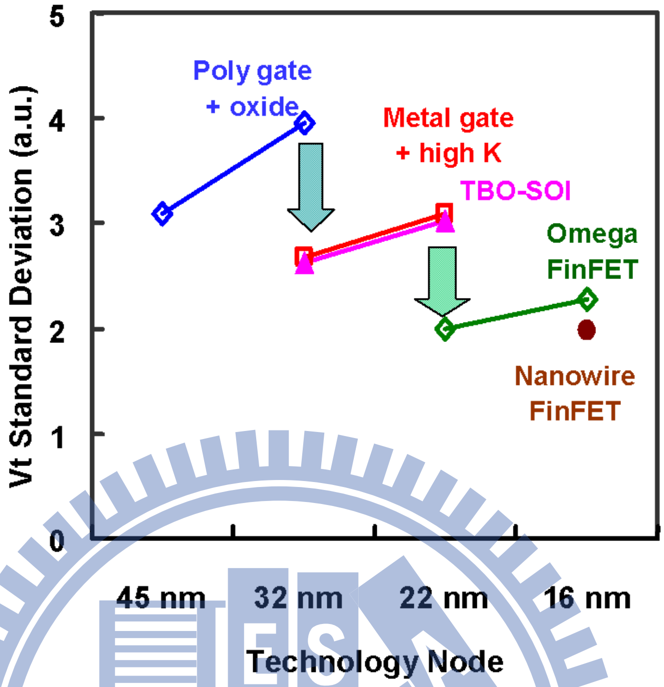


Figure 1.7: The threshold voltage fluctuation versus technology node.

very thin body (less than 10 nm) is necessary for SCE control but meanwhile the thin body will degrade drive current due to ”quantum confinement” [50]. Then non-planar transistors such as FinFETs may emerge instead [51-56]. Their V_{th} fluctuation characteristics should be addressed as well.

5. So far the most of aforementioned works are focused on the fluctuation of DC characteristics, the investigation of device’s AC as well as circuit’s fluctuations are lacked [84-91]. Though several works have addressed the importance of device variability in circuit, the simulation approach uses the compact model, which can not capture

the random-dopant-position induced fluctuation and may underestimate the influence of fluctuation.

To deal with the aforementioned problems, this work extensively study the FinFET variability and its fluctuation on circuits by a statistically-sound 3D ”atomistic” coupled device-circuit simulation approach [64-67,115-118]. The impact of individual fluctuation sources, consisting of gate length deviation, line edge roughness, random-dopant-fluctuation, and workfunction fluctuation, on the device's DC/AC and circuit's timing/power/high-frequency characteristic fluctuations are explored. The dominant fluctuation source in each characteristics are found. For the device characteristic fluctuations, the ”atomistic” simulation approach is effective to capture not only the randomness of doping concentration but also the random placement of dopants induced device variability. Moreover, a statistic simulation approach is applied to characterize the emerging workfunction fluctuation induced variability. The physical model of devices has been calibrated with experiential data [15-17,63]. To accurately describe the device variability in circuits, the circuit characteristics fluctuation are obtained by solving the both device transport and circuit nodal equations (so it's called coupled device-circuit simulation). Unlike the compact model simulation approach, the coupled device-circuit simulation approach solves the device transport characteristics in circuit simulation and therefore provide the most device physics inside circuit fluctuation. The extensive study assesses the fluctuations on circuit performance and reliability, which can in turn be used to optimize nanoscale MOSFET and circuits.

1.4 Outline

This dissertation is organized as follows. Chapter 2 shows the used device model and numerical methods. The quantum-mechanical corrected transport equations and numerical simulation methods are introduced, where a nanoscale FinFET is used as an example for simulation and calibration. Chapter 3 introduces the computer characterization technique for studying the effect of intrinsic parameter fluctuations including process-variation-effect (PVE), random dopant fluctuation (RDF), and workfunction fluctuation (WKF). The accuracy of characterization has been confirmed. Chapter 4 presents the random-dopant-induced characteristics fluctuation in vertical-channel transistors, where the impact of discrete dopant fluctuation on transistor physical and electrical characteristics are explored. This chapter also extensively explores the random-dopant-fluctuation in SOI transistors from single-gate to double-gate, triple-gate, and surrounding-gate transistor architectures. The effect of surrounding-gate coverage ratio on fluctuation resistivity is also discussed. Chapter 5 examines the impact of the intrinsic parameter fluctuations, PVE, RDF, WKF, in nanoscale FinFETs. The implications of device variability in circuits are explored in Chapter 6, in which the coupled device-circuit simulation approach is used instead of compact modeling approach for pursuing best accuracy. Finally, conclusions are drawn, suppression technique are prospected, and future work is suggested.

Chapter 2

Device Model and Numerical Methods

2.1 The Quantum-Mechanical Corrected Transport Equations

2.1.1 The Density-Gradient Equations

The technology computer-aided design (TCAD) simulations, such as process and device simulations, are widely used for the analysis of semiconductor devices. The process simulation can generate the device geometry and doping profile according to the parameters of the fabrication processes. The output of process simulation is then used in the device simulation to estimate device characteristics. The drift-diffusion (DD) and hydrodynamic

(HD) models play a crucial role in the development of semiconductor device simulator in the macroscopic point of view. The DD model was derived from Maxwell's equation as well as charges' conservation law and has been successfully applied to study device transport behavior, in the past decades. It assumes local isothermal conditions and is still widely employed in semiconductor device design.

Classical drift-diffusion model consists of at least three coupled partial differential equations (PDEs) for, such as electrostatic potential and electron-hole densities. When device channel is specified, a set of the DD equations in semiconductor device simulation is solved:

$$\triangle\phi = \frac{q}{\varepsilon_s}(n - p + D), \tag{2.1}$$

$$\frac{1}{q} \bigtriangledown \cdot J_n = R(n, p), \tag{2.2}$$

and

$$\frac{1}{q} \bigtriangledown \cdot J_p = -R(n, p), \tag{2.3}$$

where ϕ is the electrostatic potential and its unit is volt. n and p are classical electron and hole concentrations (cm^{-3}). q is the elementary charge and its unit is coulomb. The net doping concentration is $D(x, y, z) = N_D^+(x, y, z) - N_A^-(x, y, z)$. R is the net recombination rate ($cm^{-3}s^{-1}$). The carrier's currents densities are given by

$$J_n = -q\mu_n n \bigtriangledown \phi + qD_n \bigtriangledown n, \tag{2.4}$$

and

$$J_p = -q\mu_p p \bigtriangledown \phi - qD_p \bigtriangledown p, \tag{2.5}$$

where μ_n and μ_p are the carrier mobility ($cm^2/V - s$). The diffusion coefficients, D_n and D_p (cm^2/s), satisfy the Einstein relation.

The quantum mechanical effects should be considered in the device simulation when the dimensions of the devices shrunk into nanometer scale. Various theoretical approaches have been presented to study the quantum confinement effects, such as full quantum mechanical model (e.g. nonequilibrium Green's function) and quantum corrections to the classical drift-diffusion (DD) or hydrodynamic (HD) transport models. A set of Schrödinger-Poisson (SP) equations has been applied to study the quantum confinement effect in the inversion layers as well as the quantum transport between source and drain, but it is a time-consuming task in the TCAD application to realistic device characterization. Therefore, various quantum correction models, density gradient (DG) [99-103], Hänsch[104], modified local density approximation (MLDA)[105], effective potential (EP)[106-108], and unitfied quantum correction Model[109], have been proposed for classical DD or HD transport models. In this investigation, the density gradient was coupled with the DD model and solved for the quantum mechanical effects. The density gradient equation can be expressed as,

$$\vec{J}_n = -q\mu_n n \bigtriangledown \phi + qD_n \bigtriangledown n - qn\mu_n \bigtriangledown \gamma_n, \tag{2.6}$$

$$\vec{J}_p = -q\mu_p p \bigtriangledown \phi - qD_p \bigtriangledown p + qp\mu_p \bigtriangledown \gamma_p, \tag{2.7}$$

where γ_n and γ_p are the quantum potentials for electrons and holes. $\gamma_n = 2b_n\frac{\bigtriangledown^2\sqrt{n}}{\sqrt{n}}$. $\gamma_p = 2b_p\frac{\bigtriangledown^2\sqrt{p}}{\sqrt{p}}$ b_n and b_p are density-gradient coefficients for electrons and holes. $b_n = \hbar^2/(12qm_n^*)$ and $b_p = \hbar^2/(12qm_p^*)$. m_n^* and m_p^* are effective masses for the electrons and holes. $\hbar$ is the Planck constant. b_n and b_p in Eqs. (2.6) and (2.7) are the density gradient coefficient which determines the strength of the gradient effect in the electron and hole gas. The last term in the right hand side of Eqs. (2.6) and (2.7) are referred to as "quantum diffusion", which makes the electron continuity equation has a fourth-order partial differential equation. Therefore, such an approach is highly sensitive to noise in the local carrier density, and the methodology is highly important in cases of strong quantization. To calculate the numerical solution of the multidimensional density-gradient model, firstly we decouple the coupled partial differential equations (PDEs); approximated with the finite volume method over nonuniform mesh. The corresponding system of the nonlinear algebraic equations is then solved with the monotone iteration methods. Iteration will be terminated and post-processes will be performed when the specified stopping criteria for inner and outer iteration loops are satisfied, respectively.

2.1.2 The Mobility Model

According to Mathiessen's rule [113,114], the mobility model used in the device simulation can be expressed as:

$$\frac{1}{\mu} = \frac{D}{\mu_{surf\_aps}} + \frac{D}{\mu_{surf\_rs}} + \frac{1}{\mu_{bulk}}, \tag{2.8}$$

where $D = \exp\left(x/l_{crit}\right)$, x is the distance from the interface and l_{crit} is a fitting parameter. The mobility consists of three parts: (1) the surface contribution due to acoustic phonon scattering, where N_i = N_A + N_D, T_0 = 300 K, $\mathbf{E}$ is the transverse electric field normal to the interface of semiconductor and insulator, B and C are parameters which based on physically derived quantities, N_0 and τ are fitting parameters, T is lattice temperature, and K is the temperature dependence of the probability of surface phonon scattering; (2) the contribution attributed to surface roughness scattering is $\mu_{surf\_aps} = \frac{B}{\mathbf{E}} + \frac{C(N_i/N_0)^{\tau}}{\mathbf{E}^{1/3}(T/T_0)^{K}}$, where $\Xi = A + \frac{\alpha\cdot(n+p)N_{ref}^{v}}{(N_i+N_1)^{v}}$, E_{ref} = 1 V/cm is a reference electric field to ensure a unitless numerator in μ_{surf_rs}, N_{ref} = 1 cm^{-3} is a reference doping concentration to cancel the unit of the term raised to the power v in the denominator of Ξ, δ is a constant that depends on the details of the technology, such as oxide growth conditions, N_1 = 1 cm^{-3}, A, α, and η are fitting parameters; (3) and the bulk mobility is $\mu_{bulk} = \mu_L(\frac{T}{T_0})^{-\xi}$, where μ_L is the mobility due to bulk phonon scattering and ξ is a fitting parameter.

2.2 The Numerical Simulation Methods

In this section, we will introduce the adaptive numerical methods in the following discussion. The implemented adaptive computing technique for semiconductor device simulation is mainly based on Gummel's decoupling method [114, 124, 125], FV approximation [112, 126], Monotone iterative method [135, 136], a posteriori error estimation [112], and an unstructure meshing scheme [111, 114, 124, 125]. This simulation methodology has recently been developed for different device simulation [112, 126, 127]. The Gummel's decoupling method controls an iterative loop over two or more coupled equations. It is used when a fully coupled method would use too many resources of a given machine, or when the problem is not yet solved and a full coupling of the equations would diverge.

2.2.1 The Gummel Decoupling Method

To explore the transport behavior of transistors, the five coupled PDEs are numerically solved with Gummel's decoupling method. With a given initial guess $(\phi^{(0)}, n^{(0)}, p^{(0)}, {\gamma_n}^{(0)}, {\gamma_p}^{(0)})$ and for each Gummel's iteration index g, $g = 0, 1, \ldots$, we first solve the nonlinear Poisson equation as well as density-gradient-corrected quantum potential equations.

$$\Delta\phi^{(g+1)} = \frac{q}{\varepsilon_s}(n^{(g)} - p^{(g)} + D(x,y) + BT(\phi^{(g+1)})). \tag{2.9}$$

$${\gamma_n}^{(g+1)} = 2b_n \frac{\nabla^2\sqrt{n^{(g)}}}{\sqrt{n^{(g)}}}. \tag{2.10}$$

$$ {\gamma_p}^{(g+1)} = 2b_p \frac{\bigtriangledown^2 \sqrt{p^{(g)}}}{\sqrt{p^{(g)}}}. \tag{2.11} $$

The nonlinear Poisson equation is solved for $\phi^{(g+1)}$, ${\gamma_n}^{(g+1)}$, and ${\gamma_p}^{(g+1)}$ given the previous states $n^{(g)}$ and $p^{(g)}$. The quantum-corrected current continuity equation of electron is then solved for $n^{(g+1)}$ with now the known functions $\phi^{(g+1)}$, $p^{(g)}$, ${\gamma_n}^{(g+1)}$, and ${\gamma_p}^{(g+1)}$.

$$ \frac{1}{q}\nabla \cdot (-q\mu_n n^{(g+1)} \nabla \phi^{(g+1)} + qD_n^{(g+1)} \nabla n^{(g+1)} - qn^{(g+1)} \mu_n \bigtriangledown {\gamma_n}^{(g+1)}) = R(n^{(g+1)}, p^{(g)}). \tag{2.12} $$

Finally, we solve the quantum-corrected current continuity equation of hole with known $\phi^{(g+1)}$, $n^{(g+1)}$, ${\gamma_n}^{(g+1)}$, and ${\gamma_p}^{(g+1)}$

$$ \frac{1}{q}\nabla \cdot (-q\mu_p p^{(g+1)} \nabla \phi^{(g+1)} - qD_p^{(g+1)} \nabla p^{(g+1)} + qp^{(g+1)} \mu_p \bigtriangledown {\gamma_p}^{(g+1)}) = -R(n^{(g+1)}, p^{(g+1)}) \tag{2.13} $$

for $p^{(g+1)}$ until all preset stopping criteria are satisfied. Equations (2.9), (2.12), and (2.13) are associated with proper boundary condition, respectively. We note that Eqs. (2.9), (2.12), and (2.13) are now three individual semilinear PDEs to be solved for each Gummel's iteration. An outer iteration in the procedure of device simulation is then defined by Gummel's decoupling method. We note that analysis of Gummel's decoupling method in device simulation have been reported [110, 112, 114, 124–128, 130]. Then we can solve each decoupled PDEs with adaptive computing technique.

```
The Gummel's decoupling method
Begin
    While $\phi$, $n$, and $p$ in outer loop (Gummel's loop) are not convergent
        If $\phi$ is convergent
            Solve the nonlinear Poisson equation as well as density-gradient-corrected quantum potential by adaptive computing technique.
        End If
        If $n$ is convergent
            Solve the quantum-corrected current continuity equation of electron with adaptive computing technique.
        End If
        If $p$ is convergent
            Solve the quantum-corrected current continuity equation of hole with adaptive computing technique.
        End If
    End While
    Call for next calculation.
End The Gummel's decoupling algorithm
```

2.2.2 The Adaptive Finite Volume Method

The discretization of semiconductor is performed based on adaptive 1-irregular mesh, triangular mesh, and finite volume (FV) approximation. The finite volume method is a numerical method for solving PDEs. It calculates the values of the conserved variables across the volume. Before using adaptive finite volume method to solve Poisson equation, we must understand the follow steps:

(1) Weak Formulation transforms into weak problem;

(2) Discretize the simulation area by one-irregular mesh;

(3) Form equation **"Ax=B"** by using FV method; and

(4) Error estimation and mesh refinement.

The discretized step divides into structured mesh and unstructured mesh. If according to geometry, it divides into rectangle mesh and triangle mesh. But the rectangle mesh is easier to build than the triangle mesh. The one-irregular method is shown in Fig. 2.1. Figures 2.2(a) and 2.2(b) are the discretization scheme by finite volume method and finite element method, respectively. The initial mesh contains 25 nodes and then refined based on the estimation of solution error element by element. Notably, the process of mesh refinement is guided by the result of error estimation automatically. As shown in plots, at the refinest level most of refined meshes are intensively located near the surface of channel and the junction of the drain side due to large variation of the solution gradient.

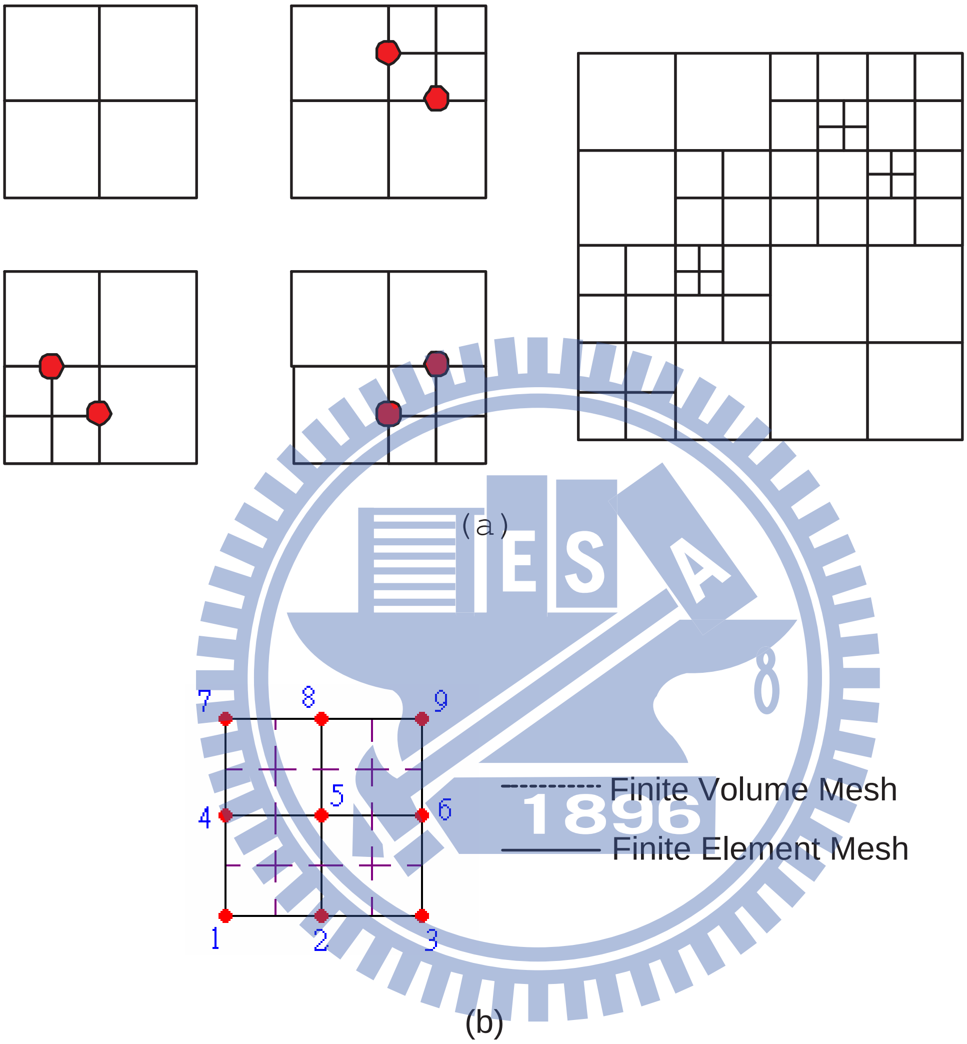


Figure 2.1: The plot of FV method. (a) One-Irregular mesh, and (b) the difference between finite element mesh and finite volume mesh.

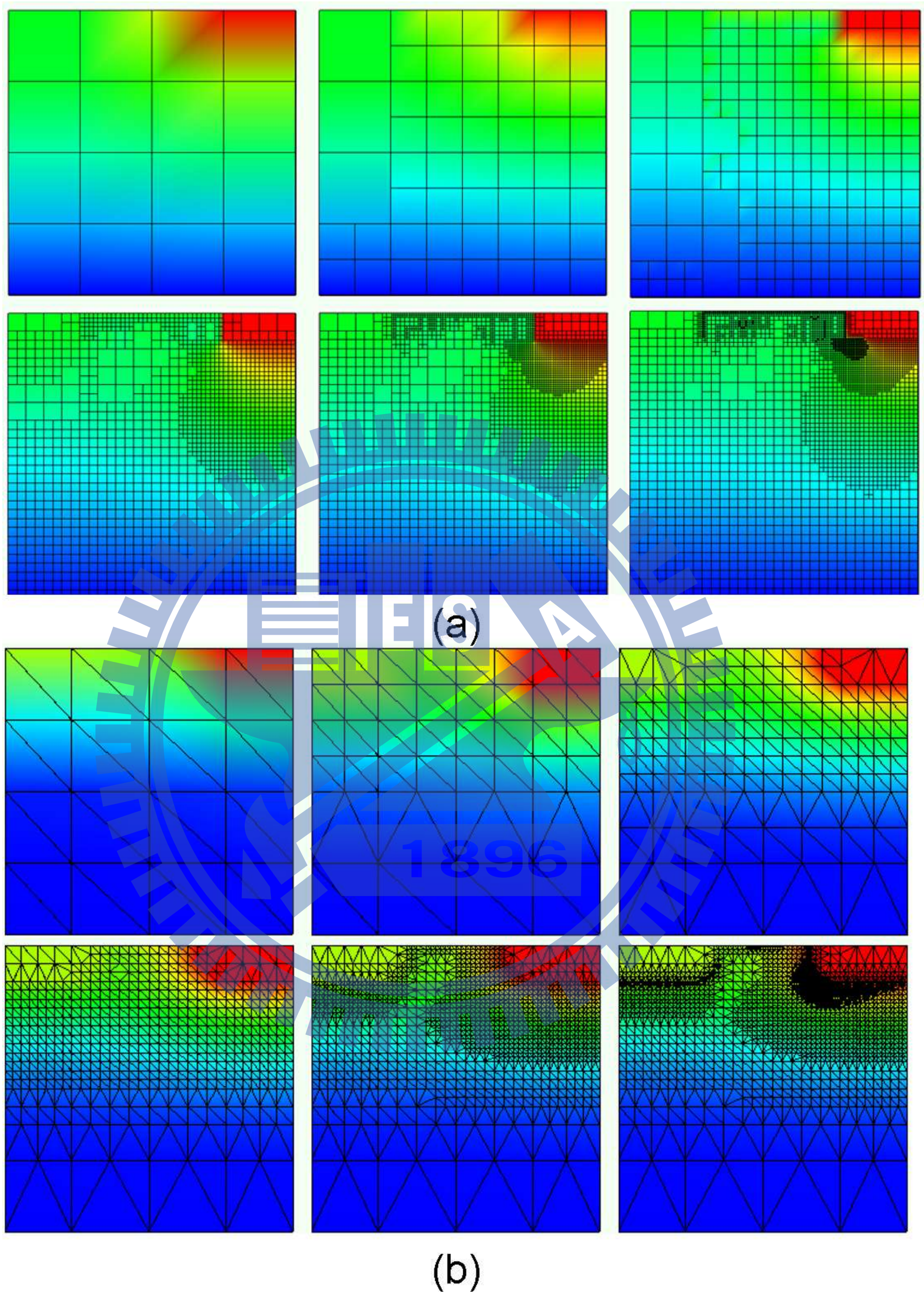


Figure 2.2: The mesh used for the solution process. Illustrations of MOSFET source/drain junction discretization. The p/n junction is discretized by (a) adaptive finite volume method and (b) adaptive finite element method.

2.2.3 The Monotone Iterative Method

In previous subsection, we apply a finite volume method with nonuniform mesh technique to discretize the above PDEs in each directions. Using the divergence theorem on a finite hexahedral volume and considering the tensor-product meshes for the hexahedral volume, the discretized Poisson equation can be written as

$$\begin{aligned}\xi_{i+1,j,k}\phi_{i+1,j,k} + \xi_{i-1,j,k}\phi_{i-1,j,k} + \xi_{i,j+1,k}\phi_{i,j+1,k} + \xi_{i,j-1,k}\phi_{i,j-1,k} \\ +\xi_{i,j,k+1}\phi_{i,j,k+1} + \xi_{i,j,k-1}\phi_{i,j,k-1} + +\xi_{i,j,k}\phi_{i,j,k} \\ = \tau_{i,j,k}\left[\frac{qn_i}{\varepsilon_{si}}\left(\exp\left(\frac{\phi_{i,j,k}}{V_T}\right) - \exp\left(-\frac{\phi_{i,j,k}}{V_T}\right)\right) - \frac{q\left(N_D^+ - N_A^-\right)_{i,j,k}}{\varepsilon_{si}}\right],\end{aligned} \tag{2.14}$$

where the arranged coefficients $\xi_{i,j,k}$ and $\tau_{i,j,k}$ for all i, j, and k are direct results from the integral approximations with the quadrature rule. After employing the boundary conditions, the above set of equations for the approximations $\phi_{i,j,k}$ at the nodes $\mathbf{X}_{i,j,k} = (x_i, y_j, z_k)$ can be written together as the compact matrix form,

$$\mathbf{A}\Phi = -\mathbf{B}\left(\mathbf{\Phi}\right). \tag{2.15}$$

$\mathbf{\Phi}$ is the unknown vector formed by $\phi_{i,j,k}$ in the natural ordering, $\mathbf{B}$ is the vector of nonlinear functions corresponding to the finite volume discretization of equations. The matrix $\mathbf{A}$ is a seven-banded block-tridiagonal form. We note all coefficients in Eq. (2.14) are nonnegative and the following relation:

$$\xi_{i,j,k} \geq \xi_{i+1,j,k} + \xi_{i-1,j,k} + \xi_{i,j+1,k} + \xi_{i,j-1,k} + \xi_{i,j,k+1} + \xi_{i,j,k-1}$$

which holds for all $\mathbf{X}_{i,j,k}$. Based on these observations, it can be shown $\mathbf{A}$ is an irreducible M-matrix. The right-hand side of Eq. (2.14) is continuously differentiable function with respect to ϕ, and the derivative of this nonlinear function is nonnegative. Then we can write $\mathbf{A} = \mathbf{D} - \mathbf{L} - \mathbf{U}$ and proceed to the description of the iterative method for solving the Eq. (2.15) arising from the finite volume discretization of semiconductor nonlinear Poisson equation. $\mathbf{D}$, $\mathbf{L}$, and $\mathbf{U}$ are diagonal, lower triangular, and upper triangular matrices of $\mathbf{A}$, respectively. This method for solving the multi-dimensional semiconductor nonlinear Poisson equation consists of only single iteration loop as follows:

$$(\mathbf{D}+\lambda\mathbf{I})\,\boldsymbol{\Theta}^{(\mathrm{m+1})} = (\mathbf{L}+\mathbf{U})\,\boldsymbol{\Theta}^{(\mathrm{m})} - \mathbf{B}\boldsymbol{\Theta}^{(\mathrm{m})} + \lambda\mathbf{I}\boldsymbol{\Theta}^{(\mathrm{m})}, \tag{2.16}$$

where the superscript index m is the iteration index; $\mathbf{I}$ is an identity matrix and $\lambda\mathbf{I}$ is a diagonal matrix determined by the function $\mathbf{B}$. The Eq. (2.16) can be regarded as a Jacobi type iterative scheme. This result demonstrates the solution sequence generating from iterative formula, Eq. (2.16), will converge monotonically to the solution of Eq. (2.15) for all choices of the initial guess. The proof has been validated in reference [135, 136]. Together with a Gummel's decoupling method, the monotone iterative method for the numerical solution of the nonlinear Poisson equation can be applied to solve various semiconductor device models. Compared with the Newton's iterative method, the monotone iterative method is easy implementing, relatively robust and fast with much less computation time, and its algorithm is inherently parallel in large-scale computing. The algorithm of the monotone iterative method is summarized as follows:

(1) Take an initial guess for $\mathbf{\Theta}^{(\mathrm{m})}$;

(2) Let m = 1 and set (i,j,k)=(1,1,1);

(3) Determine the parameter of monotone iterative approach $\lambda\mathbf{I}$ instantaneously;

(4) Compute the $\mathbf{\Theta}^{(\mathrm{m}+1)}$ with Eq. (2.16), and

(5) Perform convergence test. If it converges, then break, else $m = m + 1$ and return to (3).

2.3 A 25-nm FinFET Simulation and Calibration

In this section, electrical characteristics of 25-nm-gate round-top-gate fin-typed field effect transistors (FinFETs) on silicon wafers are calibrated and explored. Furthermore, by considering different short-channel effects, dependence of the device performance on the non-ideal fin angle and fin height is investigated. Optimal structure configuration for the round-top-gate bulk FinFETs is thus drawn to show the strategy of fabrication in sub-25 nm metal oxide semiconductor field effect transistors devices. The physical models have been calibrated with experimentally measured data.

Field effect transistors with multiple-gate structures, such as fin-type FETs (FinFETs) have been of great interest due to the excellent controlling ability of carriers in the device's channel, which suppressed the short-channel effect. Channel doping for adjusting

Unit (nm)	
Fin Height (H_{fin})	37.5
Fin Width (W_{fin})	25
Gate Length (L_g)	25
Spacer	25
Oxide Thickness	1.6

Midgap Gate
WorkFunction=4.71eV

Doping	Unit(cm^{-3})
S/D	1×10^{20}
Well	1×10^{19}
Channel	1×10^{16}

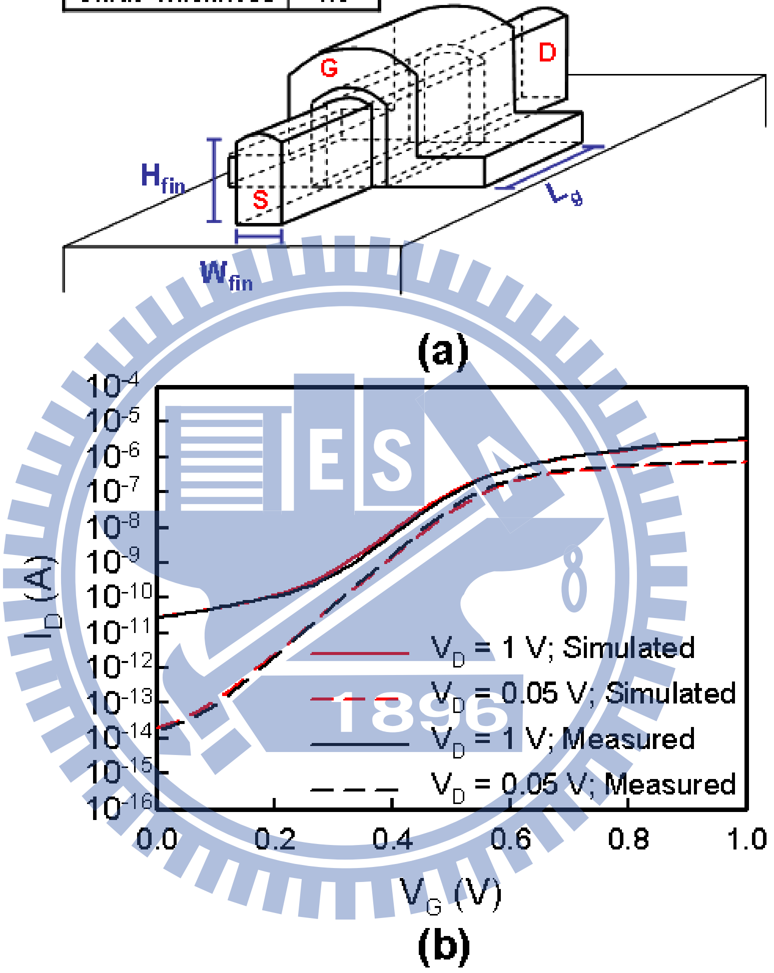


Figure 2.3: (a) An illustration of the simulated fin-type field effect transistors. The top of the fin is formed to a round shape naturally and the fin bottom is not actually rectangular for the lithography and silicon etching processes. (b) The I_D-V_G curves for the FinFETs. The red and black lines are the simulated and measured data, respectively.

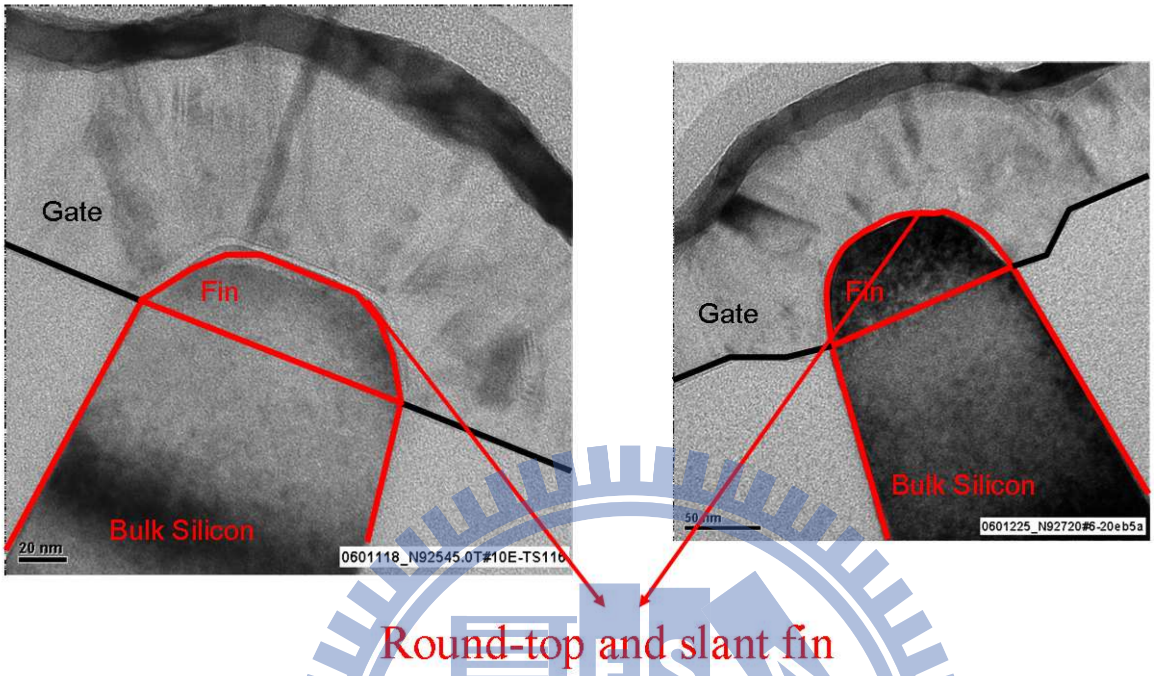
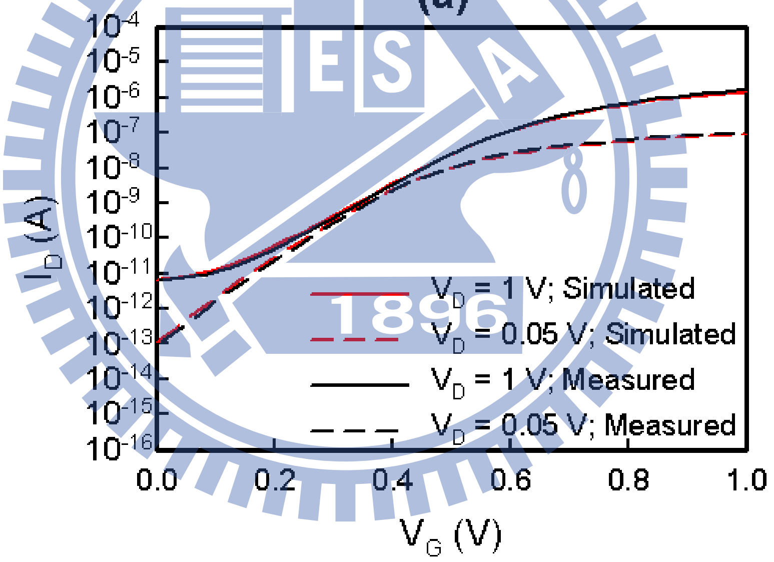


Figure 2.4: SEM pictures of bulk FinFETs with a round-top and slant fin.

the threshold voltage is still necessary in nowadays manufacturing process. Various studies have been reported to simulate the multiple-gate device by using 3D quantum/classical models, and device models coupled with process models. We herein use the 3D quantum-corrected drift-diffusion models to simulated the characteristics of bulk FinFETs. The employed device models have been calibrated. Figure 2.3(a) shows the geometry and parameters of the simulated FinFET with 4.71 eV workfunction, 37.5 nm fin height (H_{fin}), 25 nm fin width (W_{fin}), 25 nm gate length (L_g) and 1.6 nm oxide thickness. The device is with a round-shape top due to the limit of manufacturing ability. In fabricating the nanoscale

N+ Metal Gate WorkFunction=4.28 eV	Unit (nm)
Fin Height (H_{fin})	37.5
Fin Width (W_{fin})	25
Gate Length (L_g)	25
Spacer	25
Oxide Thickness	1.6
Oxide Thickness	1.6
S/D	$1x10^{20}$
Well	$1x10^{19}$
Channel	$6x10^{18}$

(a)



(b)

Figure 2.5: (a) The device dimension and parameter setting of the simulated fin-type field effect transistors, in which the device workfunction is 4.28 eV. (b) The characteristics of the I_D-V_G curves for the FinFETs. The red and black lines are the simulated and measured data, respectively. The simulation shows a good agreement with measurement data, which represents the accuracy of the calibrated 3D device simulation.

FinFETs, the minimum dimension of the device has transferred from the gate length to the fin thickness. Top of the fin is formed to a round shape naturally and the fin bottom is not actually rectangular for the lithography and silicon etching processes, as shown in Fig. 2.4. These non-ideal processes will result in a wider fin bottom with respect to the fin top; thus it leads to a slanted edge of the channel fin [51-56]. Such geometric derivation degrades device performance and raises serious SCEs, such as a large subthreshold swing, low ratio of the on- and off-state currents, and large drain induced barrier lowering. The measurement and simulated results are presented in Fig. 2.3(b), where the red and black lines are the simulated and measured data, respectively. The simulation shows a good agreement with measurement data. Similarly, we change the device workfunction and parameters as shown in Fig. 2.5(a). The simulated data in Fig. 2.5(b) also exhibit a good accuracy with measurement data, which represents the accuracy of the calibrated 3D device simulation. The properties of the material are summarized in Tab. 2.1.

Then we change the device geometry setting to explore the electrical characteristics of 25-nm-gate round-top-gate FinFETs on silicon wafers, as shown in Fig. 2.6. The oxide thickness, the fin width, and the fin height are fixed at 1.2 nm, 20 nm and 50 nm, respectively. Figures 2.7(a) shows a 3D doping profile and the corresponding refined mesh of the device, where the color of the mesh indicates the assigned doping concentration at meshing lines. The fin height = 50 nm and the fin angle = 70°. Plots of the 3D simulated on-

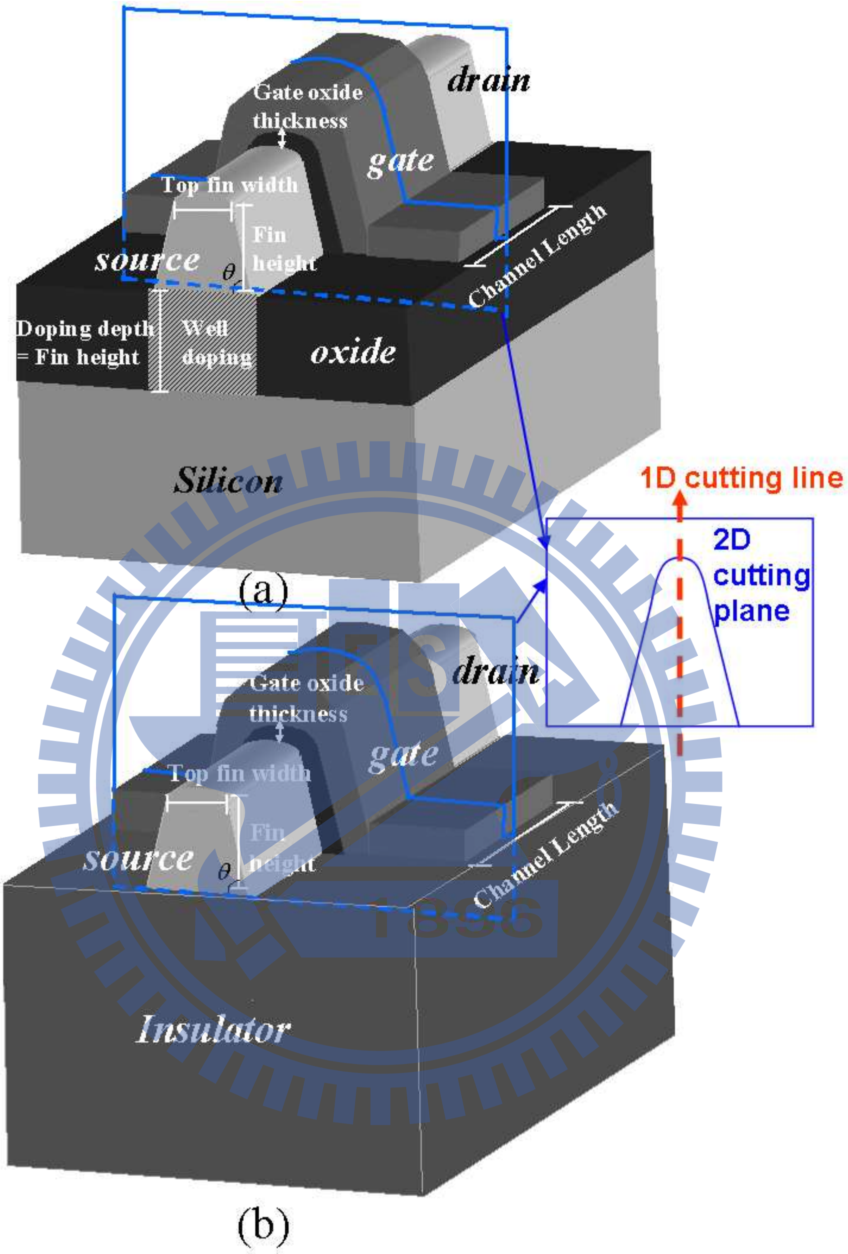
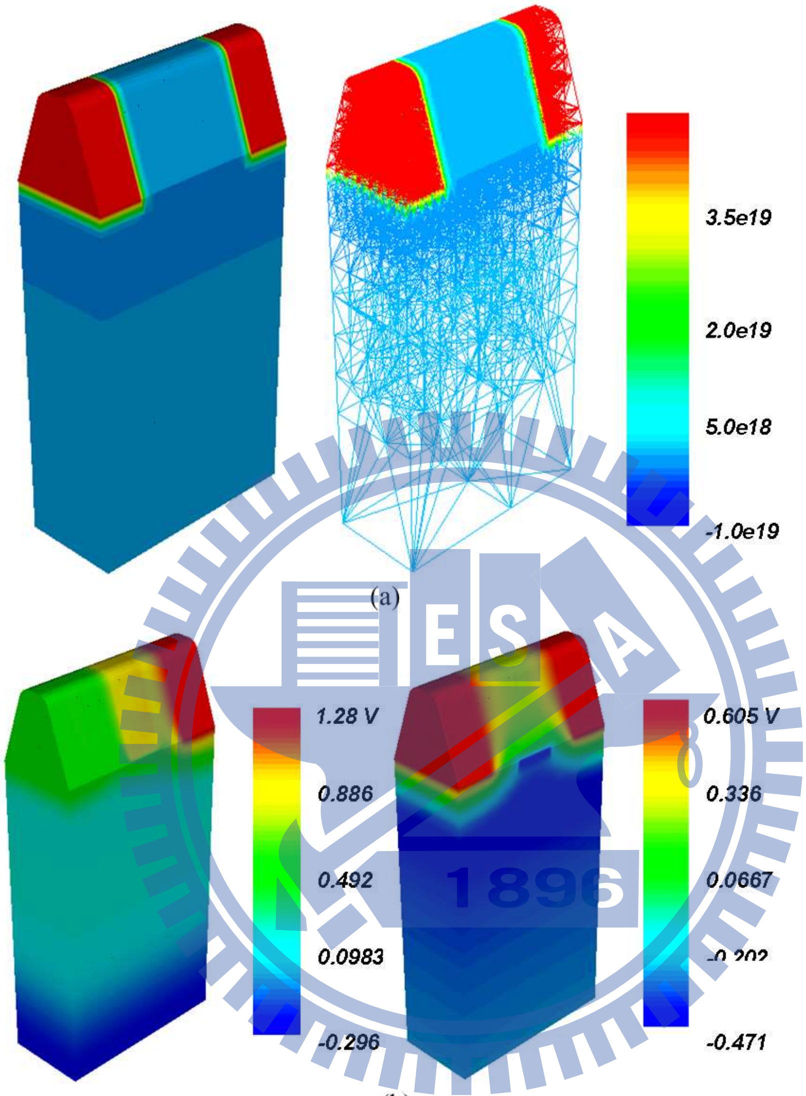


Figure 2.6: Three-dimensional schematic plots for the (a) bulk FinFETs and (b) SOI FinFETs. Θ is the fin angle and the inset shows a 2D cutting-plane extracting from the center of channel.



(a)

(b)

Figure 2.7: (a) A plot of the 3D doping profile of the round-top-gate bulk FinFET. The left plot is the contour of doping profile and the right one is the corresponding mesh. (b) The left plot is the on-state potential of the round-top bulk FinFET and the right one is the off-state potential.

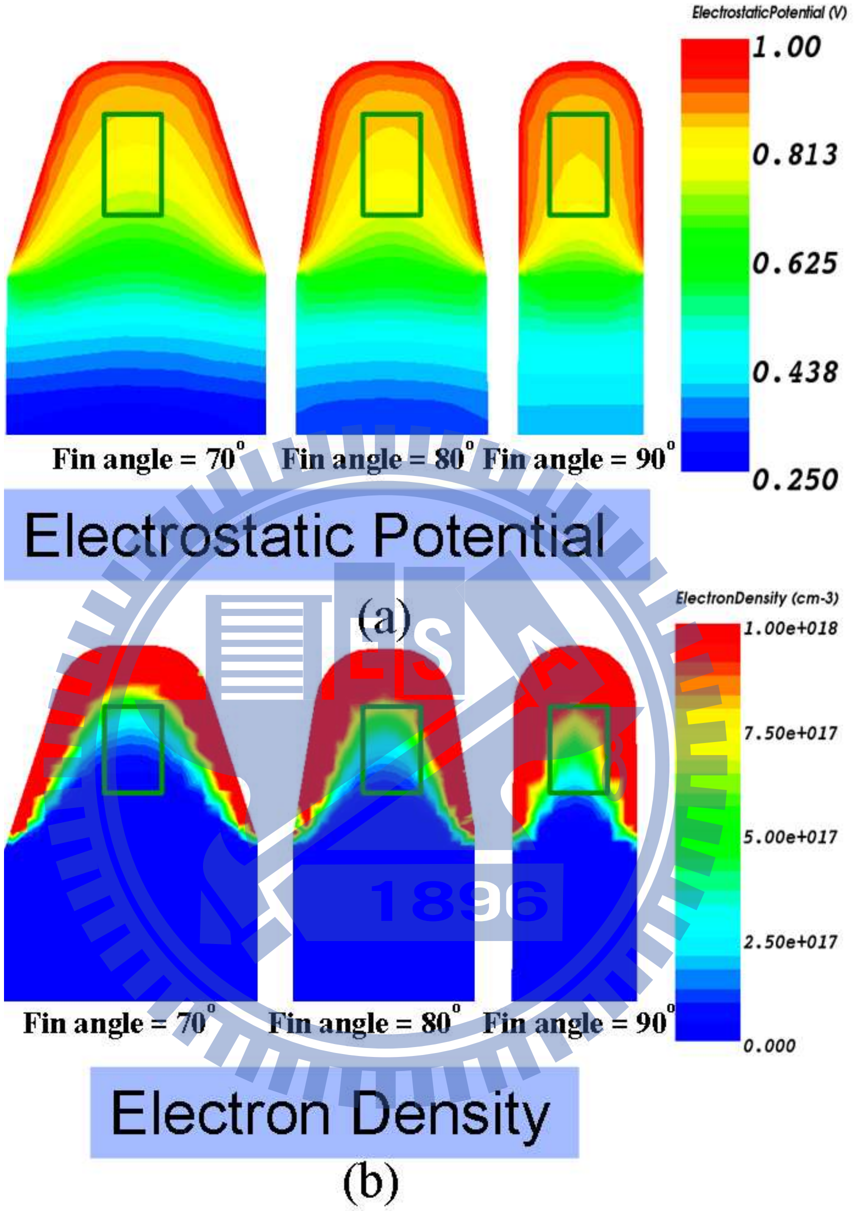
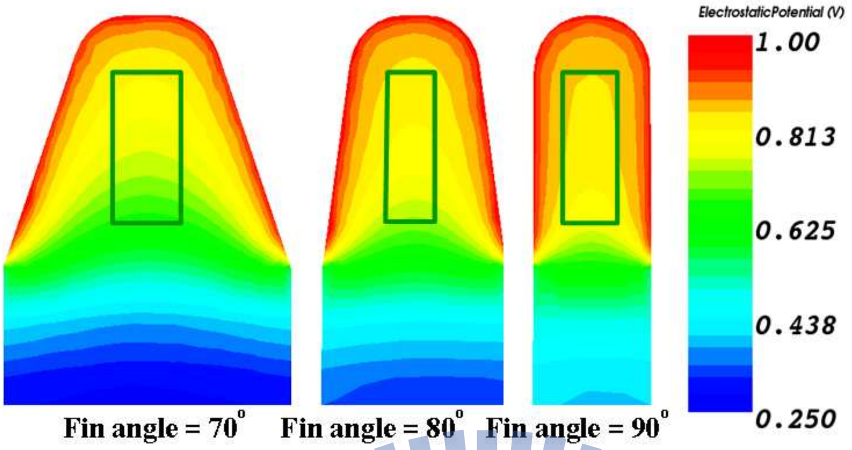
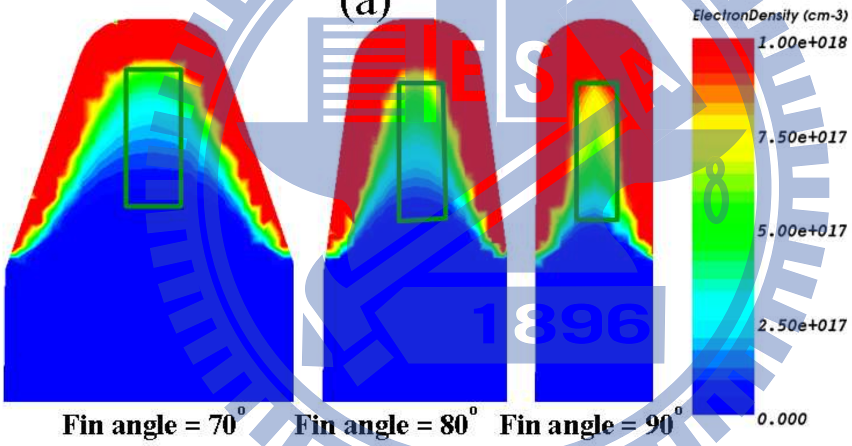


Figure 2.8: Plots of the 2D cutting plane of the simulated on-state (V_D = 1.0 V and V_G = 1.0 V) (a) potential and (b) electron density at the center of channel of the 30 nm-height bulk FinFET. The fin angles are the 90°, 80° , and 70°, respectively.



Electrostatic Potential

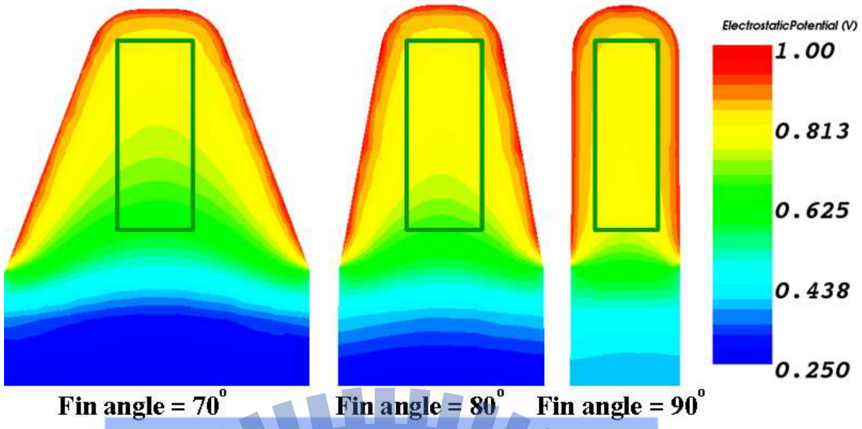
(a)



Electron Density

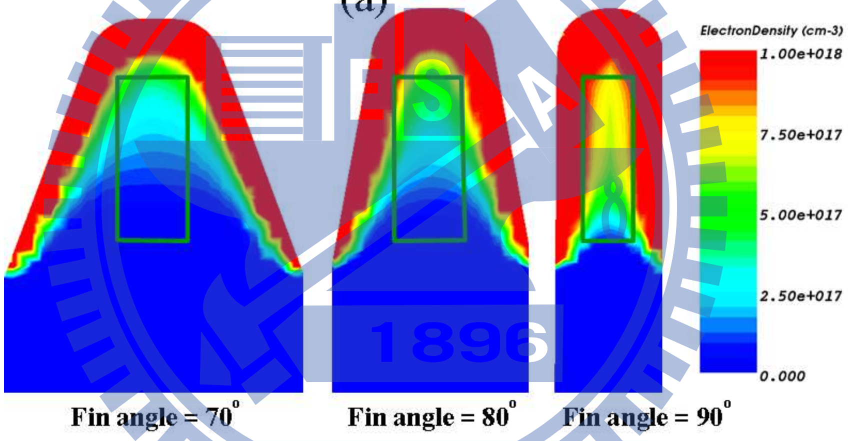
(b)

Figure 2.9: Plots of the 2D cutting plane of the on-state (a) potential and (b) electron density at the center of channel of the 40 nm-height bulk FinFET. The fin angles are the 90°, 80° , and 70°, respectively.



Electrostatic Potential

(a)



Electron Density

(b)

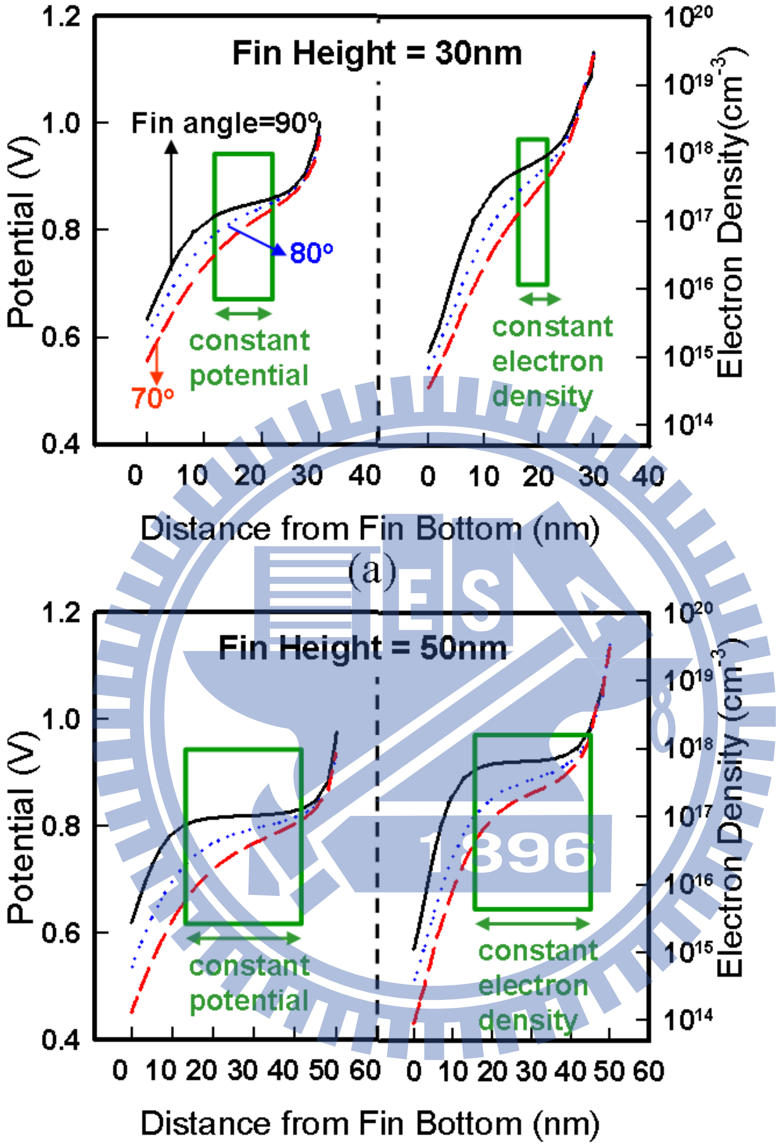
Figure 2.10: Plots of the 2D cutting plane of the on-state ((a) potential and (b) electron density at the center of channel of the 50 nm-height bulk FinFET. The fin angles are the 90°, 80° , and 70°, respectively.

Table 2.1: Material parameters setting for silicon, poly-silicon, SiO_2 and Si_3N_4. The epsilon is the ratio of the permittivities of material and vacuum.

Model	Silicon	Poly-Si	SiO_2	Si_3N_4
Epsilon	11.7	11.7	3.9	7.5
Heat Capacity (J/(kg-K))	705	705	733	710.6
Bandgap (eV)	1.17	1.17	9	4.7
Thermal conductivity (W/(K-cm))	$1/(0.03+1.56e\text{-}3*T+1.65e\text{-}6*T^2)$	1.5	0.014	0.185
Constant Mobility ($cm^2/(V\text{-}s)$)	electron: $200*(T/300)^{-2.5}$ hole: $70*(T/300)^{-2.2}$			

(the drain voltage V_D = 1.0 V and V_G = 1.0 V) and off-state (V_D = 0.05 V and V_G = 1.0 V) electrostatic potentials are shown in Fig. 2.7(b) for reference. For $V_D = V_G$ = 1.0 V, contour plots of the potential and electron density (the 2D cutting planes along the center of channel) are shown in Figs. 2.8(a) and 2.8(b). The plots are device with three different angles of fin-taper: 70°, 80°, and 90° (from the left plot to the right one). Nonuniform distributions of the potential and current density along the longitudinal direction are observed. This a direct result of donor's and bias' impacts on the channel along the direction of the fin top to bottom. The potential attains the minimum value at the fin bottom, which increases rapidly toward the fin top. For the same distance, the larger potential associated with the larger fin taper angle is perceived from the fin bottom. The current density is reduced when the distance (from the top fin) is broadened; similarly, it has the minimum value at the fin bottom. For the device with the fin height = 30 nm, we find that the case of 90^o, shown in Fig. 2.8, exhibits the most uniform distribution of the potential in the center of channel. The potential decreases more quick with a more slanted fin angle, which leads to a stronger longitudinal electric field and may degrade the device performance. Similar results can be observed for the cases of fin height = 40 nm and 50 nm, as shown in Figs. 2.9 and 2.10.

For V_D = V_G = 1.0 V, the distributions of potential and electron density for device with the fin height = 30 nm (see Fig. 2.11(a)) and 50 nm (see Fig. 2.11(b)) are extracted according to the 1D cutting line, as shown in the inset of Fig. 2.4(b). The plots are device with three different angles of fin-taper: 70^o, 80^o, and 90^o. Non-uniform distributions of the potential and electron density along the longitudinal direction are observed. This is a direct result of donor's and bias' impacts on the channel along the direction of the fin top to bottom. The potential attains the minimum value at the fin bottom, which increases rapidly toward the fin top. For the same distance, the larger potential associated with the larger fin taper angle is perceived from the fin bottom. The electron density is reduced when the distance (from the top fin) is broadened; similarly, it has the minimum value at the fin bottom. For the device with the fin height = 30 nm, shown in the left plot of Fig. 2.11(a), the case of 90^o (i.e., the solid lines) exhibits the most uniform distribution of the potential in the center of channel. The potential decreases more quick with a more slanted fin angle, which leads to a stronger longitudinal electric field and may degrade the device performance.



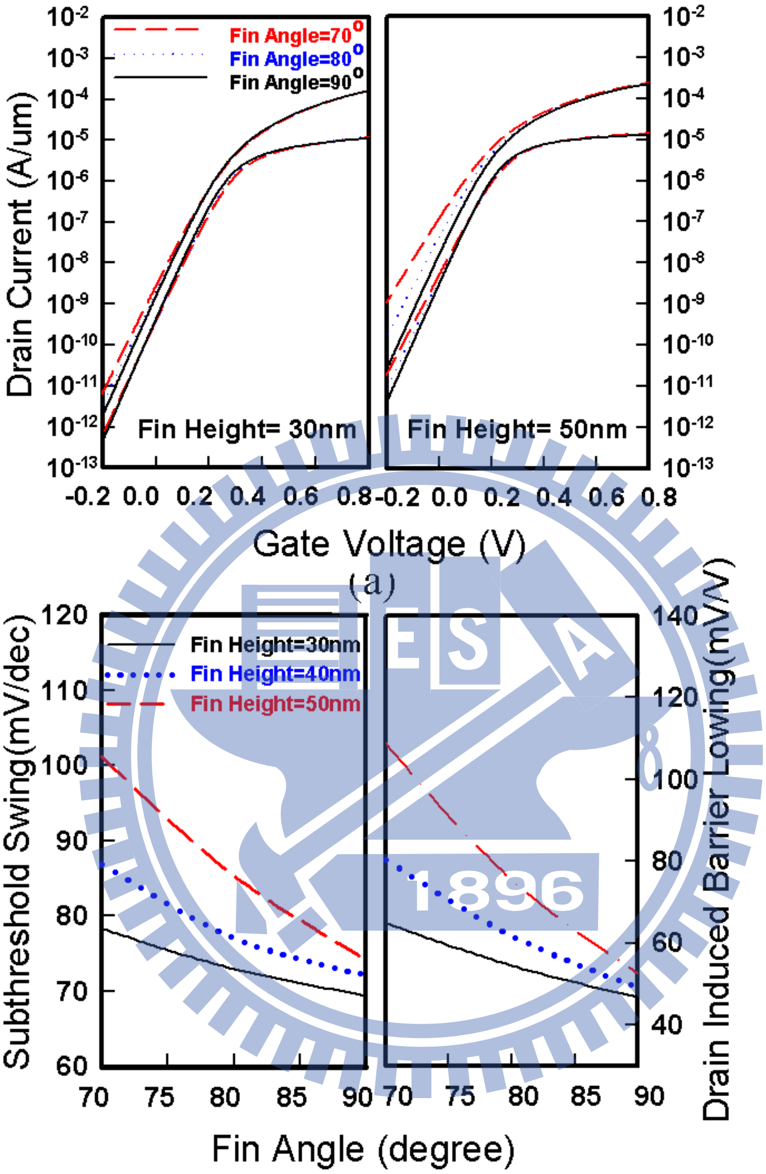
(a)

(b)

Figure 2.11: Plots of 1D cutting lines of the potential and electron density at the center of channel. The device is with the fin height of (a) 30 nm, and (b) 50 nm, where the solid line is the result of 90°, the dotted line is for the 80°, and the dashed line is for the 70°. The circled windows indicate the regimes where nearly constant potential and electron density are occurred in device channel.

Similar results can be observed for the cases of fin height 50 nm. Moreover, it is found that the variation of potential almost keeps constant within the longest distance inside the channel region. The potential variation is significant when the fin angle is decreased, and the case of 70^o (the dashed lines) possesses the largest potential variation among three angles. The variation is even more appreciable when the fin height is increased. For the different fin angles and fin heights, the right plots of Figs. 2.11(a) and 2.11(b) disclose the variation of the electron density versus the distance from the fin bottom. The variation of this physical quantity predicts the same trend as depicted above. It is found that the device with an approximately ideal fin angle (i.e, the fin angle approaches to 90^o) behaves the most uniform distribution of the examined physical quantities within the device channel.

Plots of the drain current versus the gate voltage for the three fin angles and two fin heights are shown in Fig. 2.12(a). The case for the fin height of 30 nm, as shown in the left plot of Fig. 2.12(a), allows a larger variation of the fin angle, compared with the result of the fin height = 50 nm. It means that the fin height of 30 nm maintains a highest ratio of the on- and off-state currents and implies better performance. The parameters of short-channel effect versus the fin angle are calculated accordingly, as shown in Fig. 2.12(b). A larger taper angle is necessary for fabrication of nanoscale bulk FinFETs to obtain robust electrical characteristics. Besides, Fig. 2.12(b) implies that a smaller fin height is essential for the device of 25 nm gate length. The calculated SS suggests that an increase of the fin



(a)

(b)

Figure 2.12: (a) The I_D-V_G curves for the device for different fin angles and heights. The solid lines are the result of 90°, the dotted lines are for the 80°, and the dashed lines are for the 70°. (b) Results of SS (the left plot) and DIBL (the right one) versus the fin angle, where the solid lines are the result of 30 nm, the dotted lines are for the 40 nm, and the dashed lines are for the 50 nm.

angle will result in better subthreshold swing; in particular, for those silicon fins with higher fin height, which improve the short-channel effect remarkably. Similarly, we also find the evidence for the drain induced barrier lowering. Consequently, for the cases with a small fin angle, the device may not have an acceptable performance. In addition, for the bulk FinFET with a high fin height, the situation is getting worse simultaneously. The fin height and the fin angle are the two critical limiting factors when the dimension of the bulk FinFET is continuously scaled down. The critical angles for the case of SS $<$ 75 mV/dec and DIBL $<$ 75 mV/V are then estimated. It' found that the critical angles when fin height / top fin width = 1.5, 2 and 2.5, and the critical angles are 71.9^o, 79.3^o, and 87.4^o, respectively. For device with a large ratio between the fin height and the top fin width, the controllability of manufacturing the fin taper angle is exceptionally important and much more efforts on processing should be made. A nearly rectangular shaped fin is only crucial for the device with a higher fin height. The following discussion of characteristics of FinFETs is based on an assumption that FinFET has a fin aspect ratio equal to one.

2.4 Summary

Nanoscale bulk FinFETs demonstrate potential application for sub-32 nm CMOS devices era, such as SRAM fabrication. This chapter described the quantum-mechanical corrected transport equations and numerical methods in device simulation, in which the density gradient was coupled with the drift-diffusion model for including the quantum mechanical effects. The coupled partial differential equations were approximated with the finite volume method over nonuniform mesh and then solved with the monotone iteration methods. The mobility model including bulk mobility, acoustic phonon scattering, and surface roughness scattering effects were calibrated and used for device simulation. Electrical characteristics of 25-nm-gate round-top-gate fin-typed field effect transistors (FinFETs) on silicon wafers are then calibrated with experimentally measured data and explored. Result shows that the importance of fin height and the fin angle in FinFETs scaling. To have a transistor with SS $<$ 75 mV/dec and DIBL $<$ 75 mV/V, the critical angles for fin height / top fin width = 1.5, 2 and 2.5 are 71.9^{o}, 79.3^{o}, and 87.4^{o}, respectively. Examinations into the effects of the top fin width and wider variation of ratio (e.g., ratio $<$ 1) on electrical characteristics will benefit the device design. Characteristic fluctuation of bulk FinFETs should also be controlled for high performance design. The intrinsic parameter induced characteristics fluctuation for the nanoscale FinFETs are presented in following chapters.

Chapter 3

Simulation of Intrinsic Parameter Fluctuation

This chapter presents the characterization technique for intrinsic parameter fluctuations consisting of process-variation-effect (PVE), random-dopant-fluctuation (RDF), and an emerging fluctuation source: workfunction fluctuation (WKF). The characterization approaches are examined with experiment data. Base upon the independent of random variables, the total threshold voltage fluctuation, $\sigma V_{th,total}$, is expressed as follows [137]:

$$\sigma^2 V_{th,total} \approx \sigma^2 V_{th,RDF} + \sigma^2 V_{th,PVE} + \sigma^2 V_{th,WKF}, \tag{3.1}$$

where $\sigma V_{th,RDF}$, $\sigma V_{th,PVE}$, and $\sigma V_{th,WKF}$ are the threshold voltage fluctuations caused by the process-variation-effect, random-dopant-fluctuation, and the workfunction fluctuation, respectively. The statistical addition of individual fluctuation sources herein, Equation (1), simplifies the variability analysis of nano-devices and circuits, significantly [137].

3.1 Process Variation Effect

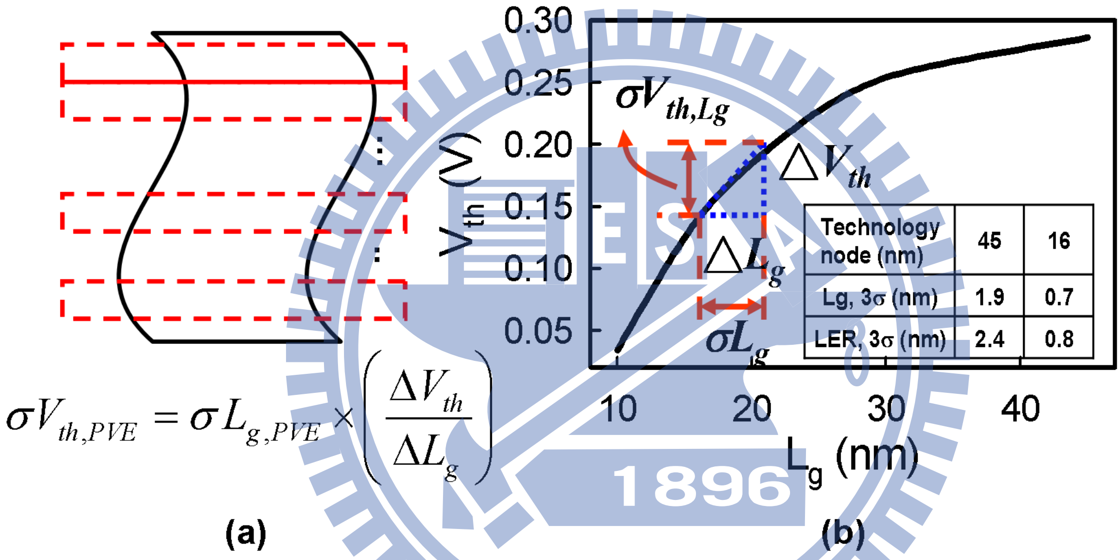


Figure 3.1: (a) An illustrates for the result of generated profile. The process-variation-effect induce gate length variation, $\sigma L_{g,PVE}$, are obtained. The inset shows the equation for the estimation of $\sigma V_{th,PVE}$. (b)A look-up table of the threshold voltage versus gate length. Using the V_{th} roll-off relation, the $\sigma V_{th,PVE}$ can be obtained.

During the manufacturing process, the inevitable variations of processing condition cause variations on device geometry, such as non-uniform gate oxide and material interface facial layer thickness, gate length deviation, line edge roughness, and so on [95]. All these fluctuations are getting worse with gate-length scaling. Among these process variation induced fluctuations, the gate-length deviation and the line edge roughness are the dominating factors; therefore, the fluctuations induced by these two effects are focused. Line edge roughness is arising not only from the resolution limit of lithography but also from the grainy nature of photo resist and gate. The effect of line width roughness is random and cannot be corrected by optical proximity correction. Therefore, a statistical approach is applied herein to evaluate the effect of process-variation-induced σV_{th}.

Figure 3.1(a) illustrates an example for the result of generated profile. The generation is similar to extraction of piecewise device gate length from SEM picture. The statistically generated profile is then averaged to obtain the effective gate length of a transistor. Then the process-variation-effect induce gate length variation, $\sigma L_{g,PVE}$, are obtained. The magnitude of the $\sigma L_{g,PVE}$ follows the roadmap of ITRS that $3\sigma L_g$ = 0.9 nm and $3\sigma LER$ = 1.2 nm for the 22 nm node and $3\sigma L_g$ = 0.7 nm and $3\sigma LER$ = 0.8 nm for the 16 nm technology node, as the inset table of Fig. 3.1(b). Fig. 3.1(b) is a look-up table of the threshold voltage versus the gate length is established. It enables us to evaluate the threshold voltage with respect to the gate length variation. Since the ΔL_g and ΔV_{th} are known parameters for the roll-off characteristics, the $\sigma V_{th,PVE}$ can be obtained for a given $\sigma L_{g,PVE}$,

$\sigma V_{th,PVE} = \sigma L_{g,PVE} \times \left(\frac{\Delta V_{th}}{\Delta L_g}\right)$. Notably, $\sigma L_{g,PVE}$ can be obtained from SEM critical dimension measurements.

3.2 Random-Dopant-Induced Characteristics Fluctuation

The random dopants come from the manufacturing process, such as ion implantation, thermal annealing. The random nature of discrete dopant distribution results in significant random fluctuations, such as the deviation of threshold voltage, drive current mismatch, and so on. The fluctuation budget has to be controlled even tighter due to the doubly increased transistor number along with technology node moving ahead. Unfortunately, the fluctuation is intrinsically increased with the scaling of transistor feature size, not even considering the worsened short channel control.

Figure 3.2 shows the equivalent number of dopants and channelling probability versus the size of channel. Under the same equivalent channel doping concentration, the equivalent number of dopants within the channel decreases significant from 78 to 17 as the channel size scales from (25 nm)^3 to (15 nm)^3. The dopant distributions are illustrated in the inset of Fig. 3.2. For larger device dimension, the surface potential is controlled by a cloud of remote charges. However, as device size scales, the surface potential is dominated by only a few dopants nearby. Impact of each discrete dopant is large enough to be distinct. A channeling probability is defined by the probability of existence of a channel

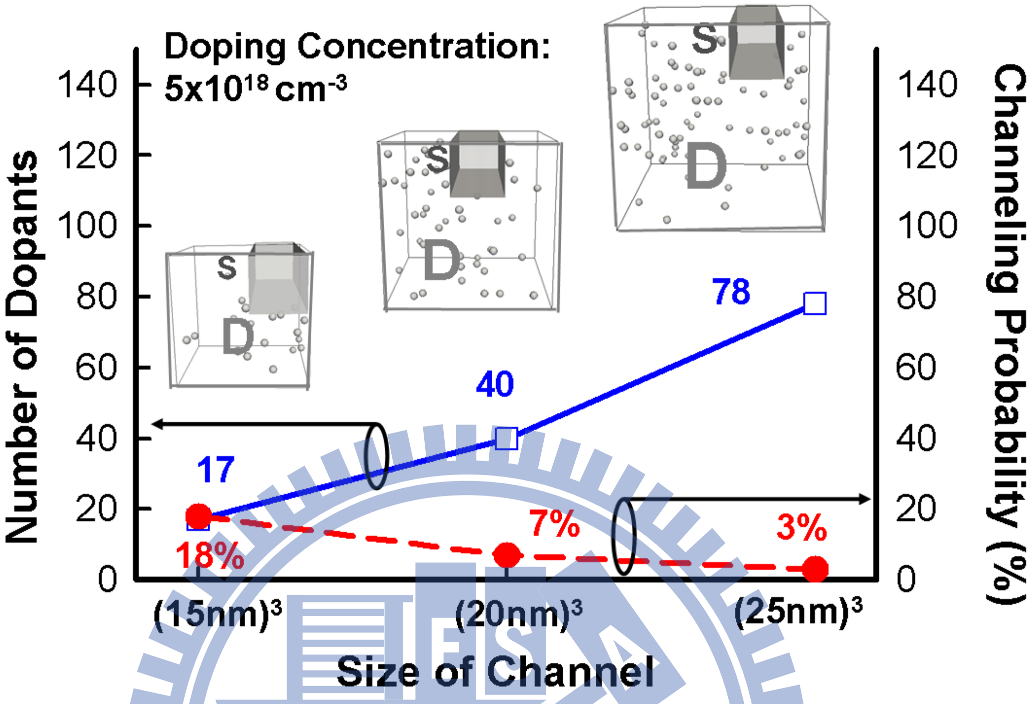


Figure 3.2: The equivalent number of dopants and channelling probability versus the size of channel.

with (7 nm)^2 cross-section between the source (S) and the drain (D) within the channel surface. The high carrier channeling probability indicates the increasing importance of dopant in scaled channel. Carriers transport in the (7 nm)^2 cross-section behaves as they are in an undoped channel. As the planar CMOS devices advance to sub-20-nm-gate lengths, double-digit channel dopants make transistor behaviours more complicated to be characterized with conventional ”continuum modelling” because every ”discrete” dopant has its significant weight impacting the resulting transistor performance. The ”discrete-dopant model" is especially validated for quantifying carrier channeling effects between the source and the drain, which can not be done by conventional continuum modeling. The next two subsections illustrate the generation approaches for discrete dopant cases.

3.2.1 Discrete Dopant Generation Method

Various random dopant effects have been recently studied in both experimental and theoretical approaches [21-27,62-89]. These studies have shown that the fluctuation of electrical characteristics are not purely a result of a variation in average doping density associated with a fluctuation in the number of dopants, but also the particular random distribution of dopants in the channel region. To characterize random dopant induced standard σV_{th} deviation, $\sigma V_{th,RDF}$, first the doping profile is analytical approximated to the device measured. Then, a statistical-sound "atomistic" simulation approach is described below, as shown in Fig. 3.3, to generate discrete dopants in the channel region. Figure 3.3 briefly illustrates how to generate discrete-dopant channel for aforementioned simulation, concurrently capturing randomness of dopant number and dopant position. Figure 3.3 (a) shows the discrete dopants randomly distributed in the cube of volume (100 nm)^3 with an average concentration of 5×10^{18} cm^{-3} which is the same as the fabricated device. There will be 5000 dopants within the (100 nm)^3 cube, but dopants vary from 24 to 56 (the average number is 40 and the standard deviation is 6.3) within its 125 sub-cubes of (20 nm)^3, as shown in Figs. 3.3(b),

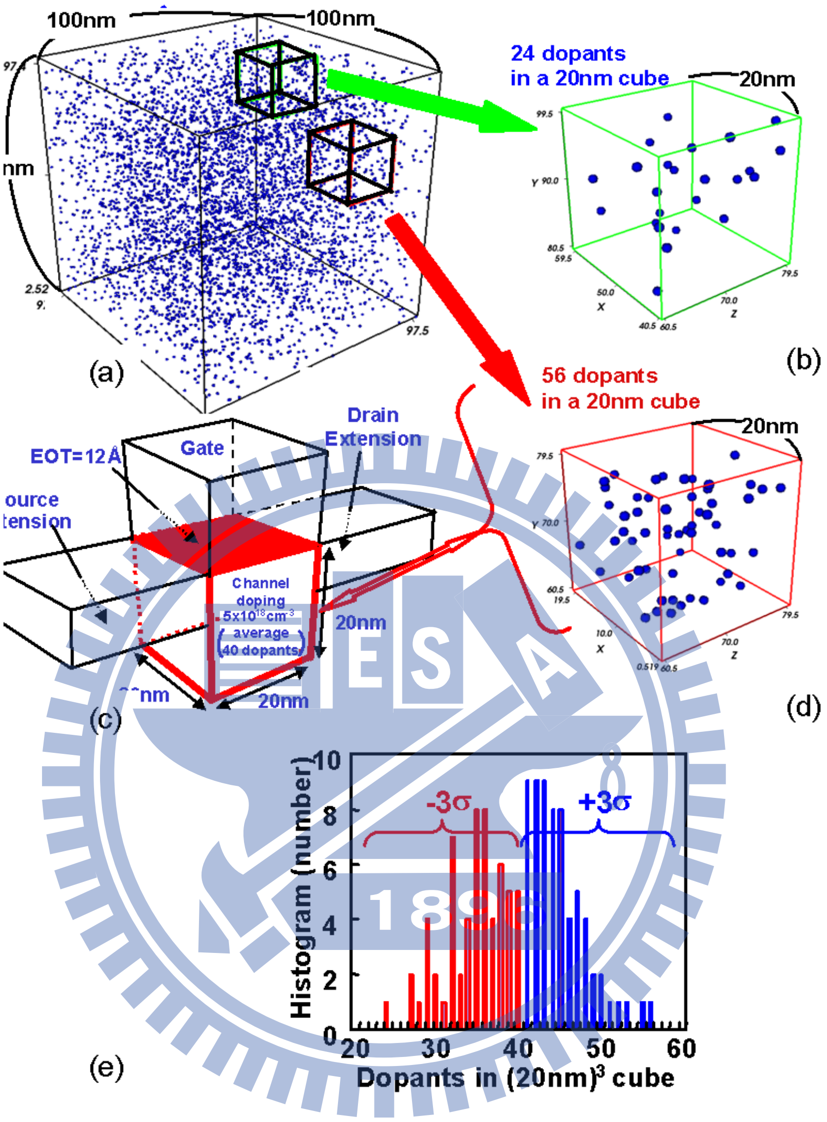


Figure 3.3: (a) Discrete dopants randomly distributed in (100 nm)^3 cube with an average concentration of 5×10^{18} cm^{-3}. 5000 dopants are in the (100 nm)^3 cube, but dopants vary from 24 to 56 (the average number is 40 and the standard deviation is 6.3) within its sub-cubes of (20 nm)^3, (the (b), (c), and (e)). These sub-cubes are then equivalently mapped into channel region for RDF simulation, as shown in the (d).

3.3(c), and 3.3(e), respectively. These 125 sub-cubes are then equivalently mapped into channel region for the discrete dopant simulation, as shown in Fig. 3.3(d). In principle, 3D device simulation with the 125 channel structures almost covers cases, shown in Figure 3.3(e), and thus will be fairly meaningful to reflect statistical randomness of dopant number and dopant position in channel region. Similarly, we can generate the discrete dopant cases for the study of nanoscale bulk FinFETs with channel size of (16 nm)^3, (22 nm)^3 and (30 nm)^3. With the same channel doping concentration. We consider three different channel dimensions, (16 nm)^3, (22 nm)^3, and (30 nm)^3. Take a device with (30 nm)^3 channel size as an example. For the channel region, to consider the effect of a random fluctuation in the number and location of discrete channel dopants, 5000 dopants are first generated in a large cube with (150 nm)^3, in which the equivalent doping concentration is 1.48×10^{18} cm^{-3}, as shown in Fig. 3.4(a). The (150 nm)^3 cube is then partitioned into 125 sub-cubes of (30 nm)^3. The number of dopants may vary from 26 to 55, and the average number is 40, as displayed in Figs. 3.4(b) and 3.4(d), respectively. These 125 sub-cubes are then equivalently mapped into the channel region of the device for the 3D discrete dopant simulation, as shown in Figs. 3.4(b), and 3.4(c). The distributions of discrete dopant fluctuated cases for 22 nm and 16 nm gate lengths can be generated by a similar approach, as show in Figs. 3.4(e) and 3.4(f). All statistically generated discrete dopants are incorporated into

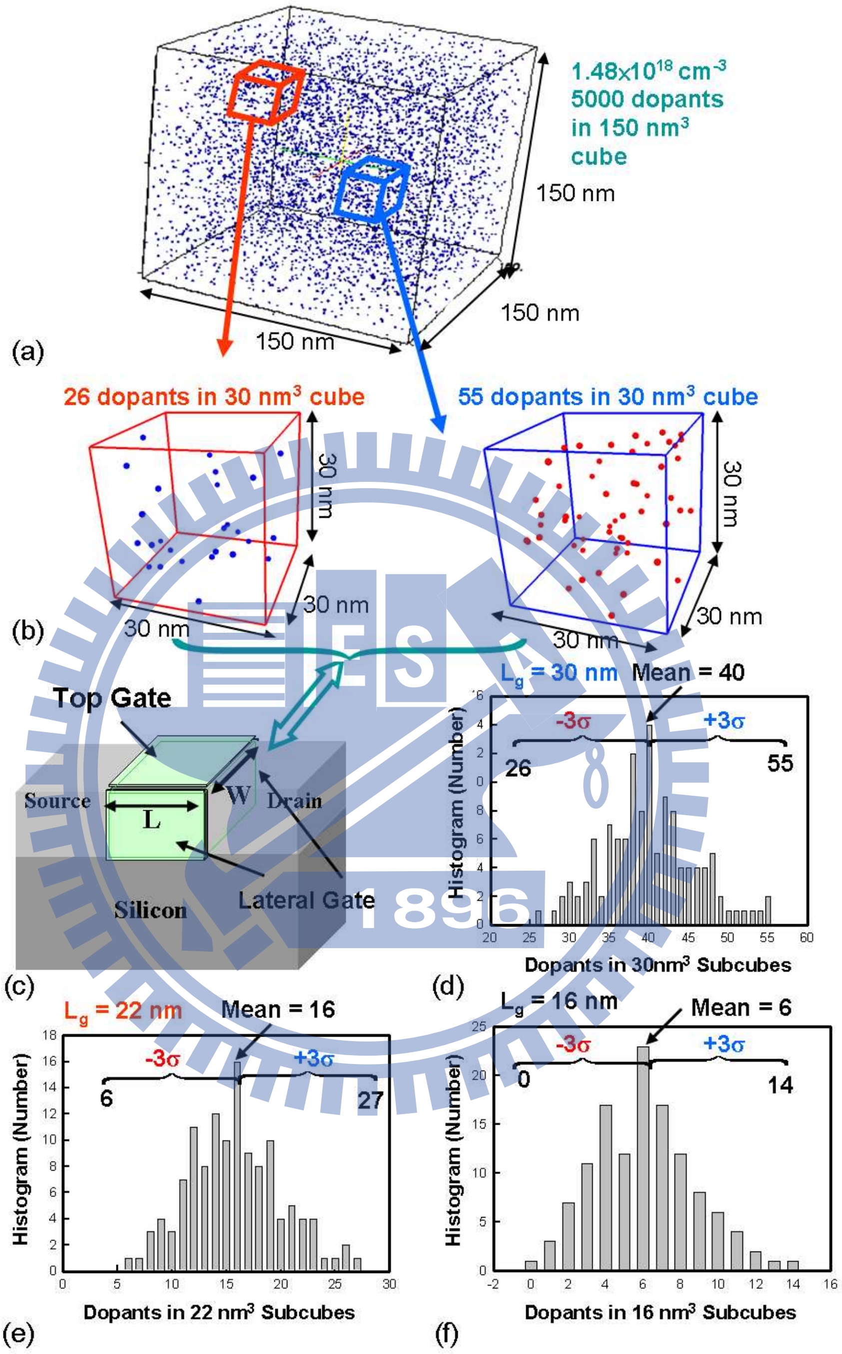


Figure 3.4: (a) Discrete dopants randomly distributed in (150 nm)^3 cube with average concentration of 1.48×10^{18} cm^{-3}. 5000 dopants are within the cube, but dopants may vary from 26 to 55 (average number is 40) within each of the sub-cubes of (30 nm)^3, [(b) and (d)]. The sub are then used for RDF simulation (c). The statistically generated discrete-dopant distributions for (e)22- and (f)16-nm-gate length.

the large-scale 3D device simulation, which is conducted using a parallel computing system. According to this analyzing scenario, only channel dopants are treated discretely. The doping concentrations remain continuous in the source/drain region because the volume of source/drain dopants is about 5 times greater than that of channel dopants. Nevertheless, this approach allows us to focus on the study of characteristic fluctuations induced by the randomness in the number and position of dopants in the channel simultaneously. The statistically sound 3D ”atomistic” device simulation technique is also computationally cost-effective.

3.2.2 Kinetic Monte Carlo Simulation

The accuracy of above large-scale statistic dopant generation has been calibrated with experimentally measured data, which will be discussed in following section. To present a more practical dopant distribution inside device channel, we further integrate the Kinetic Monte Carlo (KMC) atomistic process simulation with atomistic device simulation [131–133]. Due to the shrinking of thermal budget, the diffusion, activation, and deactivation are shrink form millisecond to nanosecond. The accuracy of continuous process simulation to model the behavior of dopants during manufacturing is questionable. The Kinetic Monte Carlo simulation is therefore used to mimic the dopant distribution inside silicon channel. Based on the given thermal budget, the dopant distribution is simulated in

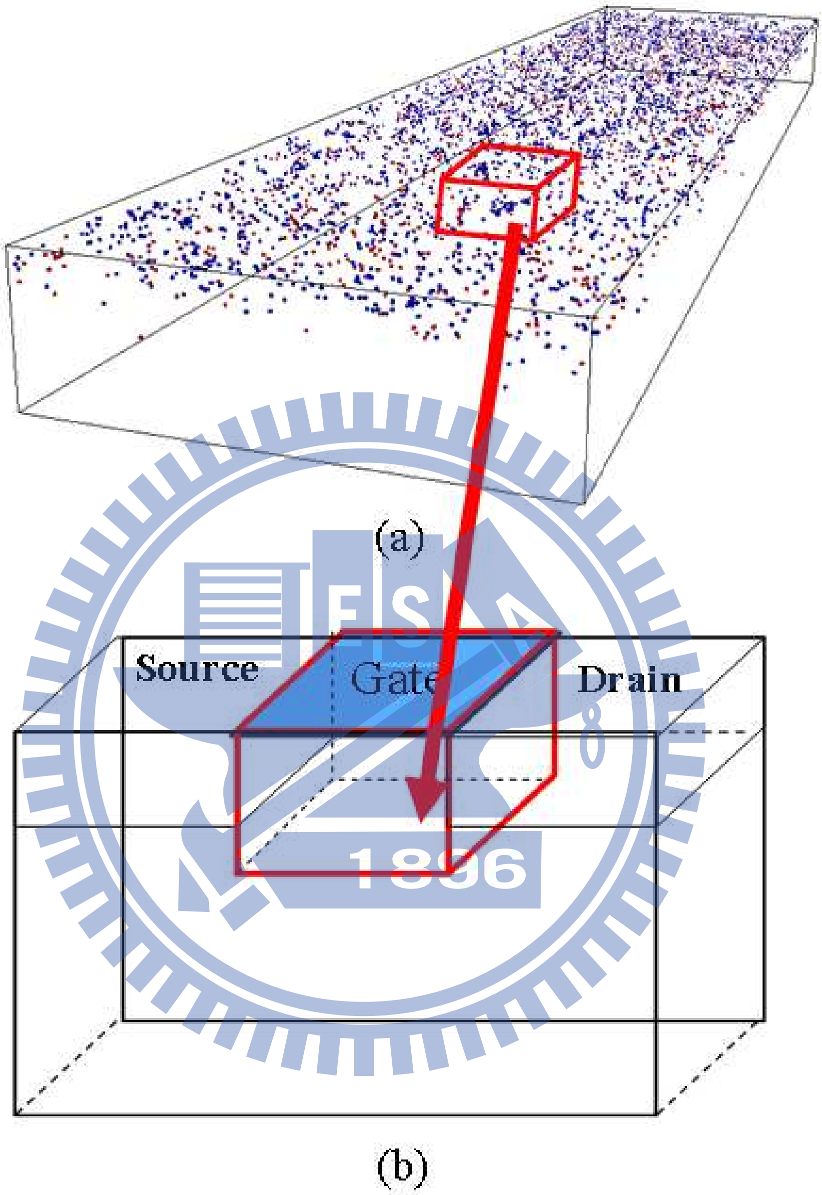
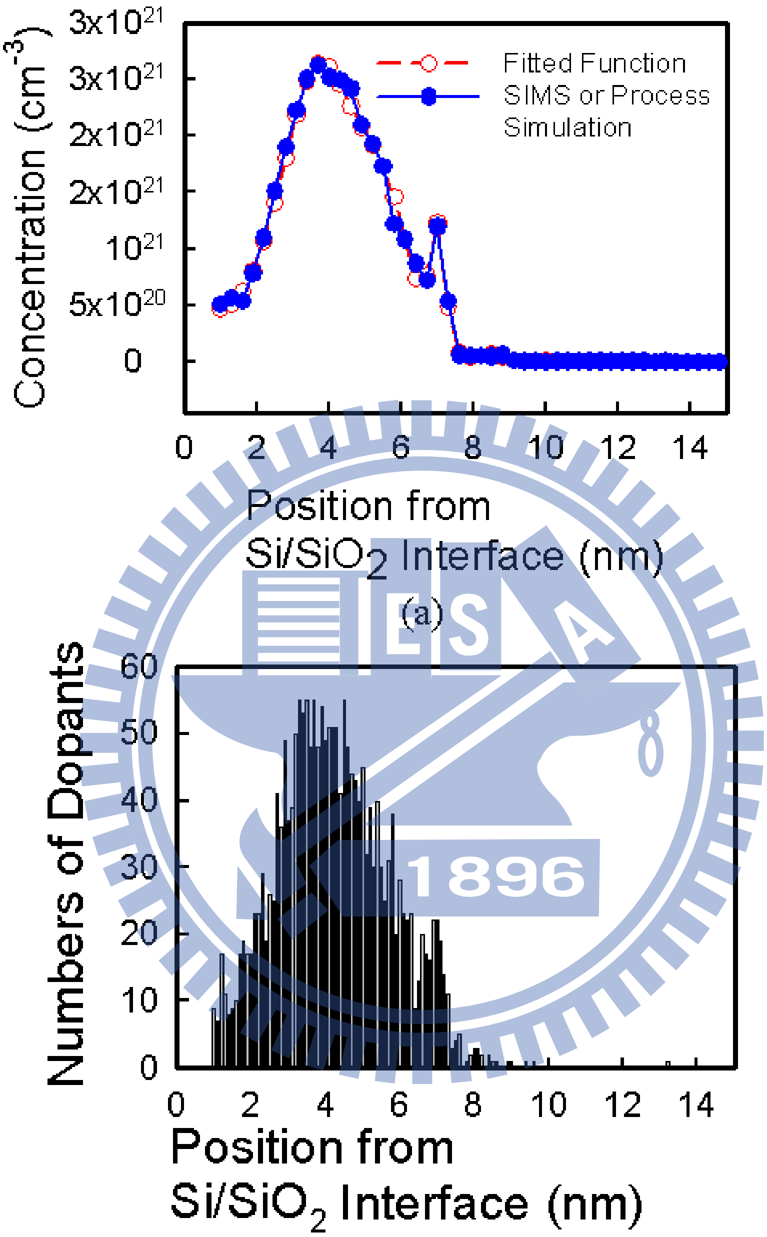


Figure 3.5: Integration of kinetic Monte Carlo (KMC) atomistic process simulation with atomistic device simulation. (a) The KMC simulation generated dopant distribution. The Kinetic Monte Carlo simulation is therefore used to mimic the dopant distribution inside silicon channel. (b) The generated dopant distribution is then mapped into device channel for simulation.



(a)

(b)

Figure 3.6: (a) The distribution of KMC simulated profile. The solid line is the dopant distribution, which can be replaced by SIMS profile. The dash line is the fitted distribution, which is similar to the original dopant distribution. (b) The generated 5000 dopants, whose distribution along the Si/SiO$_2$ interface is similar to the original profile, the solid line in (a).

Fig. 3.5(a). The simulation domain of KMC simulation is flexible. The generated positions of dopants are then mapped in to device channel region for atomistic device simulation, as plotted in Fig. 3.5(b). Figure 3.6(a) shows the distribution of KMC simulated profile. The simulated distribution can be replaced by measured secondary ion mass spectrometry (SIMS) doping profile. The solid line is the dopant distribution, which can be replaced by SIMS profile. The dash line is the fitted distribution, which is similar to the original dopant distribution. As the distribution of dopants is obtained, we can fit the distribution function of the profile then generate the associated dopant distribution for random dopant simulation, as presented in Fig. 3.6(b). There are 5000 generated dopants, whose distribution along the Si/SiO$_2$ interface is similar to the original profile, the solid line in Fig. 3.6(a). Consequently, our dopant generation approach is flexible to capture any distribution of dopants with adequate the accuracy.

3.3 Workfunction fluctuation

High-κ/metal-gate technology has been recently recognized as the key to sub-45 nm transistor fabrication due to the small gate leakage current with an increased gate capacitance. Moreover, the sheet resistance is reduced with the use of metal as gate material. Comparing to the poly-gate technology, the metal-gate material will not react with high-κ material and therefore there existing less interface charge and V_{th} pinning effect. The gate depletion in

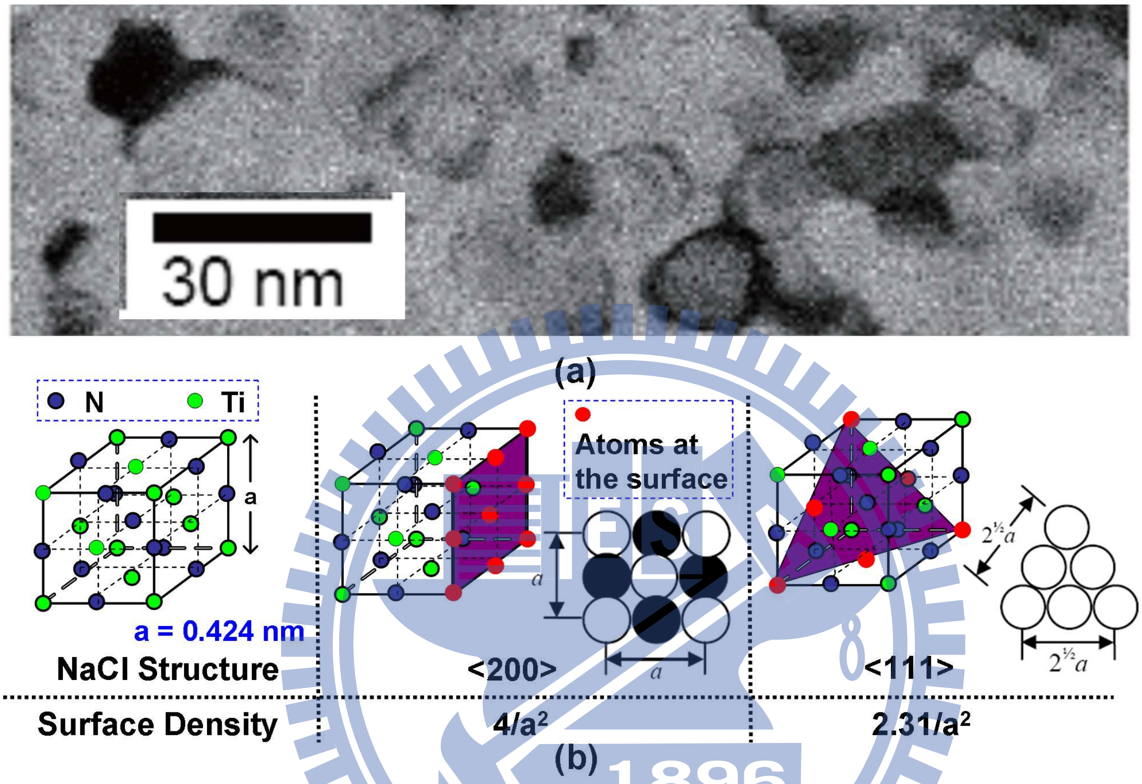
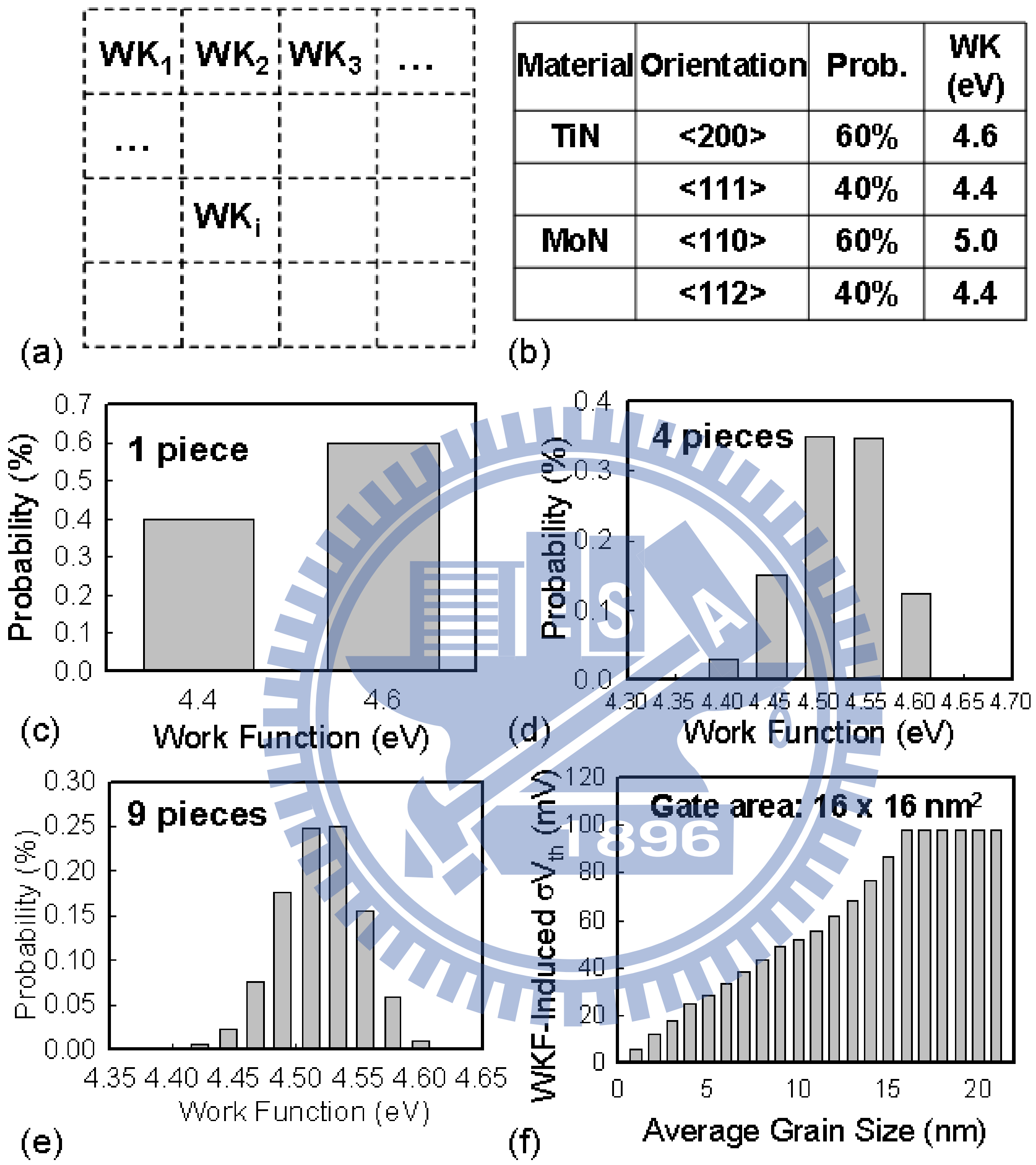


Figure 3.7: (a) The SEM pictures and illustration of TiN surface, which containing numbers of grain with various grain orientation. (b) An illustration of crystal structure of copper with <200>, and <111> orientation. Each grain orientation has its own strength of dipoles and therefore different workfunction. Therefore, the combination of device workfunction will become a probabilistic distribution rather than a deterministic value.

poly-gate material is no longer existed. Additionally, the phono scattering effect is significantly reduced due to the less quantum resonance effect. However, the grain orientation of metal is uncontrollable during growth period. The use of metal as a gate material introduces a new source of random variation due to the dependency of workfunction on the orientation of metal grains [121-123]. Figure 3.7(a) shows the SEM pictures of Titanium nitride (TiN) [123]. TiN is a rocksalt-structure (NaCl structure) compound consisting of Ti atoms filled in FCC-based lattice with all octahedral sites filled with nitrogen atoms. As shown in the plot, the surface is composed by numbers of grain and each grain may have different orientation, as illustrated in Fig. 3.7(b). Since the different grain orientation has its own strength of dipoles, the workfunction in each grain orientation is different. The device V_{th} will become a probabilistic distribution rather than a deterministic value.

To characterize the metal-gate induced workfunction fluctuation, a statistically sound Monte-Carlo approach is advanced here for examining such distribution. The simulation flow is expressed in Fig. 3.8. At first, the gate area is partitioned into several parts according to the average grain size, as shown in Fig. 3.8(a). Then the grain orientation of each parts and total gate workfunction are randomly generated based on properties of metal as shown in Fig. 3.8(b) [122]. The workfunction of each partitioned area (WK_i) is a random value. The summation of WK_i is then averaged to obtain the effective workfunction of transistor



Material	Orientation	Prob.	WK (eV)
TiN	<200>	60%	4.6
	<111>	40%	4.4
MoN	<110>	60%	5.0
	<112>	40%	4.4

Figure 3.8: The gate area is partitioned into several pieces according to the average grain size. The workfunction of each partitioned area (WK_i) is a random value, whose probability follows (b). The obtained probability distributions of TiN workfunction for devices with (c) 1, (d) 4, and (e) 9, grains on the gate area. (f) Dependence of TiN metal-gate induced $\sigma V_{th,WKF}$ versus the average grain size. The gate area is 16×16 nm^2

and then used for WKF-induced threshold voltage fluctaution estimation. Figures 3.8(c)-3.8(e) show the probability distributions of workfunction for devices with one, four, and nine grains on the gate area. The distribution is similar to the normal distribution as the numbers of grain increases. In other words, in nanoscale transistor with scaled gate area, the distribution is not a normal distribution and therefore the WKF-induced σV_{th} may not be a normal distribution as the gate area scales. Figure 3.8(f) examines the dependence of WKF-induced σV_{th} versus the average grain size on a 16 × 16 nm^2 gate area. The material is TiN. The WKF-induced σV_{th} increases significantly as the average grain size increases, which imply the importance of controlling metal-gate grain size in reducing WKF effect. The $\sigma V_{th,WKF}$ saturates after 16 nm average grain size because the average grain size becomes larger than gate area. The average grain size of this study is four nm [122]. Notably, the different process of gate formulation, gate first or replacement gate, may change the thermal budget and changes the grain size of metal material.

Notably, the results of statistical generation approach is similar to previous literature [122]. However, the previous literature used a probability density function to estimate the population of workfunction. The estimation approach is fast, but can not consider the residual blocks during the discretization procedure, as illustrated in inset of Fig. 3.9. Thus, we use a monte carlo random generator to estimate the random gate workfunction fluctuation. Figure 3.9 presents the MoN induced V_{th} fluctuation for device with 16-nm-gate area.

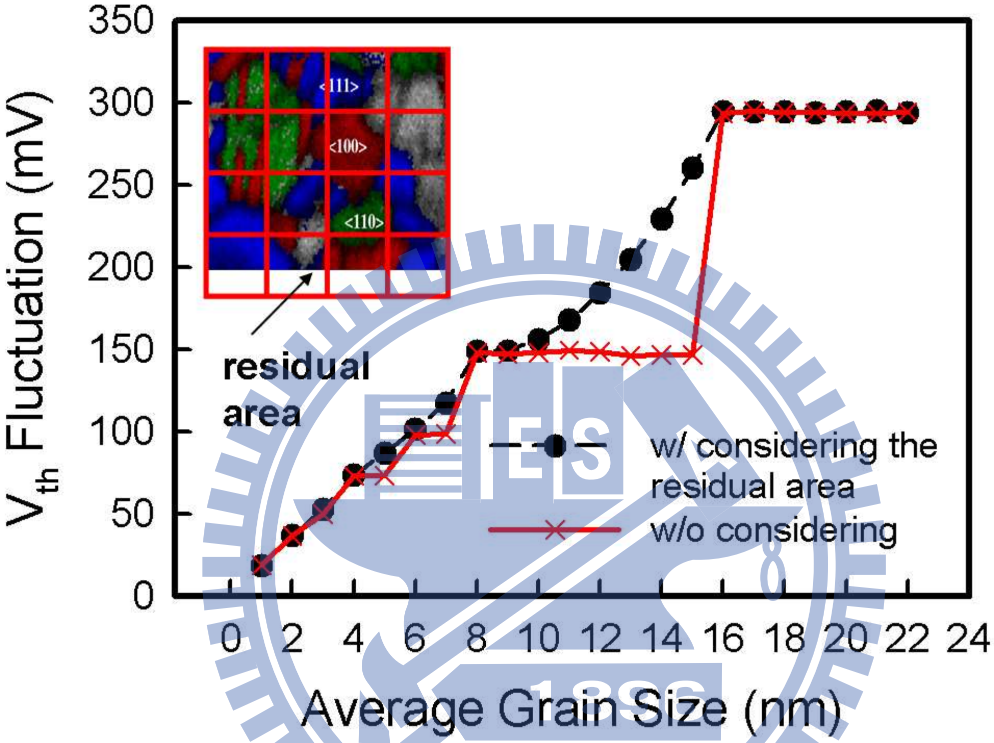


Figure 3.9: WKF induced V_{th} fluctuation versus average grain size with and without taking residual gate area into consideration. The inset illustrates the residual gate area during the discritization of gate area. The flat area in the solid line may mislead the impact of WKF.

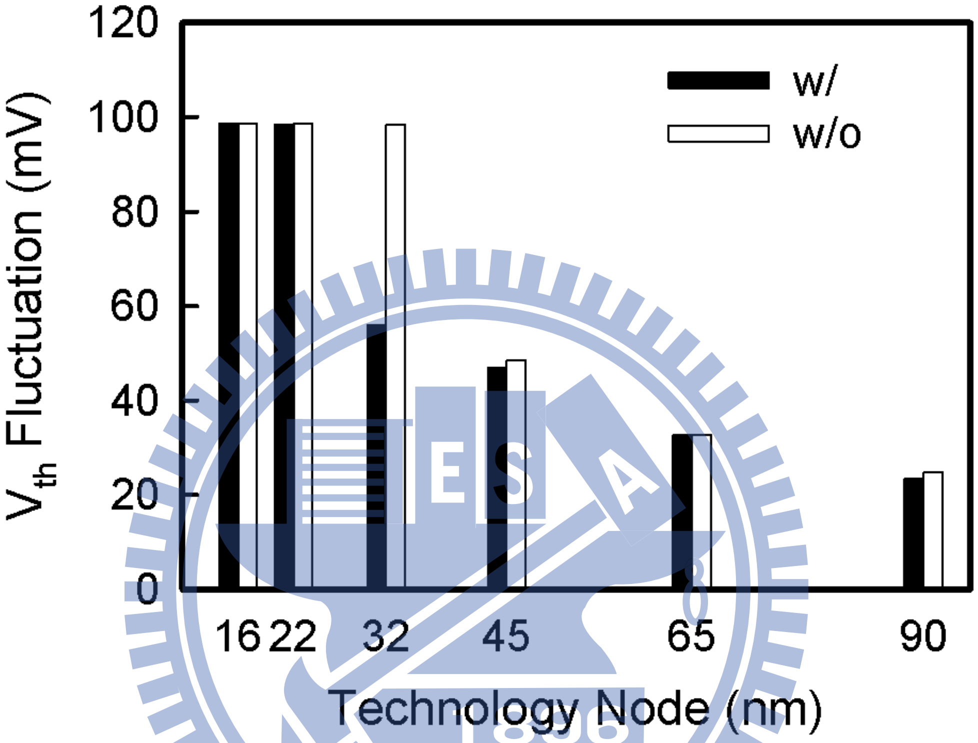


Figure 3.10: WKF induced V_{th} fluctuation in various technology node with and without taking residual gate area into consideration. The WKF effect saturates after 32 nm, which is similar to the results of previous literature [122]. However, for the newly developed Monte Carlo simulation approach, the WKF effect saturates after 22 nm. Since the average grain size is 22 nm, having the same V_{th} fluctuation after 22 nm is reasonable.

The dash and symbol line shows the Monte Carlo results with considering the discreteized residual area. As the average grain size decreases, the gate area contains a large number of grain and therefore the difference of averaged workfunction is averaged. The solid line is the control group without considering residual area. The trend of V_{th} fluctuation is the same as the other; however, there are several flat area existing in the solid line, which may mislead the impact of WKF. For example, Fig. 3.10 shows the WKF induced V_{th} fluctuation for 90 nm to 16 nm technology node with and without taking residual gate area into consideration. In previous literature, the WKF effect saturates after 32 nm, which is similar to the results without residual gate area. However, for the newly developed Monte Carlo simulation approach, the WKF effect saturates after 22 nm. Since the average grain size is 22 nm, having the same V_{th} fluctuation after 22 nm is reasonable. The obtained distribution of workfunction is then mapped to the device gate area for workfunction fluctuation simulation. We have to notice that though the current computation methodology can provide a fast estimation of WKF-induced fluctuation, the obtained WKF is an averaged result containing no crystallized grain in simulation. Therefore, the impact of WKF may be underestimated. More complicated WKF simulation including the nucleation and growth of metal and grain boundary effect has been taken into our future work.

3.4 Calibration and Verification

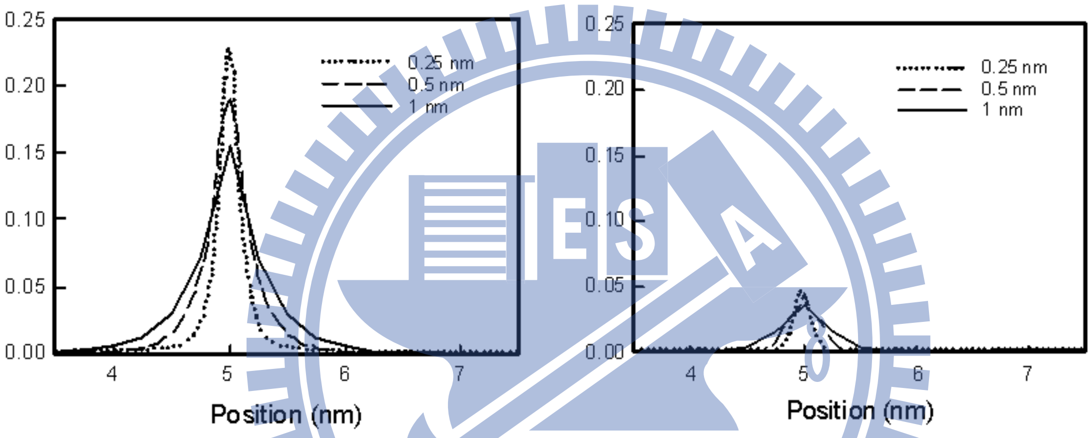
The device is simulated by solving a set of 3D Poisson equation and electron-hole current continuity equations with quantum corrections [99-103]. A step function, N_A, is used to define the concentration and positions of dopants.

$$N_A = \sum_{i=0}^{k} N_A^{dopant} \cdot \begin{bmatrix} H\left(x - x_l, y - y_l, z - z_l\right) \\ -H\left(x - x_u, y - y_u, z - z_u\right) \end{bmatrix}, \tag{3.2}$$

where

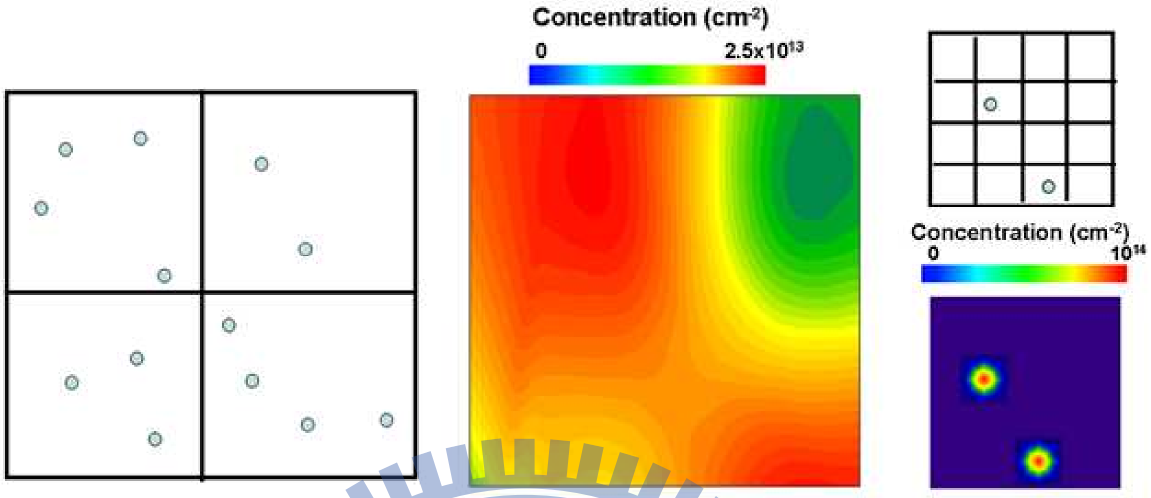
$$H\left(x, y, z\right) = \begin{cases} 1, x \geq 0, y \geq 0, z \geq 0 \\ 0, \text{otherwise} \end{cases} \tag{3.3}$$

(x_l, y_l, z_l) and (x_u, y_u, z_u) are the lower and upper coordinates of a discrete dopant; k is the number of dopants in the device channel; N_A^{dopant} is the associated doping concentration for a dopant within a box. Then, N_A is substituted into the source of the Poisson equation and solved with the electron-hole current continuity equations and density-gradient quantum correction equations simultaneously for device characteristics. Notably, in ”atomistic” device simulation, the resolution of individual charges within a conventional drift-diffusion simulation using a fine mesh creates problems associated with singularities in the Coulomb potential [81-83]. The potential becomes too steep with fine mesh and therefore the majority carriers are unphysically trapped by ionized impurities and the mobile carrier density is reduced [81-83]. Thus, the density gradient approximation is used to handle discrete charges by properly introducing the related quantum mechanical effects [99-103]. All statistically generated discrete dopants are advanced and incorporated into the 3D device simulation under our parallel computing system [109-112]. Such large-scale simulation approach allows us to explore the electrical characteristic fluctuations induced by randomness of dopant number and position in the channel region concurrently. Figures 3.11(a) and 3.11(b) illustrate the mesh size dependence of the classical and quantum mechanical potentials for a single discrete dopant within the silicon channel. In the "atomistic" simulation, the key point to study random impurities induced fluctuation relies on how to introduce the microscopic non-uniformity of localized impurity distributions inside



(a) (b)

Figure 3.11: Potential profiles for (a) classical (b) and quantum potential with different mesh size.



(a) (b)

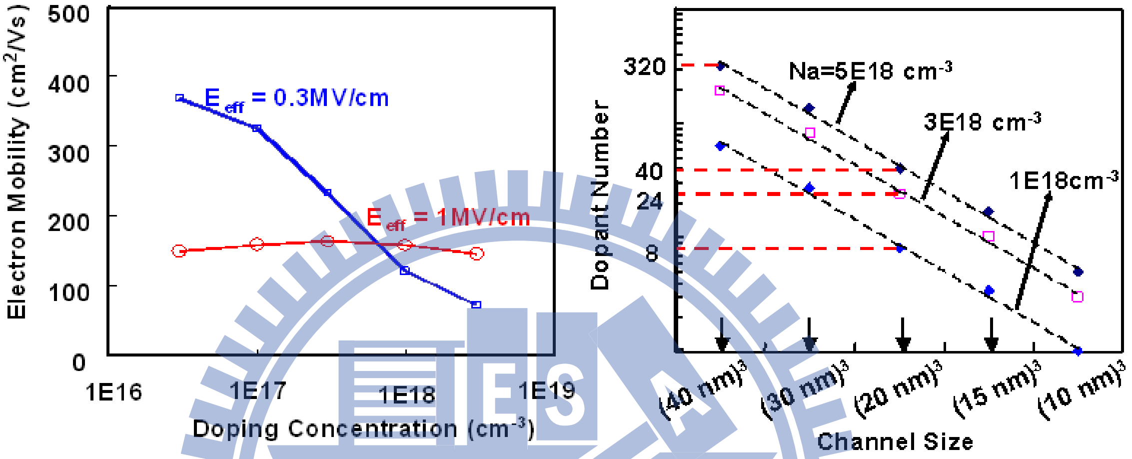
Figure 3.12: Meshing and dopant distribution for (a) long channel and (b) nanoscale transistors. The fine mesh in nanoscale transistor creates problems of singularities in the Coulomb potential and un-physically trap majority carriers.

the device. In conventional drift-diffusion approach for a large device size, the number of impurities included in each mesh exceeds one and the equivalent doping concentration does not change abruptly at every mesh node. Also, the dopant density at each mesh node changes gradually and the non-uniformity of impurity arrangement is averaged, as shown in Fig. 3.12(a). However, for the nanoscale transistor, the corresponding number of impurities is significantly reduced. Most meshes contain no dopant or, at most, one dopant. The dopant density at each mesh node changes its order of magnitude and behaves like a

-function, as shown in Fig. 3.12(b). The resolution of individual impurities for the conventional drift-diffusion simulation using a fine mesh creates problems of singularities in the Coulomb potential, as shown in Fig. 3.11(a). The sharp Coulomb potential wells may un-physically trap majority carriers, reduce the mobile electron concentration, modify the depletion region, and alter the threshold voltage. Therefore, the density gradient quantum correction [99-103] is used to handle the discrete dopant effect by properly introducing the related quantum mechanical effects, as plotted in Fig. 3.11(b). The quantum mechanical potential show less sensitivity to the mesh size and is quite similar for mesh spacing below 0.5 nm. We notice that the potential barrier of the Coulomb well is about 45 mV, which roughly corresponds to the ground state of a hydrogenic model of an impurity in silicon.

To extract the experimental data of $\sigma V_{th,RDF}$, the $\sigma V_{th,total}$ and $\sigma V_{th,PVE}$ are first directly measured from experimental data. Since the mean gate length deviation, line edge roughness and random dopant distribution are the major variation sources of threshold voltage. The $\sigma V_{th,RDF}$ thus can be extracted from the approximated equation of Eq. 3.1. Notably, the equation implies two important insights: $\sigma V_{th,total}$ reduction more relies on dominant factor improvement and the 2^{nd} order factors will not impact the derived value of $\sigma V_{th,RDF}$. For example, assuming the $\sigma V_{th,RDF}$ and $\sigma V_{th,PVE}$ are 40 and 30 mV, respectively, the $\sigma V_{th,total}$ is 50 mV. The 16% reduction of $\sigma V_{th,RDF}$ achieves 16% reduction of $\sigma V_{th,total}$; however, it requires the 31% reduction of $\sigma V_{th,PVE}$ to obtain the same $\sigma V_{th,total}$.

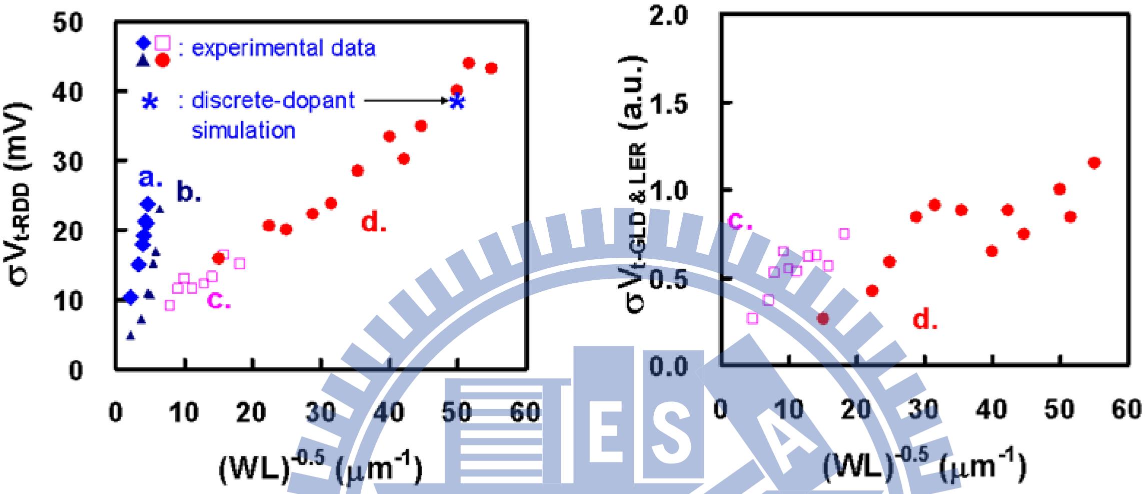
Moreover, even with an addition fluctuation sources, 20 mV, is introduced. The $\sigma V_{th,total}$ is around 52 mV, which indicates the 2^{nd} order factors will not impact the derived value of $\sigma V_{th,RDF}$.



(a) (b)

Figure 3.13: (a) Extracted non-strain mobility versus doping concentration at 0.3 and 1 MV/cm vertical field, and (b) scaling of average channel dopant numbers versus channel size.

The employed physical model is first calibrated with experiment data. The mobility model is quantified with device measurements for the best accuracy. The used mobility model can generate mobility that is in good agreement with the extracted mobility, as shown in Fig. 3.13(a). The low-field electron mobility at 0.3 MV/cm is greatly reduced with increasing doping concentration. That is why we limit our channel doping concentration



(a) (b)

Figure 3.14: (a) Experimentally extracted $\sigma V_{th,RDF}$, and discrete-dopant simulation (*, L_g = W = 20 nm, EOT = 1.2 nm) for various devices with nominal L_g from 55 nm down to 20 nm. The width is fixed and the length is varying to give the range of values of (WL)$^{-0.5}$. The sample size for each data point of V_{th} is around 100 points. (b) The extracted $\sigma V_{th,PVE}$ for c and d conditions. The value was normalized against the $\sigma V_{th,PVE}$ of nominal L_g case in d condition.

Table 3.1: The trend of V_{th} for technology scaling. The nominal L_g cases in table are nominal gate lengths for each technology node respectively.

	EOT (nm)	Channel Doping (cm^{-3})	Nominal L_g (nm)	Width (nm)
a	2.4	1.0×10^{18}	55	1000
b	1.8	3.0×10^{18}	35	1000
c	1.2	5.0×10^{18}	20	200
d	1.2	5.0×10^{18}	20	20

Table 3.2: Summary of experimental and simulation results of discrete dopant fluctuated 20-nm-gate planar CMOS transistors.

L_g (nm)	Width (nm)	Data Source	Channel Doping (cm^{-3})	EOT(nm)	$V_{th,RDF}$ (mV)
20	200	experimental	5.0×10^{18}	1.2	17
20	200	simulation	5.0×10^{18}	1.2	17.7
20	20	experimental	5.0×10^{18}	1.2	40
20	20	simulation	5.0×10^{18}	1.2	39

around 1×10^{18} cm^{-3}. Less channel doping concentration may reduce $\sigma V_{th,RD}$, but channel dopants will quickly approach to single-digit number, as shown in Fig. 3.13(b). The random-dopant-induced V_{th} fluctuation, $\sigma V_{th,RDF}$, has then been experimentally extracted, as shown in Fig. 3.14(a). Discrete-dopant simulation for L_g = width (W) = 20 nm (data represented with symbol *, as shown in Fig. 3.14(a)) in good agreement with the experimental data, which confirms the channel doping is randomly distributed as statistically modeled. As shown in Fig. 3.3, more than 100 cases are required for a set of L_g and width; we notice that each 3D simulation case may take about 3 to 7 days for final convergent result. Without loss of generality, due to the heavy computing resource, we select the most critical case (i.e., length = width = 20 nm) for comparison between simulation and measurement. Figure 3.14(b) shows the extracted $\sigma V_{th,PVE}$ of c and d conditions. The $\sigma V_{th,PVE}$ contains the contribution from the mean gate length deviation and the line edge roughness. In our experimental data, the $\sigma V_{th,PVE}$ increases as the (WL)$^{-0.5}$ increased, and it has similar trend, compared with $\sigma V_{th,RDF}$. Table 3.1 summaries the corresponding parameters for all cases in Fig. 3.13. Figure 3.13(a) shows the extracted mobility versus the doping concentration from samples of the cases a and b, as shown in Fig. 3.14(a). Table 3.2 summaries the experimental and simulation results of discrete dopant fluctuated 20-nm-gate planar CMOS transistors. The summary corresponds to Fig. 1.2 in previous section. The experimentally extracted $\sigma V_{th,RDF}$ for devices with 200-nm- and 20-nm-width are about 17 and

40 mV. The result of developed simulation metrology is similar to the experimental data, which confirms the reliability of this approach. The mathematical device simulation accuracy is calibrated with full quantum mechanical simulation and energy level of impurities. The accuracy of large-scale statistical methodology is verified by experimental data. The proposed simulation approach is convincing in study of nanoscale transistor variabilities.

3.5 Summary

For PVE, the $\sigma L_{g,PVE}$ can be obtained from extracted the line-edge shape of a device gate from SEM pictures or through the statistically generated line-edge profile. The process-variation-effect includes the gate length variation and line edge roughness, whose magnitude follows the ITRS roadmap. The look-up table of the threshold voltage versus the gate length from threshold voltage roll-off slope is provided to estimate the effect of $\sigma L_{g,PVE}$ in $\sigma V_{th,PVE}$. The simulation of random dopant effect relies on the generation and assignment of discrete impurities in transistors. The large-scale generation approach is similar to the manufacturing process. Then the generation approach has been extended by using ”atomistic” process simulation and SIMS profile. After the dopant generation, the dopants are assigned into device channel region by using step function for discrete dopant simulation. The simulation result has been verified with experimentally measured data. The workfunction fluctuation is an emerging source of fluctuation accompanied by the high-κ/metal-gate technology. In this thesis, an statistical generation approaches has been applied and used for device and circuit fluctuation analysis. However, we have to notice the simulation approach can be further improved by incorporating the nucleation and growth of metal and grain boundary effect. Based on the large-scale statistic approaches, the fluctuation of device characteristics can be obtained then used for evaluation of circuit reliability.

Chapter 4

Random-Dopant-Induced Characteristics Fluctuation in Vertical-Channel Devices

ITRS roadmap [1] has forecasted the transition from planar MOSFETs structure to vertical channel device structure and bulk silicon substrate to insulator substrate for performance enhancement and leakage current reduction. Though the un-doped SOI devices can prevent the random-dopant-induced fluctuation, they may suffer from more significant SCEs. Thus, the channel doping must be employed to alter the threshold voltage and provide the promising electrical characteristics in today's semiconductor manufacturing processes. Consequently, characteristic fluctuation that is induced by discrete dopants is important in these nanoscale MOSFETs, which with fascinating structures. Since the random dopant fluctuation is the dominating factor in device variability, this chapter investigates the discrete-dopant-induced device fluctuation in bulk FinFETs and SOI devices from single-gate to surrounding-gate nanowire transistors by using 3D atomistic device simulation with density-gradient quantum correction on our parallel computing systems. An insight into the intrinsic fluctuation and the mechanism of immunity against fluctuation in multiple-gate devices has been provided.

4.1 Bulk Fin-Type Field Effect Transistors

The bulk FinFET has shown its promising characteristics in nanoscale transistor era. This section explores the characteristic fluctuations of bulk FinFETs from (30 nm)^3 to (22 nm)^3 and (16 nm)^3 by 3D statistically full-scale "atomistic" device simulation technique. The fluctuation resistance of bulk FinFETs are compared with planar MOSFET with high-κ material, whose equivalent oxide thicknesses ranging from 1.2 nm to 0.2 nm (e.g., SiO_2 for the 1.2 and 0.8 nm EOTs, Al_2O_3 for the 0.4 nm EOT and HfO_2 for the 0.2 nm EOT). Finally, the discrete-dopant-fluctuated V_{th} roll-off characteristics are explored. The relation between device geometry and fluctuation are established for future fluctuation estimation.

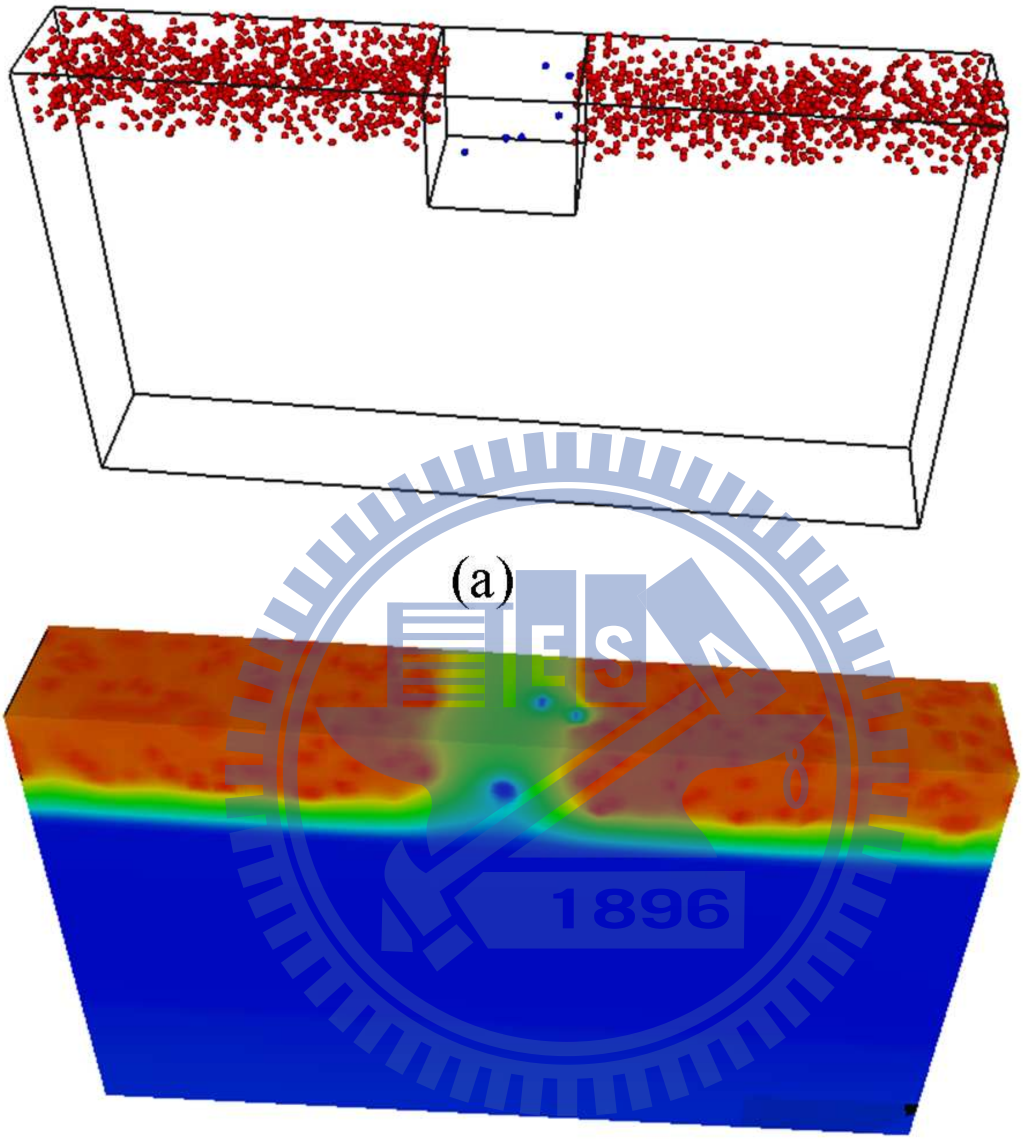
Table 4.1: The the threshold voltage fluctuation induced by S/D dopants only, channel dopants only, and fully discrete schemes and the simulation time for one transistor.

RDF Scheme	σV_{th} (mV)	Computation time (HR)
Source/Drain dopants only	10.5	∼24
Channel dopants only	28.3	∼6
Source/Drain + Channel dopants	29.3	∼42

4.1.1 Roll-Off Characteristics

As MOSFETs shrink in size, unlike the electrostatic potential in large MOSFETs, which is controlled by a cloud of remote charges, the electrostatic potential of small MOSFETs is dominated by only a few nearby charges whose contributions are large enough to be distinct. Many approaches have been reported for the investigation of the dependence of device scaling on discrete-dopant-induced fluctuation. The fluctuation of V_{th} in planar MOSFETs is inversely proportional to square root of the device area. However, for bulk FinFET device, because of the variety of device structures, the dependence of V_{th} fluctuation on the channel area of the device is not clear yet. Therefore, we thus explore the fluctuations of V_{th}roll-off in nanoscale bulk FinFETs by a 3D statistically full-scale ”atomistic” device simulation technique.

The explored devices are of three different dimensions: (16 nm)^3, (22 nm)^3 and (30 nm)^3. The nominal channel doping concentration of these devices is 1.48×10^{18} cm^{-3}.



(a)

(b)

Figure 4.1: (a) The dopant distributions for the fully discrete scheme in 16-nm-gate transistor. Both source/drain and channel dopants are placed randomly in device. (b) The associated potential distribution, in which the effective device gate length was disturbed.

They have a workfunction of 4.4 eV and a gate oxide thickness of 1.2 nm. Outside the channel, the doping concentrations in the source/drain and the background are 3×10^{20} cm^{-3} and 1×10^{15} cm^{-3}, respectively. The generation approaches are shown in Fig. 3.4. At first, to clarify the importance of source/drain dopants and channel dopants in device variability, the RDF simulation is separated as S/D dopants only, channel dopants only, and fully discrete schemes. Figures 4.1(a) show the dopant distributions for the fully discrete scheme in 16-nm-gate transistor, in which both source/drain and channel dopants are placed randomly in device. The associated potential distribution is shown in Fig. 4.1(b). The source/drain dopants will influence the resistance of source/drain of device and disturb the device effective gate length. The simulation result is summarized in Tab. 4.1, where the threshold voltage fluctuation induced by correspondent fluctuation sources and the simulation time for one transistor are presented. Comparing to the fully discretized scheme, the channel dopant is in charge of 95% of totally discrete impurities induced σV_{th}. Since the volume and the average number of dopants in the source/drain region (4608 dopants in $16\times8\times120$ nm^3) are several times larger than that of the channel region (6 dopants in $16\times16\times16$ nm^3), the impact of source/drain dopants is averaged and therefore bring less impact on device threshold voltage fluctuation. Additionally, the computation time considering channel dopants only is 7 times reduced. Therefore, in the following work, we focus on the channel dopant induced fluctuation to compromise the simulation accuracy

Table 4.2: Threshold voltage of the studied devices with nominal continuous channel doping

Technology node (nm)	Nominal V_{th} (V)	Maximum V_{th} (V)	Minimum V_{th} (V)
30	0.226	0.268	0.211
22	0.192	0.225	0.168
16	0.139	0.195	0.125

and speed. Notably, since the effect of source/drain and channel dopants are independent, according to the statistic theory the overall σV_{th} induced by source/drain and channel dopants are about 30.2 mV ($\simeq$ (10.5)$^{0.5}$ + (28.3)$^{0.5}$), which is similar to the result of fully discrete scheme. Therefore, the simulation approach is mathematically verified.

The maximum differences in V_{th} induced by the discrete-dopant-position effect for 30-, 22-, and 16-nm-gate-lengths are then normalized with respect to their nominal V_{th}, as plotted in Fig. 4.2. The result shows a significant increase of discrete-dopant-induced V_{th} fluctuation in nanoscale transistors. The results for the studied devices with the same doping concentration of 1.48$\times$10^{18} cm^{-3} are summarized in Table 4.2. Figure 4.3 shows the fluctuations of V_{th} for the 30-, 22- , and 16-nm-gate bulk FinFETs. All V_{th}'s of the studied devices are normalized by their corresponding nominal V_{th}. As bulk FinFETs shrink in size, the V_{th} scales with an increasing fluctuation of V_{th}. In addition to the fluctuation of V_{th}, the fluctuation of current is significant. Figure 4.4 shows the I_{on}-I_{off} characteristic

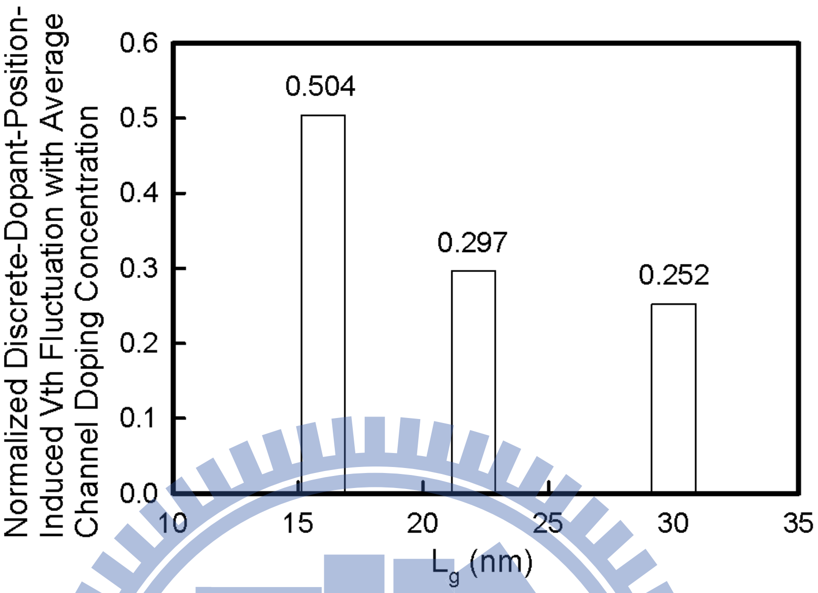


Figure 4.2: For cases with 1.48×10^{18} cm^{-3} average channel doping concentration, the maximum differences in threshold voltage induced by discrete-dopant-position effect for 30-, 22-, and 16-nm-gate-lengths, which are normalized by the corresponding nominal threshold voltage.

fluctuations. For cases with similar I_{on}, the maximum fluctuation of I_{off} increases significantly as the gate length is scaled down. The plot of V_{th} roll-off and fluctuation of V_{th} against the gate length of bulk-FinFETs is shown in Fig. 4.5. The V_{th} fluctuation of the 22- and 16-nm-gate bulk FinFETs are 1.28 and 1.61 times larger than that of the 30-nm-gate device. Fluctuation of V_{th} for bulk FinFETs and planar MOSFETs are presented in Fig. 4.6. For the gate length of 16 nm, the V_{th} fluctuation of FinFETs is only half that of

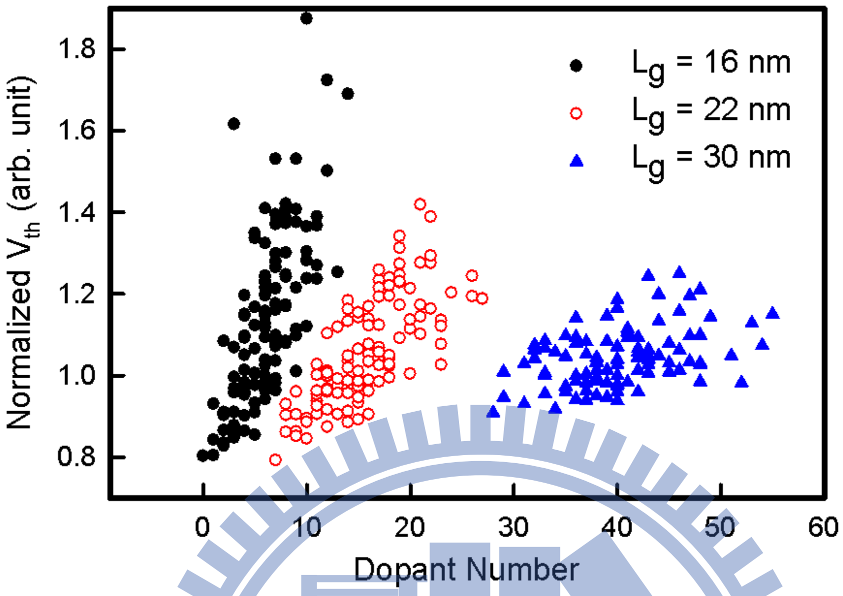


Figure 4.3: Fluctuations of threshold voltage for the 30-, 22- , and 16-nm-gate bulk FinFETs. The threshold voltages of the studied devices are normalized by the corresponding nominal threshold voltage.

planar MOSFETs. Moreover, as gate length is reduced from 30 nm to 16 nm, the fluctuation of V_{th} is increased by 11 mV, which is better than the increase in the case of planar MOSFETs, 27.3 mV. With varying variations of W and L, the fluctuation of V_{th}, follows

$$\sigma_{v_{th}} \approx (WL)^{-\gamma}, \tag{4.1}$$

where γ is 0.5 for the planar MOSFETs [21-22,76]. The dependence factor of threshold voltage, $(WL)^{-\gamma}$, is then plotted as a function of γ, as shown in Fig. 4.7(a). As γ decreases, the difference between 60 nm and 16 nm decreases. The difference is greater than one

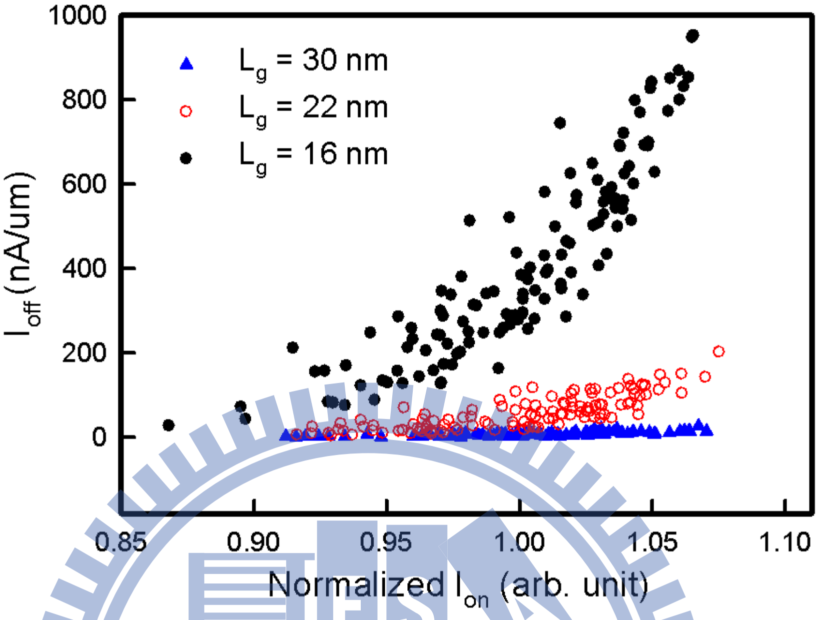


Figure 4.4: On-off state current characteristics of the 30-, 22- , and 16-nm-gate bulk FinFET devices.

order for γ = 1 and less than one order for γ = 0.5. The dependence on device dimension is eliminated at γ = 0, which means that the V_{th} fluctuation will be constant regardless of the size of the device. Assume the fluctuation of V_{th} for the 60-nm-gate device to be 1 mV. Figure 4.7(b) shows the increase in V_{th} fluctuation as the device becomes smaller. The fluctuation of V_{th} decreases as γ decreases. According to this relationship and the aforementioned results, the γ factor of the bulk FinFETs on device dimension is then fitted to be 0.25. For the device with 16 nm gate length, the fluctuation of device with γ = 0.5, as shown in Fig. 4.7(b), is about two times larger than that of γ = 0.25, which is similar to the

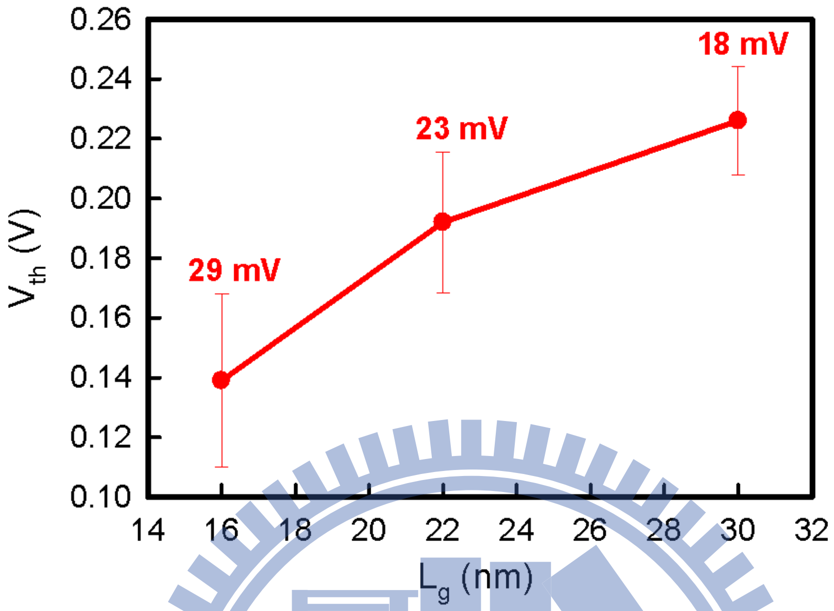


Figure 4.5: Plot of threshold voltage roll-off for the 30-, 22- , and 16-nm-gate bulk FinFETs, where the bars indicate the fluctuation of threshold voltage.

results in Fig. 4.6.

Figure 4.8(a) shows the large-scale statistically computed results of I_D as a function of V_G for the bulk FinFET device with L_g of 16 nm, where the red solid line presents the nominal case (continuous doping profile: 1.48×10^{18} cm^{-3}) and the dotted lines show the discrete dopant fluctuated cases. The spread of the I_D-V_G curves indicates the magnitude of the effect of discrete dopants. The characteristics of fluctuation are further explored with respect to the I_{on}, I_{off}, and V_{th}, as shown in Figs. 4.8(b), 4.8c), and 4.8(d), respectively.

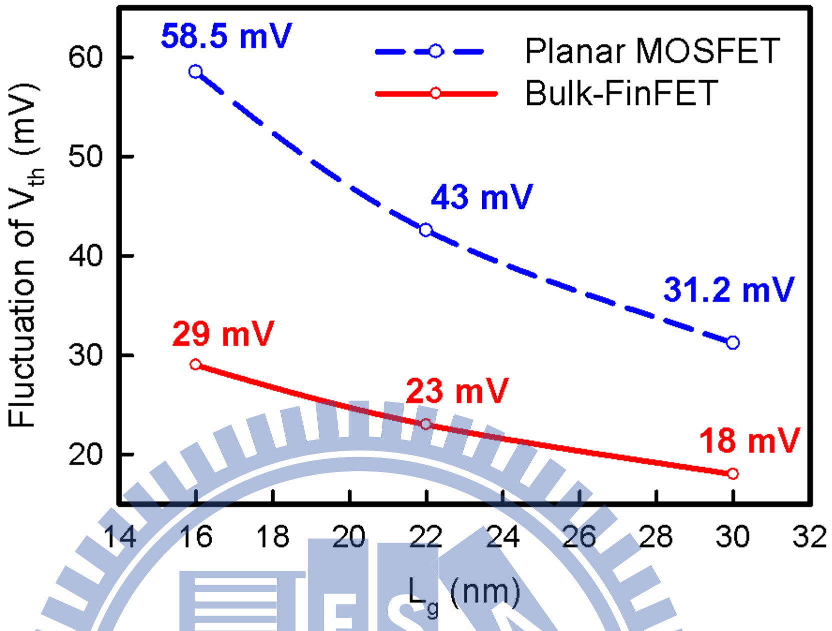
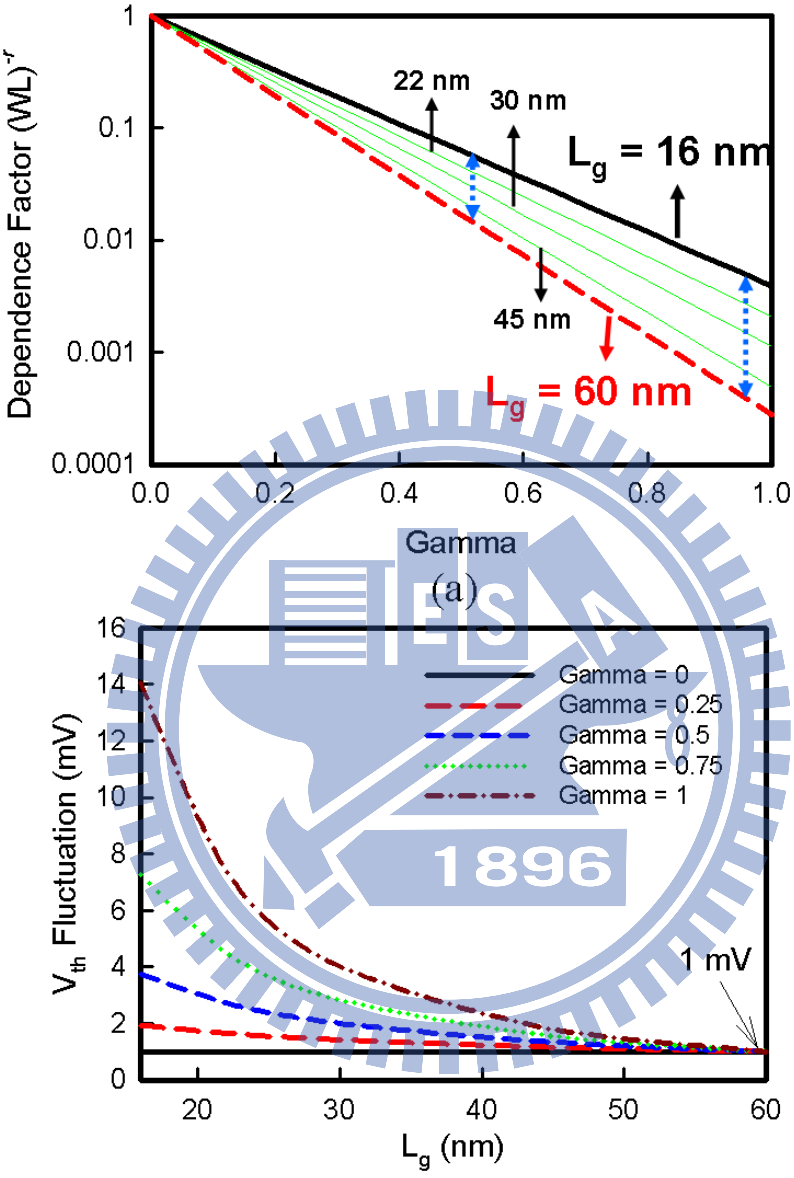


Figure 4.6: Fluctuations of threshold voltage roll-off (i.e., versus the L_g) of bulk FinFETs and planar MOSFETs.

From the random-dopant-number point of view, the equivalent channel doping concentration increases as the dopant number increases; this substantially alters the V_{th}, I_{on} and I_{off}. Moreover, it is observed that even for devices with the same numbers of dopants inside the channel, the effect of random dopant position induces different fluctuations of characteristics in spite of there being the same number of dopants. Furthermore, the magnitude of the spread characteristics increases as the number of dopants increases. To explore the random-dopant-position-induced V_{th} fluctuation, the on-state potential distributions of the



(a)

(b)

Figure 4.7: Threshold voltage fluctuation as a function of device dimension. (a) Plots of dependence factor on γ for various device dimensions. (b) Fluctuation of threshold voltage for the 60-nm-gate device was assumed to be 1 mV.

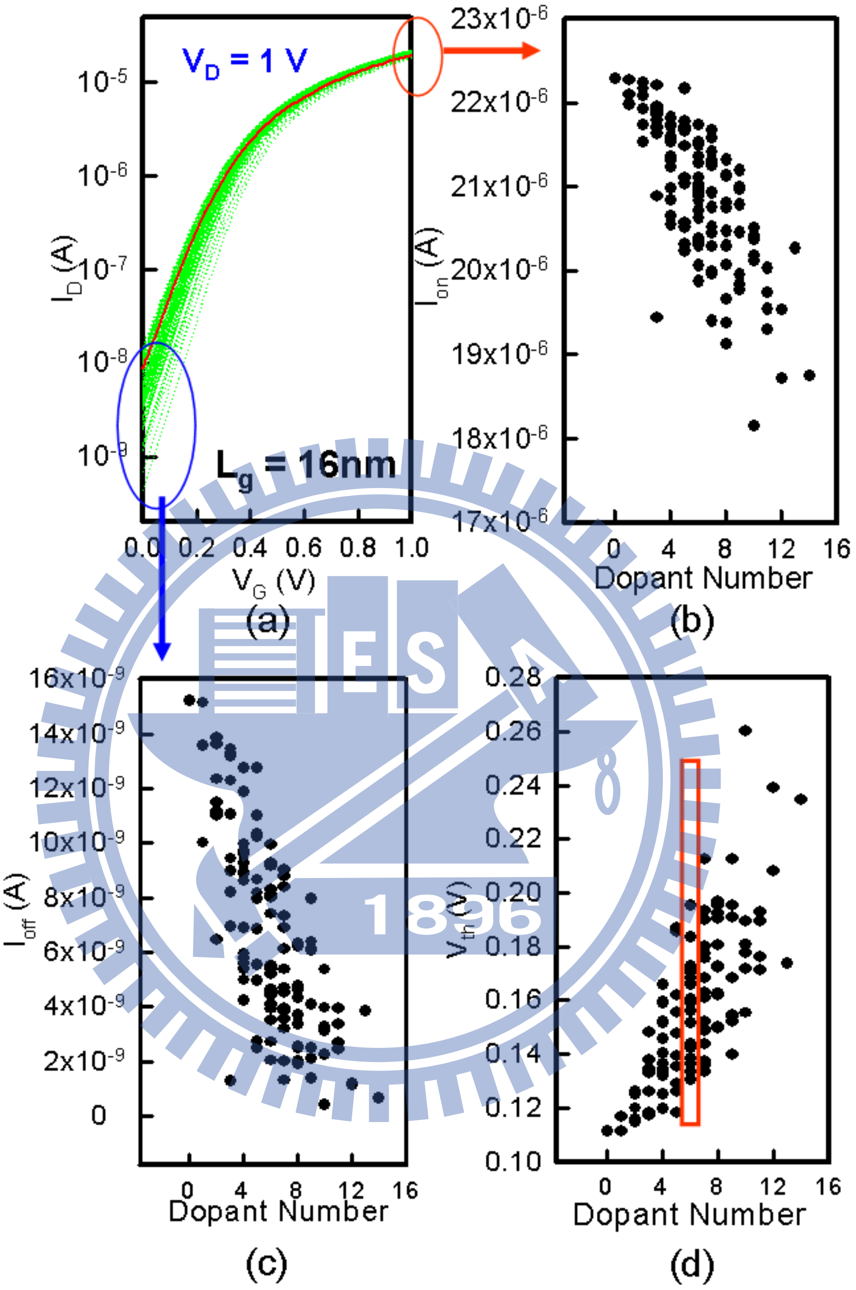


Figure 4.8: (a) The characteristics of I_D-V_G, where the solid line indicates the continuous (i.e., the nominal) case. The fluctuations of (b) on-state current, (c) off-state current and (c) threshold voltage as a function of the number of dopants.

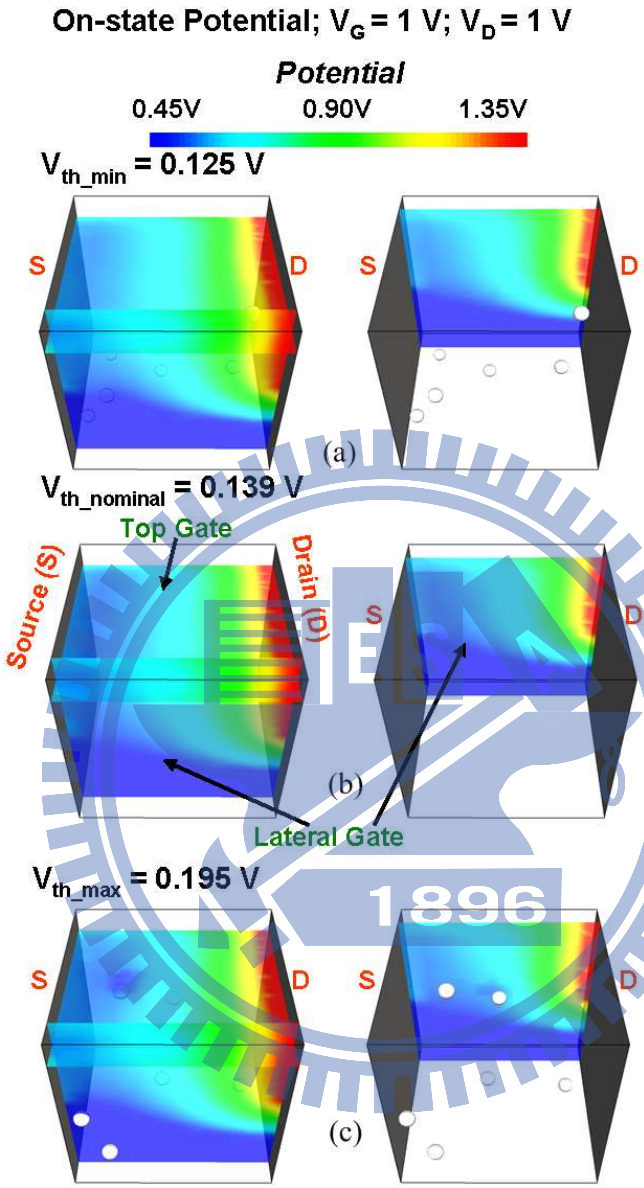


Figure 4.9: The on-state potential distributions of the 16-nm-gate bulk FinFETs with six discrete dopants inside the channel (average concentration: 1.48×10^{18} cm^{-3}), and the nominal case. The potential distributions are 2 nm below the top and lateral gates. The potential distributions for the device with (a) minimal threshold voltage (b) nominal threshold voltage and (c) maximal threshold voltage.

16-nm-gate bulk FinFETs with six discrete dopants inside the channel (average concentration: 1.48×10^{18} cm^{-3}), as shown by the rectangle in Fig. 4.8(d), and the nominal case (continuous doping profile: 1.48×10^{18} cm^{-3}) are investigated and shown in Fig. 4.9, where the potential distributions are 2 nm below the top and lateral gates. We note that the V_{th} is determined from the current criterion that I_D = 1.0×10^{-7}(W/L) A. Because of the lack of discrete dopants located near the channel surface, the device with minimal V_{th}, as shown in Fig. 4.9(a), exhibits a larger potential distribution than that in the nominal case, as shown in Fig. 4.9(b). On the other hand, in a device with maximal V_{th}, as shown in Fig. 4.9(c), there are four dopants located near the surface of the channel. The corresponding potential distributions near these dopants are significant decreased, which significantly changes the electron conducting path. The random dopant position induces rather different fluctuations of characteristics in spite of there being the same number of dopants.

Figure 4.10(a) shows the characteristics of I_{on}-I_{off}. For cases with similar I_{on}, the maximum fluctuation of I_{off} is within 5 times. For a 16-nm-gate conventional planar MOSFETs, our calculation finds that the fluctuation of I_{off} is 10 times larger than that of bulk FinFET. Figures 4.10(b)- 4.10(d), 4.10(b')- 4.10(d') and 4.10(b")- 4.10(d") disclose three different discrete-dopant channels, having very similar values of I_{on} or I_{off} but with various dopant positions. The cross-sectional (both the top- and lateral-view) on-state current density and off-state electrostatic potential at 1 nm and 5 nm below the gate

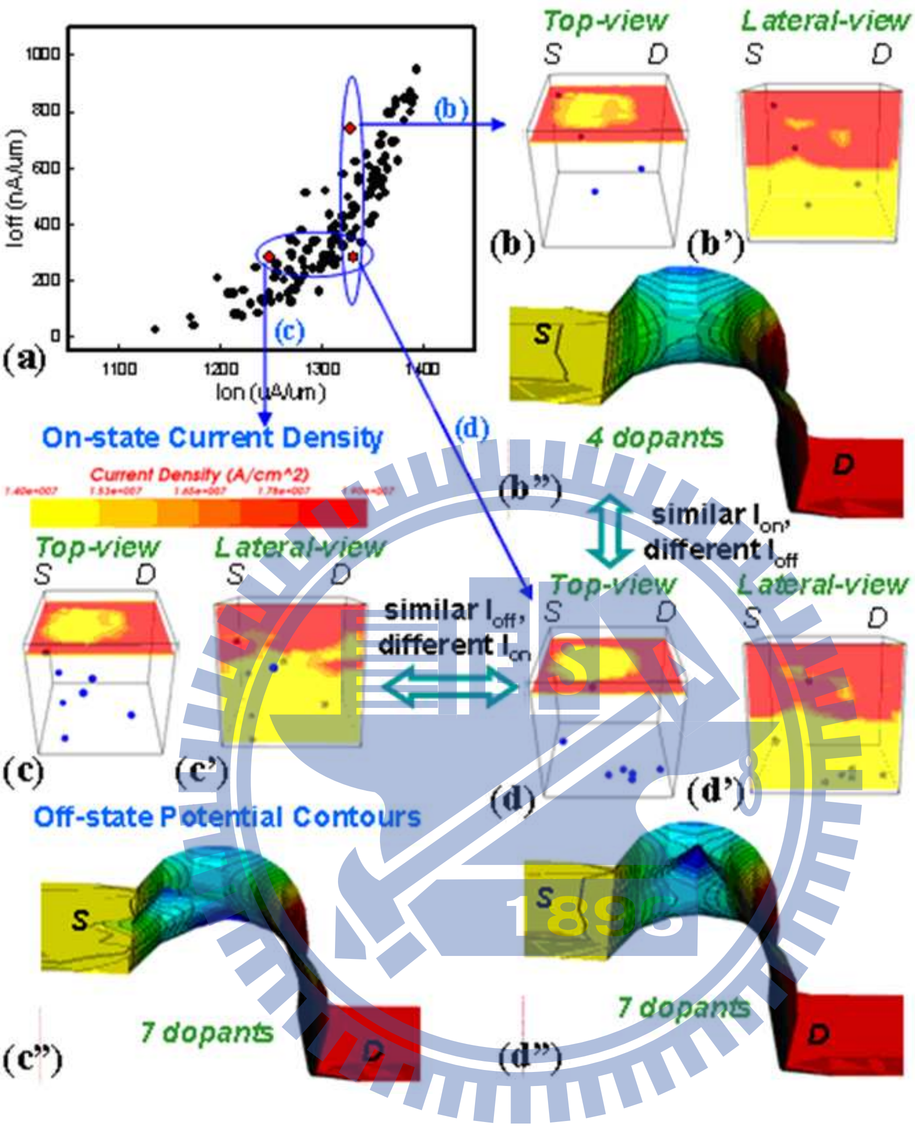


Figure 4.10: (a) The characteristics of I_{on}-I_{off} of the 125 discrete-dopant 16-nm-gate bulk FinFETs. Three cases are selected to evaluate similar I_{on} but different I_{off} (plots of (b) and (c)) and similar I_{off} but different I_{on} (plots of (c) and (d). Plots of (b)-(d) and (b')-(d') show the corresponding top and lateral views of the on-state current density, which are extracted at the 1 nm below the gate oxide, respectively. Plots of (b")-(d") show the off-state potential contours.

oxide are examined. Figures 4.10(b)- 4.10(d) and 4.10(b')- 4.10(d') show the top and lateral views of the distribution of the on-state current. For the top-gate, the three different cases of the dopant, shown in Figs. 4.10(b)- 4.10(d), imply that bulk FinFET has very similar conducting-current paths. However, the lateral-view plots, shown in Figs. 4.10(b')- 4.10(d'), exhibit different current distribution due to an impurity appearing on the surface of the lateral-gate, as shown in Fig. 4.10(c'). The different conducting paths that locate at the lateral-gate result in different on-state currents even we have very similar off-state currents, shown in Fig. 4.10(a). For the device having very similar on-state (or off-state) current with different off-state (or on-state) situations, Figs. 4.10(b")- 4.10(d") are plots of the off-state potential distribution at the 5 nm below gate oxide. As shown in Fig. 4.10(a), the device possesses very similar on-state current (the vertical ellipse circled), but with different off-state current ($>$ 3 times) resulting from the different randomness of the dopant number and position, shown in Figs. 4.10(b") and 4.10(d"). Furthermore, the magnitude of the spread characteristics increases as the number of dopants increases.

4.1.2 Comparison with Planar MOSFETs with High-κ Dielectrics

Gate oxide scaling has become as the key in scaling silicon CMOS technology. The metal gate and high-κ dielectric are very attractive to maintain low gate leakage and control short channel effects [27,63]. This subsection discusses and compares the dependency of process-variation-effect and random-dopant-induced V_{th} fluctuation on 16-nm-gate planar MOSFETs and bulk FinFETs. The threshold voltage fluctuation for the planar MOSFETs with equivalent oxide thicknesses from 1.2 nm to 0.2 nm (e.g., SiO_2 for the 1.2 and 0.8 nm EOTs, Al_2O_3 for the 0.4 nm EOT and HfO_2 for the 0.2 nm EOT) are compared with the results of bulk FinFETs.

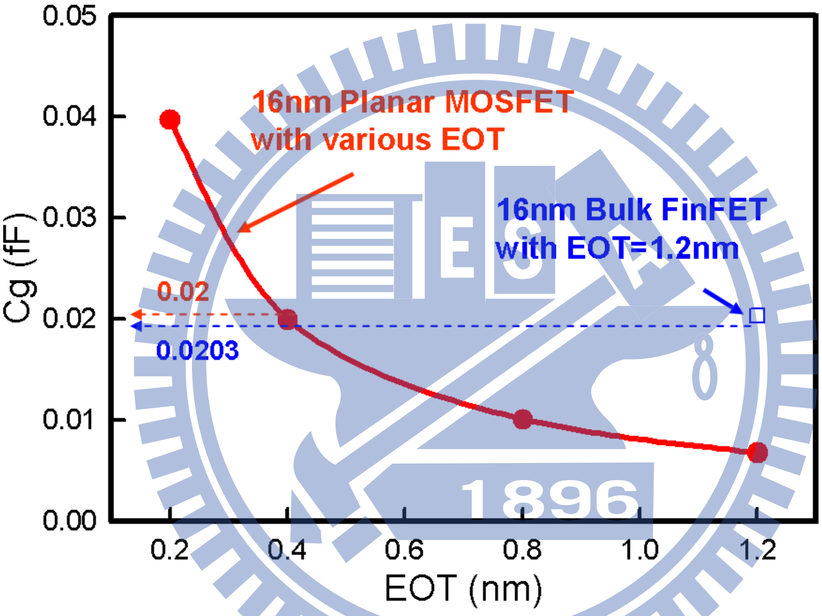


Figure 4.11: The gate capacitance as a function of the EOT, where the solid line shows the planar MOSFETs with various EOT and the square symbol indicates the bulk FinFET device with 1.2 nm EOT.

Gate capacitance is one of the most important indexes for channel controllability. Figure 4.11 plots the gate capacitance as a function of the EOT, where the solid line shows

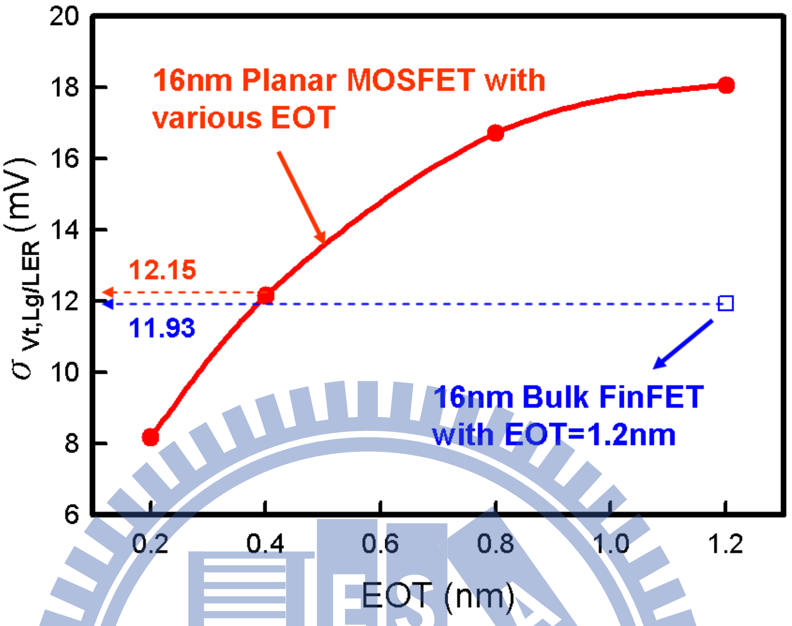
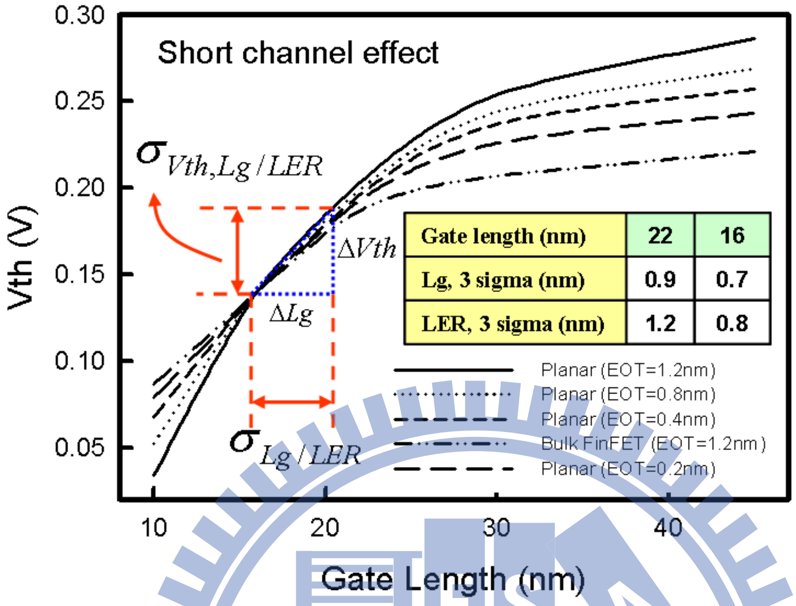


Figure 4.12: The process-variation-induced threshold voltage fluctuation for the studied devices.

the planar MOSFETs with various EOT and the square symbol indicates the bulk FinFET device with 1.2-nm EOT. The planar MOSFET with 0.4-nm EOT, where Al_2O_3 is used for gate dielectric, exhibits a similar gate capacitance with the bulk FinFET device with 1.2-nm EOT because the gate size of the explore bulk FinFETs is about three times larger than the planar MOSFETs. Since the process variation is resulted from the enhancement of the short channel effect, the bulk FinFETs with 1.2-nm EOT is expected to have similar immunity against process-variation induced fluctuation with the planar MOSFETs with 0.4-nm EOT. The $\sigma V_{th,Lg/LER}$ of the planar MOSFETs and bulk FinFETs presented in Fig. 4.12



Gate length (nm)	22	16
Lg, 3 sigma (nm)	0.9	0.7
LER, 3 sigma (nm)	1.2	0.8

Figure 4.13: The threshold voltage roll-off of the studied devices, where the variation follows the projection of ITRS 2005 roadmap. These results are used to estimate the V_{th} fluctuation resulting from the gate-length deviation and the line-edge roughness.

confirmed this viewpoint, in which the V_{th} roll-off characteristics in Figure 4.13 are used for the $\sigma V_{th,Lg/LER}$ estimation. The bulk FinFET device with 1.2 nm EOT exhibits a similar immunity against process-variation-induced fluctuation with the planar MOSFET with 0.4-nm EOT. However, the trend still is not valid in the random-dopant-induced fluctuation.

Figure 4.14 shows the random-dopant-induced V_{th} fluctuation, $\sigma V_{th,RD}$, of the studied devices. The $\sigma V_{th,RD}$ decreases significantly as the EOT is scaled down. However, the

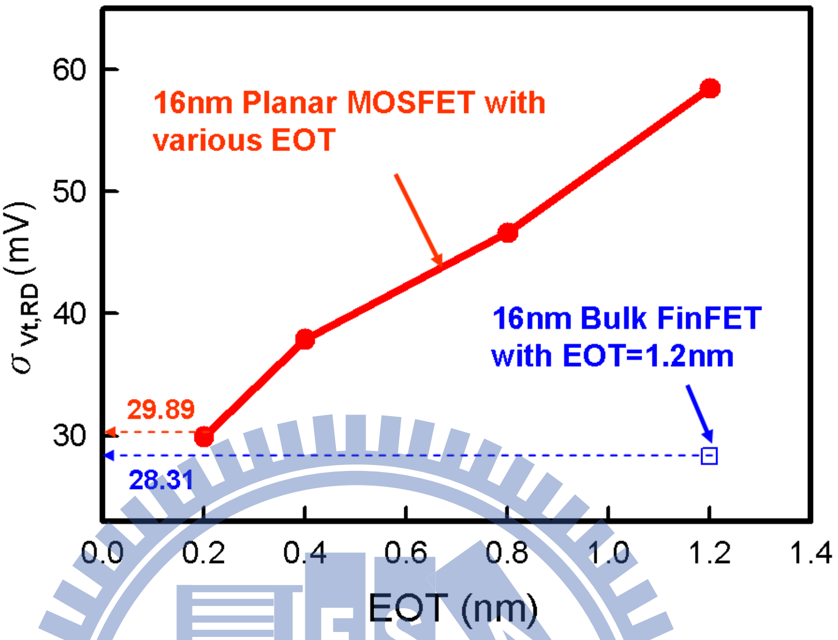


Figure 4.14: The random-dopant-induced threshold voltage fluctuation for the studied devices.

expectation between gate capacitance and $\sigma V_{th,RD}$ is invalid. The $\sigma V_{th,RD}$ of bulk FinFETs approximates the planar MOSFETs with 0.2-nm EOT. To further investigate the mechanism of bulk FinFETs in fluctuation suppression, the potential distributions (V_G = 1 V V_D = 0 V) extracted 1 nm below the top gate of channel are examined. Figure 4.15(a) shows the dopant distribution and Figs. 4.15(b) - 4.15(f) are the explored devices with various EOT. The potential barriers are induced by the corresponding dopants at positions: A, B, and C, respectively, as shown in Fig. 4.15(a). The potential barrier is largest at C because two discrete dopants are located close to each other there. For planar MOSFETs with various

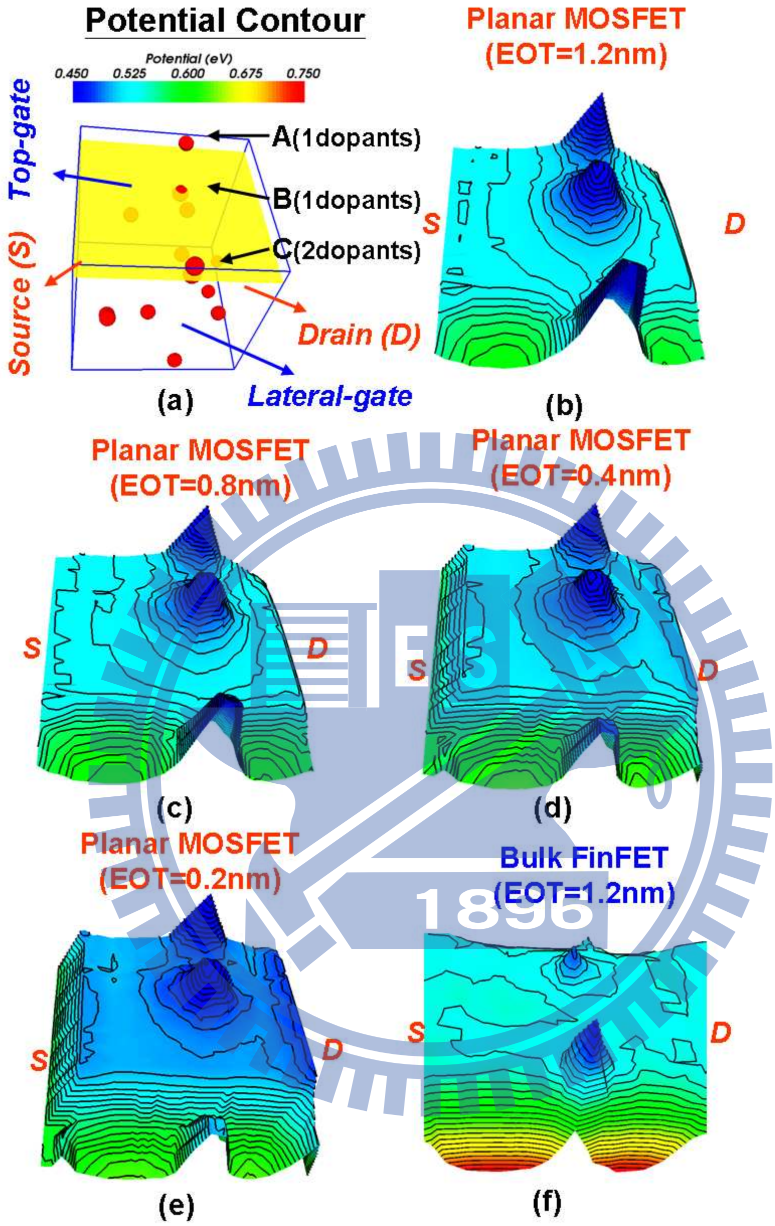


Figure 4.15: Top-gate potential contours of the planar MOSFETs with various EOT ((b) EOT = 1.2 nm, (c) EOT = 0.8 nm, (d) EOT = 0.4 nm, (e) EOT = 0.2 nm) and (f) bulk FinFETs with 1.2 nm EOT. The distributions of potential barriers are induced by the corresponding dopants location (i.e., A, B and C). The corresponding distribution of discrete dopants is shown in (a) and all the plots are extracted 1 nm below the gate oxide.

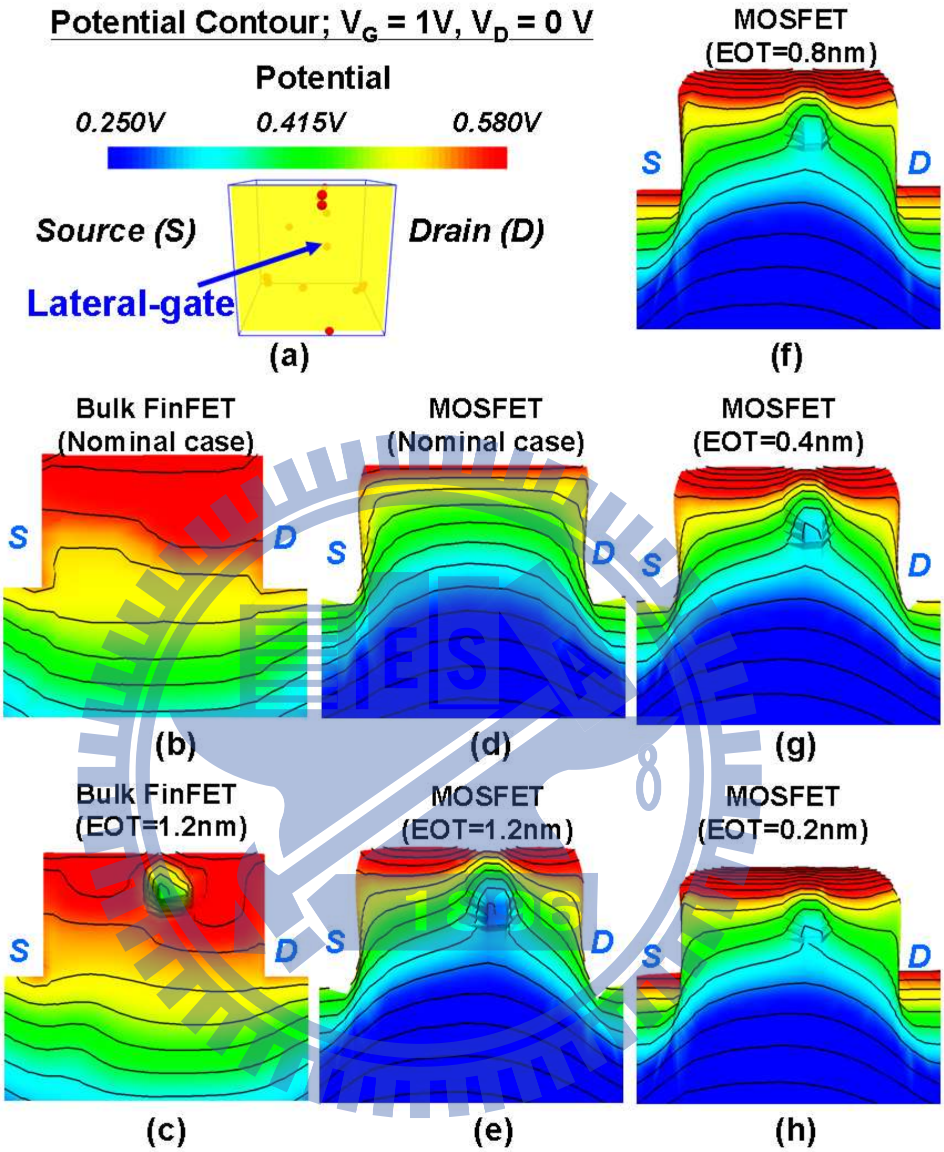


Figure 4.16: Lateral-gate off-state potential contours for the studied planar MOSFET and bulk FinFET devices, where (b) and (c) show the nominal (continuously doped) and discrete dopant fluctuated cases of bulk FinFETs. The nominal and discrete dopant fluctuated cases of planar MOSFETs with different EOTs are shown in (d)-(h).

EOTs, the sizes of the potential barriers are suppressed as the equivalent gate oxide thickness is reduced. The results for planar MOSFETs, as displayed in Figs. 4.15(b) - 4.15(e) are then compared with that of a bulk FinFET device, as shown in Fig. 4.15(f), indicating that the potential barriers of bulk FinFET are smaller than those of planar MOSFETs, especially at position A. The potential barrier induced by corresponding dopant in A is significantly reduced in bulk FinFET device because of the strong electric field around the corner to suppress the potential barrier induced by dopants. The strengthen electric field is owing to the changed gate structure, which causes the different suppression mechanisms between the planar MOSFETs and bulk FinFETs. Figure 4.16 shows the lateral side potential distributions of the studied devices, in which Fig. 4.16(a) plots the dopant distribution. Figures 4.16(b) and 4.16(c) show the potential contours of the nominal (continuous channel doping concentration: 1.48×10^{18} cm^{-3})) and discrete dopant fluctuated cases of bulk FinFETs with 1.2 nm EOT. Figures 78(d)-78(h) show the nominal and discrete dopant fluctuated cases of planar MOSFETs with EOT scaling. The potential fluctuation is mitigated as the equivalent gate oxide thickness is scaled down, as shown in Figs. 4.16(f) - 4.16(h). For the discrete-dopant-fluctuated bulk FinFET device in Fig. 4.16(c), although the potential distribution is disturbed by a dopant that is located on lateral side of the channel, the overall potential distribution in the case of fluctuation is still quite similar to that in the nominal case. However, for MOSFETs in Fig. 4.16(e), due to the lack of lateral gate structure, the potential fluctuation is still significant. This result reconfirms the effect of the lateral gate in bulk FinFET devices in suppressing potential fluctuations.

Figure 4.17 plots the top and lateral views of the on-state current density (V_G = 1V; V_D = 1V) of planar and bulk FinFET devices with 1.2 nm EOT. All cross-sectional plots are from 1 nm below the top and lateral side of channel surface. The top views of the channel, as presented in Figs. 4.17(b) and 4.17(e), reveal that bulk FinFET device provides a larger and more uniform current distribution than the planar MOSFET due to the smaller fluctuation of potential. The lateral views of channel, Figs. 4.17(c) and 4.17(d), show that the current conducting paths of planar MOSFETs are easily disturbed by discrete dopants. However, in the bulk FinFETs, Figs. 4.17(f) and 4.17(g), even current conducting paths are retarded in parts of channel surface; the tri-gate structure of bulk FinFETs provides more alternative conducting paths that prevent a significant fluctuation of conduction current. Thus, benefiting from the superiority of the vertical channel structure, the bulk FinFET device suppresses potential fluctuations and maintains a more stable conduction current than the planar MOSFET. Figure 4.18 plots the on-/off- state current characteristics of the studied devices. For devices with similar on-state current, the maximum difference of off-state current is declined from approximately 2000 nA/um to 800 nA/um as the EOT is scaled from 1.2 nm to 0.2 nm. Comparing the results for planar MOSFETs with those of

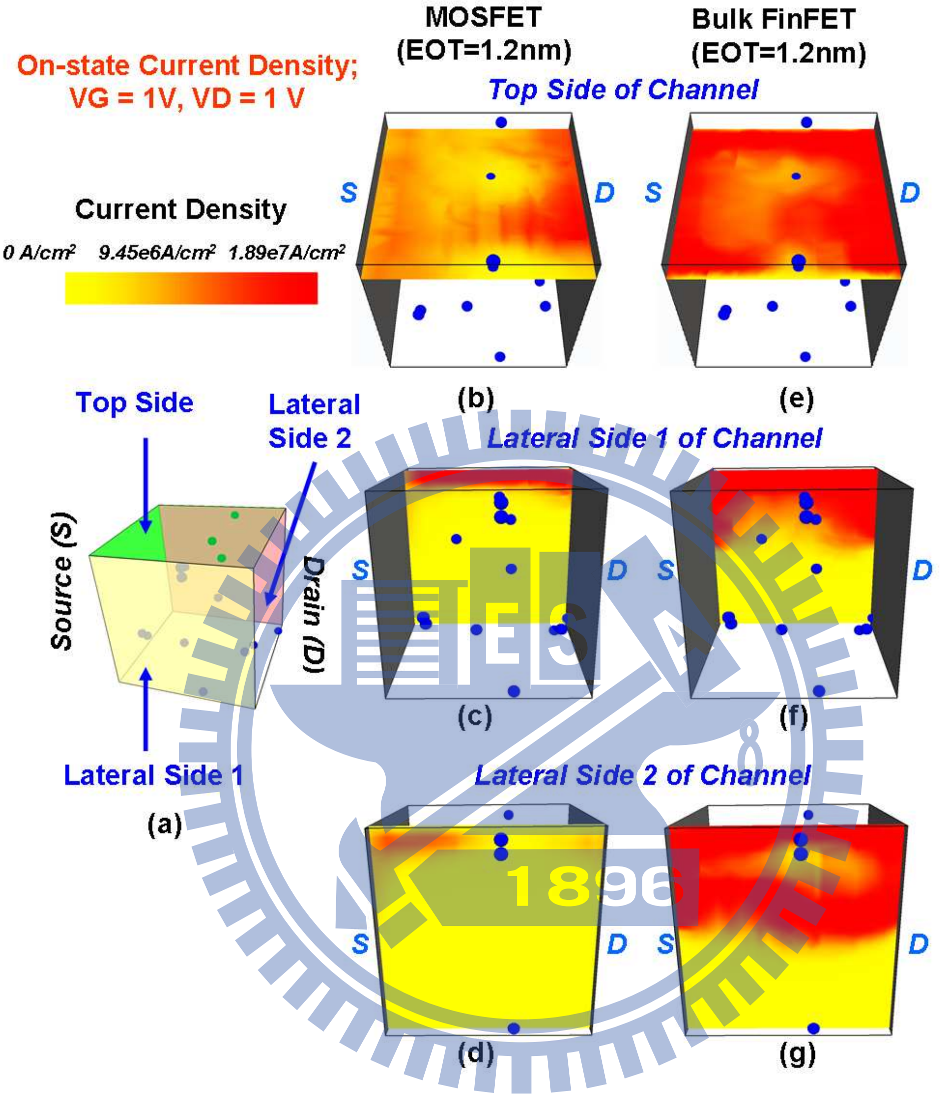


Figure 4.17: Cross-sectional views of on-state current density distribution in channel of device, where (b), (c), and (d) show the planar MOSFET device and (e), (f), and (g) show the bulk FinFET device. The corresponding distribution of discrete dopants is shown in (a) and all the cross-section plots are extracted 1 nm below the channel surface.

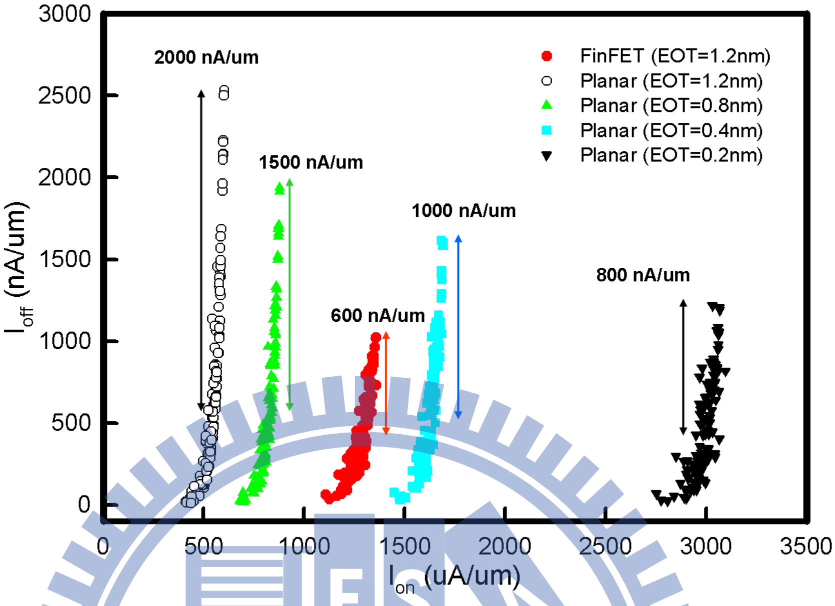


Figure 4.18: I_{on}-I_{off} current characteristics of the studied 16-nm-gate planar MOSFET and bulk FinFET devices.

bulk FinFETs, even though the planar device with 0.4-nm and 0.2-nm EOTs has a better on-off state characteristic, the bulk FinFET device exhibits a smaller current fluctuation (about 600 nA/um). The bulk FinFET device can provide a more uniform potential distribution and a more stable current flow than that of the planar MOSFET. The additional structural improvement of bulk FinFET devices enhances the immunity of device against random-dopant-induced fluctuation, which cannot be evaluated from the trend of gate capacitance. The process-variation-effect and random-dopant-fluctuation induced V_{th} fluctuations are summarized in Table 4.3 and Figs. 4.19. The random dopant effect is the dominating factor

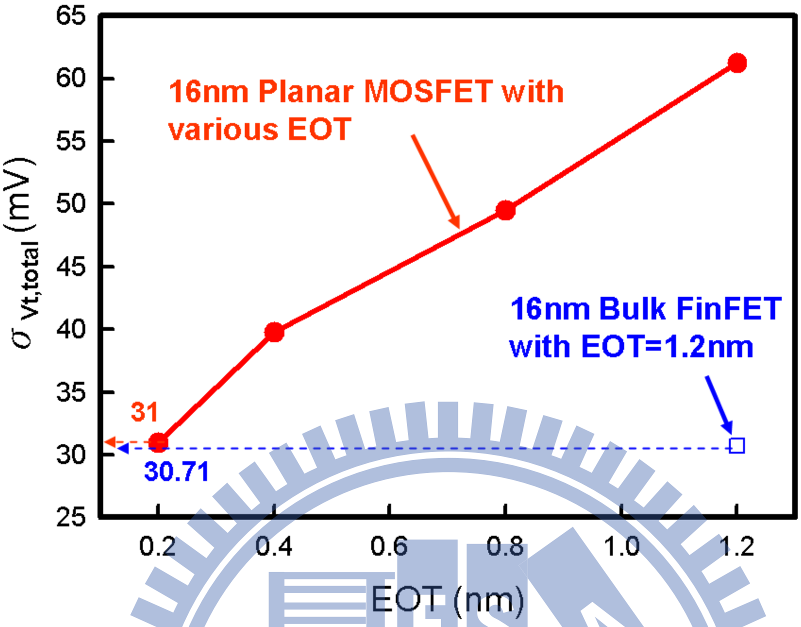


Figure 4.19: Total threshold voltage fluctuation for the studied devices.

in this scenario. The planar MOSFETs with 0.2-nm EOT and the bulk FinFETs possess the best fluctuation immunity. The V_{th} fluctuations are suppressed with the gate oxide thickness scaling. However, the immunity of the planar MOSFETs suffers from nature of structural limitations and the use of vertical channel transistors can alleviate this problem.

Table 4.3: Summary of the threshold voltage fluctuation of the explored planar MOSFETs and bulk FinFETs.

	Planar MOSFETs	Planar MOSFETs	Planar MOSFETs	Planar MOSFETs	Bulk FinFETs
EOT (nm)	1.2	0.8	0.4	0.2	1.2
$V_{th,L_g/LER}$	18.1	16.7	12.2	8.18	12.6
$V_{th,RD}$	58.5	46.6	37.9	29.9	28.3
$V_{th,total}$	61.2	49.5	39.8	31.0	30.7

4.2 Silicon-on-Insulator Transistors

This subsection initially discusses the physical fluctuations that are induced by discrete dopants, and then the characteristic fluctuations and mechanism of immunity against fluctuations of multiple-gate SOI devices are studied. The dopant generation and simulation has been presented in previous chapters. Figure 4.20 displays the explored 16-nm-gate single-, double-, triple- and surrounding-gate SOI devices. Discrete-dopant-induced fluctuations, caused by local potential spikes, are determined by the corresponding dopants within the device channel. The potential spike alters not only the electric field and current conducting path, but also the electron velocity, carrier mobility and electron temperature distribution.

Figure 4.21 depicts for example discrete-dopant-induced fluctuations of a triple-gate

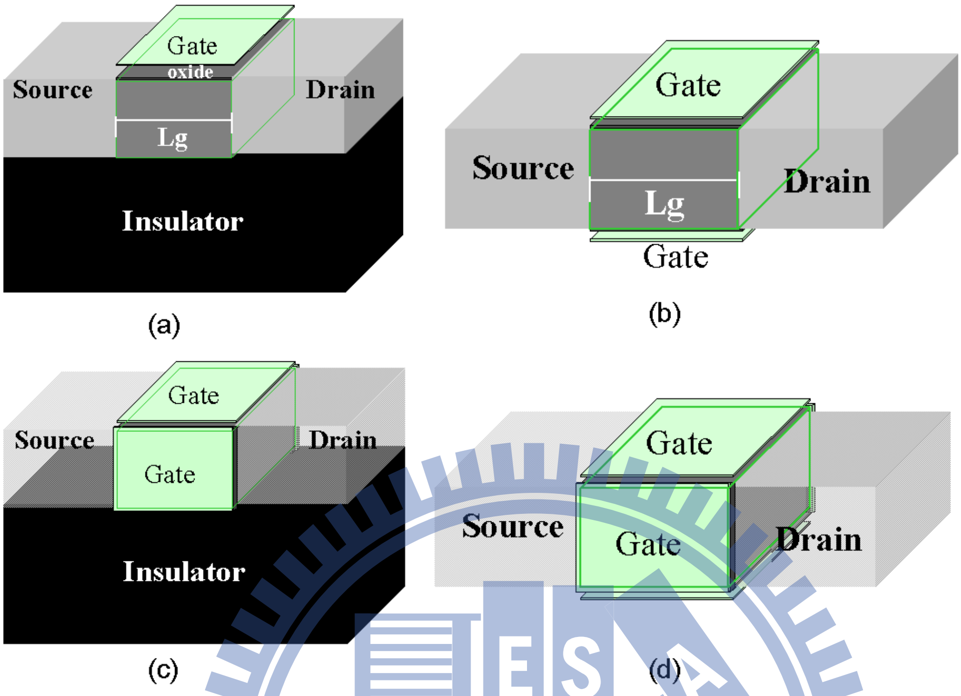


Figure 4.20: The (a) single-gate; (b) double-gate; (c) triple-gate; and (d) quadruple surrounding-gate for the dopant position/number-sensitive device simulation.

SOI transistor. All cross-sectional plots of the distributions of the on-state current density and the contours of the off-state potential are extracted 1nm below the top-gate oxide. Figures 41(a) and 4.21(a') refer to the nominal case (continuous doping is assumed) and the discretely doped case, respectively. The on-state potential contour and current density distribution of the discretely doped case, shown in Figs. 4.21(b'), and 4.21(c'), are investigated to elucidate the effect of discrete dopant on the potential and current distribution of the device. The potential spikes in Fig. 4.21(b') are associated with the corresponding

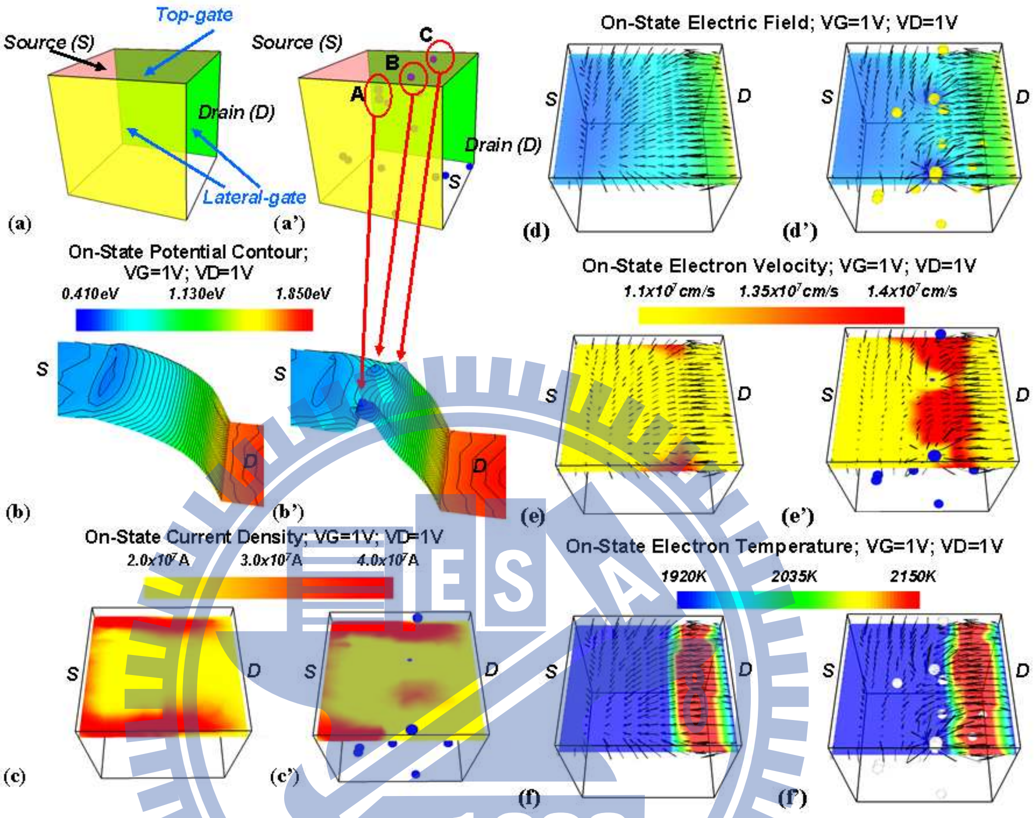


Figure 4.21: Comparison of the on-state potential contours ((b) and (b')), the current density distributions ((c) and (c')), the electric field ((d) and (d')), the electron velocity ((e) and (e')), and the electron temperature ((f) and (f')) of the (a) the nominal case and (a') discretely doped cases. The potential spikes (marked as A, B, and C) in (b') are induced by corresponding dopants in (a')). All cross-sectional plots of the on-state current density distributions and off-state potential contours are extracted at 1 nm below the top-gate oxide.

dopants (spikes A, B and C) in Fig. 4.21(a'). The potential distribution near spike C does not vary significantly with structure of the triple-gate. Comparison of Figs. 4.21(c) and 4.21(c') reveals that the current conducting path is disturbed and impeded by dopants in the channel. Changing the number and position of discrete dopants in the channel causes a significant potential variation and change in current. The current may avoid the high potential barrier region and pass through the valley between two potential spikes (such as spikes A and B). Additionally, the local field distribution, shown in Fig. 4.21(d'), is also perturbed significantly by discrete dopants. In the on-state condition (the gate voltage V_G = 1V; the drain voltage V_D = 1V), since the potential distribution near the dopant is relatively negative in the channel, the dopant acts as a center of a whirlpool-like electric field to repel electrons. As electrons drift from source to drain, some of them encounter a negative electric field that is induced by the dopant. The lateral electric field between the source and the drain, combined with the repulsion of the dopants, twists the electron field and increases the electron velocity near the dopant, as shown in Figs. 4.21(e), and 4.21(e'). This phenomenon explains why the distribution of the electron velocity remains the same to the left of the dopants at device's source. The fluctuation in the electron velocity also indicates a fluctuation of the distribution of electron temperatures, as plotted in Figs. 4.21(f) and 4.21(f').

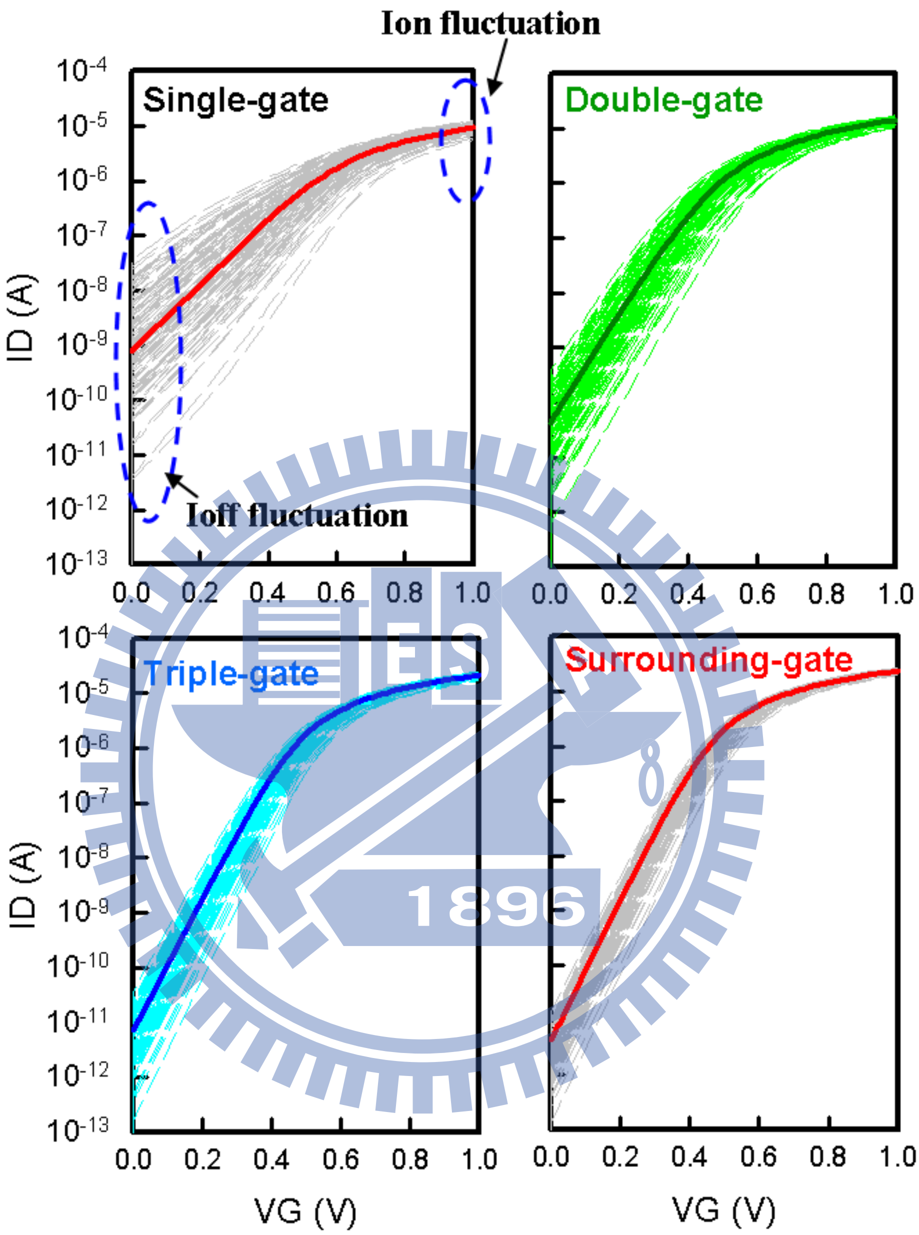


Figure 4.22: The I_D-V_G characteristics of the 500 discrete-dopant-fluctuated 16-nm-gate single- and multiple-gate SOI devices, where the solid lines indicate the nominal case and the dash lines indicate the discretely doped cases.

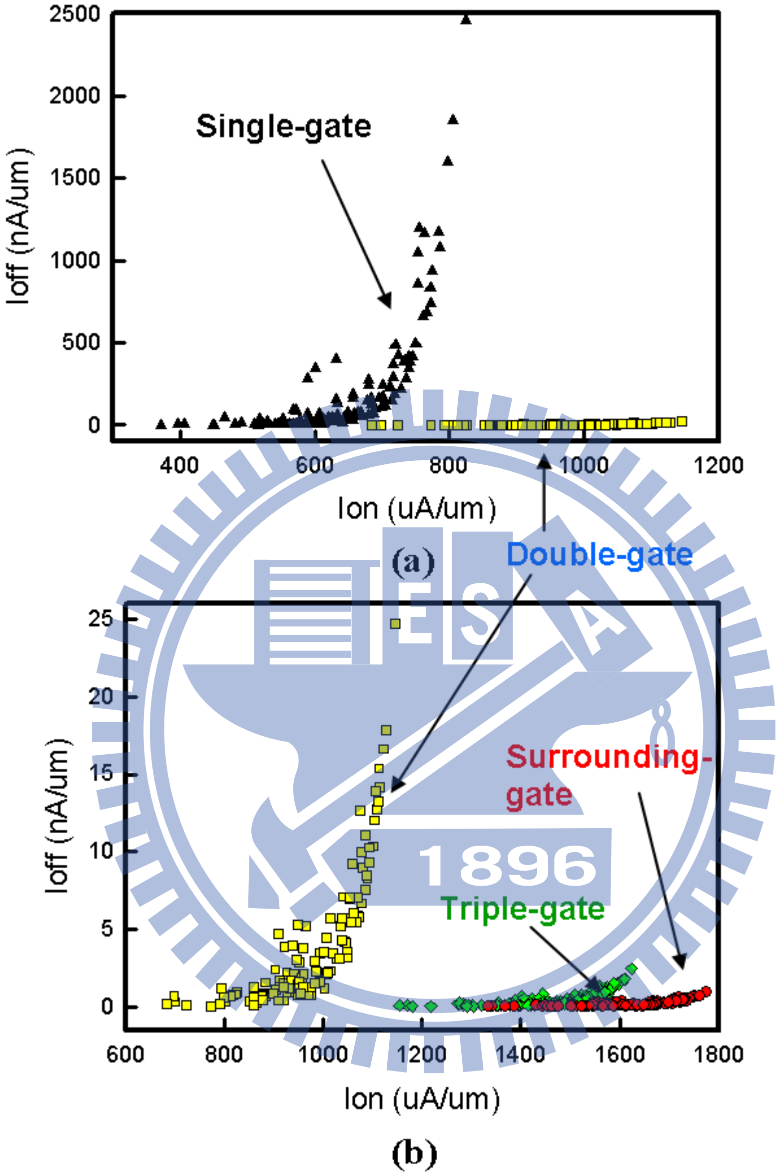
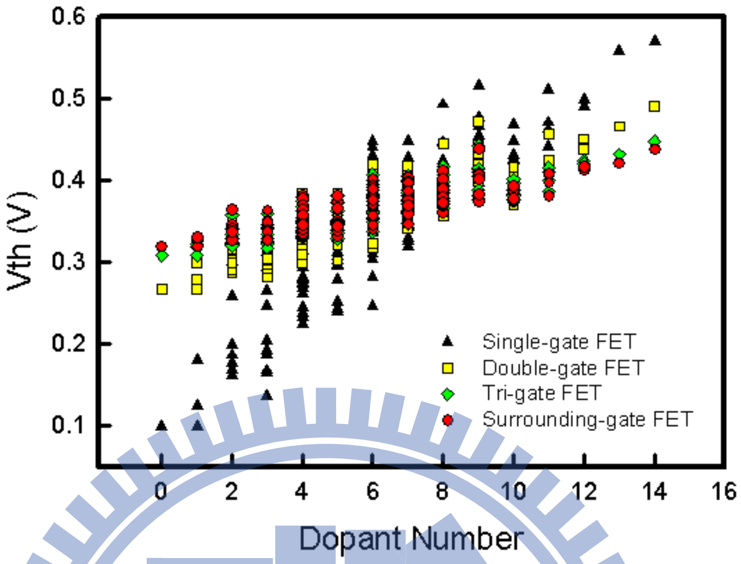
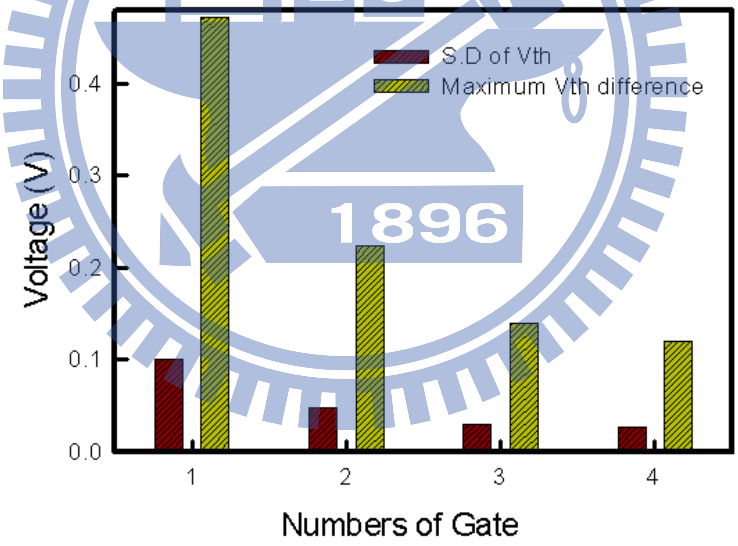


Figure 4.23: The on-off state current characteristics of the 500 discrete-dopant-fluctuated 16-nm-gate single- and multiple-gate SOI devices. (a) Comparison between the single- and double-gate devices. (b) Comparison among the double-, triple-, and quadruple surrounding-gate devices.



(a)



(b)

Figure 4.24: (a) Comparison of V_{th} fluctuation of the 16-nm-gate single- and multiple-gate SOI MOSFETs. (b) Plots of the standard deviation (S.D.) and the maximum difference of V_{th} with respect to different gate number.

The characteristic fluctuations of multiple-gate SOI devices are also investigated. Figure 4.22 plots fluctuations of I_D-V_G for single- and multiple-gate SOI devices. The solid lines represent the nominal case and the dashed lines represent the discretely doped cases. The spread of the I_D-V_G curves shows the magnitude of the current fluctuation that is induced by discrete dopants. The result shows that the single-gate device exhibits much larger current fluctuations than the multiple-gate devices. Figure 4.23 plots the corresponding on- and off-state current characteristics. For cases with similar on-state currents, the maximum fluctuation of the off-state current declines as the number of gates increases; moreover, the maximum fluctuation of I_{off} in multiple-gate devices is within 20 nA/um, whereas the planar device (with a single gate) exhibits a much larger fluctuation of I_{off} (> 2000 nA/um). Figure 4.24(a) statistically compares the threshold voltage fluctuations of the aforementioned devices. As expected, the multiple-gate device exhibits better immunity against fluctuation and the magnitude of the V_{th} fluctuation (both standard deviation and difference between maximum and minimum V_{th} declines as the number of gates increases, as plotted in Fig. 4.24(b). The standard deviations (S.D.) of single-, double-, triple- and surrounding-gate devices are 102 mV, 46.2 mV, 30.9 mV and 25.5 mV, respectively. Calculations demonstrate that the fluctuations of V_{th} of the double-, triple- and quadruple surrounding-gate devices are 2.2, 3.3 and four times smaller, respectively, than that of the planar SOI device. The equivalent channel doping concentration increases with the dopant number, substantially altering V_{th}, as shown in Fig. 4.24(a), and the on- and off-state currents, as plotted in Fig. 4.22. The magnitude of spread increases with the number of dopants increases. The discrete-dopant-position affects the fluctuation of characteristics in a different manner for a fixed number of dopants.

The mechanism of immunity of single- and multiple-gate devices against fluctuation is studied with reference the extracted physical quantities. Figures 4.25(b) - 4.25(e) plot the on-state potential along the center of the device's channel, shown in Fig. 4.25(a), and display 3D electric fields of single-, double-, triple- and quadruple surrounding-gate devices, respectively. The potential and electric field of multiple-gate devices are more uniform than those of the planar device because the channel controllability is better than that of a planar device for a large gate-coverage ratio. Figure 4.26 compares the on-state current density, plotted in Figs. 4.26(a) - 4.26(d), and the contour of the off-state potential, shown in Figs. 4.26(a') - 4.26(d'), for the 16-nm-gate single-, double-, triple- and quadruple surrounding-gate SOI devices, respectively. All cross-sectional plots of the on-state current density and the off-state potential are at 1 nm below the top-gate oxide. As the gate-coverage ratio is increased, the on-state current density is increased and the heights of off-state potential spikes (A, B and C in Fig. 4.26(a)) are reduced. The lateral-gate structure of triple- and quadruple surrounding-gate devices effectively suppresses the potential (spike C), and then increases the on-state current at the lower side of the channel, shown

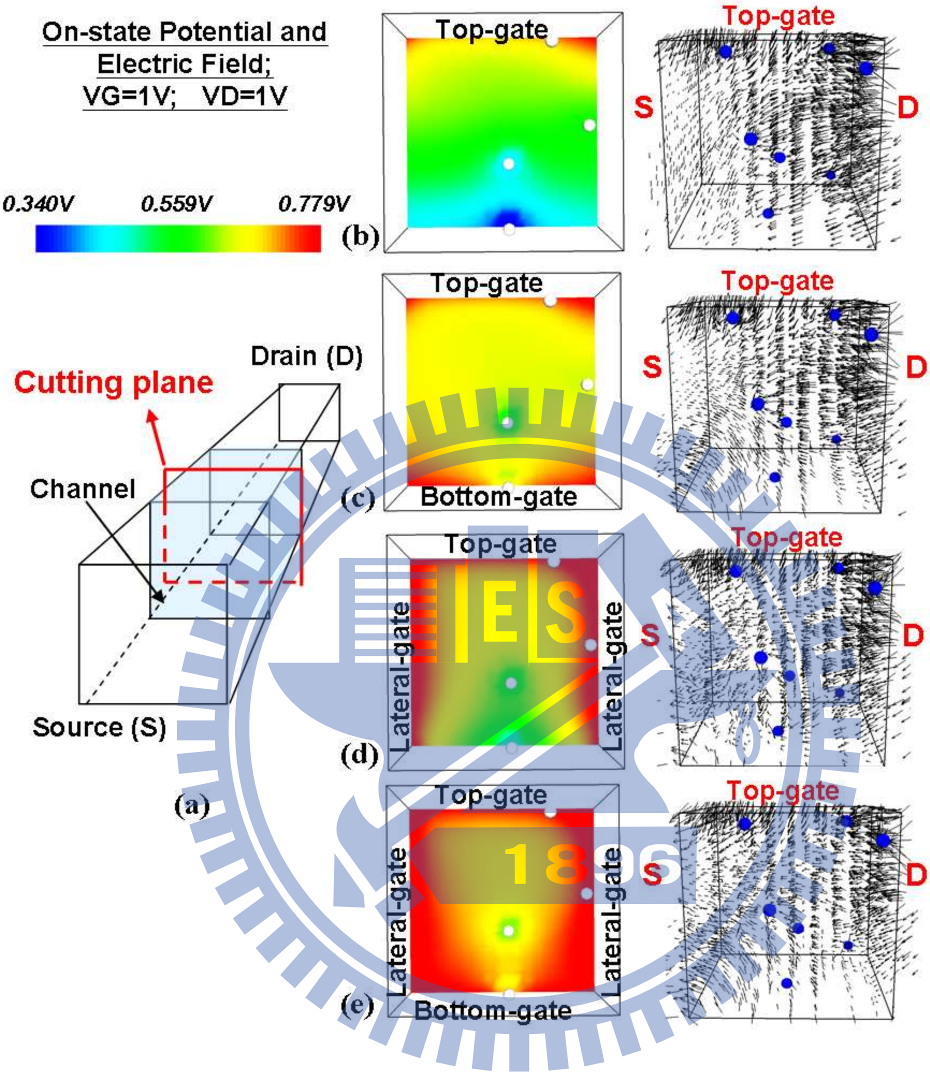


Figure 4.25: Plots of the on-state potential and 3D electric field distribution of the 16-nm-gate SOI MOSFET with the (b) single- (c) double-, (d) triple- and (e) quadruple surrounding-gate structure. The cross-sectional plots of the on-state potential distributions are extracted along the center of the device's channel, as shown in (a).

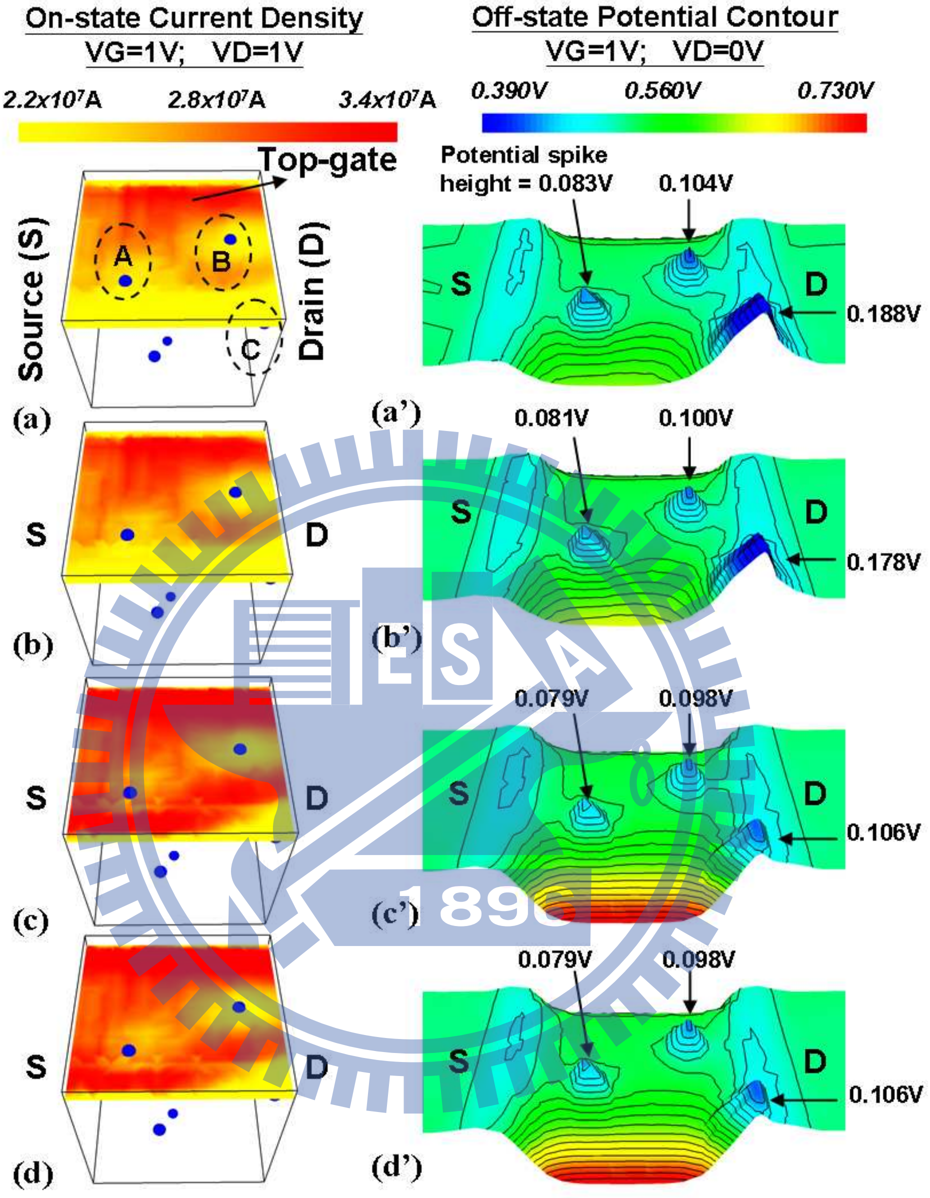


Figure 4.26: Plots of the on-state current density distributions ((a)-(d)) and the off-state potential contours ((a')-(d')) of the 16-nm-gate SOI MOSFETs ((a) and (a') are for the single-gate; double-gate: (b) and (b'); triple-gate: (c) and (c'); quadruple surrounding-gate: (d) and (d')). The potential spikes in (a')-(d') are induced by corresponding dopants in channel (spikes A, B, and C shown in (a)). The height of potential spikes is decreased as gate number is increased. All cross-sectional plots of the on-state current density distributions and off-state potential contours are extracted at 1 nm below the top-gate oxide.

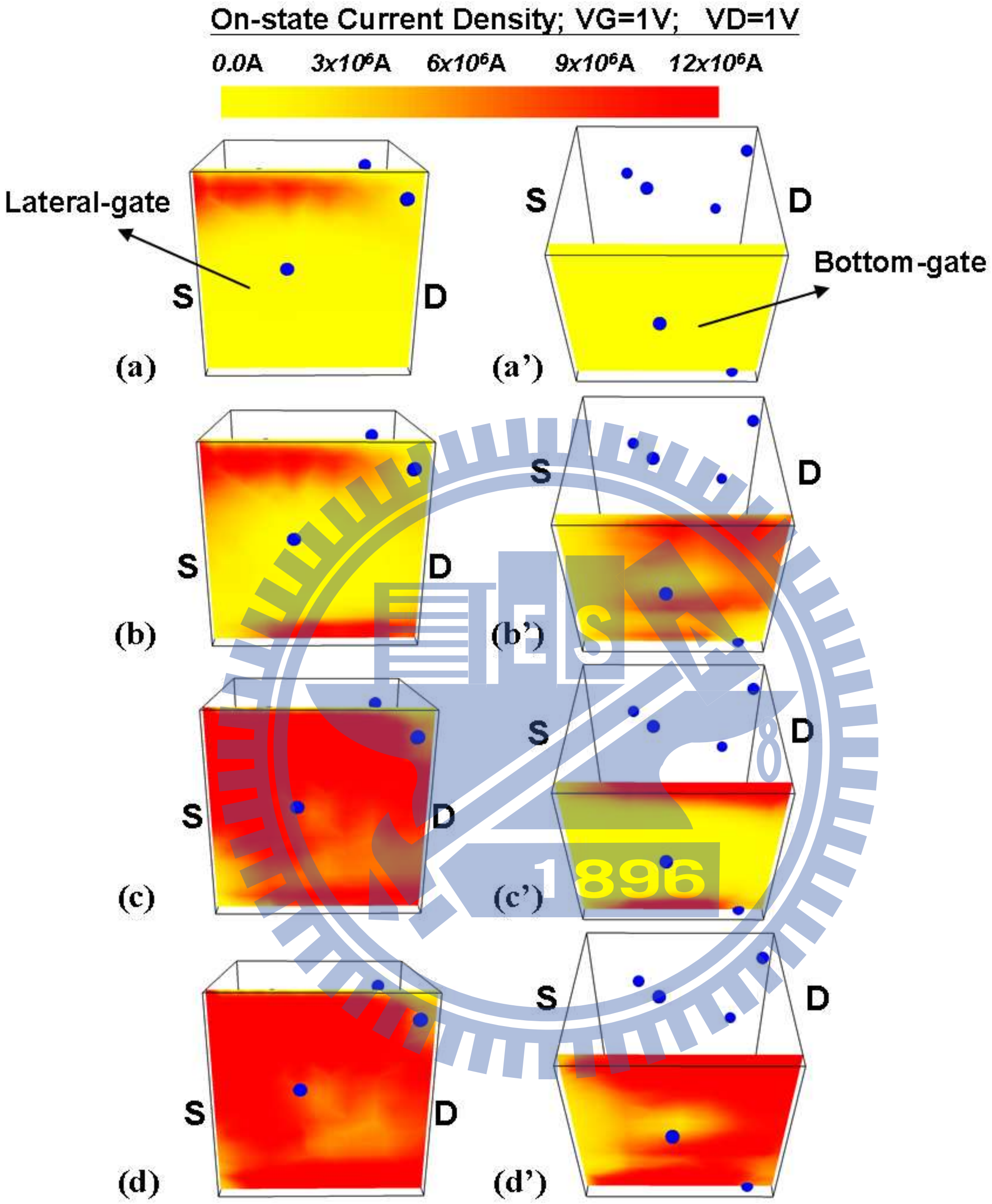


Figure 4.27: Plots of the lateral-side ((a)-(d)) and bottom-gate ((a')-(d')) on-state current density distributions of the 16-nm-gate devices ((a) single-gate; (b) double-gate; (c) triple-gate; (d) quadruple surrounding-gate). All cross-sectional figures are extracted at 1 nm below the lateral-side and bottom-gate oxides.

in Figs. 4.26(c) and 4.26(d). The lateral-gate of multiple-gate intrinsically enhances the controllability of dopant-induced fluctuations near the sidewall of the channel surface. It also accounts for why spike ”C” in Fig. 4.21(a’) has a weaker influence on the potential distribution than spike ”B”. Figure 4.27 shows the lateral- and bottom-gate on-state current densities of the structures. Similarly, all cross-sectional plots are obtained at 1 nm below the lateral- and bottom-gate oxides. Once current paths are impeded by discrete dopants on parts of channel surface, the well-gate-controlled multiple-gate structure bridges alternative conducting paths to prevent a significant fluctuation of the conduction current. Thus, the benefit of the superior vertical channel structure is that multiple-gate devices suppress potential fluctuation and provide a more stable conduction current than the planar device. As a result, the immunity against fluctuation in multiple-gate SOI devices results mainly from the uniform potential distribution and the fact that the current conduction area (multiple paths) is larger than that of a planar SOI device.

Besides the aforementioned multiple-gate devices, nanowire FinFETs are ultimate structures and potential candidates for next generation nanoelectronic devices [16-18, 29-39]. Due to the limitation of manufacturability, nanowire transistors with a perfect gate structure (i.e., a surrounding gate with 100% gate-coverage ratio) theoretically are not always guaranteed. Impact of the discrete dopants on device performance is crucial in determining the behaviour of nanoscale semiconductor devices. The immunity of nanowire transistor against random discrete-dopant-induced fluctuation may suffer from the variation of gate-coverage-ratio. This section first discusses the fluctuations of potential and current density due to discrete dopants; and then the impact of non-ideal nanowire gate-coverage ratio on immunity against discrete-dopant-induced fluctuations is studied.

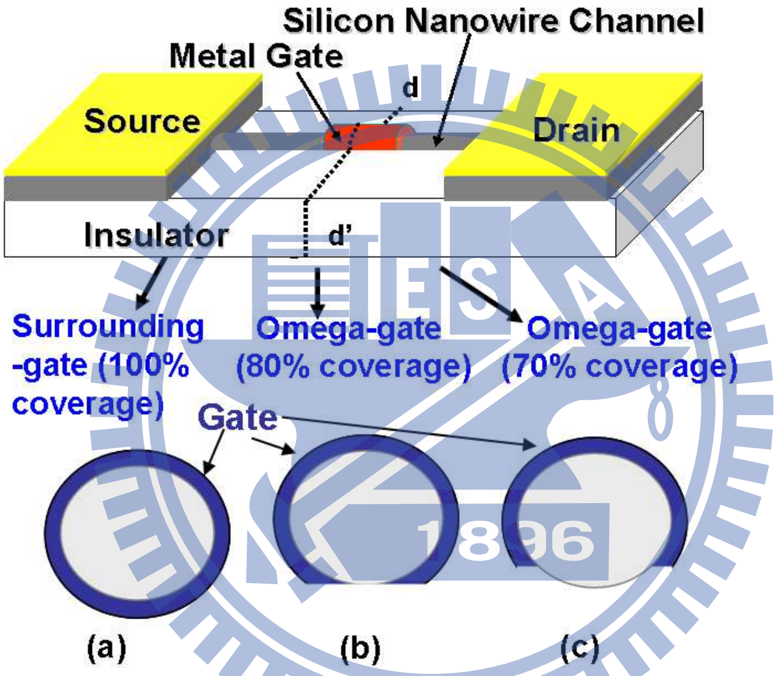


Figure 4.28: The 16-nm-gate silicon nanowire transistor with structures of (a) surrounding-gate (i.e., 100% coverage), (b) the omega-gate with 80% coverage-ratio, and (c) the omega-gate with 70% coverage-ratio.

Figures 4.28(a) - 4.28(c) illustrates the 16-nm-gate silicon nanowire transistor with

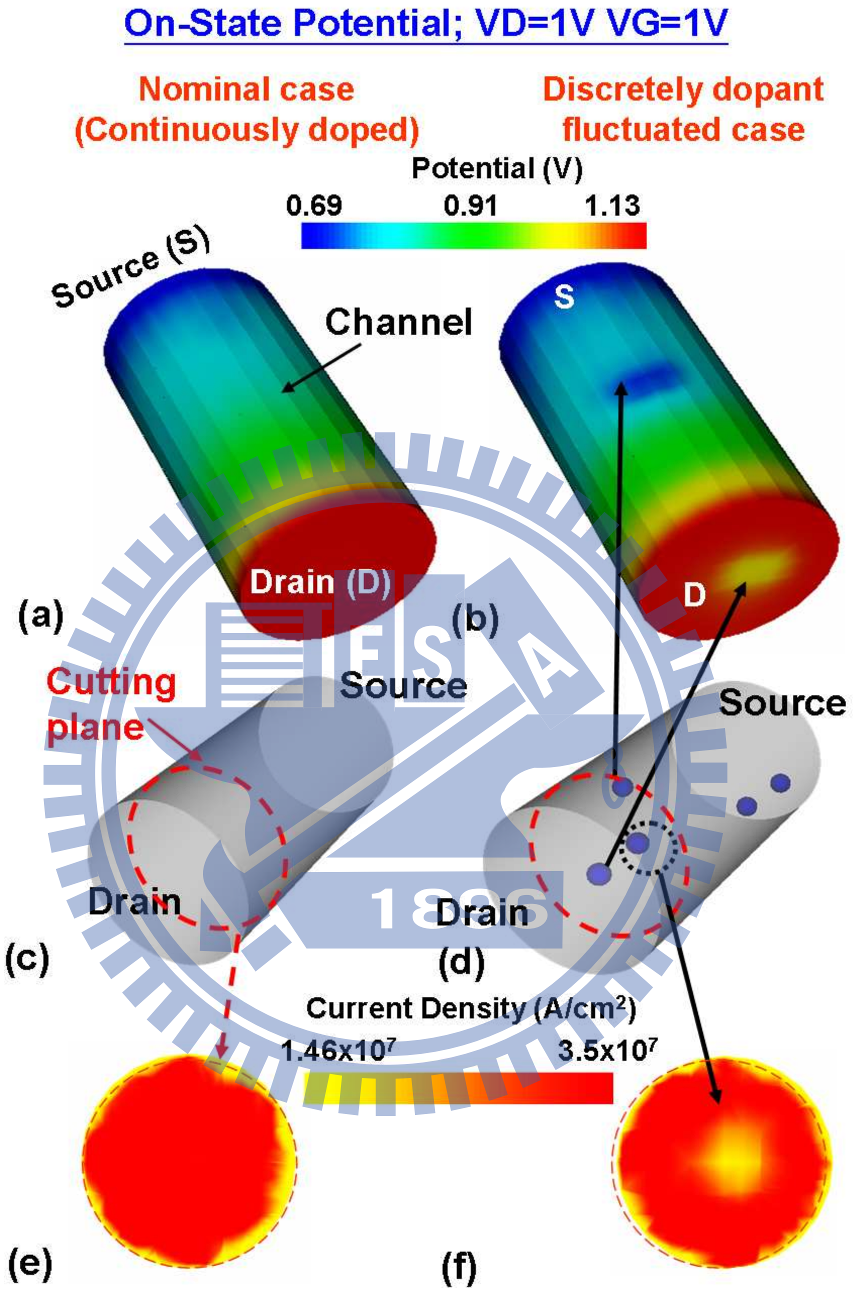


Figure 4.29: Comparison of the on-state potential ((a) and (b)), the current density distributions ((e) and (f)) of the (c) the nominal case and (d) discretely doped cases. The potential fluctuations are induced by corresponding dopants in (d)).

structures of surrounding-gate (i.e., 100% coverage), the omega-gate with 80% coverage-ratio, and the omega-gate with 70% coverage-ratio, respectively. The used physical models have been calibrated with experimental data. The on-state (the device is with V_D = V_G = 1V) potential distribution of the discretely doped case, shown in Figs. 4.29(a), and 4.29(b), are investigated to elucidate the effect of discrete dopant on the potential and current distributions of the device. The potential fluctuations, shown in Fig. 4.29(b), are associated with the corresponding dopants in Fig. 4.29(d). Comparison between Figs. 4.29(e) and 4.29(f) reveals that the current conducting path is disturbed and impeded by the discrete dopants locating at the channel. Since the potential distribution near the dopant is relatively negative in the channel, the dopant acts as a center of a whirlpool-like electric field to repel electrons. As electrons transport from the end of source to the drain side, some of them will encounter a negative electric field that is induced by the discrete dopants. The lateral electric field between the source and the drain, combined with the repulsion of the dopants, twists the electric field and increases the electron velocity near the dopants. The potential fluctuations not only alter the electric field and current conducting path, but also the electron velocity, and carrier mobility.

Figure 4.30 shows the comparisons of potential and current density distributions, respectively, for the nanowire transistors with the surrounding-gate (i.e., 100% gate-coverage-ratio) and the omega-gate (i.e., 80% and 70% gate-coverage-ratios) structures. The discrete

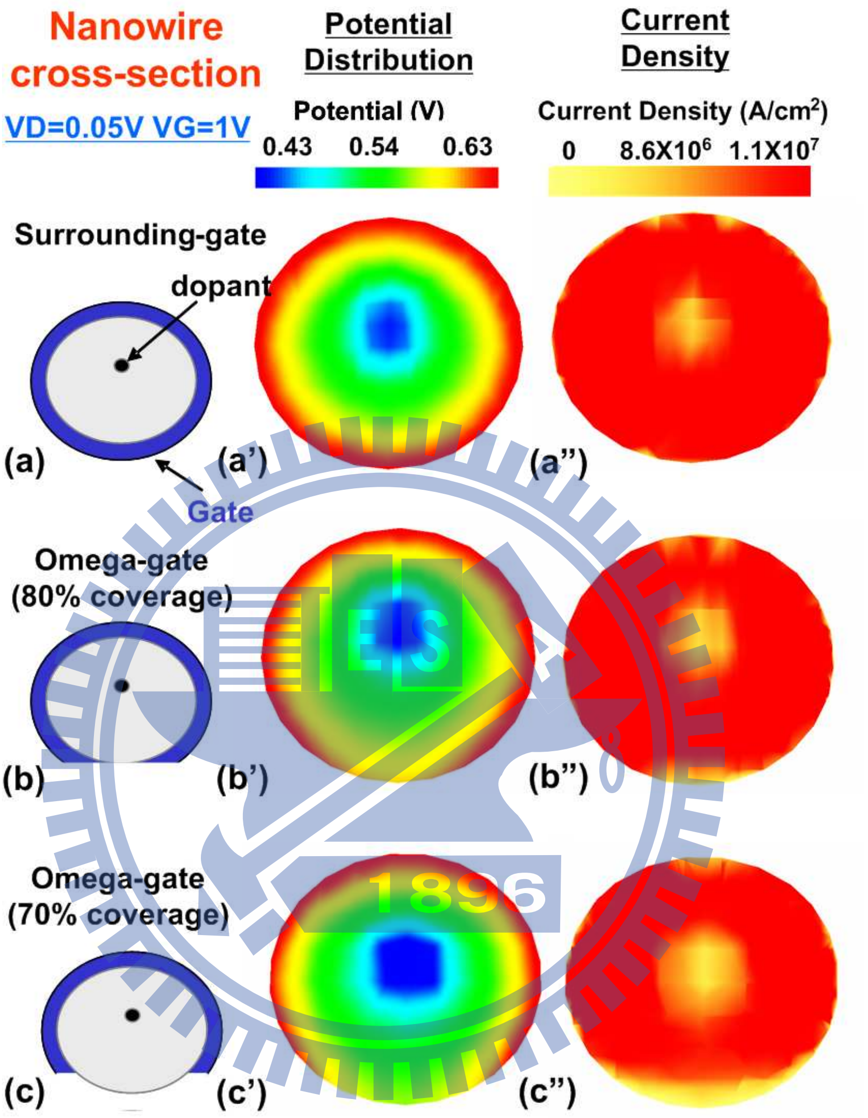


Figure 4.30: Comparison of potential (plots of (a'), (b'), and (c')) and current density distribution (plots of (a"), (b"), and (c")) in nanowire transistors with surrounding-gate (100% gate-coverage-ratio) and omega-gate (80% and 70% gate-coverage-ratio) structures.

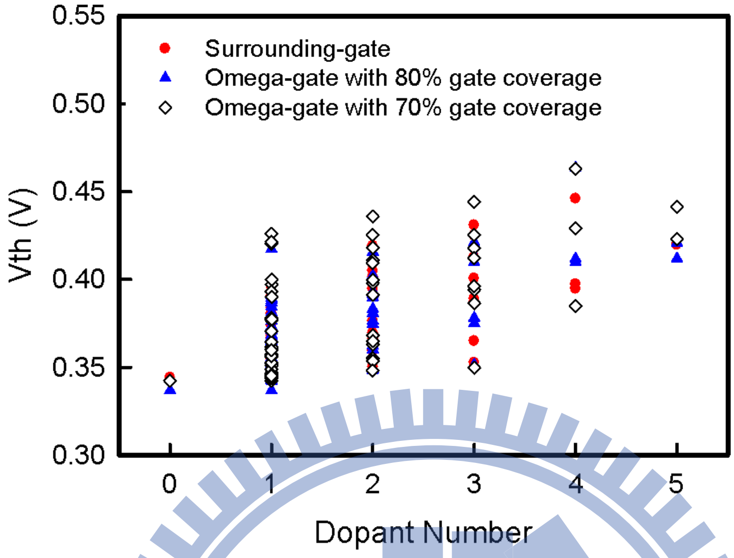


Figure 4.31: Comparison of the threshold voltage fluctuation of the 16-nm-gate silicon nanowire FET with surrounding-gate, omega-gate with 80%, and 70% gate-coverage-ratio.

dopants positioned in the channel induce a potential fluctuation and substantially disturbs the current density distribution and the corresponding conduction path. The magnitude of potential and current density fluctuations is increased as the gate-coverage-ratio decreases. The non-ideal gate-coverage disturbs the channel controllability of the explored nanowire transistors and thus decreases the immunity against discrete dopant induced fluctuation. In our study, for a 16-nm-gate silicon nanowire transistor, the threshold voltage fluctuations of the omega-gate devices with 80% and 70% gate-coverage are 1.04 and 1.19 times larger than that of the surrounding-gate structure, as shown in Fig. 4.31. For current fluctuations,

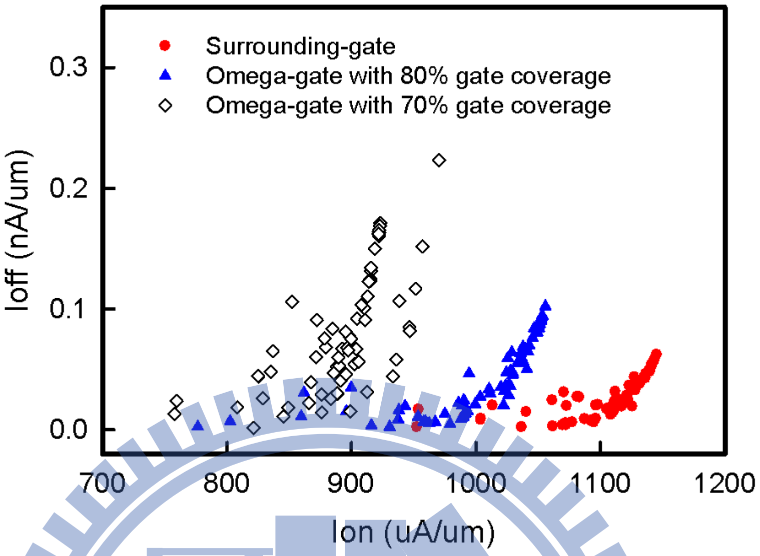


Figure 4.32: Comparison of the on-off state current fluctuation of the 16-nm-gate silicon nanowire FET with surrounding-gate, omega-gate with 80%, and 70% gate-coverage-ratio.

the ratio is 1.75 and 4.5 times larger than that of the surrounding-gate one, as shown in Fig. 4.32. The results confirm that the influence of non-ideal gate-coverage on the disturbances of the channel controllability of nanowire transistors. The immunity against discrete dopant induced fluctuation is thus decreased. Figure 4.33 shows the characteristics of the on-state and off-state currents (I_{on}-I_{off}). For those cases with similar I_{on}, the maximum fluctuation of I_{off} is within 0.05 nA/um. This figure discloses three different discrete-dopant channels, having similar values of I_{on} or I_{off} but with various dopant positions. The cross-sectional on-state current density and off-state potential distributions extracting

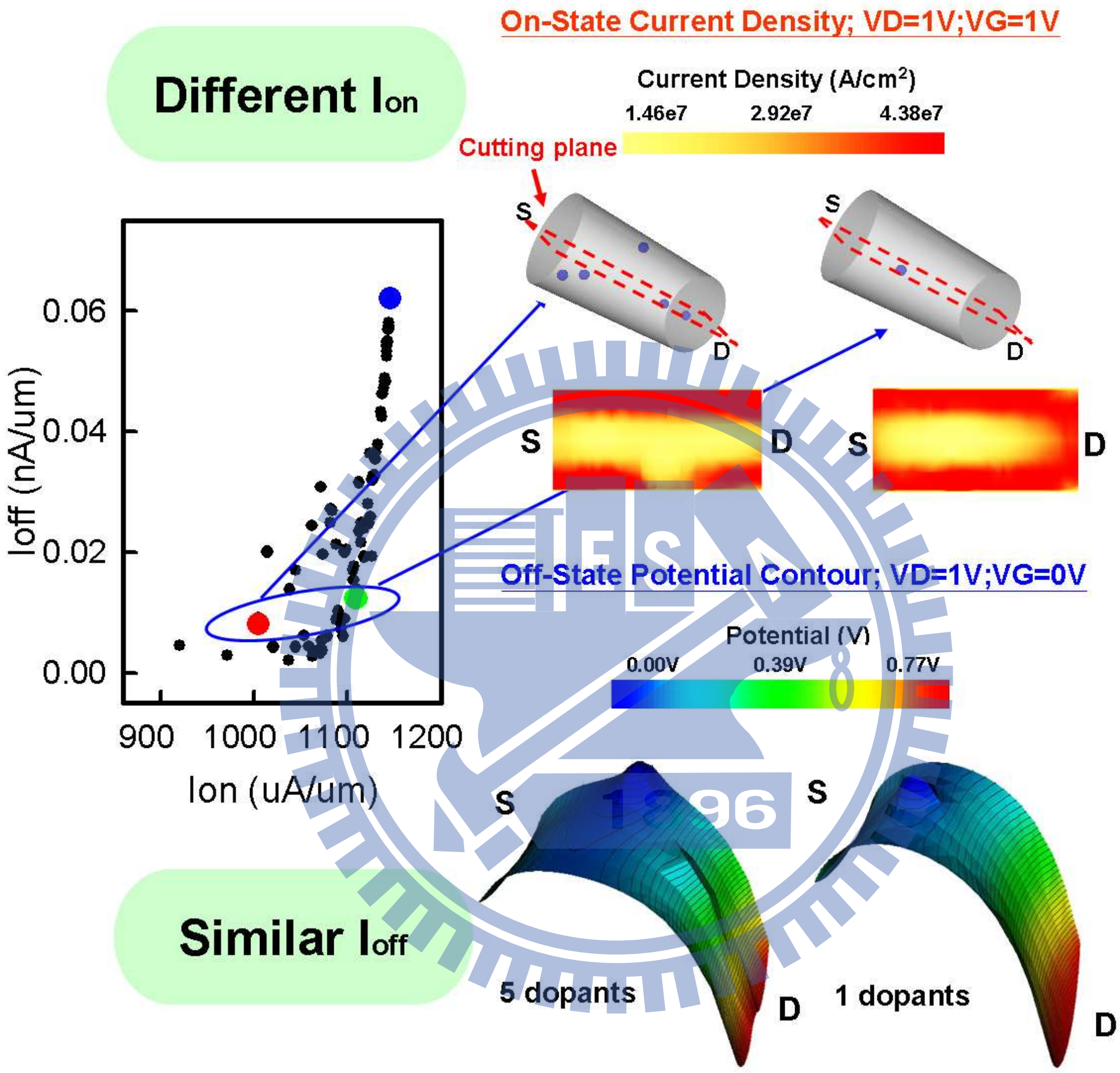


Figure 4.33: Effect of discrete-dopant-position in silicon nanowire FET, where the devices are with different I_{on} but similar I_{off}

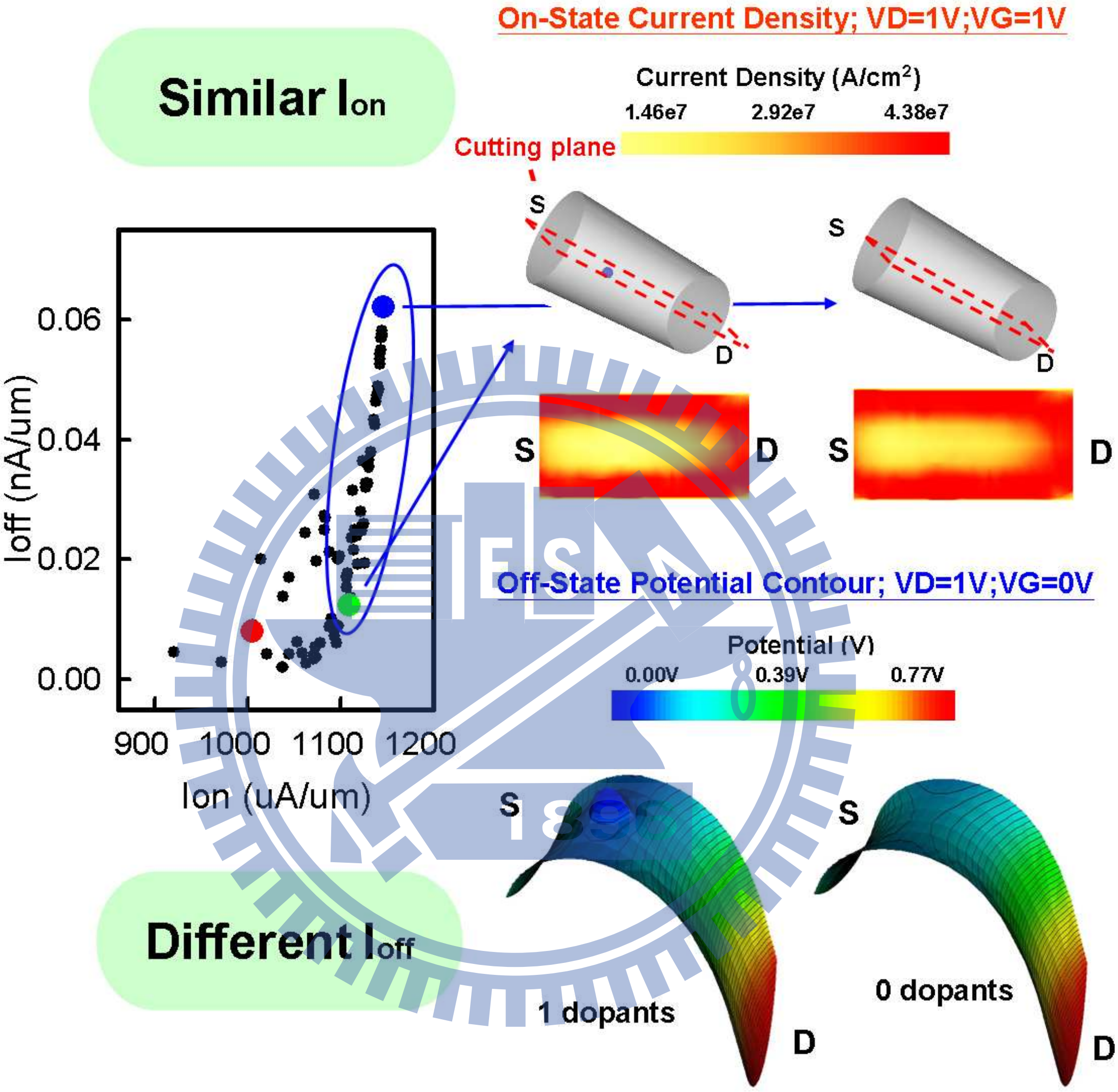


Figure 4.34: Effect of discrete-dopant-position in silicon nanowire FET, where the devices are with similar I_{on} but different I_{off}

from the center of channel are examined. Due to the difference of discrete dopant position, the different conduction paths of devices result in different on-state currents even we have very similar off-state currents, shown in Fig. 4.33. For the device having very similar on-state current with different off-state situations, Fig. 4.34 shows the off-state potential distribution at device's channel. However, due to the effect of discrete dopant position, there is no potential barrier located in the channel region.

4.3 Summary

The dependence of the threshold voltage fluctuation of bulk FinFETs on device dimension was empirically fitted as $\sigma V_{th} \propto (WL)^{-0.25}$, which is superior to that of planar MOSFETs. The preliminary results indicate the bulk FinFETs can not only provide better immunity against discrete-dopant-fluctuation induced threshold voltage fluctuations, but also show less sensitivity to device size than planar MOSFETs. The superior immunity against fluctuation and the more stable fluctuation of threshold voltage roll-off indicate the bulk FinFET to be a promising device for the sub-16-nm era. For the SOI transistors, the fluctuations of V_{th} of double-, triple-, and quadruple surrounding-gate SOI MOSFETs and the influence of non-ideal gate coverage disturbs the channel controllability of nanowire FinFETs are shown. Thus, the benefit of the superior vertical channel structure is that multiple-gate devices suppress potential fluctuation and provide a more stable conduction current than the planar device. As a result, the immunity against fluctuation in vertical-channel devices results mainly from the uniform potential distribution and the fact that the current conduction area (multiple paths) is larger than that of a planar transistors.

Chapter 5

Intrinsic Parameter Fluctuation in Fin-Typed Field Effect Transistors

Metal gate and multi-gate transistors are key technologies for the reduction of intrinsic parameter fluctuations. However, the use of metal as a gate material introduces a new source of random variation due to the dependency of workfunction on the orientation of metal grains. The WKF-induced threshold voltage fluctuation has been reported and the scope is limited to the transistors [121,122]. Additionally, the device and circuit performance may depend on different device characteristics. The comprehensive understanding of the dominant fluctuation source in the device and circuit characteristic fluctuations is urgent for the development of nanoscale systems. Therefore, this chapter estimates the influences of the intrinsic parameter fluctuations consisting of metal gate workfunction fluctuation, process variation effect and random dopant fluctuation on 16-nm-gate planar MOSFET and SOI FinFET devices. The DC characteristics are examined in terms of I-V and V_{th}. The AC parameters are investigated in terms of gate capacitance (C_g) and cutoff frequency (F_T). Then the dominant fluctuation sources in different devices are found.

5.1 DC Characteristic Fluctuation

The devices we investigated are the 16-nm-gate bulk MOSFETs (width: 16 nm) and SOI FinFETs (fin width/fin height: 16 nm / 32 nm) with amorphous-based TiN/HfSiON gate stacks with an EOT of 1.2 nm [121]. The dimensions of planar MOSFETs and SOI FinFETs are designed to have the same layout area. To compare the MOSFETs and FinFETs on the same basis, their nominal channel doping concentrations are 1.48×10^{18} cm^{-3} and the V_{th} are calibrated. Additionally, to compare fairly the NMOSFET- and PMOSFET-induced characteristic fluctuation and eliminate the effect of transistor size on fluctuation, the dimensions of the PMOSFETs were the same as those of the NMOSFETs. For $\sigma V_{th,RDF}$ of FinFETs, to consider the random fluctuation effect of the number and location of discrete channel dopants, 1516 dopants are randomly generated in a large cube, in which the equivalent doping concentration is 1.48×10^{18} cm^{-3}, as shown in Fig. 5.1(a). The large cube is then partitioned into 125 sub-cubes. The number of dopants may vary from two to 22, and

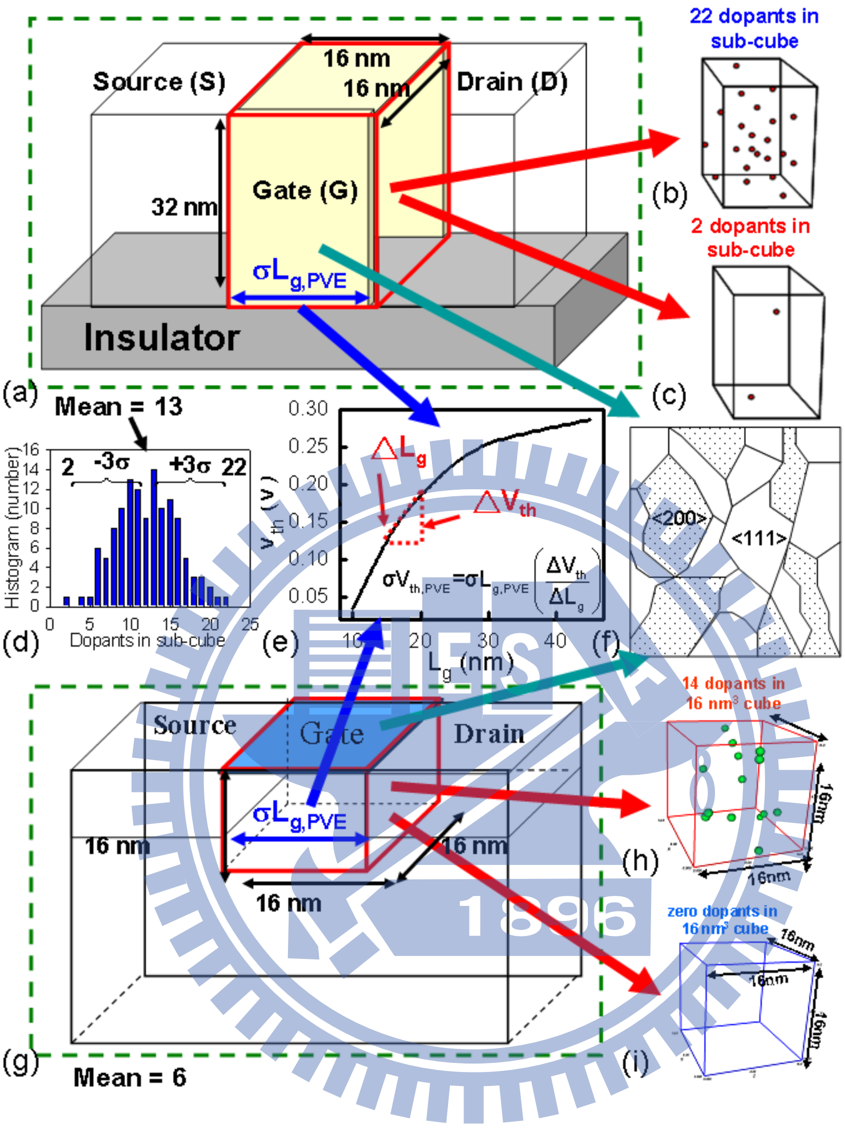


Figure 5.1: (a) An illustration of FinFET structure. 1516 dopants are randomly generated in a large cube of 80×80×160 nm^3, in which the equivalent doping concentration is 1.48×10^{18} cm^{-3}. The large cube is then partitioned into 125 sub-cubes of 16×16×32 nm^3. The number of dopants in sub-cube may vary from two to 22, and the average number is 13 ((b)-(d)). These 125 sub-cubes are equivalently mapped into the device channel of device for the 3D device simulation with discrete dopants. (e) The V_{th} roll-off is used for PVE estimation. The PVE includes the gate length deviation and the line edge roughness, whose magnitude follow the projections of the ITRS roadmap [1]. (f) The $\sigma V_{th,WKF}$ is estimated by a statistically sound Monte-Carlo approach. ((g)-(i)) Similarly, 758 dopants are generated in a large cube of 80×80×80 nm^3 and into 125 sub-cubes of 16×16×16 nm^3 for planar MOSFETs discrete dopant simulation.

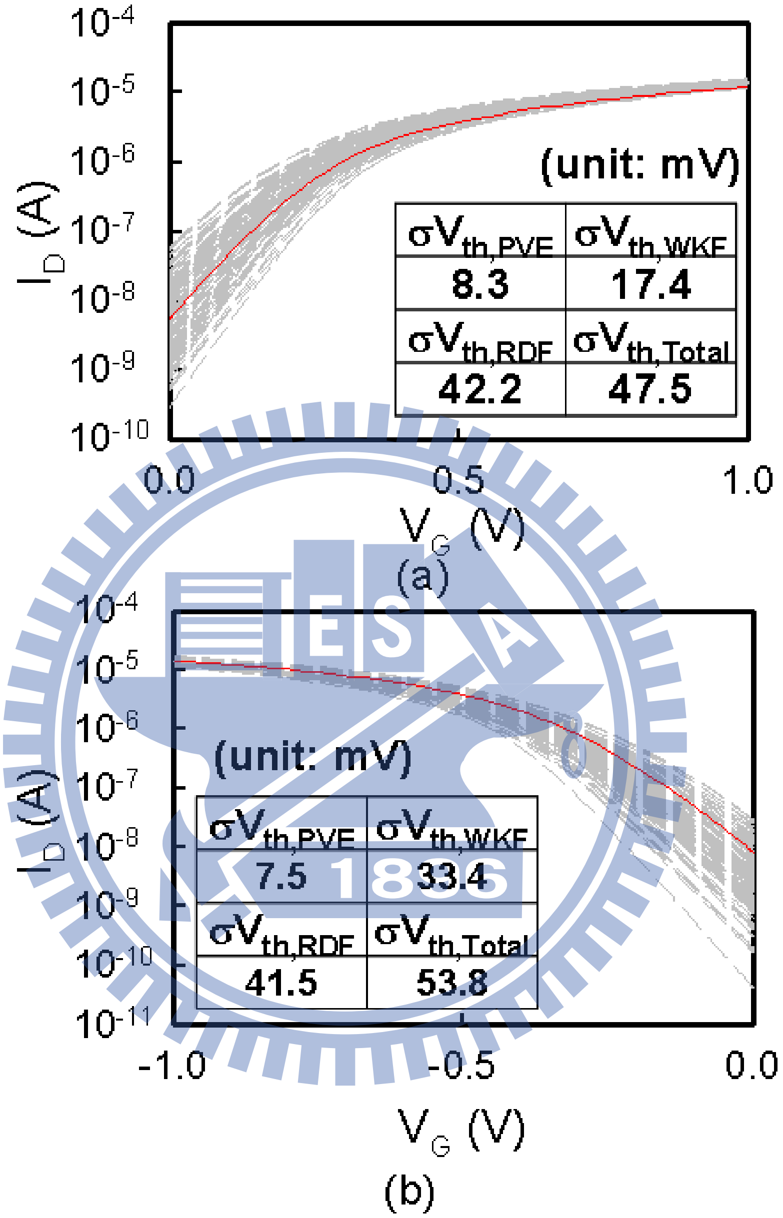
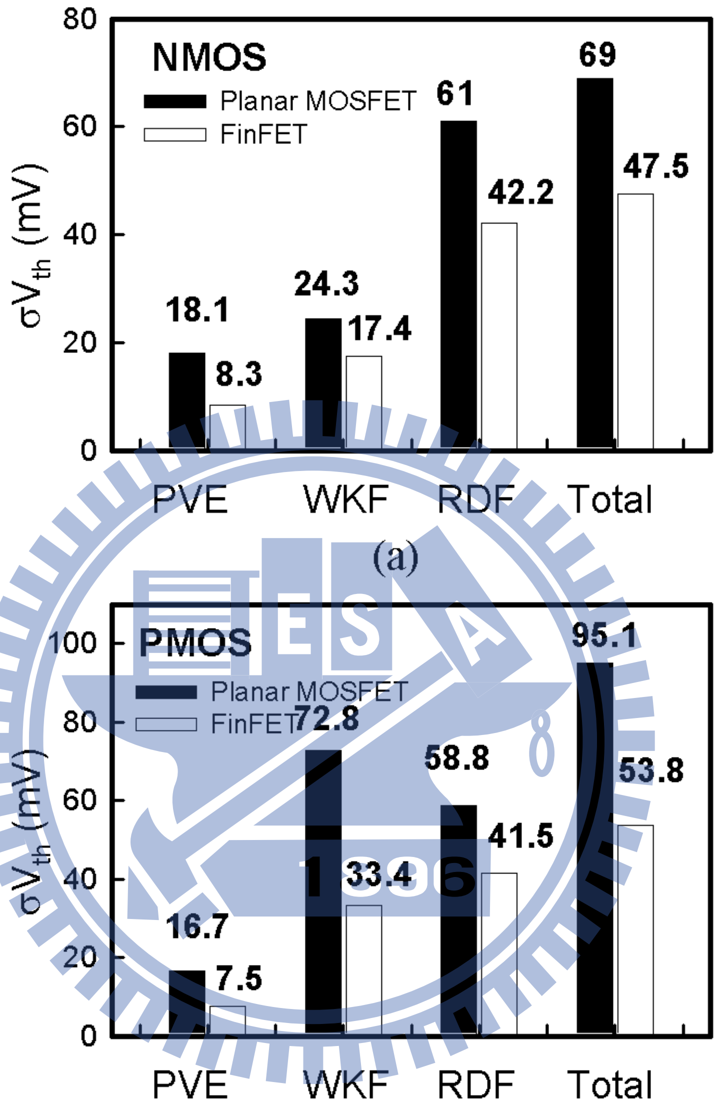


Figure 5.2: The I_D-V_G fluctuations for (a) NMOSFETs and (b) PMOSFETs, where the solid line shows the nominal case with expected device dimensions, workfunction, and 1.48×10^{18} cm^{-3} continuous channel doping. The dashed lines are fluctuated cases.

the average number is 13, as shown in Figs. 5.1(b) - 5.1(d), respectively. These 125 sub-cubes are equivalently mapped into the device channel for the 3D device simulation with discrete dopants, as shown in Fig. 5.1(a). The device is simulated by solving a set of 3D density-gradient equations coupled with Poisson equation and electron-hole current continuity equations [99-108]. The physical model and accuracy of such large-scale simulation approach have been quantitatively calibrated by experimentally measured results [20,63]. The PVE includes the gate length deviation and the line edge roughness, whose magnitude follow the projections of the ITRS roadmap [1]. Figure 5.1(e) shows the threshold voltage roll-off characteristic to estimate $\sigma V_{th,PVE}$. The $\sigma V_{th,WKF}$ is estimated by a statistically sound Monte-Carlo approach, as shown in Fig. 5.1(f). Similarly, 758 dopants are generated in a large cube of 80×80×80 nm^3 and partitioned and into 125 sub-cubes of 16×16×16 nm^3 for planar MOSFETs discrete dopant simulation, as shown in Figs. 5.1(g) - 5.1(i). The dopants in sub-cubes may vary from zero to 14, and the average number is six.

Figures 5.2(a) and 5.2(b) shows the I_D-V_G characteristics for NMOS and PMOS devices, respectively. The solid line shows the nominal case with expected device dimensions, workfunction, and 1.48×10^{18} cm^{-3} continuous channel doping. The dashed lines are fluctuated cases.The insets summary the σV_{th}s. Figures. 5.3(a) and 5.3(b) then compare the V_{th} fluctuations of NMOSFETs and PMOSFETs for bulk MOSFETs and SOI FinFETs, respectively. The total V_{th} fluctuation ($\sigma V_{th,total}$) is given by according to the independency



(a)

(b)

Figure 5.3: The summarized V_{th} fluctuation for (a) NMOSFETs and (b) PMOSFETs, where the filled-in bars are the results of planar MOSFETs and the open bard are the results of FinFETs.

of the fluctuation components:

$$(\sigma V_{th,total})^2 \approx (\sigma V_{th,RDF})^2 + (\sigma V_{th,WKF})^2 + (\sigma V_{th,PVE})^2 \tag{5.1}$$

in which the $\sigma V_{th,RDF}$, $\sigma V_{th,WKF}$, and $\sigma V_{th,PVE}$, are the random-dopant-induced, workfunction-fluctuation-induced and process- variation-induced V_{th} fluctuation, respectively. The results show that in SOI FinFET devices the RDF dominates the V_{th} fluctuation in both NMOSFETs and PMOSFETs. However, for planar transistors, the V_{th} fluctuation of PMOS is mainly determined by the WKF because of the large deviation of the workfunction for different grain orientation. The WKF in SOI FinFETs is less important due to the large gate coverage area of the designed device structure. Our preliminary results show that the SOI FinFET is less sensitive to the intrinsic parameter fluctuations due to the larger gate control area and thus suffers from less short channel effect. The $\sigma V_{th,total}$s of n-type and p-type FinFETs are 1.45 and 1.77 times smaller than those of planar MOSFETs. Notably, the statistical addition of individual fluctuation sources herein, Equation (1), simplifies the variability analysis of nano-devices and circuits, significantly. The dominant source of fluctuation will not be significantly altered.

5.2 AC Characteristic Fluctuation

The WKF, PVE, and RDF fluctuated C_g are presented in Figs. 5.4(a)- 5.4(c), where the solid line shows the nominal case with expected device dimensions, workfunction, and

1.48×10^{18} cm^{-3} continuous channel doping. The different intrinsic parameter fluctuations induced rather different C-V characteristics. Figure 3(d) summarizes the gate capacitance fluctuations (σC_g) with 0 V, 0.5 V and 1.0 V gate bias. Different to the results of V_{th} fluctuation, the WKF brought less impact on gate capacitance fluctuation. At low gate bias or negative gate bias, the accumulation layer screens the impact of WKF. Additionally, at low gate bias, the total capacitance decreases because of the increased depletion region. The associated value of C_g fluctuation is small. The capacitive response is then dominated by increment of inversion in the moderate inversion. The device characteristics are then impacted by intrinsic parameter fluctuated electrostatic potentials. If the high V_G is achieved, the capacitive response becomes dominated by the inversion layer, the impact of the individual dopants on the device electrostatics is screened by the inversion layer itself. The variation of capacitance is now again becomes the variation of gate oxide. The impact of WKF induced electrostatic potential variations is therefore bringing less impact on channel surface. Our preliminary results show that the RDF and PVE dominate the gate capacitance fluctuations at all gate bias conditions, respectively. The impacts of the WKF on C_g is reduced significantly at high gate voltage (V_G) due to the screening effect of inversion layer of device, which screens the variation of surface electrostatic potential and decreases the fluctuation of gate capacitance. The screening effect resulting from the inversion layer also decreases the RDF induced gate capacitance fluctuation at high gate bias; however, the screening effect of inversion layer is weakened by discrete dopants positioned near the channel surface. Notably, the PVE brings direct impact on gate length and therefore influences the gate capacitance. The PVE induced gate capacitance fluctuation is independent of screening effect and should be noticed when the transistor operated in high gate bias, as shown in Fig. 5.4(d).

Attention should be drawn on the existence of nonlinear effect for gate capacitance fluctuation. Figure 5.5(a) plots the C_g-V_G characteristics of 16 nm planar NMOSFETs with discrete dopant fluctuations. The solid and dot lines are the cases with and without random-dopant-position effect, respectively. The cases without random-dopant-position effect are simulated by changing their channel doping concentration continuously from 1.0×10^{15} cm^{-3} to 3.4×10^{18} cm^{-3}. Figure 5.5(b) plots the slope of the C_g-V_G curves, in which the gate capacitance is fixed to 5.0×10^{-18} F. The dash line indicates the cases without random-dopant- position effect, and the symbols are the cases with random-dopant-position effect. The slope of C_g-V_G curve for the cases without random-dopant-position effect is nearly independent of doping concentration, which implies the lateral shift of the C_g-V_G curves. The lateral shift of gate capacitance is resulted from the variation of V_{th}, and can be described by the correspond parameters in compact model. However, the slopes of C_g-V_G curves are substantially altered as the random-dopant-position effect is taken into consideration, as shown in Fig. 5.5(b). The variation of the slopes of C_g-V_G curves

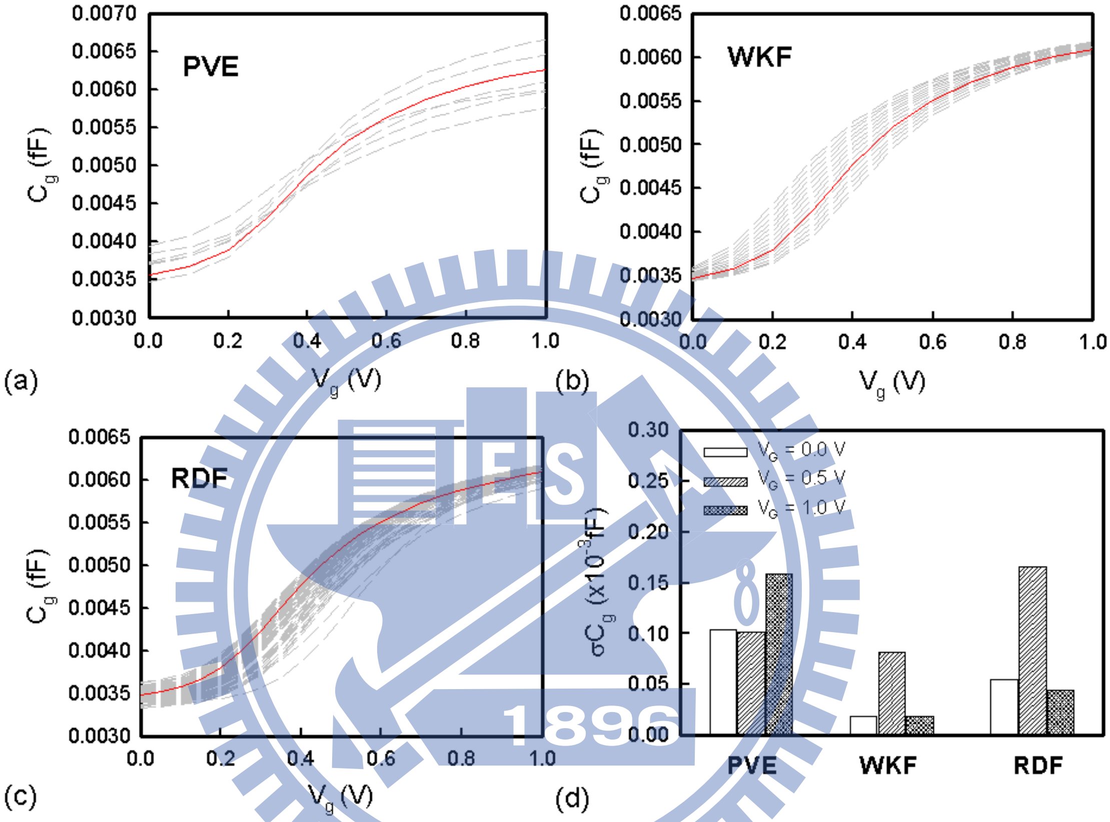


Figure 5.4: The C_g-V_G characteristics for the explored devices with (a) PVE, (b) WKF, and (c) RDF. (d) The C_g fluctuation for 16-nm-gate MOSFETs with WKF, PVE, and RDF. The applied voltage for the bars are V_G = 0, 0.5, and 1 V, respectively.

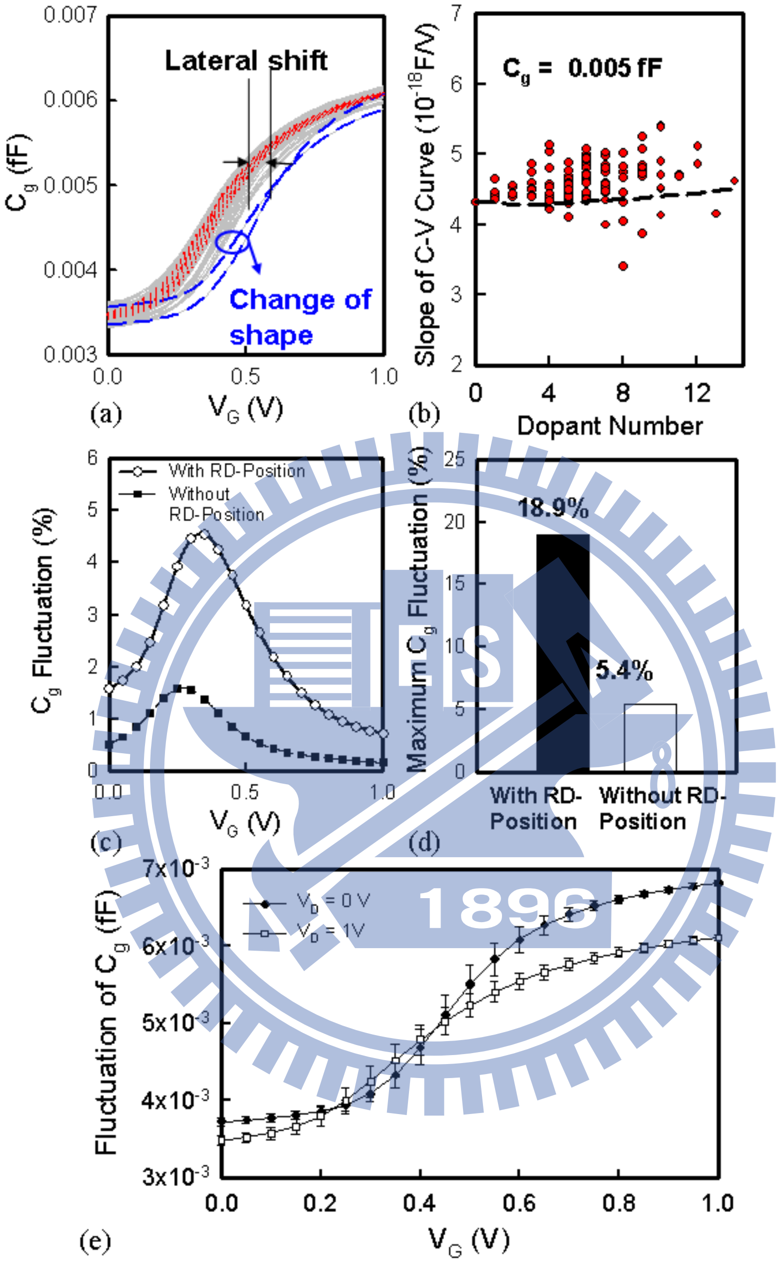


Figure 5.5: The (a) C_g-V_G curves and (b) the slope of the C_g-V_G curves for cases with and without taking random-dopant-position effect into consideration, where the solid line shows the nominal case and the dashed lines are random-dopant-fluctuated devices. The solid and dot lines in (a) are the cases with and without random-dopant-position effect, respectively. The dash line in (b) indicates the cases without random-dopant-position effect, and the symbols are the cases with random-dopant-position effect. The (c) normalized gate capacitance fluctuation and (d) maximum gate capacitance fluctuation are calculated. (e) The C fluctuation with different drain bias.

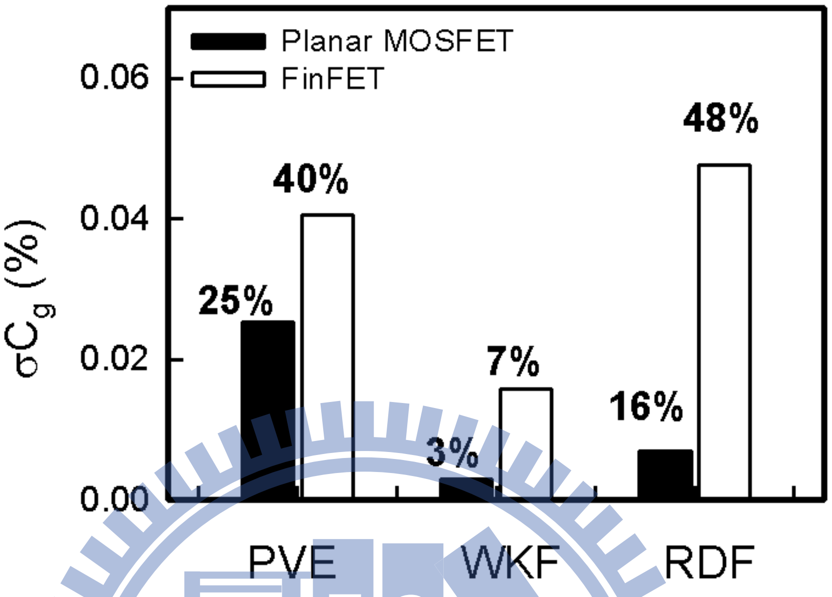


Figure 5.6: The C_g fluctuation for planar MOSFETs and SOI FinFETs with WKF, PVE, and RDF. The filled-in bars are the results of planar MOSFETs and the open bars are the results of SOI FinFETs.

indicates the change of shape of C_g-V_G curves, as illustrated in Fig. 5.5(a). The variation of C_g-V_G curves is resulted from the randomness of dopant position in the depletion region of channel and therefore is hard to be described in current compact model [64-67,77]. To the best of the author's knowledge, the fluctuation in gate capacitance has not yet been modeled and a coupled device-circuit simulation must be performed to estimate its impact on circuit characteristics. Figure 5.5(c) plots the normalized C_g fluctuation as a function of gate bias. The C_g fluctuations are normalized by the nominal C_g. The result implies the importance of random-dopant- position effect. Moreover, the device under subthreshold operation suffers from the largest fluctuation. For device with high gate voltage (V_G), the screening effect of inversion layer of device screens the variation of electrostatic potential and decreases the fluctuation of gate capacitance [77]. The normalized maximum variations of C_g are summarized in Fig. 5.5d), in which the normalized maximum variation of C_g is about 18.9$\%$. The neglect of the random-dopant-position effect may under estimate the C_g fluctuation by a factor of five. Figure 5.5(e) shows the σC_g with different drain bias. The device with high drain bias has a less gate capacitance fluctuation due to the pinch-off effect and smaller gate-to-drain capacitance at a high drain bias. Figure 5.6 compares the gate capacitance fluctuations for planar MOSFETs and SOI FinFETs. Under the layout area, the SOI FinFETs exhibits a larger gate capacitance fluctuation due to the large numbers of dopants in the large depletion region of the SOI FinFETs.

Figures 5.7 and 5.8 show the cutoff frequency (F_T = v_{sat} / $2\pi L_g$ = g_m / $2\pi C_g$) and its fluctuation versus the gate voltage for planar MOSFETs and SOI FinFETs, in which the solid line shows the nominal case with 1.48$\times$10^{18} cm^{-3} channel doping, the dashed lines are fluctuated cases, and the symbol line shows averaged result. The g_m and v_{sat} are the transconductance and the saturation velocity of the transistors, respectively. The planar MOSFETs possess higher F_T than that of FinFETs due to the smaller gate capacitance; WKF-induced F_T fluctuation diminished as the saturation of the carrier velocity occurs.

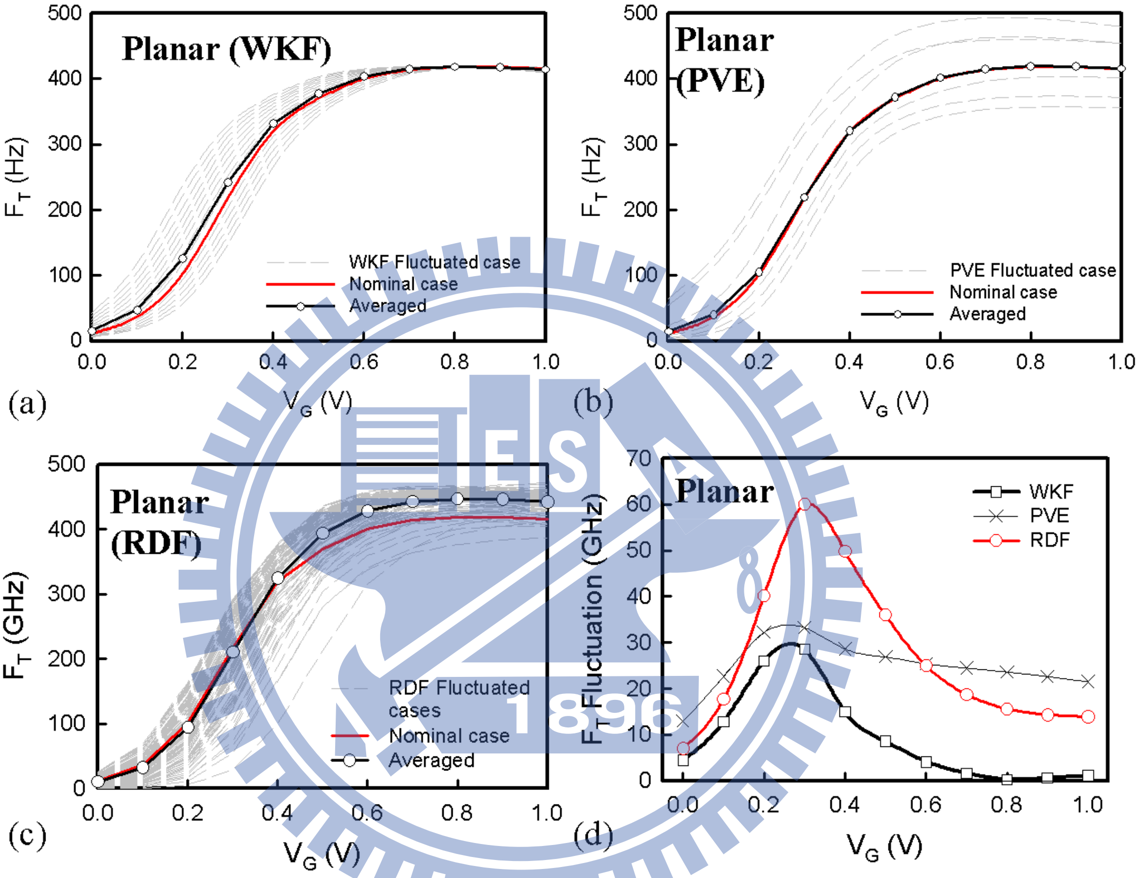


Figure 5.7: The (a)WKF, (b)PVE, and (c) RDF induced F_T characteristics fluctuation of planar MOSFETs. (d)The summarized F_T fluctuations.

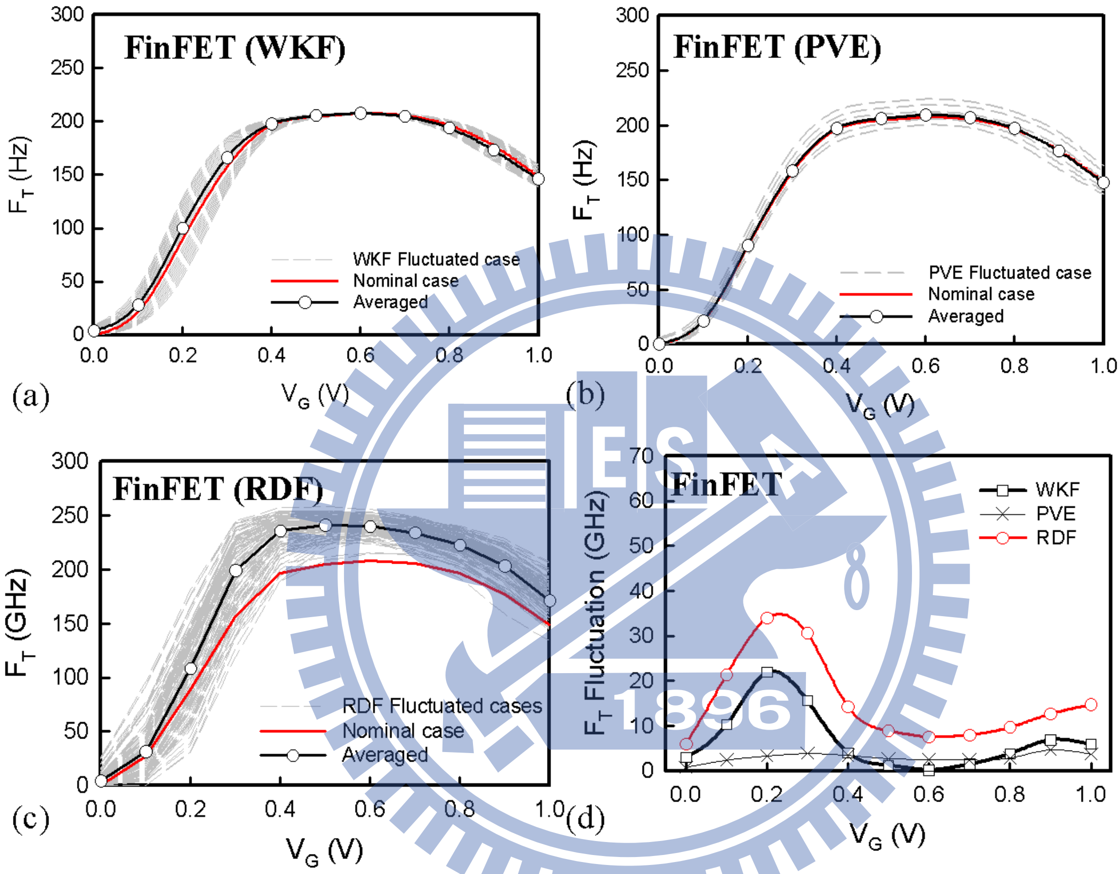


Figure 5.8: The (a)WKF, (b)PVE, and (c) RDF induced F_T characteristics fluctuation of FinFETs. (d)The summarized F_T fluctuations.

However, the PVE-induced F_T fluctuation is still significant owing to the direct influence of gate length (L_g) on gate capacitance. As for RDF, the carrier-impurity scattering alters the saturation velocity, and therefore F_T fluctuation does not diminish in high-field region. It's worth to note that the nominal and the averaged values of F_T are similar to the results of WKF and PVE. However, in RDF, the deviation between the nominal and the averaged F_T increases as V_G increases due to the randomness of carrier-impurity scattering events and carrier velocity variations. As shown in Figs. 5.7(d) and 5.8(d), RDF plays the dominating factor in the F_T fluctuation. For planar MOSFETs, PVE become dominates F_T fluctuation as V_G larger than 0.6 V due to the screening effect in RDF and WKF fluctuations. The obtained results are similar to the results as shown in Fig. 5.4(d), in which the PVE dominates the gate capacitance fluctuation in high gate voltage. As for the SOI FinFETs, the RDF is the dominant fluctuation sources due to the larger gate area and smaller WKF and PVE fluctuation comparing to planar MOSFETs.

5.3 Summary

This chapter have estimated the influences of the intrinsic parameter fluctuations in 16-nm-gate devices. The dimensions of planar MOSFETs and SOI FinFETs are designed to have the same layout area; also, their threshold voltages were calibrated to 140 mV. The RDF dominates the V_{th} fluctuation of FinFETs in both NMOSFETs and PMOSFETs. However, for planar transistors, the V_{th} fluctuation of PMOS is mainly determined by the WKF because of the large deviation of the workfunction for different grain orientation. Although the WKF in SOI FinFETs is less important due to the large gate coverage area of the designed device structure, the impact of WKF starts to draw people's attention device reliability. As for the AC characteristics, the nonlinear variation of C_g-V_G curves resulted from the randomness of dopant position in the depletion region of channel has been found. The nonlinear effect is hard to be described in current compact model, and therefore a coupled device-circuit simulation were employed to estimate its impact on circuit characteristics. The impacts of the WKF on C_g is reduced significantly at high gate voltage (V_G) due to the screening effect of inversion layer of device. The screening effect resulting from the inversion layer also decreases the RDF induced gate capacitance fluctuation at high gate bias; however, it is weakened by discrete dopants positioned near the channel surface. Notably, the PVE induced gate capacitance fluctuation is independent of screening effect and should be noticed.

Chapter 6

Implication of Device Variability in Circuits

The impact of intrinsic parameter fluctuation on device reliability has been discovered in the previous chapter. This chapter then explores the associated device variability in the state-of-art circuits using nanoscale transistors. Since there is no well-established compact models for describing the behaviors of nanoscale transistors, the coupled device-circuit simulation approach [64-67,115-118] is then developed to ensure the best simulation accuracy. Then the implication of nanoscale device variability in circuits is studied and the dominant fluctuation sources in each circuit characteristics are identified and verified.

6.1 The Coupled Device-Circuit Simulation Technique

For state-of-art nanoscale VLSI circuits and systems, the local device variation and uncertainty of signal propagation time have become crucial in the variation of system timing and the high frequency characteristics. Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, variations in the process parameters, and other factors are known as indispensable components of the circuit design procedure [44-48]. Diverse approaches have recently been presented to investigate fluctuation-related issues in transistors [21-27,62-83] and circuits [61-67,84-89]. However, most of they relies on the use of compact models. Thought the extraction of compact model provides an efficient way to estimate circuit characteristics fluctuation, the random dopant induced nonlinear device gate capacitance fluctuations make the device characteristics difficult to be modelled using present compact models [64-67,77]. Moreover, the well-established compact model of ultrasmall nanoscale devices is not available yet. To capture the discrete-dopant-position-induced fluctuations in nanoscale transistor circuits, a coupled device-circuit simulation approach [64-67,115-118] is then proposed. The characteristics of the devices of the circuit are first estimated by solving the device transport equations. The obtained result is then used as initial guesses in the coupled device-circuit simulation. The nodal equations of the test circuit are formulated and then directly coupled to the device transport equations (in the form of a large matrix that contains both circuit

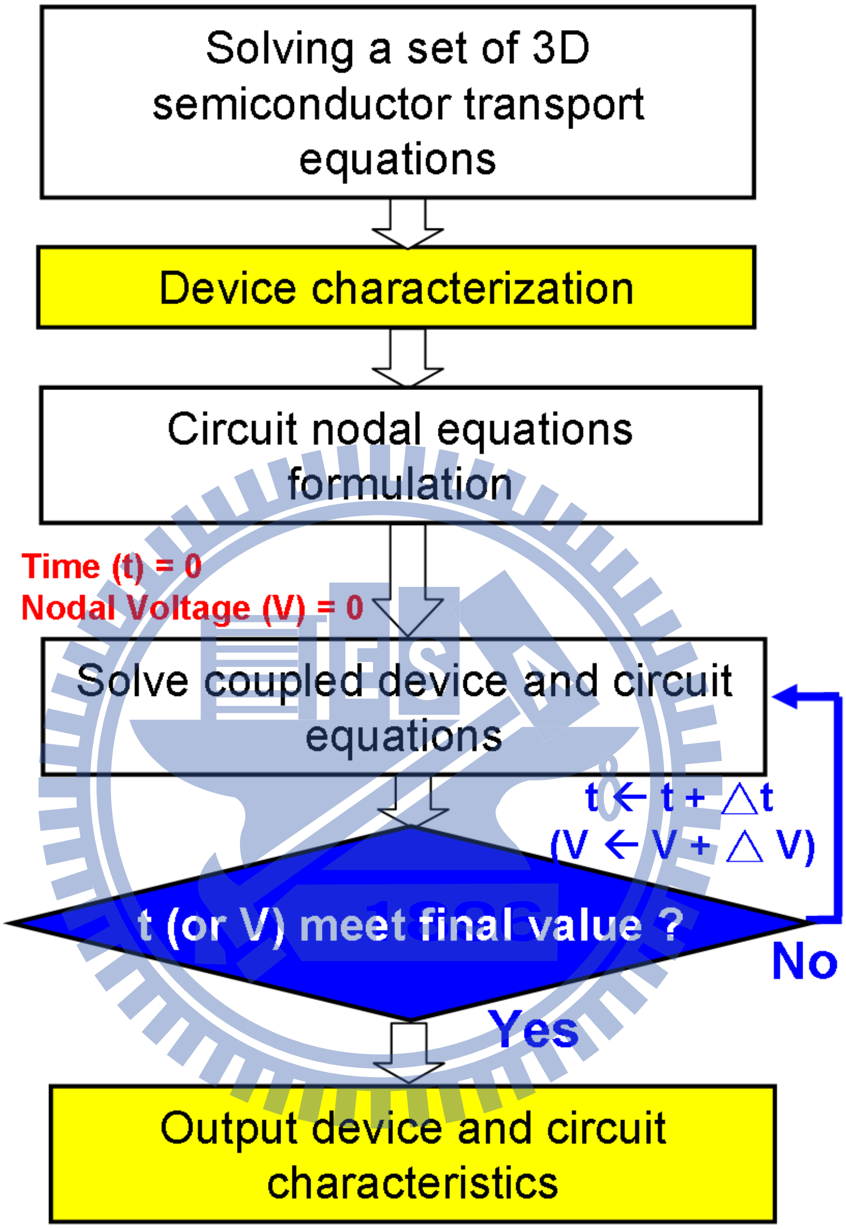


Figure 6.1: Time domain coupled device circuit simulation flow [64-67,115-118]. The characteristics of the devices of the circuit are first estimated by solving the device transport equations. The obtained result is then used as initial guesses in the coupled device-circuit simulation. The nodal equations of the test circuit are formulated and then directly coupled to the device transport equations, which are solved simultaneously to obtain the devices and circuit characteristics.

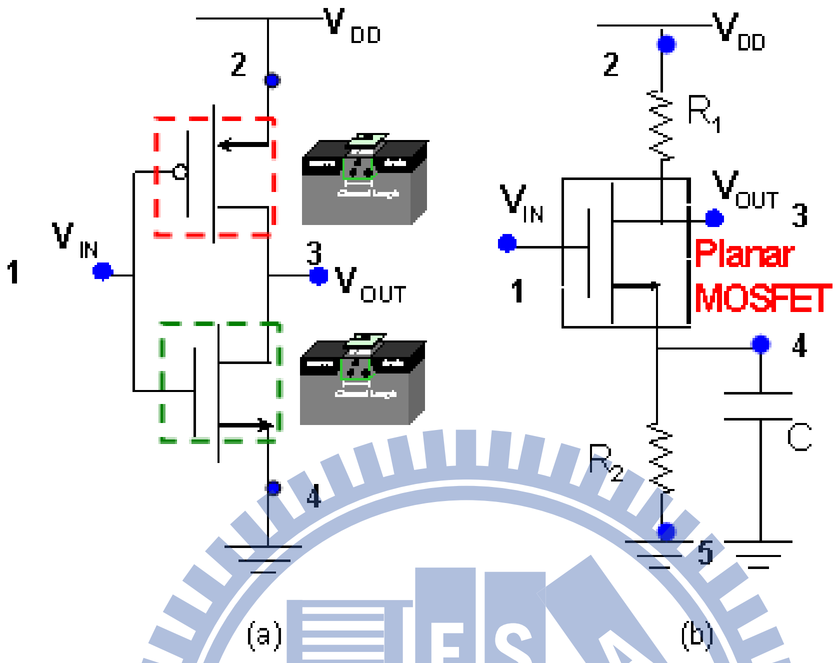


Figure 6.2: The (a) inverter circuit and (b) common source amplifier circuits as examples for digital and analog/high-frequency characteristics fluctuation exploration.

and device equations), which are solved simultaneously to obtain the circuit characteristics. The device characteristics, such as distributions of potential and current density, obtained by device simulation are input in the circuit simulation through device contacts. The effect of discrete dopants in the transistor on circuit characteristics is thus properly estimated.

The time domain coupled device-circuit simulation chart is shown in Fig. 6.1. Figures 6.2(a) and 6.2(b) are the inverter circuit and common source amplifier circuits as examples for digital and analog/high-frequency characteristics fluctuation exploration. In coupled device-circuit simulation, the time dependent device transport equations are shown in below:

$$\Delta\phi = \frac{q}{\varepsilon_s}\left(n - p + N_D - N_A\right), \tag{6.1}$$

$$\frac{\partial n}{\partial t} + \nabla \cdot \left(\mu_n n \nabla \left(\phi - \frac{KT}{q}\log\left(\frac{n}{n_i}\right) + \gamma_n\right)\right) + R = 0, \tag{6.2}$$

$$\frac{\partial p}{\partial t} - \nabla \cdot \left(\mu_p p \nabla \left(\phi - \frac{KT}{q}\log\left(\frac{p}{n_i}\right) + \gamma_p\right)\right) + R = 0, \tag{6.3}$$

and

$$\gamma_n = 2b_n\frac{\nabla^2\sqrt{n}}{\sqrt{n}}; b_n = \frac{\hbar^2}{12qm_n^*}; \gamma_p = 2b_p\frac{\nabla^2\sqrt{p}}{\sqrt{p}}; b_p = \frac{\hbar^2}{12qm_p^*}, \tag{6.4}$$

The above equations represent the Poisson equation, current continuity equation for electron, current continuity equation for hole, and quantum corrected equation for electron and hole. ϕ, n, p, t, and T are the electrostatic potential, electron densities, hole densities, time, and temperature to be solved, respectively. ε_s is the silicon permittivity, 1.05×10^{-10} F/m. q is the elementary charge, 1.06×10^{-19} Coulombs. k_B is Boltzmann constant, 8.6174 $\times10^{-15}$ eV/K. R, μ_n, and μ_p are the net electron-hole recombination rate, electron and hole mobilities. N_D and N_A are the number of ionized donors and acceptors, respectively. γ_n and γ_p are the quantum potential for electrons and holes. b_n and b_p are density-gradient coefficient for electrons and holes. $\hbar$ is the reduced Planck constant. m_n^* and m_p^* are the effective mass for the electrons and holes. The following equations express the circuit nodal equations (node 1 to node 2) for a inverter circuit, as shown in Fig. 6.2(a).

$$\mathrm{Node1 : V_1 = V_G,} \tag{6.5}$$

$$\mathrm{Node2 : V_2 = V_{DD},} \tag{6.6}$$

$$\mathrm{Node3 : I_{D,PMOS} = I_{D,NMOS},} \tag{6.7}$$

and

$$\mathrm{Node4 : V_4 = 0.} \tag{6.8}$$

After solving the device transport equation, the device and circuit equations are coupled and solved simultaneously to obtain circuit characteristics. The coupled device-circuit simulation approach directly transfers the device characteristics to circuit and connecting the device physics with circuit characteristics. The following shows the nodal equations of Fig. 6.2(b).

$$\mathrm{Node1 : V_1 = V_{in},} \tag{6.9}$$

$$\mathrm{Node2 : V_2 = V_{DD},} \tag{6.10}$$

$$\mathrm{Node3 : V_3 = V_{DD} - I_D R_1,} \tag{6.11}$$

$$\mathrm{Node4 : \frac{V_4}{R_2} + C\frac{dV_4}{dt} = I_D,} \tag{6.12}$$

and

$$\mathrm{Node5} : \mathrm{V}_5 = 0. \tag{6.13}$$

The coupled device-circuit simulation is beneficial in studying of nanoscale transistor circuits. Moreover, the simulation results may be further used for the construction reliable compact model including variability issues. Since the physical and mathematic accuracy of large-scale statistical methodology are verified, it's believed the given simulation approach can use for devices and circuits characterization and optimization.

6.2 Digital Circuits

The inverter circuit with planar MOSFETs circuit is first explored to illustrate the details of random-dopant-fluctuation in high-frequency integrated circuits. Then the comparison between FinFETs and planar devices circuit performance is drawn. Figure 6.3(a) shows the voltage transfer curves for the 16-nm-gate planar CMOS inverters with discrete dopants. Two points on the voltage transfer curve determine the noise margins of the inverter. These are the maximum permitted logic ”0” at the input, V_{IL}, and the minimum permitted logic ”1” at the input, V_{IH}. The two points on the voltage transfer curve are defined as those values of V_{in} where the incremental gain is unity; the slope is -1 V/V. The nominal value and fluctuations of the V_{IL} and V_{IH} are shown in the insets of Fig. 6.3(a). σV_{IL} exceeds

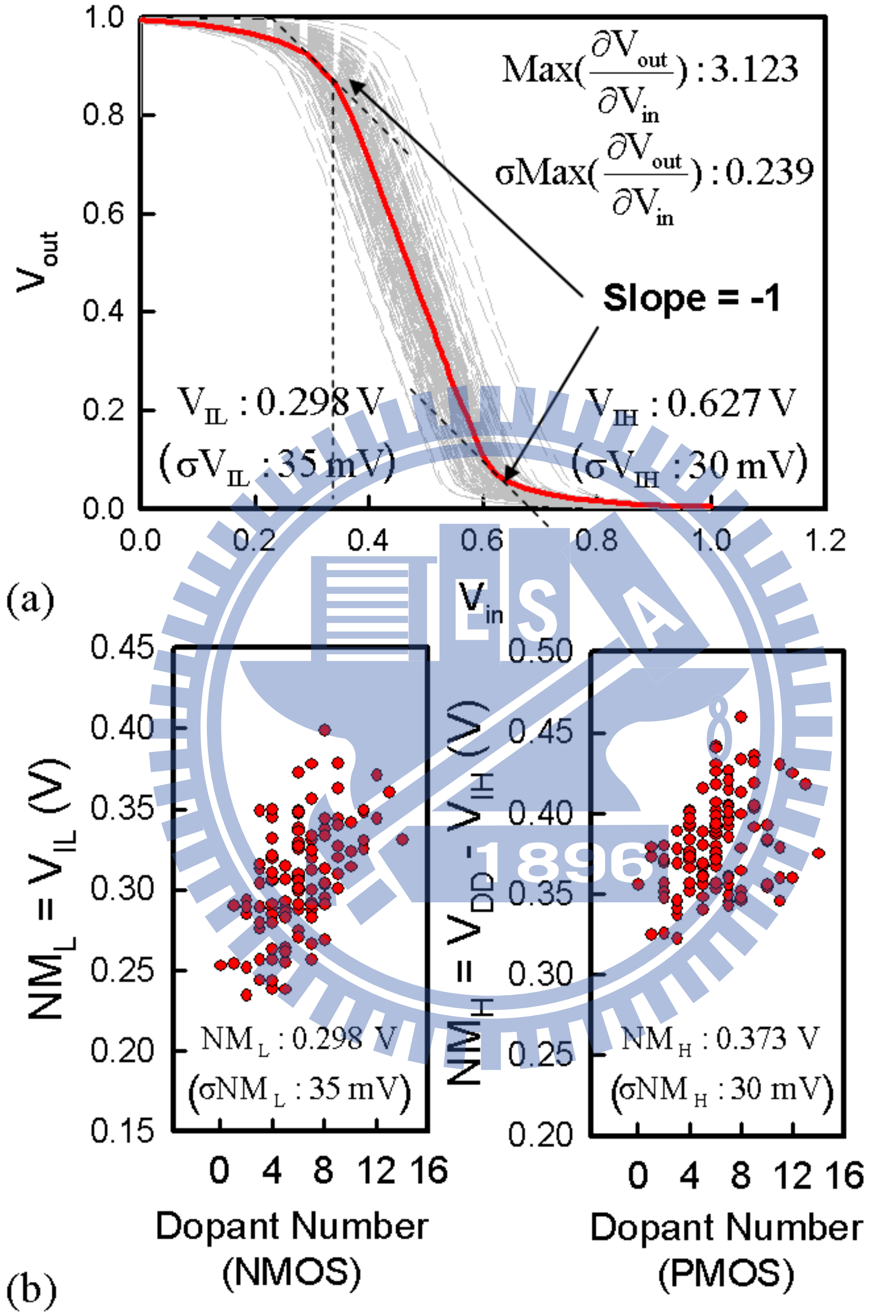


Figure 6.3: (a) The voltage transfer curves for the studied 16-nm-gate planar MOSFET circuit. (b) The noise margins, NM_L and NM_H, as a function of the dopant number in the NMOSFET and PMOSFET.

σV_{IH} because the σV_{th} of NMOSFETs exceeds that of PMOSFETs. The maximum slope of the voltage transfer curve indicates the maximum voltage gain of the inverter. The 7% of normalized voltage gain fluctuation of the inverter is therefore estimated, as shown in the inset of Fig. 6.3(a). Figure 6.3(b) plots the noise margins for the logic ”0” and ”1”, NM_H and NM_L, as a function of the dopant number. The NM_H and NM_L are defined in insets. The NM_L is increased with the increasing dopant number in the NMOSFET due to the increased V_{th} of device. For the NM_H, as numbers of dopant in the PMOSFET increases, the increased V_{th} of device may decrease the V_{IH} of voltage transfer curve and thus increase the NM_H. We notice that even for cases with the same number of dopants within device channel, their noise margins are still quite different due to the different distribution of random dopants. The noise margins of the inverter circuit increases as dopant number increases; however, the fluctuations of the noise margins are also increased due to the more sources of fluctuation in device channel region.

Figure 6.4(a) presents the input and output signals; the solid line represents the nominal case (continuously doped channel with a channel doping concentration of 1.48×10^{18} cm^{-3}) and the dashed lines represent cases with discrete dopant fluctuations. The rise time (t_r), fall time (t_f), and hold time of the input signal are 2 ps, 2 ps, and 30 ps, respectively. Figures 6.4(b) and 6.4(c) display the zoom-in plots of the falling and rising transitions. The term t_r is the time required for the output voltage (V_{out}) to rise from 10% of the logic

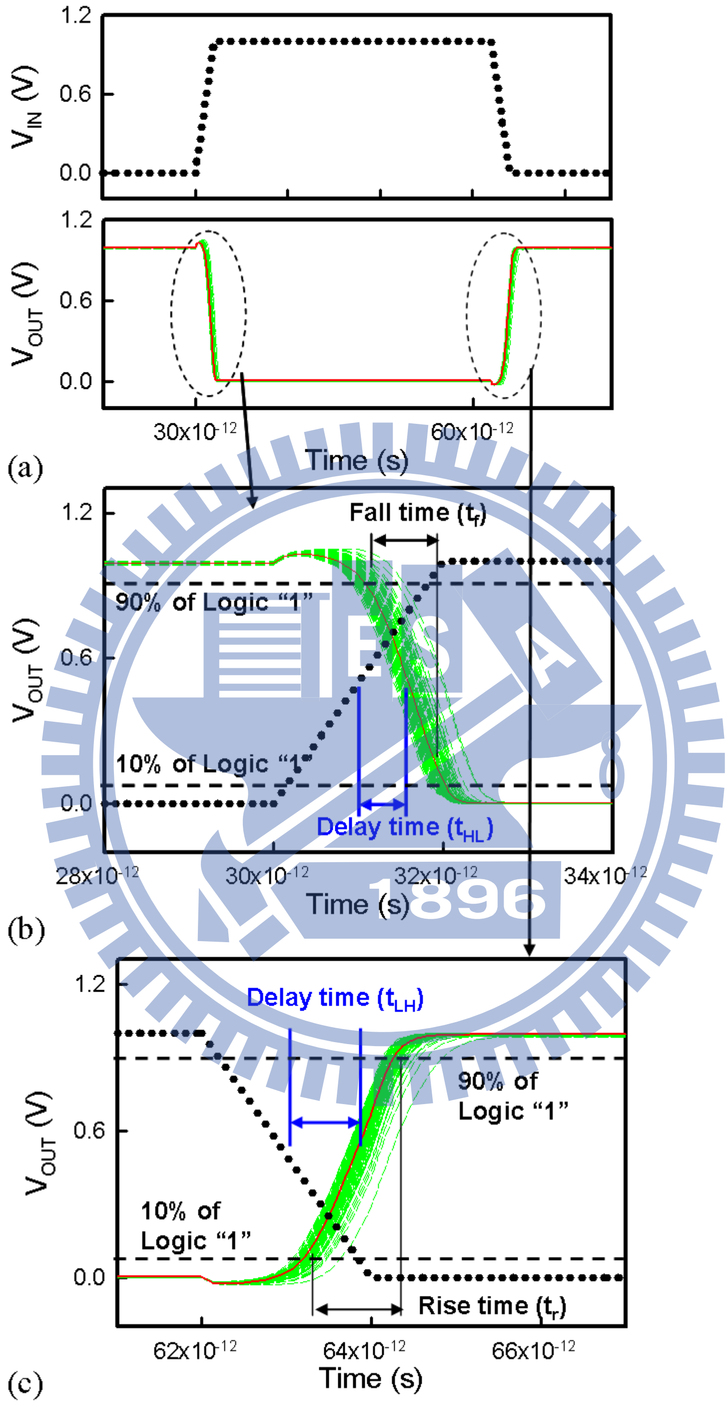


Figure 6.4: (a) The input and output signals for the discrete-dopant-fluctuated 16-nm-gate planar inverter circuit. The magnified plots show (b) the fall and (c) the rise transitions, where the rise time, fall time, high-to-low delay time, and low-to-high delay time are defined.

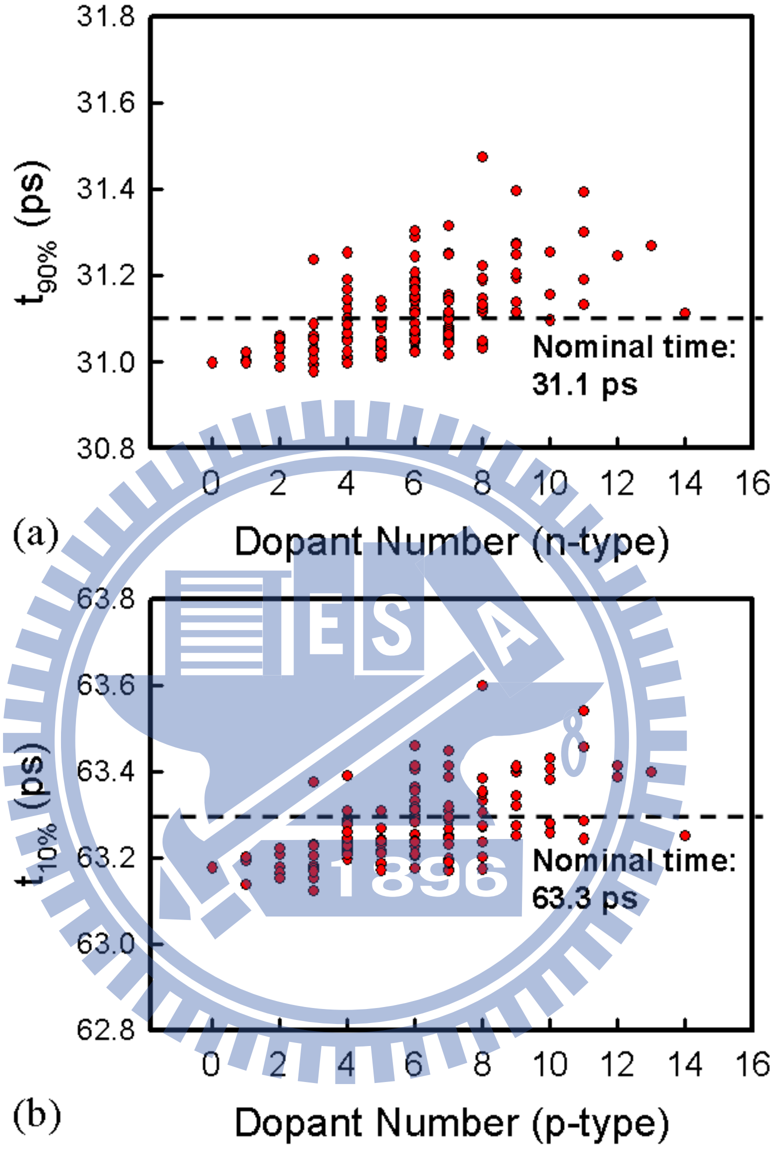


Figure 6.5: The fluctuations of (a) fall and (b) rise signal transition points as a function of dopant number in n-type and p-type MOSFETs for the discrete dopant fluctuated inverter circuits.

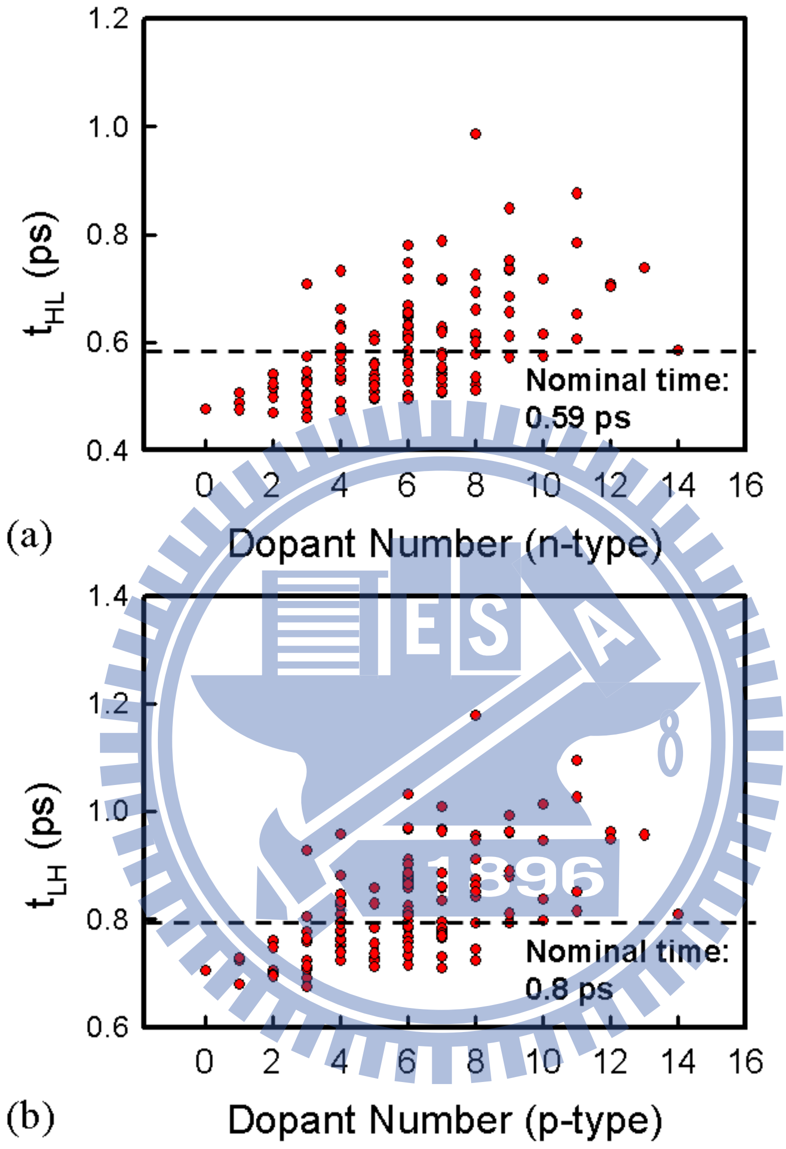


Figure 6.6: The fluctuations of (a) high-to-low and (b) low-to-high delay time as a function of dopant number in n-type and p-type MOSFETs for the discrete dopant fluctuated inverter circuits.

”1” level to 90% of the logic ”1”, and the t_f denotes the time required for the output voltage to fall from 90% of the logic ”1” level to 10% of the logic ”1” level. The low-to-high delay time and high-to-low delay time are defined as the difference between the times of the 50% points of the input and output signals during the rising and falling of the output signal, respectively. For the high-to-low transition, the NMOSFET is on and starts to discharge load capacitance, causing the output signal to transit from logic ”1” to logic ”0”. Similarly, for the low-to-high transition characteristics, the PMOSFET is turned on and starts to charge the load capacitance, causing the output voltage to transit from logic ”0” to logic ”1”. The 90% ($t_{90\%}$) and 10% ($t_{10\%}$) of the logic ”1” level are defined as starting points for the high-to-low and low to-high transition and plotted in Figs. 6.5(a) and 6.5(b), respectively. During the high-to-low signal transition, the output signal falls as the NMOSFETs is turned on. Therefore, the fluctuation of the starting points for high-to-low signal transition is determined by the V_{th} of the NMOSFET. With the increasing number of dopants in NMOSFET, the increased V_{th} delays the starting point of signal transition ($t_{90\%}$) and increases the high-to-low delay time, as shown in Fig. 6.6(a). Similarly, the starting point of low to-high transition (the time of 10% of the logic ”1” level) is influenced by V_{th} of PMOSFET and increased as numbers of dopants in PMOSFET, as shown in Fig. 6.5(b). Figures 6.6(a) and 6.6(b) plot the high-to-low delay time and low-to-high delay time for the planar inverter circuits with discrete dopants, respectively. Since the

Table 6.1: Transition time variation for the 16-nm-gate planar inverter circuits. (* normalized by the nominal value)

(unit: ps)	t_r	t_f	t_{LH}	t_{HL}
Nominal	1.021	0.897	0.800	0.590
Fluctuation	0.036	0.021	0.105	0.108
Normalized Fluctuation*	3.5%	2.4%	13.2%	18.3%
Normalized Maximum Fluctuation*	23.2%	12.3%	73.5%	101.8%

delay time is dependent on the start of the signal transition, the t_{HL} and t_{LH} are increased as channel dopant number increases. Notably, even with the same dopant number inside the channel, the delay time can still vary significantly. Take the cases of six dopants inside the NMOSFETs as an example; the maximum t_{HL} difference is about 0.3 ps, where the nominal t_{HL} is 0.59 ps. We refer to this effect as discrete-dopant-position-induced fluctuation. The magnitude of discrete-dopant-position-induced fluctuations increases as dopant number increases because of the increasing number of fluctuation sources (dopants).

Table 6.1 summarized the normalized timing characteristic fluctuations (the standard deviation / nominal value × 100%). For the 16-nm-gate CMOS inverter, as the number of discrete dopants varies from zero to 14, fluctuations of t_r, t_f, t_{LH}, and t_{HL}, of 0.036, 0.021, 0.105, and 0.108 ps respectively, may occur. The normalized fluctuation for t_r, t_f, t_{LH}, and t_{HL} are 3.5%, 2.4%, 13.2%, and 18.3%, respectively. The delay time fluctuations dominate the timing characteristics. The normalized maximum fluctuations (the maximum

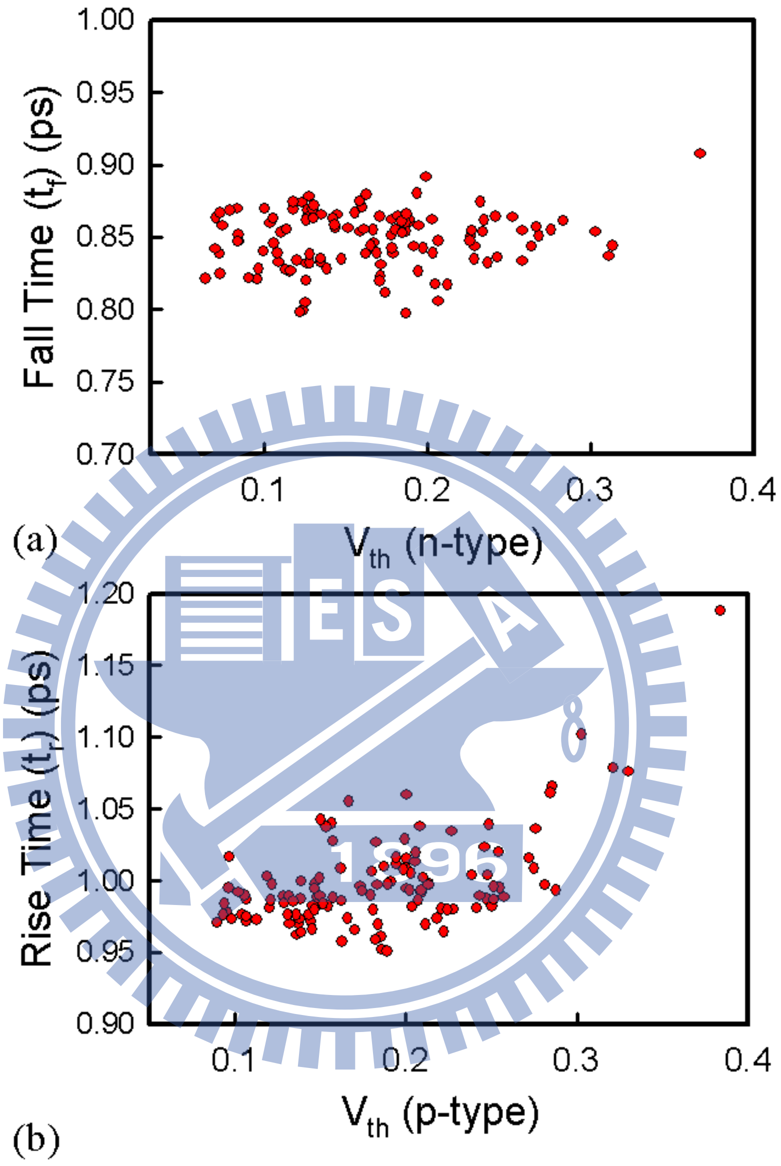
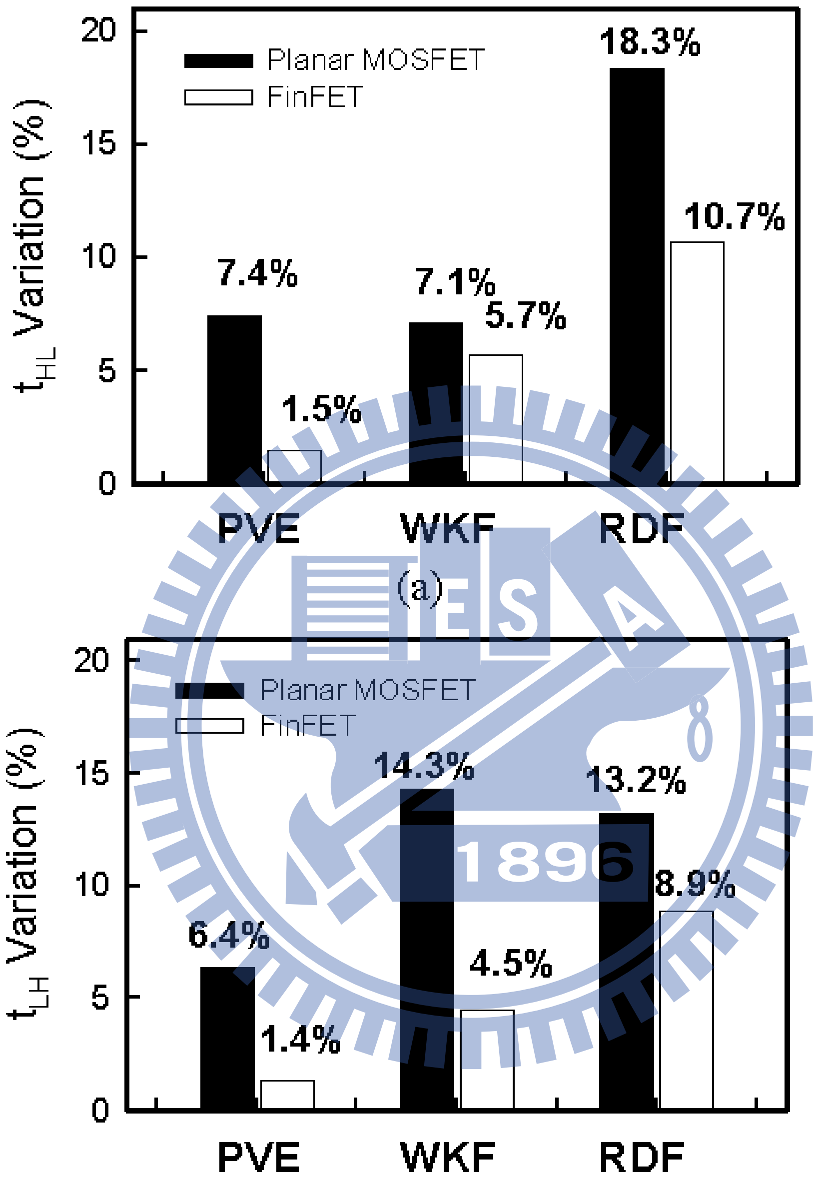


Figure 6.7: The fluctuations of (a) the fall and (b) rise time as a function of the threshold voltage in the n-type and p-type MOSFETs for the discrete-dopant-fluctuated CMOS inverters.

variation of time / nominal value × 100%) of the low-to-high and high-to-low delay times are about 73.5% and 101.8%. Notably, the maximum and minimum delays associated with this specific set of 125 randomized channels would vary such that their range would increase, as the number of samples increased. For the high-to-low signal transition of the output signal, the delay time is dominated by the starting points of the signal transition and then controlled by the on/off state of the NMOSFETs in the inverter planar circuit. Therefore, the fluctuation of the threshold voltage of NMOSFETs substantially affects the high-to-low delay time characteristic. Similarly, the low-to-high delay time fluctuation is strongly influenced by the σV_{th} of PMOSFETs. σt_{HL} exceeds σt_{LH} because the σV_{th} of NMOSFETs exceeds that of PMOSFETs. The rise/fall time fluctuations depend on the charge/discharge capability of the PMOSFETs/ NMOSFETs. Therefore, σt_r exceeds the σt_f because the driving capability of PMOSFETs is weaker than that of NMOSFETs in the given device dimensions scenario. The device with larger driving capability requires less time to charge and discharge a given load capacitance and so exhibits a less fall time fluctuations. Figures 6.7(a) and 6.7(b) show the fall time and rise time as a function of the threshold voltage for NMOSFETs and PMOSFETs, respectively. The fall time is dependent on the discharge capability of the NMOSFETs, and the rise time is dependent on the charge capability of the PMOSFETs. As the threshold voltages of the NMOSFETs and PMOSFETs are increased, the discharge and charge ability for given values of t_f and

t_r decrease. Therefore, the time required for the fall and rise transitions increases. The trend for t_f is not clear because herein only the transistors gate capacitance was used as the load capacitance. The small load capacitance and strong driving capability of NMOSFETs make the trend of t_f fluctuation insignificant. Notably, the rise and fall time fluctuations generally may not be as important as the delay time fluctuation in circuit timing; however, their maximum variations can exceed 0.237 and 0.110 ps, respectively, which exceed the delay time fluctuation and should therefore be considered in statistical timing analysis in circuit and system design. Moreover, fluctuations in the rise and fall time can be added to the delay time, and increasing the delay time fluctuations.

Figure 6.8(a) and 6.8(b) compare the high-to-low delay time (t_{HL}) and low-to-high delay time (t_{LH}) for the planar MOSFETs and FinFET devices. Since the t_{HL} and t_{LH} are dependent on the V_{th} fluctuations for NMOSFET and PMOSFET, respectively, according to the results of Fig. 5.3, the RDF and WKF are the dominating factors in timing fluctuations and WKF introduces a largest t_{LH} fluctuation due to the large workfunction deviation in scaled gate area as shown in Fig. 5.3(b). The WKF has shown its increasing importance in nanoscale transistor, especially in PMOSFET characteristics. Figure 6.9 estimates the power for the studied transistors. The total power (P_{total}) is consisting of the dynamic power (P_{dyn}), the short circuit power (P_{sc}), the static power (P_{stat}). Their definitions are



(a)

(b)

Figure 6.8: Comparison of the variations of (a) t_{HL} and (b) t_{LH} with respect to WKF, PVE, and RDF for the planar MOSFETs and FinFETs.

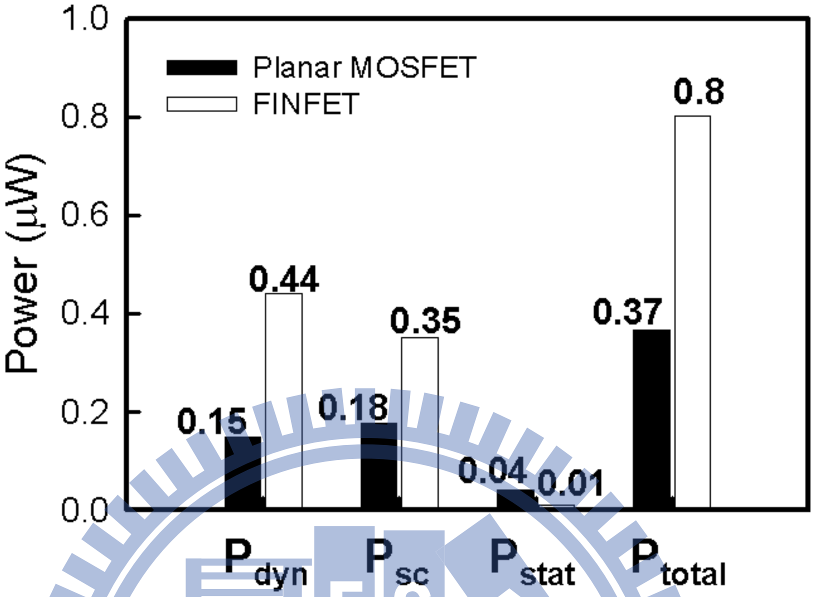


Figure 6.9: The nominal power for the bulk planar MOSFET and SOI FinFET inverter circuits.

shown in below.

$$P_{dyn} = C_{load} V_{dd}^2 f_{0->1} \tag{6.14}$$

$$P_{sc} = f_{0->1} V_{DD} \int_T I_{sc}(\tau) d\tau \tag{6.15}$$

, and

$$P_{stat} = V_{DD} I_{leakage} \tag{6.16}$$

The $f_{0->1}$ is the clock rate. I_{sc} is the short circuit current, which is observed as both NMOSFET and PMOSFET turned on resulting a DC path between the power rails. T is the switching period. $I_{leakage}$ is the leakage current that flows between the power rails in the absence of switching activity. As plotted in Fig. 6.9, the SOI FinFETs show larger dynamic power dissipation due to its larger load capacitance than that of planar MOSFETs. The short circuit power is determined by the time of existence of DC path between the power rails and the short circuit current. Since the V_{th} for the explored devices are calibrated, the P_{sc} is then determined by the I_{sc}. The I_{sc} is dependent on the saturation current of the devices. Since the SOI FinFET maintains a larger driving current than the planar MOSFETs, the larger short circuit power dissipation of SOI FinFETs is larger than that of the planar devices. As for the static power consumption, the SOI FinFET shows a smaller P_{stat} than the planar MOSFETs due to the smaller leakage current resulting from the better channel controllability. Notably, the P_{dyn} and P_{sc} are the dominating factors in power dissipation.

Figure 6.10(a) shows the dynamic power fluctuation (σP_{dyn}) for bulk planar MOSFET and SOI FinFET inverter circuits with WKF, PVE, and RDF. The dynamic power fluctuation of the SOI FinFETs is significantly larger than that of planar MOSFETs due to the larger gate capacitance fluctuation as aforementioned, Fig. 5.6. The RDF and PVE dominate the dynamic power fluctuation; additionally, the WKF shows less impact due to the smaller gate capacitance fluctuations. Figure 6.10(b) displays the short circuit power fluctuations (σP_{sc}) for the studied inverter circuits. Different to the results of σP_{dyn}, the SOI

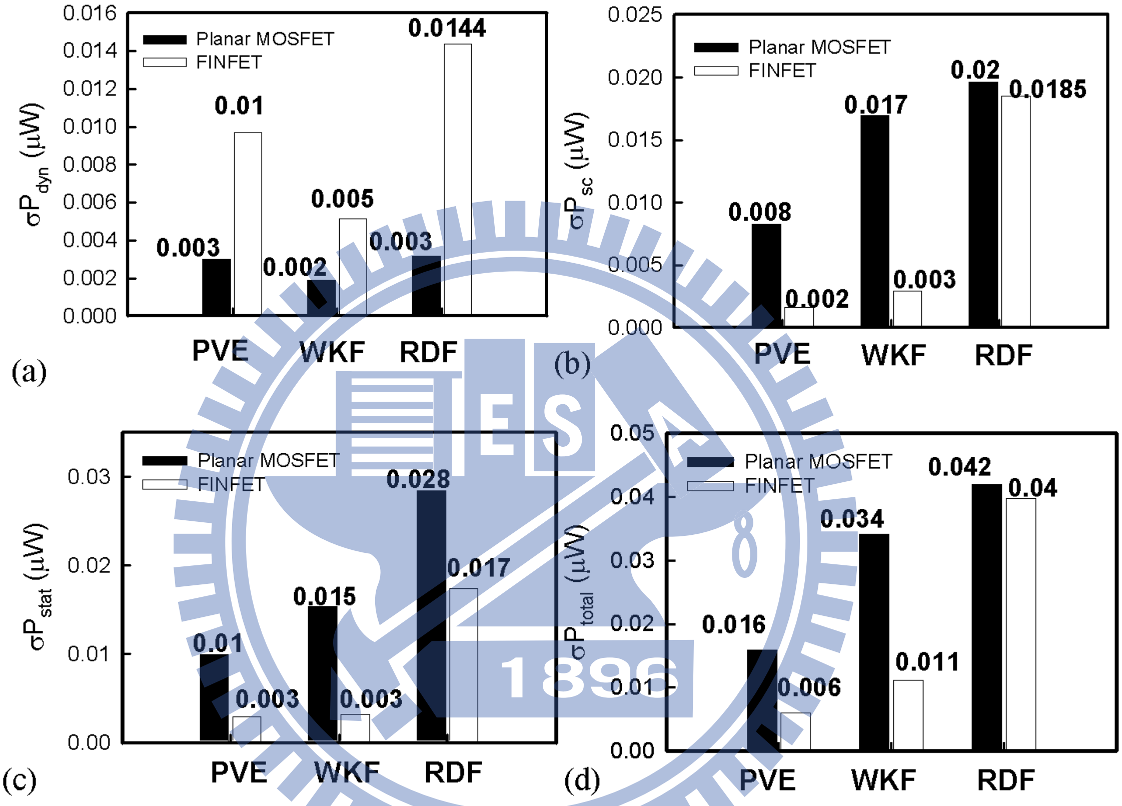


Figure 6.10: The (a) dynamic power, (b) short-circuit power, (c) static power, and (d) total power fluctuations for the explored devices with WKF, PVE, and RDF.

FinFETs exhibits a smaller short circuit power fluctuation because of the smaller V_{th}. The WKF starts to play an important role in P_{sc} of planar MOSFETs because of the significant σV_{th} induced by workfunction fluctuation. Figure 6.10(c) summarizes the static power fluctuations (σP_{stat}). Since the static power fluctuation is related to the device leakage current fluctuation, the RDF dominants the σP_{stat} due to the induced larger σV_{th}. Notably, though the static power is not an important part in total power dissipation, the static power fluctuation may not be neglected in the total power fluctuation due to the exponential relationship between the leakage current and V_{th}. The total power fluctuations (σP_{total} = $[(\sigma P_{PVE})^2 + (\sigma P_{WKF})^2 + (\sigma P_{RDF})^2]^{0.5}$) are summarized in Fig. 6.10(d). The P_{stat} is one of the major sources of the power fluctuation and the RDF is the dominating factors in power fluctuation of planar MOSFETs. The SOI FinFETs exhibit a smaller total power fluctuation, 0.0419 W, than the planar MOSFETs, 0.0564 W. The total power fluctuation for the planar MOSFETs and SOI FinFETs are 15.2% (σP_{total} / P_{total} = 0.0564 / 0.37) and 5.2%, respectively, which may bring significant impacts on the reliability of circuits, such as temperature and timing.

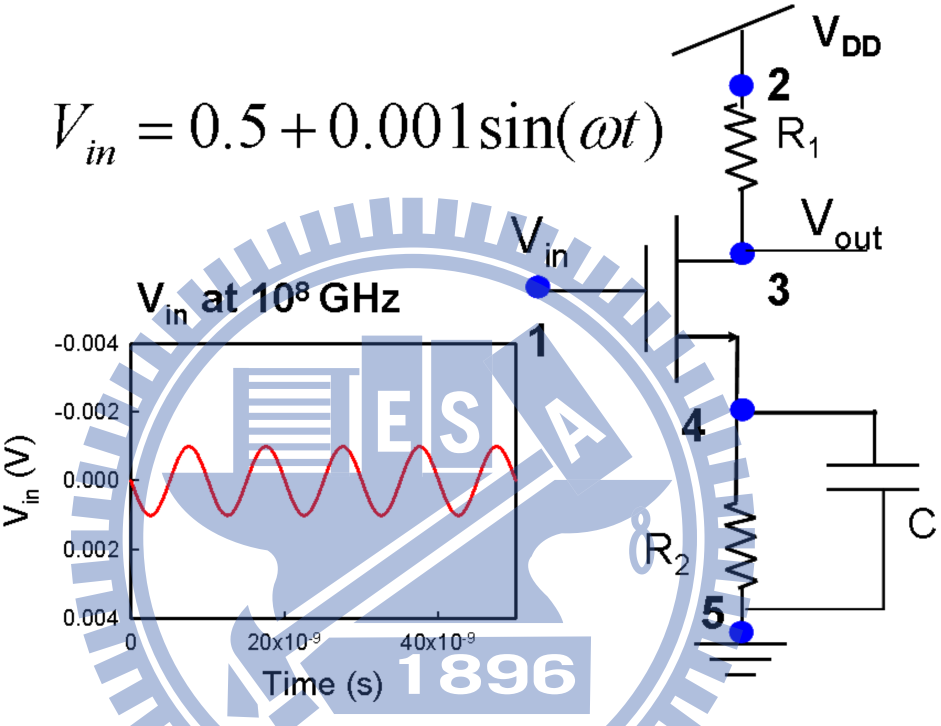


Figure 6.11: The common-source circuit is used as a tested circuit to explore the fluctuation of high-frequency characteristics. The input signal is a sinusoid input wave with 0.5 V offset. The frequency is sweep from 1×10^8 Hz to 1×10^{13} Hz.

6.3 Analog/High-Frequency Circuits

The common-source circuit with sinusoid input wave (offset is equal to 0.5 V), as shown in Fig. 6.11, is used as a tested circuit to explore the fluctuation of high-frequency characteristics. The time-domain simulation results are simultaneously used for the calculation of the property of the frequency response, where the frequency is sweep from 1×10^{8} Hz to 1×10^{13} Hz. The common-source amplifier circuit with planar MOSFETs circuit is first explored to illustrate the details of random-dopant-fluctuation in high-frequency integrated circuits.

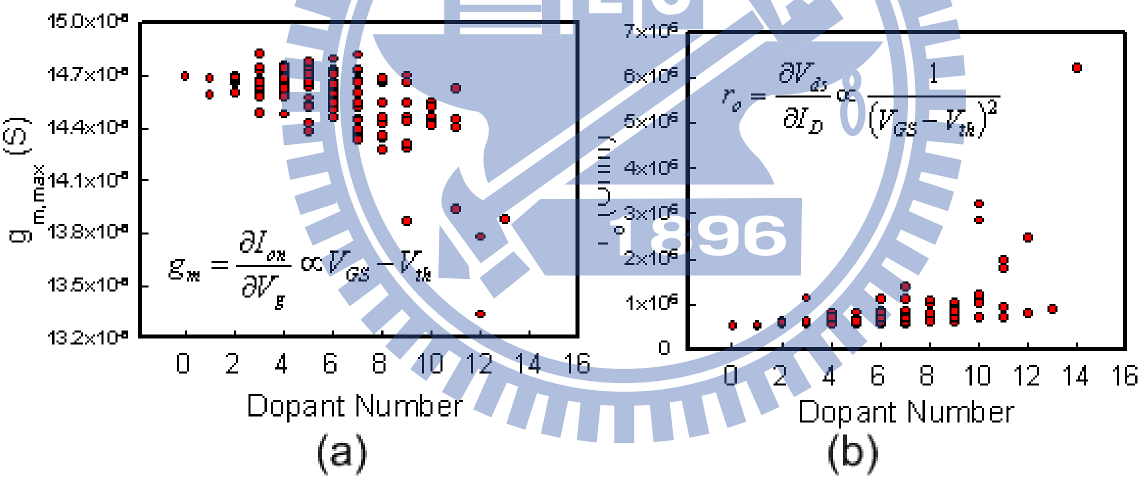


Figure 6.12: DC characteristic fluctuations of (a) $g_{m,max}$, and (b) r_o of the 125 discrete dopant fluctuated 16-nm-gate planar MOSFET. The definitions are shown in the insets.

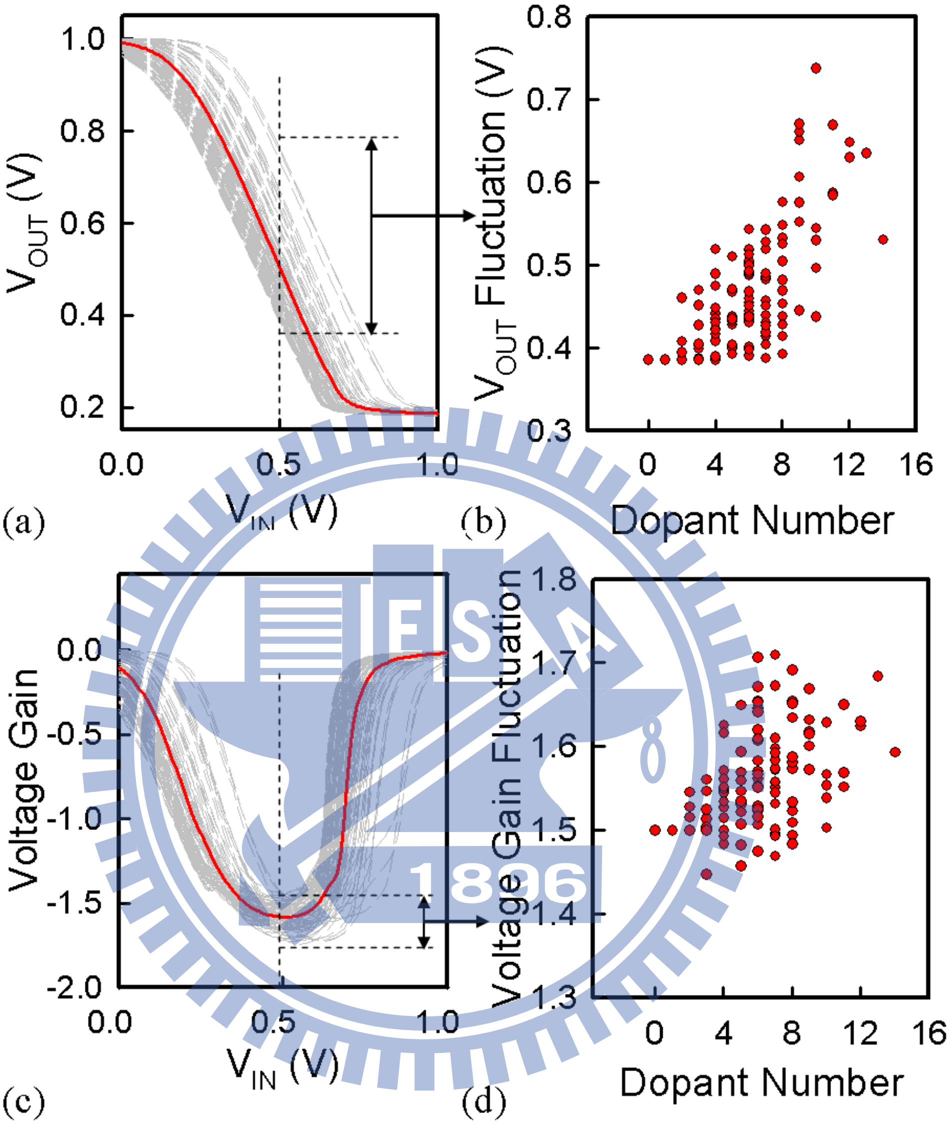


Figure 6.13: The (a) voltage-transfer-curve, (b) the output voltage, (c) the voltage gain, (d) and the fluctuation of voltage gain for the studied discrete-dopant-fluctuated 16-nm-gate common-source circuits. The solid line shows the capacitance of the nominal case (continuously doped channel with 1.48×10^{18} cm^{-3} doping concentration) and the dashed lines are the random-dopant-fluctuated devices.

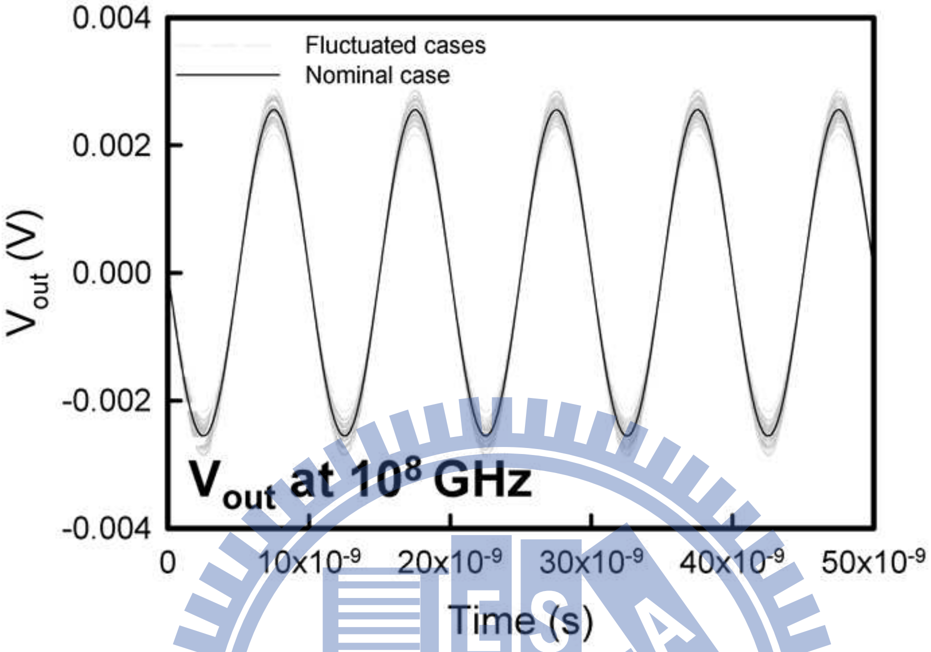
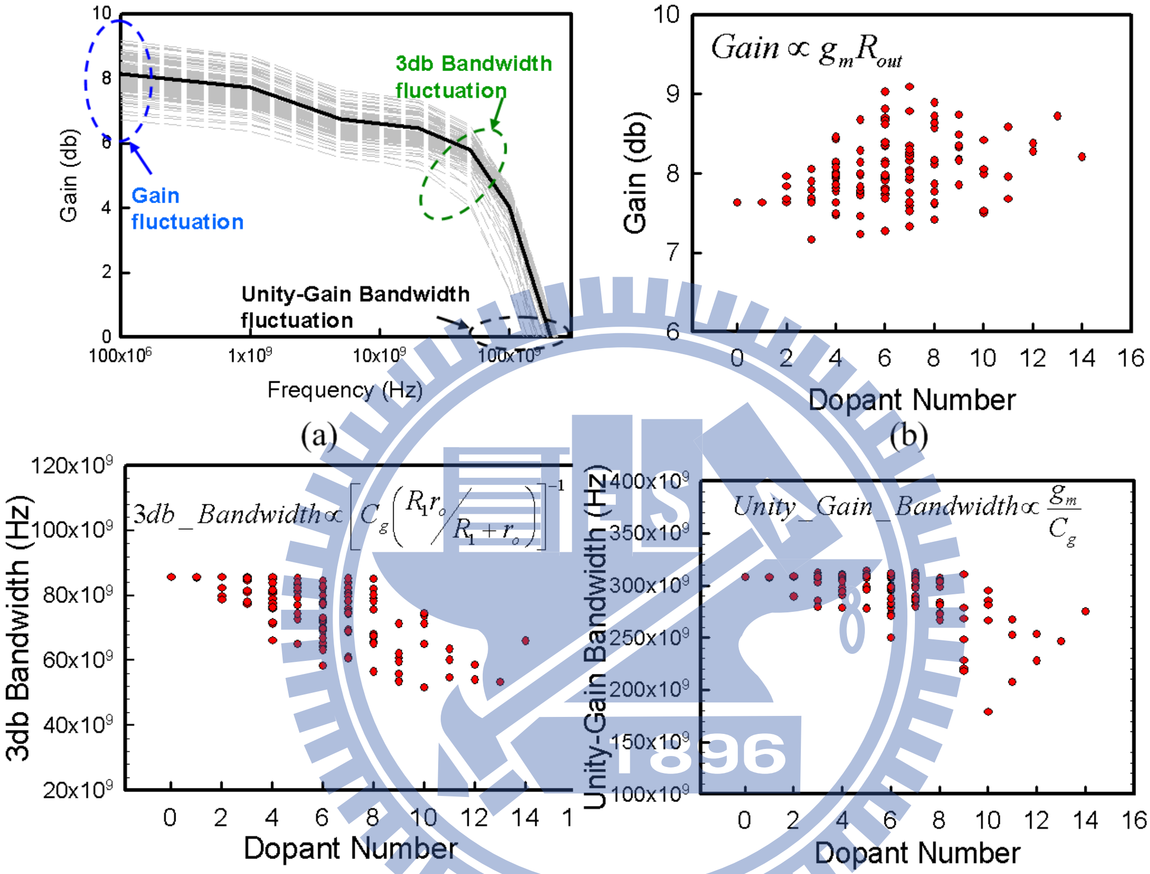


Figure 6.14: The output signal fluctuation of the discrete-dopant-fluctuated circuits at 10^8 Hz. The solid line is the nominal case and the dashed lines are transistors with discrete dopants.

Figures 6.12(a) and 6.12(b) are the maximum transconductance ($g_{m,max}$), and output resistance of transistor (r_o) with versus dopant number, where the expression of $g_{m,max}$ and the output resistance of transistor are shown in insets. Since the threshold voltage is increased with increasing channel doping concentration, according to the definition in insets of Figs. 6.12(a) and 6.12(b), $g_{m,max}$ is decreased and r_o is increased as the number of dopants is increased. The position of random dopants induced different fluctuation of characteristics in spite of the same number of dopants. Furthermore, the magnitude of the spread characteristics increases as the number of dopants increases. Figures 6.13(a) and 6.13(b) explore the voltage-transfer-curve (VTC) and corresponding output voltage (V_{out}) of the discrete-dopant-fluctuated 16-nm-gate planar MOSFET circuits, respectively. The derived voltage gain and its fluctuation of the studied circuit are shown in Figs. 6.13(c) and 6.13(d). The V_{out} is increased as the number of dopant in device channel is increased due to the decreasing output current and voltage drop across R_1. The variation of V_{out} will influence the capacitance of the studied MOSFETs and alters the high frequency response. Moreover, as expected, the fluctuations of V_{out} and voltage gain are increased as dopant number is increased. Beside the fluctuations of the nodal voltage of circuits, the output signal is also fluctuated. Without loss of generality, Fig. 6.14 plots the output signal of the discrete-dopant-fluctuation circuits at 10^8 Hz. The solid line is the nominal case and the dashed lines are transistors with discrete dopants. The output signal corresponds to the input signal plotted in Fig. 6.11. The discrete dopant fluctuation not only impacts the operation points of circuits, but also influences the magnitude of output signal.

Figure 6.15(a) shows the circuit gain versus operation frequency for all fluctuated cases, where the solid line shows the nominal case, whose channel doping profile is continuously doped with 1.48×10^{18} cm^{-3}. The circuit gain, 3dB bandwidth, and unity-gain bandwidth of the nominal case are 8.14 db, 68 GHz, and 281 GHz, respectively. The corresponding



(a) (b)

(c) (d)

Figure 6.15: The (a) frequency response, (b) high-frequency circuit gain, (c) 3dB bandwidth, (d) and unity-gain bandwidth fluctuations of the studied discrete-dopant-fluctuated 16-nm-gate common-source circuits.

high-frequency characteristic fluctuations for the explore circuit are explored, as shown in Figs. 6.15(b) - 6.15(d), where the insets show the trend of circuit gain, 3dB bandwidth, and unity-gain bandwidth as a function of device characteristic and circuit element. The gain of the studied circuit is proportional to transconductance multiplied by output resistance of circuit. The circuit output resistance, R_{out}, is given by

$$R_{out} = \left(\frac{I_{out}}{V_{out}} + \frac{1}{r_o} \right)^{-1}, \tag{6.17}$$

where I_{out} and V_{out} are the output current and voltage of the studied circuit. As the number of dopants in device channel is increased, the on-state current of transistor, which associated with the output current of the test circuit, is decreased and thus increases the output voltage of the circuit. Additionally, the output resistance of transistor, r_o, is increased with increasing threshold voltage. Therefore, the circuit output resistance, R_{out}, is increased as threshold voltage is increased. We notice that although the dependence of R_{out} and g_m on threshold voltage is opposed, the trend of circuit gain fluctuation is dominated the output resistance due to the square dependence of r_o on V_{GS}-V_{th}. Therefore, the trend of circuit gain fluctuation is dominated by the output resistance and increased as number of dopant is increased, as shown in Fig. 6.15(b). Figures 6.15(c) and 6.15(d) show the fluctuation of 3dB bandwidth and the unity-gain bandwidth of the nano-MOSFET circuit, which indicate the variations of switching speed nano-MOSFET circuit resulted from random discrete dopants. The insets of Figs. 6.15(c) and 6.15(d) show the main sources of variations contributed from device characteristics fluctuations, g_m, r_o, and C_g , as shown in Figs. 6.12. As the number of dopant in device channel is increased, the depletion width is decreased, and then increases the gate capacitance. The fluctuation of C_g accompanied with increasing r_o and decreasing g_m result in a decrement of 3dB bandwidth and the unity-gain bandwidth on increasing dopant number. Similar to the DC characteristic of device, the high-frequency characteristic fluctuation of the nanoscale MOSFET circuit is much more scattered as number of dopants is increased. The standard deviations of the gain, 3dB bandwidth, unity-gain bandwidth, and gain-bandwidth product are 0.46 dB, 9.63 GHz, 29.3 GHz, and 64.4 GHz, respectively. The high-frequency characteristic fluctuations of the tested circuit are summarized in Table 6.2. Both the discrete-dopant-induced DC and high-frequency characteristics fluctuations of 16-nm-gate MOSFET circuit have been studied using a 3D ”atomistic” simulation technique. Using the experimentally calibrated analyzing technique, the result have shown that the discrete-dopant fluctuated 16-nm-gate MOSFET circuit exhibits 5.7% variation of the circuit gain, 14.1% variation of the 3dB bandwidth and 10.4% variation of the unity-gain bandwidth.

Power-added efficiency (PAE), defined in below, is a measure for the power conversion

Table 6.2: Summarized high-frequency characteristic fluctuations of the nano-MOSFETs circuit.

	Gain (dB)	3dB bandwidth (Hz)	Unity-gain bandwidth (Hz)
Nominal	8.138	6.84×10^{10}	2.81×10^{11}
Nominal	0.465	9.63×10^{9}	2.93×10^{10}
Nominal	0.057	0.141	0.104

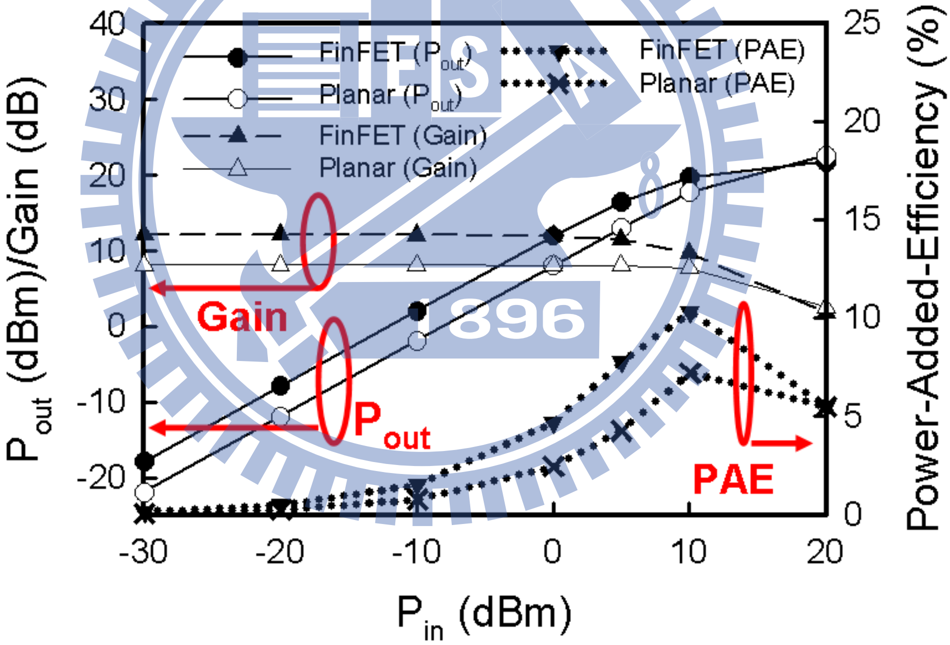
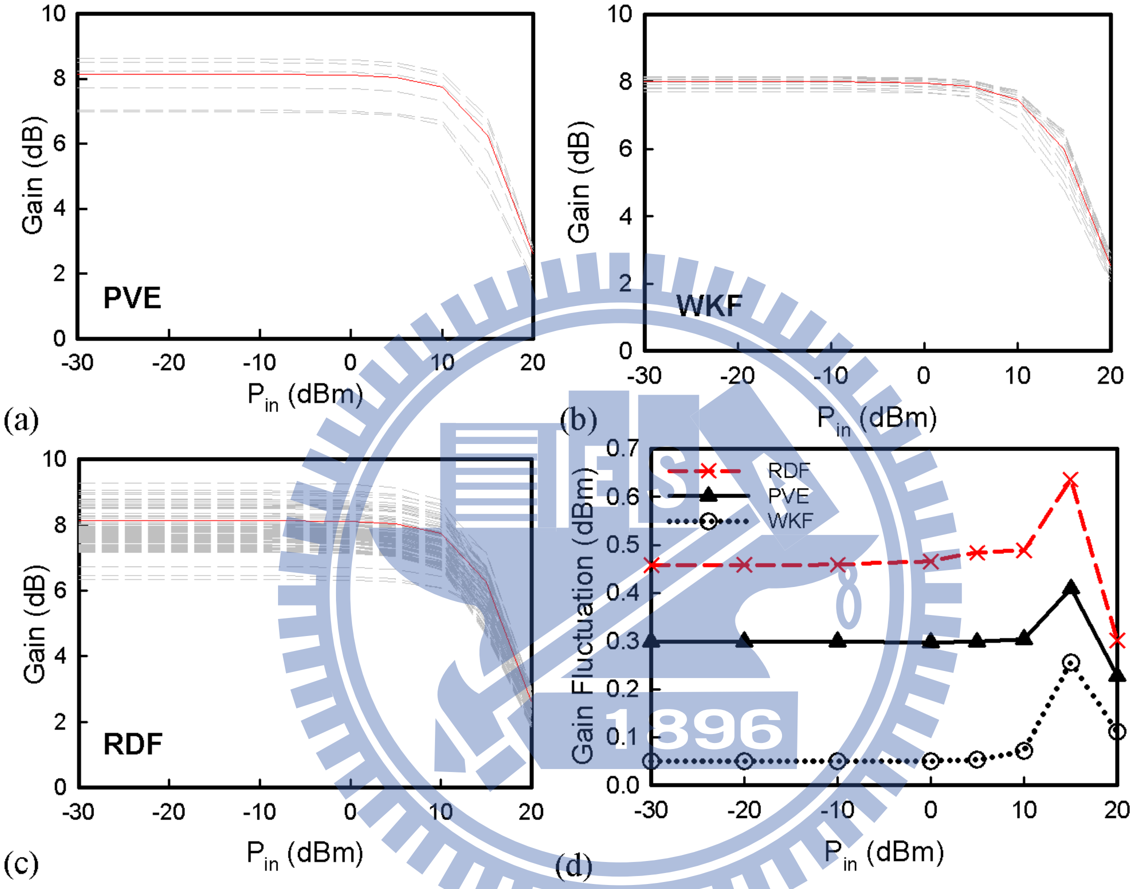


Figure 6.16: Output power, circuit gain, and power-added-efficiency of the explored devices as a function of input power.



(a) (b) (c) (d)

Figure 6.17: The circuit gain characteristics of the planar MOSFETs with (a)PVE, (b)WKF, and (c)RDF fluctuations, respectively. (d) The summarized circuit fluctuations.

efficiency of power amplifiers.

$$PAE\,(\%) = \left(\left(P_{out} - P_{in}\right)/P_{DC}\right) \times 100\% \tag{6.18}$$

where P_{out}, P_{in} and P_{DC} are output, input and DC supplied power, respectively. Figure 6.16 presents the nominal output power, circuit gain, and power-added-efficiency of the common-source power amplifier as a function input power. A sinusoid input wave with 0.5 V offset voltage is used as input signal. The device channel is continuously doped and the operation frequency is 10^8Hz. Owing to the limitation of output signal swing, the nominal value of P_{out} is saturated after 10 dBm input power, which in turn decreases the gain of circuit. The gain fluctuations of the planar MOSFETs resulted from WKF, PVE, and RDF are explored in Figs. 6.17(a)- 6.17(d). Since the PVE and RDF dominate gate capacitance fluctuations due to significant affected the channel length and depletion region, the PVE and RDF play important roles in high frequency characteristic fluctuation, as shown in Fig. 6.17(d). Effects of WKF in high frequency characteristics may be neglected in this scenario. Since the input signal is a sinusoid wave, the device may operate in different operation region if the amplitude of sinusoid wave large enough. The enlarged gain fluctuation with increasing input power is resulted from the larger portion of device operation in linear region. While the magnitude of input signal swing increases larger than 0.178 V (input power larger than 15 dBm), some part of device operation enters cutoff region and therefore decreases the gain fluctuation. The high frequency characteristic fluctuations are then investigated in Fig. 6.18(a), in which the fluctuation of high frequency circuit gain, 3dB bandwidth, and unity-gain bandwidth are extracted, Figs. 6.18(b)- 6.18(d). Similar to the result of Figs. 5.7 and 5.8, the RDF and PVE dominates the high frequency characteristic fluctuations and WKF become less important in this analyzing skeleton.

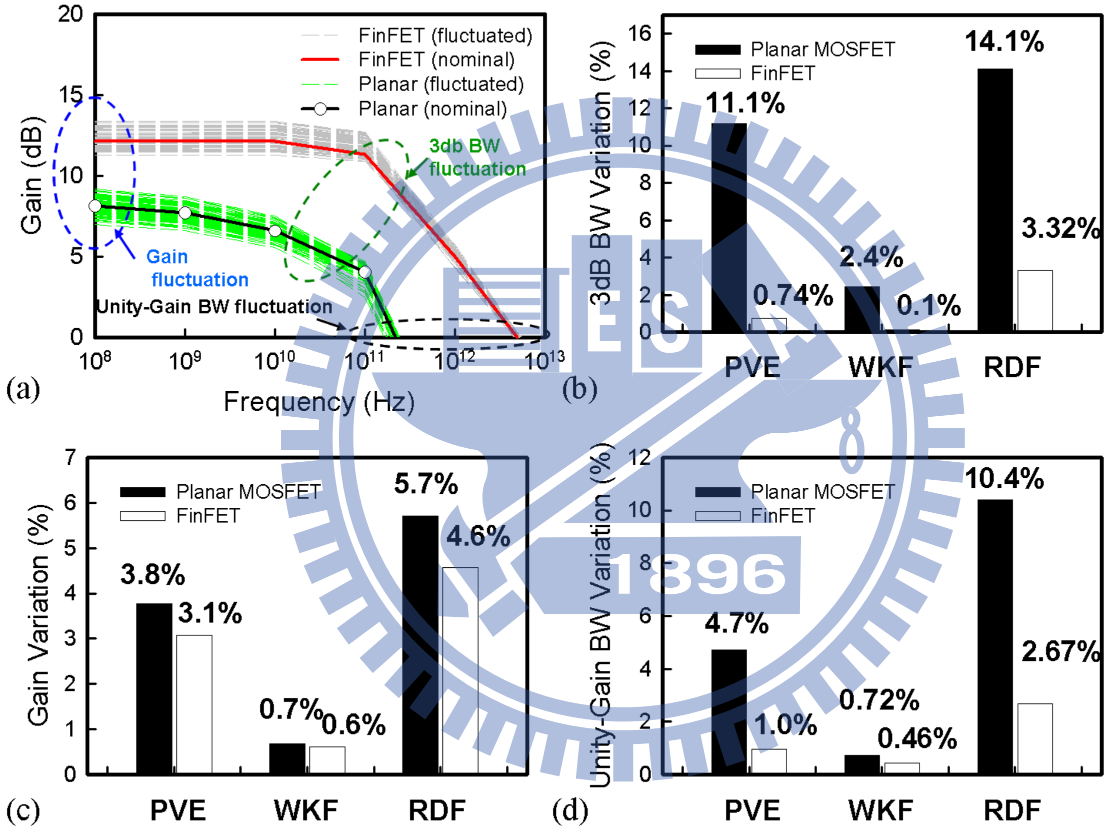


Figure 6.18: (a) The frequency response of the planar MOSFET and FinFET common-source amplifiers, in which (b) 3dB bandwidth, (c) gain, and (d) unity-gain bandwidth are extracted.

6.4 Summary

This chapter have estimated the influences of the intrinsic parameter fluctuations in 16-nm nanoscale circuits. The WKF and RDF dominate the device threshold voltage fluctuation; and therefore impact the timing and static noise margin of the explored digital inverter and SRAM circuits. The fluctuations of delay time and static noise margin depend on the V_{th} fluctuation which follows the trend of V_{th} fluctuation. The WKF effect in PMOSFETs may bring significant impact on t_{LH} characteristics due to the large difference of workfunction in different grain orientation. The power fluctuations consisting of dynamic power, short circuit power, and static power were estimated. The total power fluctuation for the planar MOSFETs and SOI FinFETs are 15.2% and 5.2%, respectively, which may induce significant performance uncertainties, such as temperature and timing, to degrade the reliability of circuits and systems. The dynamic power and short circuit power are the most important power dissipation sources. However, the static power fluctuation dominates the total power fluctuation due to the exponential relationship between the leakage current and the V_{th}. The significant leakage power fluctuation was further investigated, which should be considered in robust circuit and system design. It has been found that under the same layout area, the SOI FinFETs shows a larger delay and power consumption due to the large gate capacitance; however, their delay and power fluctuations are significantly suppressed because of the better channel controllability of vertical channel structure. For the high-frequency characteristics, the circuit gain, power, and power-added efficiency were also explored. Similar to the trend of the device cutoff frequency, the PVE and RDF dominate the device and circuits characteristic fluctuations and the WKF shows less impact on high-frequency characteristic owing to the small gate capacitance fluctuation. The sensitivities of circuit performance with respect to device parameter fluctuation have been reported. It is necessary to include both the WKF and RDF effects in studying digital circuit reliability; however, for the high frequency applications, the PVE and RDF effect are dominating factors. The extensive study has assessed the fluctuations on nano-CMOS circuit performance and reliability, which can in turn be used to optimize nano-CMOS circuits and systems.

Chapter 7

Conclusions and Future Work

7.1 Conclusion of This Study

The variability of performance and yield in various nanoscale transistors are great of interest and become crucial for circuit design. This thesis explores the characterization techniques for device variability and its impact on circuits. The mathematical device simulation accuracy is calibrated with full quantum mechanical simulation and the accuracy of large-scale statistical methodology is verified by experimental data. Intrinsic parameter fluctuations, consisting of workfunction fluctuation, random dopant fluctuation, and process variation effect are investigated and compared with planar MOSFETs. The vertical channel transistors, FinFETs and multiple-gate SOI FETs, present promising characteristics on fluctuation suppression. Consequently, the links should be established between circuit design and fundamental device technology to allow circuits and systems to accommodate the individual behavior of every transistor on a silicon chip.

7.2 Suggestions on the Suppression Approaches

Channel engineering technique has been known to be an effective way to suppress the random-dopant-induced characteristic fluctuation11 [64,66,67]. We have examined the effectiveness of the vertical and lateral direction doping profile engineering on suppression of DC and high frequency characteristics. We herein demonstrate the doping profile engineering to suppress the RDF in 16-nm-gate planar MOSFETs.

7.2.1 Vertical Doping Profile Engineering

Discrete dopants located near the channel surface induce potential barriers and disturb the current conducting path. Therefore, the idea of vertical doping profile engineering is to leave dopants away from the channel surface and reduce the fluctuation. Figure 7.1(a) illustrates the vertical doping profile engineering, where the doping profile along the longitudinal diffusion direction from surface to substrate follows the normal distribution. Both the mean position and the three sigma of this distribution are eight nanometers, which can

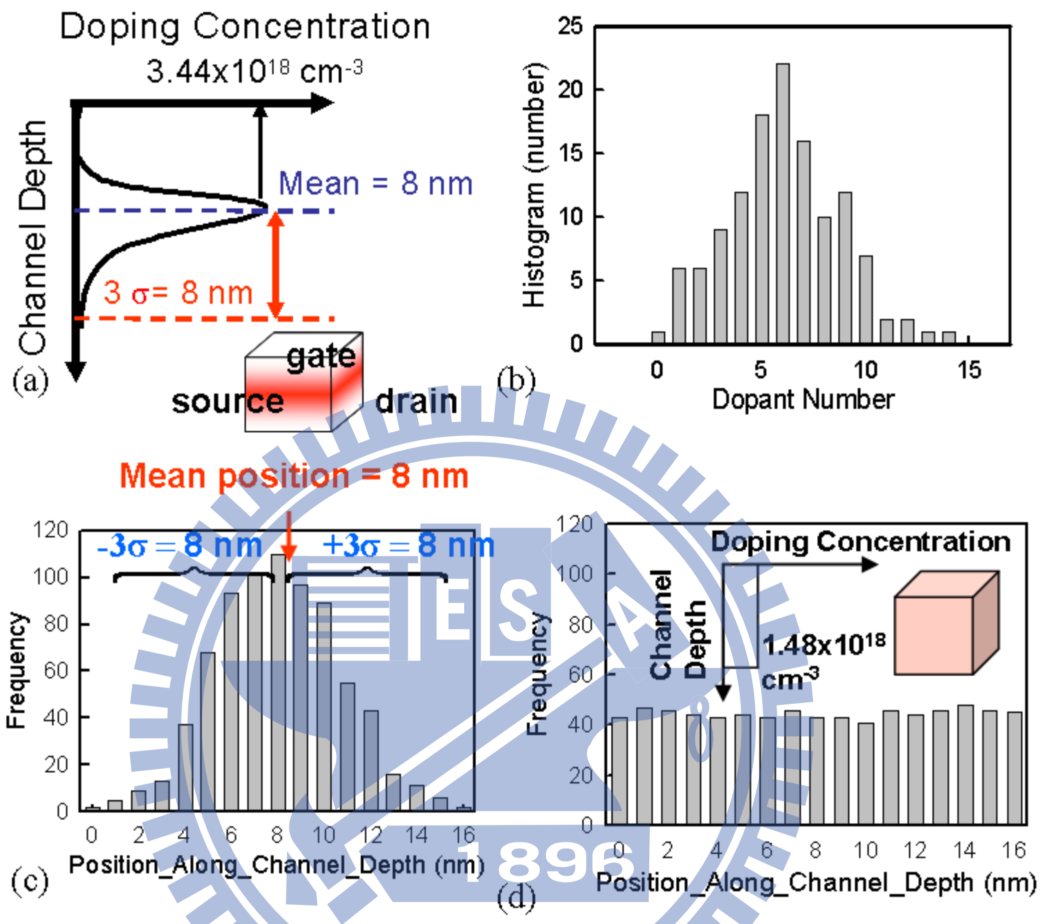


Figure 7.1: There will be 758 dopants are within a large rectangular solid, in which the equivalent doping concentration is 1.48×10^{18} cm^{-3}). The dopant distribution in the direction of channel depth follows the normal distribution (a). Similarly, dopants within the (16 nm)^3 cubes may vary from zero to 14 (the average number is six) (b). The vertical dopant distribution of the vertical doping profile engineering and the original doping profile are shown in (c) and (d), respectively.

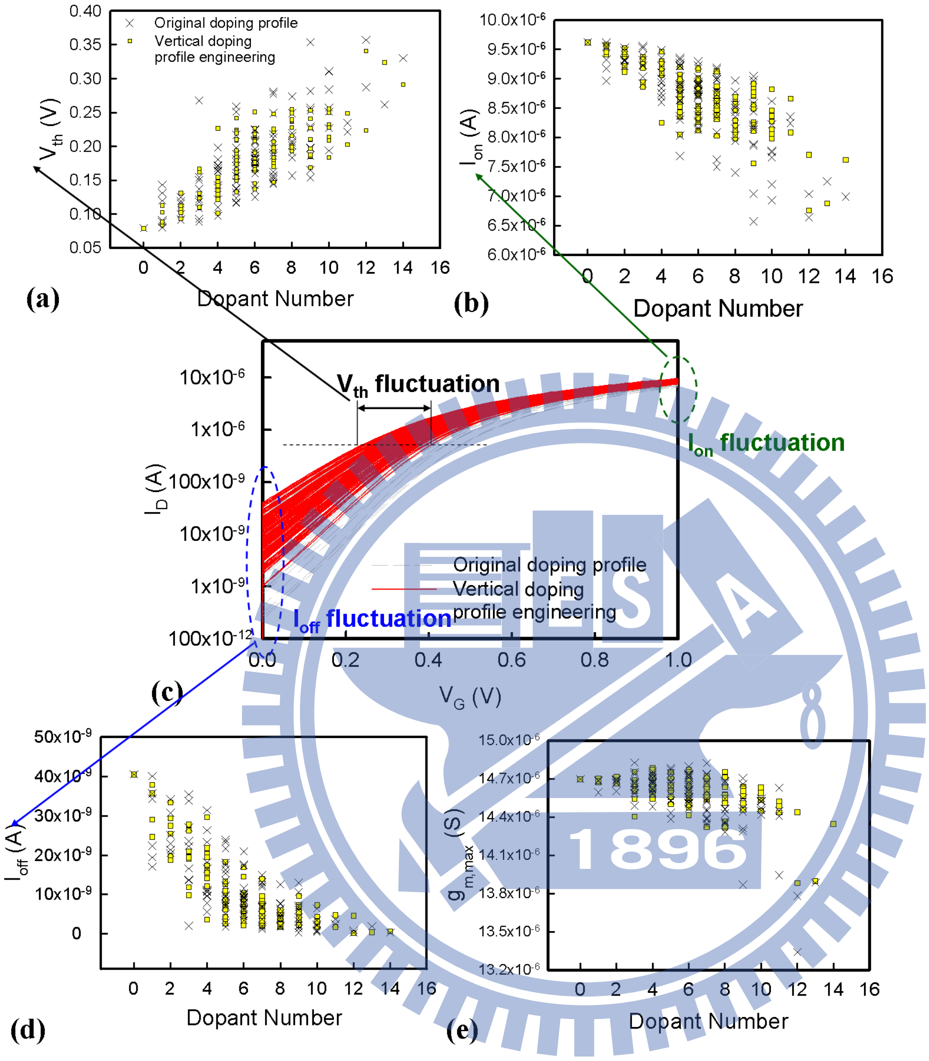


Figure 7.2: DC characteristic fluctuations of the 250 discrete dopant fluctuated 16-nm-gate planar MOSFET from the original and the improved doping profile. The studied fluctuations of (a) threshold voltage, (b) on-state current, (c) I_D-V_G curves, (d) off-state current, (e) and maximum transconductance.

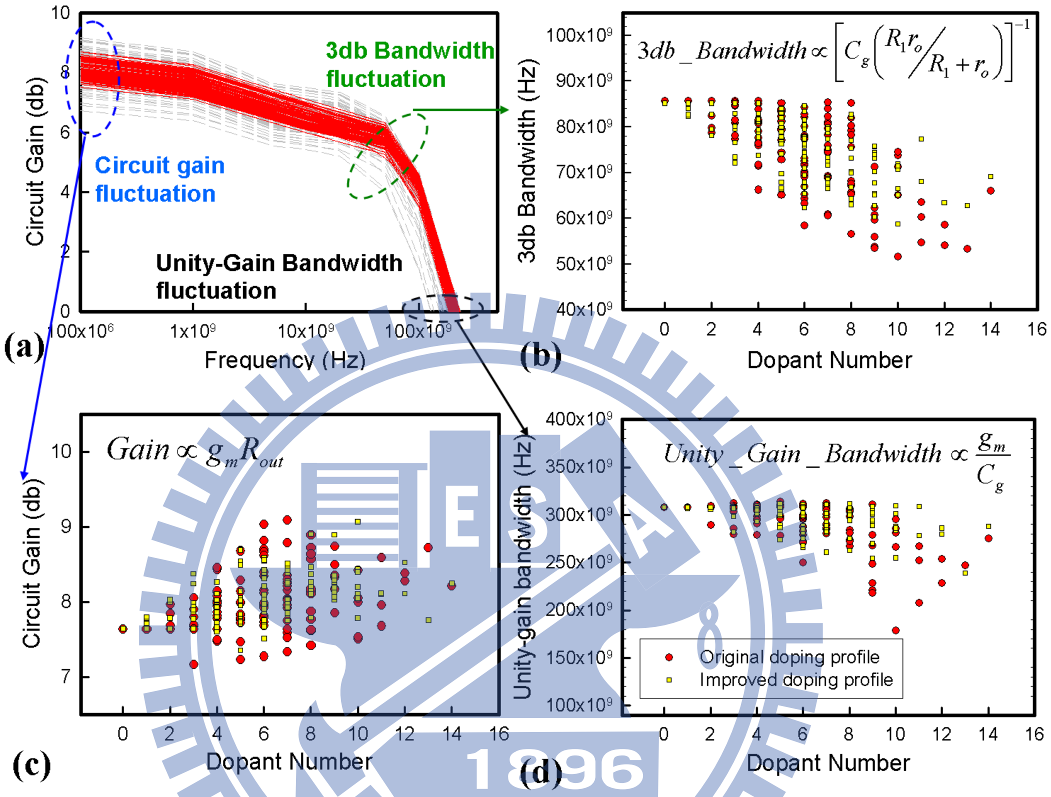


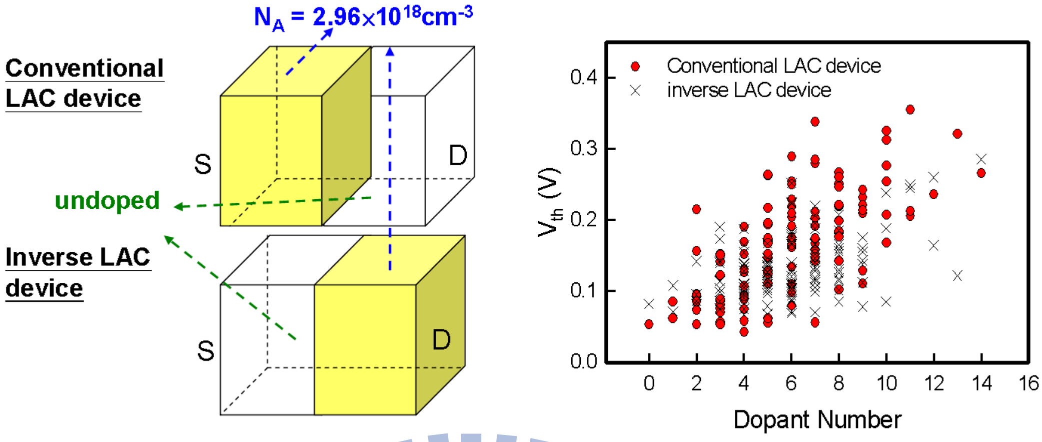
Figure 7.3: (a) Comparison of frequency response fluctuations of the discrete dopant fluctuated 16-nm-gate cases generated from the improved (dashed line) and original (solid line) doping distributions. Comparison of (a) Gain, (b) 3dB bandwidth, (c) and unity-gain bandwidth fluctuations of the 125 discrete dopant fluctuated 16-nm-gate planar MOSFET circuit with the improved (squares) and original ("×") doping profiles.

be controlled by the manufacturing processes of ion implementation and thermal annealing. To compare the vertical channel engineering with the original cases on a fair basis, the nominal threshold voltage of the vertical channel engineering is adjusted to 140 mV. 758 dopants are firstly randomly generated in a large rectangular solid (x × y × z = 16 nm × 2000 nm × 16 nm), in which the equivalent doping concentration is 1.48×10^{18} cm^{-3}). The inset of Fig. 7.1(a) shows the nominal case of the vertical doping profile engineering, where the darker region indicates the higher doping concentration. The large rectangular solid is then partitioned into 125 sub cubes of $(16\text{ nm})^3$ cube and mapped into device channel for discrete dopant and coupled device-circuit simulation. Similar to the original doping profile, the number of dopants may vary from zero to 14, and the average number is six, as shown in Fig. 7.1(b). The longitudinal dopant distribution of the improved and the original doping profile are shown in Figs. 7.1(c) and 7.1(d), respectively. Since the position of discrete dopants of the original is random in each direction, the distribution of dopant number in channel depth is uniform. Additionally, for the vertical doping profile engineering, numbers of dopant appearing near the channel surface is significant less than that of the original doping profile and thus may induce less surface potential fluctuation than the other. Figure 7.2 shows the comparison of DC characteristic fluctuations for the original and the vertical doping profile engineering. Figure 7.2(c) shows the I_D-V_G characteristics of the discrete dopant fluctuated device generated from the improved (dashed lines) and the original (solid lines) doping profiles. The spreading range of the vertical doping profile engineering is reduced and indicates a suppression of fluctuation on DC characteristic of device. The fluctuation of the threshold voltage is shown in Fig. 7.2(a), where the square symbol indicates the cases of the vertical doping profile engineering and the ”×” symbols symbol shows the cases of original doping profile. The scattering range of the threshold voltage is significantly suppressed, and the fluctuation of threshold voltage is reduced from 58.5 mV to 50.2 mV. The fluctuation of the on-state current, off-state current, and maximum transconductance are shown in Figs. 7.2(a), 7.2(b), 7.2(d), and 7.2(e), respectively. The fluctuation of on-state current and maximum transconductance is effectively suppressed due to the less dopant locating near the channel surface. Notably, the suppression of I_{off} fluctuation is not significant due to the similar numbers of dopant locating near the path of leakage current (about 4 nm below the gate oxide). The proper selection of the dopant distribution near channel surface is a critical issue. The high-frequency response of the nanoscale MOSFET circuit is shown in Fig. 7.3(a). The spreading range of the improved doping profile is reduced through the improvement of doping profile. The fluctuation of the high-frequency characteristics, the circuit gain, the 3dB bandwidth and the unity-gain bandwidth of the nanoscale MOSFET circuit are calculated; as shown in Figs. 7.3(b) - 7.3(c), the square and ”×” symbols indicate the cases of the improved and original doping distributions. The fluctuation suppressions of the characteristics of the nanoscale device circuit are more pronounced than that of device due to the second-order nonlinear effect of circuit characteristics. The fluctuation suppression of the high frequency characteristics is resulted from less DC characteristic and gate capacitance fluctuation of device by introducing a doping profile of Gaussian distribution along the longitudinal direction from surface to substrate. The result confirms the fluctuation suppression technique on high-frequency characteristic fluctuation of nanoscale device circuit and show the effectiveness of fluctuation suppression technique.

7.2.2 Inverse Lateral Asymmetry Doping Profile

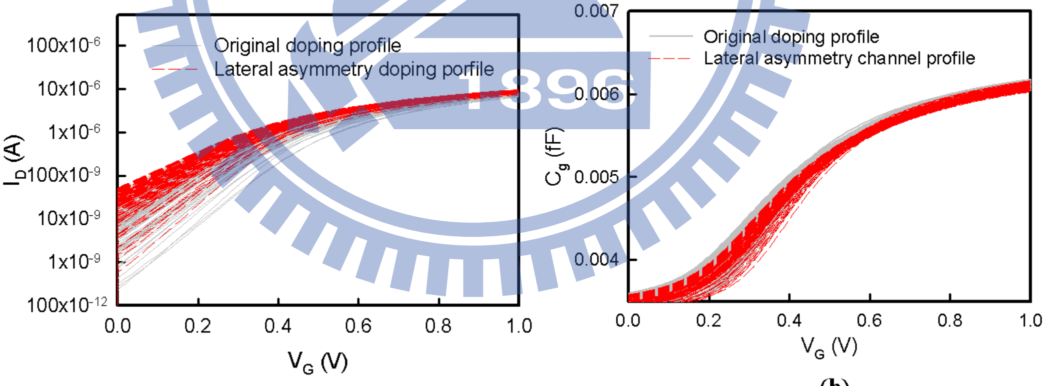
In nanoscale FETs, the lateral asymmetric channel (LAC) devices have shown better control of the short channel effect [122,123]. The high concentration channel doping near the source-end reduces short channel effect while low doping concentration near the drain end ensures high mobility. However, attention is less drawn on the existence of random doping effect for the lateral asymmetry channel doping profile [64]. Therefore, we design a lateral asymmetry doping profile with higher channel doping concentration at near the drain-end of channel to suppress RDF.

First, we compare the fluctuation of conventional LAC device with inverse lateral asymmetry doping profile, as illustrated in Fig. 7.4(a). The V_{th} fluctuations are then compared in Fig. 7.4(b), where the ”×” and ”o” indicate the cases of the conventional LAC doping



(a) (b)

Figure 7.4: (a) Illustration of conventional and proposed lateral asymmetry doping profile. (b) Comparison of the V_{th} fluctuations for the conventional and proposed lateral asymmetry doping profile.



(a) (b)

Figure 7.5: The explored I_D-V_G and high frequency response characteristics for the proposed inverse lateral asymmetry doping profile and original doping profile.

Table 7.1: Effectiveness of vertical doping profile engineering and lateral asymmetry doping profile with respect to the original doping profile.

	Vertical doping profile engineering (%)	Lateral asymmetry doping profile (%)
V_{th}	14.2	21.8
I_{on}	22.0	32.2
I_{off}	2.0	-45.2
C_g	16.4	62.6
Gain	32.3	22.2
3dB bandwidth	19.4	63.1
Unity-gain bandwidth	51.8	41.4

profile and inverse LAC doping profile. The V_{th} fluctuation for the proposed inverse lateral asymmetry doping profile device is 1.6 times smaller than the conventional LAC device because of the smaller injection velocity and current fluctuation for dopants located near the drain-end of the channel [123]. The DC and high-frequency characteristics of proposed inverse lateral asymmetry doping profile are then compared with the original doping profile and shown in Figs. 7.5(a) and 7.5(b). The spreading range of the I_D-V_G and high frequency response characteristics are significantly suppressed. Figure **??** summaries the threshold voltage, on-state current, gate capacitance, circuit gain, 3dB bandwidth, and the unity-gain bandwidth, are reduced by 21.8%, 32.3%, 62.6%, 22.2%, 63.1% and 41.4%, respectively. Note that the 3dB bandwidth is strongly dependent on the gate capacitance and therefore exhibits similar improvement to gate capacitance fluctuation. However, unfortunately, the off-state current fluctuation increases by 45.2% due to the strengthened short channel effect. In the lateral asymmetry doping profile, unlike the profiles of conventional lateral asymmetry devices with higher channel doping concentrations nearer the source end of the channel region, the channel doping concentration is higher nearer the drain end of the channel region. Dopants at the source end of the channel may induce larger current fluctuation than they at the drain end of the channel. The effectiveness of vertical and lateral doping profile engineering are summarized in Table 7.1. The lateral asymmetry doping profile exhibits promising fluctuation suppression on threshold voltage, on-state current, gate capacitance, and 3dB bandwidth characteristics. However, the leakage current fluctuation is increased by 45.2% due to the stronger short channel effect. For future low power application, the vertical doping profile engineering is more suitable. Notably, the channel engineering is a trade-off between fluctuation and performance. The vertical and lateral channel profile co-design becomes an important issue in future nanoscale technology.

7.3 Suggestions on the Future Work

The future work is suggested from simulation, physics, device, and circuit viewpoints. From the simulation viewpoint, firstly, the 3D coupled simulation-optimization approach for nanoscale transistor requires much more computation time; however, it still worth to do. Secondly, the characterization and measurement of metal-gate workfunction on high-κ dielectrics are required. The multi-layer structure and interface effects should be further considered. Additionally, the first principle simulation of high-κ/metal materials is important, which guides the material selection process and will help us to narrow down to the most promising material. As for the device simulation, an universal mobility model of silicon FETs is important for device simulation. The calibration result can be further extended and compared with experimental data to facilitate the device simulation in various device dimensions. From the physics viewpoint, to investigate the carrier-dopant interaction, such as back scattering in strain silicon channel is interesting. From the device viewpoint, to distinguish the correlation between intrinsic parameter fluctuations and study more fluctuation source, such as oxide thickness variation, fin shape variation and so on, may be required. Moreover, since the strain technology is promising in nanoscale transistor, the impact of stress and substrate orientation on the device performance and reliability are urgent. Another important issue is the suppression of intrinsic parameter fluctuations. The suppression may result in some drawbacks, which should be addressed properly. Also, the fluctuation induced by source/drain dopants will become more and more important. Even the channel is undoped in ultra-small nano-devices, the RDF still impacts the device reliability significantly due to the dopants in source and drain. As the device gate length below 10 nm, the source/drain dopants induced fluctuation will become more and more important. They not only impact the resistance of source/drain region, but also influence the effective gate length of transistors. From the circuit viewpoint, it is imperative to derive a well-established compact model consisting of the randomness effect to realize the nanoscale device and circuit design. The coupled device-circuit simulation may provide an effective way to obtain circuit characteristics without use of compact model. However, there is still a lot of room to improve the numerical stability and numerical method in the coupled device-circuit simulation. Additionally, many the manufacturing of nanoscale transistor and development of related computer-aided-design software, such as layout and routing tools are open problems nowadays. To improve the reliability of VLSI circuits and systems, the development of fluctuation suppression approach from circuit viewpoint is necessary. An example is the use of 8T SRAM architecture to replace the 6T SRAM. Consequently, to suppress the intrinsic parameter fluctuations, the suppression techniques integrating process, device and circuit design viewpoints is required. The nanoscale technology in now facing great challenge and provide abundant chances in new semiconductor application.

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Doctoral thesis title: Intrinsic Parameter Fluctuation in Nanoscale MOSFET with Vertical Silicon Channels

Awards and Honors:	第三屆台積電傑出學生研究獎銅牌獎 (shown as attachment)
	2008年思源EDA頂尖國際會議論文獎 (shown as attachment)
	2008 IEDMS Best Paper Award (shown as attachment)
	2009 ASQED Best Paper Award (shown as attachment)

Selected Publication List:

Journal papers

[1]. Yiming Li and **Chih-Hong Hwang**, "DC Baseband and High-Frequency Characteristics of Silicon Nanowire Field Effect Transistor Circuit," Semiconductor Science and Technology, Vol. 24, No. 4, April 2009.

[2]. Yiming Li, **Chih-Hong Hwang**, and Hui-Wen Cheng, "Process-Variation- and Random-Dopants-Induced Threshold Voltage Fluctuations in Nanoscale Planar MOSFET and Bulk FinFET Devices," Microelectronic Engineering, Vol. 86, No. 3, March 2009, pp. 277-282.

[3]. Yiming Li, **Chih-Hong Hwang**, and Hsuan-Ming Huang, "Large-Scale Atomistic Approach to Discrete-Dopant-Induced Characteristic Fluctuations in Silicon Nanowire Transistors," Physica Status Solidi (a), Vol. 205, No. 6, June 2008, pp. 1505-1510.

[4]. Yiming Li and **Chih-Hong Hwang**, "Discrete-Dopant-Fluctuated Threshold Voltage Roll-Off in Sub-16nm Bulk FinFETs," Japanese Journal of Applied Physics, Vol. 47, No. 4, Apr. 2008, pp. 2580-2584.

[5]. Yiming Li and **Chih-Hong Hwang**, "Effect of Fin Angle on Electrical Characteristics of Nanoscale Round-Top-Gate Bulk FinFETs," IEEE Transactions on Electron Devices, Vol. 54, No. 12, Dec. 2007, pp. 3426-3429.

[6]. Yiming Li and **Chih-Hong Hwang**, "Discrete-Dopant-Induced Characteristic Fluctuations in 16nm Multiple-Gate Silicon-On-Insulator Devices," Journal of Applied Physics, Vol. 102, No. 8, Oct. 2007, 084509.

[7]. Yiming Li and **Chih-Hong Hwang**, "Electrical Characteristic Fluctuations in 16nm Bulk-FinFET Devices," Microelectronic Engineering, Vol. 84, No. 9-10, Sep.-Oct. 2007, pp. 2093-2096.

Conference papers

[1]. **Chih-Hong Hwang**, Tien-Yeh Li, Ming-Hung Han, Kuo-Fu Lee, Hui-Wen Cheng, and Yiming Li, "Statistical 3D Simulation of Metal Gate Workfunction Variability, Process Variation, and Random Dopant Fluctuation in Nano-CMOS Circuits," Proceedings of The 2009 IEEE International Conference on Simulation of

Semiconductor Processes and Devices (IEEE SISPAD 2009), Hotel Del Coronado, San Diego, California, USA, Sept. 9-11, 2009.

[2]. **Chih-Hong Hwang**, Tien-Yeh Li, Ming-Hung Han, Hui-Wen Cheng, and Yiming Li, “Quantum Hydrodynamic Simulation of Discrete Dopant Fluctuated Physical Quantities in Nanoscale FinFET Device,” Conference on Computational Physics (APS CCP 2009), Koahsiung, Taiwan, Dec. 15-19, 2009.

[3]. Yiming Li, **Chih-Hong Hwang**, Ta-Ching Yeh, and Ming-Hung Han, "Simulation of Electrical Characteristic Fluctuation in 16-nm FinFETs and Circuits," Device Research Conference (IEEE DRC), Penn State University, PA, USA, June 22-24, 2009.

[4]. Yiming Li, **Chih-Hong Hwang**, Ta-Ching Yeh, and Tien-Yeh Li “Large-Scale Atomistic Approach to Random-Dopant-Induced Characteristic Variability in Nanoscale CMOS Digital and High-Frequency Integrated Circuits,” Proceedings of The 2008 IEEE/ACM International Conference on Computer-Aided Design (IEEE/ACM ICCAD 2008), San Jose, CA, USA, Nov. 10-13, 2008, pp. 278-285.

[5]. Yiming Li, **Chih-Hong Hwang**, Ta-Ching Yeh, Hui-Wen Cheng, and Tien-Yeh Li, “Discrete Dopant Fluctuated Transient Behavior in 16-nm-Gate CMOS,” The 2008 International Conference on Solid State Devices and Materials (SSDM 2008), Tsukuba International Congress Center (EPOCHAL TSUKUBA), Ibaraki, Japan, Sept. 23-26, 2008 pp. 894-895.

[6]. Yiming Li, **Chih-Hong Hwang**, Shao-Ming Yu, Hui-Wen Cheng, Hsuan-Ming Huang, and Ta-ChingYeh, “Process-Variation- and Random-Dopant-Induced Threshold Voltage Fluctuations in Nanometer Scale Planar MOSFET and Bulk FinFET Devices,” International Symposium on Advanced Gate Stack Technology (IEEE ISAGST 2007), Westin City Center Hotel, Dallas, Texas, Sept. 26-28, 2007.

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Attachment:

台灣積體電路製造股份有限公司
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獎狀

國立交通大學電信工程學研究所
黃至鴻同學
作品：
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傑出論文獎

Electrical Characteristics Dependence on the Channel Fin Aspect Ratio of Multi-Fin Field Effect Transistors

Hui-Wen Cheng Chih-Hong Hwang

Chung-Jung Hsieh Yiming Li

中華民國九十七年十一月二十九日

Attachment:

July 15-16 2009, Kuala Lumpur, Malaysia

ASQED'09 Best Paper Award

Process-Variation- and Random-Dopant-Induced Static Noise Margin Fluctuation in Nanoscale CMOS and FinFET SRAM Cells

Tien-Yeh Li, Chih-Hong Hwang, Yiming Li
National Chiao Tung University

Ali Iranmanesh
President ISQED

Tanay Karnik
Technical Program

JA Lew
Conference Chair

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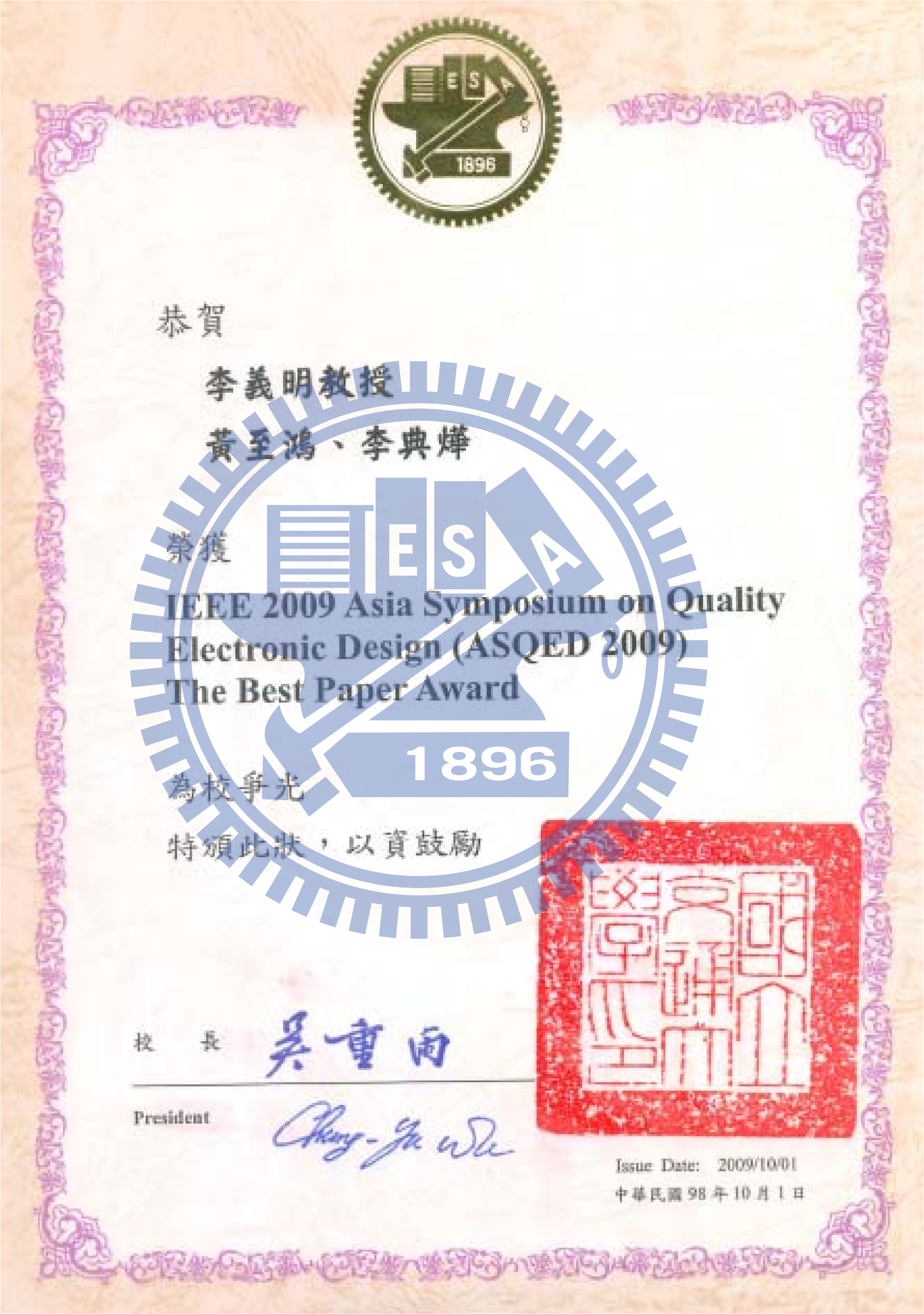

恭賀

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黃至鴻、李典燁

榮獲

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