國 立 交 通 大 學

電信工程學系

博 士 論 文

利用金氧半場效電晶體，鍺化矽電晶體，和磷化銦鎵/砷化鎵異質接面電晶體技術之射頻吉伯特混波器及接收機系統架構

RF Gilbert Mixers and Receiver Architectures Using CMOS, SiGe BiCMOS, and GaInP/GaAs HBT Technologies

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中 華 民 國 九 十 六 年 七 月

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摘　　要

本篇博士論文的研究主題包含新式高IIP_2吉伯特混波器架構、升頻混波器、創新的鏡像抑制接收器架構及並串串並雙迴授寬頻放大器。首先本論文中針對吉伯特混波器發明了更高性能的新架構，可使對稱性大幅提升，進而使得在RF 頻率為 10-GHz時IIP_2的性能提升至 33 dBm。本文利用 2 um GaInP/GaAs HBT技術第一個完整地去比較現有主動次諧波混頻器的優劣，並且實作出了一個 5.2-GHz次諧波混波器，其 2LO-to-RF 隔絕度世界最高。在傳送機方面，利用 2 um GaInP/GaAs HBT 及 0.35 um SiGe BiCMOS實作出結合微小化集總微波分波器及LC電流鏡之高性能的升頻器。

接著，本論文實作出傳統的 Hartley 及 Weaver 鏡像抑制接收器，其抑制能力分別為 47 及 48 dB。其中，Weaver 降頻器利用把 LO 訊

號連結在一起，可以不需自我校正而達到 48 dB 的鏡像訊號抑制。另外，本論文還提出了嶄新的 2.4/5.7-GHz 雙頻帶射頻接收機系統架構，並且利用 0.18 um CMOS 及 0.35 um SiGe BiCMOS 加以驗證實作。

最後，本論文針對常用的並串串並雙迴授寬頻放大器提出了全新的設計理論，並且經由 0.13 um CMOS 實驗結果加以驗證之。量測結果和理論完全符合。

RF Gilbert Mixers and Receiver Architectures Using CMOS, SiGe BiCMOS, and GaInP/GaAs HBT Technologies

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Abstract

The research topics of this dissertation include novel high IIP_2 Gilbert mixer topologies, active sub-harmonic mixers, up-conversion mixers, novel image rejection receiver architectures, and the design methodology of the shunt-series series-shunt double feedback wideband amplifier.

Several mixer building blocks are demonstrated in this work. A novel truly-phase-balanced sub-harmonic Gilbert mixer topology with high IIP_2 is proposed. The sub-harmonic mixer exhibits 33 dBm IIP_2 when the RF frequency is 10-GHz. A high isolation 5.2-GHz stacked-LO Gilbert mixer is demonstrated and the highest 2LO-to-RF isolation for the direct-conversion architecture is achieved. In addition, up-conversion mixers using the active/passive LC current mirrors and lumped rat-race hybrids are demonstrated at 5-GHz by using GaInP/GaAs HBT and SiGe HBT technologies. The design principles of the LC current mirror are developed.

Next, a conventional SiGe HBT 47 dB image rejection Hartley system and a GaInP/GaAs HBT 48 dB image rejection Weaver system are demonstrated and analyzed. In addition, 2.4/5.7-GHz dual-band image rejection architecture that combines the Weaver and Hartley systems is proposed for the first time. The novel Weaver-Hartley down-converters are demonstrated using 0.18 um CMOS and 0.35 um SiGe BiCMOS technologies. A powerful diagrammatic explanation using the complex

mixing technique is developed to analyze the image rejection mechanism and the secondary image signals of the Weaver architecture in this dissertation.

Finally, a shunt-series series-shunt double feedback loops wideband amplifier is demonstrated in 0.13 um CMOS technology. The design formulas of the small signal S parameters are determined to design the wideband amplifier. The experimental results highly agree with the design equations.

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Chapter 1

Introduction

The RFICs (Radio Frequency Integrated Circuit) become the key building block of the telecommunication circuit in the past decade. Conventionally, the RFIC pursued the high performance at the high frequency region, and the MESFET, GaInP/GaAs HBT, BiCMOS, and PHEMT technologies had played the dominant roles. In this dissertation, the research results start from conventional circuit topology using the advanced technology, and end with novel circuit schematic using the main stream silicon technology.

Many high performance RFICs with conventional circuit topologies are demonstrate using the 2 um GaInP/GaAs HBT technology. There are some unique advantages within the GaInP/GaAs HBT technology: the semi-insulating substrate, high mobility, and the low phase noise. The intrinsic GaAs material has wide band gap when compared with silicon, and the carrier concentration of the GaAs substrate is about $10^7/cm^2$ [1], which is 1000 times lower than the silicon substrate. Therefore, the GaAs substrate is a high-resistivity substrate, and conventionally called "semi-insulating". The advantage of the semi-insulating substrate is that the notorious substrate coupling can be totally eliminated, and the RF performance can be improved. For instance, the LO substrate leakage of the Gilbert mixer [2] can be eliminated. In Chapter 2, the state-of-the-art 2LO-to-RF isolation of the direct-conversion sub-harmonic Gilbert mixer [3] is achieved because the 2LO-to-RF substrate coupling is eliminated.

In addition to the elimination of the unwanted coupling substrate, the semi-insulating substrate also helps to provide accurate on-chip passive element. The quality factors as well as the accuracies of the passive elements on the silicon substrate are very difficult to maintain. The substrate parasitics inevitably degrades the quality factor of the on-chip inductors and capacitors [4]. The semi-insulating substrate assures high Q on-chip capacitor because the parasitic substrate capacitances and resistances are eliminated in the semi-insulating substrate. In Chapter 3, accurate

on-chip rat-race hybrids [5] consisting of the inductors and capacitors are demonstrated. The high-performance rat-race hybrids are employed in the up-conversion Gilbert mixers, and thus the up-converters exhibit excellent RF performances.

A major research topic in this dissertation is the image rejection architectures, and all the image rejection systems require quadrature signals. The RC-CR polyphase filters [6] are often used to generate quadrature signals. The quadrature accuracy of the polyphase filters relies on precision resistors and capacitors. The poly silicon resistor has been widely used in the advanced silicon technology, but the process variation is typically larger than 20%. For instance, the typical sheet resistance of the P^+-poly resistor without silicide is 311 Ω per square with 20% error in the 0.18 um CMOS technology. Although the sheet resistance of the P^+-poly resistor with silicide is 7.8 Ω per square and the low resistance is adequate to implement the quadrature generator, the typical process variation of this on-chip resistor is about 30%. On the other hand, the thin film resistors provided by the GaInP/GaAs HBT technology is accurately fabricated because the thickness of the film can be precisely in-situ monitored during the fabrication. In Chapter 4, a high performance Weaver image rejection down-converter [7] is demonstrated using the GaInP/GaAs HBT technology.

The final advantage of the GaInP/GaAs HBT technology is its low 1/f noise corner. The CMOS transistor suffers from the 1/f noise because the inversion layer is located adjacent to the Si-SiO_2 interface. Many dangling bonds (traps) existing in this interface make the device 1/f noise worse. On the other hand, the ledge of the HBT structure [8] as shown in Fig. 1-1, and the low DX centers of the GaInP/GaAs material make the 1/f noise of the HBT device minimized. The 1/f noise is very important for the RF circuits especially the oscillator and the direct-conversion mixer. The 1/f noise of the mixer can directly influence the output of the mixer, and the CMOS direct-conversion Gilbert mixer is suffered from the worse 1/f noise performance of the CMOS device [9]. The experimental results show that the GaInP/GaAs HBT has 1/f noise corner as low as 400-Hz (depend on the bias condition and the emitter area), and several excellent direct-conversion sub-harmonic Gilbert mixers with less influence of 1/f noise are demonstrated in Chapter 2.

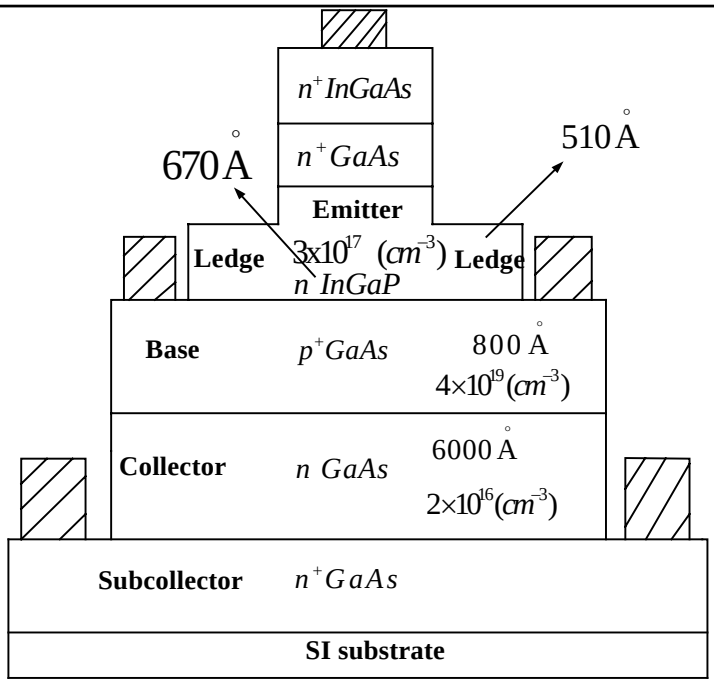


Fig. 1-1. The HBT layer structure including emitter ledge.

In general, the compound technologies such as GaAs HBT and PHEMT are considered as “Advanced but Expensive”, because the compound technologies above are very difficult to be integrated with the baseband chip. As the silicon-based technology improves rapidly, the RF-baseband SOC solution becomes possible. Commercially available 5 GHz WLAN transceivers except power amplifiers (PAs) have been using advanced CMOS and SiGe BiCMOS technology recently. It is commonly believed that RFICs made by silicon technology, especially the CMOS technology, have the lowest cost and can be easily integrated with digital CMOS ICs to form a wireless system on chip (SOC). CMOS transceivers integrated with the digital CMOS ICs have been successfully demonstrated, and so as to make the silicon technology more attractive. However, it is still difficult to integrate the high power PA with the RF transceiver. There exist stand-alone high power CMOS PAs [10] and SiGe PAs for 2.4 GHz WLAN applications [11]. The strong coupling in the Silicon substrate makes it difficult to merge the power amplifier into the RF transceiver. Thus, the PAs at 5 GHz are stand-alone and dominated by the GaAs technology.

As the CMOS device scaling by deep submicron technology continues, the cost of fabrication becomes very high and the device operating voltage decreases. Thus, the integration of high power amplifiers with the SOC becomes more difficult.

Moreover, the size of RFICs does not follow the scaling rule as the digital IC does. It is worthwhile to mention that the cost of research and development for the deep submicron CMOS IC design has increased dramatically due to the high cost photo masks. The high R&D cost has set a big barrier for many companies to enter the wireless IC markets.

In the past, the CMOS technology is very cost effective when compared with the 2 um GaInP/GaAs HBT technology. As the channel length shrinking, the barrier (the R&D cost) of the deep submicron CMOS is already higher than that of the 2 um GaInP/GaAs. A rough estimation of the cost per mm^2 (USD/mm^2) of the 0.13 um CMOS technology for the RF application (including ultra think metal for on-chip inductors) is 5,300 USD/mm^2, and that for 2 um GaInP/GaAs HBT technology is 60 ~121 USD/mm^2 only. The cost of 0.13 um CMOS technology is 44 times of the cost of GaAs HBT technology! As shown in Fig. 1-2, the prediction of the CMOS scaling roadmap [12] made by the ITRS (International Technology Roadmap for Semiconductors) predicts that the gate length shrinking becomes very challenging.

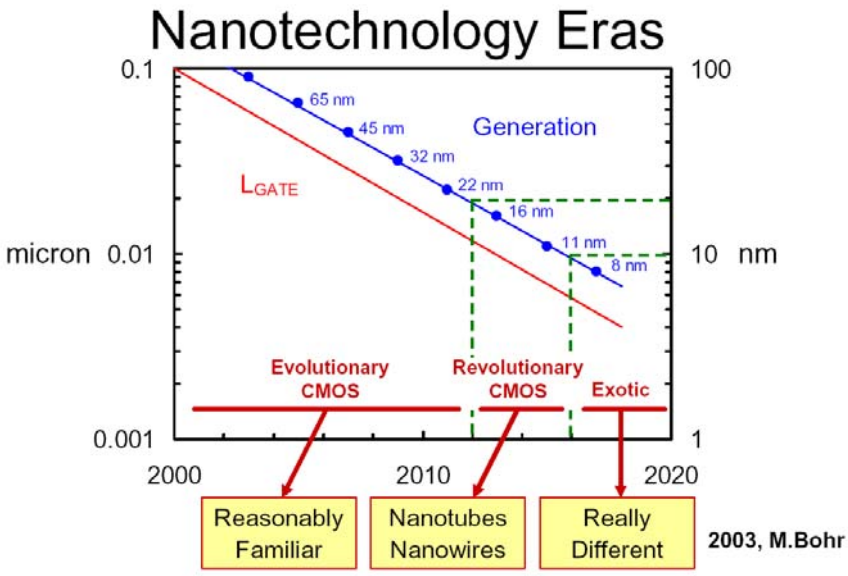
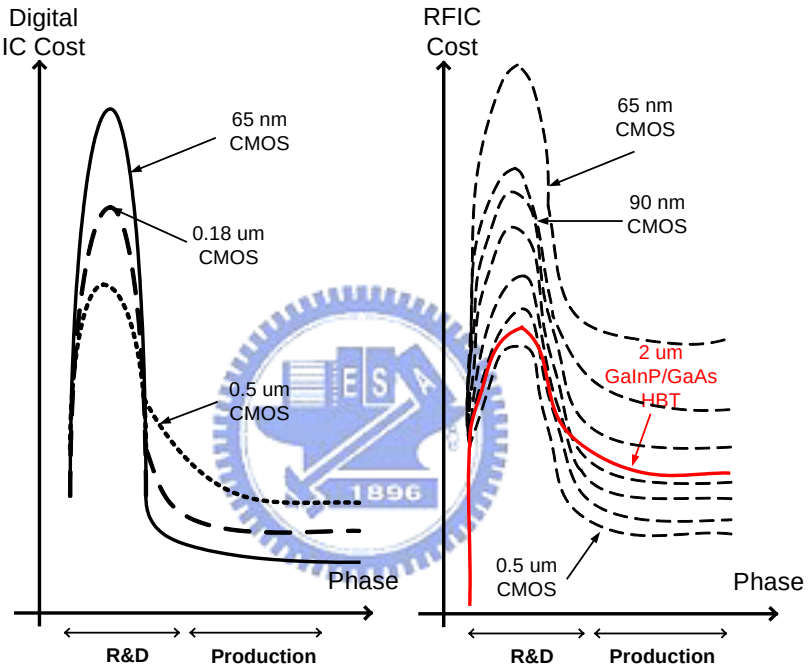


Fig. 1-2. The prediction of the CMOS scaling roadmap made by the ITRS. [2]

Although it is believed that the cost can be lower down when the final product is entering mass production (may not be true for the nano tubes), the barrier makes it very hard to finish a final product. The concept of the barrier for the CMOS R&D cost is illustrated in Fig. 1-3(a) and (b). The Y-axis is the cost and the X-axis might be the

product phase. Fig. 1-3(a) shows the cost reduction of the digital circuit as CMOS scaling, and the Fig. 1-3(a) is similar to a conventional diagram of the activation energy. On the other hand, the diagram for the RFIC is shown in Fig. 1-3(b) when the size of the CMOS is scaled down. Only when the RF solution provider expanses enormous investment, the final product can be realized. Figure. 1-4 manifests the same idea and depicts the R&D cost estimated by TSMC [13]. The average R&D cost of the 0.13 um CMOS is about 10 million USD, and the cost of 65 nm CMOS is as high as 45 million USD!



(a) (b)

Fig. 1-3. The cost for (a) digital scaling and (b) the RF scaling.

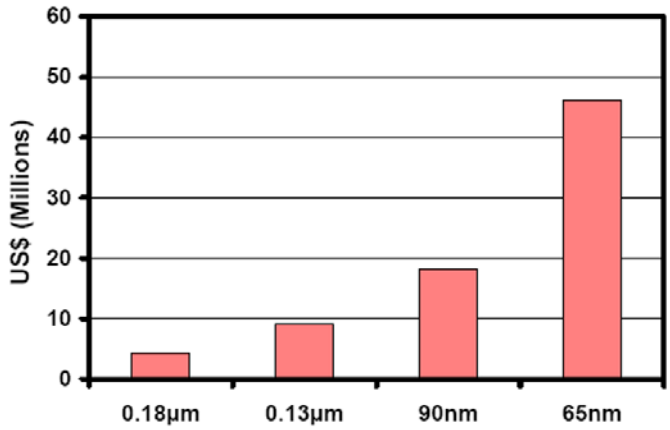


Fig. 1-4. The R&D cost of the deep sub-micron CMOS technology. (Estimated by TSMC) [3]

GaInP/GaAs HBT PAs are made by lower-cost 2 um photolithography. The cost for photo masks with 2 um accuracy is much lower than that for photo masks with 0.13 um accuracy. Thus, the IC design R&D cost for HBT technology is significantly lower than that for deep submicron CMOS technology. Conventionally, GaInP/GaAs HBT technology needs only roughly 10 mask steps while CMOS technology has more than 20 mask steps. There already exist 6-inch GaAs fabs when compared with the 12-inch Si fabs. Thus, there is a chance that the production cost for GaAs HBT RF transceivers can be lower down when compared with CMOS RF transceivers. If the external GaInP/GaAs HBT PA is still unavoidable, it is straightforward to think of the possibility of integrating the whole transceiver including PAs in GaInP/GaAs HBT technology because the semi-insulating GaAs substrate eliminate the cross coupling between the PA with the RF transceiver. In this work, several high-performance RFIC building blocks are demonstrated in 2 um GaInP/GaAs HBT technology. The research result shows that it is possible to accomplish a fully integrated RFIC including the power amplifier. It is might be another choice for the RF SOC.

Recently, there is a new trend to design the RF transceiver in the digital domain: the software-defined radio [14] and the DRP (Digital RF Processor) architecture [15]. These efforts are reducing the complexity of the RF transceiver and move the functions into the digital domain. Although these new concepts are interesting, there are still some serious drawbacks. In order to demodulate or convert the analog signal to digital domain, a high-speed and high-resolution A/D converter with high power consumption is required [14]. In addition, the down-conversion process is more difficult and can not be real time when the RF signals are distorted too much [14].

In this dissertation, in addition to the RFICs in GaInP/GaAs HBT technology, other high performance silicon based RFICs with novel circuit topologies are also demonstrated for completeness. The research results demonstrated in this dissertation include the image rejection low-IF architecture, direct-conversion sub-harmonic Gilbert mixers, fully integrated up-convertors, and shunt-series series-shunt double feedback amplifiers. The demonstrated RF circuits are implemented using the GaInP/GaAs HBT, SiGe BICMOS, and CMOS technologies.

The organization of this dissertation is itemized below: First, the sub-harmonic

mixers are described in Chapter 2. Next the Chapter 3 introduces the high performance up-conversion mixers. Chapter 4 discusses the conventional image rejection down-converters including Hartley and Weaver systems. The novel Weaver-Hartley dual-band down-converter is demonstrated in Chapter 5. The shunt-series series-shunt double feedback amplifier is described in Chapter 6. Finally, Chapter 7 concludes this dissertation and discusses the future work.

The super-heterodyne system is a reliable system through many years. The low-IF system [16][17] and the direct-conversion system [18] are presented in order to increase the integration level. The image rejection off-chip filter can be removed in the low-IF system because the IF polyphase filter is used to eliminate the image IF signal in the Hartley system [6][16][17]. In addition to the Hartley system, the Weaver system is the other practical receiver architecture to reject the image signal without the off-chip image rejection filters. The Weaver system cleverly utilizes the frequency shifting technique to block the unwanted image signals. The down-converted image signal can be totally rejected by the lowpass filter or the frequency response of the output amplifier.

The direct-conversion architecture is a highly integrated system. This compact system suffers from the notorious self-mixing problem. In order to eliminate the image signal, the IF frequency of the direct-conversion system is set to be zero. However, the LO frequency is the same with the RF frequency and thus the LO signal can be down-converted to the IF band if the LO signal leaks to the RF port. The above scenario is the cause of the self-mixing.

Many sub-harmonic direct-conversion Gilbert mixers are demonstrated in Chapter 2. The conventional stacked-LO, top-leveled-LO, and bottom-leveled-LO sub-harmonic mixers are demonstrated using the 2 um GaInP/GaAs HBT technology. The design trade-offs of the sub-harmonic mixers are discussed in detail. In addition, a novel LO-compensated highly symmetrical Gilbert sub-harmonic mixer topology is proposed. The new sub-harmonic mixer demonstrates excellent IIP_2 and 2LO-to-RF isolation when the RF frequency is 10 GHz.

Chapter 3 introduces a systematic analysis of the up-conversion Gilbert mixer using the lumped-element rat-race hybrid and the passive L-C current mirror. The

design consideration of the L-C current mirror including the parasitic resistance of the on-chip inductors is established. In addition to the passive inductor, a version of the up-conversion mixer with the active inductor is demonstrated. The active inductor successfully saves the valuable chip area at the expense of the dynamic range.

In the dissertation, a 0.35 um SiGe HBT Hartley image rejection down-converter is demonstrated in Chapter 4. This 5.2 GHz down-converter can provide image rejection ratio up to 47 dB. A 2 um GaInP/GaAs HBT 5.2/5.7 GHz Weaver down-converter is also presented in Chapter 4. The image rejection ratio of the Weaver down-converter is 48 dB.

Chapter 5 presents a novel dual band Weaver-Hartley architecture. A 0.35 um SiGe and a 0.18 um CMOS 5.7/2.4 dual band Weaver-Hartley systems are demonstrated. Both circuits exhibit 40 dB image rejection ratio for the band selection using the Weaver system and 46 dB image rejection ratio for the adjacent channel image signal using the polyphase filter.

Finally, a 0.13 um CMOS wideband amplifier is demonstrated in Chapter 6. The wideband amplifier is the well-known Meyer topology, and this amplifier contains double feedback loops. The design formulas of the shunt-series series-shunt double feedback amplifier are discovered. The experimental results of the S parameters are highly agreed with our theory and the insight of the Meyer amplifier is obtained in this chapter.

Chapter 2

High Performance Direct-Conversion Sub-Harmonic Gilbert Mixers

Among all the receiver architectures, the most popular system is the direct-conversion system [18]. The direct-conversion mixer is the most challenging topics when compared with the mixers used in the low-IF system [16][17]. The direct conversion system is the simplest system while the mixer is hardest to be designed. In this chapter, we start from conventional direct-conversion sub-harmonic Gilbert mixers using the advanced technology and end with a novel sub-harmonic Gilbert mixer topology.

More and more RF transceiver architectures are proposed because the wireless communication applications grow rapidly. The heterodyne system has been used for many years; however, the off-chip image rejection SAW filter limits the circuit integration of the heterodyne system. The active or passive polyphase filters are used in the low-IF system to filter out the image signal, but the polyphase filters occupy too many valuable IC estates [6], [17]. The direct-conversion architecture is proposed to increase the integration level. The direct-conversion system eliminates many bulky and expensive off-chip components, such as image-rejection and channel-select filters [18]. The RF frequency is arranged to be equal to the LO frequency in the direct-conversion system and thus the image signal is the RF signal itself. As a result, the image-rejection filter is no longer necessary. The direct-conversion structure reduces the manufacture cost and improves the circuit integration.

The direct-conversion transceiver is highly integrated at the cost of many novel problems such as the DC offset, the LO leakage, the I/Q signal mismatch, the even-order distortion and the flicker noise. Most important of all, the LO frequency of the direct-conversion mixer is too close to the RF frequency so that the self-mixing problem caused by the LO leakage can degrade the transceiver performance. In order to prevent the self-mixing problem, the sub-harmonic mixer topologies are proposed [3], [19]-[22].

Conventionally, the passive harmonic mixers have been used for many years. The passive diode mixers using the nonlinear property of the diodes and these mixers have super gain compression point (IP_{1dB}) at the cost of larger conversion loss and larger LO pumping power. On the other hand, sub-harmonic Gilbert mixers usually provide conversion gain at the cost of slower operation speed.

Three distinct sub-harmonic Gilbert mixers topologies based on the double-balanced structure have been proposed. The first topology is the three-level stacked-LO structure [3], [19], [20]. The working principle of the stacked Gilbert cell is to mix down the RF signal with the quadrature LO signals. On the contrary, the top-LO-configuration [21], and the bottom-LO-configuration [22] mixers are the leveled-LO sub-harmonic structures and their operations are based on the transistor's nonlinearity. In this work, all three different types of the conventional sub-harmonic Gilbert mixers are demonstrated using GaInP/GaAs HBT technology for the first time to the best of our knowledge. The pros and cons of the conventional sub-harmonic Gilbert mixers are discussed.

Ideally, the double balanced sub-harmonic mixer can totally eliminate the 2LO leakage; however, the 2LO leakage occurs when non-ideal effects such as circuit mismatches and the imperfections of the LO signal take place. In addition, the self-mixing problem caused by the 2LO leakage is more pronounced through the substrate coupling. The isolation properties can be improved using the deep N-well in the advance CMOS technologies [23] and the deep trench isolation in the SiGe bipolar technology [24]. Compared with the silicon substrate, the GaInP/GaAs HBT technology possesses a perfect semi-insulating substrate, and thus the high frequency 2LO leakage signal can not leak to the RF port through the GaAs substrate. Because the substrate coupling is eliminated in this work, the 2LO-to-RF isolation performances among the Gilbert sub-harmonic mixer topologies can be fairly investigated. According to our experimental results, the stacked-LO sub-harmonic mixer is the best topology to achieve the highest 2LO-to-RF isolation.

It is easy to generate accurate quadrature signals in the GaInP/GaAs HBT technology. Almost all the published sub-harmonic mixers were fabricated on the

lossy silicon substrates [21]-[24]. The effectiveness of the quadrature signals is limited by the fabrication variation and the silicon substrate parasitic effect. However, the LO quadrature generator, which is often a polyphase filter [6], can be implemented precisely using GaInP/GaAs HBT technology because of the accurate thin film resistors with 50 Ω sheet resistance, the 0.36 fF/um^2 MIM Si_3N_4 capacitors, and the semi-insulating GaAs substrate. It is noticed that a capacitor in the standard silicon process has a smaller area and thus suffers more from fabrication variation because of the 1 fF/um^2 MIM capacitor employed in the silicon process.

Because the passivated ledge is employed over the extrinsic base surface [8], [25] and the DX center trap in the GaInP material is absent, the GaInP/GaAs HBT technology has low flicker noise. According to the previous literatures [9], [26], [27], the 1/f noise dominates the low frequency noise figure in the direct-conversion mixer. The HBT device in this work has very low 1/f noise and the measured slope of the mixer noise figure as a function of the IF frequency validates this characteristic.

2.1 Conventional Sub-Harmonic Gilbert Mixers

In this section, the design trade-offs among the conventioanl sub-harmonic Gilbert mixers are discussed. Each sub-harmonic mixer topology has its own advantage. The stacked-LO structure [28] requires a smaller LO pumping power, but inevitably needs a larger DC supply voltage. The cascode stacked-LO structure makes the 2LO leakage very difficult to leak to the RF port, and thus the best 2LO-to-RF isolation is achieved in this structure.

On the other hand, the leveled-LO mixers can be potentially operated at higher frequency but needs a larger LO pumping power. When compared with the stacked-LO mixer, the leveled-LO mixers can operate at higher frequencies because this LO stage operates using the transistor's nonlinearity. The leveled-LO mixers (both the bottom-LO-configuration and the top-LO-configuration mixers) are likely to be faster than the stacked-LO mixer. The bottom-LO-configuration is the simplest topology, but it provides a smaller conversion gain and poor 2LO-to-RF isolation. The bottom-LO-configuration provides the minimal port-to-port isolation due to the circuit

topology.

The stacked-LO mixer with two Gilbert cells consumes smaller current because the DC current is reused in the cascode structure. The stacked-LO sub-harmonic Gilbert mixer has two LO ports and one RF port, as shown in Fig. 2-1.

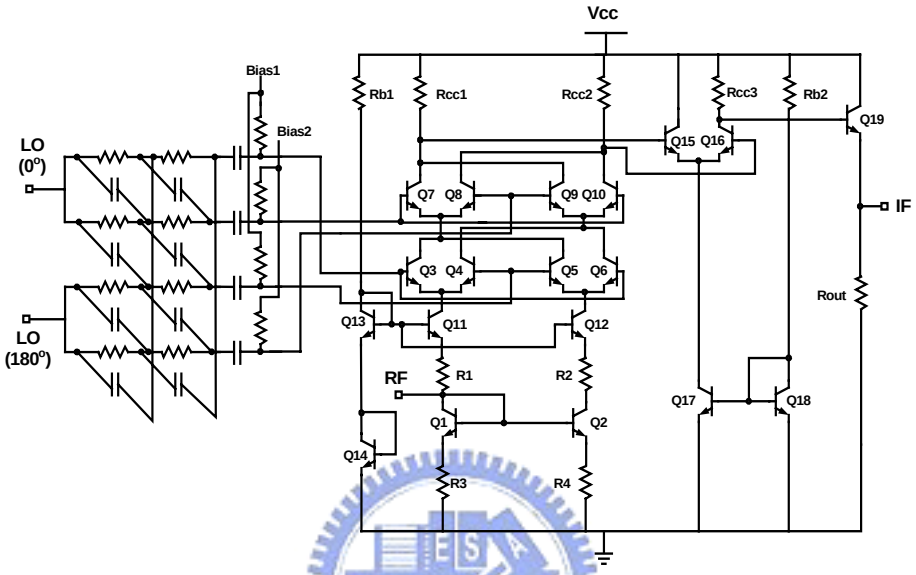


Fig. 2-1. The schematic of the 5.2 GHz three-level stacked-LO sub-harmonic GaInP/GaAs HBT Gilbert downconversion mixer.

The bottom LO Gilbert cell transistors (Q_3-Q_6) are fed by I+ and I- LO input signals while the top LO Gilbert cell transistors (Q_7-Q_{10}) are fed by Q+ and Q- LO input signals. If the I-phase and Q-phase LO signals are respectively defined as $\cos\omega_{LO}t$ and $\sin\omega_{LO}t$, the equivalent LO signals can be determined as follows:

$$\cos\omega_{LO}t \cdot \sin\omega_{LO}t = \frac{1}{2}\sin 2\omega_{LO}t \qquad (2.1)$$

Hence, the down-converted IF output frequency of the stacked-LO Gilbert mixer is the difference of the RF and the 2LO frequencies. This topology with two stacked HBT-type Gilbert cells only needs very small LO pumping power when compared with the CMOS technologies. Because the transconductance of the HBT is an exponential function of the base-emitter voltage, the current in the LO Gilbert cell can be commutated by the small twist voltage on the order of several thermal voltage, V_T.

The stacked-LO cell actually provides a composite switching function, and the simplified stacked-LO sub-harmonic mixer is shown in Fig. 2-2(a). The switching function of the top and bottom Gilbert cells in Fig. 2-2(b) are expressed as $S_1(t)$ and $S_2(t)$, respectively. If the signal $S_1(t)$ is behind $S_2(t)$ by a quarter period, the composite switching function represented as S(t) is the exclusive OR function of $S_1(t)$ and $S_2(t)$. As shown in Fig. 2-2(b), the stacked-LO cell has a switching function S(t), whose switching frequency is doubled. The corresponding paths in the composite switching half-periods A, B, C, and D are drawn in Fig. 2-2(a) and only half of the switching paths are drawn for simplicity.

The stacked-LO Gilbert mixer requires quadrature LO signals, and thus a two-section passive polyphase filter is employed to generate the accurate LO signals. The LO stages are stacked and biased at the different DC levels; hence, four DC blocking capacitors of 2 pF and biasing resistors of 3 kΩ are used in the top and bottom LO stages, as illustrated in Fig. 2-1.

The common-emitter transistor Q_2 the common-base transistor Q_{11} and the resistors R_1 to R_4 form the single-to-differential input stage, when Q_1 and Q_2 constructed as a current mirror (or the micromixer) [29], [30]. The common-base transistor Q_{11} possesses good frequency response, and the micormixer topology achieves the impedance matching at the RF input port. Thus, the chip area is saved. An output buffer consisting of an asymmetric differential amplifier and a common-collector output stage are incorporated to combine the IF output differential signals and to perform the output impedance matching.

The leveled-LO sub-harmonic mixer is an appropriate topology for the high-frequency and low-voltage mixer design. Figures 2-3(a) and (b) show the top-LO-configured leveled-LO mixer [21] and the bottom-LO-configured leveled-LO mixer [22]. By feeding LO signals with proper phases, the even harmonic leveled-LO structure can be employed to commutate RF currents at the rate of 2LO frequency [21]. Compared with the stacked-LO sub-harmonic mixer, the leveled-LO structure uses the transistor's nonlinearity. The 2um GaInP/GaAs HBT transistor employed in this work has a maximum f_T of 40 GHz (when the current density is 0.2

mA/um^2) and BV_{CEO} of 13V.

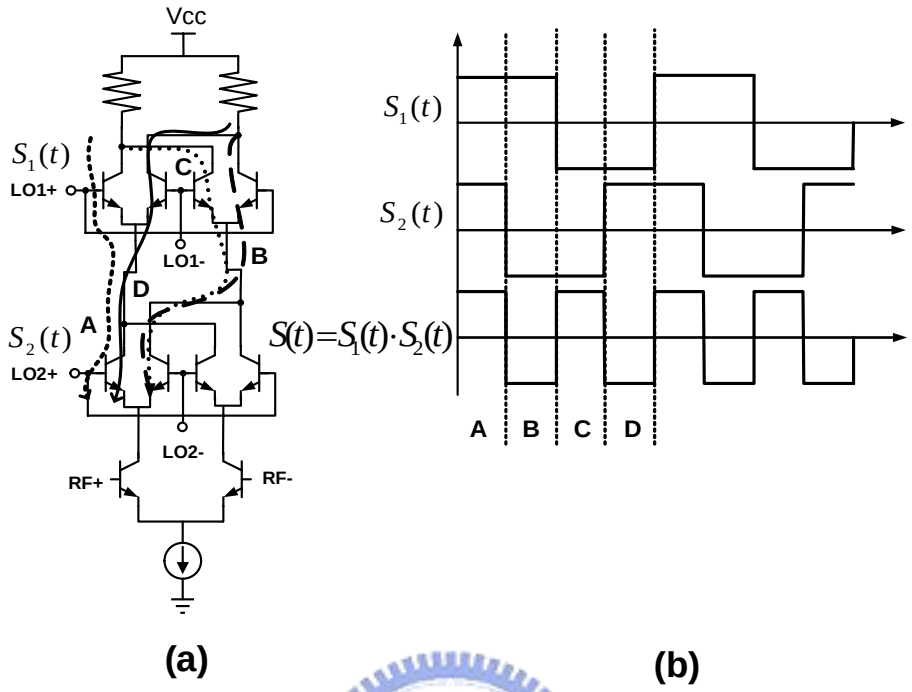


Fig. 2-2. (a) The simplified schematic of the three-level stacked-LO mixer, and (b) the timing diagram of the stacked-LO Gilbert cells.

When a step voltage function is stimulated at the base-emitter terminal, the collector output current is generated after a phenomenological time delay τ. The time delay τ was employed in the linear model in the literature [31], [32]. In other words, the I-V characteristic transfer function should be expressed in terms of V_{BE}, V_{CE} and τ. The output collector current follows the terminal base-emitter and collector-emitter voltages in an adiabatic way only if the operating radian frequency is much less than the reciprocal of the time delay τ. In general, active circuits operate much slower than the time delay τ which is normally on the order of one-third of the transistor transit-time delay [31], [32]. Therefore, the transit-time cut-off frequency f_T is still a good practical indication to judge whether the quasi-static model is valid for the second harmonic frequency or not.

The stacked-LO mixer basically trades the head room with higher 2LO-to-RF isolation. Because the stacked-LO topology has smaller head room, the reused biasing current of the LO cell and the RF input stage can not be very large. On the other hand, there are fewer transistor levels stacked together in the leveled-LO topology and thus

the biasing current can be larger. In other words, the level-LO topology operates at higher transit time cut-off frequency than the stacked-LO topology does.

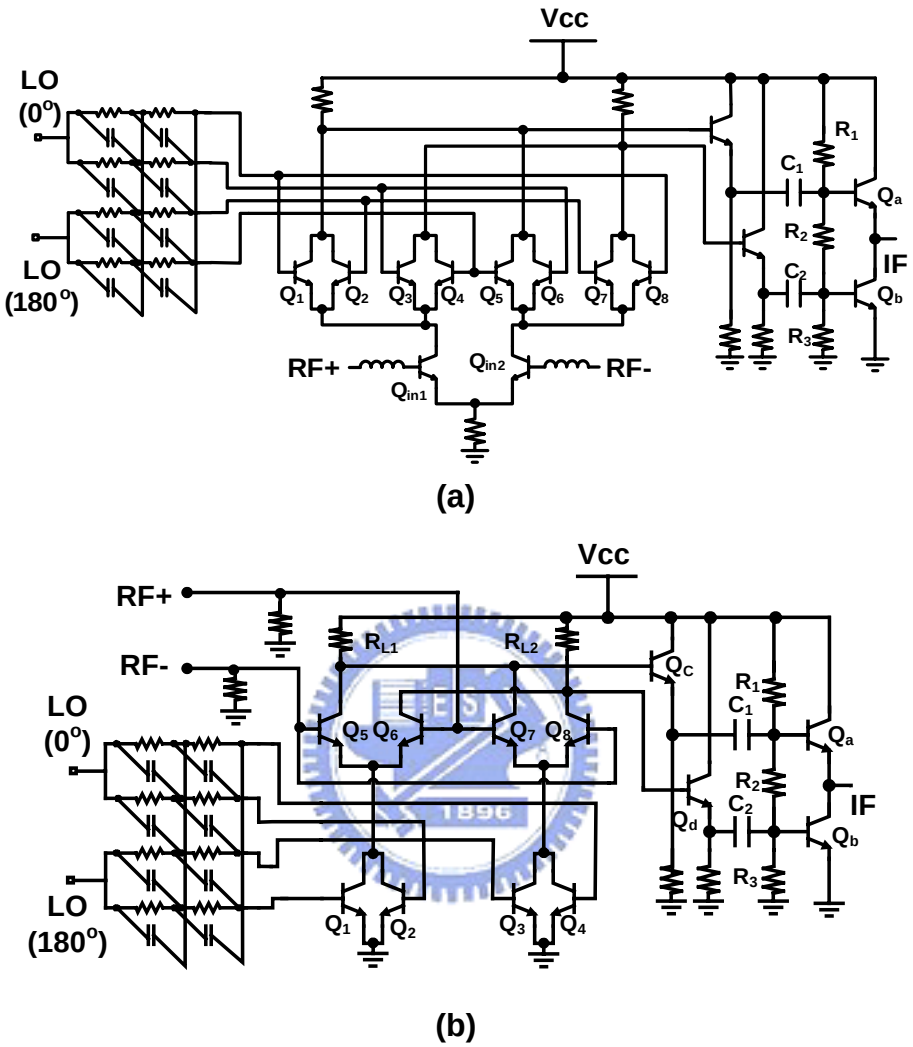


Fig. 2-3. The schematics of the (a) top-LO-configured; and (b) bottom-LO-configured leveled-LO sub-harmonic mixers.

An HBT transistor is a nonlinear device with exponential dependence between the collector current and the base-emitter voltage. The top-LO-configuration is shown in Fig. 2-3(a). The emitter-coupled pairs consisting of transistor pairs Q_1-Q_2 to Q_7-Q_8 forms the leveled-LO cell when their collectors are connected together. If 0^O and 180^O differential input signals are injected into the leveled-LO Q_1-Q_2 pair, the fundamental signals are eliminated by shorting the collectors of the differential pair and only the even harmonic currents appear at the collector nodes. Simultaneously, 90^O and 270^O LO signals are injected into the leveled-LO Q_5-Q_6 pair to generate the 2LO signal that is out of phase to the 2LO signal generated by leveled-LO Q_1-Q_2 pair. The transistor

pairs Q_1-Q_2 and Q_5-Q_6 work together to provide perfect 2LO differential signals [21]. Consequently, this structure can be used for the sub-harmonic mixer, and these emitter-coupled leveled-LO pairs shown in Fig. 2-3(a) are able to double the LO frequency.

As shown in Fig. 2-3(a) and (b), the difference between these two types of leveled-LO mixers is the location of the LO cell. The top-LO-configuration mixer consists of four leveled-LO pairs (Q_1 to Q_8) above the RF input stage while the bottom-LO-configuration mixer contains two leveled-LO cells under the RF input stage. The differential-quadrature LO signals of the double-balanced structure used in this work can be generated by a two-section polyphase filter.

In order to discuss the operation mechanism of the leveled-LO topology, the HBT exponential I-V transfer function can be expressed as the modified Bessel function [33], [34]. As shown in Fig. 2-3(a), the transistors Q_1 and Q_2 form a leveled-LO cell. The input LO signals of transistor Q_1 and Q_2 are defined as two out-of-phase signals $\hat{v}\cos\omega t$ and $-\hat{v}\cos\omega t$, respectively. The output collector currents can be described as follows:

$$I_{CQ1} = I_S e^{\frac{\hat{v}\cos\omega t}{V_T}}$$
$$= I_S[I_0(x) + I_1(x)\cos\omega t + I_2(x)\cos 2\omega t + I_3(x)\cos 3\omega t + \ldots] \quad (2.2a)$$

$$I_{CQ2} = I_S e^{\frac{-\hat{v}\cos\omega t}{V_T}}$$
$$= I_S[I_0(x) - I_1(x)\cos\omega t + I_2(x)\cos 2\omega t - I_3(x)\cos 3\omega t + \ldots] \quad (2.2b)$$

Where x is equal to the ratio of $\frac{\hat{v}}{V_T}$. The $I_n(x)$ in (2.2a) and (2.2b) is the modified Bessel function. Because the collector nodes of the transistors Q_1 and Q_2 are tightened together, the overall collector current of the leveled-LO cell is the summation of I_{CQ1} and I_{CQ2}. It is:

$$I_{total} = 2I_S[I_0(x) + I_2(x)\cos 2\omega t + \ldots] \quad (2.3)$$

Where $I_0(x)$ is the DC bias component, and the $I_2(x)$ is the 2LO current. Figure 2-4 shows the simulated modified Bessel function. The generated 2LO signal $I_2(x)$ is normalized by the DC term $I_0(x)$, as shown in Fig. 2-4.

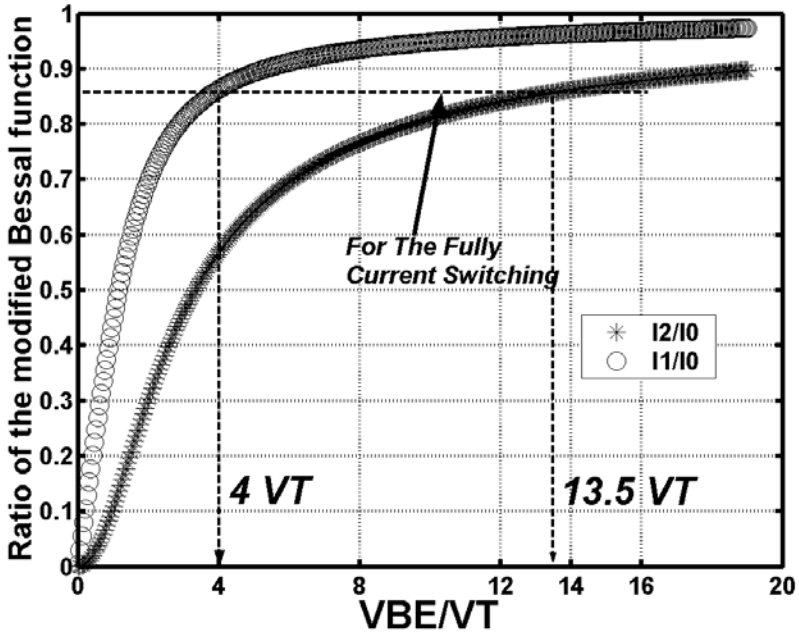


Fig. 2-4. The simulated ratio of the modified Bessel function as a function of the LO input voltage V_{BE}.

The fundamental signal $I_1(x)$ used in the conventional Gilbert mixer is cancelled in the leveled-LO cell. However, the term of $I_1(x)/I_0(x)$ is also simulated and normalized to compared with $I_2(x)/I_0(x)$. Generally speaking, the conventional LO Gilbert cell begins to fully switch when the ratio of V_{BE}/V_T is equal to 4. According to Fig. 2-4, the value of $I_1(x)/I_0(x)$ is 0.8635, but that of $I_2(x)/I_0(x)$ is only 0.5682 when the ratio of V_{BE}/V_T is 4 (the value of fully commutation of the conventional Gilbert cell). Therefore, the x of $I_2(x)$ must be 13.5 V_T (extra 10.57 dBm pumping power) in order to fully steer the 2LO cell when using the $I_2(x)$ signals. In other words, the leveled-LO cell, which uses the $I_2(x)$ current for the LO switching, definitely requires a much larger LO pumping power than the fundamental active mixer does.

A series inductor can easily achieve the input impedance matching of the top-LO-configuration mixer. On the contrary, the impedance matching at the RF input port is difficult to be achieved for the bottom-LO-configuration. The RF input stage of the bottom-LO-configuration is above the leveled-LO cell shown in Fig. 2-3(b). For the RF stage, the emitter is in series with a high resistance caused by the leveled-LO

stage. Large inductance and capacitance are required to match the high input impedance of the RF port. As a result, a brutal-forced matching resistor is shunt at the RF input port to save the chip area at the cost of worse noise figure and smaller conversion gain.

In our work, the IF output has a bandwidth of several hundreds MHz. Since the leveled-LO sub-harmonic mixer is designed for a wider IF output bandwidth, the differential amplifier is not fast enough. As shown in Fig. 2-3(a) and (b), a unity gain output buffer consisting of a common-collector transistor Q_a and a common-emitter transistor Q_b preserves the isolation properties of the differential signals in a double-balanced mixer structure and simultaneously drives the spectrum analyzer. Two DC blocking capacitors of 8.1 pF are incorporated to bias the output stage here. Practically, larger blocking capacitor is able to diminish the DC offset, to push the lower boundary of the IF bandwidth in a direct-conversion receiver.

Neglecting the substrate leakage, the bottom-LO-configuration inevitably has poor 2LO-to-RF isolation when compared with the top-LO-configuration. Any 2LO leakage power appearing at the collector of the LO transistors (Q_1 to Q_4) easily leaks to the base node of the RF transistors (Q_5 to Q_8) in the bottom-LO-configuration. On the contrary, the 2LO leakage power is hard to leak to the RF port in the top-LO-configuration because the 2LO leakage power has to pass through more transistors to the RF node (from the collector node of LO transistors (Q_1 to Q_8) to the base node of the RF transistors). The cascode topology in the top-LO configuration decreases the signal leakage at the cost of the circuit complexity, and larger biasing currents.

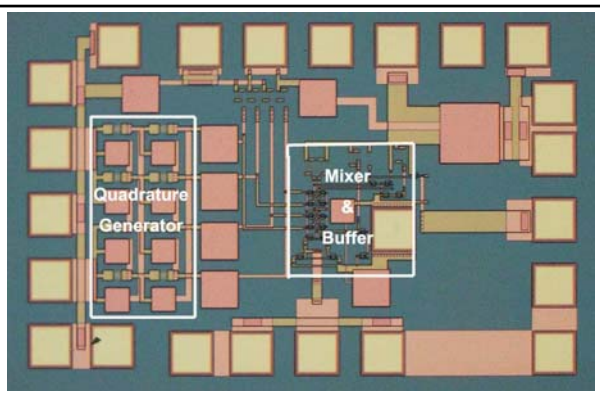
The head room problem limits the biasing current in the demonstrated mixers. The emitter areas of the transistors for the stacked-LO sub-harmonic are all 2×6 um^2 excluding the transistors used in the current source and the output buffer. The transistor sizes of the top-LO mixer cores (Q_1-Q_8) are 2×2 um^2 while the sizes of the transistors Q_5-Q_8 and Q_1-Q_4 in the bottom-LO mixer cores are 2×2 um^2 and 2×4 um^2, respectively. The device sizes of the mixer core are chosen for the optimal transistor cut-off frequency f_T. The knee voltage of the HBT is around 0.6 V, and the

emitter-collector voltages in our work are well designed to prevent the waveform clippings.

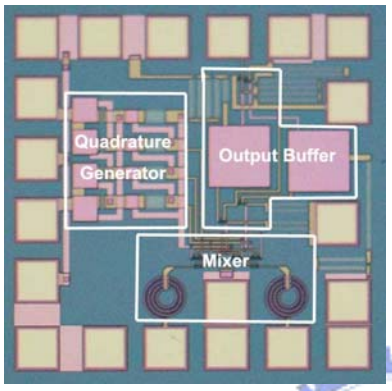
The die photo of the 5.004 GHz three-level stacked-LO sub-harmonic Gilbert mixer demonstrated in 2um GaInP/GaAs HBT is shown in Fig. 2-5(a). The LO and IF frequencies are 2.6 GHz and 400 KHz. The emitter areas of the GaInP/GaAs HBTs are 2um x 6um for the mixer core and 3um x 9um for the output buffer. The DC power supply is 3.3 V and the current consumption is only 4 mA including the output buffer. The die size including probing pads is 1 x 1.5 mm^2.

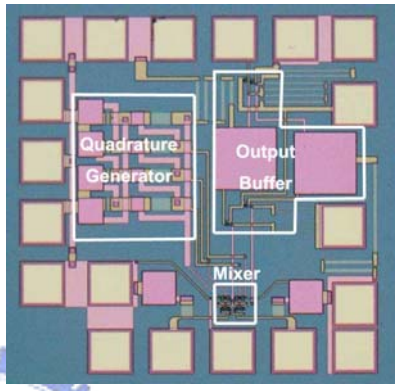
The die photos of the 10 GHz top-LO-configured and bottom-LO-configured mixers using the same technology are shown in Fig. 2-5(b) and Fig. 2-5(c), respectively. The LO and IF frequencies are 5 GHz and 100 MHz. Their die sizes including probing pads are both 1 x 1 mm^2. The chip sizes of the leveled-LO sub-harmonic mixers can be shrunk because of the smaller RC values of the polyphase filter in higher frequencies. As shown in Fig. 2-5(b) and Fig. 2-5(c), there are two DC blocking capacitors of 8.2 pF. The core current of the top-LO-configuration mixer and the bottom-LO-configuration mixer are 2 mA and 0.8 mA, respectively. The circuit topology of the bottom-LO-configured mixer is the simplest and thus the DC current can be reduced.

An off-chip 180 degrees hybrid and a pair of phase shifters are used to keep the phase accuracy; as a result, the intrinsic performance of the port-to-port isolation in a fully balanced Gilbert mixer is maintained. As shown in Fig. 2-6, the measured LO-to-IF, LO-to-RF, and 2LO-to-IF isolations are better than -40 dB, -50 dB, and -64 dB for the LO frequencies from 2.5992GHz to 2.6012 GHz. The 2LO leakage appearing at the RF port is directly measured by the spectrum analyzer [3]. The measured 2LO-to-RF leakage power is less than -83 dBm when the LO input power equals -8 dBm and the LO frequency is 2.6 GHz. The experimental result shows that the stacked-LO sub-harmonic topology and the GaAs semi-insulating substrate effectively reduce the 2LO-to-RF leakages. For comparison, the simulated 2LO-to-RF and 2LO-to-IF isolation are also plot.



(a)Stacked-LO-Configuration





(b) Top-LO-Configuration (c) Bottom-LO-Configuration

Fig. 2-5. The die photos of (a) the 5.2 GHz stacked-LO sub-harmonic mixer, (b) the 10 GHz top-LO-configured sub-harmonic mixer, and (c) the 10 GHz bottom-LO-configured sub-harmonic mixer.

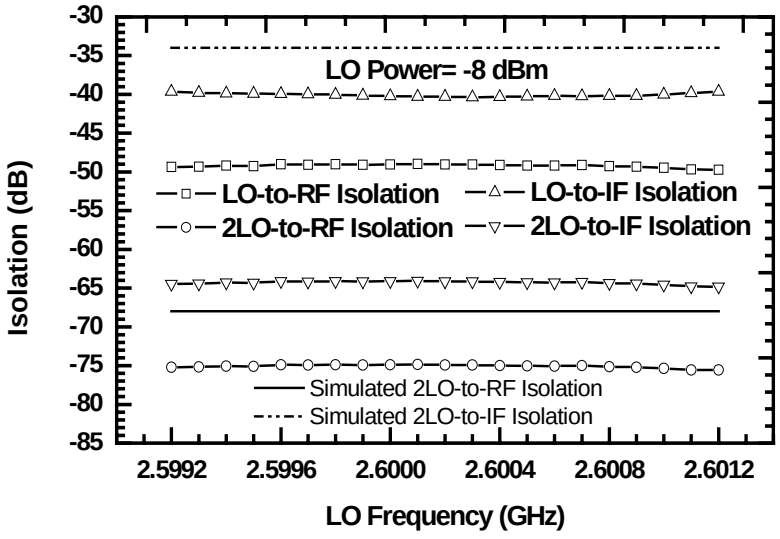


Fig. 2-6. The measured and simulated LO-to-IF, 2LO-to-IF, LO-to-RF, and 2LO-to-RF isolations as a function of the LO frequency for the stacked-LO sub-harmonic mixers.

Figure 2-7 illustrates the LO-to-IF, 2LO-to-IF, LO-to-RF and 2LO-to-RF isolations as a function of LO frequency for the leveled-LO sub-harmonic mixers. The top-LO-configured mixer has -32 dB LO-to-RF isolation, -59 dB 2LO-to-RF isolation, -32 dB LO-to-IF isolation, and -46 dB 2LO-to-IF isolation, while the bottom-LO-configured counterpart has the -23 dB LO-to-RF isolation, -32 dB 2LO-to-RF isolation, -35 dB LO-to-IF isolation, and -48 dB 2LO-to-IF isolation.

The 2LO-to-RF isolation of the top-LO-configured mixer is better. The LO-to-RF isolation can be used to indicate the self-mixing problem for the CMOS passive mixer. Compared with previous literatures, the measured performance of the 2LO-to-RF isolations of the stacked-LO sub-harmonic mixers in our work is second to none when the RF frequency is around 5 GHz, as shown in the table 2-1.

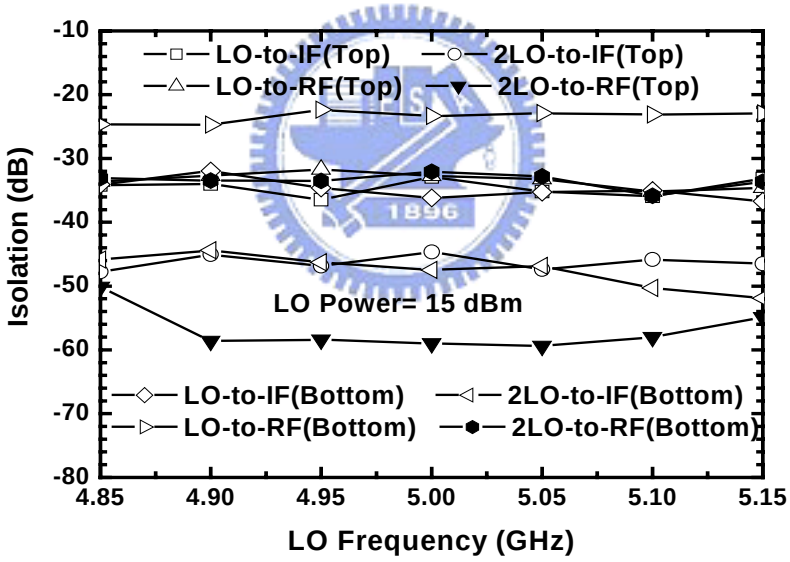


Fig. 2-7. The measured LO-to-IF, 2LO-to-IF, LO-to-RF, and 2LO-to-RF isolations as a function of LO frequency for the top-LO-configured and bottom-LO-configured sub-harmonic mixers.

The measured RF-to-IF isolation of the stacked-LO sub-harmonic mixer is -36 dB when the RF frequency is 5.2004 GHz. The RF-to-IF isolations of the top-LO and the bottom-LO sub-harmonic mixers as a function of RF frequency are shown in Fig. 2-8. The bottom-LO-configured mixer has better RF-to-IF isolation than the top-LO-configured one does.

Table 2-1: The 2LO-to-RF Isolations of Active Gilbert Sub-Harmonic Mixers

	2LO-to-RF Isolation (dB)	RF frequency (GHz)	Die Size (mm^2)	Power Consumption (mW)	Technology
Stacked-LO	75	5.2	2	13.2	2um GaInP/GaAs HBT
Top-LO	59	10	1	10	2um GaInP/GaAs HBT
Bottom-LO	32	10	1	4	2um GaInP/GaAs HBT
Ref[3]	70	2	1.92	9.24	0.5um SiGe HBT
Ref[20]	50	5-6	4.14	16.5	0.5um SiGe HBT
Ref[39]	64	5	1.8	72	0.13um CMOS
Ref[41]	35	5-6	0.7	47.5	0.5um SiGe HBT

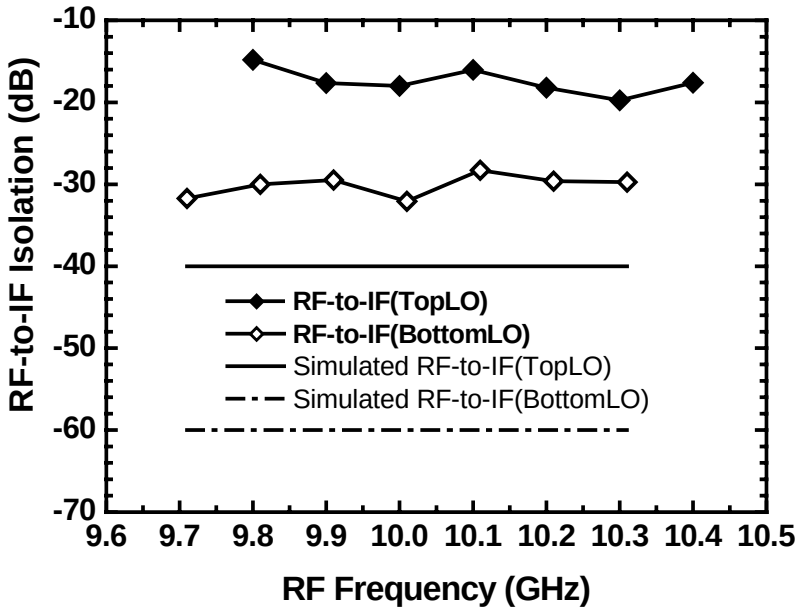


Fig. 2-8. The measured and simulated RF-to-IF isolations as a function of RF frequency of the top-LO-configured and bottom-LO-configured sub-harmonic mixers.

Figure 2-9 shows the measured conversion gain as a function of the LO power of all the sub-harmonic mixers. The conversion gain of the stacked-LO sub-harmonic mixer is 14.5 dB when LO power is larger than -10 dBm. As shown in Fig. 2-9, both leveled-LO sub-harmonic mixers require very large LO pumping powers. Compared with the stacked-LO structure, the LO pumping power of the leveled-LO mixer has to be 12 dBm for the optimal conversion gain while the stacked-LO structure only requires -9 dBm.

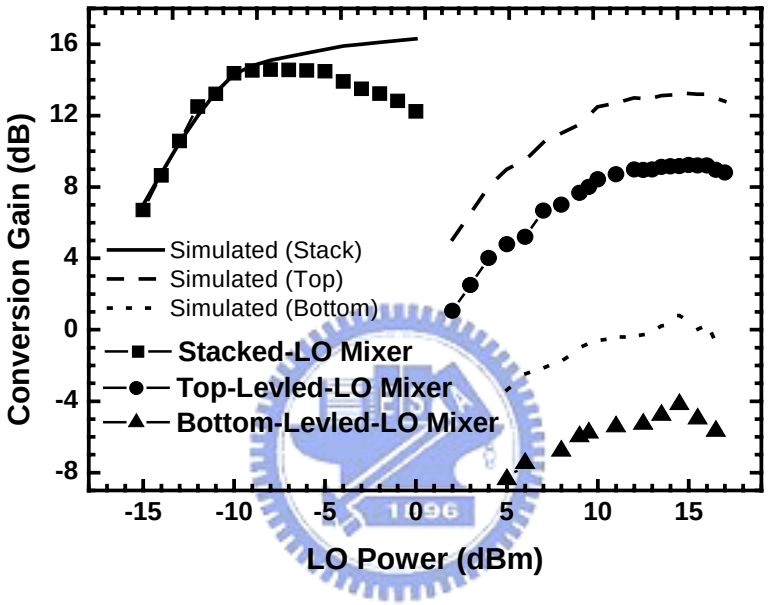


Fig. 2-9. The measured and simulated conversion gain as a function of the LO power of the stacked-LO, and leveled-LO mixers.

As discussed in the section previously, the leveled-LO mixer inevitably needs more LO pumping powers for the LO current fully switching, and the reason is that the leveled-LO mixer operates using the transistor second-harmonic currents. The leveled-LO cell requires extra 10 dBm LO power to perform the current commutation as analyzed previously. In addition, the loss of the polyphase filter used in the stacked-LO mixer is 2.4 dB while that of the leveled-LO mixer is about 6.5 dB according to our simulation. The measurement result is closed to our analysis as the polyphase loss is considered.

As shown in Fig. 2-10, the measured IP_{1dB}, IIP_3 and IIP_2 performances of the 5.2 GHz GaInP/GaAs HBT stacked-LO sub-harmonic mixer are –18 dBm, –5 dBm, and

13 dBm, respectively. Figure 2-11 shows the measured power performances of the leveled-LO mixer when the IF frequency is 100 MHz. The IP_{1dB}, IIP_3, and IIP_2 of the top-LO-configuration are -15 dBm, -7.5 dBm, and 17 dBm, respectively while the IP_{1dB}, IIP_3, and IIP_2 of the bottom-LO-configuration are -4 dBm, 5 dBm, and 17dBm. The bottom-LO-configuration mixer attains a wider dynamic range because of the higher IP_{1dB} and IP_3.

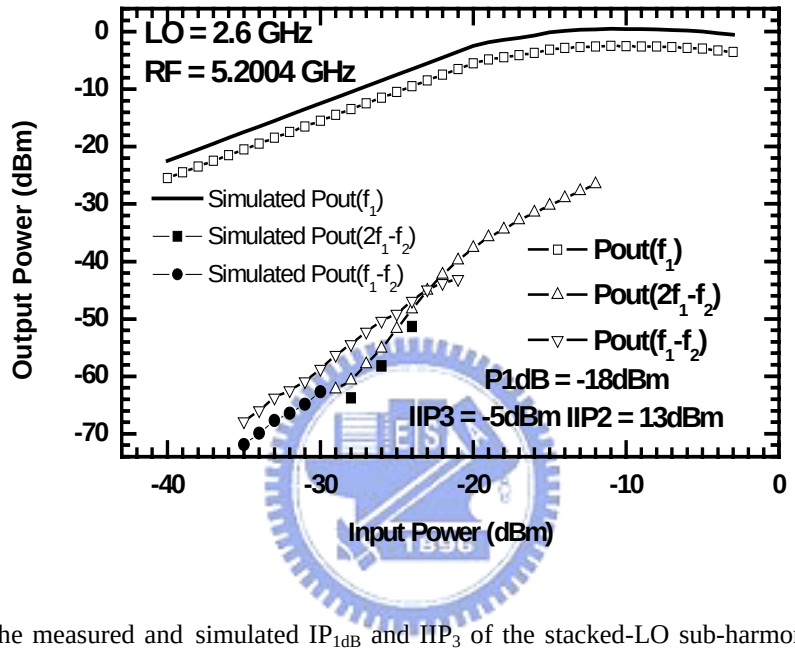


Fig. 2-10. The measured and simulated IP_{1dB} and IIP_3 of the stacked-LO sub-harmonic GaInP/GaAs HBT Gilbert downconversion mixer.

The measured 1/f noise corner of the GaInP/GaAs HBT device used in the stacked-LO mixer is shown in Fig. 2-12. The 1/f noise corner can be as low as 400 Hz [8]. As shown in Fig. 2-13, the measured double sideband noise figure of the stacked-LO sub-harmonic mixer is 24 dB from 100 KHz to 100 MHz. The slope of the measured noise figure is kept constant without the appearance of the 1/f noise. According to previous works [26], [27], the device 1/f noise and the parasitic capacitance in the current source dominate the low frequency noise performance of the direct-conversion mixer.

Some excellent works of direct-conversion mixers with low 1/f noise are achieved in the CMOS technologies. Reducing the noise pulses in LO switches [26], designing novel LO switches [35], [36], and canceling the tail current parasitic capacitance with inductors [37] are useful techniques to improve the noise

performance of CMOS direct-conversion mixers.

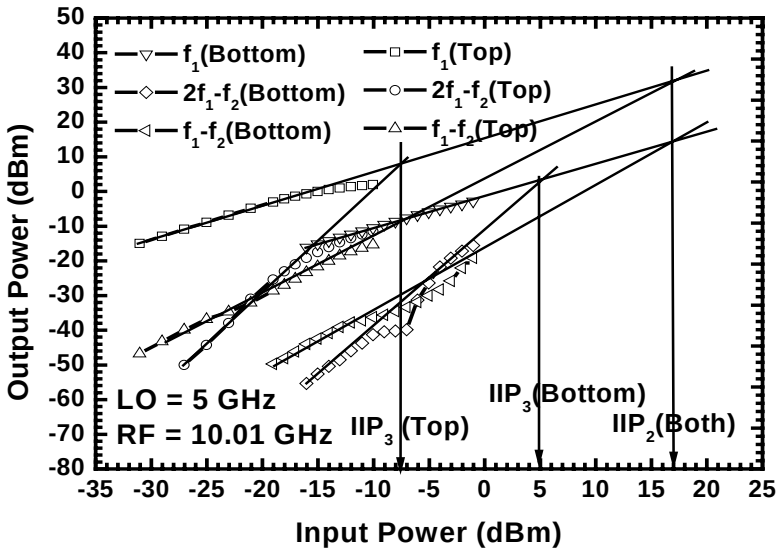


Fig. 2-11. The P_{1dB}, IIP_3 and IIP_2 of the top-LO-configured and bottom-LO-configured sub-harmonic mixers.

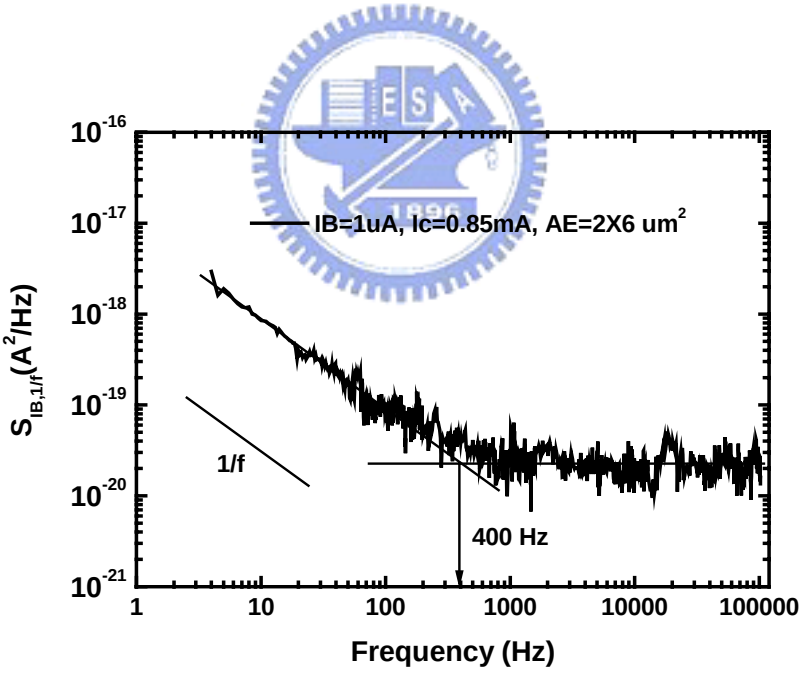


Fig. 2-12. Measured low-frequency noise spectrum of the GaInP/GaAs HBT ($AE=2x6um^2$, IC=0.85mA, and IB=1uA).

The ledge-passivated GaInP/GaAs HBT devices naturally have better 1/f noise performance than the CMOS devices [8]. Moreover, the semi-insulating GaAs substrate eliminates the parasitic capacitance at the tail current [26] and thus the indirect noise no longer degrades the low-frequency noise performance of the

GaInP/GaAs HBT mixers. The double sideband noise figure in this work is not excellent owing to the extra resistors used in the mircomixer input stage and the lacking of the noise figure optimization in our circuit. However, the GaInP/GaAs HBT technology potentially can be used to implement very high performance direct-conversion mixers with low 1/f noise.

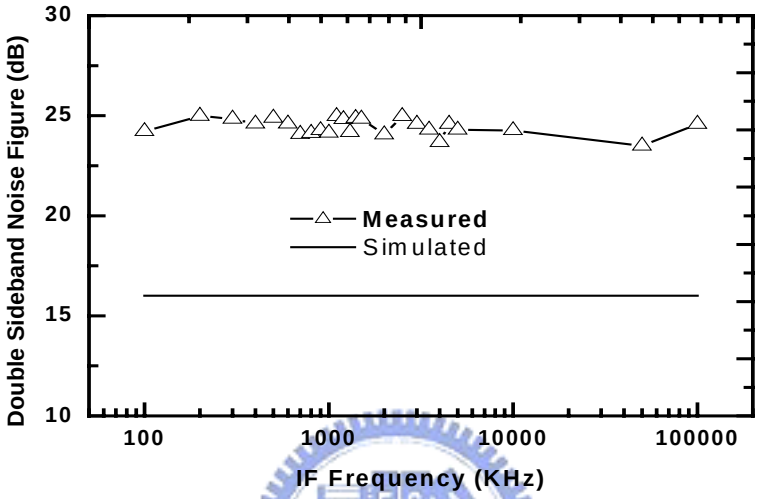


Fig. 2-13. The measured and simulated DSB noise figure of the stacked-LO sub-harmonic mixer.

Recently, the passive CMOS mixers [35], [38]-[40] exhibit excellent noise performance. Although the CMOS device intrinsically has poor 1/f performance, the passive CMOS mixer can achieve excellent noise performance and the corner frequency of the noise figure is as low as 30 KHz. The passive CMOS mixer consists of a low noise input transconductance input stage, CMOS switches, and output filters. The low noise figure can be achieved because the low noise tranconductance input stage (or the LNA) effectively moderates the noise of the following stage [35], [39] and the large-sized CMOS switch [39], [40] prevents the 1/f noise by applying rail-to-rail square wave LO signals [38], [39]. Obviously, the heavily-driven square-waved LO pumping signals can not be employed in the conventional active Gilbert mixer. There might be many advantages using the CMOS passive mixer in terms of the low 1/f noise and high IIP_2; however, the circuit complexity and the area wasted by the compensation capacitors of the filters [38] are the trade-offs of CMOS passive mixers.

The measured double sideband noise figure of the top-LO-configuration sub-harmonic mixer is 24 dB while the bottom-LO-configuration sub-harmonic mixer exhibits 22 dB double sideband noise figure when the IF frequency is 50 MHz. Because of the output blocking capacitor, the noise figure is not measured at the low frequencies. The bottom-LO-configuration mixer using fewer transistors has a better double sideband noise figure, even if the resistor for the input impedance matching may degrade the noise figure, as shown in Fig. 2-3(b).

Table 2-2: The Simulated Noise Contribution of Each Device for The Active Sub-Harmonic Mixers

Stacked-LO		Top-LO		Bottom-LO	
Q2	15%	Qin1	24%	Q5	22%
Q11	12%	Qin2	24%	Q6	22%
R4	8%	Q1	6%	Q7	22%
R1	8%	Q2	6%	Q8	22%
R2	8%	Q3	6%	RL1	2.6%
Q7	4%	Q4	6%	RL2	2.6%
Q8	4%	Q5	6%	Q1	1.4%
Q9	4%	Q6	6%	Q2	1.4%
Q10	4%	Q7	6%	Q3	1.4%
Rcc1	4%	Q8	6%	Q4	1.4%
Rcc2	4%	The rest	4%	The rest	1.2%
Q3	4%				
Q4	4%				
Q5	4%				
Q6	4%				
The rest	9%				

The noise of the direct conversion mixer basically results from the LO switch and the RF input stage. Because the 1/f noise of the GaInP/GaAs HBT device is very small, the noise level is dominated by the RF input stage thermal noise. Our simulation shows a lower noise figure when compared with the experimental results. The discrepancy between the simulation and the measurement are caused by the difficulties in modeling the noise parameters of the HBT device such as base access resistance in the Gummul-Poon model. Thus, the simulated noise might be under estimated. The contribution from the RF input stage transistor might be higher in the

real circuit because of the inaccuracy in modeling the base access resistance. Table 2-2 summarizes the noise contribution of each device used in the active sub-harmonic mixers. For the stacked-LO topology, the micromixer input stage (R_1, R_2, R_4, Q_1, and Q_{11}) produces 51% noises. The RF input stage (Q_{in1} and Q_{in2}) of the top-LO configuration produces 48% noises. Finally, 88% of the noises in the bottom-LO sub-harmonic mixer are caused by the RF input stage (Q_5-Q_8). A low noise input stage is important to improve the noise figure for all the sub-harmonic mixers.

The sub-harmonic mixer using top and bottom LO topologies have the conversion gain of 13 dB and 0 dB, as depicted in Fig. 2-14. Both mixers have about 300 MHz IF-bandwidth. When the IF frequency is below 20 MHz, the conversion gain rolls off due to the on-chip DC blocking capacitors in the output buffer.

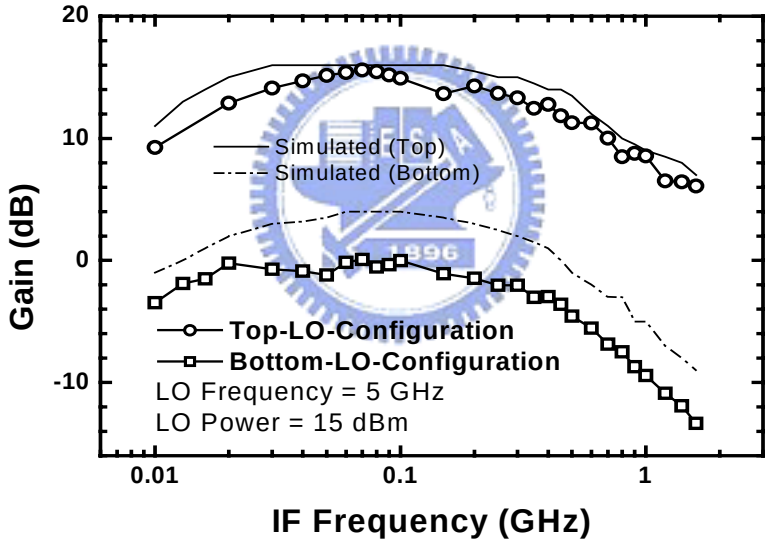


Fig. 2-14. The measured and simulated conversion gain as a function of the IF frequency of the top-LO-configured and bottom-LO-configured sub-harmonic mixers.

The return losses of all are shown in Fig. 2-15. The measured RF S_{11} and IF S_{22} of the stacked-LO mixer are better than -18 and -10 dB, respectively. The measured S_{11} of the bottom-LO-configured mixer is below 10 dB. The S_{11} of the top-LO-configured mixer has a notch at 10 GHz and it is below -10 dB from 8.2 GHz to 12.5 GHz. The inductors used for the impedance matching in the top-LO configuration cause this notch of the RF input return loss. For the leveled-LO mixers, the RF inputs are differential. The experimental results of the S_{11} are obtained by

measuring one of the RF differential ports when the other RF input port is terminated by 50 ohms load.

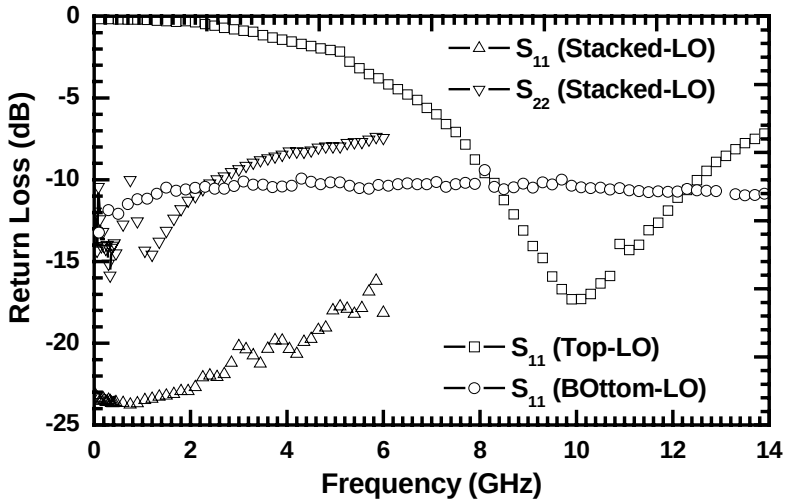


Fig. 2-15. The measured return loss of the stacked-LO, top-LO-configured, and bottom-LO-configured sub-harmonic mixers.

The measured performances of all three different types of the sub-harmonic Gilbert mixers demonstrated in this work are summarized in the table 2-3. Three different types of the Gilbert sub-harmonic mixers are demonstrated using 2 um GaInP/GaAs HBT technology in this work. Because the GaAs semi-insulating substrate eliminates the substrate effect, the intrinsic performance of the 2LO-to-RF isolation can be investigated among these three different sub-harmonic mixer topologies. According to our experiment results and analysis, the stacked-LO sub-harmonic mixer is the best topology to achieve the highest 2LO-to-RF isolation. A record-high 2LO-to-RF isolation is accomplished when RF frequency is around 5 GHz.

The design trade-offs of the conventional sub-harmonic topologies are discussed in this dissertation. The stacked-LO sub-harmonic mixer can operate with the smallest LO pumping power at the cost of a higher DC voltage supply. On the other hand, the leveled-LO sub-harmonic mixers including the top-LO-configured and the bottom-LO-configured mixers can operate in higher frequencies. In addition, there are

still some design trade-offs in the two leveled-LO mixer topologies. The top-LO-configuration mixer has higher conversion gain and 2LO-to-RF isolation but the bottom-LO-configuration mixer has advantage in terms of the power consumption, the linearity and the RF-to-IF isolation.

The measured 1/f noise corner of the 2 um GaInP/GaAs HBT device is about 400 Hz as demonstrated in this work. The measured slope of the low-frequency noise figure keeps constant from 100 KHz to 100 MHz, and the 1/f noise corner does not appear. The HBT device used in this work is adequate to achieve high performance direct-conversion sub-harmonic mixer with small low-frequency noise figure.

Table 2-3: The Measured Performances

	Three-Level Stacked-LO	Top-LO-Configuration	Bottom-LO-Configuration
RF frequency (GHz)	5.2	10	10
Gain (dB)	14.5	13	0
2LO-to-RF Isolation (dB)	75	59	32
2LO-to-IF Isolation (dB)	64	46	48
LO-to-RF Isolation (dB)	50	32	23
LO-to-IF Isolation (dB)	40	32	35
RF-to-IF Isolation (dB)	36	18	30
IP1dB (dBm)	-18	-15	-4
IIP3 (dBm)	-5	-7.5	5
IIP2 (dBm)	13	17	17
Double Sideband Noise Figure (dB)	24	24	22
DC Current (mA)	4*	2	0.8

* Including the output buffer

2.2 Novel Highly Symmetrical Sub-Harmonic Gilbert Mixer Using Compensated Stacked-LO Stage

The direct conversion architecture plays a dominant role in the RF receiver design. The integration level of the direct conversion receiver is very high but suffers from the self-mixing problem; therefore, sub-harmonic mixer topologies [3] are proposed. The stacked-LO sub-harmonic mixer [3] contains two stacked Gilbert cells and these Gilbert cells switch the RF currents in quadrature phase.

A Gilbert multiplier can be used as the frequency doubler [42] for the stacked-LO cell. A novel highly symmetrical stacked-LO doubling cell [43], [44] is employed to improve the LO speed, IIP_2 and the RF-to-IF isolation. In general, the HBT device generates output collector current with a time delay with respect to the input base-emitter voltage. This time delay limits the speed of the LO stage as well as the performances of IIP_2 and RF-to-IF isolation. When two quadrature LO signals are injected into a conventional stacked-LO doubler as shown in Fig. 2-16, the signal from node X to node Z suffers from a larger time delay when compared with the signal from node Y to node Z. This time delay generates a DC term (-1/2sinθ) in the conventional stacked-LO doubling cell [43], [44] as shown in Fig. 2-16.

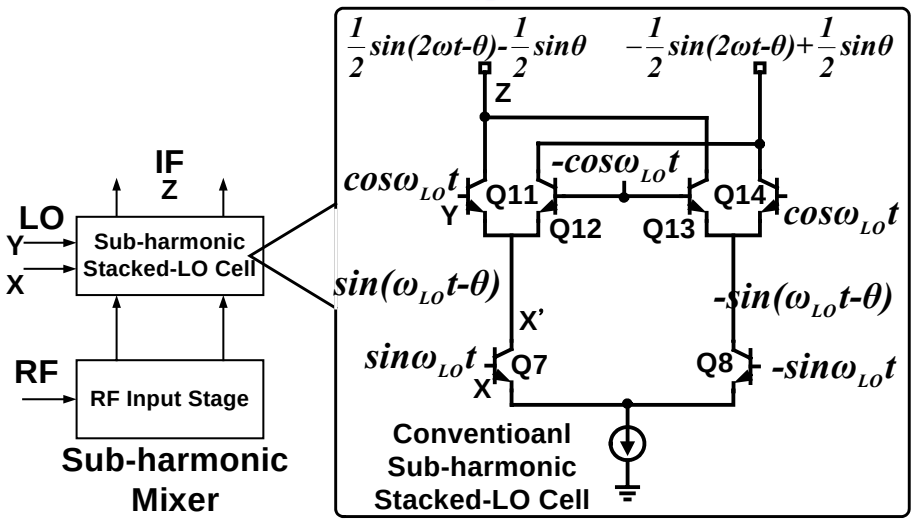


Fig. 2-16. The conventional stack-LO doubler with the time delay effect.

Assuming that the delay between the upper and lower input signals is defined as ϕ, then the output signal is:

$$\sin\omega t \times \cos(\omega t - \phi) = \frac{1}{2}\sin(2\omega t - \phi) + \frac{1}{2}\sin\phi \tag{2.4}$$

As shown in equation (2.4), the DC term of the output signal is 0.5sinϕ. This DC term also makes the notorious DC offset problem in the direct-conversion system more seriously. The time delay of the LO stage is simulated, and the time delay is 5.1 ps or 9.2^{O} for the 0.35um SiGe HBT technology when the LO input signal for the 2LO stage is 5 GHz. On the other hand, if the nodes A and B as shown in the Fig. 2-17(b) are connected together, the output signal becomes:

$$\begin{aligned} A + B &= [\cos\omega t \cdot \sin(\omega t - \phi) + \sin(\omega t) \cdot \cos(\omega t - \phi)] \\ &= \sin(2\omega t - \phi) \end{aligned} \tag{2.5}$$

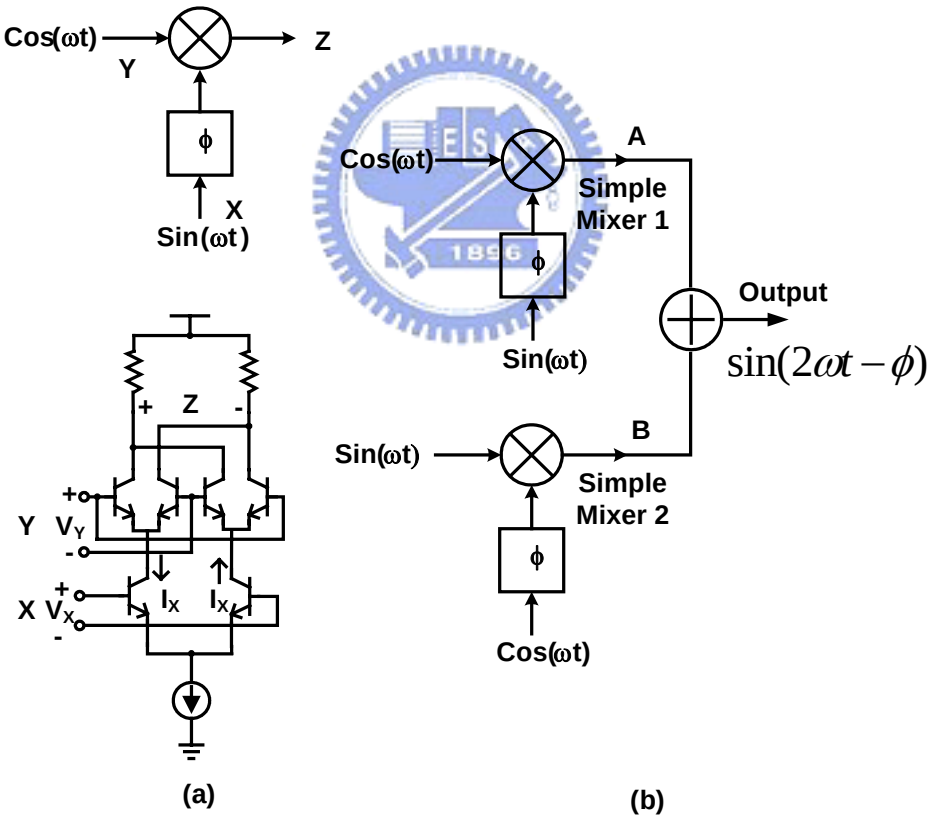


Fig. 2-17. (a) A simple multiplier; and (b) a block diagram of the phase-delay cancelled multipliers pair.

Figure 2-18 shows the fully symmetrical 2LO cell. Transistors Q_7, Q_8, Q_{11}, Q_{12}, Q_{13}, and Q_{14} form a simple multiplier (the simple multiplier 1 in Fig. 2-17(b)) while transistors Q_9, Q_{10}, Q_{15}, Q_{16}, Q_{17}, and Q_{18} form the other mixer (the simple multiplier 2 in Fig. 2-17(b)). When their output ports are connected as shown in Fig. 2-18, the

DC term caused by the transistor time delay can be canceled at the IF port as shown in equation (2.5). The output IF signal shown in Fig. 2-18 can be described as follows:

$$\begin{aligned}&\cos\omega_{RF}t\times\sin(2\omega_{LO}t-\phi)\\&=\sin(\omega_{RF}t+2\omega_{LO}t-\phi)-\sin(\omega_{IF}t+\phi)\end{aligned}\tag{2.6}$$

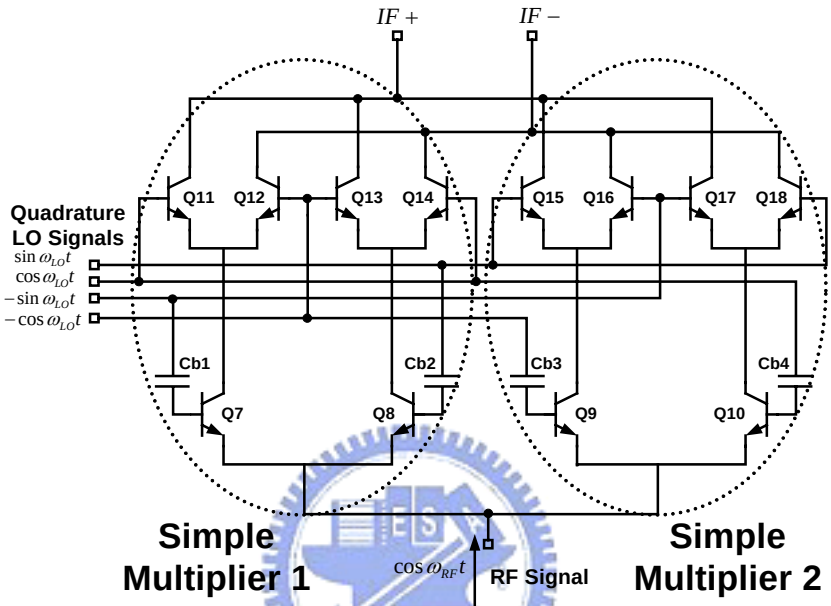


Fig. 2-18. Fully symmetrical 2LO cell with the time delay compensation ability (neglecting the biasing circuits).

According to (2.6), the output IF signal is the product of the 2LO and the RF signals. Consequently, the double balanced sub-harmonic micromixer with time-delay compensated multiplier is proposed and the circuit schematic is shown in Fig. 2-19. The GaInP/GaAs HBT sub-harmonic mixer in Fig. 2-19 has a single-ended micromixer input stage [29], [30], and the resistor achieves the input impedance matching. The micromixer input stage consists of transistors Q_1-Q_4 together with resistors to facilitate the input impedance matching. The micromixer input stage improves the frequency response [29] when compared with the widely used emitter-coupled differential pair input stage. Therefore, the RF input frequency can be easily extended to 10 GHz. The RF signal is 10.0001 GHz, the LO signal is 5 GHz and the IF signal is 100 KHz.

As shown in Fig. 2-19, the LO time-delay compensated multipliers consists of

transistors Q_7-Q_{30}. The transistors Q_7-Q_{30} form two LO networks. One LO network consists of transistors Q_7-Q_{18} and the other consists of transistors Q_{19}-Q_{30}. The double balanced structure used here is helpful to improve the port-to-port isolation. This novel LO cell has the ability to equal the time-delay when they are used to double the LO frequency. A passive poly-phase filter as shown in the Fig. 2-19 is employed to generate the 5 GHz LO quadrature signals. The other double balanced sub-harmonic micromixer with time-delay compensated multiplier using 0.35 um SiGe HBT technology is demonstrated and its topology is shown in Fig. 2-20.

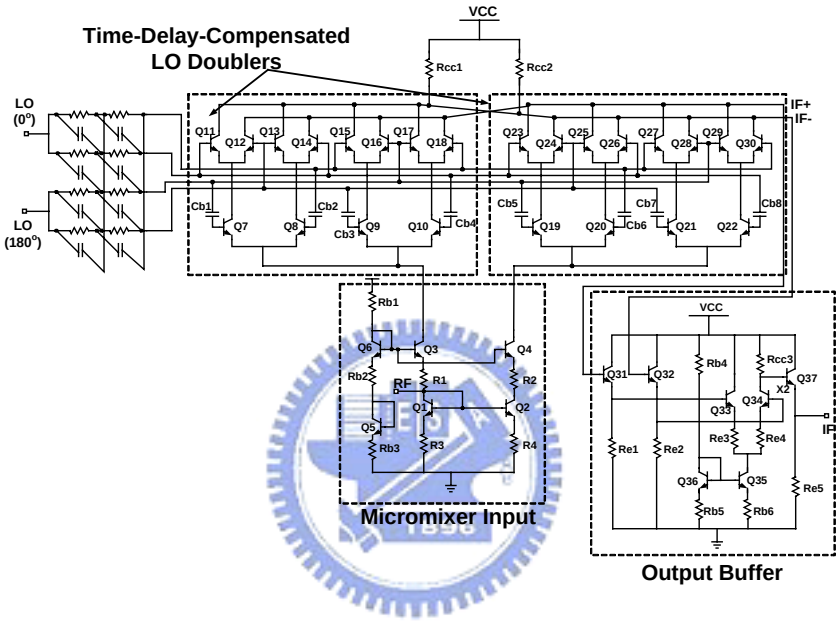


Fig. 2-19. The circuit schematic of the GaInP/GaAs HBT 10 GHz double-balanced sub-harmonic mixer with the LO time-delay compensation.

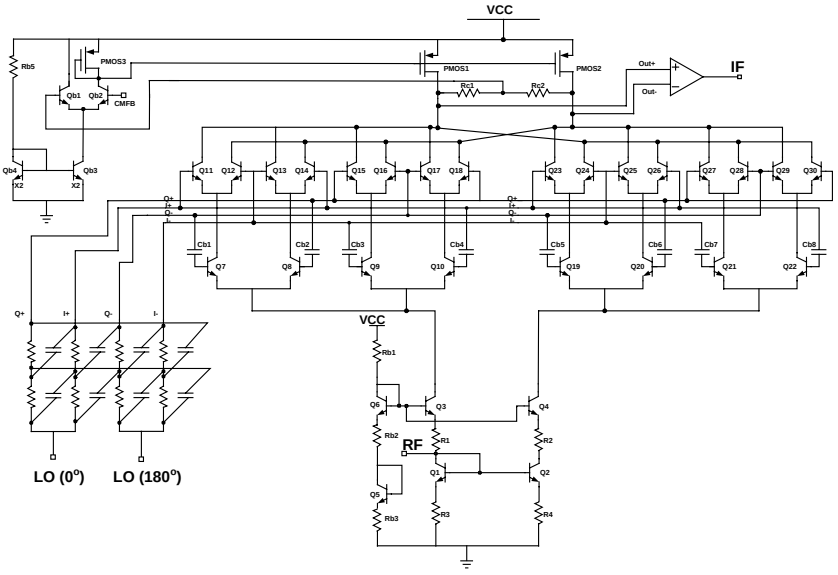


Fig. 2-20. The circuit schematic of the double balanced SiGe BiCMOS 10 GHz sub-harmonic down-conversion micromixer for compensating the LO time-delay neglecting some biasing circuits.

The GaInP/GaAs HBT device has the peak cut-off frequency of 40 GHz and BV_{CEO} of 13 V. The DC supply voltage is 5 V and the current consumption of the mixer core is 4 mA. The die photo of the 10 GHz double-balanced down-conversion sub-harmonic mixer is shown in Fig. 2-21 and the die size is 1mm x 1mm.

As shown in Fig. 2-22, the measured power performance of IP_{1dB}, IIP_3, and IIP_2 are –12 dBm, 2 dBm and 33 dBm, respectively when the IF frequency is 100 KHz. The time-delay-compensated LO cell provides higher order symmetry [44]. Even-order harmonics can be eliminated and the IIP_2 performance can be improved. Moreover, the GaAs technology also helps to maintain the balance of the sub-harmonic mixer as described in the introduction.

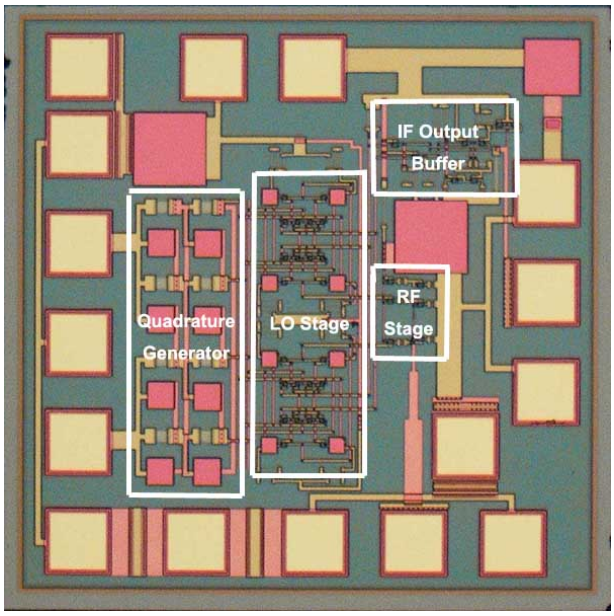


Fig. 2-21. The photomicrograph of the GaInP/GaAs HBT 10 GHz sub-harmonic mixer with the LO time-delay compensation.

The IIP_2 of some excellent BJT-type sub-harmonic Gilbert mixers are compared in Table 2-4. As described in the introduction, it is difficult to achieve good IIP_2 performance at high frequencies [45]. Our work has second to none IIP_2 performance for the RF frequency around 10 GHz when compared with other works because a high-speed and fully balanced LO stage is achieved using GaInP/GaAs HBT technology [45].

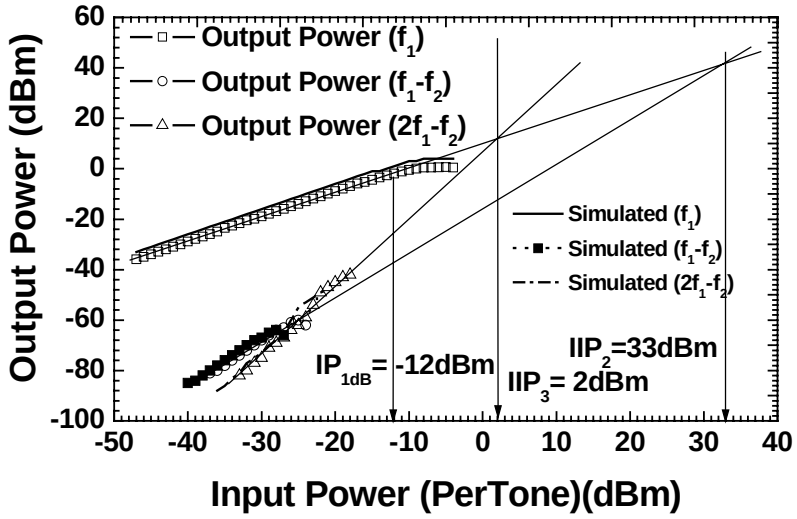


Fig. 2-22. The measured and simulated power performances of the 10 GHz sub-harmonic mixer with the LO time-delay compensation.

Table 2-4: The Comparisions of the IIP_2 of Sub-Harmonic Gilbert Mixers

	GaAs Work	Ref [3]	Ref [20]	Ref [21]	SiGe Work
Technology	2 um GaInP/ GaAs HBT	0.5 um SiGe	0.5 um SiGe	0.35 um SiGe	0.35 um SiGe
RF (GHz)	10	1	5-6	2	10
IIP_2 (dBm)	33	35	29	27	10
IP_{1dB} (dBm)	-12	N/A	-5.4	-16	-20
RF-to-IF Isolation (dB)	-50	N/A	N/A	N/A	-45
DSB Noise (dB)	14	7	N/A	8	16
Power (mW)	20	9.24	16.5	12.6	9.9
Die Size (mm^2)	1	1.92	4.14	0.175	0.985

The demonstrated mixer has better than 15 dB input return loss and 11 dB output return loss from DC to 20 GHz. The measured RF-to-IF isolation is about –50 dB when the RF frequency is 10 GHz. The good RF-to-IF isolation demonstrated here indicates that the time-delay compensated LO doublers are effective. The LO-to-RF the LO-to-IF, 2LO-to-RF [20] and the 2LO-to-IF isolations are –65 dB, –48 dB, –75 dB and –62 dB, respectively, when the LO frequency is 5 GHz.

The Low-frequency noise figure is another important issue for a

direct-conversion receiver and the 1/f noise dominates the low-frequency noise figure of the direct-conversion mixer [9]. Generally speaking, the CMOS direct-conversion mixer suffers from high 1/f noise corner. The current conduction mechanism of a ledge-passivated GaInP/GaAs HBT is the bulk conduction [8], thus the 1/f noise performance is better than that of the surface-conducting CMOS device. The measured low frequency noise of the GaInP/GaAs HBT device is shown in Fig. 2-23. The 1/f noise corner is about 400 Hz and the measured slope is 20 dB/decade.

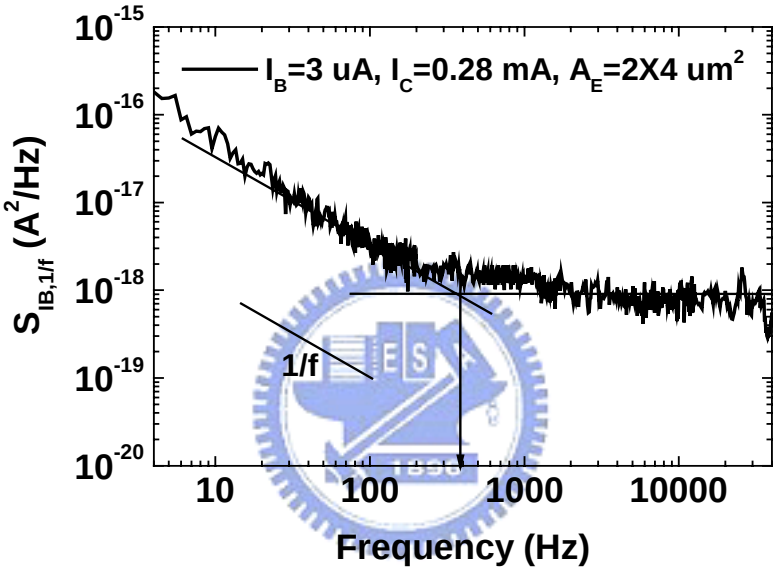


Fig. 2-23. Measured low-frequency noise spectrum of the HBT (AE = 2X4 um^2, IC=2.8 mA, and IB = 3 uA).

Figure 2-24 shows the measured double sideband noise figure and conversion gain as a function of IF frequency. The measured IF bandwidth is 30 MHz. Because of the characteristic of the HBT device, the measured low-frequency noise keeps constant from 100 KHz to 40 MHz without extra circuit design techniques [9]. As shown in Fig. 2-24, the double sideband noise figure is about 14 dB without the appearing of the 1/f noise corner. Compared with the former result [9], this work has 2 dB improvement of noise figure. It is because the base resistance of the heavily doped base in the GaInP/GaAs HBT device is much smaller and thus the thermal noise is less.

The series sub-harmonic doubler core presented in this work contains much more transistors when compared with the parallel sub-harmonic core [21]. The resistor Rb dominates the thermal noise floor and thus the series sub-harmonic doubler cores suffer from more noise contributors. On the other hand, the thermal noise is smaller in the parallel structure because the resistors Rb are in parallel. The P_{1dB} of the presented structure is also limited in the series sub-harmonic mixer in this work. Because there are too many Gilbert cell stacked together, the signals waveform clippings of the demonstrated mixer are more serious than that of the parallel sub-harmonic core.

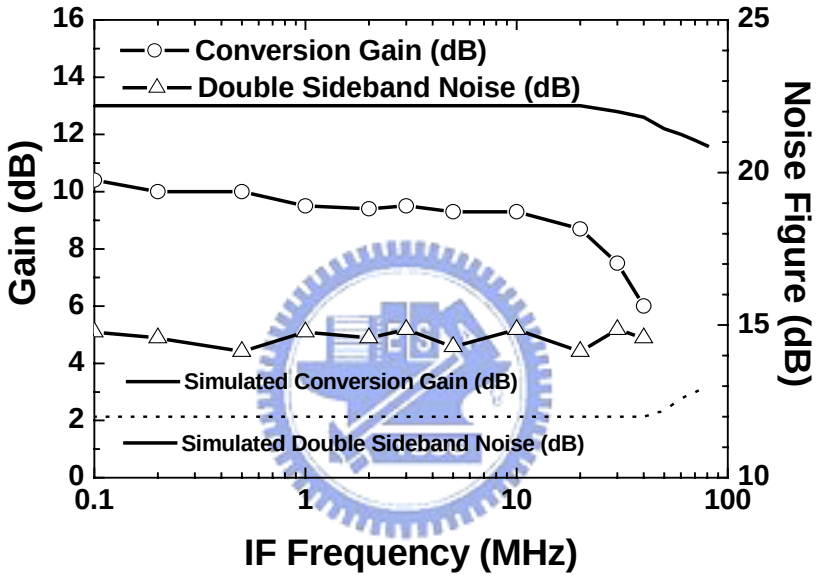


Fig. 2-24. The measured and simulated double sideband noise figure and conversion gain of the 10 GHz sub-harmonic micromixer as a function of IF frequency.

A 10 GHz sub-harmonic Gilbert mixer is also demonstrated in this work using the 0.35 um SiGe BiCMOS technology. The time-delay when the sub-harmonic LO (Local Oscillator) stage generates sub-harmonic LO signals is compensated by using fully symmetrical multiplier pairs. High RF-to-IF isolation and sub-harmonic LO Gilbert cell with excellent frequency response can be achieved by the elimination of the time-delay. The SiGe BiCMOS sub-harmonic micromixer exhibits 17 dB conversion gain, -74 dB 2LO-to-RF isolation, IP_{1dB} of –20 dBm, and IIP_3 of –10 dBm. The measured double sideband noise figure is 16 dB from 100 KHz to 100 MHz because the SiGe bipolar device has very low 1/f noise corner.

When compared with the MOS device, the SiGe HBT device intrinsically possesses very low 1/f noise corner [48][49]. The measured 1/f noise spectrum is shown in Fig. 2-25. The device has the emitter area of 2.97 um ^{2} and the bias condition is the same with the transistors used in the LO cell as shown in Fig. 2-20. The measured 1/f noise corner is around 500 Hz.

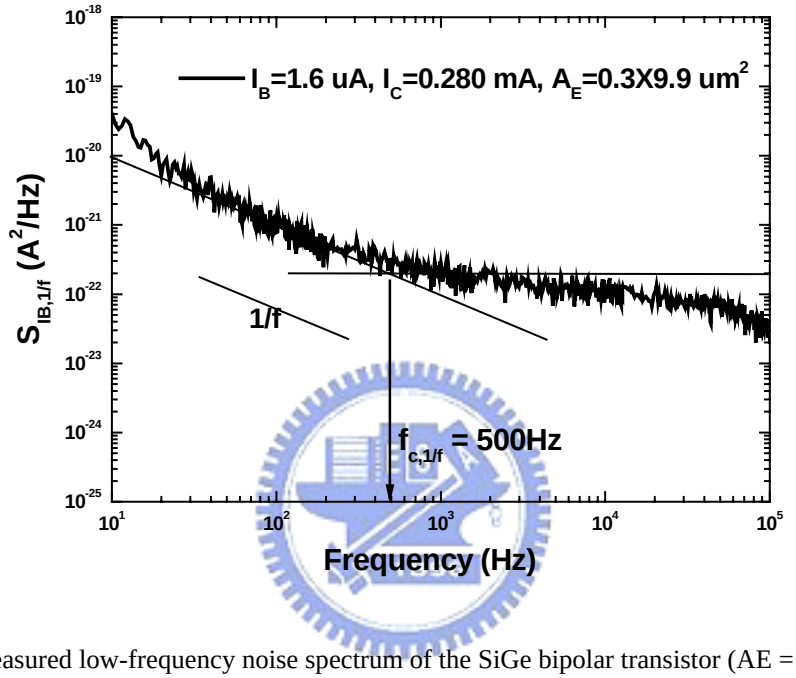


Fig. 2-25. Measured low-frequency noise spectrum of the SiGe bipolar transistor (AE = 0.3 X 9.9 um ^{2}, and IB = 1.6 uA).

As shown in Fig. 2-20, a common-mode feedback technique is used to further increase the conversion gain without sacrificing the signal headroom. Because the PMOS is provided in the SiGe BiCMOS technology, a PMOS current mirror is employed as the loading network instead of resistors. However, the active load needs a common-mode feedback loop to maintain the common-mode bias condition. The transistor Q_{b1}-Q_{b4} is a comparison amplifier, and a resistive sensing scheme is to stabilize the bias point of the PMOS loads. An output buffer is used to perform the differential-to-single conversion and output impedance matching for the on-wafer measurement. This output buffer consists of an asymmetric emitter-degenerated differential amplifier and a common-collector output stage.

The SiGe HBT device used in the circuit has BV_{CEO} of 3.8 V and peak f_T of 49

GHz. The emitter areas of the transistors used in this work are: 0.3 x 9.9 um^2 for the mixer and 0.3 x 13.9 um^2 for output buffer. The PMOS transistor used in this work has gate length of 0.5 um, gate width of 5 um and 5 gate fingers. The SiGe BiCMOS technology provides deep trench isolation, and it is able to reduce the coupling among the SiGe HBT devices. Each PMOS transistor is in its own n-well to reduce the coupling. The current consumption of mixer core is 3 mA. The implemented chip photo of the SiGe BiCMOS sub-harmonic mixer at 10 GHz is shown in Fig. 2-26. The die size is 1 x 0.985 mm^2.

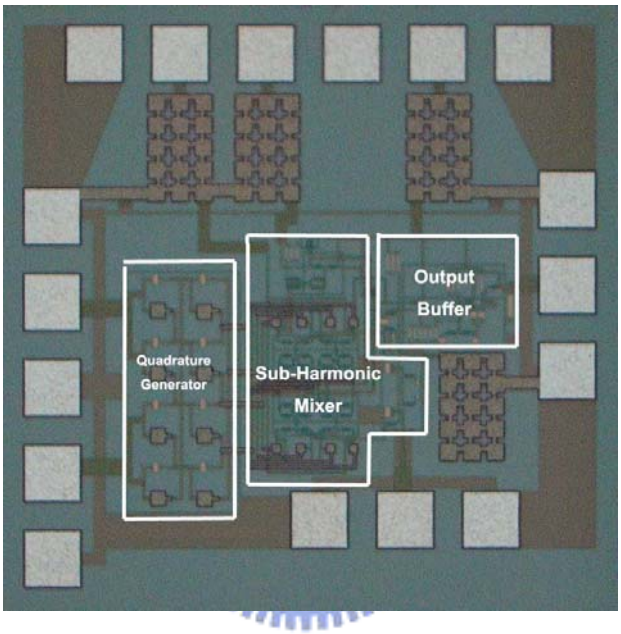


Fig. 2-26. The die photograph of the SiGe BiCMOS 10 GHz sub-harmonic down-conversion mixer for compensating the LO time-delay.

The measured conversion gain as a function of the LO power is shown in Fig. 2-27. As shown in Fig. 2-27, the SiGe BiCMOS mixer has the conversion gain of 17 dB. The measure IP_{1dB}, IIP_3, and IIP_2 of the SiGe BiCMOS sub-harmonic mixer are shown in Fig. 2-28. The measured power performance of IP_{1dB}, IIP_3, and IIP_2 is –20 dBm, -10 dBm and 10 dBm, respectively. The IIP_2 is not very excellent resulting from the mismatches of the IF amplifier and the PMOS loading transistors ($PMOS_1$ and $PMOS_2$). Moreover, the mismatches of the polyphase filter used to generate the quadrature LO signal also degrade the balance of the demonstrated mixer.

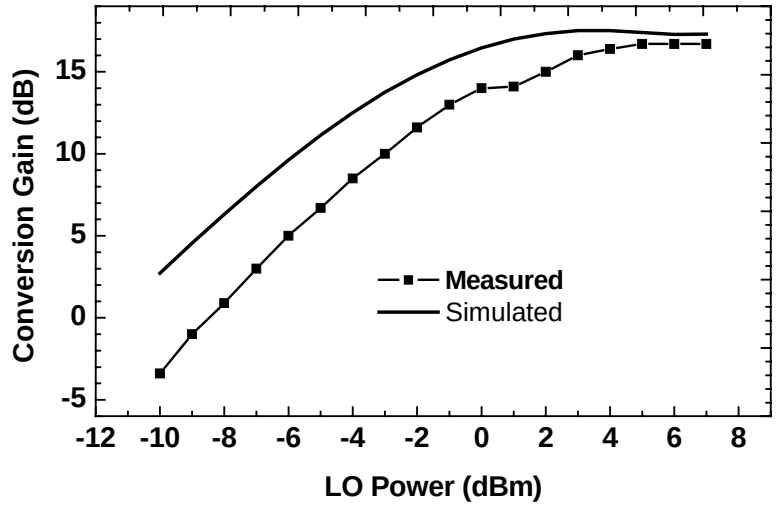


Fig. 2-27. The measured and simulated results of the conversion gain as a function of LO input power of the down-conversion sub-harmonic mixer using the SiGe BiCMOS technology.

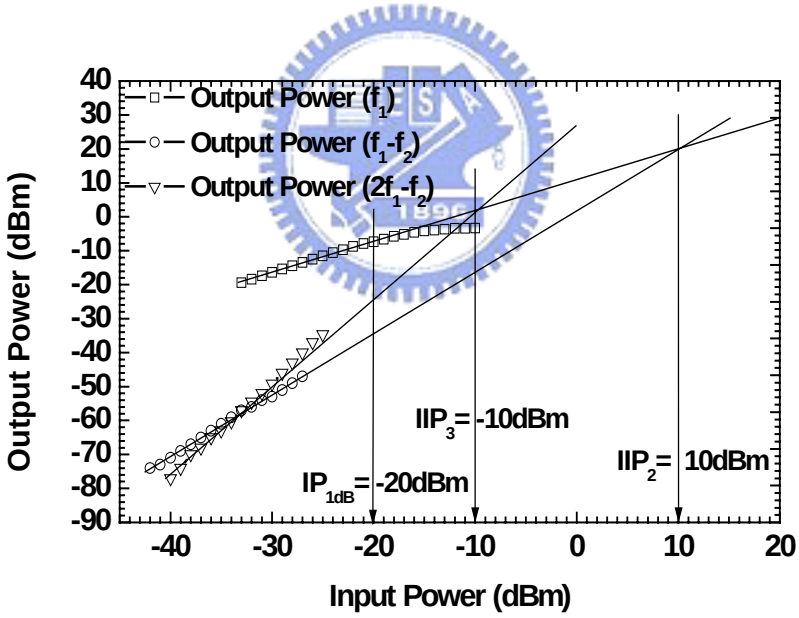


Fig. 2-28. The measured power performance of the 10 GHz sub-harmonic mixer using the SiGe BiCMOS technology.

The SiGe BiCMOS sub-harmonic mixer has 10 dB input return loss, 19 dB output return loss. The sub-harmonic mixer demonstrated in this work exhibits wideband input and output matching bandwidth. For the input impedance matching, it is attributed to the micromixer input stage. The resistive matching method of the micromixer input stage realizes a very wide input matching bandwidth. The chip size

is very compact because only resistors are used to perform input impedance matching. The output matching bandwidth is also very wide resulting from the output Darlington buffer.

Figure 2-29 shows the measured the LO-to-RF isolation and the 2LO-to-RF isolation. The LO-to-RF isolation of the SiGe BiCMOS sub-harmonic mixer is –58 dB when the LO frequency is 5 GHz. Due to the common-base-transistors Q_3 and Q_4, the micromixer input stage has 12 dB improvement of the LO-to-RF isolation in simulation when compared with the conventional differential amplifier input stage. On the other hand, we also simulate the LO-to-RF isolation for the conventional differential RF input pair. The LO-to-RF isolation can be improved about 18 dB when the compensated LO stage is used.

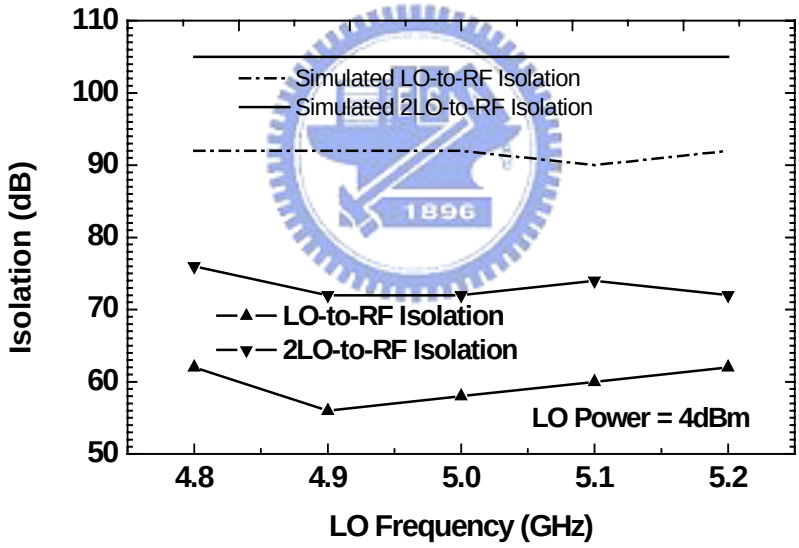


Fig. 2-29. The measured and simulated LO-to-RF and 2LO-to-RF isolations of the sub-harmonic mixer using the SiGe BiCMOS technology.

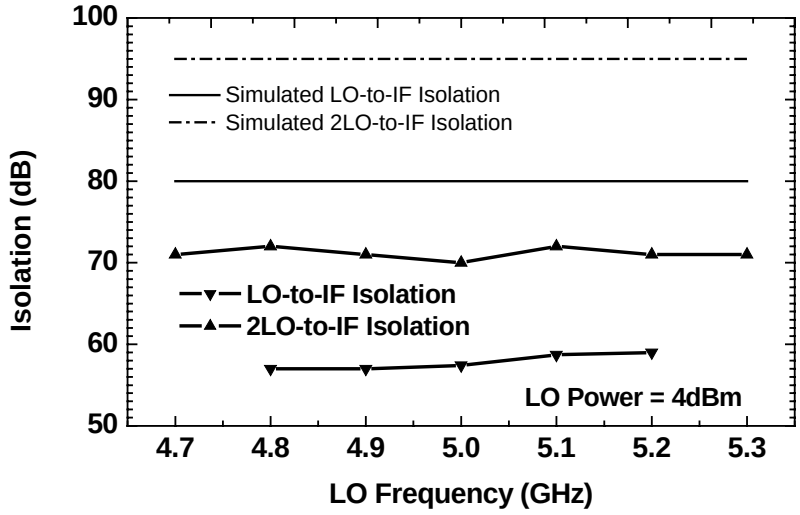


Fig. 2-30. The measured and simulated LO-to-IF and 2LO-to-IF isolations of the sub-harmonic mixer using the SiGe BiCMOS technology.

Figure 2-30 shows the LO-to-IF isolation and the 2LO-to-IF isolation, respectively. The LO-to-IF isolation and the 2LO-to-IF isolation of the SiGe BiCMOS sub-harmonic mixer are –56 dB and –70 dB when the LO frequency is 5 GHz.

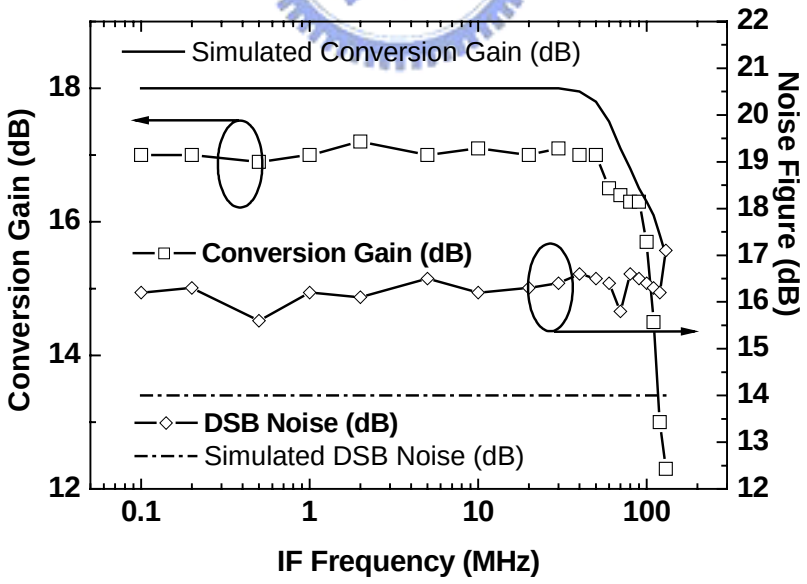


Fig. 2-31. The measured and simulated IF bandwidth and the double sideband noise figure of the sub-harmonic mixer using the SiGe BiCMOS technology.

Figure 2-31 shows the IF bandwidth of the 10 GHz SiGe sub-harmonic mixer,

and the IF bandwidth of the demonstrated mixer is basically limited by the PMOS loading network. The measured 3-dB bandwidth is 100 MHz. The double sideband noise figure is 16 dB. As shown in Fig. 2-31, the slope of the low frequency noise keeps constant when the frequency is down to 100 KHz. Because the SiGe bipolar device has very low 1/f noise corner, the measured low frequency noise figure of the demonstrated mixer keeps constant from 100 KHz to 100 MHz.

In summary, all the sub-harmonic mixers demonstrated in the dissertation is compared in Table 2-5. The GaInP/GaAs HBT sub-harmonic mixer using the LO time-delay compensation has the best performance within all the demonstrated mixers.

Table 2-5: The Measured Performances of the Demonstrated Sub-Harmonic Mixers

	Stacked-LO	Top-LO	Bottom-LO	Compensated LO (GaAs)	Compensated LO (SiGe)
RF frequency (GHz)	5.2	10	10	10	10
Gain (dB)	14.5	13	0	10	17
2LO-to-RF Isolation (dB)	75	59	32	75	72
2LO-to-IF Isolation (dB)	64	46	48	62	70
LO-to-RF Isolation (dB)	50	32	23	65	58
LO-to-IF Isolation (dB)	40	32	35	48	56
RF-to-IF Isolation (dB)	36	18	30	50	48
IP1dB (dBm)	-18	-15	-4	-12	-20
IIP3 (dBm)	-5	-7.5	5	2	-10
IIP2 (dBm)	13	17	17	33	10
Double Sideband Noise (dB)	24	24	22	14	16
DC Current (mA)	4	2	0.8	4	3
Die Size (mm^2)	2	1	1	1	1

Chapter 3

High Performance Up-Conversion Mixers Using the LC Current Mirror and the Lumped Rat-Race Hybrid

The demonstrated up-conversion Gilbert mixers are discussed in this chapter. The up-conversion mixers generally connect with the power amplifier at the output nodes. In most cases, the power amplifiers are single-ended because the antenna is usually single-ended. Therefore, the up-converter is convenient when the output nodes are combined. Output LC current mirror are employed in this work, and this bandpass current mirror is effective to the differential-to-single application.

In order to generate accurate LO signal for the up-conversion Gilbert mixer, an on-chip balun is used. The on-chip balun is a lumped-element rat-race hybrid. The experimental results show that the rat-race hybrid is practical for the up-conversion Gilbert mixer because the excellent port-to-port isolation of a fully balanced mixer is obtained.

The design methodology and the analysis of the LC current mirror including the parasitic resistors are developed in this work. The design consideration of the rat-race hybrid is also obtained. In this work, up-conversion mixers using the LC current mirror and the lumped rat-race hybrid are demonstrated using 0.35 um SiGe HBT technology and GaInP/GaAs HBT technology.

In addition to the passive inductors used in the LC current mirror, the active inductor formed by the conventional common-collector output buffer is also employed. A compact up-onversion Gilbert mixer using the active inductor for the LC current mirror is demonstrated, and the chip area is effectively saved.

3.1 SiGe HBT Up-Conversion Gilbert Mixer Using the LC Current Mirror and the Lumped Rat-Race Hybrid

Because of the excellent port-to-port isolations and compact size, the double balanced Gilbert mixer [2] has been widely used in RFIC applications. A 5.2GHz fully integrated Gilbert upconversion mixer with the single-ended IF port, LO port and RF port is demonstrated using 0.35 um SiGe HBT technology. However, the

advantages of the truly balanced operation are remained in our work. An upconverter with single-ended IF port, LO port and RF port is suitable for stand-along hybrid RF system applications [50]. Figure 3-1 shows the circuit topology of the 5.2 GHz upconverter. The upconversion mixer shown in Figure 3-1 consists of a single-to-differential IF stage [29], [30], an RF output LC current mirror [51], [52] with Darlington output buffer, a LO Gilbert mixer core, and an on-chip lumped-element rat-race hybrid in the LO stage [5], [53], [54].

The mixer input transconductance stage can transform the unbalanced IF input signal into differential RF currents that are needed by the Gilbert mixer core and provide wideband impedance matching. The Gilbert mixer core of the upconverter requires balanced LO signals in order to maintain the truly balanced operation. For this reason, a miniature lumped-element rat-race hybrid is integrated into the upconverter. The integrated lumped rat-race hybrid provides good phase accuracy. The lumped rat-race hybrid input stage generates balanced LO input signals; hence, the conversion gain and port-to-port isolations can be both maintained. There is another obvious advantage that when the integrated lumped-element rat-race hybrid is used to generate differential LO signals, the upconverter does not require extra off-chip trimming method to maintain balanced LO signals. A lumped-element rat-race hybrid consisting of inductors L_3 to L_6, capacitors C_2 to C_8, and an on-chip 50-ohm resistor is incorporated into this circuit to generate balanced LO input signals. A passive LC current mirror is applied at the output of the Gilbert mixer core to provide the differential-to-single conversion and to double the output current at the resonant frequency. It is better to combine the output signals for a stand-along mixer application. Since the output node of the LC current mirror behaves similarly to a high impedance current source, a Darlington output buffer is designed to achieve output matching. In addition, the output buffer is proved that it is able to improve the performance of the conversion gain.

Design concepts used to optimize the value of the LC current mirror and to improve the power gain of the mixer by output buffer are demonstrated in this work. When compared with the lossless output passive matching network, the active output buffer can increase the power gain. The conversion gain can be effectively improved by properly designing the LC current combiner and by adding an active output buffer.

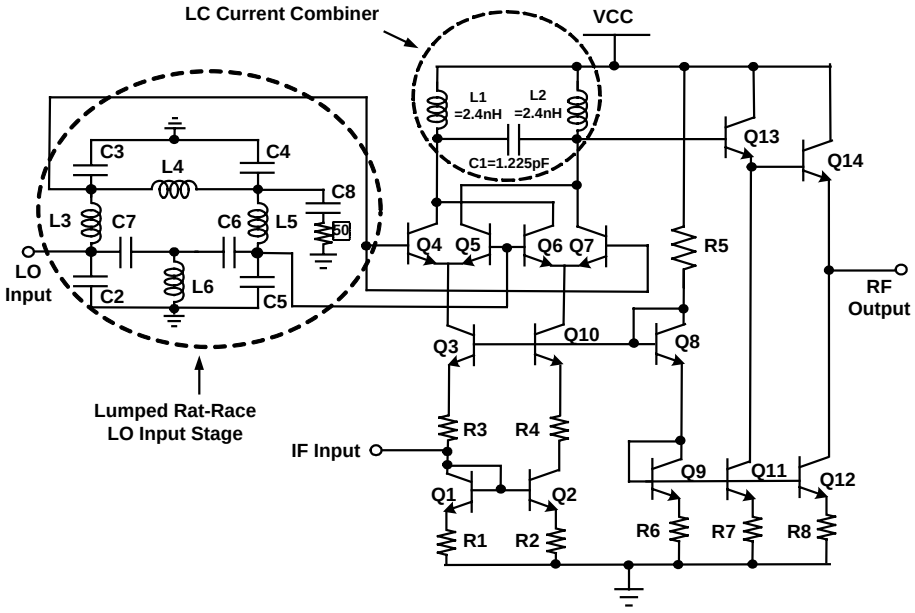


Fig. 3-1. Schematic of the 5.2 GHz SiGe upconverter using the output LC current mirror and the LO lumped balun.

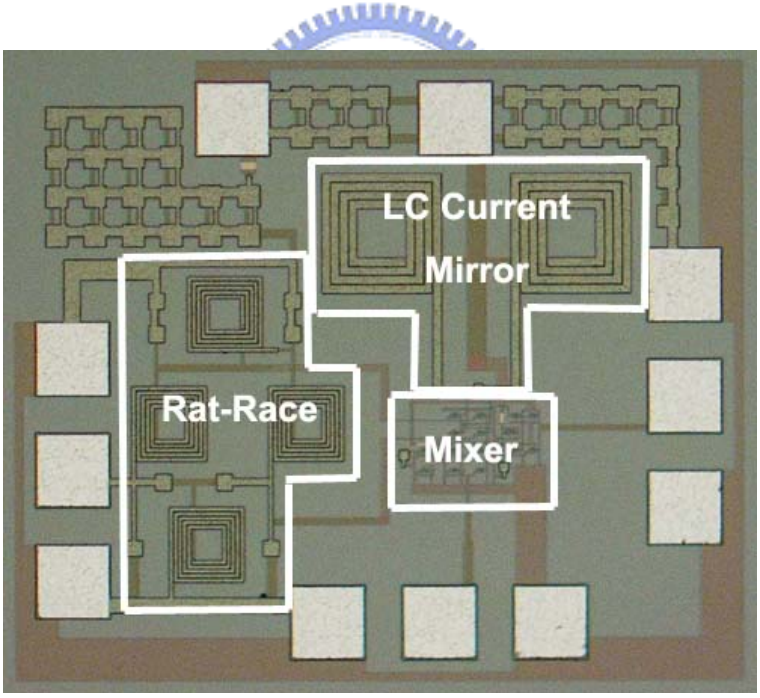


Fig. 3-2. Photograph of the 5.2 GHz SiGe upconverter using the output LC current mirror and the LO lumped balun.

The die photo of the implemented upconverter is shown in Fig. 3-2. The total chip area is 0.98 x 0.83 mm^2 and there are six on-chip inductors. The SiGe HBT device used in this work has the following properties: the emitter width is 0.35 μm, BV_{CEO} equals to 2.5V, and the peak f_T is around 67 GHz. The emitter length of HBT

is 5.1 um with a non-self-aligned and poly-emitter device technology.

As shown in Fig. 3-1, the common base stage, Q_3, has the equal but out of phase transconductance gain as the common emitter stage, Q_2, for the same DC bias currents. Thus, by connecting Q_1 and Q_2 as a current mirror pair, the differential currents needed by the Gilbert cell can be obtained. The mixer input stage used in this work has a very good frequency response because the frequency response of the common emitter stage is improved by lowering the impedance seen at the base of Q_2.

The rat-race hybrid is a microwave device used to generate two balanced signals. A typical distributed rat-race hybrid is shown in Fig. 3-3(a). When the signal is injected at port 1, balanced signals appear at ports 2 and 3 but no signal appears at port 4, as shown in Fig. 3-3(b) and 3(c). The Sparameter of the rat-race hybrid when the signal is injected into port 1 can be determined as follows [53]:

$$
\begin{aligned}
S_{21} &= \frac{2}{j\frac{Z_C}{Z_0} + j\frac{2Z_0}{Z_C}} \\
S_{31} &= -\frac{2}{j\frac{Z_C}{Z_0} + j\frac{2Z_0}{Z_C}} \\
S_{11} &= \frac{j\frac{Z_C}{Z_0} - j\frac{2Z_0}{Z_C}}{j\frac{Z_C}{Z_0} + j\frac{2Z_0}{Z_C}} \\
S_{41} &= 0
\end{aligned}
\qquad (3.1)
$$

where Z_C and Z_0 are the characteristic impedances of the transmission lines in the rat-race and port connection, respectively. According to (3.1), S_{21} and S_{31} are balanced while port 4 is the isolated port because S_{41} equals zero. It can be observed that the output signals of ports 2 and 3 are equal magnitude but out-of-phase because the incident wave travels a distance of λ/4 to port 2 and travels a distance of 3λ /4 to port 3 as shown in Fig. 3-3(b). On the other hand, a destructive interference appears at port

4 because the incident wave travels a distance of λ/2 in the clockwise path and a distance of λ in the counterclockwise path as shown in Fig. 3-3(c). The signal cancellation makes port 4 intersection a virtual short point. The distance from port 4 to port 2 (port 3) is λ/4. Thus, the impedance becomes infinite when looking from port 2 (port 3) into port 4. As a result, the rat-race hybrid can be simplified into the structure shown in Fig. 3-3(d). The impedance at input port when looking into port 2 is Z_C^2/Z. Where Z is the load impedance at port 2 and port 3.

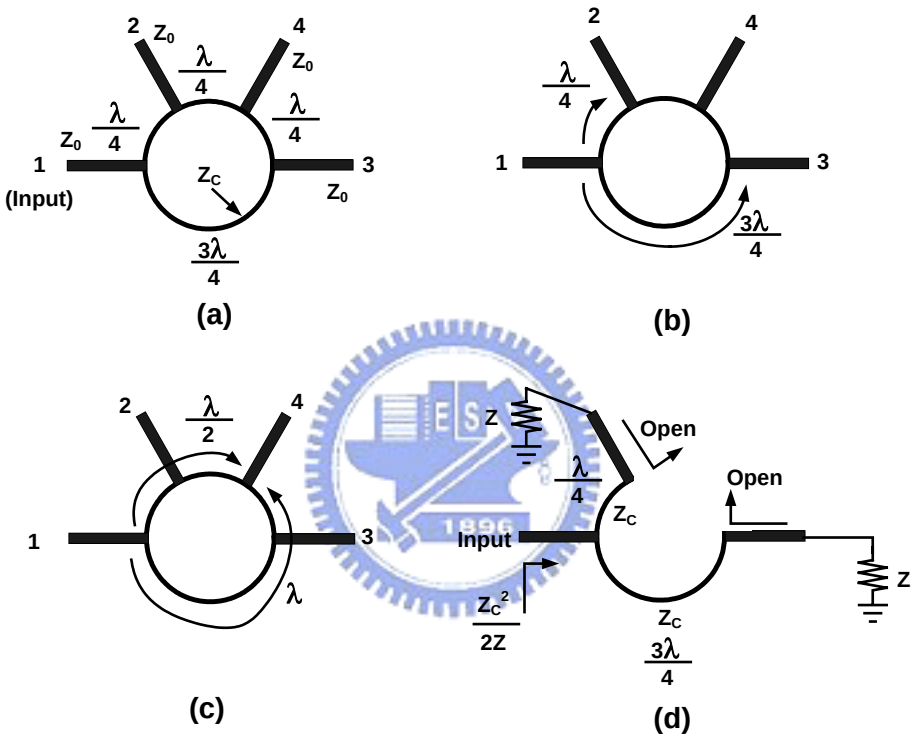


Fig. 3-3. (a) The typical rat-race hybrid; (b) Output balance signals; (c) Signal cancelation at port 4; (d) Impedance of the input port.

For the same reason, the impedance when looking into port 3 is Z_C^2=Z. Thus, the input impedance of port 1 is Z_C^2=2Z. In the special case, the input impedance of port 1 is Z_0 (or 50Ω) when Z equals Z_0 and Z_C is $\sqrt{2}Z_0$. However, the characteristic impedance, Z_C, is not necessary equal to $\sqrt{2}Z_0$ for generating the balanced signals in the LO stage. The impedance at the LO port, Z, is very high, thus the input impedance of port 1 can not be Z_0 even if the characteristic impedance Z_C is $\sqrt{2}Z_0$. The requirement of $\sqrt{2}Z_0$ characteristic impedance is not important in our case because

port 2 and port 3 are always out-of-phase in the rat-race hybrid. The rat-race hybrid used for the mixer LO stage consequently is much easier to be designed.

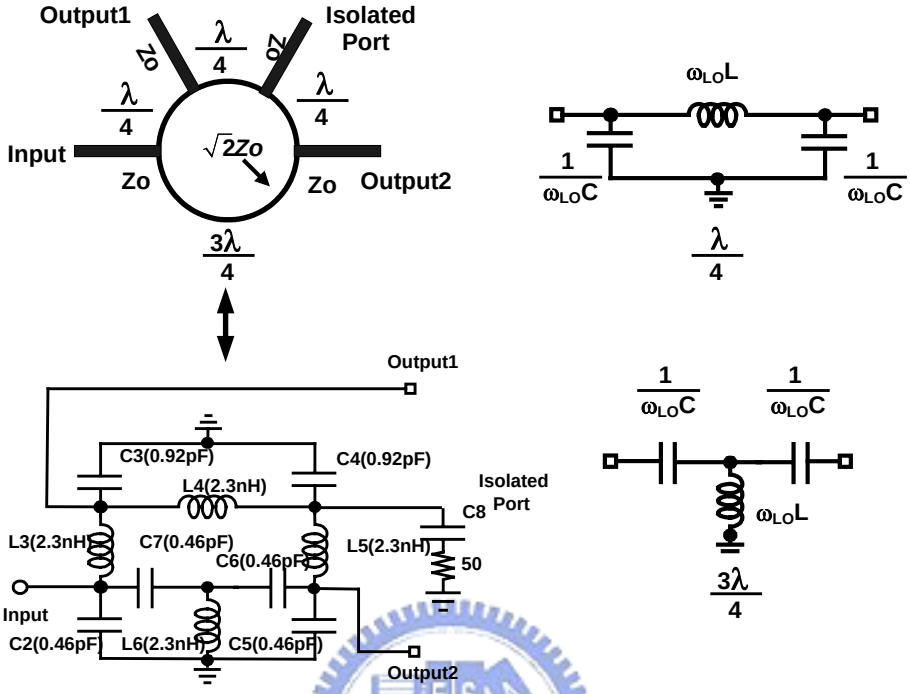


Fig. 3-4. The lumped-element rat-race balun.

The lumped equivalent version is shown in Fig. 3-4. In order to shrink the die size, the quarter-wavelength transmission line is replaced by a π-shaped low-pass lumped network while a three-quarter-wavelength transmission line can be replaced by a T-shaped high-pass lumped network, respectively [5][54]. The π network and the T network in the lumped rat-race hybrid replace 3λ/4 and λ/4 transmission lines at the resonate frequency, I_0, and the equivalent characteristic impedance, Z_C, of each lumped network:

$$Z_C = \sqrt{\frac{L}{C}} \tag{3.2}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

The advantage of integrating the lumped-element rat-race hybrid in a chip is that the on-chip lumped-element rat-race hybrid is very balanced. Extra efforts in the

off-chip board level tuning are needed to accomplish the balanced signals when the distributed rat-race hybrid is implemented in the printed PC board technology. The error in lengths of signal path causes the phase imbalances and can be reduced from the orders of millimeters to micrometers by using IC technologies. Thus, a lumped-element rat-race hybrid is connected at the LO port of the current commutating Gilbert cell (Q_4, Q_5, Q_6, and Q_7) to generate the balanced differential LO signals as shown in Fig. 3-1. The lumped-element rat-race hybrid is equivalent to the distributed rat-race hybrid only at the designed frequency. The bandwidth of the lumped rat-race hybrid is narrower than that of the distributed version but the size of the lumped rat-race hybrid is small enough to fit in the modern IC technology. The values of inductors and capacitors of the lumped rat-race hybrid used for the LO stage determine the resonate frequency. On the other hand, the characteristic impedance does not need to be specified in our case.

For the mixer LO stage, although the lumped rat-race hybrid is smaller and its design seems easier, the performance of the lumped rat-race hybrid is directly affected by the on-chip inductors. The quality factor of an inductor is defined by:

$$Q_L = \frac{L}{R} \tag{3.3}$$

where the resistor, R, is the parasitic series resistance of the on-chip inductor. When the Q is high enough, the effect of the parasitic resistance, R, can be ignored.

High Q and small size inductors are always desirable to the RFIC designers. Some physical approaches are proposed to increase the quality factor of the inductors or transformers [55]-[57], and some works are dedicated to shrink the chip area of the on-chip inductors [58], [59]. In addition, previous work has proposed a method to fabricate variable RF inductor [60]. Although conventional on-chip inductors are used In this work, the lumped rat-race hybrid can be improved using the methods above.

In this work, the values of the inductors used in Fig. 3-4 (L_3, L_4, L_5, and L_6) are the same. The capacitors C_3 and C_4 provide the shunt capacitances of the three

π-shaped lowpass networks. Therefore, the capacitance of capacitors C_3 and C_4 are two times of the capacitance of capacitors C_2, C_5, C_6, and C_7.

The current mirrors as the loading networks are widely used in many analog applications, but they still suffer from some drawbacks. First of all, an active current mirror limits the swing of the output signal. Second, the active current mirror has slow frequency response. Therefore, a passive LC current mirror instead of the active current mirror is used in this work to combine the output currents. The passive LC current mirror is able to double the output current at the resonant frequency and the detail mechanism will be discussed in this section. A circuit using the LC current combiner as the loading network has good linearity than that using the active current mirror because the LC current combiner only consists of passive elements such as inductors and capacitors. The LC current combiner consists of two rectangular on-chip inductors as shown in Fig. 3-2 for the die photograph. A Darlington buffer consisting of transistor Q_{13} and Q_{14} is used to maintain the voltage gain.

The detailed operational principle of the LC current combiner with inductor loss is explained in Fig. 3-5. I_{S1} equals to I_{S2} in Fig. 3-5 for the differential excitation of the current combiner. The combination of the LC current combiner and the current source I_{S1} can be represented by its Norton equivalence I_{out} and Z_{out} in Fig. 3-5. The I_{out} and Z_{out} can be related to the ABCD matrix elements of the LC current combiner as shown in Fig. 3-5.

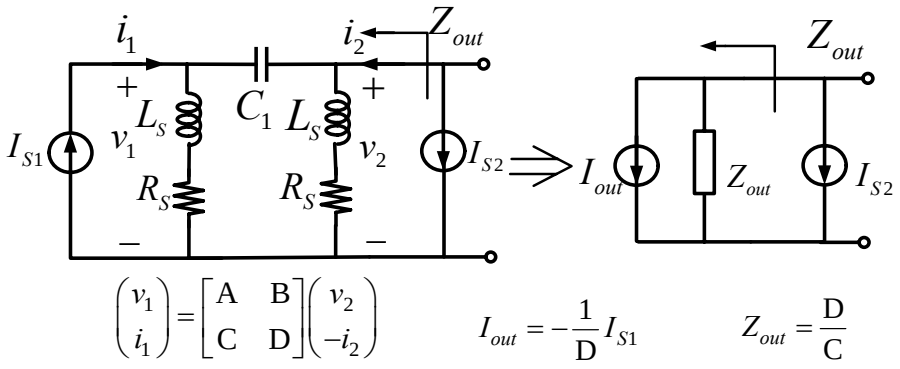


Fig. 3-5. The LC current combiner operational principle. The inductor loss is included in the analysis.

The ABCD matrix of the LC current combiner obtained by cascading the ABCD matrix of the shunt inductors and the series capacitor is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \dfrac{R_S + j\omega L_S + \dfrac{1}{j\omega C_1}}{R_S + j\omega L_S} & \dfrac{1}{j\omega C_1} \\ \dfrac{2\left(R_S + j\omega L_S\right) + \dfrac{1}{j\omega C_1}}{\left(R_S + j\omega L_S\right)^2} & \dfrac{R_S + j\omega L_S + \dfrac{1}{j\omega C_1}}{R_S + j\omega L_S} \end{bmatrix} \tag{3.4}$$

The effect of the current doubling occurs at the resonant frequency, ω_R. Here,

$$\omega_R = \sqrt{\frac{1}{2L_S C_1}} \tag{3.5}$$

Thus, I_{out} and Z_{out} at the resonant frequency can be expressed as follows.

$$I_{out} = -\frac{R_S + j\omega_R L_S}{R_S - j\omega_R L_S} I_{S1} \tag{3.6}$$

$$Z_{out} = \frac{R_S^2 + \left(\omega_R L_S\right)^2}{2R_S} = \frac{R_S\left(1 + Q_R^2\right)}{2} = \frac{R_P}{2} \tag{3.7}$$

Here, Q_R in (3.7) is the quality factor of the inductor at the resonant frequency. R_P in (3.7) can be interpreted as the parallel resistor when the series inductor model with L_S and R_S is replaced by the parallel inductor model with L_P and R_P. The output resistance is simply expressed as $R_P/2$. If the quality factor Q_R is much larger than one, I_{out} equals to I_{S1} and L_P equals to L_S. Thus, the voltage at the output node of the LC current combiner equals to $I_{S1}R_P$ for a differential excitation because of the current doubling effect.

In addition, the operational principle of the output LC current combiner can be diagrammatically analyzed and it is shown in Fig. 3-6. The Gilbert switching quad commutates the differential IF currents at the rate of LO frequency. Thus, the collectors of the Gilbert mixer core can be considered as a pair of differential current sources at the RF frequency attributed to the mixing operation. Figure 3-6(a) represents the equivalent circuit of the Gilbert mixer output with an LC current mirror

load. The output is taken at the single side but the current is doubled due to the combing ability of the LC current mirror. The parasitic series resistance of the on-chip inductor is also included in Fig. 3-6(a) in order to analyze the conversion gain.

First, we change the Norton representation shown in Fig. 3-6(a) into the Thevenin equivalent circuit shown in Fig. 3-6(b). The capacitance $1/2C_S$ in Fig. 3-6(a) can be treated as two C_S capacitors in series. The inductor L_S, parasitic series resistor R_S, and the capacitor C_S are now in series; therefore, the total series impedance equals to R_S at the resonant frequency as shown in Fig. 3-6(c). Thus, the resistance R_S is then in series with the remaining capacitor C_S. The resonant frequency is shown in Fig. 3-6(b) and can be defined as:

$$\omega_R = \sqrt{\frac{1}{L_S C_S}} \tag{3.8}$$

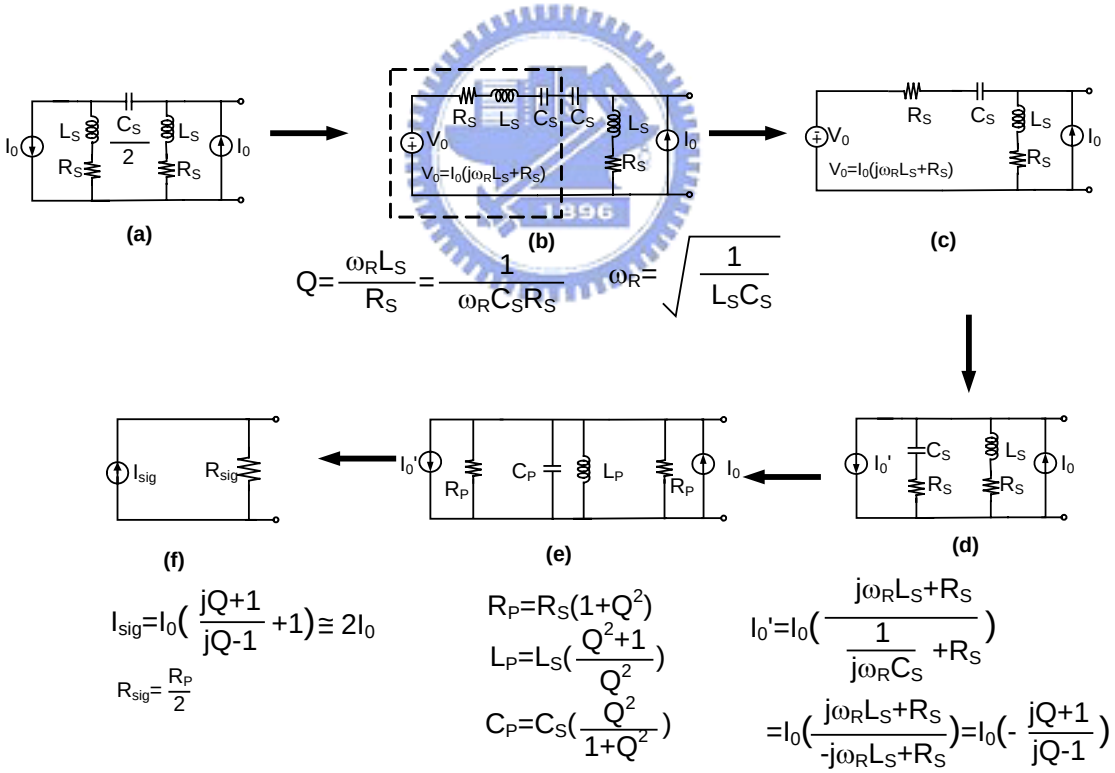


Fig. 3-6. The operational principle of the LC current mirror when the inductor has ohmic loss.

The quality factor Q of the series R-L-C network in Fig. 3-6(b) equals to:

$$Q = \frac{\omega_R L_S}{R_S} = \frac{1}{\omega_R C_S R_S} \tag{3.9}$$

Next, the circuit shown in Fig. 3-6(c) can be changed to its Norton equivalence as shown in Fig. 3-6(d) and the equivalent current source can be expressed as follows.

$$I_0' = I_0\left(\frac{j\omega_R L_S + R_S}{\frac{1}{j\omega_R C_S} + R_S}\right) = I_0\left(\frac{j\omega_R L_S + R_S}{-j\omega_R L_S + R_S}\right)$$
$$= I_0\left(-\frac{jQ+1}{jQ-1}\right) \cong -I_0 \quad if\ Q >> 1 \tag{3.10}$$

Thus, the direction of the current flow is reversed if the quality factor is larger than one. The series R-C and series R-L shown in Fig. 3-6(d) can be transformed to their parallel counterparts as shown in Fig. 3-6(e). The series resistance R_S can be changed to the parallel resistance R_P by the equation below.

$$R_P = (1+Q^2)R_S \tag{3.11}$$

$$\omega_R = \sqrt{\frac{1}{L_S C_S}} = \sqrt{\frac{1}{L_P C_P}} \tag{3.12}$$

Finally, at the resonant frequency the reactance from L_P and C_P cancels out and the net impedance becomes $R_P/2$. The resulting total current I_{sig} in Fig. 3-6(f) can be expressed as:

$$I_{sig} = I_0' + I_0 \cong 2I_0 \tag{3.13}$$

From the above derivation, the output current is doubled at resonant frequency if the quality factor is high enough. Therefore, the resulting equivalent circuit of the LC current mirror at the resonant frequency can be represented a current source of $2I_0$ and a parallel resistor of $R_P/2$.

The parasitic series resistance of the on-chip inductor has to be dealt with in a careful way in order to maximize the conversion gain of an upconverter with the passive LC current mirror load. The analytic equation derived in this work is useful to maximize the voltage gain and a simple series L-R equivalent circuit model is used in the derivation. A large effective inductor can maintain the high conversion because of

the associated high R_P. The inductance should be as large as possible for larger series resistance, but the inductor still functions as an effective inductor at the operating frequency. Thus, there exists a maximum inductor at a given operating frequency. Once the maximum inductor is chosen and then the capacitance is determined by the resonant frequency.

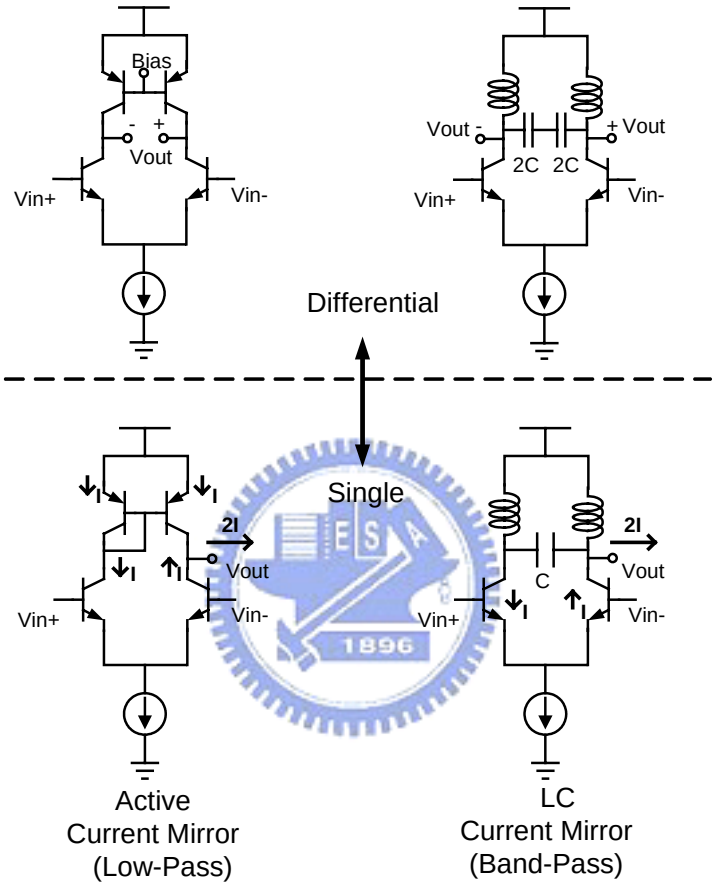


Fig. 3-7. The similar concept between the active current mirror and the LC current mirror. The common mode feedback circuitry for the active differential load is neglected for simplicity.

The comparison between the active load and the LC passive load is shown in Fig. 3-7. The voltage gain is the same for a differential amplifier with the active differential load and the current mirror load because of the current doubling effect in the active current mirror load. The same scenario can be applied to the differential passive LC load and the passive LC current mirror load. It is straightforward from Fig. 3-6(f) that the differential LC load has the same voltage gain as the LC current mirror load at the resonant frequency. In other words, the passive LC current mirror is similar to the active current mirror but the frequency response of the LC current mirror is a

band-pass response. The LC current mirror is adequate in the high frequency IC design because the values of inductance and the capacitance are small and can be realized in the IC technology.

As shown in Fig. 3-1, there is an output voltage buffer to perform the output impedance matching. This section will focus on the power gain property of the output voltage buffer. It is interesting to see that the output voltage buffer in fact provides power gain. Furthermore, the power gain obtained from the voltage buffer is even better than that obtained from a pure reactive matching. The equivalent single-ended output circuitry of the LC current combiner from the previous derivation is shown in the Fig. 3-8(a). The Norton equivalent circuit can be changed to the Thevenin equivalent circuit in order to discuss the power delivered to the load in this section.

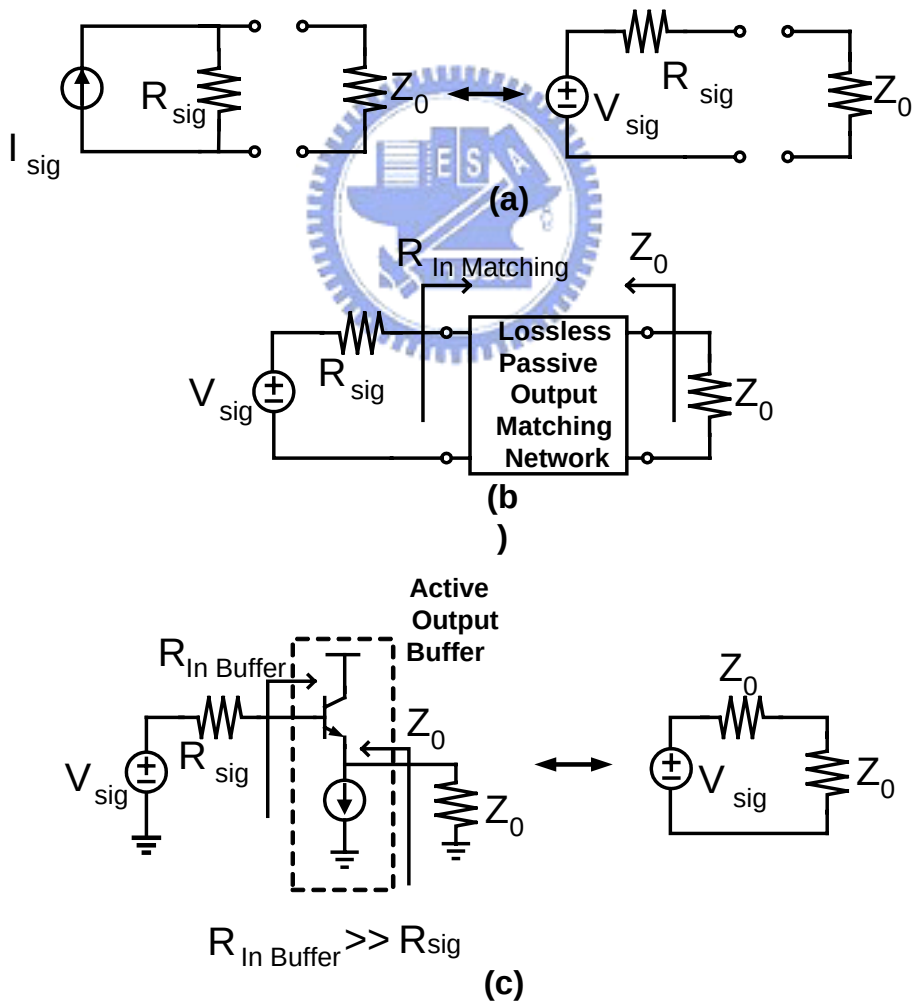


Fig. 3-8. The output power transfer of the LC current mirror and the output buffer.

As shown in Fig. 3-8(b), if a reactive matching network is employed to match the

LC current mirror output to the 50 Ω. The maximum power delivered to the load at the simultaneously conjugate condition can be determined by following equation [61]:

$$P_{L\ Passive\ Matching} = \frac{\left|I_{sig}\right|^2 R_{sig}}{4} \tag{3.14}$$

However, if an active output voltage buffer is used, the power delivered to the load can be analyzed by the condition shown in Fig. 3-8(c). The output of the voltage buffer is match to 50 ohms and the input impedance of the voltage buffer is much larger than the impedance from the LC current mirror. Thus, the power delivered to the load when the active voltage buffer is employed can be expressed as follows:

$$P_{L\ Active\ Buffer} = \frac{\left|V_{sig}\right|^2}{4Z_0} = \frac{\left|I_{sig}\right|^2 R_{sig}^2}{4Z_0} \tag{3.14}$$

Compared with the equation (3.14) and the equation (3.15), it is found that the power delivered to the load is higher using an active output buffer. Hence, the improvement can be seen from the ratio of equation (3.14) and equation (3.15):

$$\frac{P_{L\ Active\ Buffer}}{P_{L\ Passive\ Matching}} = \frac{\frac{\left|I_{sig}\right|^2 R_{sig}^2}{4Z_0}}{\frac{\left|I_{sig}\right|^2 R_{sig}}{4}} = \frac{R_{sig}}{Z_0} = \frac{R_P}{2Z_0} \tag{3.15}$$

Therefore, the improvement in power gain can be obtained using equation (3.15), the ratio of the resistance $R_P/2$ and the characteristic resistance, Z_0. In the analog circuit design, an output buffer does not provide the voltage gain; however, a common collector output buffer can provide the power gain. In fact, the power gain comes from the active output buffer and the active output buffer provides extra power through the current instead of the voltage signal. It is interesting to notice that the input resistance of the active output buffer, R_{out}, is not the conjugate value of resistor R_{sig}, The design approach is quite different from the reactive matching principle in the microwave amplifier circuit design. The design concept provided here not only agrees

with the analog design concept but also gives a clear transformation from the voltage/current gain, which is well known in the analog IC design, to the power gain, which is suitable for RFIC design. It is worthwhile to mention that the common-collector output buffer at very high frequencies behaves as an inductor. Figure 8 shows a simple common collector output buffer. In order to obtain the output impedance of the common-collector transistor Q_{14}, the output buffer can be viewed as a shunt-shunt feedback topology as shown in Fig. 3-9.

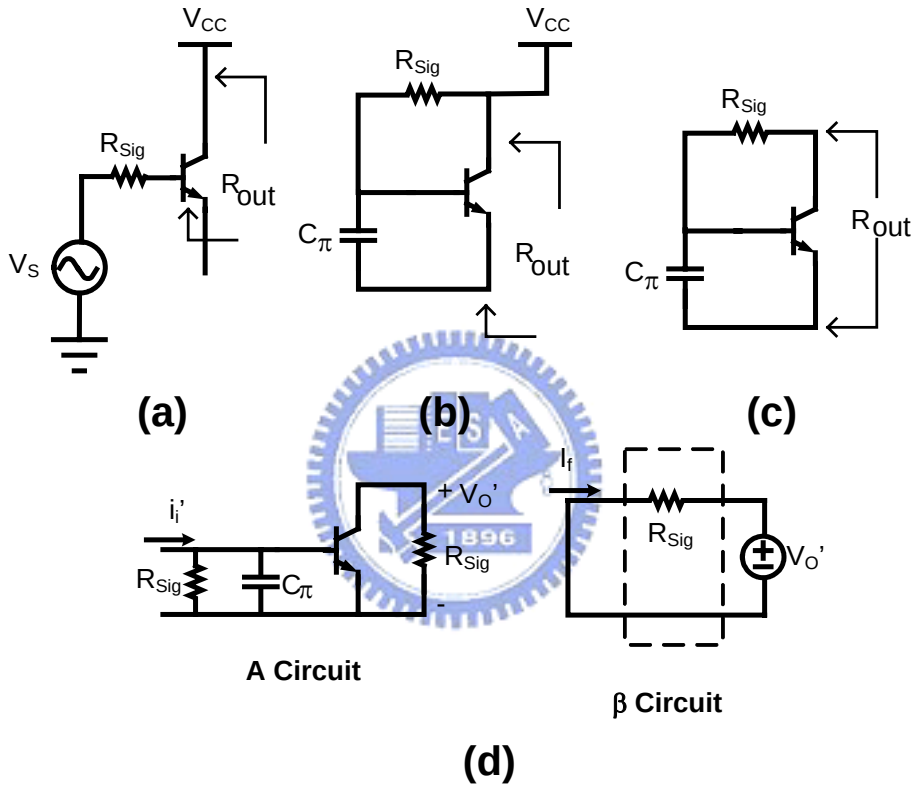


Fig. 3-9. The block diagram of the common-collector output buffer.

The original circuit topology is shown in Fig. 3-9(a), and it is equivalent to Fig. 3-9(b) for obtaining the output impedance. The output impedance in Fig. 3-8(b) is identical to the output impedance of a shunt-shunt feedback circuit shown in Fig. 3-9(c). The output impedance can then determined from the A circuit without feedback and the β feedback network shown in Fig. 3-9(d). The shunt-shunt feedback resistor is denoted as R_{Sig}, which is equivalent to the resistance R_P=2 in our work. The open-loop gain of the output buffer without feedback and the feedback factor in Fig. 3-9(d) are:

$$A(S)=\frac{V_O'}{i_i'}=\frac{-g_m R_{Sig}(R_{Sig}\parallel r_\pi)}{1+\frac{S}{\omega_P}} \tag{3.17}$$

$$\beta=-\frac{1}{R_{Sig}}$$

where

$$\omega_p=\frac{1}{C_\pi(R_{Sig}\parallel r_\pi)} \tag{3.18}$$

Therefore, the output resistance becomes:

$$R_{out}(S)=\frac{R_{Sig}}{1+\beta A(S)}=\frac{R_{Sig}}{1+\frac{g_m R_{Sig}(R_{Sig}\parallel r_\pi)}{1+\frac{S}{\omega_P}}}$$

$$=\begin{cases}\dfrac{R_{Sig}}{g_m R_{Sig}(R_{Sig}\parallel r_\pi)+1} & \textbf{when } \omega<\omega_p \\ \dfrac{R_{Sig}\,j\omega L_{out}}{R_{Sig}+j\omega L_{out}} & \textbf{when } \omega_p<\omega<\omega_T \\ R_{Sig} & \textbf{when } \omega_T<\omega \end{cases} \tag{3.19}$$

where

$$L_{out}=\frac{R_{Sig}}{\omega_T}$$

$$\omega_T=\frac{g_m}{C_\pi} \tag{3.20}$$

As shown in Fig. 3-10, the output impedance of the common collector is resistive

when the operation angular frequency is lower than ω_P. However, the output impedance becomes inductive when the angular frequency is higher than ω_P. Therefore, the common-collector output buffer will maintain a constant resistive output impedance as long as the circuit is operated lower than the angular frequency ω_P from eq. (3.19). In our case, the ω_P of the output buffer is 6.58×10^{10} rad/s, or 10.5 GHz in our work. As a result, the output buffer used here still provides a constant output impedance at 5.2 GHz.

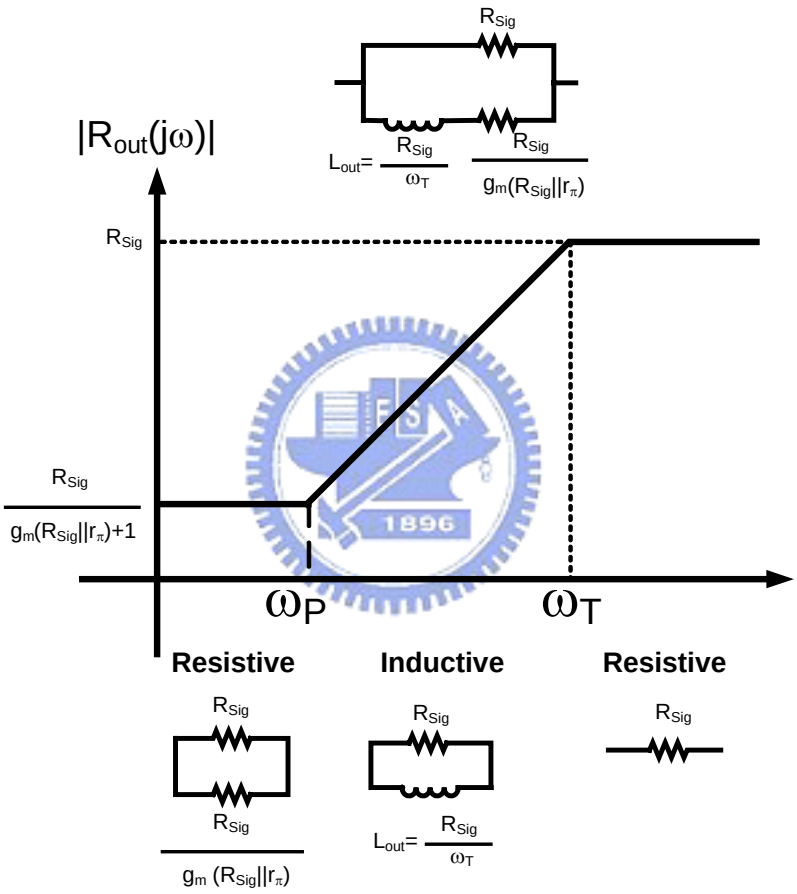


Fig. 3-10. The output impedance of the common-collector output buffer as a function of frequency.

The 5.2 GHz upconverter with the integrated RF LC current combiner and the lumped-element ratrace hybrid in the LO stage also facilitates on-wafer RF measurements. As shown in Fig. 3-2, the input GSG IF port is on the bottom side of the chip while the output GSG RF port is on the right. LO GSG signal port is on the left and the DC pads are on the top. The supply voltage of the SiGe 5.2 GHz upconverter is 3.3 V and the current consumption is 11.5 mA. The measured conversion gain as a function of LO power is shown in Fig. 3-11. As shown in Fig.

3-11, the peak conversion gain is –1dB when LO power changes from –6 to 5 dBm. In other words, the required LO power is small and there exists a wide range of LO power for optimum conversion gain because it only requires a small voltage swing for current steering in the bipolar type LO switching quad.

Figure 3-12 shows the measured return losses of both IF and RF port. The RF output return loss is better than 13.5 dB from 0.1 GHz up to 20 GHz. The input impedance matching of a this upconverter is wideband in nature and the measured IF input return loss is better than 10 dB for frequencies up to 20 GHz as shown in Fig. 3-12. The power performance of the upconverter is shown in Fig. 3-13. Experimental results show that the OP_{1dB} is –10 dBm and the OIP_3 is 6 dBm. The high linearity property of the upconversion mixer is directly attributed to the passive LC current combiner as loading elements.

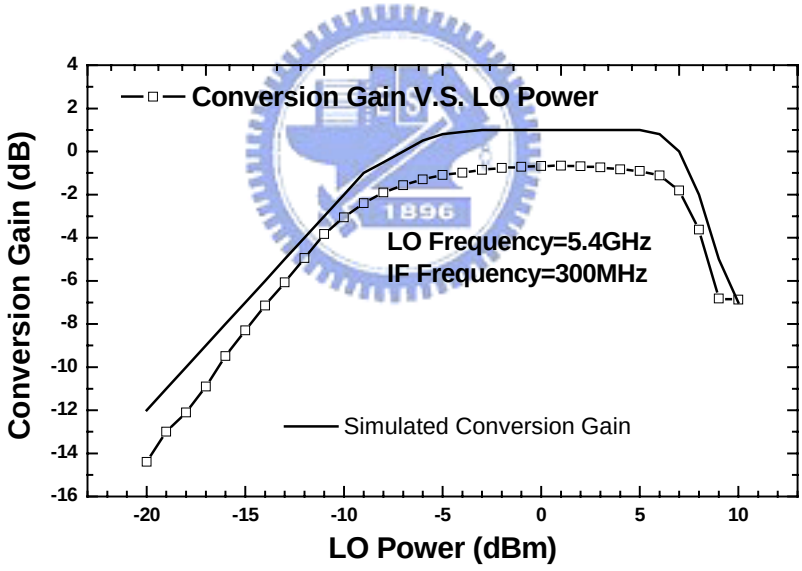


Fig. 3-11. Measured and simulated conversion gain vs. LO power of the 5.2 GHz SiGe upconverter using the output LC current mirror and the LO lumped balun.

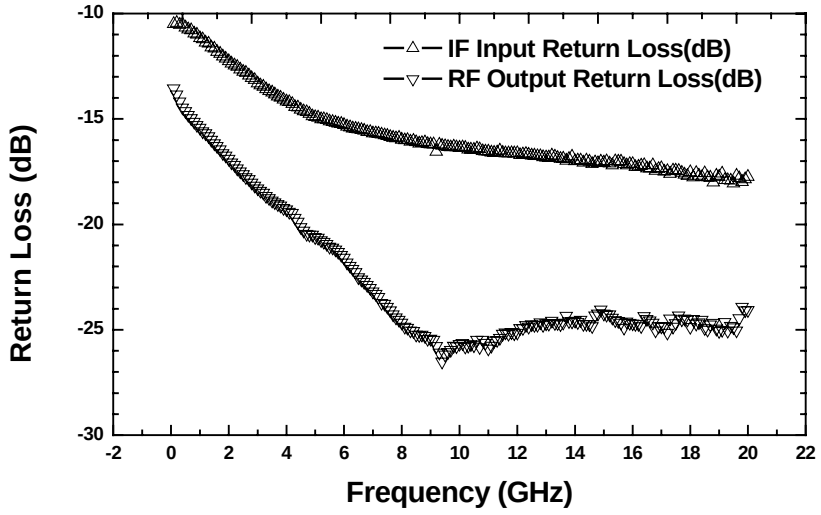


Fig. 3-12. Measured IF port input return loss and RF port output return loss of the 5.2 GHz SiGe upconverter using the output LC current mirror and the LO lumped balun.

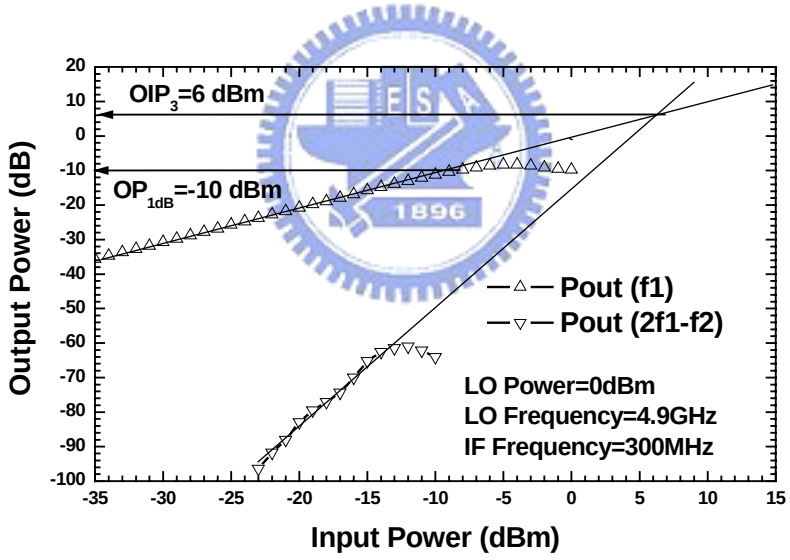


Fig. 3-13. Power performance of the 5.2 GHz SiGe upconverter using the output LC current mirror and the LO lumped balun.

Figure 3-14 shows the LO-to-IF and LO-to-RF isolations. The measurement result shows that LO-to-IF isolation is 36 dB for 4.9 GHz LO input frequency. The LO-to-RF isolation is better than -38 dB for the LO frequency from 4.86 to 4.94 GHz. The LO-to-RF isolation is -39 dB when the LO frequency is 4.9 GHz. The high isolation property results from the truly balanced operation of the upconverter demonstrated in this work.

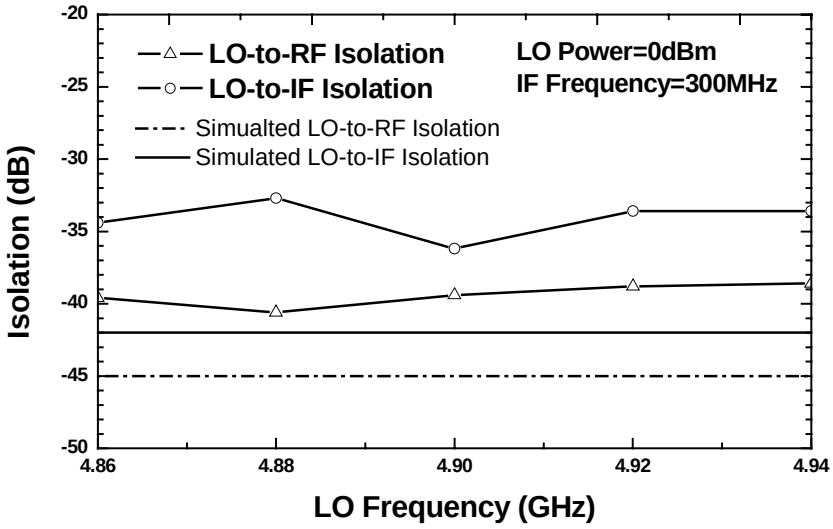


Fig. 3-14. Measured and simulated LO-to-RF and LO-to-IF isolations of the 5.2 GHz SiGe HBT upconverter.

The RF bandwidth and the IF bandwidth of the upconverter are shown in Fig. 3-15 and 3-16, respectively. The RF bandwidth can be measured when the LO frequency is fixed to 4.9 GHz and the IF frequency is swept from 10MHz to 0.9 GHz. As shown in Fig. 3-15, the output RF 3-dB bandwidth is about 0.6 GHz caused by the narrow-band frequency response of the LC current mirror.

The input IF bandwidth of the upconverter naturally should be very wide because of the wideband micormixer input stage; however, the measured IF bandwidth is limited by the bandwidth of the lumped rat-race hybrid at the LO stage. From literatures, the IF bandwidth is measured by sweeping both LO and IF frequencies but keeping the RF output frequency the same. When the LO frequency is sweeping, the generated LO signals become no longer truly balanced. Therefore, the conversion gain falls and the IF bandwidth decreases. The narrow-band lumped LO stage makes that the IF has a lowpass frequency response. Figure 3-16 shows the IF bandwidth in this work is about 1 GHz.

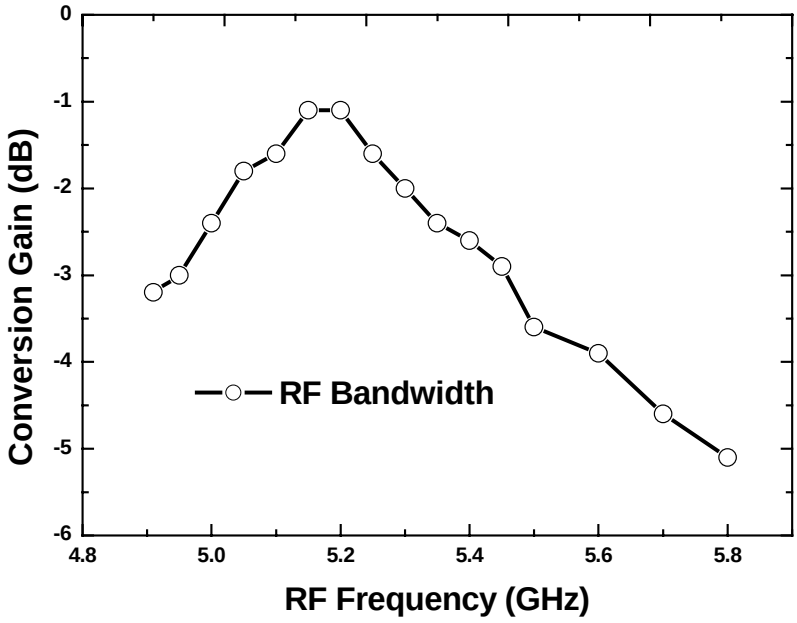


Fig. 3-15. Measured RF output bandwidth of the 5.2 GHz SiGe HBT upconverter using the output LC current mirror and the LO lumped balun.

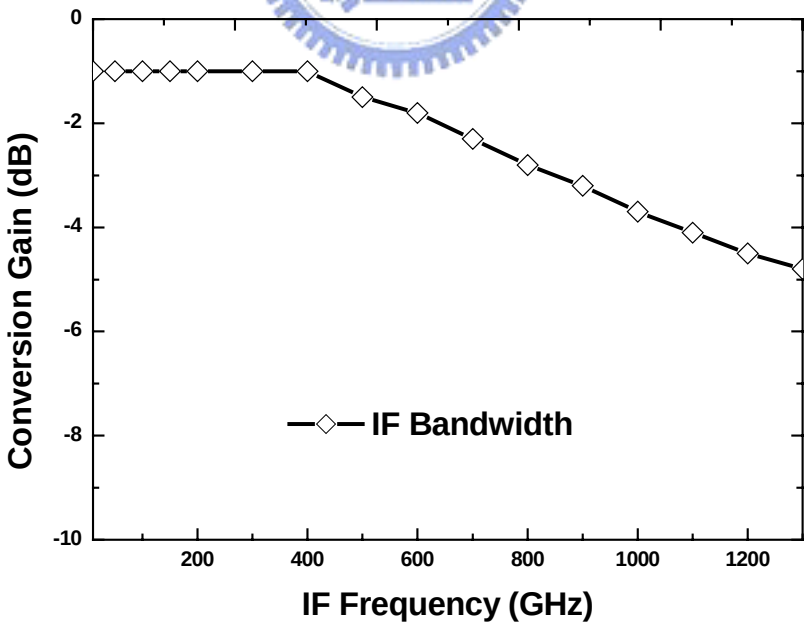


Fig. 3-16. The IF input bandwidth of the 5.2 GHz SiGe HBT upconverter using the output LC current mirror and the LO lumped balun.

3.2 GaInP/GaAs HBT Up-Conversion Mixer Using the LC Current Mirror and the Lumped Rat-Race Hybrid

A fully integrated GaInP/GaAs HBT Gilbert upconversion mixer is shown in Fig. 3-17. The upconversion mixer in Fig. 3-17 consists of a LO Gilbert mixer core (Q_5, Q_6, Q_7, and Q_8) with a lumped 180° rat-race hybrid, an active IF balun (Q_1, Q_2, Q_3, and Q_4), and an RF output LC current combiner with a Darlington common-collector output buffer (Q_9 and Q_{10}). The lumped rat-race hybrid shown in Fig. 3-17 employs the pi low-pass network and the tee high-pass network to replace the quarter-wavelength and three-quarter-wavelength sections of the distributed counterparts, respectively [5]. The lumped rat-race hybrid generates balanced LO signals for the mixer core. The LC current combiner formed by two inductors L_S and one capacitor C_1 as shown in Fig. 3-17 is located at the RF output of the Gilbert mixer core to perform the differential-to-single conversion. A Darlington common collector output follows the current combiner to facilitate impedance matching at the RF port. The common-base-configured Q_3 and common-emitter-configured Q_2 form the active IF balun by providing equal but out of phase transconductance gain when Q_1 and Q_2 are connected as a current mirror [29]. The single-to-differential transconductor replaces the conventional emitter-coupled-pair transconductor in the Gilbert upconverter and does not consume extra power.

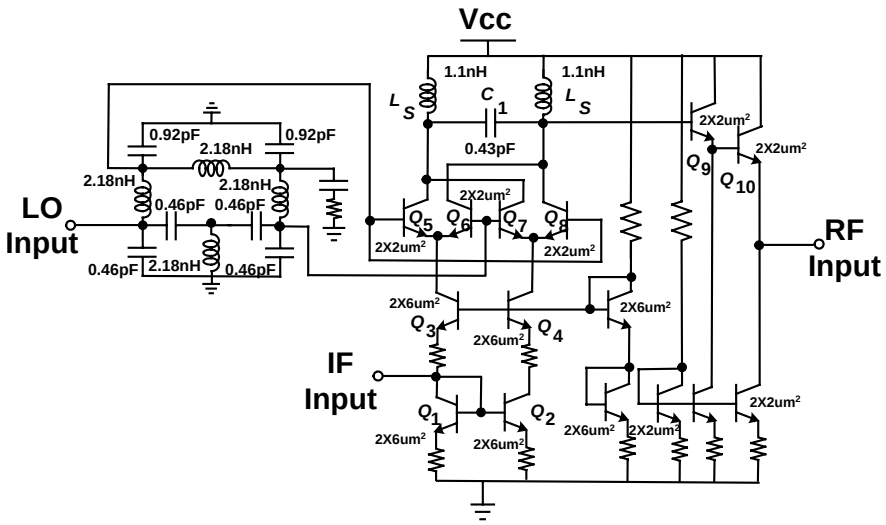


Fig. 3-17. Schematic diagram of the GaInP/GaAs HBT Gilbert upconverter with the lumped rat-race hybrid and the LC current combiner.

The RF 3-dB bandwidth and IF 3-dB bandwidth are determined by the RF LC current combiner and the LO lumped ratrace hybrid, respectively. The simulated RF 3-dB bandwidth is 280 MHz by fixing the LO frequency at 4.9 GHz and sweeping the IF frequency. The simulated IF 3-dB bandwidth is 140 MHz by fixing the RF frequency at 5.2 GHz and sweeping the IF frequency.

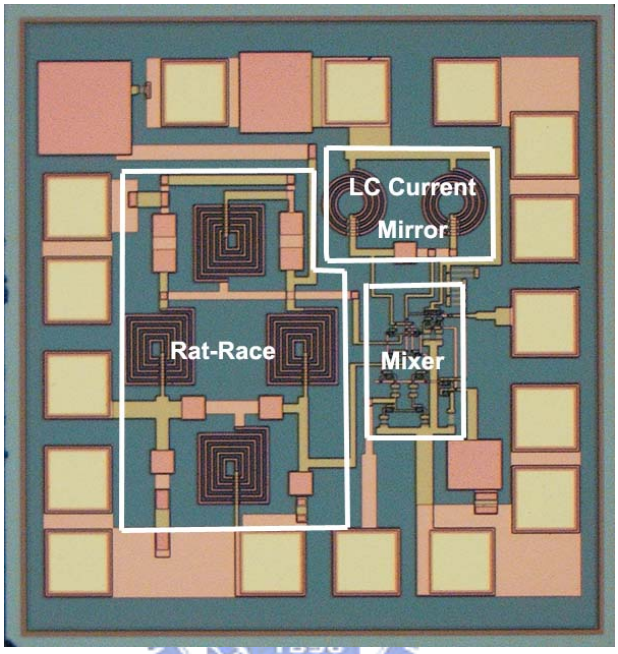


Fig. 3-18. Photograph of the GaInP/GaAs HBT Gilbert upconverter with the lumped rat-race hybrid and the LC current combiner.

The photograph of the upconverter is shown in Fig. 3-18. The die size is 1 mm^2. The 2 um GaInP/GaAs HBT technology has a peak f_T around 40 GHz. 2 x 2 μm^2 single-emitter HBT devices are used throughout most of the circuits except for the IF active balun and diode-connected current-mirror transistors that use the 2 x 6 μm^2 single-emitter HBT devices. Four 5.5-square-turn (2.18 nH) inductors are employed in the rat-race hybrid and two 3.5-circular-turn (1.1 nH) inductors are employed in the LC current combiner, respectively.

The GaInP/GaAs HBT Gilbert upconverter with single-ended IF, LO, and RF ports facilitates on-wafer rf measurements. The supply voltage is 5 V and the current consumption is 6.5 mA. The measured peak conversion gain is 1 dB when LO power is -7 dBm and LO frequency is 4.9 GHz. The measured conversion gain varies within 1 dB when LO power changes from – 12 dBm to -1 dBm. The output RF return loss is

23 dB at 5.2 GHz and the IF input return loss is better than 25 dB for frequencies up to 8 GHz. The power performance of the upconverter is shown in Fig. 3-19. The fully integrated Gilbert upconverter has conversion gain of 1 dB, OP_{1dB} of −10 dBm, and OIP_3 of 2 dBm when input IF=300 MHz, LO=4.9 GHz and output RF=5.2 GHz. The measured LO-to-RF isolation is 38 dB.

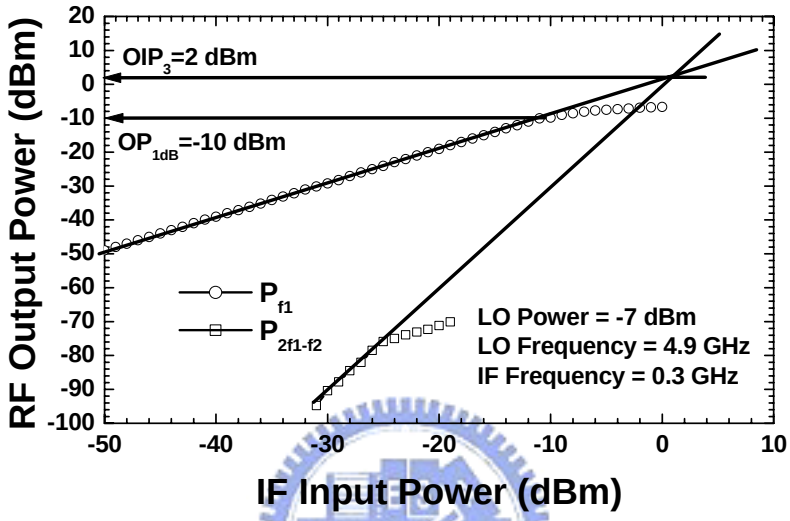


Fig. 3-19. Power Performance of the GaInP/GaAs HBT Gilbert upconverter with the lumped rat-race hybrid and the LC current combiner.

3.3 SiGe HBT Up-Conversion Mixer Using Active-Inductor LC Current Mirror

Recently, the band-pass LC current mirror has been used to increase the conversion gain by combining the output differential currents at the high frequency [62]. However, the passive inductors employed in the LC current mirror always occupy large chip area. In this work, the passive inductors in the LC current mirror are replaced by the active inductors consisting of the common-collector transistors and feedback resistors to save the die area and still preserve the upconverter performance.

The active inductors have been widely used in the LC tank circuits, monolithic filters, and matching networks [63], [64]. Compared with the passive counter parts, the silicon active inductors have major advantages over spiral inductors in terms of

the area, the inductance tuning capability, and higher quality factor, at the expense of the linearity, higher current consumption, and noise performance degradation. In the upconverter application, the noise performance is insignificant and the power amplifier basically dominates the linearity of the whole transmitter chain. The active inductors are incorporated in a current-reused topology in this work. Consequently, the active inductor is adoptive in our upconversion mixer design.

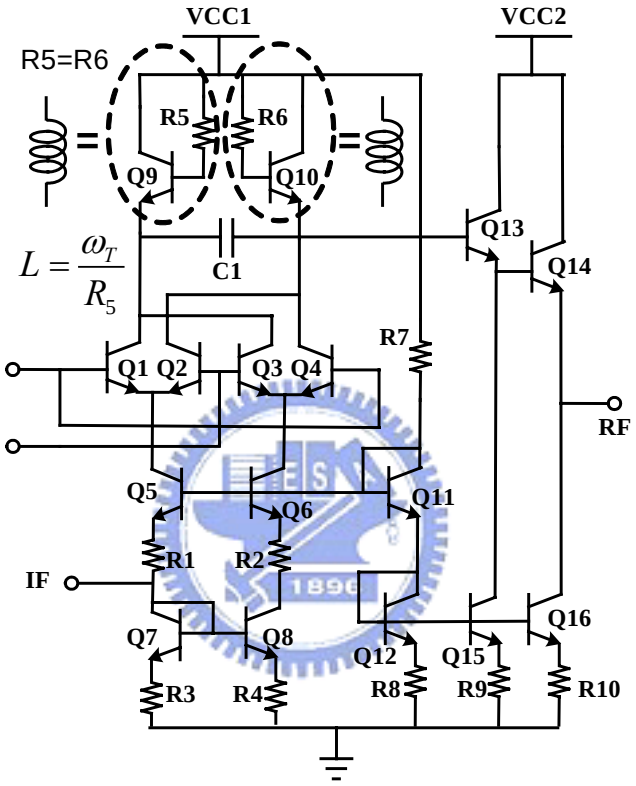


Fig. 3-20. The schematic of the upconversion micromixer using the active-inductor LC current mirror.

The circuit schematic of the 5.2 GHz SiGe upconverter is shown in Fig. 3-20. The demonstrated upconversion Gilbert mixer consists of a micromixer input (transistors Q_5-Q_8, and resistors R_1-R_4), a LO current-commutation cell (transistors Q_1-Q_4), an LC current mirror (transistors Q_9-Q_{10}, resistors R_5-R_6, and the capacitor C_1), and a Darlington output buffer. The input stage of the upconverter is the single-to-differential micromixer topology [29]. The chip area can be saved because no inductors and capacitors are used at the input port for the impedance matching.

The common-collector transistor Q_9 (Q_{10}), and the resistor R_5 (R_6) are designed together to function as an inductor when looking into the emitter terminal. The LC

current mirror is able to double the output current at the resonant frequency $f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{2LC_1}}$, which is the designated output RF frequency. The active inductor is valid for the frequency ranging from $f_p = \frac{1}{2\pi(R_5 // r_{\pi 9})C_{\pi 9}}$ to the transistor cut-off frequency, f_T. The $C_{\pi 9}$, $r_{\pi 9}$, R_5, and f_{T9} are 0.3 pF, 700 Ω, 300 Ω, and 25 GHz; therefore, the output impedance of the common-collector transistor keeps inductive from 1.8 GHz to 25 GHz in this work.

The 0.35 um SiGe HBT device has BV_{CEO} of 2.5V, and the maximum f_T of 67 GHz when the current density is 3 mA/um^2 at V_{CE}=1V. The photograph of the fabricated circuit is shown in Fig. 3-21, and the total chip area is 0.89 x 0.83 mm^2. Obviously, the pads for the on-wafer measurement dominate the chip area, and the mixer only occupies a small chip area of 200 um x 200 um as shown in Fig. 3-21.

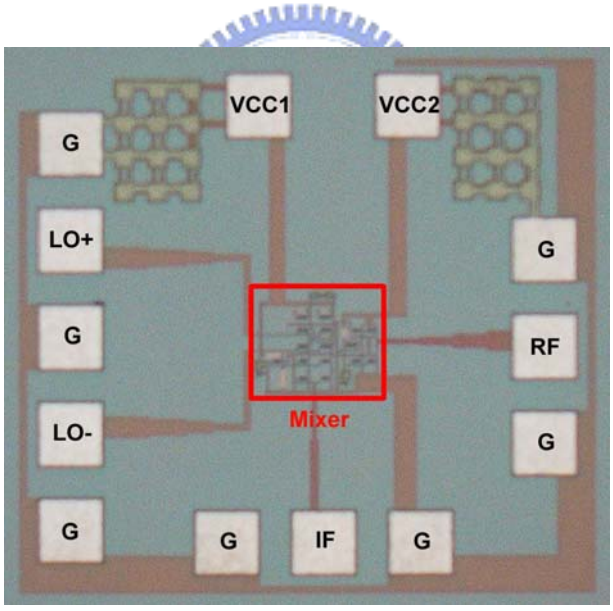


Fig. 3-21. The photograph of the upconversion micromixer using the active-inductor LC current mirror.

The supply voltage is 3.3 V, and the current consumption is 9 mA. The peak conversion gain of the demonstrated upconverter is –3.5 dB when the LO power reaches -1 dBm. As shown in Fig. 3-22, the OP_{1dB} is –10 dBm and the OIP_3 is 0 dBm.

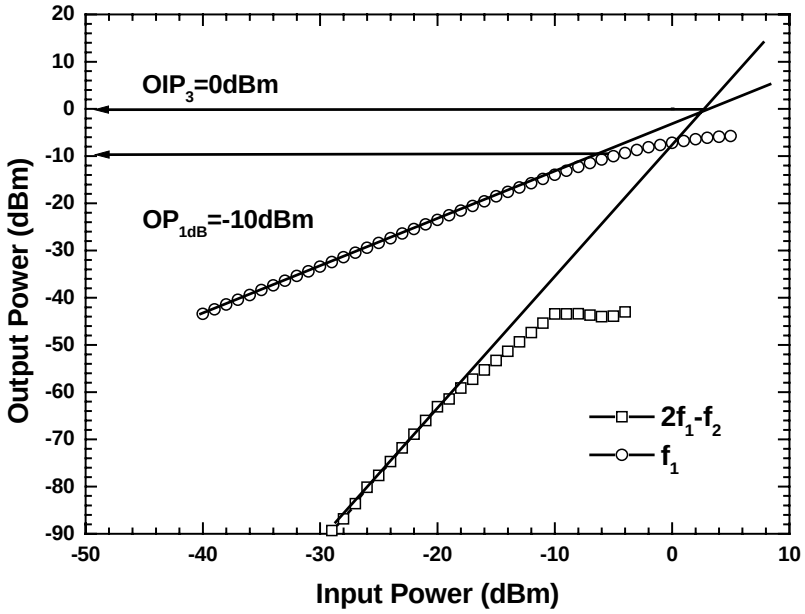


Fig. 3-22. Power performances of the upconversion micromixer using the active-inductor LC current mirror.

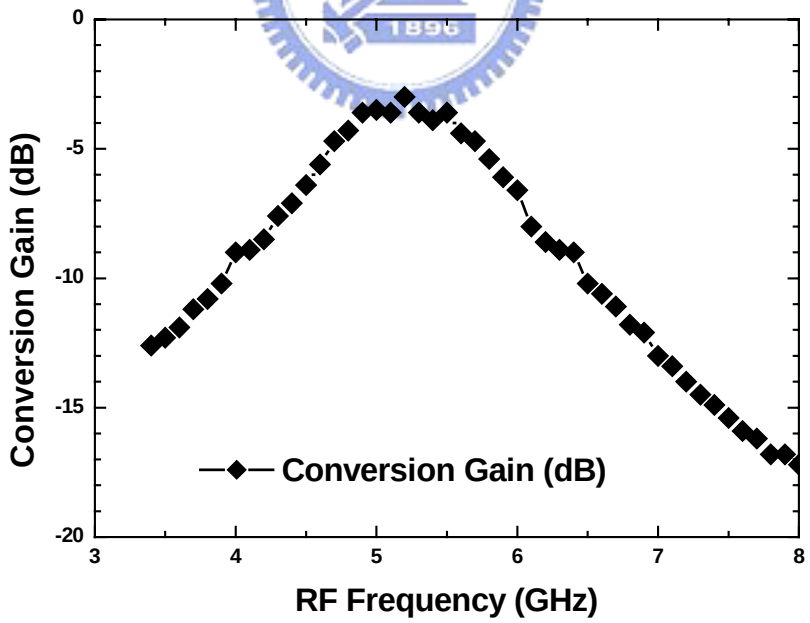


Fig. 3-23. The conversion gain as a function of the RF frequency of the upconversion micromixer using the active-inductor LC current mirror.

Despite of using the active inductors, the measured power performance is

acceptable. The micromixer input stage is wideband and the measured IF input return loss is better than 10 dB for the frequencies up to 20 GHz. The measured output return loss is better than 30 dB from 3 to 7 GHz. The LO-to-RF isolation of the mixer is 35 dB when the LO input frequency is 4.9 GHz, while the LO-to-IF isolation is 34 dB.

The conversion gain versus the RF frequency shown in Fig. 3-23 has a band-pass frequency response with the peak at 5.2 GHz. The experimental result of the conversion gain as a function of the RF frequency manifests the effectiveness of the band-pass active-inductor LC current mirror.

In conclusion, the performances of the demonstrated up-conversion mixers are summarized in Table 3-1. The GaInP/GaAs HBT up-converter has better performance of smaller power consumption. However, the active area of the SiGe up-converter using the active inductors is very compact.

Table 3-1: The Measured Performances of the Demonstrated Up-Conversion Mixers

	GaAs Up-Converter Using Passive Inductor	SiGe Up-Converter Using Passive Inductor	SiGe Up-Coverter Using Active Inductor
RF frequency (GHz)	5.2	5.2	5.2
Gain (dB)	1	-1	-3
LO-to-RF Isolation (dB)	38	38	35
LO-to-IF Isolation (dB)	36	36	34
OP1dB (dBm)	-10	-10	-10
OIP3 (dBm)	2	6	0
DC Current (mA)	6.5	11.5	9
Supply Voltage (V)	5	3.3	3.3
Die Size (mm^2)	1	1	1

Chapter 4

Conventional Image Rejection Architectures

In Chapter 2, the direct-conversion mixers are discussed. The other important mixer architecture is the image rejection system. The rejection of the image signal is a necessary requirement for the RF receiver design. There already exist several useful architectures to suppress image signals. For instance, one of these architectures is the heterodyne system, and the system uses the off-chip SAW image rejection filter to filter out the image signal. There is an obvious drawback that the integration level of the heterodyne system is reduced due to the off-chip SAW filter. In this chapter, two conventional image rejection architectures including the Hartley and the Weaver systems are demonstrated using the advanced HBT technologies.

The Hartley low-IF architecture uses quadrature signals and the multi-section polyphase filters to filter out the image signals [6], [16], [17], [65]-[69]. The low-IF structure can effectively suppress the unwanted image signal; however, many sections of polyphase filters have to be cascaded in the low-IF system to extend the image rejection bandwidth. Both multi-section passive or active polyphase filters consume large chip areas. A 5.2 GHz GaInP/GaAs HBT low-IF Hartley down-converter [66] has been demonstrated and the four-section passive polyphase filter was incorporated to filter out the image signal in the low-IF down-converter. The fabricated chip shows that the IF polyphase filters occupy many valuable IC estates.

A suitable solution to deal with the image signal is the Weaver architecture [7], [70]-[72]. The Weaver down-converter demonstrated in this work is implemented using GaInP/GaAs HBT technology; therefore, the demonstrated Weaver down-converter has some advantages such as the semi-insulating substrate, and accurate thin-film resistors.

Section 4.1 introduces a Hartley image rejection system implemented by 0.35 um SiGe HBT technology. The other image rejection architecture --- Weaver system is reported in Section 4.2. The SiGe HBT Hartley down-converter exhibits 47 dB image rejection ratio while the GaAs HBT Weaver down-converter provides 48 dB image rejection ratio.

4.1 Hartley Image Rejection Architecture

In the past decade, the low-IF (Low Intermediate Frequency) double quadrature configuration with integrated polyphase filters for image signal suppression has been used in CMOS technology [6], [16], [17], [65]. The off–chip image rejection filter is replaced by integrated polyphase filters in a low-IF receiver topology. When a large image rejection ratio (IRR) is required in a low-IF topology, a double quadrature (DQ) downconversion sysytem is better than a single quadrature (SQ) downconversion system because the DQ downconversion architecture requires less quadrature accuracy in LO and RF. The signal imbalance only influences the IRR to the second order in a DQ system while the imperfection signals influences the IRR to the first order in the SQ system. If the phase error of the signal is 3%, the image rejection ratio of the DQ system is only influenced by 0.09%, which is the product of 3% by 3% [6]. Therefore, it can resist more circuit imperfections.

The LO and RF quadrature signal can be generated by the polyphase filter in a DQ downconverter [6], [66]. An HBT (Heterojunction Bipolar Transistor) has better device matching property than a MOS device. Thus, it is desirable to have a high image rejection double quadrature Gilbert downconverter with polyphase filters in the SiGe HBT technology. This is the first SiGe HBT image rejection double quadrature Gilbert downconverter with passive polyphase filters above 5 GHz to the best of our knowledge. The low-IF downconverter demonstrated in this work can be suitable for WLAN application [67].

Figure 4-1 illustrates the functional diagram of a double quadrature downconverter with polyphase filters. The frequency of the input RF signal is defined as $\omega_{LO} + \omega_{IF}$ and the frequency of the image signal is defined as $\omega_{LO} - \omega_{IF}$. Differential RF and differential LO signals are fed externally and two polyphase filters are employed to generate the RF and LO differential quadrature signals. The RF (LO) differential quadrature signals are denoted as RF_{I+} (LO_{I+}), RF_{Q+}, (LO_{Q+}), RF_{I-} (LO_{I-}) and RF_{Q-} (LO_{Q-}) as shown in Fig. 4-1. The RF and image differential quadratrue signals are summarized in table 4-1 for convenience.

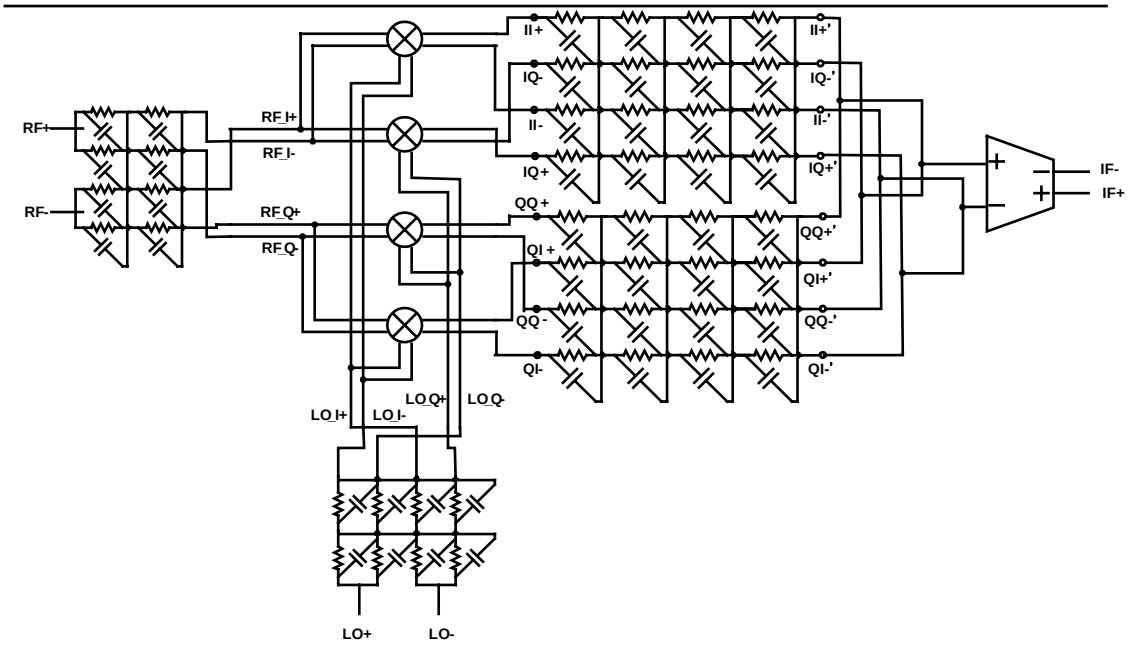


Fig. 4-1. Block diagram of a double quadrature downconversion mixer with polyphase filters.

Table 4-1: The quadrature signals of the RF, the image, the error RF and the error image signals generated by the quadrature generator

	RF Signal (RF_{ID})	Image Signal ($Image_{ID}$)	Error RF Signal (RF_{ER})	Error Image Signal ($Image_{ER}$)
I+	$\cos(\omega_{LO}+\omega_{IF})t$	$\cos(\omega_{LO}-\omega_{IF})t$	$E_{r1}\cos(\omega_{LO}+\omega_{IF})t$	$E_{r1}\cos(\omega_{LO}-\omega_{IF})t$
Q+	$\sin(\omega_{LO}+\omega_{IF})t$	$\sin(\omega_{LO}-\omega_{IF})t$	$-E_{r1}\sin(\omega_{LO}+\omega_{IF})t$	$-E_{r1}\sin(\omega_{LO}-\omega_{IF})t$
I-	$-\cos(\omega_{LO}+\omega_{IF})t$	$-\cos(\omega_{LO}-\omega_{IF})t$	$-E_{r1}\cos(\omega_{LO}+\omega_{IF})t$	$-E_{r1}\cos(\omega_{LO}-\omega_{IF})t$
Q-	$-\sin(\omega_{LO}+\omega_{IF})t$	$-\sin(\omega_{LO}-\omega_{IF})t$	$E_{r1}\sin(\omega_{LO}+\omega_{IF})t$	$E_{r1}\sin(\omega_{LO}+\omega_{IF})t$

Four multipliers are employed to mix the RF signals and the image signals with LO signals as shown in Fig. 4-1. There are totally 8 output IF signals resulting from the four multipliers. The 8 downconverted IF signals can be grouped in two groups of differential quadrature signals as summarized in table 4-2.

The first differential quadrature IF signals consist of II+, IQ-, II-, and IQ+ and the other differential quadrature IF signals consist of QQ+, QI+, QQ-, and QI- downconverted signals. Here, the first letter represents the constituent RF (IM) signal and the second letter represents the constituent LO signal for the composite IF signal. In either group, the differential quadrature IF signals are in the counter-clockwise sequence for the RF_{ID} x LO_{ID} mixing and in the clockwise sequence for the IM_{ID} x LO_{ID} mixing [6] as shown in the table 4-2. The same ployphase filter connects to each

group signal as shown in Fig. 4-1.

Table 4-2: The downconverted IF signals of the desired and image signals with LO signals (neglecting the high frequency components).

	RF_{ID} X LO_{ID}	$Image_{ID}$ X LO_{ID}
II+	$0.5\cos\omega_{IF}t$	$0.5\cos\omega_{IF}t$
IQ-	$0.5\sin\omega_{IF}t$	$-0.5\sin\omega_{IF}t$
II-	$-0.5\cos\omega_{IF}t$	$-0.5\cos\omega_{IF}t$
IQ+	$-0.5\sin\omega_{IF}t$	$0.5\sin\omega_{IF}t$
QQ+	$0.5\cos\omega_{IF}t$	$0.5\cos\omega_{IF}t$
QI+	$0.5\sin\omega_{IF}t$	$-0.5\sin\omega_{IF}t$
QQ-	$-0.5\cos\omega_{IF}t$	$-0.5\cos\omega_{IF}t$
QI-	$-0.5\sin\omega_{IF}t$	$0.5\sin\omega_{IF}t$

It is important that the sequences of the generated IF differential quadrature signals are different for the RF and IM signals because the IF polyphase filter can pass one sequence and block the other sequence as explained in reference [6]. Thus, the RF signal can be downconverted to the IF terminals and the image signal is blocked when the (II+, IQ-, II-, and IQ+) and (QQ+, QI+, QQ-, and QI-) IF differential quadrature signals are connected to the polyphase filters as shown in Fig. 4-1. On the other hand, if the polyphase filters are fed with (II+, IQ+, II-, and IQ-) and (QQ+, QI-, QQ-, and QI+) IF differential quadrature signals, the RF signal will be blocked while the image signal can pass. At the output of the polyphase filters, the in-phase (anti-in-phase) and quadrature-phase (anti-quadrature-phase) terminals are connected together to form the differential IF signals as shown in Fig. 4-1.

Imperfect RF and LO signals can be decomposed into an ideal sequence with an opposite error sequence as explained in reference [6]. The imperfections in RF and LO signals can be caused by feeding the unbalanced signals to the mixer and the mismatches in the mixer itself. The image rejection ratio degrades when the non-ideal effects occur. If the perfect RF signal is represented by the counter-clockwise sequence shown in table 4-1, the error RF signal (RF_{ER}) caused by the mismatches can be represented by the clockwise error sequence in table 4-1. The term, Er_1, in table 4-1 is the magnitude of the RF error signal normalized by the magnitude of the

RF ideal signal. Similarly, the imperfect LO signal (LO_{ER}) can also be decomposed into the ideal sequence and the opposite error sequence. The term, Er_2, here represents the magnitude of the LO error signal normalized by the magnitude of the LO ideal signal. There are totally 8 downconverted outputs for the double quadrature downconverter as shown in Fig. 4-1.

As shown in Fig. 4-1, the RF and the error RF signals are multiplied with the LO and the error LO signals by four mixers. The resulting signals at node IQ- can be described as follows:

$$\begin{aligned} &-[\cos(\omega_{LO}+\omega_{IF})t + Er_1\cos(\omega_{LO}+\omega_{IF})t]\times(\sin\omega_{LO}t - Er_2\sin\omega_{LO}t) \\ &= \frac{1}{2}[-\sin(2\omega_{LO}+\omega_{IF})t + \sin\omega_{IF}t - Er_1\sin(2\omega_{LO}+\omega_{IF})t + Er_1\sin\omega_{IF}t \\ &+Er_2\sin(2\omega_{LO}+\omega_{IF}) - Er_2\sin\omega_{IF}t + ErEr_2\sin(2\omega_{LO}+\omega_{IF}) - Er_1Er_2\sin\omega_{IF}t] \end{aligned} \quad (4.1)$$

The mixer and the output buffer amplifier have the low-pass frequency response and thus the high frequency mixing components can be neglected. For convenience, the total mixed signals at the port II+, IQ-, II-, IQ+, QQ+, QI+, QQ-, and QI- as shown in Fig. 4-2 are listed in table 4-3.

As shown in table 4-3, the multiplied signals of RF_{ID} x LO_{ER} and RF_{ER} x LO_{ER} are in the clockwise sequence; therefore, they can not pass the polyphase filter. The remained signals include the multiplied products of RF_{ID} x LO_{ID} and RF_{ER} x LO_{ID}. The sequence of the output signals of the polyphase filter is the same as the sequence of the input signals. In other words, II+', IQ-', II-', IQ+' (QQ+, QI+, QQ-, and QI-) has the same sequence as II+, IQ-, II-, IQ+ (QQ+', QI+', QQ-', and QI-'). Although the RF_{ER} x LO_{ID} signals can pass the polyphase filter, connecting the nodes II+' with QQ+' and IQ-' with QI+' together as shown in Fig. 4-2, the RF_{ER} x LO_{ID} signals can be canceled. As a result, only the product of the RF and the LO signals exists at the output ports of the polyphase filter.

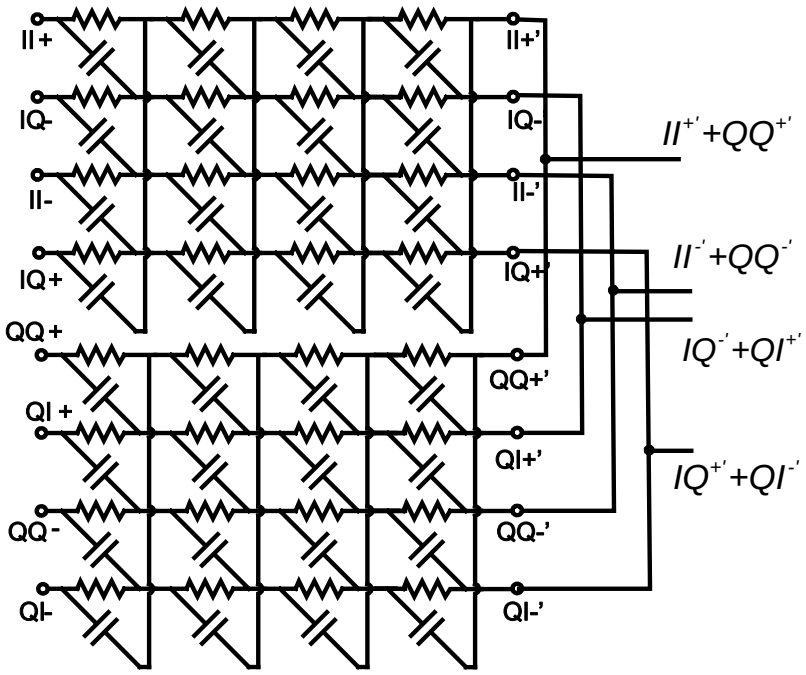


Fig. 4-2. The illustration of the nodes connection at the output ports to cancel the $RF_{ER}xLO_{ID}$ signals.

Similarly, the mixing results of the image and the LO signals when considering the imperfect quadrature signals are also summarized in table 4-3. According to table 4-3, the $Image_{ID}$ x LO_{ID}, $Image_{ER}$ x LO_{ID}, and $Image_{ID}$ x LO_{ER} signals can be filtered out by the polyphase filter or canceled by the proper connections as described above. However, The signals caused by the $Image_{ER}$ x LO_{ER} signals directly pass through the polyphase filter and thus the image rejection degrades. The advantage of the double quadrature system can be easily observed from the discussions above because the magnitude of the IF error signal is the product of Er_1 and Er_2, and thus it is a second order effect. The double quadrature system can increase the image rejection ratio when the imperfect quadrature signals are considered.

Consequently, the detail circuit topology and signals connections of a typical polyphase filter are shown in Fig. 4-1. A two-stage polyphase filter is used to generate both LO and RF differential quadrature signals from their differential counterparts. A conventional Gilbert cell with a differential common collector output buffer is used as the multiplier. The circuit schematic of the Gilbert mixer is shown in Fig. 4-3.

Table 4-3: The downconverted IF signals considering the imperfect quadrature signals (neglecting the high frequency components).

	RF_{ID} X LO_{ID} (Counter Clockwise)	RF_{ER} X LO_{ID} (Counter Clockwise)	RF_{ID} X LO_{ER} (Clockwise)	RF_{ER} X LO_{ER} (Clockwise)
II+	$0.5\cos\omega_{IF}t$	$Er_1 0.5\cos\omega_{IF}t$	$Er_2 0.5\cos\omega_{IF}t$	$Er_1Er_2 0.5\cos\omega_{IF}t$
IQ-	$0.5\sin\omega_{IF}t$	$Er_1 0.5\sin\omega_{IF}t$	$-Er_2 0.5\sin\omega_{IF}t$	$-Er_1Er_2 0.5\sin\omega_{IF}t$
II-	$-0.5\cos\omega_{IF}t$	$-Er_1 0.5\cos\omega_{IF}t$	$-Er_2 0.5\cos\omega_{IF}t$	$-Er_1Er_2 0.5\cos\omega_{IF}t$
IQ+	$-0.5\sin\omega_{IF}t$	$-Er_1 0.5\sin\omega_{IF}t$	$Er_2 0.5\sin\omega_{IF}t$	$Er_1Er_2 0.5\sin\omega_{IF}t$
QQ+	$0.5\cos\omega_{IF}t$	$-Er_1 0.5\cos\omega_{IF}t$	$-Er_2 0.5\cos\omega_{IF}t$	$Er_1Er_2 0.5\cos\omega_{IF}t$
QI+	$0.5\sin\omega_{IF}t$	$-Er_1 0.5\sin\omega_{IF}t$	$Er_2 0.5\sin\omega_{IF}t$	$-Er_1Er_2 0.5\sin\omega_{IF}t$
QQ-	$-0.5\cos\omega_{IF}t$	$Er_1 0.5\cos\omega_{IF}t$	$Er_2 0.5\cos\omega_{IF}t$	$-Er_1Er_2 0.5\cos\omega_{IF}t$
QI-	$-0.5\sin\omega_{IF}t$	$Er_1 0.5\sin\omega_{IF}t$	$-Er_2 0.5\sin\omega_{IF}t$	$Er_1Er_2 0.5\sin\omega_{IF}t$
	$Image_{ID}$ X LO_{ID} (Clockwise)	$Image_{ER}$ X LO_{ID} (Clockwise)	$Image_{ID}$ X LO_{ER} (Counter Clockwise)	$Image_{ER}$ X LO_{ER} (Counter Clockwise)
II+	$0.5\cos\omega_{IF}t$	$Er_1 0.5\cos\omega_{IF}t$	$Er_2 0.5\cos\omega_{IF}t$	$Er_1Er_2 0.5\cos\omega_{IF}t$
IQ-	$-0.5\sin\omega_{IF}t$	$-Er_1 0.5\sin\omega_{IF}t$	$Er_2 0.5\sin\omega_{IF}t$	$Er_1Er_2 0.5\sin\omega_{IF}t$
II-	$-0.5\cos\omega_{IF}t$	$-Er_1 0.5\cos\omega_{IF}t$	$-Er_2 0.5\cos\omega_{IF}t$	$-Er_1Er_2 0.5\cos\omega_{IF}t$
IQ+	$0.5\sin\omega_{IF}t$	$Er_1 0.5\sin\omega_{IF}t$	$-Er_2 0.5\sin\omega_{IF}t$	$-Er_1Er_2 0.5\sin\omega_{IF}t$
QQ+	$0.5\cos\omega_{IF}t$	$-Er_1 0.5\cos\omega_{IF}t$	$-Er_2 0.5\cos\omega_{IF}t$	$Er_1Er_2 0.5\cos\omega_{IF}t$
QI+	$-0.5\sin\omega_{IF}t$	$Er_1 0.5\sin\omega_{IF}t$	$-Er_2 0.5\sin\omega_{IF}t$	$Er_1Er_2 0.5\sin\omega_{IF}t$
QQ-	$-0.5\cos\omega_{IF}t$	$Er_1 0.5\cos\omega_{IF}t$	$Er_2 0.5\cos\omega_{IF}t$	$-Er_1Er_2 0.5\cos\omega_{IF}t$
QI-	$0.5\sin\omega_{IF}t$	$-Er_1 0.5\sin\omega_{IF}t$	$Er_2 0.5\sin\omega_{IF}t$	$-Er_1Er_2 0.5\sin\omega_{IF}t$

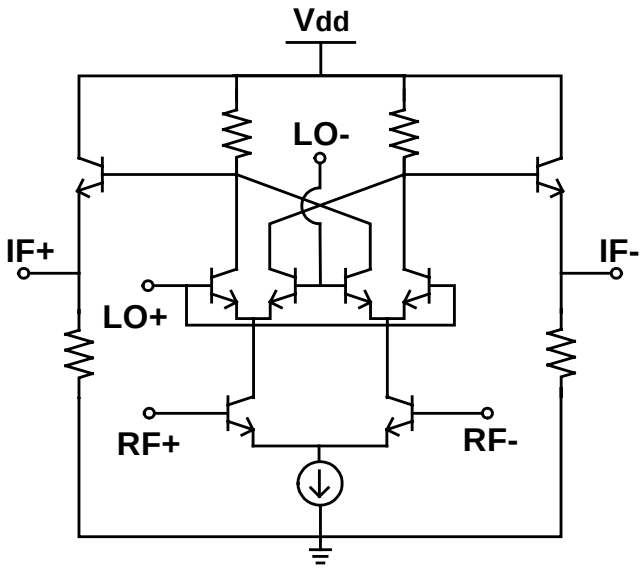


Fig. 4-3. The schematic of the Gilbert mixer used in this work.

The image rejection is performed by using two four-stage RC-CR polyphase filters. The bandwidth and the image rejection ratio are dominated by the number of the cascading polyphase filters [6]. If the large bandwidth and high image rejection ratio are desired, there must be more sections of polyphase filters in cascaded; however, the performances of the gain and the noise figure will be degraded. In this work, the IF polyphase filter degrades the gain about 7 dB and the RF input quadrature generator degrades the gain about 2 dB in the simulation. The differential quadrature IF signals are combined into differential signals by shorting the differential quadrature IF signals and a differential buffer amplifier is also included in the IF final stage as illustrated in Fig. 4-1.

One goal of this work is to accomplish an image rejection downconverter that can operate under the 2.7 V DC power supply to be powered by the battery. This low DC power requirement limits the DC voltage headroom of the Gilbert mixer. Because the RF input polyphase filter has considerable losses, the mixers are designed to provide conversion gain to compensate the losses. The gain performance can be easily further improved by inserting several IF amplifiers into the polyphase filter chain [6]. This prototype downconverter does not include this arrangement for the simplicity, but an IF amplifier is used at the end of the polyphase filters to provide some gain to compensate the loss of the IF polyphase filters. The schematic of the output buffer is shown in Fig. 4-4.

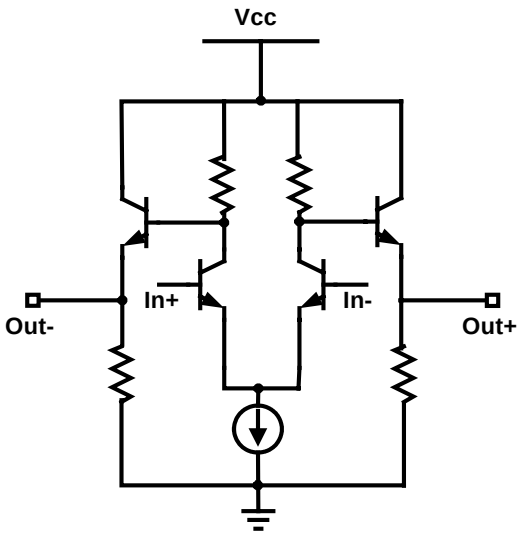


Fig. 4-4. The schematic of the output buffer used in this work.

The die photograph of a SiGe HBT double quadrature downconverter mixer with polyphase filters is shown in Fig. 4-5. The die size is 1 x 1 mm^2. All transistors used in the SiGe downconverter are the same. The SiGe HBT device used in this work has BV_{CEO}=3.8 V and peak f_t around 49 GHz. The emitter area is 0.3um x 9.9 um. The supply voltage is 2.7 V and current consumption is 10 mA.

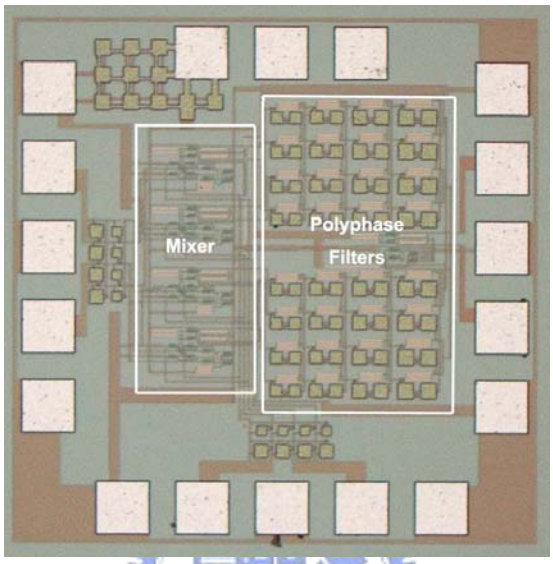


Fig. 4-5. Photograph of a SiGe HBT double quadrature downconverter with polyphase filters

On-wafer RF measurements can be performed because the fabricated circuit in Fig. 4-5 has a balanced GSGSG RF input on the left side of the chip, a GSGSG IF output on the right side and a balanced GSGSG LO input on the bottom side. Two rat-race couplers are used to convert the single-ended signals to differential signals. One rat-race coupler for RF signals is centered at 5.2 GHz and the other rat-race coupler for LO signals is centered at 5.17 GHz. The phase imbalance is less than 1^o and the magnitude imbalance of the rat-race coupler is less than 0.03 dB in 0.1 GHz bandwidth. Bias tees are inserted between the retrace and the signal generator to provide dc bias for transistors at RF and LO ports.

The conversion gain is 1 dB for 0 dBm LO pumping power when LO=5.17 GHz and RF=5.2 GHz. The conversion gain varies within 1 dB while LO power changes from 0 dBm to 10 dBm as shown in Fig. 4-6. In other words, the required LO power is small and there exists a wide range of LO power for optimum conversion gain. A Gilbert mixer core implemented with bipolar type technology needs a small local

oscillator power and has a wide range of LO power for optimum conversion gain.

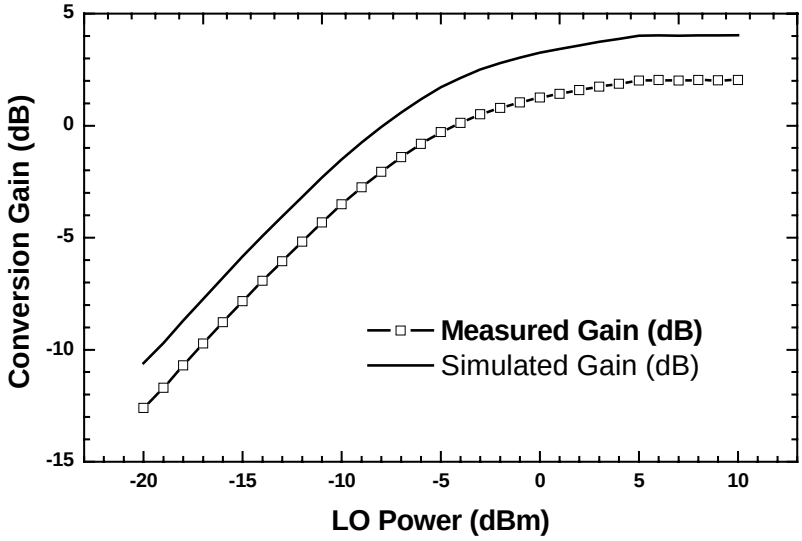


Fig. 4-6. Measured and simulated conversion gain as a function of the LO power of the SiGe HBT double quadrature downconverter with polyphase filters.

When LO power equals to 0 dBm, the LO-to-IF isolation measurement results are illustrated in Fig. 4-7. 48 dB LO-to-IF isolations are achieved in the downconverter when LO frequency is around 5.2 GHz. The circuit has more than 49 dB RF-to-IF isolation as shown in the Fig. 4-8 when the LO frequency is at 5.17 GHz and the power equals to 0 dBm. There is no IF balun used to measure LO-to-IF and RF-to-IF isolations and thus the data is directly taken from a single output port instead of combing differential outputs.

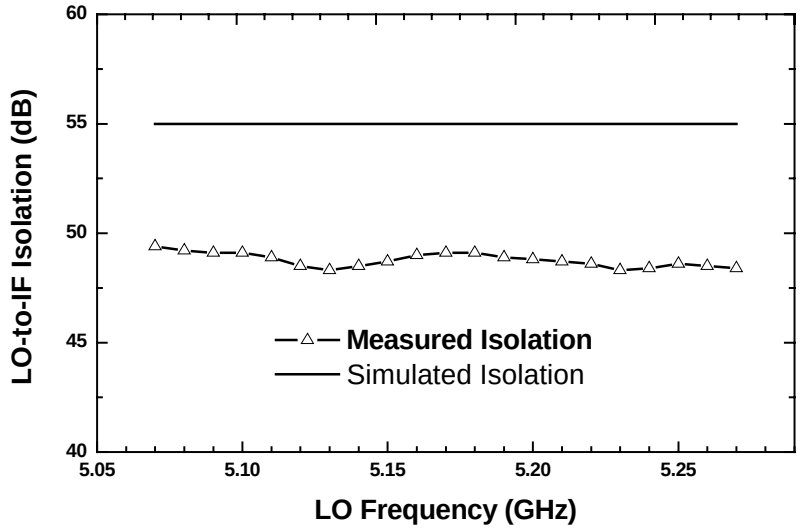


Fig. 4-7. Measured and simulated LO-to-IF isolation of the SiGe HBT double quadrature downconverter with polyphase filters.

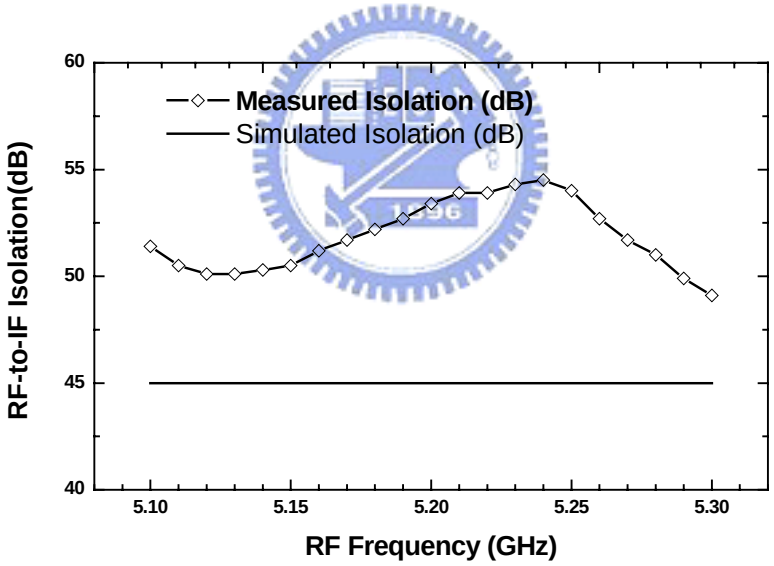


Fig. 4-8. Measured and simulated RF-to-IF isolation of the SiGe HBT double quadrature downconverter with polyphase filters.

The one-tone and two-tone power performance is shown in Fig. 4-9 and Fig. 4-10, respectively. The fabricated SiGe HBT double quadrature Gilbert downconversion mixer with polyphase filters has 1 dB conversion gain, IP_{1dB}= -19 dBm and IIP_3= -9 dBm. All the power measurements are performed when RF=5.2 GHz and LO=5.17 GHz at 0 dBm.

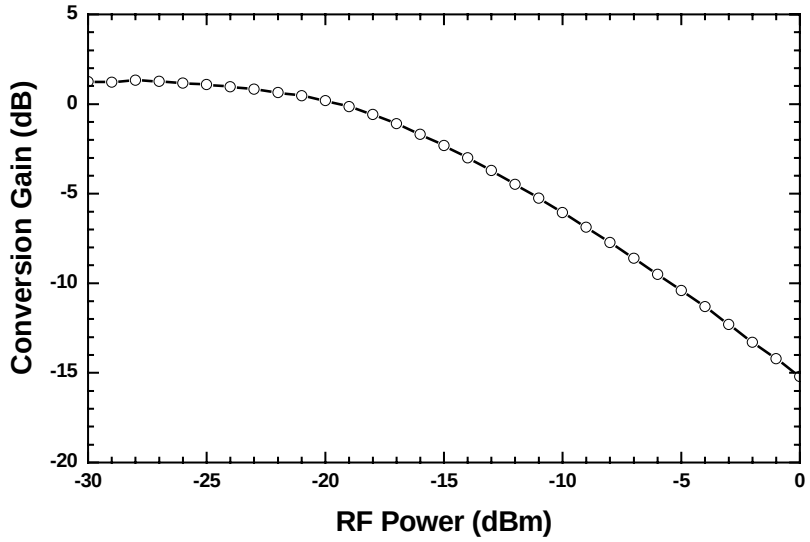


Fig. 4-9. One tone power measurements of the SiGe HBT double quadrature downconverter with polyphase filters.

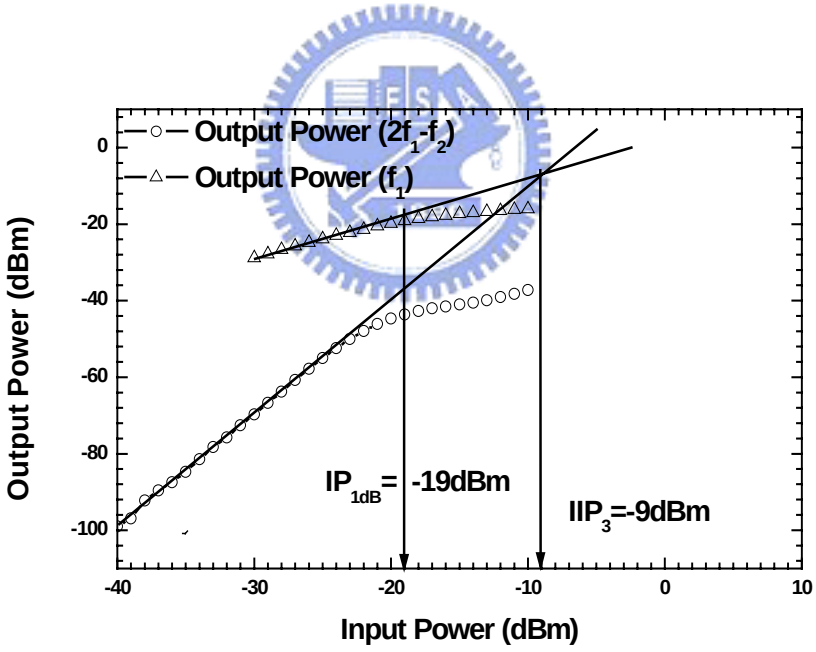


Fig. 4-10. One tone and two tone power measurements of the SiGe HBT double quadrature downconverter with polyphase filters.

Figure 4-11 illustrates the conversion gain as a function of positive IF frequency and negative IF frequency when LO=5.17 GHz and 0 dBm. The IF frequency is positive if the RF frequency is larger than the LO frequency; otherwise, the IF frequency is negative. The axis of the negative IF frequency is folded back to

highlight the comparison with positive frequency in Fig. 4-11.

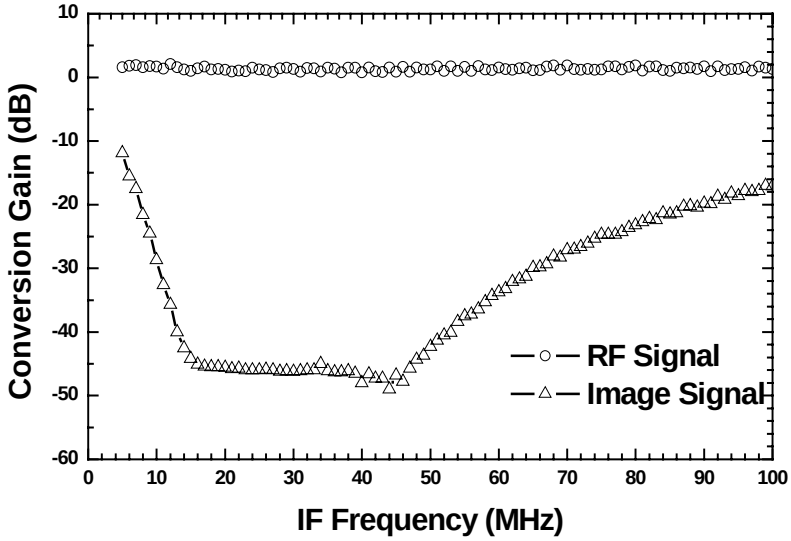


Fig. 4-11. Conversion gain as a function of IF frequency for the SiGe HBT double quadrature downconverter with polyphase filters.

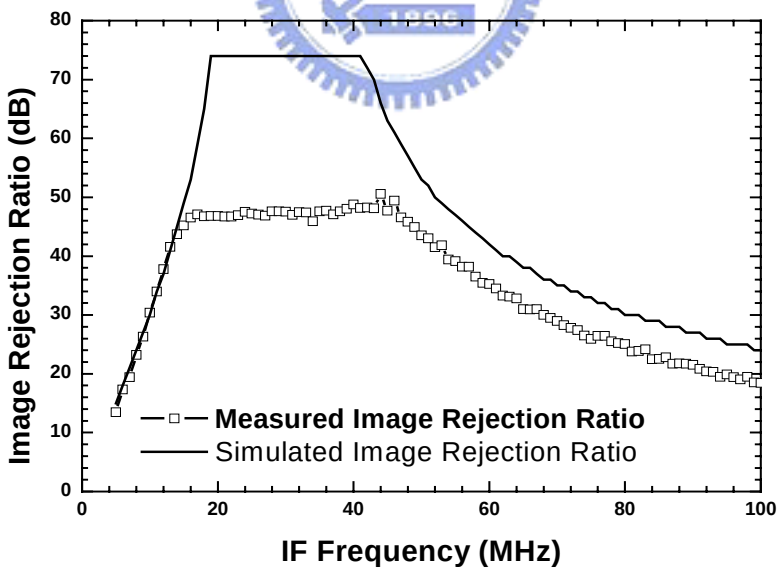


Fig. 4-12. Measured and simulated image rejection ratios of the SiGe HBT double quadrature downconverter with polyphase filters.

The conversion gain is about 1 dB for 15 to 45 MHz positive IF frequency and is -46 dB for 15 to 45 MHz negative IF frequency. The image rejection ratio defined

as the ratio between positive IF conversion gain and negative IF conversion gain is plotted in Fig. 4-12. Image rejection ratios are better than 47 dB for 15 to 45 MHz IF frequencies. The RF measurement setup is pre-calibrated for the phase imbalances, and the spectrum analyzer directly measures the image rejection ratio. Several samples are used to obtain the image rejection performance, and the experimental results show that the performance of the image rejection ratio is quite uniform.

Figure 4-13 shows the RF input return loss, the IF output return loss, and the LO return loss. The input return loss is –12 dB when the RF frequency is 5.2 GHz. The output return loss is around –26 dB when IF frequency is below 100 MHz. The LO port return loss is about –9 dB when the LO frequency is 5.17 GHz.

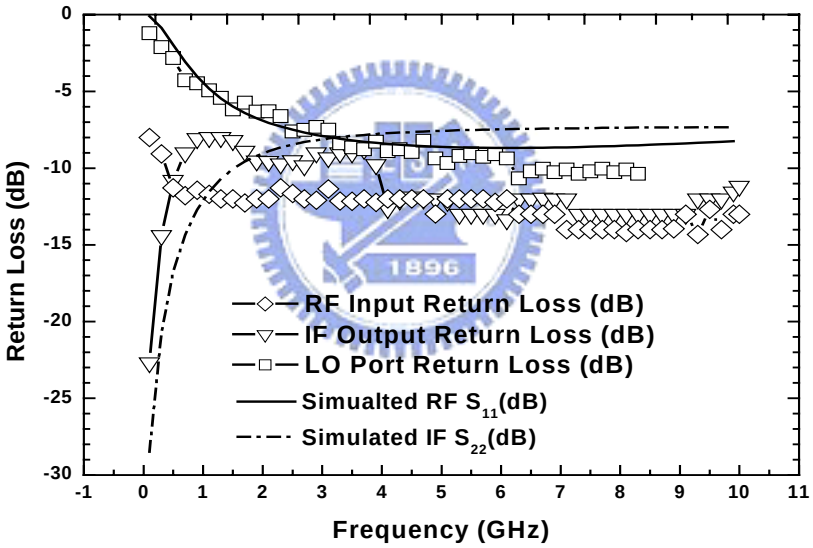


Fig. 4-13. Measured and simulated RF, IF, and LO return losses of the SiGe HBT double quadrature downconverter with polyphase filters.

Table 4-4 summarizes state-of-the-art silicon image rejection mixers using polyphase filters. The section number of the polyphase filter dominates the image rejection ratio and the filter bandwidth. Compared with other results, only the mixer with five-section polyphase filters has larger IRR than our work. It is worthwhile to mention that the die size of this work is smallest, and this work has best IRR at 5 GHz.

Table 4-4: The Comparison of Silicon Image Rejection Mixers

	This Work	Ref. [6]	Ref. [68]	Ref. [69]
Technology	0.35 um SiGe HBT	0.6 um CMOS	0.13 um CMOS	0.25 um SiGe HBT
RF (GHz)	5.2	0.27	2	5-6
IRR (dB)	47	60	47	32
Sections of PPF	4	5	5	2
Gain (dB)	1	N/A	12	25-30 *
IIP3 (dBm)	-9	N/A	-7	-12
IF center frequency (MHz)	30	10	2.84	40
IF Bandwidth (MHz)	30	10	5.68	20
Die Size (mm^2)	1	N/A	4.1	2.3 **
Power dissipation (mW)	27	N/A	24.3	14.9

* Including the gain of LNA

** Including the chip area occupied by LNA

A fully integrated SiGe double quadrature Gilbert downconversion mixer with passive polyphase filters has been demonstrated for the first time in this work to the best of our knowledge. A high image rejection double quadrature Gilbert downconverter with polyphase filters in the SiGe HBT technology has been achieved. The image rejection ratio is better than 47 dB when LO=5.17 GHz and IF is in the range of 15 MHz to 45 MHz.

4.2 Weaver Image Rejection Architecture

The other suitable solution to deal with the image signal is the Weaver architecture [7], [70]-[72]. The Weaver down-converter demonstrated in this work is implemented using GaInP/GaAs HBT technology; therefore, the demonstrated Weaver down-converter has some advantages such as the semi-insulating substrate, and accurate thin-film resistors. The substrate-coupling problem is notorious in the silicon substrate and this drawback may degrade the performance of RFICs. However, the GaInP/GaAs HBT semi-insulating substrate eliminates such a problem and thus good RF performance can be achieved. To the best of our knowledge, the Weaver down-converter with GaInP/GaAs HBT technology is demonstrated for the first time. The integration level of this GaInP/GaAs IC in this work is quite high and the IC contains 166 GaInP/GaAs HBTs.

Although many useful analyses based on trigonometric functions have been employed to explain the image rejection mechanism of the Weaver architecture [70]-[73], a diagrammatic explanation is developed in this work by using the complex signal mixing technique [74], [75]. A typical block diagram of the Weaver down-converter is shown in Fig. 4-14(a).

As shown in Fig. 4-14(a) and Fig. 4-14(b), the angular frequencies of the desired RF signal, the unwanted image signal, the LO_1 signal, and the LO_2 signal are denoted as ω_{RF}, ω_{IM}, ω_{LO1}, and ω_{LO2}, respectively. Both LO_1 and LO_2 signals are quadrature signals and the LO_1 frequency is designed to be four times of the LO_2 frequency in our work. In addition, the angular frequencies of the output signals that are mixed down by the first stage mixers are set to be ω_{IF1}, and the angular frequencies of the output signals that are mixed down by the second stage mixers are denoted as ω_{IF2}. Therefore, the relations among them can be expressed as:

$$\begin{aligned} &\omega_{IF2} = \omega_{IF1} - \omega_{LO2} = \omega_{RF} - \omega_{LO1} - \omega_{LO2} \\ &and \qquad \omega_{RF} - \omega_{LO1} = \omega_{LO1} - \omega_{IM} = \omega_{IF1} \end{aligned} \tag{4.2}$$

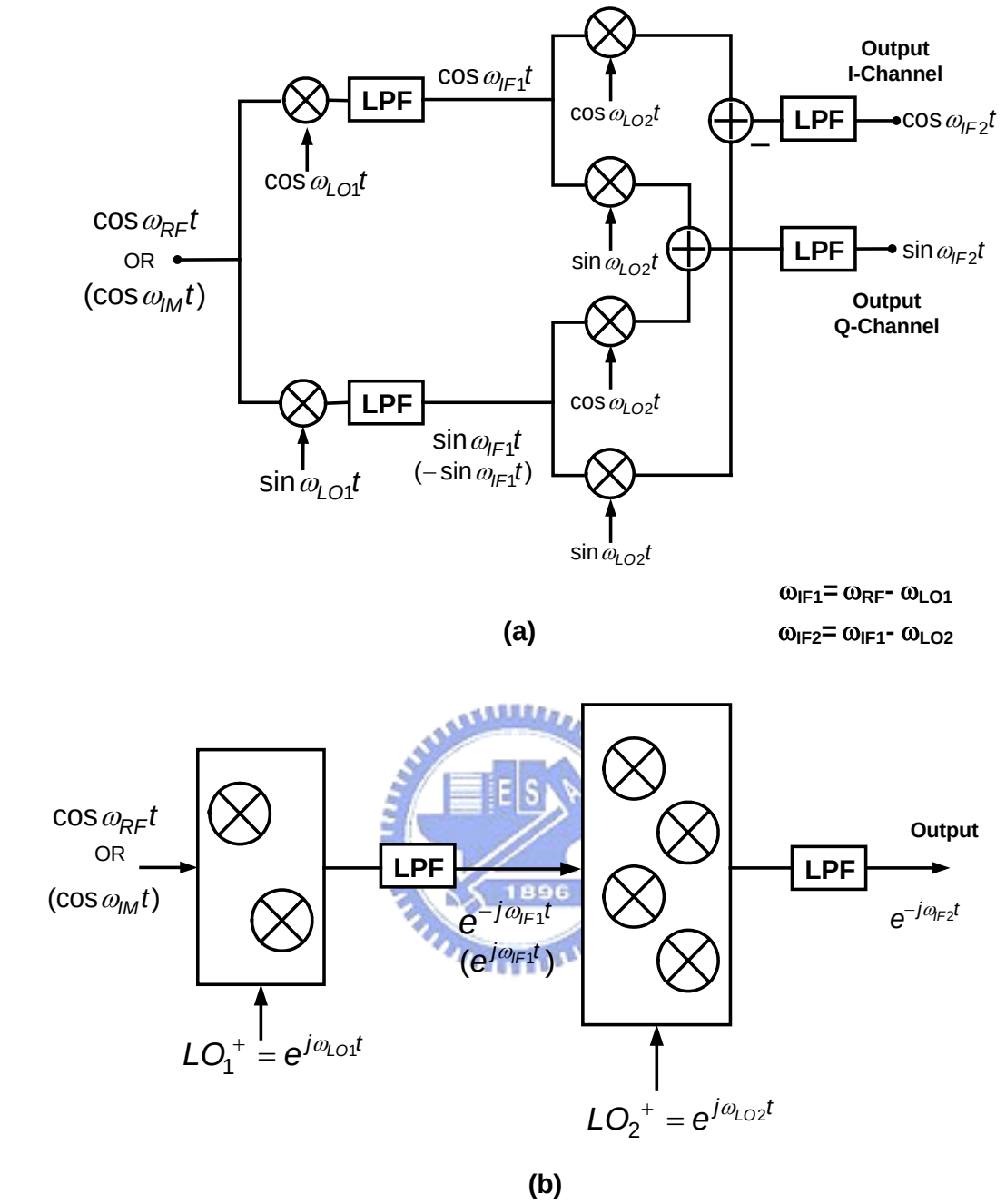


Fig. 4-14. (a) The block diagram of the Weaver down-converter; and (b) the representation of the Weaver architecture using complex signal mixing approach.

These two mixers at the first stage as shown in Fig. 4-14(a) actually form a complex mixer [74], [75]. The notation LO_1 is changed to LO_1^+ for the following derivations, and the frequency relationship described in equation (4.2) is still valid. As shown in Fig. 4-14(b), the equivalent complex mixer LO_1^+ provides a mixing function of $\exp(j\omega_{LO1}t)$. When the complex LO_1^+ mixes, the spectrum of the RF signal is shifted upwards by a value of ω_{LO1} as represented in Fig. 4-15(a) and Fig. 4-15(b).

Furthermore, when the second complex mixer LO_2^+ ($\exp(j\omega_{LO2}t)$) mixes down the signal again, the resulting signal becomes:

$$\cos\omega_{RF}t \times LO_1^+ \times LO_2^+ = \frac{e^{-j\omega_{RF}t} + e^{j\omega_{RF}t}}{2} \times e^{j\omega_{LO1}t} \times e^{j\omega_{LO2}t}$$
$$= \frac{e^{-j\omega_{IF1}t} + e^{j(2\omega_{LO1}+\omega_{IF1})t}}{2} \times e^{j\omega_{LO2}t} = \frac{e^{-j\omega_{IF2}t} + e^{j(2\omega_{LO1}+\omega_{LO2}+\omega_{IF1})t}}{2} \quad (4.3)$$

On the other hand, when the first complex LO_1^+ and the second complex LO_2^+ mix down the unwanted image signal, the output signal can be described as:

$$\cos\omega_{IM}t \times LO_1^+ \times LO_2^+ = \frac{e^{-j\omega_{IM}t} + e^{j\omega_{IM}t}}{2} \times e^{j\omega_{LO1}t} \times e^{j\omega_{LO2}t}$$
$$= \frac{e^{j\omega_{IF1}t} + e^{j(2\omega_{LO1}-\omega_{IF1})t}}{2} \times e^{j\omega_{LO2}t} = \frac{e^{j(2\omega_{IF1}-\omega_{IF2})t} + e^{j(2\omega_{LO1}+\omega_{LO2}-\omega_{IF1})t}}{2} \quad (4.4)$$

The output low-frequency signals of the RF signal and the image signal after mixing down by the two complex mixers are shown in Fig. 4-15(c). As shown in Fig. 4-15(c), the image signal is shifted to the positive frequency while the RF signal is down-converted to the negative frequency in the spectrum. The down-converted RF signal locates at the negative frequency $-\omega_{IF2}$ while the down-converted unwanted signal locates at the positive frequency $2\omega_{IF1}$-ω_{IF2}. The down-converted the image signal is located at the opposite end of the spectrum when compared with the RF signal as shown in Fig. 4-15(c), and thus the image signal can be easily filtered out either by an IF low-pass filter or by the frequency response of the IF circuits. The diagrammatic explanation of the Weaver architecture gives the designer an instinct to design the Weaver system.

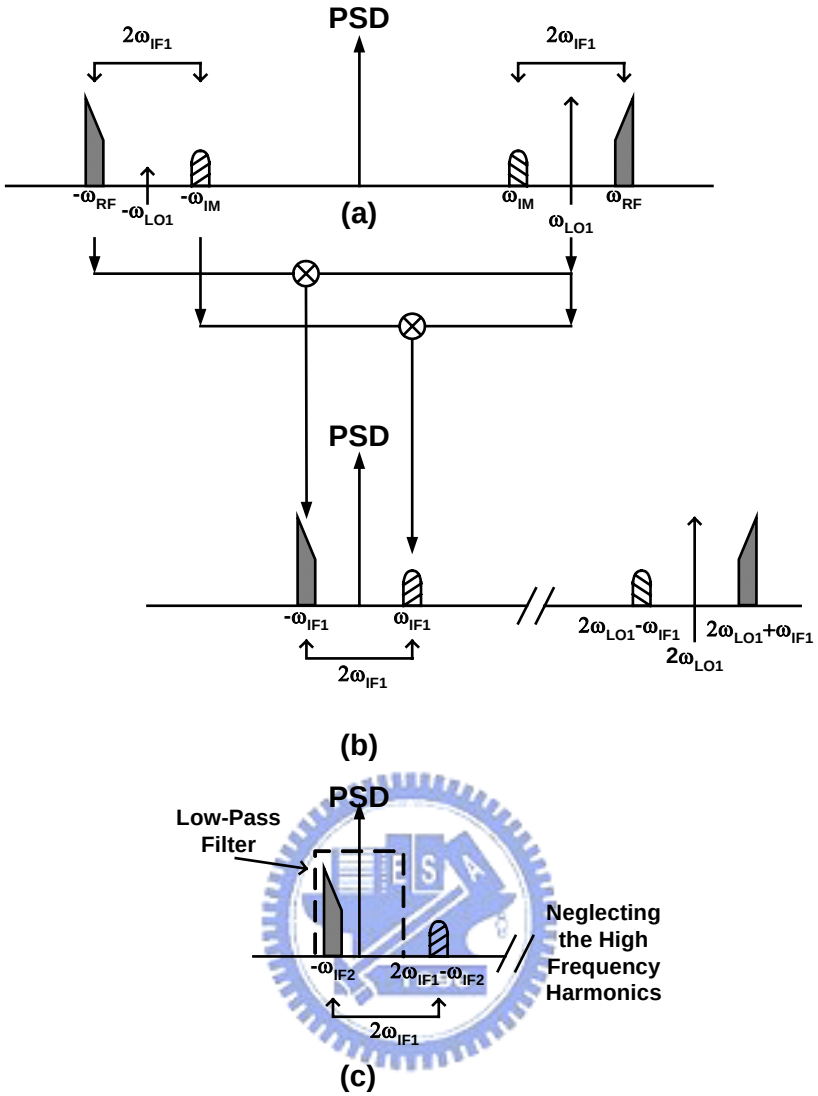


Fig. 4-15. The spectrum analysis of the Weaver down-converter using the complex mixing analysis: (a) the original RF and image signals before down-conversion, (b) the signals after down-converted by the first stage complex mixer, and (c) the final signals after down-converted by the first and second stage complex mixers.

A novel frequency quadrupler is used to generate LO_1 signals from LO_2 signals. Hence, in practical applications, the circuit demonstrated in this work needs only one low frequency local oscillator. This frequency planning provides good frequency spacing between LO and RF signals with reasonable circuit complexity. In addition, the low frequency oscillator is much easier to be implemented.

4.2a The Diagrammatic Explanation of the Image Rejection Degradation in Weaver Architecture

In this section, an interesting property is obtained to improve the image rejection

capability of the Weaver architecture. It is found in this dissertation that when the phase error of LO_1 and LO_2 is equal, the image rejection ratio can be optimized. The image rejection degradation can be caused by either signal mismatches or circuit mismatches. In order to determine the influences of LO signal mismatches, the diagrammatic explanation is used to analyze this problem. The ideal down-conversion process is shown in Fig. 4-15 and assuming that the RF and LO signals are perfectly matched without any phase error. Figure 4-16 shows a down-conversion process of the Weaver architecture when mismatches are taken into consideration. As shown in Fig. 4-16(a) and equation (4.2), the desired signal is mixed to the IF band by LO_1^+ ($\exp(j\omega_{LO1}t)$) and LO_2^+ ($\exp(j\omega_{LO2}t)$) signals that are both in the positive frequency spectrum.

However, when the LO_1 signal becomes slightly mismatch or it contains some phase errors, there will be an LO_1^- signal ($\exp(-j\omega_{LO1}t)$). The LO_1^- signal is drawn in the dot-line and located in the negative spectrum as shown in Fig. 4-16(b). The LO_1^- signal arises with the existence of phase errors. The image signal mixed by the LO signal imperfections is shifted to the positive frequency in the spectrum by LO_1^- at first. Next, it is shifted to the negative frequency in the spectrum by the LO_2^+ as shown in Fig. 4-16(b). The process of the image signal down-converted by the LO_1^- and LO_2^+ can be described as:

$$\begin{aligned}&\text{Image (Down-converted by } LO_1^- \text{and } LO_2^+) \\ &= \cos\omega_{IM}t \times LO_1^- \times LO_2^+ = \frac{e^{j\omega_{IM}t} + e^{-j\omega_{IM}t}}{2} \times e^{-j\omega_{LO1}t} \times e^{j\omega_{LO2}t} \\ &= \frac{e^{-j\omega_{IF1}t} + e^{j(-2\omega_{LO1}+\omega_{IF1})t}}{2} \times e^{j\omega_{LO2}t} = \frac{e^{-j\omega_{IF2}t} + e^{j(-2\omega_{LO1}+\omega_{IF1}+\omega_{LO2})t}}{2}\end{aligned} \tag{4.5}$$

Comparing equation (4.3) and (4.5) there is an in-band image signal in the IF bandwidth. As illustrated in Fig. 4-16(c), there is a down-converted unwanted signal caused by the mismatch LO_1^- just located in the same frequency band of the desired signal. As a result, the image rejection ratio is likely degraded by the signal imperfection as illustrated in these figures. Figure 4-16 can visualize the image rejection mechanism of the Weaver architecture. It is important that the image rejection of the Weaver architecture only can be degraded by the signal as shown in

equation (4.4) when mismatch signals are taken into consideration.

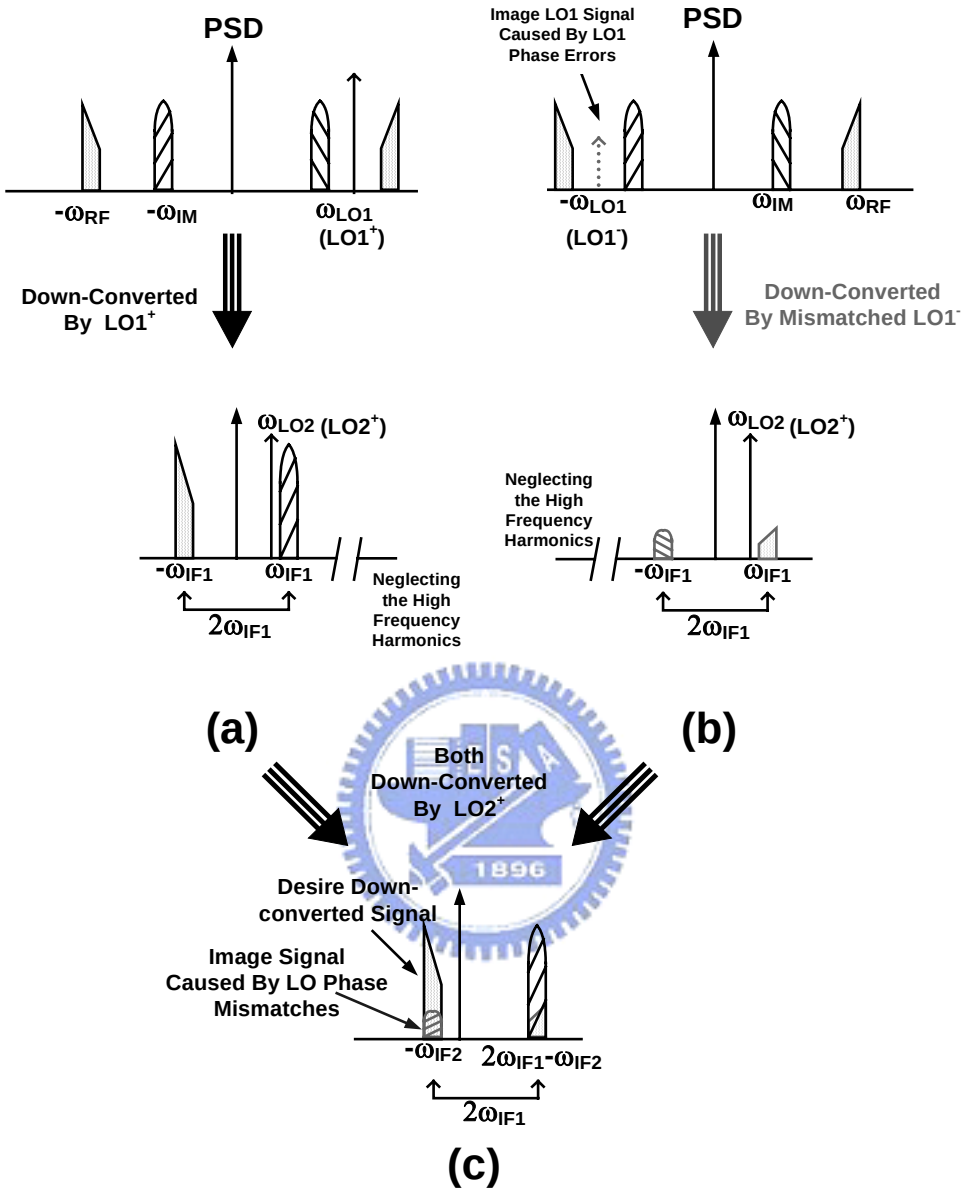


Fig. 4-16. The spectrum analysis of the Weaver down-converter when the effect of LO_1 and LO_2 signal mismatches are considered. (a) The desired IF signal, (b) the unwanted image signal caused by signal mismatches, and (c) the final mixed signals.

According to previous work [70] the image rejection ratio is influenced by mismatch signals and can be determined by:

$$IR(dB) = 10 \times \log\left[\frac{1+(1+\Delta A)^2 + 2(1+\Delta A)\cos(\phi_{\varepsilon 1}+\phi_{\varepsilon 2})}{1+(1+\Delta A)^2 - 2(1+\Delta A)\cos(\phi_{\varepsilon 1}-\phi_{\varepsilon 2})}\right] \tag{4.6}$$

The coefficient ΔA describes the gain or magnitude mismatches between in-phase and quadrature-phase paths, and the factor $\phi_{\varepsilon 1}$ and $\phi_{\varepsilon 2}$ represent the phase errors of the signal LO_1 and the signal LO_2, respectively [70]. According to the equation (4.6), it is found that if the $\phi_{\varepsilon 1}$ is equal to $\phi_{\varepsilon 2}$, the image rejection performance can be optimized. The detailed derivation of image rejection ratio in the Weaver down-converter is given in appendix A; in addition, the discussion and comparison of image rejection ratio between Weaver and Hartley architectures are also summarized in appendix A. In our work, no intentional low pass filter is used and the low pass function as shown in Fig. 4-14(a) is achieved sufficiently by the frequency response of the IF circuits. It is because the gain and phase mismatches of the additional low pass filters caused by the process variation can degrade the image rejection ratio.

Instead of the complicated trigonometric analysis, the diagrammatic explanation of the complex mixing gives the RF designers an instinct to arrange the frequency planning when they design the Weaver image rejection architecture. Consequently, the Weaver receiver can filter out the image signals referred to the frequency of the first LO signal. In our work, the frequency of image signal is 3.1 GHz when the frequency of RF signal is 5.7 GHz and the designed frequency of LO_1 is 4.4 GHz. Similarly, when RF signal is 5.2 GHz and LO_1 equals to 4 GHz, the image signal is 2.8 GHz.

4.2b Image Rejection Improvement of the Weaver Down-Converter

In this section, a useful technique to improve the image rejection performance of the Weaver down-converter is discussed. As shown in Fig. 4-14(a), the Weaver architecture requires quadrature LO signals at both LO_1 and LO_2 frequencies in order to eliminate the image signal. Different LO signals can be either generated by two separate local oscillators or by one local oscillator with some circuits that can produce the other LO frequency. Generally speaking, there are two methods to generate different LO frequencies with only one LO signal source: the frequency dividing or the frequency multiplying. The frequency of LO_2 is usually lower than that of LO_1 in a Weaver down-converter, and one possible approach of generating LO signals is to scale the LO_1 frequency down to the LO_2 frequency. In this kind of arrangement, a precise divider circuit is needed not only to scale down the LO frequency but also to

generate accurate quadrature signals. Instead of frequency dividing, a frequency multiplying circuit is incorporated to generate the LO signals in this work. Obviously, it is much easier to implement a good low frequency oscillator than a good high frequency oscillator in the same technology. In this work, the Weaver down-converter only needs a single low frequency local oscillator, and a special multiplier is employed to generate the LO_1 signals.

Generating another signal from one local oscillator inevitably produces extra phase error compared with original signals. Both multiplying and dividing processes will distort the generated signal because of the imperfections of multiplier and divider themselves. Basically, the analog Gilbert multiplier [2] is widely used to multiply signals and the Gilbert multiplier contains a differential pair and a current commutation Gilbert cell for its two input port. If the time delays between the upper (the Gilbert cell) and lower (the emitter-coupled pair transistors) input ports of the multiplier are considered, there is actually a time delay $\Delta\theta$ between two input signal paths. As a result, the output signal will consist of additional phase errors.

On the other hand, if the multiplier used in this work is able to minimize the time delay when it multiplies, the LO_1 signal will contain much less phase errors. The image rejection can be defined by (4.6) [70]. Figure 4-17 shows a simulation result of image rejection ratio with ideal system components by the ADS harmonic balance simulation. The image rejection ratio is a function of the LO_2 and the LO_1 phase errors. In this simulation, the LO_1 phase error is set to be equal to the LO_2 phase error plus additional 3 degrees error. The other simulation result is that the LO_1 and LO_2 phase errors are set to be equal. As shown in Fig. 4-17, the image rejection ratio is much larger when the LO_2 phase error is equal to the LO_1 phase error.

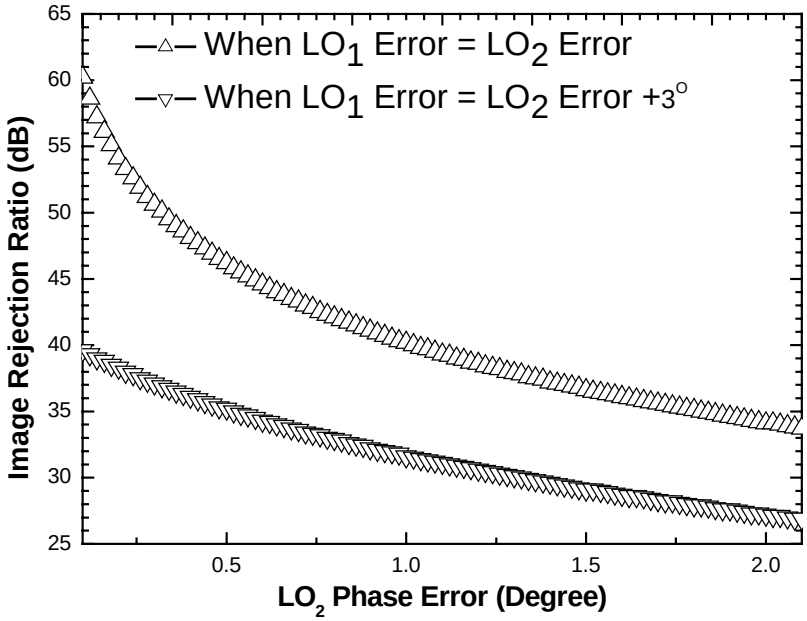
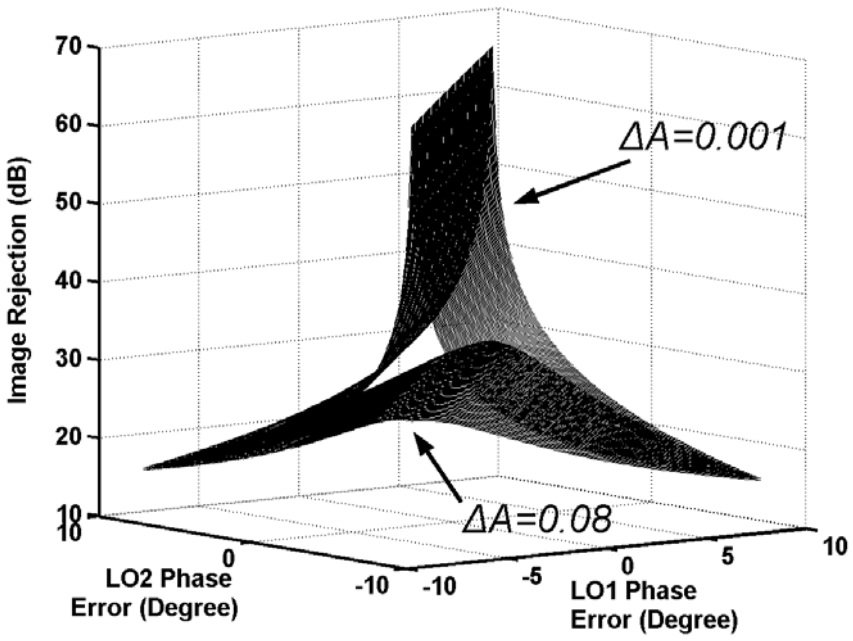
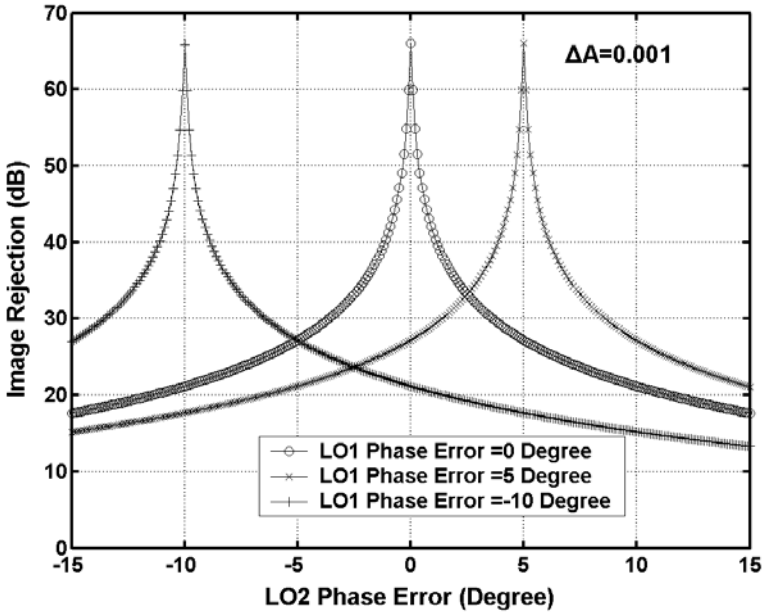


Fig. 4-17. The ADS simulation results of the image rejection ratio influenced by different LO phase mismatches.



(a)



(b)

Fig. 4-18. (a) The simulated image rejection ratio as a function of phase error $\phi_{\varepsilon 2}$ of the LO_2 signal and the phase error $\phi_{\varepsilon 1}$ of the LO_1 signal, and (b) a simplified simulated image rejection ratio as a function of LO_1 and LO_2 phase errors.

Figure 4-18(a) shows the simulated image rejection ratio as a function of the phase errors, $\phi_{\varepsilon 1}$ and $\phi_{\varepsilon 2}$ with gain mismatch, ΔA as a parameter. The maximum image rejection ratio occurs when the LO_1 phase error equals the LO_2 phase error as shown in Fig. 4-18(a). The image rejection in equation (4.6) as a function of the phase error of LO_2 when the gain mismatch and the phase error of LO_1 are fixed is shown in Fig. 4-18(b). The gain mismatch is fixed to be 0.001, and the phase error of LO_1 is fixed to 0^o, 5^o, and -10^o, respectively. As shown in Fig. 4-18(b), the maximum image rejection ratio occurs when $\phi_{\varepsilon 1}$ and $\phi_{\varepsilon 2}$ are identical. Therefore, as long as the $\phi_{\varepsilon 1}$ and $\phi_{\varepsilon 2}$ are identical, the image rejection ratio can be maximized.

A time-delay compensated multiplier that will be discussed in the next section can reduce the phase error of LO_1. This fully symmetrical frequency quadrupler circuit is incorporated in this work to generate the LO_1 signal from the LO_2 signal. Compared with the analog Gilbert multiplier, the frequency quadrupler used here can compensate the time delay produced by the multiplier circuit when the LO_1 is generated from the LO_2. It is worthwhile to mention that the frequency quadrupler employed in this work is useful to improve the image rejection performance. The

added phase error in multiplying process is minimized when the frequency quadrupler generates LO_1 signals. As mention in previous section, the equation (4.6) has a maximum value when $\phi_{\varepsilon 1} = \phi_{\varepsilon 2}$.

Moreover, the quadrature generator used in this work is a multi-section passive polyphase filter. The polyphase filters used here are carefully designed to have a reasonable bandwidth to overcome the fluctuation caused by any process variation. Because the GaInP/GaAs technology provides accurate thin-film resistor that helps to fabricate precision resistors, the passive polyphase filters become more accurate. As a result, the phase error ϕ_1 caused by the quadrature generator can be minimized.

The 5.2 and 5.7 GHz GaInP/GaAs HBT Weaver down-converter has the following frequency planning: (1) When RF signal is 5.7 GHz, the LO_1 signal equals to 4.4 GHz and the LO_2 is 1.1 GHz. (2) When RF signal is 5.2 GHz, the LO_1 is 4 GHz and the LO_2 is 1 GHz. IF signals are designed always 200 MHz in both cases, and the measured image rejection ratio is 44 dB in case (1), and 48 dB in case (2).

4.2c Implementation of the GaInP/GaAs HBT Weaver System

A detailed schematic of the total circuit is shown in Fig. 4-19. The circuit topology of the first stage mixer is shown in Fig. 4-20. This type of mixer is known as the micromixer [29], [30] for the RF active mixer design. If the resistance of resistor R_1 and R_3, and the transconductance of transistor Q_5 are properly designed, the input resistance when looking into the RF input port is matched to 50 Ω.

The RF input stage of the micromixer is single-ended and the input stage functions as a high-frequency active balun that can be used to generate differential RF currents. A common-collector output buffer is employed to drive the circuits of the next stages. This mixer stage provides about 8 dB conversion gain in simulation when the RF frequency is 5.2 GHz.

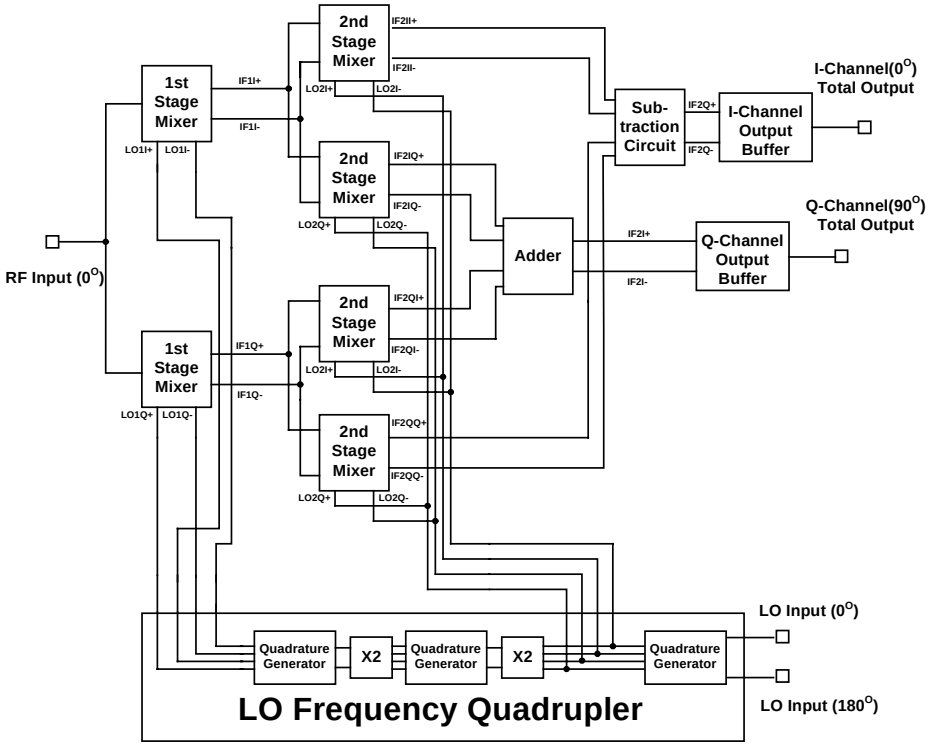


Fig. 4-19. The total schematic of the 5.2/5.7 GHz GaInP/GaAs HBT 48 dB image rejection Weaver down-converter.

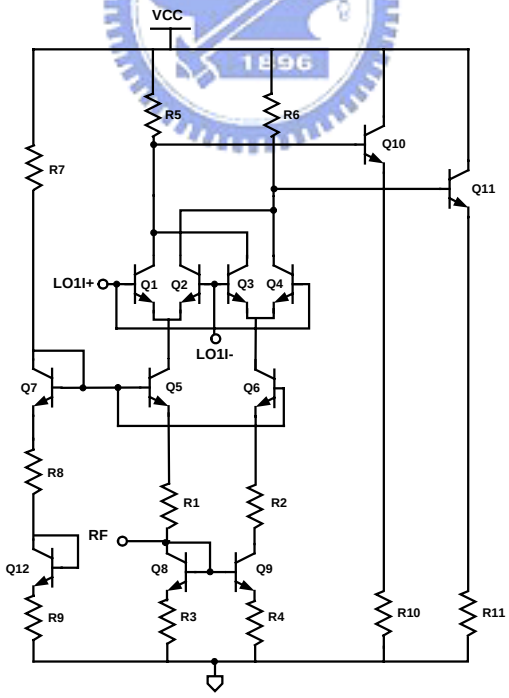


Fig. 4-20. The schematic of the micromixer used as the first stage mixer.

Figure 4-21 shows the schematic of the second stage mixer, and it is a conventional Gilbert mixer [2]. The Gilbert active mixer usually suffers from the slow

frequency response of the emitter-coupled pair at the RF input port. The RF input signal of the second stage mixer has been already down-converted by the first stage mixer; therefore, the RF input frequency of the second stage mixer is much lower than that of the first stage mixer. Thus, the conventional Gilbert type active mixers can be used here for the second stage. In order to increase the P_{1dB} of the differential pair, emitter degenerated resistors are added. In the second stage, the mixer must be designed to obtain enough input signal dynamic range. This stage is designed to provide about 7 dB conversion gain in simulation.

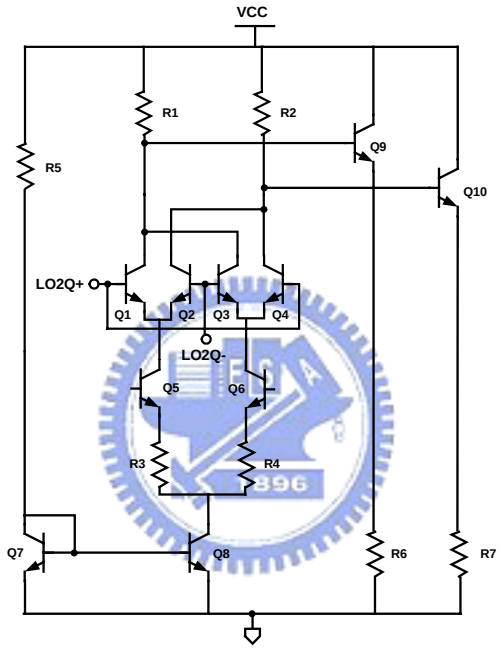


Fig. 4-21. The schematic of the Gilbert mixer used as the second stage mixer.

For the requirements of addition and subtraction in the complex Weaver architecture, two circuits based on the degenerated differential amplifier are designed: one for addition, and the other for subtraction. As shown in Fig. 4-22(a), this circuit functions as an adder if the outputs of the two differential amplifiers are directly connected together. It is the current mode adding technique. However, if the outputs of differential amplifiers are connected in an anti-phase way, the output currents subtract each other.

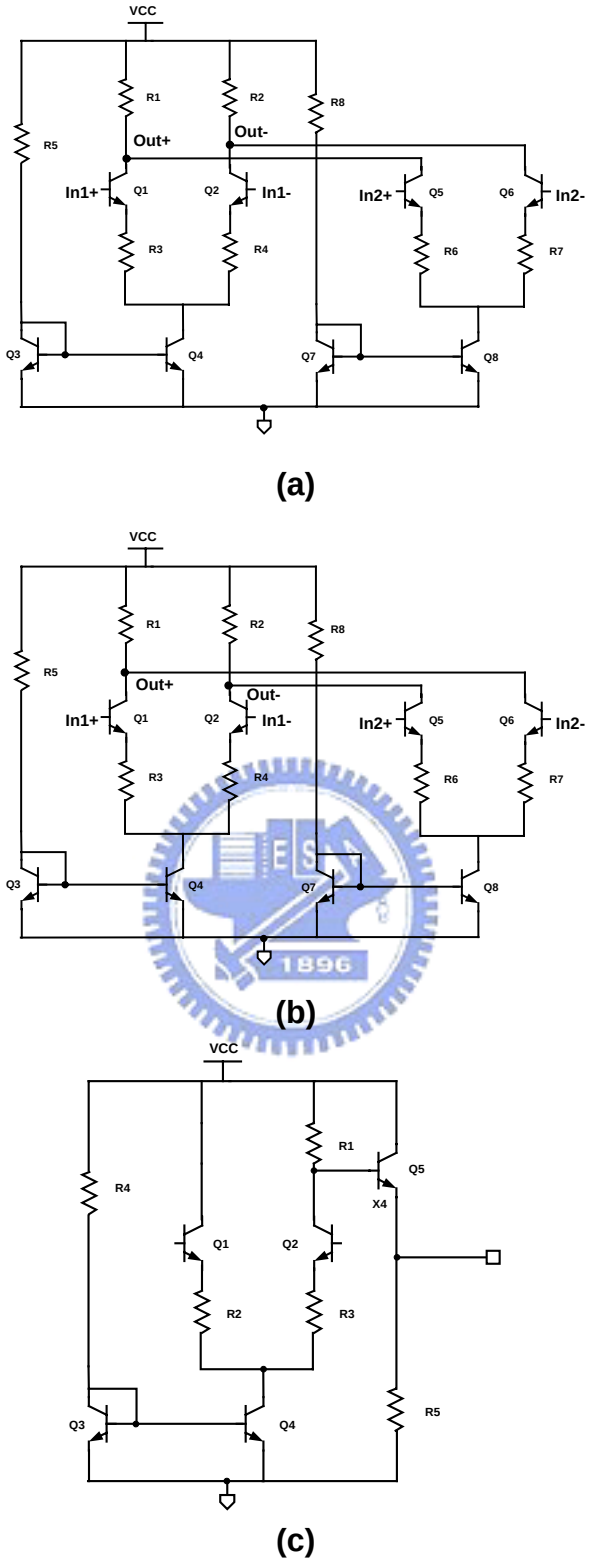


Fig. 4-22. The schematic of (a) the adder, (b) the subtraction cell, and (c) the output buffer.

Figure 4-22(b) illustrates a subtraction circuit. In this stage, the down converted 5.2 GHz RF signals are already amplified about 16 dB by previous two mixer stages in our simulation. Therefore, the addition and subtraction stages should be designed to

prevent the early gain compression. If the signal waveform is clipped, or in other words the waveform is distorted, the image rejection ratio degrades dramatically. In addition, the adder and subtraction circuit also behave as a voltage buffer, and thus the loading effect of the mixers can be reduced.

Figure 4-22(c) illustrates the output buffer. The output buffer is an asymmetrical differential amplifier with emitter degeneration. This stage is designed to drive the output as well as amplification. The transistor Q_5 as shown in Fig. 4-22(c) consists of four transistors to increase the output current with reasonable current density. There are several ways to generate quadrature signals: frequency dividers, the VCO that can directly generate quadrature output signals, and passive RC networks. The frequency quadrupler used in this work can generate 4 GHz signals for the first stage mixer.

The frequency quadrupler consists of two truly-phase-balanced frequency multipliers [43], [44], [76], three two-section passive polyphase filters and an output buffer. The polyphase filters are employed to generate quadrature LO signals and the symmetrical multiplier is used to double the LO signal. First of all, the external differential LO_2 signals become differential-quadrature after passing through the polyphase filters. Secondly, the symmetrical multipliers will double the frequency of quadrature LO_2.

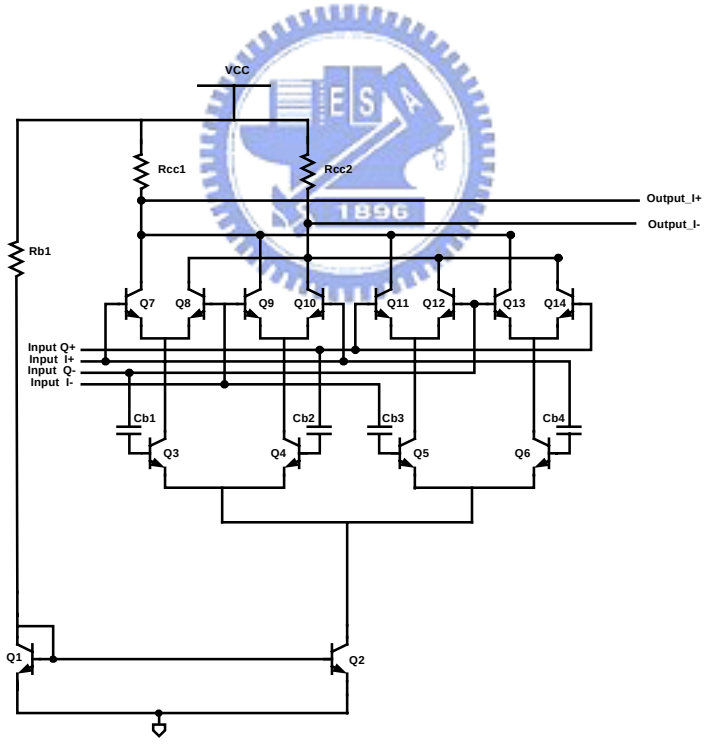
Repeating the process above, the LO_1 signal can be generated from LO_2 signals. Only one external 1 GHz LO signal is needed in this work when the RF frequency is 5.2 GHz. Because the loss caused by the passive polyphase filters is considerable, each section of frequency multipliers is designed to provide certain gain to compensate the loss of the passive polyphase filters. The circuit topology of the truly-phase-balanced frequency multiplier is illustrated in Fig. 4-23(a). The highly symmetrical multiplier consists of a pair of two conventional multipliers.

One multiplying path contains a phase lead and the other path contains a phase lag as shown in Fig. 4-23(b). Thus, the time delays between the upper and lower input stages can be set as a phase lead $-\Delta\theta/2$ and a phase lag $\Delta\theta/2$, respectively. When the node A and the node B are connected together, the signals contain no additional phase

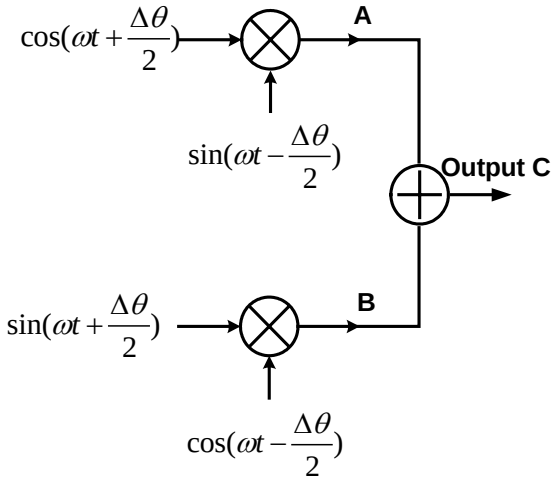
error [43], [44], [76]. It can be described as:

$$A = \cos(\omega t + \frac{\Delta\theta}{2}) \times \sin(\omega t - \frac{\Delta\theta}{2}) = \frac{1}{2}[\sin 2\omega t - \sin\Delta\theta]$$
$$B = \sin(\omega t + \frac{\Delta\theta}{2}) \times \cos(\omega t - \frac{\Delta\theta}{2}) = \frac{1}{2}[\sin 2\omega t + \sin\Delta\theta] \quad (4.7)$$
$$\therefore C = A + B = \sin 2\omega t$$

As a result, the multiplier is suitable for generating accurate high frequency signals in our work. The frequency quadrupler is shown in Fig. 4-24. Using the compensation mechanism of the quadruple frequency multiplier, no extra phase difference of the LO_1 and LO_2 caused by the multiplying process occurs, and thus the image rejection is improved. Because the frequency doubler is a wideband multiplier, it is very easy to generate the 4 GHz and 4.4 GHz LO_1 signals. An output buffer is used to drive LO_1 stage with enough pumping power.



(a)



(b)

Fig. 4-23. (a) The schematic of the highly symmetrical frequency multiplier, and (b) the block diagram of the multiplier.

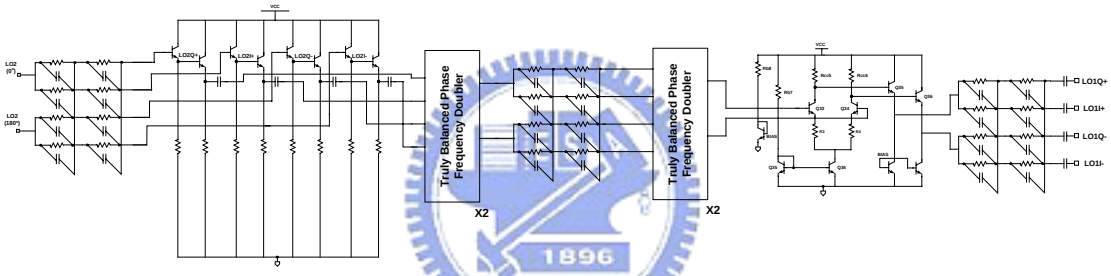


Fig. 4-24. The schematic of the frequency quadrupler used to correlate the LO_1 and LO_2 signals.

Figure 4-25 is the die photograph of the demonstrated GaInP/GaAs HBT Weaver down-converter. The total chip size is 2.5 mm x 2 mm. As shown in Fig. 4-25, RF input GSG pad is on the left side of the chip, while the differential LO GSGSG pad is on the right side of the die. The IF output GSGSG pad is on the top of the chip, and DC pads are on the bottom of the die.

The demonstrated Weaver down-converter is fabricated using the 2 um GaInP/GaAs HBT technology. This HBT process provides following technical capability: The cutoff frequency of the HBT device is 40 GHz and the BV_{CEO} is about 11 V. This work is designed using 2 um x 2 um, 2 um x 4 um, and 2 um x 6 um transistors. All of the transistors used in this work are single-emitter, single-base, and single-collector transistors. The DC supply voltage of the Weaver down-convert is 5 V. The measured conversion gain as a function of LO power when the RF = 5.7 GHz and

the IF = 200 MHz is shown in Fig. 4-25.

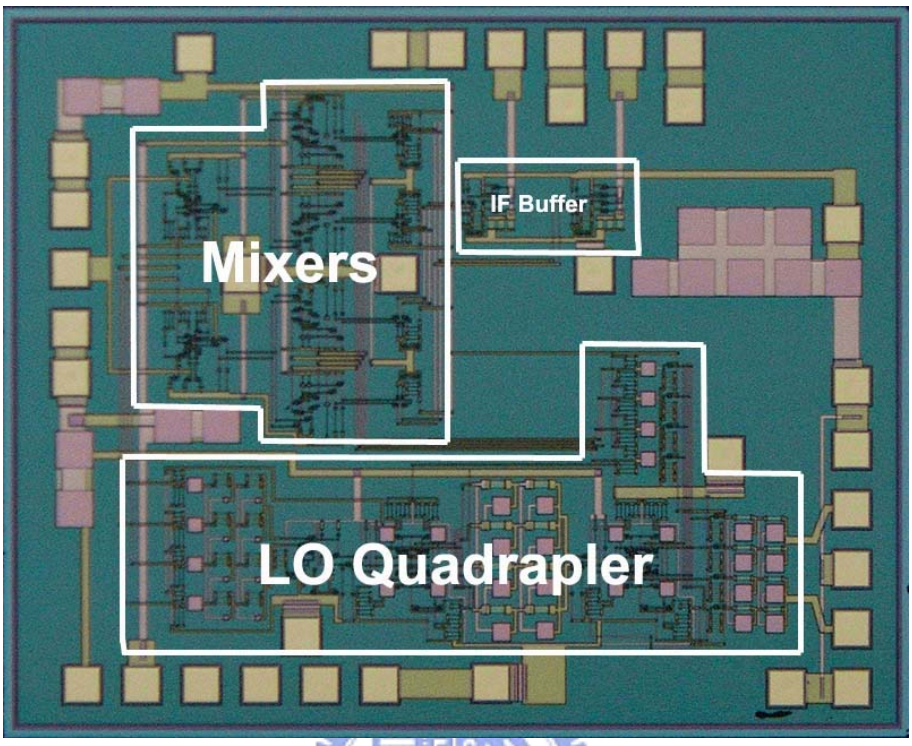


Fig. 4-25. The die photo of the 5.2/5.7 GHz GaInP/GaAs HBT 48 dB image rejection Weaver down-converter using LO frequency quadrupler.

As shown in Fig. 4-26, the peak conversion gain is 18.5 dB for LO powers from 0 to 5 dBm when RF frequency is equal to 5.7 GHz. Figure 4-26 also depicts the conversion gain as a function of the LO power when RF frequency is 5.2 GHz and IF frequency is 200 MHz. As shown in Fig. 4-26, the conversion gain reaches the maximum value (20.5 dB) when the LO power is larger than 4 dBm.

The following section reports the image rejection ratio of the Weaver down-converter when the RF frequency is 5.7 GHz and 5.2 GHz. Because the frequency quadrupler minimizes the phase error of LO_1, the image rejection can be improved as discussed in Fig. 4-18. The measurement setup is carefully prepared to provide balanced LO signals and thus the intrinsic high image rejection ratio of our work can be demonstrated. In addition, the LO signal paths are well organized, the length of each quadrature LO paths are carefully laid out and their lengths are made as equal as possible.

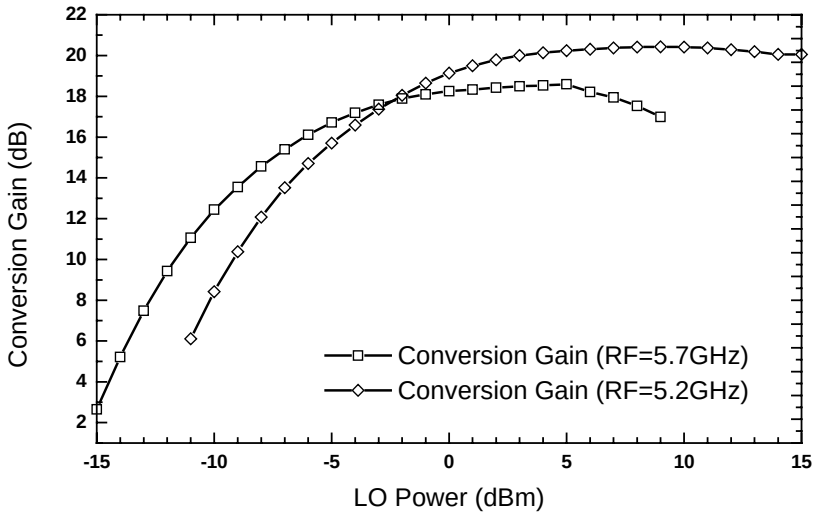
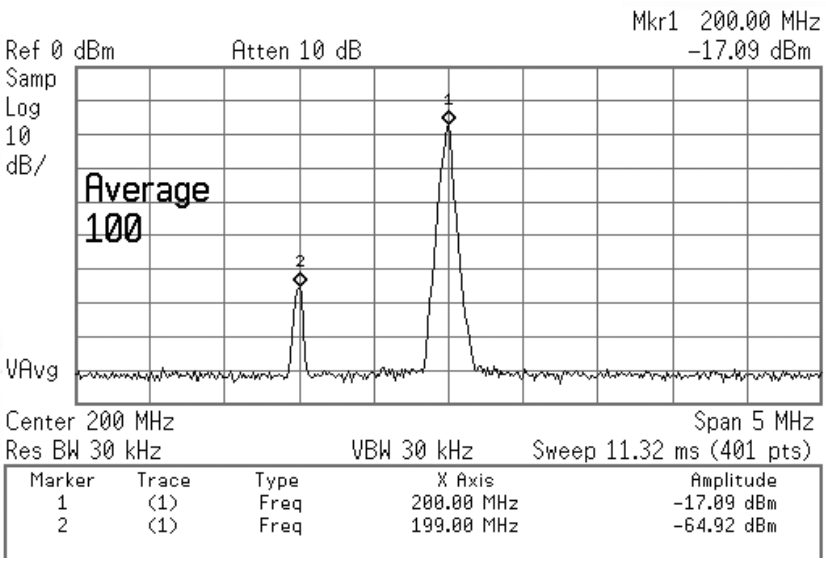
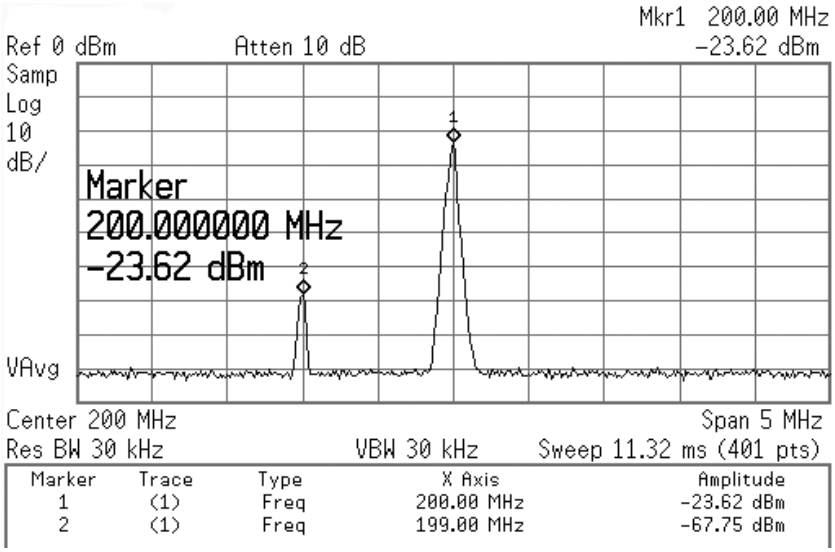


Fig. 4-26. The measurement results of the conversion gain as a function of LO input power of the Weaver down-converter when input RF frequency is 5.7 GHz and input RF frequency is 5.2 GHz respectively.

Fig. 4-27 shows the measurement results of the image rejection ratio when the RF input frequency is 5.2 GHz. The measured spectrum shows the IF output power when the desired and image signals are both sent to the RF input port of the Weaver down-converter. In simulation, the image rejection ratio is up to 60 dB. According to the experimental results, the image rejection performance is degraded, and it could be due to the circuit mismatch in fabrication.



(a)



(b)

Fig. 4-27. The measured image rejection of the proposed Weaver down-converter (a) when the RF frequency is 5.2 GHz and the image signal is 2.8 GHz; (b) when the RF frequency is 5.7 GHz and the image signal is 3.1 GHz.

As shown in Fig. 4-27, there is a deliberate 1 MHz offset between the desired and image signals in order to indicate the image rejection ratio in the output IF spectrum of the spectrum analyzer. The measurement result indicates that the image rejection ration is 48 dB when the desired signal is 5.2 GHz. Similarly, the image rejection ratio between RF and image signals is about 44 dB when RF input frequency is 5.7 GHz. Balanced external LO_2 signals are applied to the chip by careful calibration. However, there are no on-chip LO_2 signal phase/gain controls and tuning employed in this work. The demonstrated 48 dB image rejection ratio is achieved because the external LO_2 signals are truly balanced and the frequency quadrupler successfully minimizes the phase error. Although the frequency quadrupler can successfully minimize the phase error, the gain mismatch still remains. However, the frequency quadrupler in the LO signal path can tolerate the gain mismatch to some degree. The LO Gilbert cell only needs a small LO power for current commutation. Therefore, the image rejection performance is insensitive to the gain mismatch of the frequency quadrupler in the LO path as long as the LO signal is large enough. Thus, the formula (2.6) can be applied to calculate the gain mismatch of our chip if LO_1 and LO_2 phase errors is zero for the maximum image rejection ratio. The calculated gain mismatch corresponding to 48 dB image rejection ratio is 0.8%

When the RF frequency is 5.2 GHz (5.7 GHz), the frequency of the secondary image [72], [73] is 4.8 GHz (5.3 GHz). The measurement results showed no secondary image rejection because the demonstrated circuit does not have the capability of filtering out the secondary image. The high-speed analog-to-digital converter together with the digital signal complex filter or the analog polyphase complex filter can be employed to remove the secondary image signal.

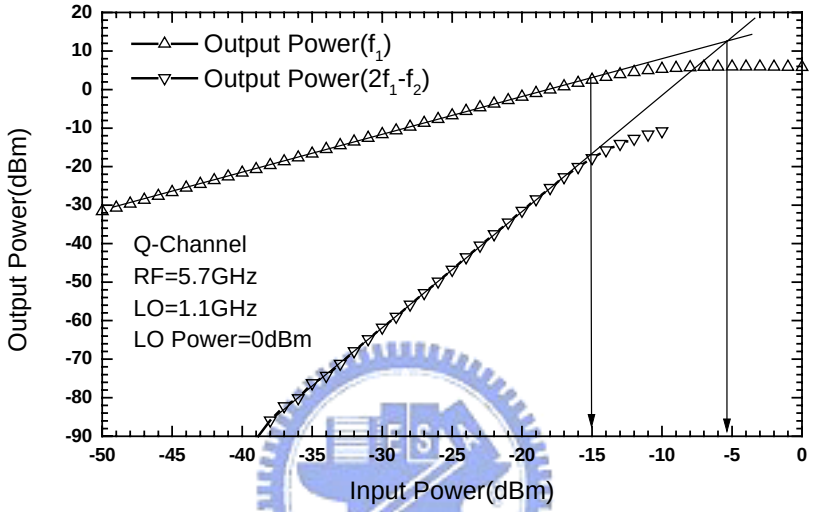


Fig. 4-28. The measured power performance as a function of RF input power of the Weaver down-converter when RF frequency is 5.7 GHz.

The measured power performance as a function of RF input power is shown in Fig. 4-29 when RF=5.7 GHz and RF=5.2 GHz. The experimental data shows that IP_{1dB} is –15 dBm, and IIP_3 is –5 dBm when RF=5.7 GHz. The IP_{1dB} is –15 dBm, and IIP_3 is –8 dBm when RF=5.2 GHz.

Figure 4-30 shows the input return loss of the RF port and the output return loss of the IF port. The input returns loss is better than 16.5 dB from DC to 6 GHz as shown in Fig. 4-30, and the output return loss is better than 11 dB when the output frequency is 200 MHz.

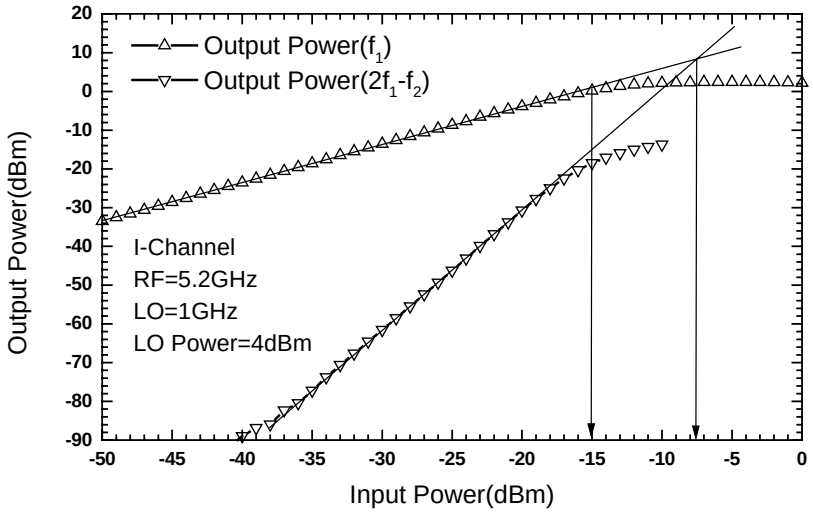


Fig. 4-29. The measured power performance as a function of RF input power of the Weaver down-converter when RF frequency is 5.2 GHz.

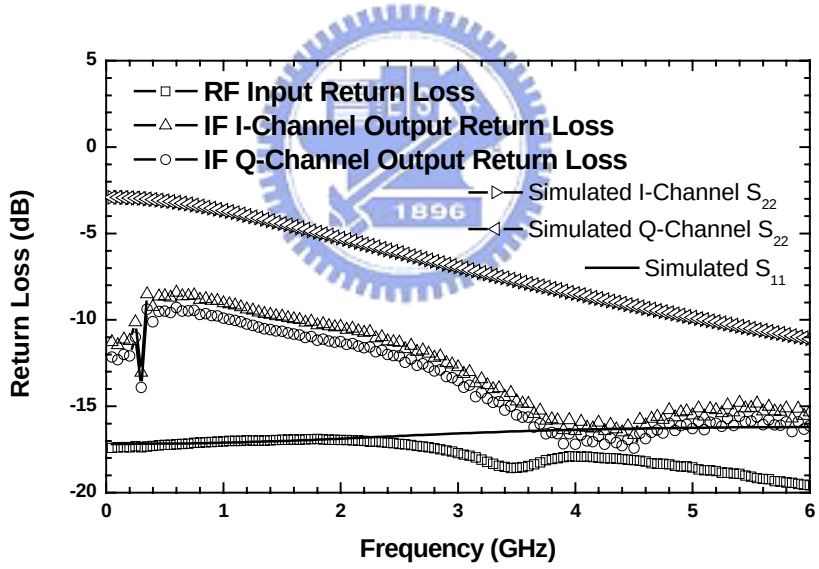


Fig. 4-30. The measured and simulated input and output return losses of the Weaver down-converter.

Figure 4-31 shows the RF-to-IF isolations when IF is fixed to 200 MHz and the isolations are better than -40 dB. Figure 4-32 shows that the LO-to-IF isolations are about -26 to -30 dB when the LO frequency starts from 0.9 GHz to 1.2 GHz. The LO to RF isolation is also illustrated in Fig. 4-32, the measurement results indicate that the isolation is better than -72 dB.

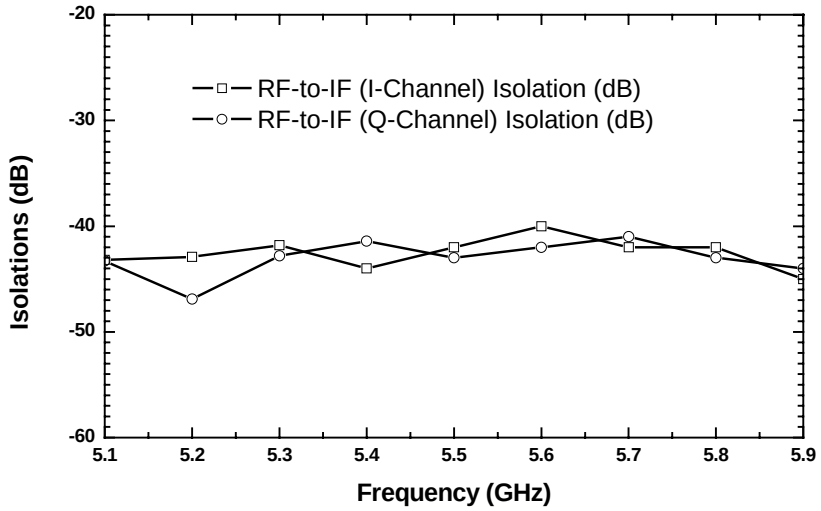


Fig. 4-31. The measured RF-to-IF isolation for both I-channel and Q-channel of the Weaver down-converter.

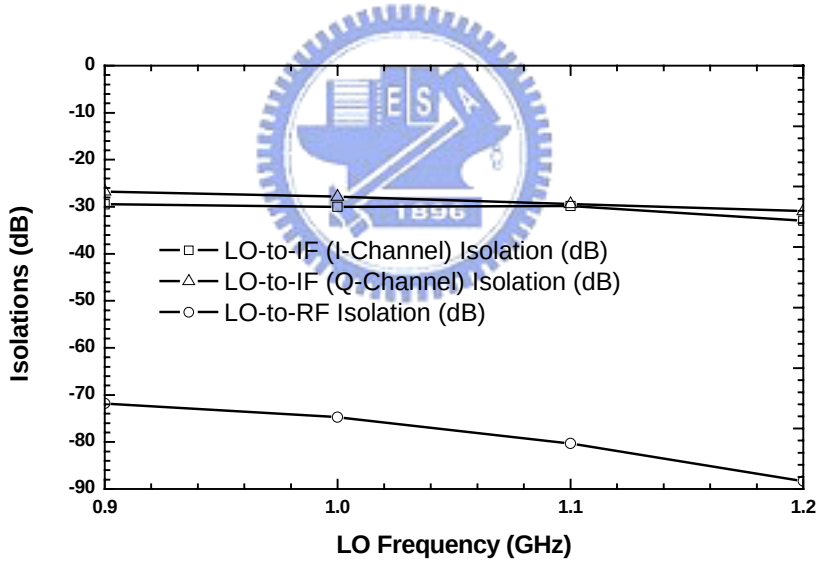


Fig. 4-32. The measured LO-to-IF and LO-to-RF isolations for both I-channel and Q-channel of the Weaver down-converter.

A diagrammatic explanation using the complex mixing technique to analyze the image rejection mechanism is developed and a 48 dB image rejection Weaver architecture down-converter when the RF frequency is 5.2 GHz is demonstrated in this dissertation. The GaInP/GaAs HBT down-converter has 44 dB image rejection ratio when the RF frequency is 5.7 GHz. Both the down-converted IF frequencies are kept the same (200 MHz) by changing the LO input frequencies for the different RF

frequency applications. The rejection capability of the image signals of 2.8 and 3.1 GHz is achieved by the Weaver architecture with the LO frequency quadrupler. Because the frequency quadrupler minimizes the phase error when generating LO_2 signals, thus the LO_1 and LO_2 signals are highly coherent. Consequently, the image rejection ratio is improved.

The conversion gain is 20.5 dB when the RF frequency is 5.2 GHz and the conversion gain is 18.5 dB while the RF frequency is 5.7 GHz. The input return loss is better than 16.5 dB from DC to 6 GHz and the output return loss is better than 11 dB when output frequency is 200 MHz. The IP_{1dB} is –15 dBm, the IIP_3 is –5 dBm when RF=5.7 GHz and the IP_{1dB} is –15 dBm, IIP_3 is –8 dBm when RF=5.2 GHz. The RF-to-IF port isolation, the LO-to-IF isolation and the LO-to-RF isolation are better than -40 dB, -26 dB and -72 dB, respectively.

There is a significant difference between the simulated and measured image rejection ratio. The cause of degradation of the image rejection ratio is the circuit mismatch during the chip fabrication. A small circuit mismatch can easily destroy the image rejection performance [6], [70], and it is not easy to predict when doing the pre-simulation in GaInP/GaAs HBT technology resulting from the lacking of the corner model for the pre-simulation. Besides, the post-simulation tool such as LPE is absence in this technology; however, the GaInP/GaAs HBT technology can provide accurate passive components and does not suffer from the parasitic effects. Therefore, the GaInP/GaAs HBT technology is still suitable for the high performance image rejection down-converter design.

Chapter 5

Dual-Band Down-Converter Using Weaver-Hartley Image-Rejection Architecture

The problem of the image signal exists in all of the wireless communication systems. In the past, an off-chip image rejection filter is employed to reject the image signal; however, the off-chip components limit the circuit integration and thus need to be removed. As a result, many highly integrated image rejection architectures are developed. One of the popular image rejection systems is the direct-conversion system as introduced in chapter 2. The direct-conversion architecture [18] eliminates the image signal by setting the IF frequency to be zero instead of using the image rejection filters. Although the integration level of the direct-conversion system can be very high, this system suffers from some series issues: the DC offset caused by the signal self-mixing problem [18], the mixer low frequency noise resulting from the transistor 1/f noise [9]. Sub-harmonic mixers and the area-consuming on-chip DC blocking capacitors are employed to prevent the DC offset problem and the transistor 1/f noise. Sometimes much more complicated octet-phase LO signal generation circuits are required for the direct-conversion system [3], [77]. Moreover, extra circuit techniques are necessary to improve the low frequency noise figure of the CMOS direct-conversion mixer [26], [36], [38]. On the other hand, the low-IF system as discussed in the previous chapter is useful to reject the image signal and thus the issues in the direct-conversion mixer are absent. The Hartley low-IF architecture is capable of rejecting image signals using the complex polyphase filters [6], [17], [75], [78], [79]. Because the IF frequency is not zero, the DC offset and the 1/f noise can be distinguished from the signal.

Another useful image rejection system is the Weaver system [7], [70], [71], [72], [80], [81] as described in Chapter 4. The Weaver system is a dual conversion system but no filter is needed when compared with the heterodyne system. The integration level of the Weaver architecture is also high because no off-chip image rejection filter is required. The Weaver system can effectively eliminate the first image signal, but the

Weaver structure suffers from the secondary image problem if the final IF is not zero [72]. A single-band low-IF dual-conversion system is implemented in [79], [80], and the secondary image is rejected by the polyphase filter in the second IF stage [79] while the first image is removed by the dual conversion mechanism [70], [81].

Most of the multi-band RF transceivers are implemented using the direct-conversion architectures [82]-[86]. These multi-band receivers use multi-LNAs and mixers to deal with each particular RF band. The direct-conversion system also requires extra approaches to eliminate the 1/f noise in the mixer stage [26], [36], [38]. In addition, the mixers can not be reused for most of the transceivers [82]-[85]. Some dual-band dual-conversion Weaver systems are demonstrated and the secondary image problem is avoided because the final IF in the second stage is set to be zero [72]. Thus, this receiver still suffers from the 1/f noise and DC offset problem; in addition, sometimes the mixers are not reused [72]. Moreover, most of these zero-IF multi-band receivers require more than one local oscillator [82], [85], [86]. Because the IF frequency is zero in the direct-conversion system, it is very difficult to design a VCO that can cover the 2.4 GHz and the 5.7 GHz by using simple dividing or multiplying. The extra VCO can cause the substrate cross talk and the spurious signals.

In this chapter, a 2.4/5.7-GHz dual-band low-IF down-converter system that combines both Weaver architecture and Hartley architectures [6], [70] is demonstrated using 0.18 um CMOS and 0.35 um SiGe BiCMOS technologies. The architecture used here combines the advantages of the previous literatures, and thus a dual-band system without the secondary image problem is achieved. When the desire signal is at 5.7-GHz, the 2.4-GHz band is set to be the image signal of the Weaver structure and vice versa [72], [86]. The LO_1 frequency is chosen to be 4.05-GHz, which is halfway between 2.4 GHz and 5.7 GHz. The 2.4/5.7-GHz band selection is achieved by changing the polarization of the complex LO_1 (first local oscillator) signals in this work. Because the low-IF architecture is employed in this work, it is very easy to perform a frequency arrangement that only needs one on-chip VCO. An LO generator consisting of a novel 50% duty cycle divide-by-five circuit and a truly balanced multiplier is employed to generate the 1.62-GHz LO_2 (second local oscillator) signal for the Weaver system and to increase image rejection performance of the entire

system [81]. Thus, the IF frequency of this low-IF down-converter is around 30-MHz. As a result, the extra VCO is not needed and the complexity is reduced. Compared with the previous literatures, the demonstrated Weaver-Hartley system has competitive rejection performance of the first image and the secondary image signals [70]- [72], [80], [81] because of the double-quadrature Hartley system [6], [75] and the coherence between the LO_1 and LO_2 signals [81]. Besides, the mixer stages (and the LNA) can be reused in our Weaver-Hartley structure.

In this work, the operational principle and the frequency planning of the proposed Weaver-Hartley image rejection architecture are discussed in Section 5.1. The diagrammatic complex mixing explanation [75], [81], [87] is employed to illustrate the image rejection mechanisms of this hybrid Weaver-Hartley architecture. Section 5.2 introduces a CMOS dual-band down-converter. When the RF signals are at 5.7-GHz, the demonstrated Weaver-Hartley down-converter achieves 40 dB image rejection ratio for the first image signal (around 2.4-GHz) and 46 dB image rejection ratio for the secondary image signals (around 5.64-GHz). On the other hand, when the RF signals are at 2.4-GHz, the demonstrated Weaver-Hartley down-converter achieves 40 dB image rejection ratio for the first image signal (around 5.7-GHz) and 44 dB image rejection ratio for the secondary image signals (around 2.46-GHz). Section 5.3 describes a 0.35 um SiGe BiCMOS dual-band down-converter

5.1 Weaver-Hartley Image Rejection Architecture

The block diagram of the proposed Weaver-Hartley image rejection structure is shown in Fig. 5-1(a). The angular frequencies of the desired, first image, and secondary image signals are denoted as ω_{RF}, ω_{IM1} and ω_{IM2}, respectively. The angular frequencies of the LO_1 and the LO_2 signals are denoted as ω_{LO1} and ω_{LO2}. The frequency of the IF signal down-converted by the first-stage mixers is defined as ω_{IF1} while the frequency of the IF signals down-converted by the second-stage mixers is defined as ω_{IF2}. The relations between the signals above are as follows:

$$\omega_{IF1} = \omega_{RF} - \omega_{LO1} = \omega_{LO1} - \omega_{IM1} \tag{5.1a}$$

$$\omega_{IF2} = \omega_{RF} - (\omega_{LO1} + \omega_{LO2}) = \omega_{LO1} + \omega_{LO2} - \omega_{IM2} = \omega_{IF1} - \omega_{LO2} \quad (5.1b)$$

As shown in Fig. 5-1(a), the first half of the down-converter is a single-quadrature Weaver system including six multipliers [70], [81]. The other half of the down-converter is a double-quadrature Hartley system consisting of four multipliers and polyphase filters [6]. The Weaver-Hartley image rejection system is formed by sharing four mixers as shown in Fig. 5-1(a). When the frequency of the desire signal is 5.7-GHz (2.4-GHz) and the LO_1 frequency is 4.05-GHz, the dual-conversion Weaver system perfectly rejects the first image signal whose frequency is near 2.4-GHz (5.7-GHz), and the frequency of the secondary image signal is around 5.46-GHz (2.46-GHz). In order to explain the function of the Weaver-Hartley structure, the complex signal block diagram representation for complex mixers is shown in Fig. 5-1 (b).

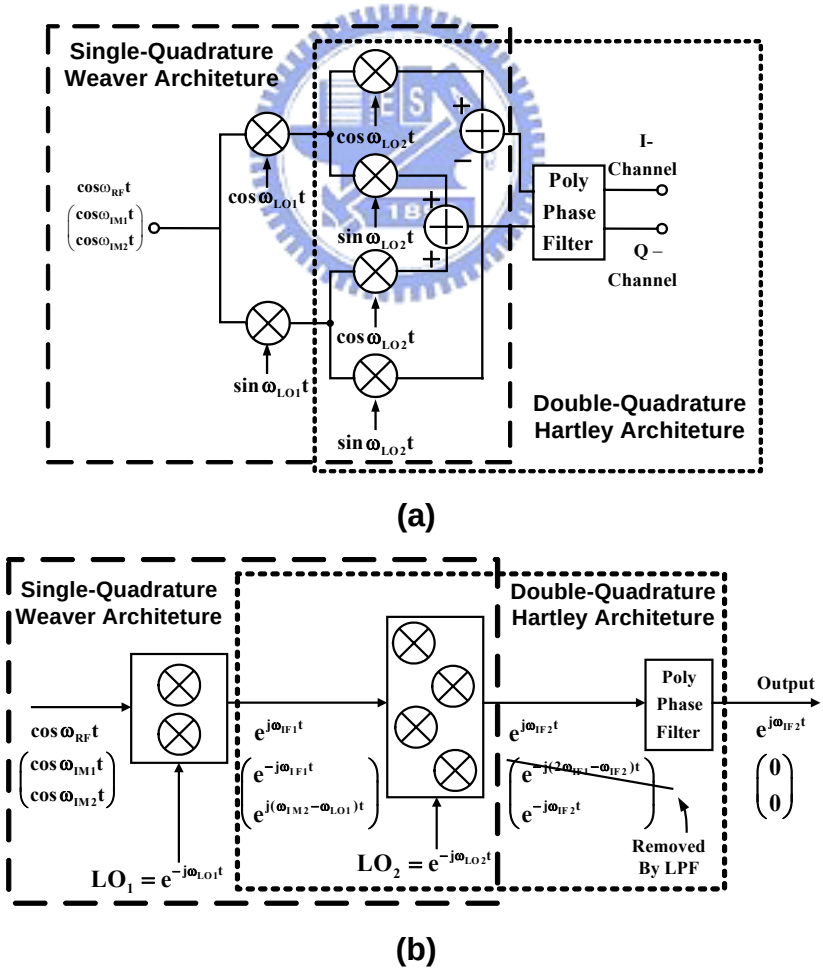


Fig. 5-1. (a) The block diagram of the Weaver-Hartley architecture, and (b) the complex representation of the Weaver-Hartley architecture.

Instead of the conventional trigonometric analysis, the complex signal diagrammatic explanation shown in Fig. 5-2 gives direct insight to the RF system architect. The RF signal and quadrature LO signals can be denoted as $\cos\omega_{RF}t$ and $e^{-j\omega_{LO}t}$, respectively. On the other hand, the first image signal and secondary image signal can be expressed as $\cos\omega_{IM1}t$ and $\cos\omega_{IM2}t$, respectively. Figure 5-2(a) shows the corresponding spectra of the ω_{RF}, ω_{IM1}, and ω_{IM2} signals.

Because the quadrature LO_1 signal ($e^{-j\omega_{LO}t}$) is located at the negative spectrum, the RF signals shifts left in the spectrum after down-conversion mixing [75], [81], [87]. In other words, after the complex LO_1 down-conversion, the positive RF complex frequency shifts to the positive ω_{IF1} complex frequency and the negative RF complex frequency shifts to the negative frequency of $\omega_{LO1}+\omega_{RF1}$ as shown in Fig. 5-2(b). Thus, the negative frequency spectrum in Fig. 5-2(b) can be omitted in the analysis for simplicity.

Next, the signals in Fig. 5-2(b) are down-converted further by the subsequent second-stage complex mixer. Similarly, the quadrature LO_2 ($e^{-j\omega_{LO}t}$) signal of the second-stage complex mixer is located at the negative spectrum. Therefore, the signals in Fig. 5-2(b) shift left in the spectrum again, as shown in Fig. 5-2(c). This process can be expressed by the complex signal multiplication [75], [81], [87] as:

$$\cos\omega_{RF}t \times e^{-j\omega_{LO1}t} \times e^{-j\omega_{LO2}t} = \frac{e^{j\omega_{IF2}t} + e^{-j(\omega_{RF}+\omega_{LO1}+\omega_{LO2})t}}{2} \tag{5.2a}$$

Similarly, the shifted IM_1 and IM_2 signals can be represented as:

$$\cos\omega_{IM1}t \times e^{-j\omega_{LO1}t} \times e^{-j\omega_{LO2}t} = \frac{e^{-j(2\omega_{IF1}-\omega_{IF2})t} + e^{-j(\omega_{IM1}+\omega_{LO1}+\omega_{LO2})t}}{2} \tag{5.2b}$$

$$\cos\omega_{IM2}t \times e^{-j\omega_{LO1}t} \times e^{-j\omega_{LO2}t} = \frac{e^{-j\omega_{IF2}t} + e^{-j(\omega_{IM2}+\omega_{LO1}+\omega_{LO2})t}}{2} \tag{5.2c}$$

The RF signal is down-converted to the positive ω_{IF2} complex frequency as shown in Fig. 5-2(c). On the other hand, the first image signal, ω_{IM1}, is

down-converted to the negative ($2\omega_{IF1} - \omega_{IF2}$) complex frequency. Because of the dual conversion phenomena, the first image signal can be easily filtered out by the low-pass filter as shown in Fig. 5-2(c). Normally, the frequency response of the IF circuits can serve as the low-pass filter as long as the ω_{IF1} is large enough.

The dual-conversion down-converter still suffers from the secondary image signal problem [72] and the frequency of the secondary image signal is $2\omega_{IF2}$ away from the RF frequency as shown in Fig. 5-2 (c).

The secondary image signal is also shifted downward twice by the two complex mixers of the Weaver system, too. However, the down-converted secondary image signal is not shifted outside of the frequency response of the low-pass filter as the first image signal, IM_1, does. Instead, the frequency of the down-converted secondary image signal is shifted to the negative ω_{IF2} spectrum while the down-converted RF signal is located at the ω_{IF2} as shown in Fig. 5-2(c). This down-converted secondary image signal can not be filtered out by the low-pass filter and disturbs the down-converted desired RF signal. On the other hand, the polyphase filter [6], [17], which is an asymmetrical complex notch filter, can filter out the down-converted secondary image signal by eliminating the signals in the negative spectrum, as illustrated in Fig. 5-2(d).

It is worthwhile to mention that the second-stage complex mixer and the IF polyphase filter form the double-quadrature Hartley system [6]. As a result, the demonstrated dual-band Weaver-Hartley system has more immunity to the non-ideal effects caused by signal mismatches for the secondary image rejection.

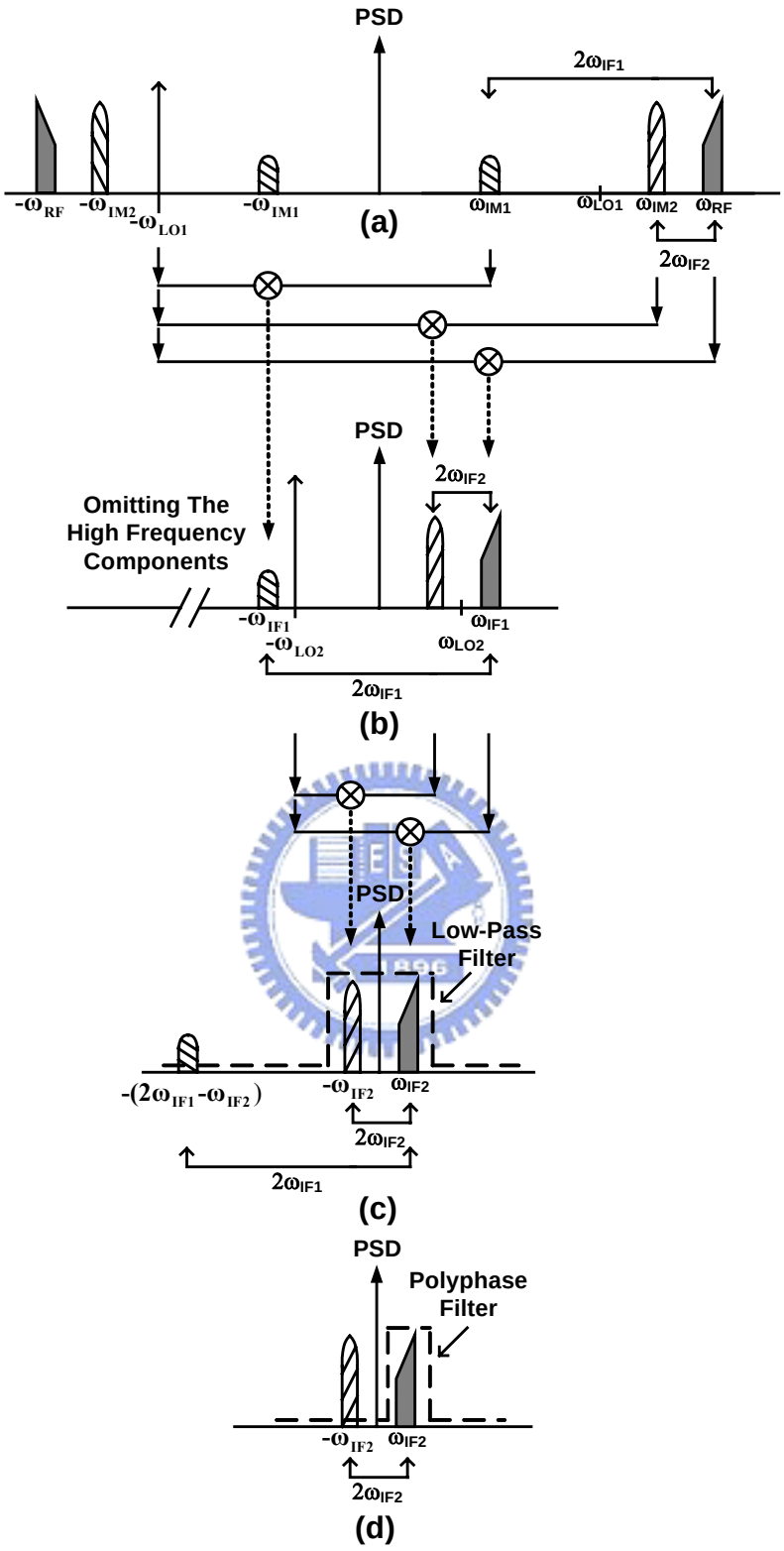


Fig. 5-2. (a) The RF, IM_1, and IM_2 signals before down-converted neglecting the signals located in the negative frequencies for simplicity; (b) the RF, IM1, and IM2 signals after down-converted by the first stage complex mixer; (c) the signals after down-converted by the second stage complex mixer; and (d) the signals filtered by the IF polyphase filters. All the high frequency harmonics are neglected.

Figure 5-3 shows a simplified down-conversion block diagram of a double quadratrue system, which is the second stage of the Weaver-Hartley system shown in Fig. 5-2, with non-ideal input signals. The degradation of the image rejection caused by the signal mismatches can be easily analyzed using the complex signal representation. When the signal mismatches such as gain and phase errors occur, it is equivalent to say that the false signals located at the negative spectrum appear [6]. Thus, in our case, the mismatched quadrature IF_1 signal can be represented as the linear combination of an ideal signal, IF_{1d} ($e^{j\omega_{IF1}t}$), and the error signal, IF_{1er} ($E_{r1}e^{-j\omega_{IF1}t}$), with different sequence orientations as follows [6]:

$$e^{j\omega_{IF1}t} + E_{r1}e^{-j\omega_{IF1}t} \tag{5.3}$$

Where E_{r1} represents the normalized magnitude of the error signal and is much less than one. The mismatched quadrature LO_2 signals can also be decomposed into ideal LO signals (LO_{2d}) and error LO signals (LO_{2er}):

$$e^{-j\omega_{LO2}t} + E_{r2}e^{j\omega_{LO2}t} \tag{5.4}$$

Where the normalized magnitude of the error signal, E_{r2}, is much less than one. The resulting signal after double-quadrature mixing can be represented as follows.

$$\begin{aligned} &IF_{1d}LO_{2d} + IF_{1d}LO_{2er} + IF_{1er}LO_{2d} + IF_{1er}LO_{2er} \\ &= e^{j\omega_{IF2}t} + E_{r2}e^{j(2\omega_{IF1}-\omega_{IF2})t} + E_{r1}e^{-j(2\omega_{IF1}-\omega_{IF2})t} + E_{r1}E_{r2}e^{-j\omega_{IF2}t} \end{aligned} \tag{5.5}$$

The second and third terms can be filtered out directly by the low-pass function in the IF port of the mixer. As shown in Fig. 5-3, the polyphase filter [6] of the double quadrature Hartley system can filter out the last term in equation (5.5). Similarly, the resulting signal for the secondary image signal after mixing can be represented as follows:

$$e^{-j\omega_{IF2}t} + E_{r2}e^{j(2\omega_{LO2}-\omega_{IF2})t} + E_{r1}e^{-j(2\omega_{LO2}-\omega_{IF2})t} + E_{r1}E_{r2}e^{j\omega_{IF2}t} \tag{5.6}$$

As a result, the image rejection ratio is finite when mismatches occur. According to (5.6), the fourth term ($E_{r1}E_{r2}e^{j\omega_{IF2}t}$) with the same frequency rotational sequence of the down-converted desired signal is a second-order error term. The second-order error inherent in the double quadrature system is much better than the first-order error in the single quadrature system. The double quadrature Hartley system has better immunity to the signal mismatches and is thus chosen for the second stage mixer in this work.

Certainly, the double quadrature multiplier can also be employed as the first stage mixer of the Weaver-Hartley system. However, the higher image rejection ratio is achieved at the cost of higher noise figure because a polyphase filter is employed to obtain quadrature RF signal [6]. The other reason of using the single quadrature Weaver system instead of using double quadrature Weaver architecture in Fig. 5-1 is to reduce the complexity. The band selection function is more complicated and requires switches in both RF and LO paths are needed. Moreover, there is another advantage in such a dual conversion image rejection system. Because the frequency of the first image signal is far away from that of the RF desire signal, all the building block within the receiver chain such as the antenna, filters, and the low noise amplifier can attenuate the image signal to some degree. Thus, the first stage of this dual-band Weaver-Hartley down-converter is chosen to be a single quadrature Weaver system.

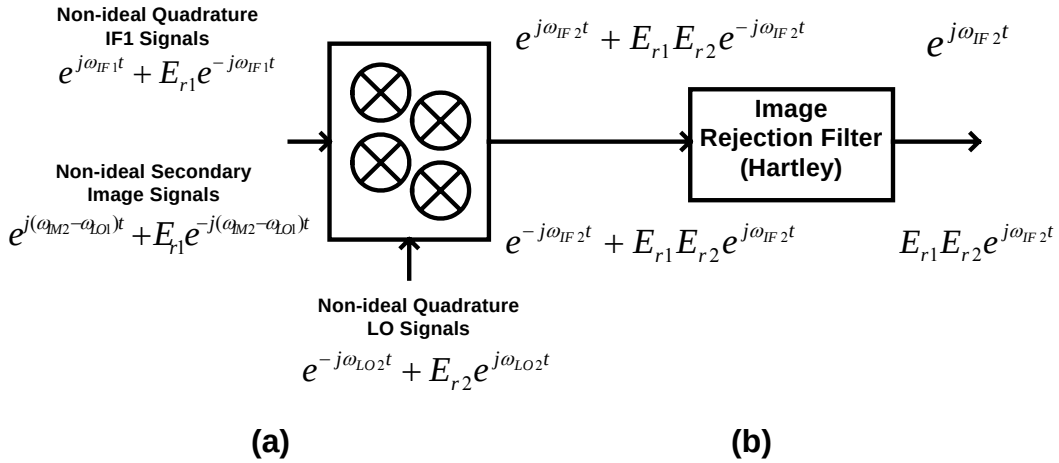


Fig. 5-3. The block diagram of a double-quadrature system with non-ideal input signals.

5.2 Spurious Response, Frequency Planning and the Band Selection

The desire signals are around 5.7-GHz and 2.4-GHz; therefore, the LO_1 signal for the Weaver system is set to be 4.05-GHz. In order to achieve the resulting IF_2 bandwidth within several tens MHz, a divide-by-2.5 divider for generating the LO_2 signal of 1.62-GHz from LO_1 signal is designed in our frequency planning. Coherent LO_1 and LO_2 signals are useful to maximize the image rejection ratio [81]. The divide-by-2.5 LO generator is based on a divide-by-five and a frequency doubler in our work.

The down-converted spurs have the frequencies of ($kf_{RF} \pm mf_{LO1} \pm nf_{LO2}$) [72]. If the LO_1 frequency is the integer multiples of the LO_2 frequency, the spurious response can easily fall into the final IF channels and degrade the performance of the image rejection receiver. On the other hand, the spurious components can hardly fall into the IF channels if the LO_1 frequency is the fractional multiples of the LO_2 frequency.

In this work, the divide-by-five and the frequency doubler are employed to provide a divide-by-2.5 divider. The spreadsheet enumerating method is employed to calculate the mixing terms of the RF, LO_1 and LO_2 signals with their fundamental, 2nd, 3rd, 4th, and 5th harmonics. There is no interfering signal caused by the spurious tone down-converted into the IF bandwidth except one mixing combination. The ($f_{RF}-3f_{LO1}+4f_{LO2}$) is the only down-converted spur. However, the spurious signal is very small because the even-harmonics are greatly suppressed in the double-balanced system.

The band selection at 5.7-GHz band is depicted in Fig. 5-4(a). The solid-line, dotted line, and the dash-line arrows are the RF signal, the IM_1 signal and the IM_2 signal. The RF signal as well as the undesired IM_1 and IM_2 signals is located at the positive spectrum, and down-converted by the $e^{-j\omega_{LO1}t}$ and $e^{-j\omega_{LO2}t}$ LO signals, respectively. As discussed above, the Weaver-Hartley architecture can reject both the first and the secondary image signals. On the other hand, when the desired signals are around 2.4-GHz, the signals located at the negative spectrum are down-converted by the $e^{j\omega_{LO1}t}$ and $e^{-j\omega_{LO2}t}$ LO signals, as shown in Fig. 5-4(b).

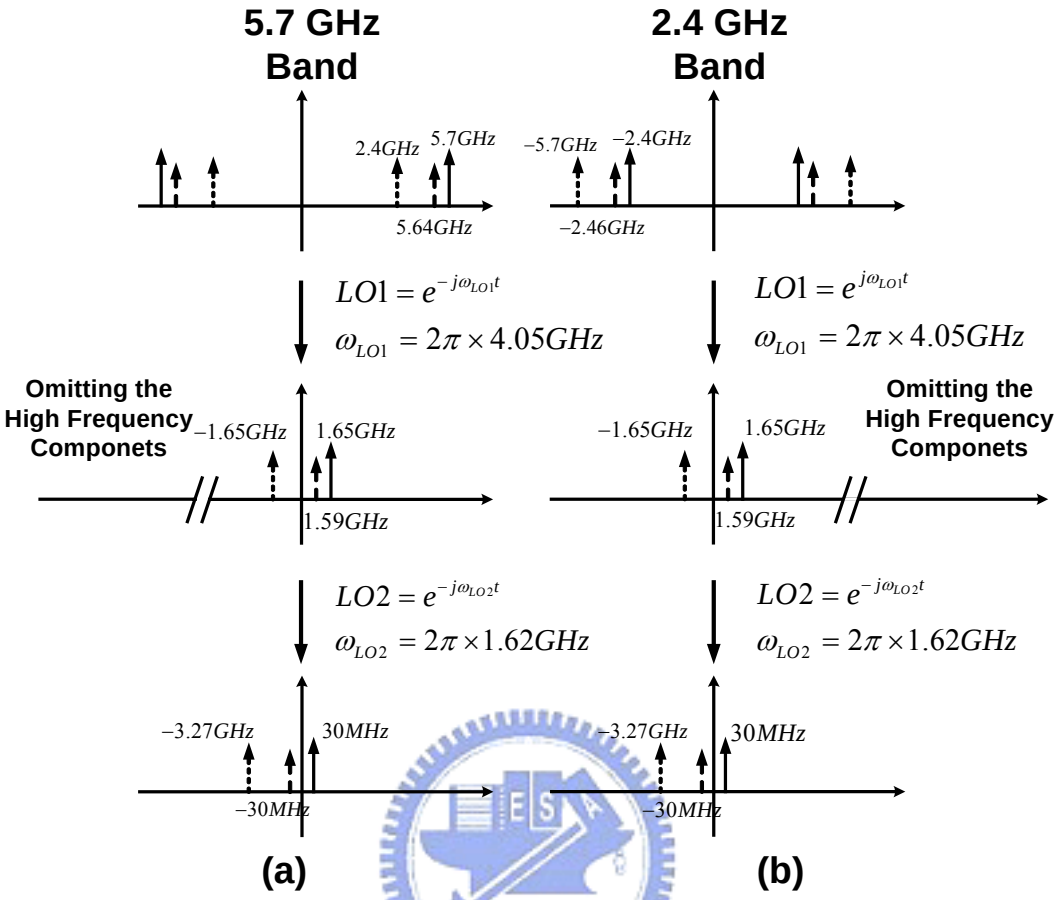


Fig. 5-4. All the high frequency harmonics are neglected. (a) The frequency shifting by the negative LO1 and negative LO2 complex signals when the RF frequency is around 5.7-GHz band; and (b) the frequency shifting by the positive LO1 and negative LO2 complex signals when the RF frequency is around 2.4-GHz band.

In the Weaver-Hartley system shown in Fig. 5-1, the band selection is achieved by intentionally changing the sequence of the complex LO_1 signals. The positive LO_1 sequence corresponds to $e^{j\omega_{LO1}t}$ while the negative LO_1 sequence corresponds to $e^{-j\omega_{LO1}t}$. The sequence of the complex LO_1 signal can be alternated using MOS switches. The MOS switching circuits are discussed in the next section.

It is worthwhile to mention that there are other types of hybrid dual-conversion systems. A complete analysis of different types of the dual-conversion image rejection systems is introduced in Chapter 7. The pros and cons of four distinct dual-conversion systems are discussed in Chapter 7 in detail.

5.3 2.4/5.7 GHz Dual Band Down-Converter Using 0.18 um CMOS Technology

The block diagram of the demonstrated Weaver-Hartley down-converter is shown in Fig. 5-5. The first-stage and second-stage complex mixers contain two and four Gilbert multipliers, respectively. The 4.05-GHz LO_1 signal is fed externally and the 1.62-GHz LO_2 signal is generated from the LO_1 signal using the divide-by-five circuit and the frequency doubler. The quadrature generators shown in Fig. 5-5 are two-section polyphase filters to generate differential-quadrature signals from differential signals. A four-section polyphase filter and an IF buffer amplifier are located at the end of the down-converter. Each sub-circuit is discussed in the following sections.

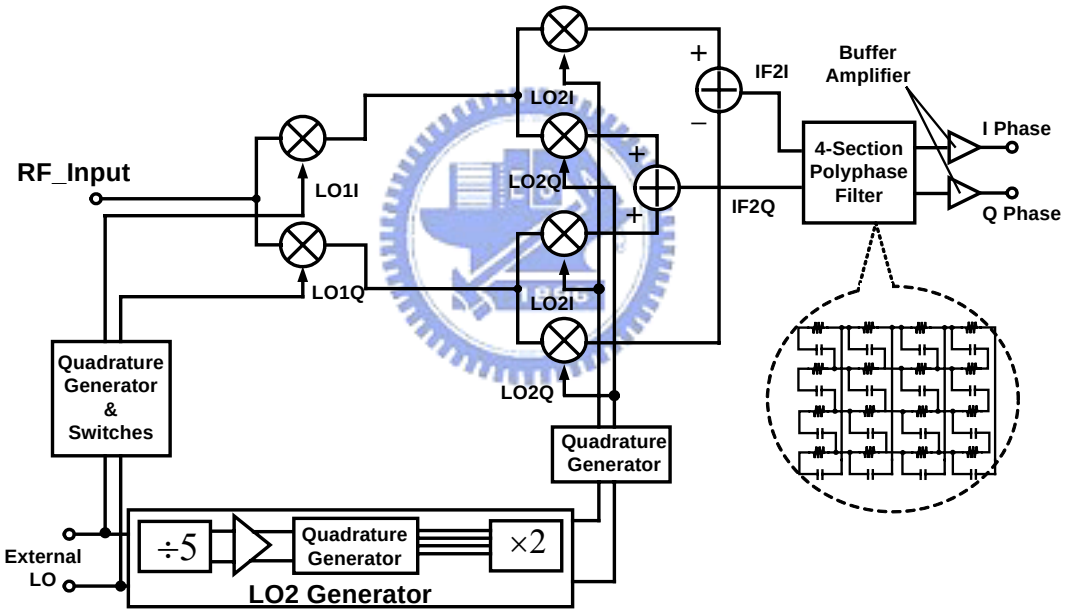


Fig. 5-5. A block diagram of the demonstrated Weaver-Hartley double-quadratrue down-converter using 0.18 um CMOS technology.

The mixers in the first and second stages are Gilbert mixers as shown in Fig. 5-6. The Gilbert active mixer has advantage in terms of higher conversion gain, smaller LO pumping power, and better port-to-port isolation when compared with passive mixers. The first-stage mixer is also a Gilbert micromixer and has the advantage of broadband matching characteristics [29], [81]. Thus, this topology is suitable for the dual band application. The second-stage mixer is a conventional Gilbert mixer employing a differential pair as the input stage. Source degenerated resistors are

employed to increase the IP_{1dB} of the second-stage Gilbert mixer.

The addition and the subtraction for the complex mixing can be achieved by the current mode operation [81]. Connecting the output currents of the mixers in the in-phase way performs the function of addition while the subtraction can be accomplished by connecting the output currents of the mixers in the anti-phase way.

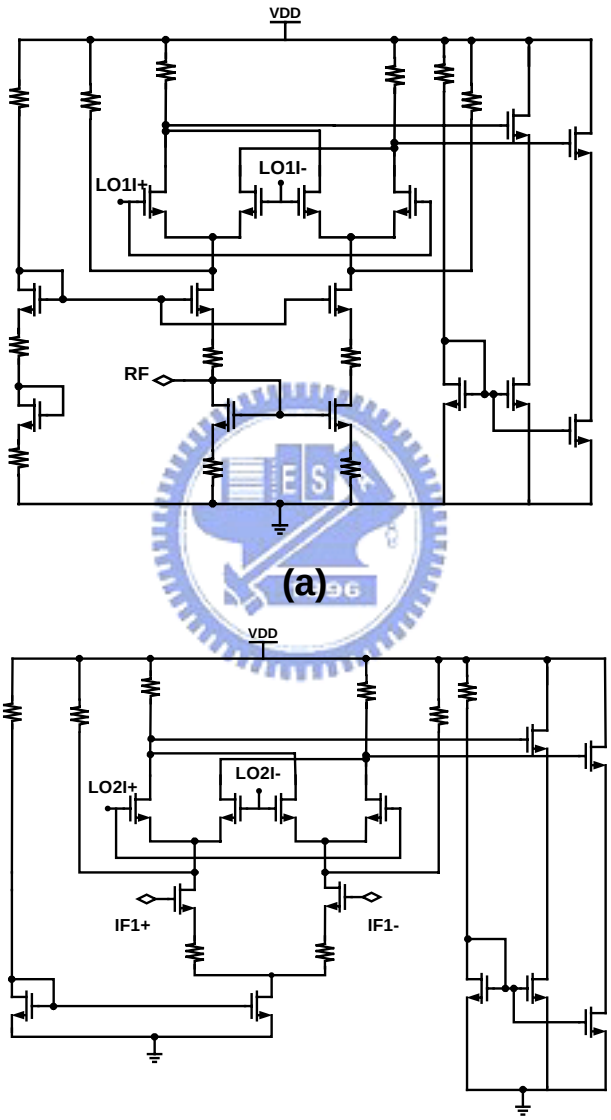


Fig. 5-6. The schematic of the Gilbert mixers used for the (a) first-stage and (b) second-stage mixers.

The image rejection depends on the magnitude and phase accuracies of the LO and RF signals [6], [70], [71], [81]. The imperfect LO and RF signals are inevitable in the circuit fabrication and thus the image rejection ratio degrades. Many methods such

as off-chip or electronic tuning are developed to increase the image rejection performance [70], [71]. The coherence between LO_1 and LO_2 signals improves the image rejection [81]. In order to achieve coherent LO signals, an accurate LO generator consisting of the 50% duty cycle divide-by-five circuit and the truly balanced frequency doubler [43], [44], [76] is employed to generate coherent signals with less phase errors. As a result, the frequency of the LO_1 signal is 2.5 times of that of the LO_2 signal and thus only one VCO is needed.

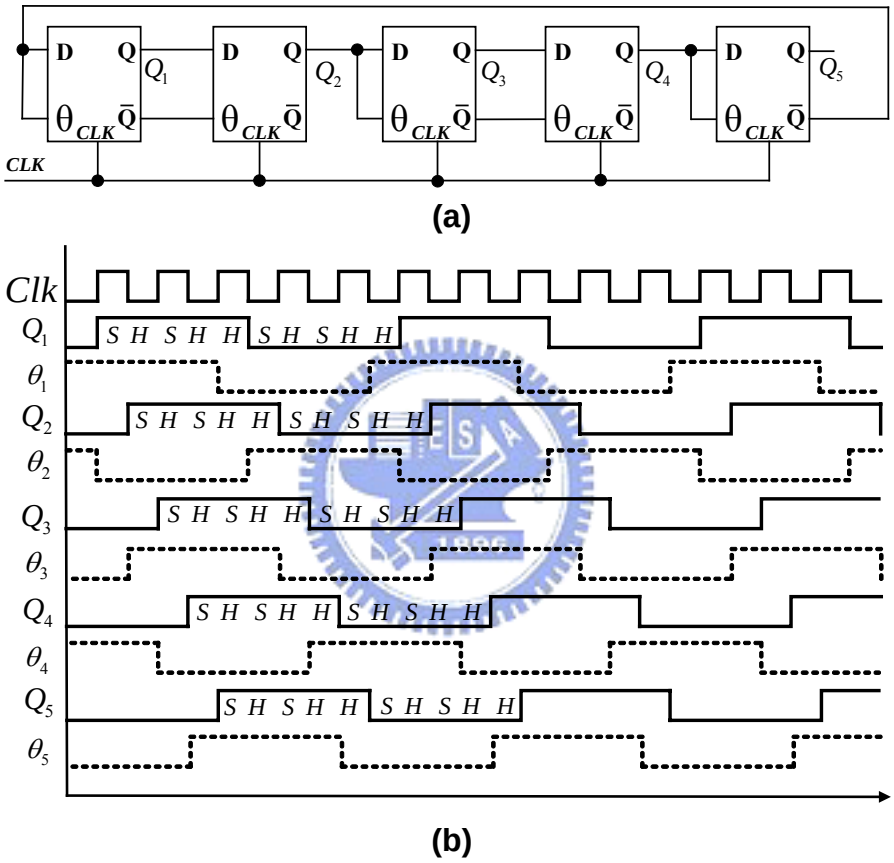
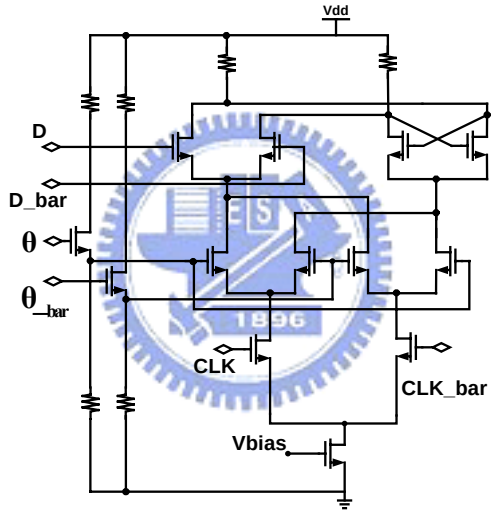


Fig. 5-7. (a)The block diagram of the 50% duty-cycle divided-by-five circuit and (b) the timing diagram.

As shown in Fig. 5-5, the LO generator consists of a divide-by-five circuit, a buffer amplifier, a quadrature generator and a frequency doubler. The block diagram of a 50% duty cycle divide-by-five circuit and its associate timing diagram is shown in Fig. 5-7(a) and Fig. 5-7(b), respectively. The 50% duty cycle is critical for the Weaver-Hartley image rejection system because the image rejection degrades if the LO signals are none 50% duty cycle. The divide-by-five circuit consists of five current switchable source-coupled logic D flip-flops [88]-[90] and employs the

sample-hold-sample-hold-hold scheme to achieve the 50% duty cycle. The schematic of the current switchable source couple logic D flip-flop [88] is shown in Fig. 5-8. Two extra differential pairs with control inputs θ and θ_bar are inserted into the conventional D flip-flop, and this current switchable D flip-flop can be triggered at both the positive edge and the negative edge.

A truly balanced frequency doubling multiplier consisting of two Gilbert multipliers as shown in Fig. 5-9 is employed to compensate the phase delay between the top and bottom signal paths in a Gilbert multiplier [43], [44]. The two-section polyphase filter in Fig. 5-9 generates quadrature signals needed by the truly balanced frequency doubler.



(a)

D	θ	CLK	Q
0	0	0	0
0	0	1	Hold
0	1	0	Hold
0	1	1	0
1	0	0	1
1	0	1	Hold
1	1	0	Hold
1	1	1	1

(b)

Fig. 5-8. (a) The schematic of the source couple logic D flip-flops, and (b) the true table.

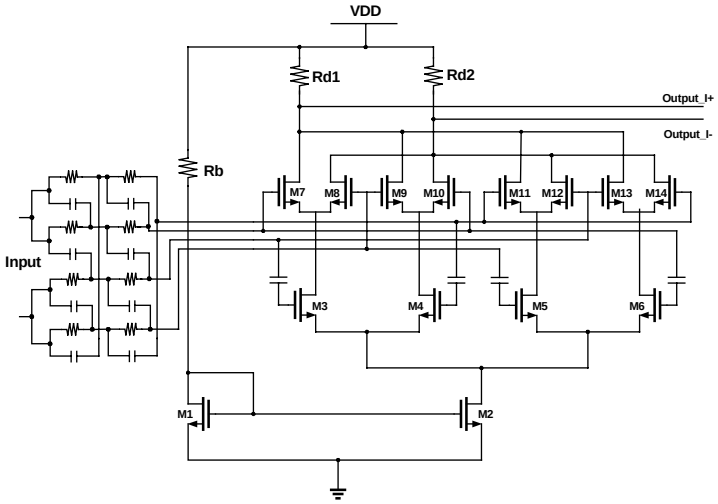


Fig. 5-9. The truly balanced multiplier.

The 2.4/5.7-GHz band selections are achieved by changing the polarity of the LO_1 signals. Figure 10 shows the band-selection switching circuits. When S1 is low and S2 is high, the 5.7-GHz band is selected. The LO_1 signals are in the clockwise sequence of I+, Q-, I-, and Q+ and can be represented by $e^{-j\omega_{LO1}t}$. On the other hand, the 2.4-GHz band is chosen when S1 is high and S2 is low. The LO_1 signals are in the counterclockwise sequence of I+, Q+, I-, and Q- and thus can be represented by $e^{j\omega_{LO1}t}$. The buffer B is a common drain output buffer to drive the LO ports of the mixers.

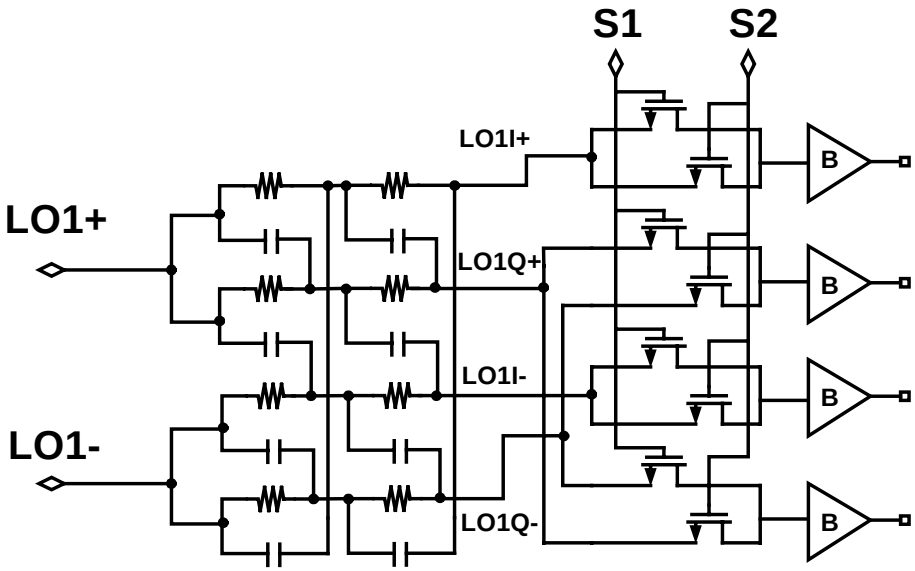


Fig. 5-10. The LO_1 signal polarization switching circuit used to perform the band selection.

The secondary image rejection of the Weaver-Hartley system relies on the polyphase filter. In order to obtain 45 dB image rejection ratio and 12-48 MHz bandwidth, a four-section polyphase filter is incorporated at the end of the down-converter as shown in Fig. 5-5. The polyphase filter is followed by buffer amplifiers to compensate the loss of the polyphase filter and to drive the spectrum analyzer for the on-wafer measurement.

The die photo of the Weaver-Hartley down-converter is shown in Fig. 5-11 and the die size is 2 X 2 mm^2. The RF, IF, LO GSGSG and six pins DC pads are located at the top, right, left and bottom of the die in sequence. The layout is very compact and many chocking capacitors are used to make sure the effectiveness of the DC supply in addition to the area occupied by the dummy metal cells. The supply voltage is 1.8 V and the total currents of the six mixers are 30 mA. The LO generator and the output buffers consume 40 mA.

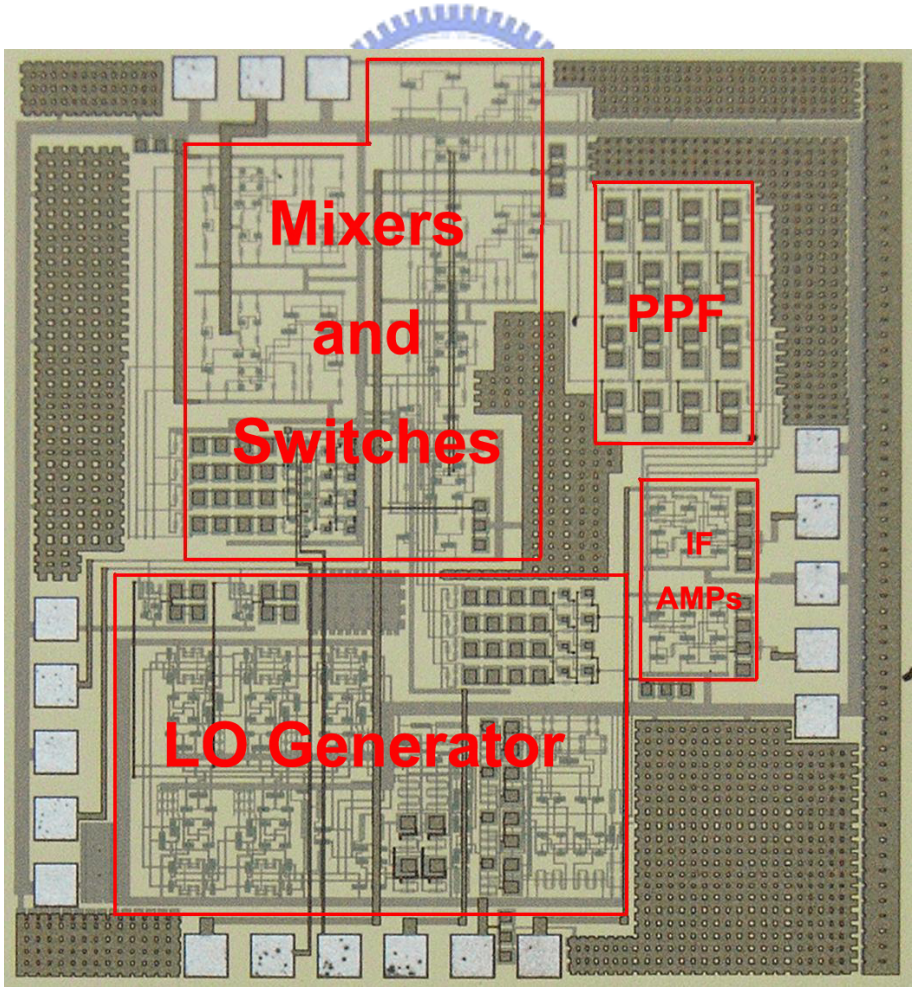


Fig. 5-11. The die photo of the Weaver-Hartley down-converter using 0.18 um CMOS technology.

Figure 5-12 shows the conversion gain as a function of the LO power for the 2.4-GHz band. The conversion gain reaches 9 dB when the LO power is larger than 5 dBm. On the other hand, the peak conversion is 8 dB when the RF frequency is 5.7-GHz and LO power is larger than 7 dBm. The simulated conversion gain is 20 and 18 dB for the 2.4 and 5.7-GHz, respectively. The gain degradation can be caused by the loss of the silicon substrate and the layout parasitic. The layout should be more carefully in order to retain the gain or using the LC tuned load to increase the gain.

When the RF frequency is 5.7-GHz, the demonstrated down-converter has the IP_{1dB} of −13 dBm and IIP_3 of 2 dBm, as shown in Fig. 5-13. When the RF frequency is 2.4-GHz, the IP_{1dB} and the IIP_3 are −11 dBm and 3 dBm, respectively.

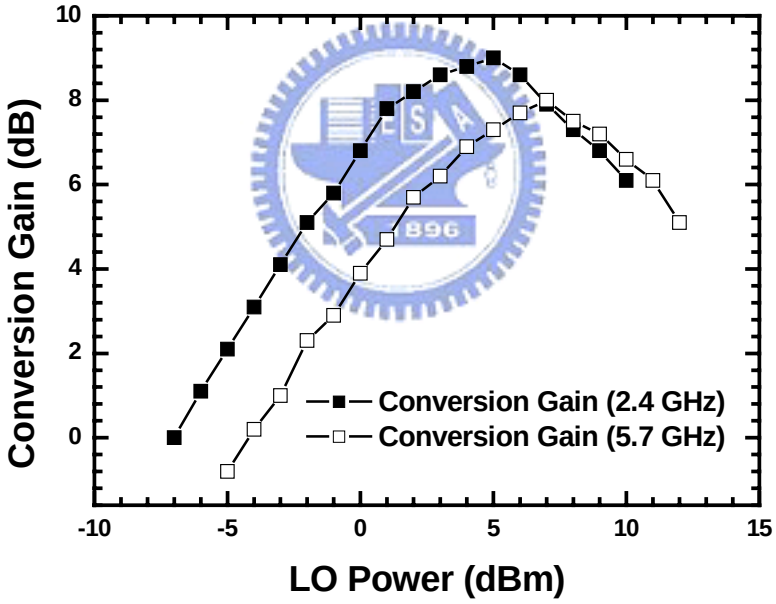


Fig. 5-12. The conversion gain as a function of LO power of the demonstrated Weaver-Hartley down-converter.

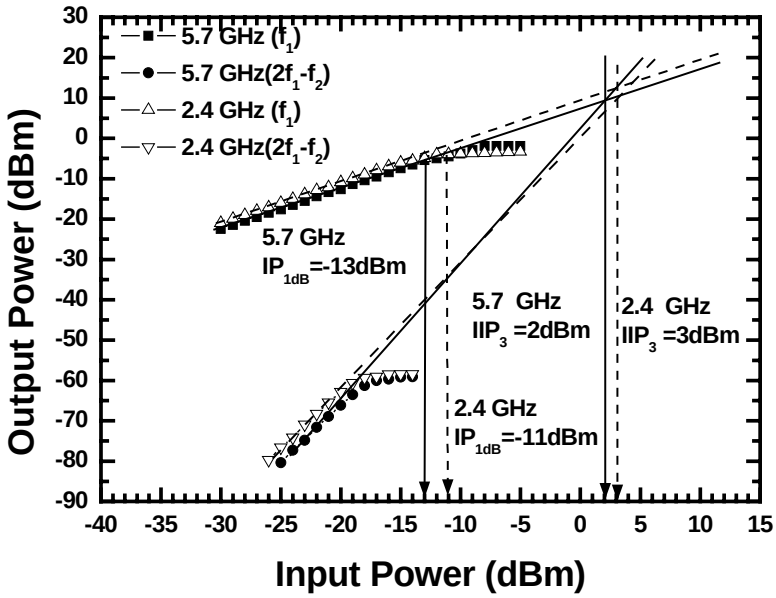


Fig. 5-13. The power performances of the demonstrated Weaver-Hartley down-converter.

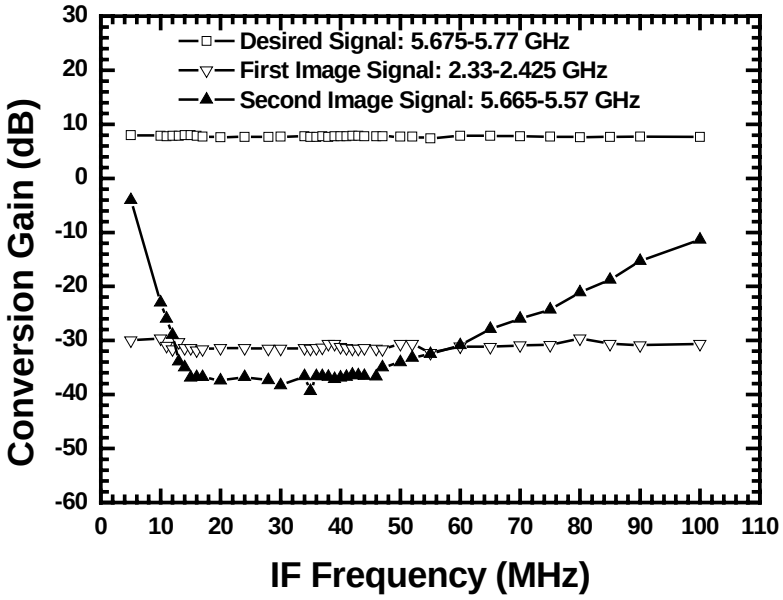
Figure 5-14 shows the conversion gain as a function of RF frequencies. The LO_1 frequency is fixed at 4.05-GHz and thus LO_2 equals to 1.62-GHz. The RF frequency is swept to obtain the gain difference between desired and image signals. The resulting IF frequencies are employed to represent the RF and image frequencies by properly folding the RF and image frequencies into the IF axis.

When the desired RF signal is around 5.7 GHz, the frequencies of the desired IF signal, the IF signals caused by first image signal, and the second image signal can be calculated by:

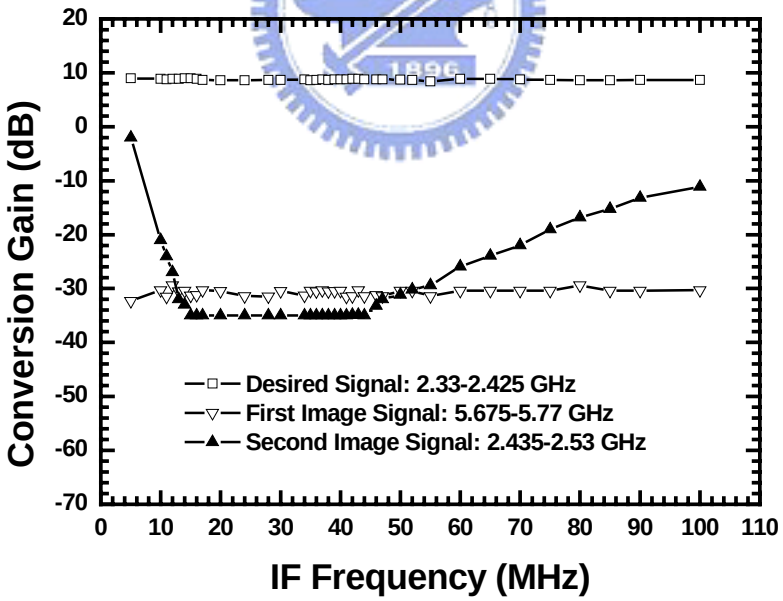
$$IF_{desired} = RF - LO_1 - LO_2 \tag{5.7a}$$

$$IF_{IM1} = LO_1 - IM_1 - LO_2 \tag{5.7b}$$

$$IF_{IM2} = LO_1 + LO_2 - IM_2 \tag{5.7c}$$



(a)



(b)

Fig. 5-14. The conversion gain as a function of RF and image frequencies of the demonstrated Weaver-Hartley dual-band low-IF down-converter. IF frequencies are employed to represent the RF and image frequencies by properly folding the RF and image frequencies into the IF axis (a) RF near 5.7 GHz. (b) RF near 2.4 GHz.

On the other hand, when the desired RF signal is around 2.4 GHz, the frequencies of the desired IF signal, the IF signal caused by first image signal, and the second image signal can be calculated by:

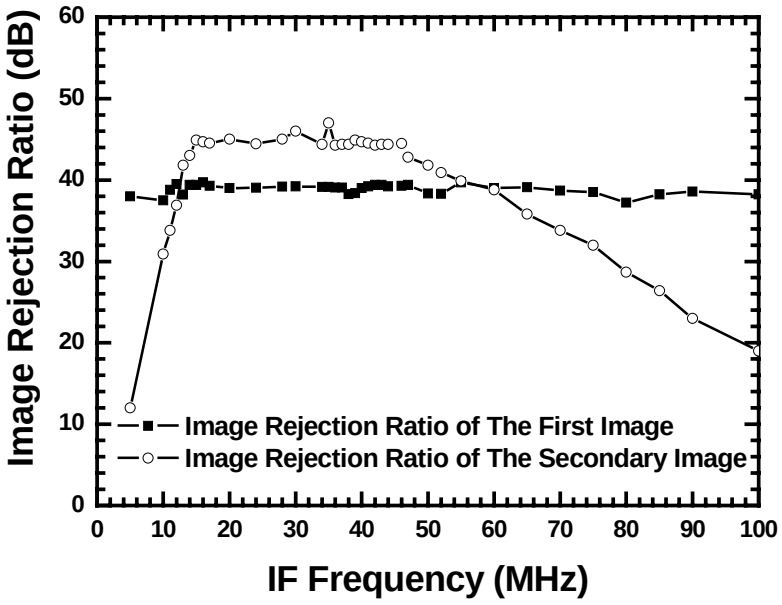
$$IF_{desired} = LO_1 - RF - LO_2 \tag{5.8a}$$

$$IF_{IM1} = IM_1 - LO_1 - LO_2 \tag{5.8b}$$

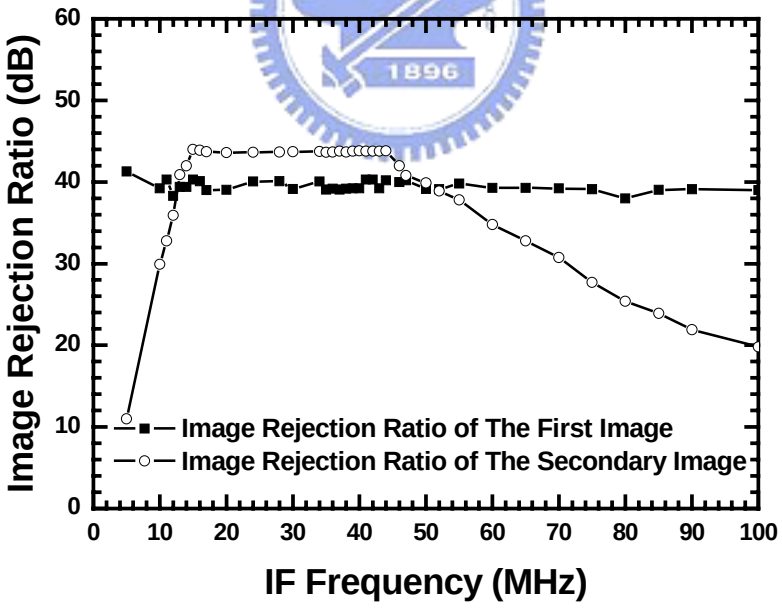
$$IF_{IM2} = IM_2 - LO_1 + LO_2 \tag{5.8c}$$

As shown in Fig. 5-14(a), the gain of the desired signal is 8 dB when the RF signal frequency is around 5.7-GHz. On the other hand, the first image signal near 2.4-GHz has conversion loss of 32 dB, and the conversion loss of the secondary image signal (5.46-GHz) is 38 dB. Similarly, the gain is 9 dB when the desired RF signal frequency is around 2.4-GHz. The first image signal near 5.7-GHz has conversion loss of 31 dB. The conversion loss of the secondary image signal (2.43-GHz) is 35 dB as shown in Fig. 5-14(b).

The image rejection ratios of both image signals for 2.4/5.7-GHz applications are plotted in Fig. 5-15 (a) and (b). When the RF frequency is 5.7-GHz, the image rejection ratios of the first and secondary image signals are about 40 dB and 45dB, respectively. The frequency response of the image rejection ratio of the secondary image signal is a band-pass shape in nature because of the complex filtering behavior of the polyphase filter. The IF bandwidth of the measured image rejection ratio of the secondary image signal starts from 12-MHz to 48-MHz. On the other hand, the image rejection ratio of the first image signal has a flat frequency response because the image rejection mechanism of the Weaver system comes from dual LO frequency shifting as discussed in Fig. 5-2. When the desire signals are around 2.4-GHz, the image rejection of the first and secondary images are 40 dB and 44 dB, respectively. The simulated first image rejection ratio is about 45 dB, and the secondary image rejection ratio is about 60 dB. The degradation of the image rejection ratio can be caused by the circuit mismatch. The measure input return loss, S_{11}, is better than –12 dB from 50 MHz to 6 GHz, shown in Fig. 5-16.



(a)



(b)

Fig. 5-15. The Image rejection ratio of the first image signal and the secondary image signal when (a) the desired signal is 5.7-GHz and (b) 2.4-GHz.

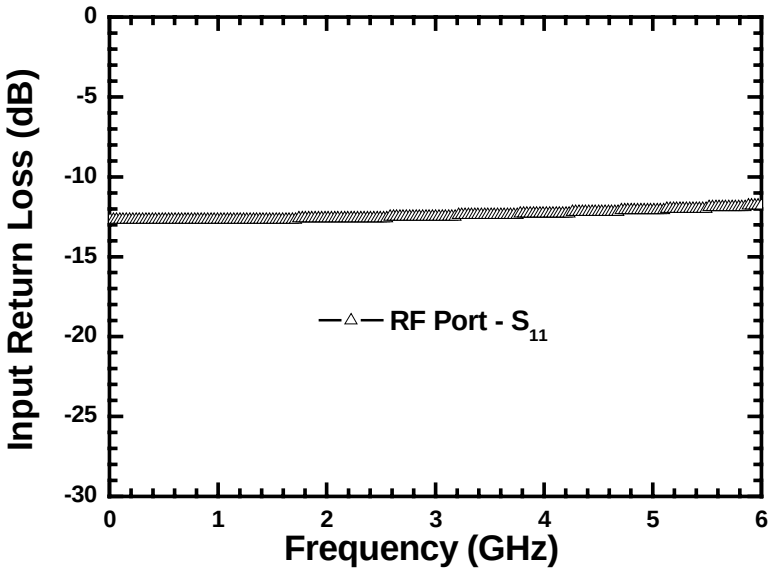


Fig. 5-16. The measured input return loss of the Weaver-Hartley down-converter.

Figure 5-17 shows the waveforms of the I and Q output ports. The measured result indicates that the output signals are quite balanced. It is worthwhile to mention that the high image rejection ratio occurs when the signal paths are truly balanced [70], [81]. The in-phase and quadrature-phase waveforms also manifest that the demonstrated circuit is highly balanced including the signal phase and the signal magnitude.

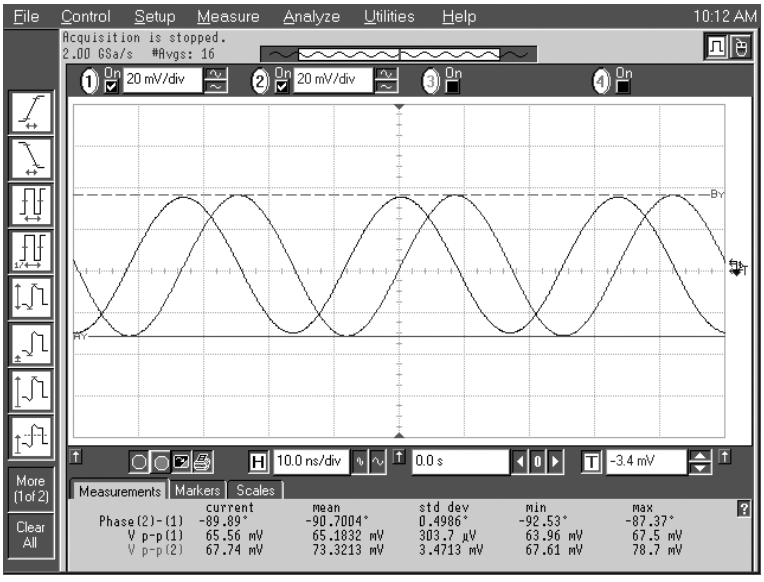


Fig. 5-17. The measured IQ waveform of the demonstrated Weaver-Hartley dual-band low-IF down-converter.

The measured RF-to-IF, LO-to-RF and LO-to-IF isolations are better than –59 dB, –64 dB and –62 dB, as shown in Fig. 5-18 and Fig. 5-19. The measured double sideband noise figure of down-converter is shown in Fig. 5-20. When the RF frequency is 2.4 and 5.7-GHz, the measured single sideband noise figure is better than 23 dB and 25 dB within the 12-MHz to 48-MHz IF bandwidth. The complexity of the down-converter and the polyphase filter degrades the system noise figure. However, the low noise amplifier preceding the Weaver-Hartley down-converter dominates the noise figure of the entire receiver chain. The performances are summarized in table 5-1.

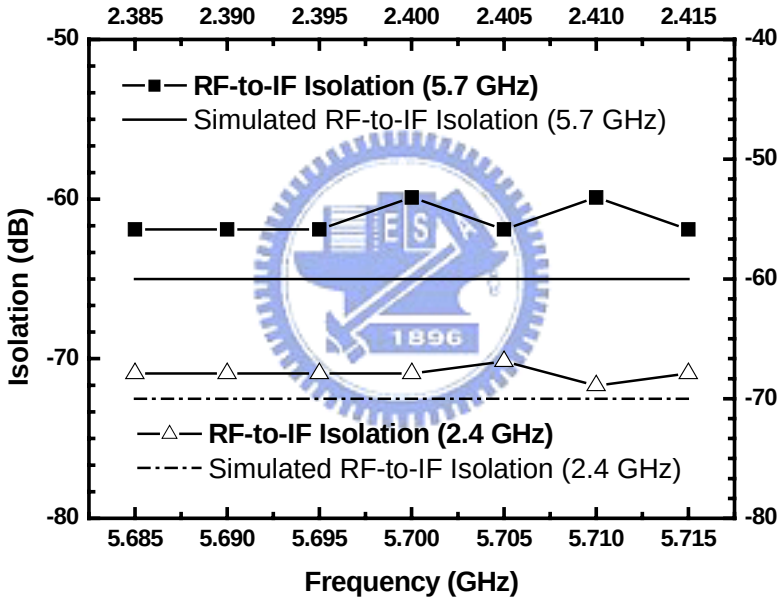


Fig. 5-18. The measured and simulated RF-to-IF isolation.

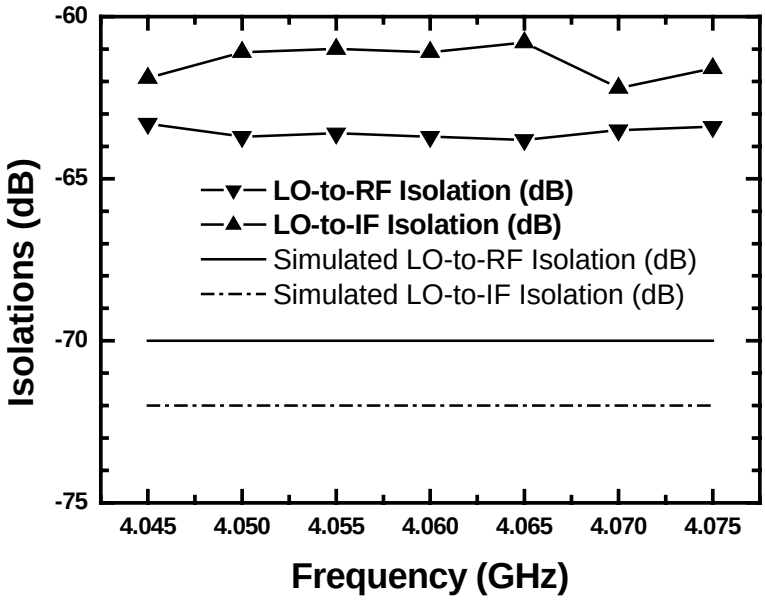


Fig. 5-19. The measured and simulated LO-to-RF, and LO-to-IF Isolations.

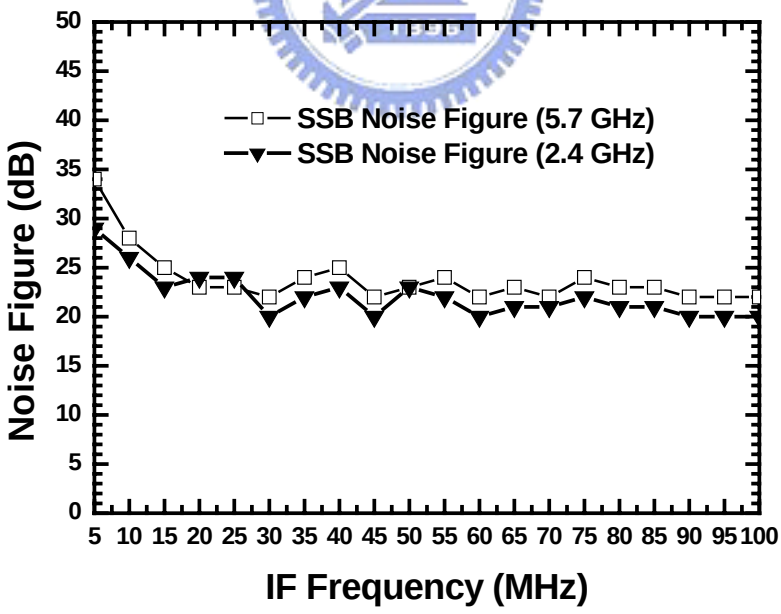


Fig. 5-20. The measured single sideband noise figure of the Weaver-Hartley dual-band low-IF down-converter.

Table 5-1: Summary of the Weaver-Hartley Down-Donverter Using 0.18 um CMOS Technology.

Item	2.4 GHz	5.7 GHz
IF Bandwidth (MHz)	12-48	12-48
Conversion Gain (dB)	9	8
Image Rejection Ratio of the First Image (dB)	40	40
Image Rejection Ratio of the Secondary Image (dB)	44	46
IP_{1dB} (dBm)	-11	-13
IIP_3 (dBm)	6	7
Input S_{11} (dB)	-12	-12
LO-to-RF Isolation (dB)	-64	-64
LO-to-IF Isolation (dB)	-62	-62
RF-to-IF Isolation (dB)	-68	-60
Double Sideband Noise Figure (dB)	23	25

Table 5-2 fairly compares some remarkable CMOS dual-band down-converters. Our solution is less complicated; however, the low-IF Weaver-Hartley system requires high speed AD. The measured noise figure is high due to the use of polyphase filter, and the LNA can be used to moderate the noise performance in our case.

Table 5-2: Comparison of the Dual-Band Down-Donverter Architectures

Item	Our Solution (CMOS)	[85]	[86]	[72]
Sets of RF Circuits	1	2	2	1
Sets of LO	1	2	2	2
1/f Noise	Free (Low-IF)	Serious (Direct-Conversion)	Serious (Direct-Conversion)	Serious (Direct-Conversion)
Band Attenuation	Weaver	LNA	LNA	Weaver
Bands (GHz)	2.4/5.7	2.4/5	2.4/5	0.9/1.8
A/D Converter Speed	High (60~70MHz)	Medium (50MHz)	Medium (50MHz)	Medium (50MHz)
Die Size (mm^2)	4	23*	12*	2
Power (mW)	70	370*	207*	75
Noise Figure (dB)	20	5.5**	5.6**	4.7**

* Including LNA, Transmitter, VCO, and Analog IF Circuits

** Including LNA

5.4 2.4/5.7 GHz Dual Band Down-Converter Using 0.35 um SiGe BiCMOS Technology

The block diagram of the demonstrated Weaver-Hartley down-converter using the 0.35 um SiGe BiCMOS technology is shown in Fig. 5-21. The system is quite similar to the 0.18 um CMOS version; however, the LO generator is completely different. The LO generator used here consists of a divied-by-2 circuit, a frequency doubler, and a single sideband mixer.

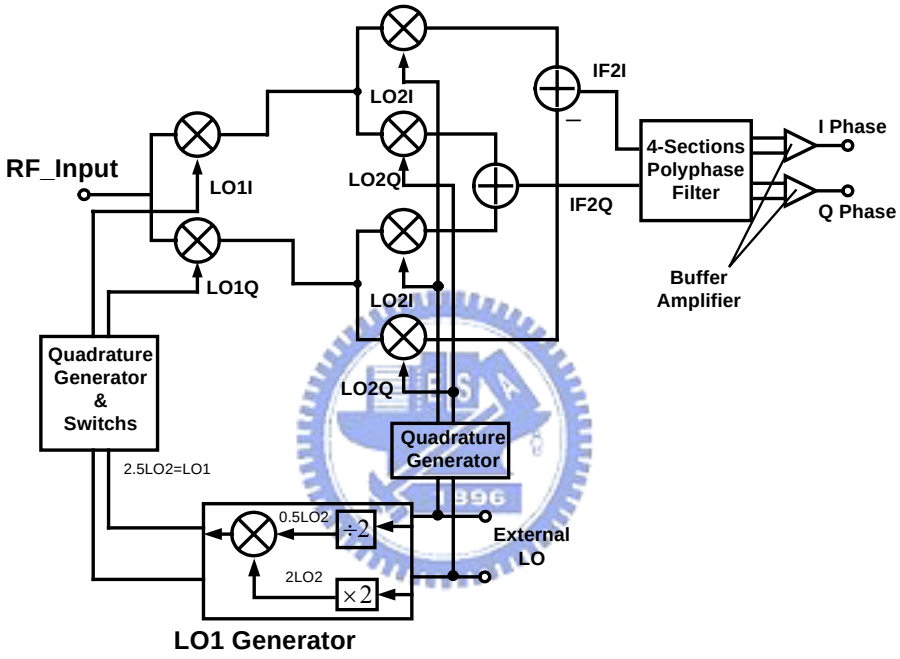


Fig. 5-21. A block diagram of the demonstrated Weaver-Hartley double-quadratrue down-converter using 0.35 um SiGe BiCMOS technology.

Figure 5-22(a) shows the block diagram of the divided-by-2 circuit, and the schematic of the D-latch is shown in Fig. 5-22(b). As shown in Fig. 5-22(b), the divided-by-2 circuit is a static divider. The frequency of the LO_2 signal is 1.62 GHz, and thus the static divider is suitable for this frequency range. Fig. 5-22(c) shows the frequency doubler. The frequency doubler is the truly phase balanced Gilbert multiplier. This highly symmetrical topology is useful to generate accurate signals. Figure 5-22(d) shows the single sideband mixer. In order to generate the required signal, the lower sideband mixing of the divided and multiplied signals is unallowable. As a result, the single sideband mixer is needed.

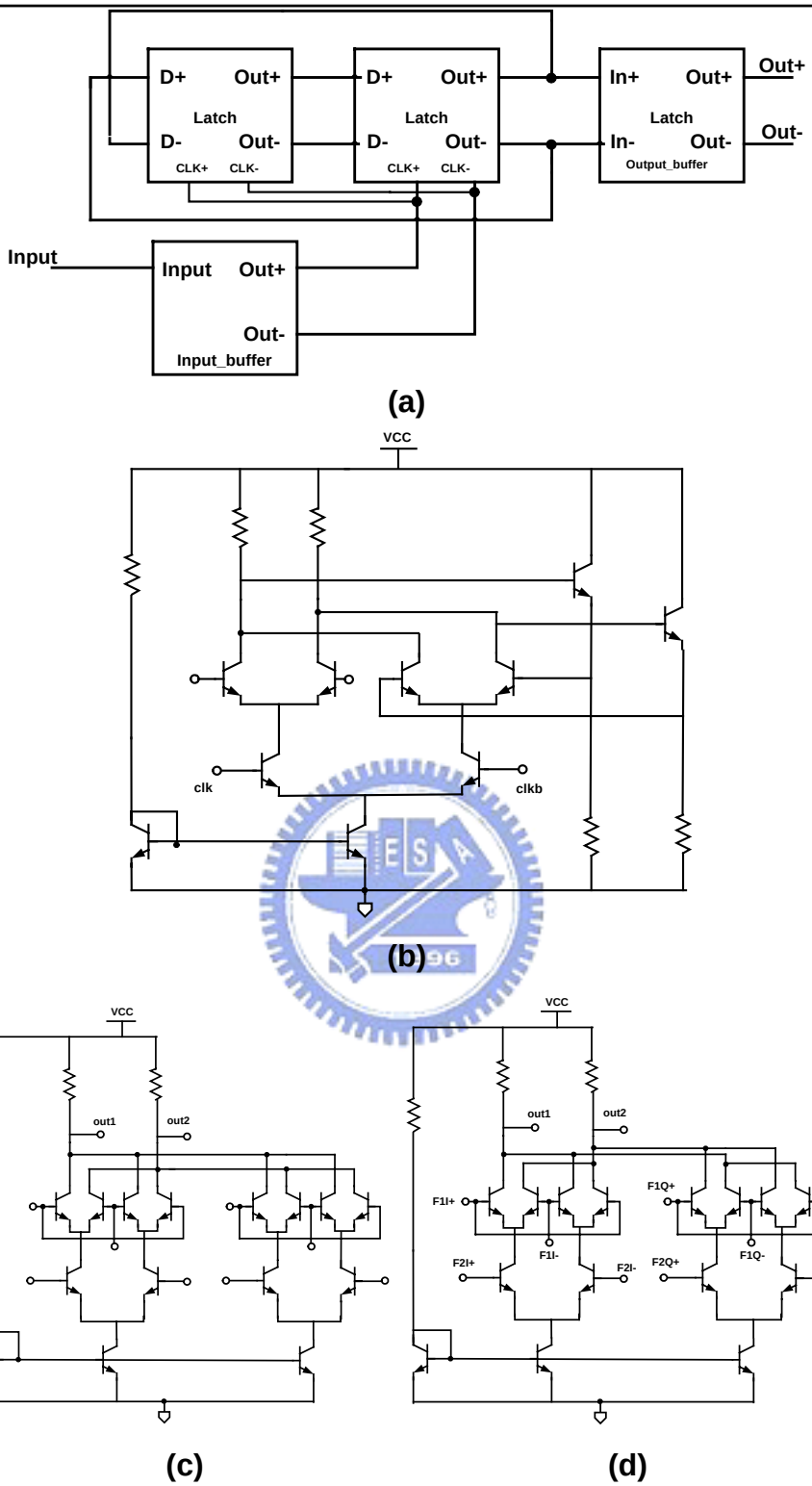


Fig. 5-22. (a) The block diagram of the divided-by-2 circuit of the LO generator, (b) the topology of the divided-by-2 circuit of the LO generator, (c) the circuit topology of the frequency doubler, and (d) the single sideband mixer.

The die photo of the Weaver-Hartley down-converter is shown in Fig. 5-23 and the die size is 1.6 x 1.5 mm^2. The RF, IF, and LO GSGSG pads are located at the right, top, left of the die in sequence. Many chocking capacitors are used to make sure the effectiveness of the DC supply. The supply voltage is 3.3 V and the total currents of the six mixers and the output buffers are 50 mA. The LO generator consumes 10 mA.

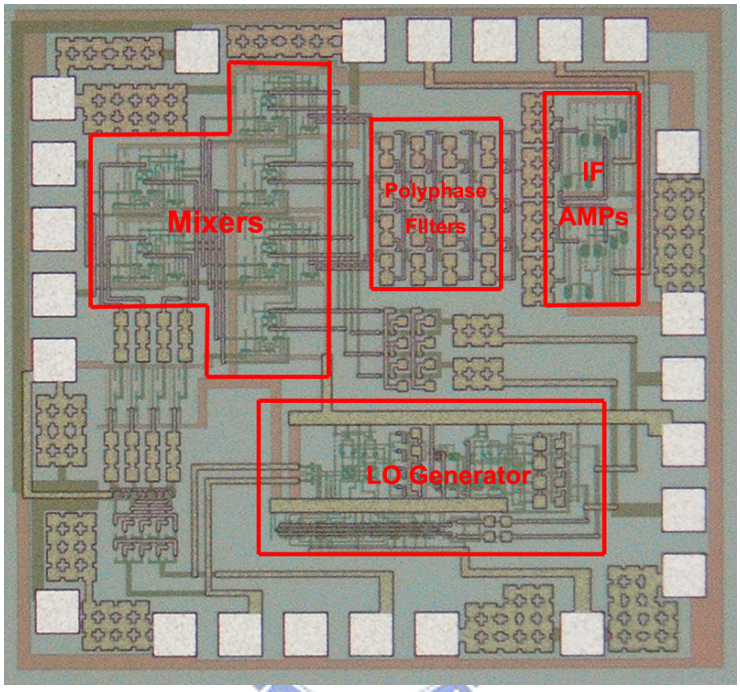
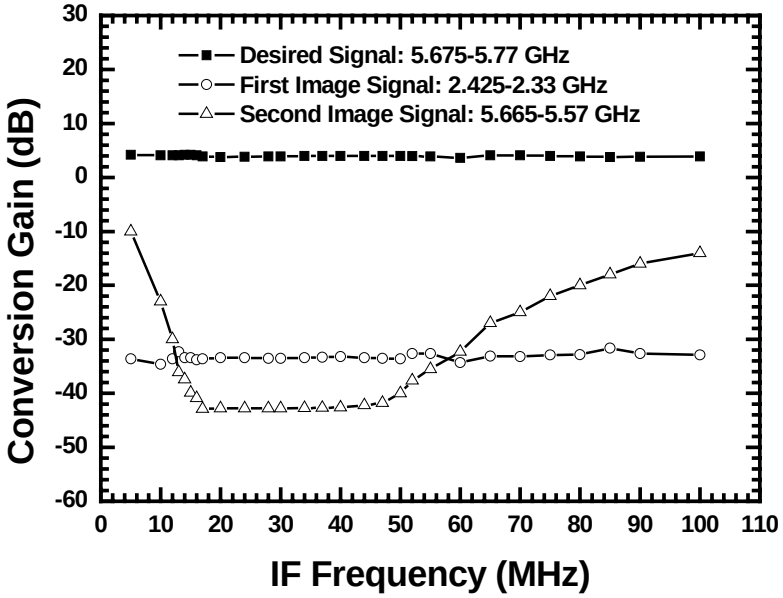


Fig. 5-23. Die photo of the demonstrated Weaver-Hartley double-quadratrue down-converter using 0.35 um SiGe BiCMOS technology.

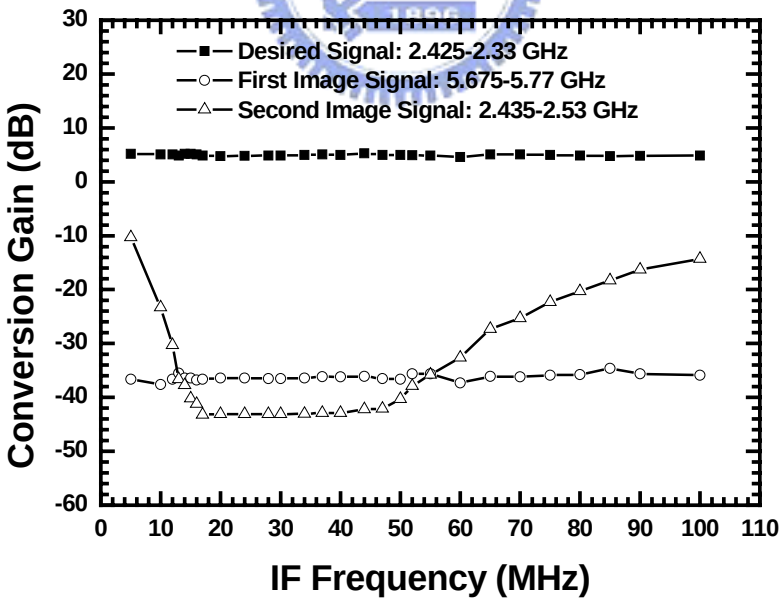
The demonstrated down-converter has conversion gain 6 dB and 5 dB for the 2.4 and 5.7 GHz bands, respectively. Figure 5-24 shows the conversion gain as a function of the RF frequencies. The LO frequency is fixed and the RF frequency is swept in order to obtain the gain difference between desired and image signals. For convenience, the axis of the RF frequencies are folded and represented by the IF frequencies. As shown in Fig. 5-24(a), the gain of the desired signal is 5 dB when the RF frequency is around 5.7 GHz. On the other hand, the image signal near 2.4 GHz has conversion loss of 33 dB, and the conversion loss of the secondary image signal (5.46 GHz) is 37 dB.

Similarly, the gain is 6 dB when the RF frequency is around 2.4 GHz. The image signal near 5.7 GHz has conversion loss of 36 dB. The conversion loss of the

secondary image signal (2.43 GHz) is about 44 dB.



(a)

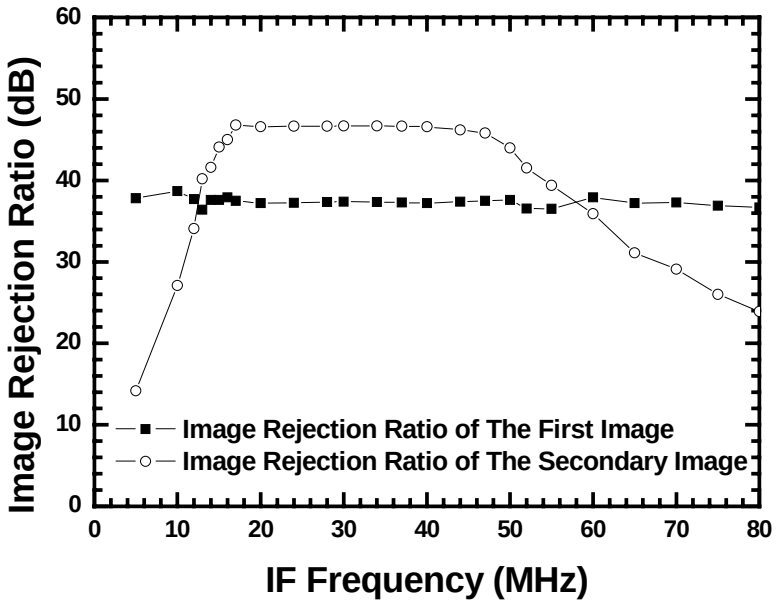


(b)

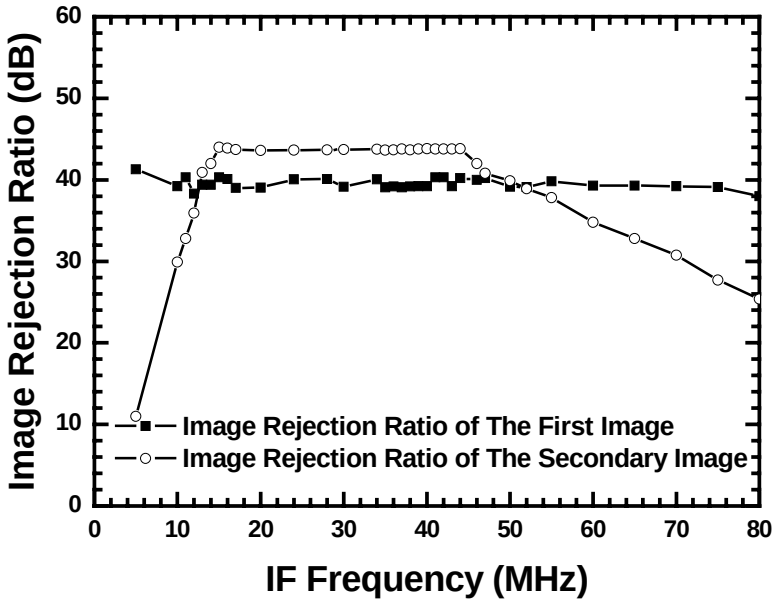
Fig. 5-24. The conversion gain as a function of RF frequencies of the demonstrated Weaver-Hartley down-converter using 0.35 um SiGe BiCMOS technology. (a) The desired RF frequencies locate from 5.675 GHz to 5.77 GHz. (b) The desired RF frequencies locate from 2.425 GHz to 2.33 GHz.

Figure 5-25 (a) and (b) plot the image rejection ratio of both image signals for 2.4/5.7 GHz applications. When the RF frequency is 5.7 GHz, the image rejection ratio of the first and secondary image signals are about 38 dB and 47 dB. The frequency response of the image rejection ratio of the secondary image signal is band-pass because the polyphase filter belongs to the band-pass filter. The bandwidth of the measured image rejection ratio of secondary image signal starts from 15 MHz to 46 MHz. On the other hand, the image rejection ratio of the first image signal has a flat frequency response because the image rejection of the Weaver system is a wideband response. When the desire signals are around 2.4 GHz, the image rejection of the first and secondary images are 40 dB and 44 dB.

The simulated first image rejection ratio is about 45 dB while the simulated secondary image signal rejection ratio is about 60 dB. Once again, the cause of degradation of the image rejection ratio is the circuit mismatch. The mismatch or the other imperfect effects are very important to the image rejection. According to the experiment, the designer should prepare the margin in advance since the degradation is inevitable.



(a)



(b)

Fig. 5-25. The Image rejection ratio of the first image signal and the secondary image signal when (a) the desired signal is 5.7 GHz and (b) 2.4 GHz.

The measure input return loss, S_{11}, is better than –6 dB from 2 GHz to 6 GHz, as shown in Fig. 5-26.

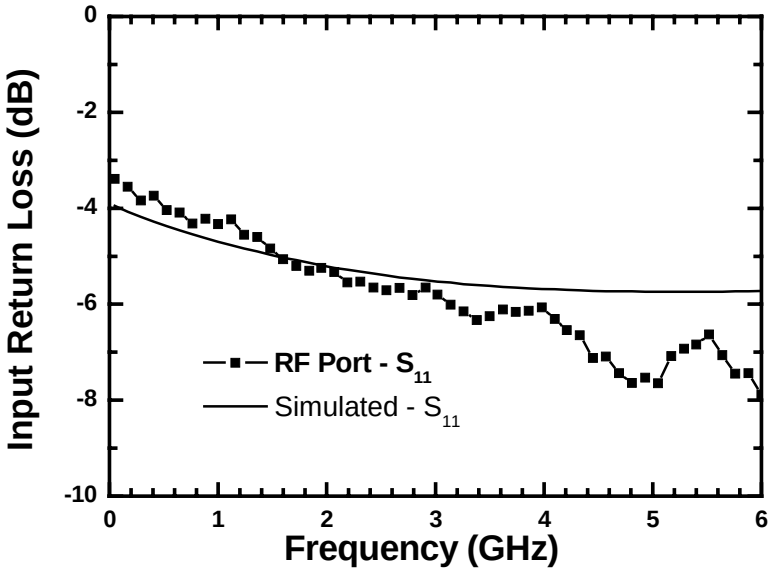


Fig. 5-26. The measured and simulated input return loss of the Weaver-Hartley down-converter.

Figure 5-27 shows the waveforms of the I and Q output ports. The I and Q waveform also manifests that the demonstrated circuit is highly balanced including the signal phase and the signal magnitude.

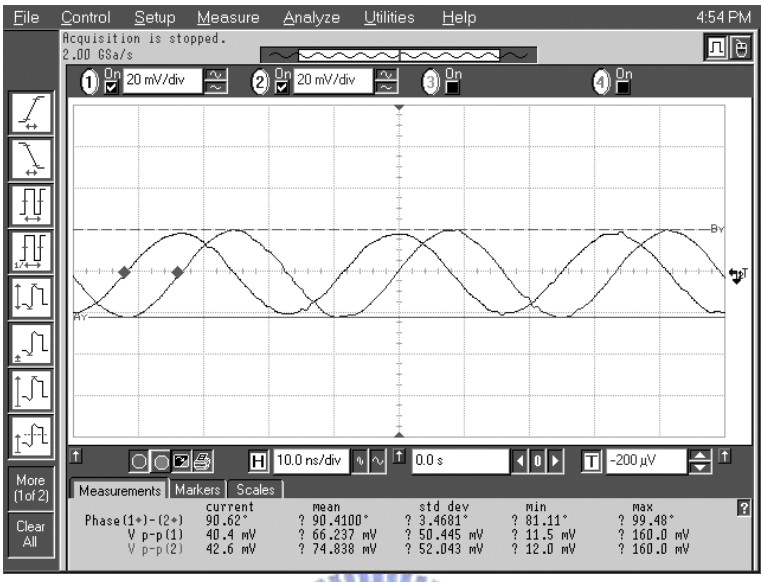


Fig. 5-27. The measured IQ waveform of the demonstrated Weaver-Hartley down-converter using 0.35 um SiGe BiCMOS technology.

The measured RF-to-IF, LO-to-RF and LO-to-IF isolations are better than –59 dB, –64 dB and –62 dB, as shown in Fig. 5-28 and Fig. 5-29.

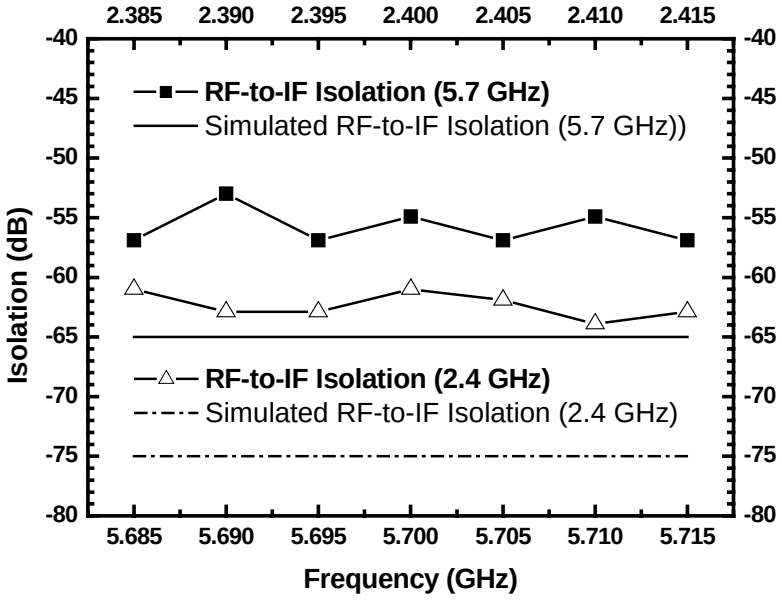


Fig. 5-28. The measured and simulated RF-to-IF isolation.

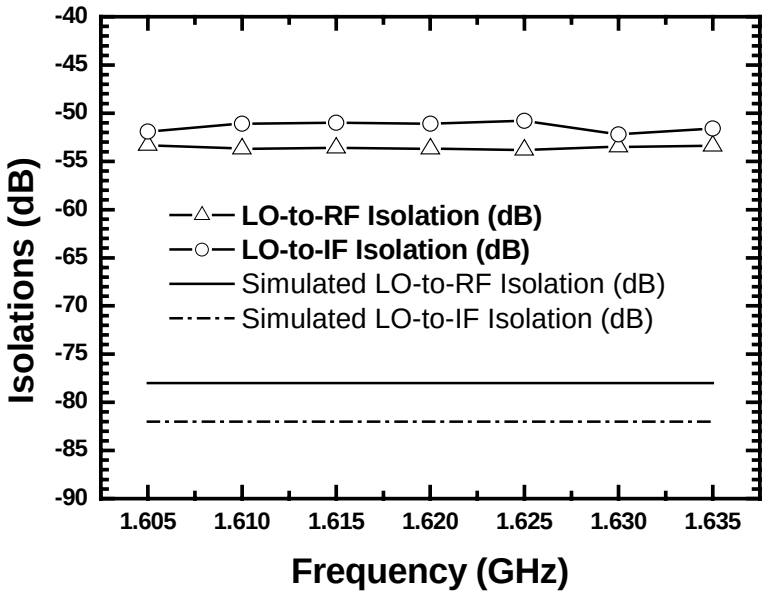


Fig. 5-29. The measured LO-to-RF, and LO-to-IF Isolations.

As shown in Fig. 5-30, the measured single sideband noise figure is better than 20 dB and 23 dB within the bandwidth when the RF frequency is 2.4 and 5.7 GHz.

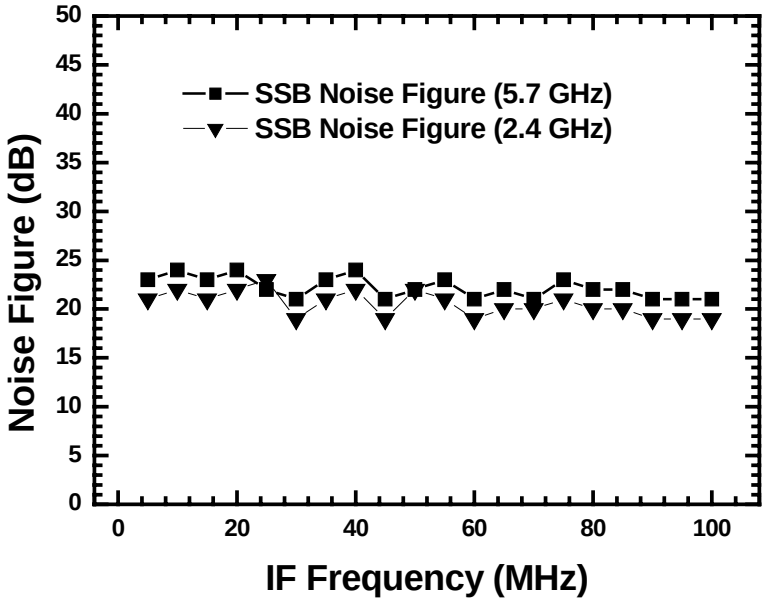


Fig. 5-30. The measured single sideband noise of the Weaver-Hartley down-converter.

When the applied RF frequency is 5.7 GHz, the demonstrated down-converter has the IP_{1dB} of –9 dBm and IIP_3 of 6 dBm, as shown in Fig 5-31. When the RF frequency is 2.4 GHz, the IP_{1dB} and the IIP_3 are –12 dBm and 3 dBm. The IP_{1dB} can be increased by adding the source degenerative resistors in our work. The circuit performances are summarized in table 5-3.

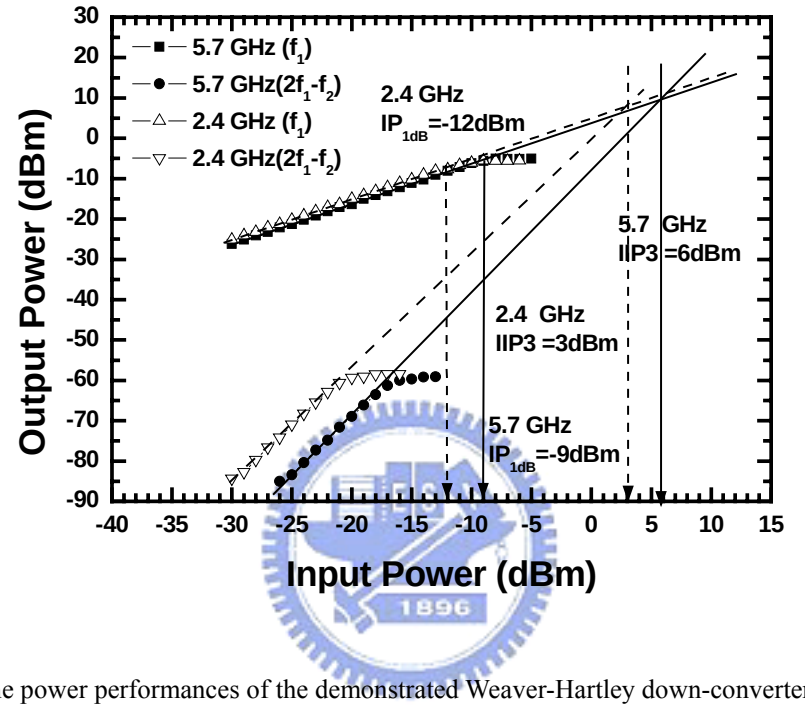


Fig. 5-31. The power performances of the demonstrated Weaver-Hartley down-converter.

Table 5-3: Summary of the Weaver-Hartley Down-Donverter Using 0.35 um SiGe HBT Technology.

Item	2.4 GHz	5.7 GHz
IF Bandwidth (MHz)	14-46	14-46
Gain (dB)	6	5
Image Rejection Ratio of the First Image (dB)	40	38
Image Rejection Ratio of the Secondary Image (dB)	44	47
IP_{1dB} (dBm)	-12	-9
IIP_3 (dBm)	3	6
Input S_{11} (dB)	-5	-6
LO-to-RF Isolation (dB)	-54	-54
LO-to-IF Isolation (dB)	-52	-52
RF-to-IF Isolation (dB)	-63	-57
Double Sideband Noise Figure (dB)	20	23

A novel image rejection low-IF topology of combing the Weaver and Hartley systems is demonstrated with the complex signal analysis in this work and dual-band down-converters are implemented using the proposed topology. The first part of the demonstrated down-converter is the Weaver system. The Weaver architecture can effectively eliminate the first image signal; however, the secondary image signal degrades the image rejection performance. The secondary image signal is rejected by the cascaded Hartley system in this work. Because the IF frequency is not zero, the frequency planning is much easier. As a result, the low-IF dual-band down-converter only requires one on-chip VCO and the down-conversion mixers are reused for both 2.4/5.7 GHz bands. Thus, the complexity is greatly reduced

Chapter 6

Analysis and Design of the Shunt-Series Series-Shunt Double Feedback Amplifier

The wideband amplifier is a general-purpose gain building block and the main requirement of a wideband amplifier is its gain and input/output matching bandwidth. It is worthwhile to mention that not only the gain bandwidth but also the matching bandwidth has to meet the system requirement to provide extra gain to any RF system. The P_{1dB} gain saturation point, the linearity performance, and the noise performance are also important criteria to judge whether a wideband amplifier is good or not. Upon so many wideband amplifier topologies, there are basically two most popular two-stage wideband amplifier configurations --- the Meyer topology [91]-[94] and the Kukielka topology [94]-[97].

The Kukielka topology is a Cherry-Hopper amplifier [98] with a global shunt-series feedback loop as shown in Fig. 6-1(a). The Cherry-Hopper amplifier basically consists of a TCA (Transconductance Amplifier) in the first stage and a TIA (Transimpedance Amplifier) in the second stage. The main advantage of the Cherry-Hopper amplifier is its high speed. The second-stage TIA is formed by a local shunt-shunt feedback loop. The input resistance of the second-stage amplifier is dramatically reduced and thus the output impedance of the first-stage amplifier (TCA) is also lowered. As a result, the speed of the first-stage amplifier can be improved because the low output resistance minimizes the Miller effect.

The Kukielka amplifier preserves the broadband characteristic of the Cherry-Hopper amplifier, and the global shunt-series feedback loop can further increase the bandwidth. The input and output matching is achieved simultaneously by the global shunt-series feedback loop and the local shunt-shunt feedback loop. The input resistance is lowered by the shunt-series feedback loop while the output counter part is reduced by the shunt-shunt feedback loop. Because of the high-speed and matched-impedance properties, the Kukielka wideband amplifier has been widely

used in wireless applications. The Kukielka wideband amplifier is also generally used in optical systems. Although a shunt-series feedback amplifier is a current amplifier, the output of the Kukielka amplifier can be the voltage signal. Therefore, the overall gain can be transimpedance gain and thus the Kukielka amplifier sometimes are employed for as TIAs [94].

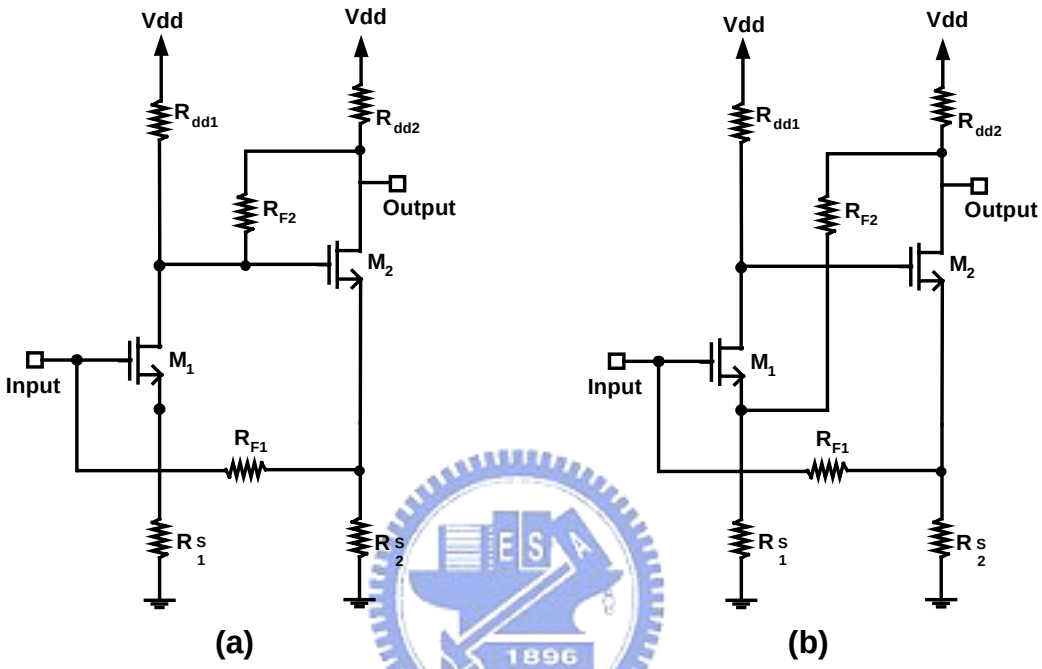


Fig. 6-1. (a) The circuit schematic of the Kukielka wideband amplifier (b) and the Meyer amplifier.

In this dissertation, the design equations of the Meyer wideband amplifier are determined. The Meyer topology is a two-stage amplifier with two global shunt-series and series-shunt feedback loops, and this schematic makes the Meyer configuration totally different from the Kukielka topology. However, The gain-bandwidth and the input/output matching bandwidth can be simultaneously achieved by two feedback loops as shown in Fig. 6-1(b). The performance of the Meyer topology is much uniform than that of the Kukielka configuration. Because there are two global feedback loops in the Meyer topology, the input and output common mode level as well as the bias currents are well defined. In other words, the DC bias points of the Meyer topology are tightly restricted. As a result, the Meyer amplifier has more advantages for mass production when compared with the Kukielka amplifier.

To realize the insights of the Meyer wideband amplifier, we use the pole and zero analysis [99] to find out all the design equations of the S-parameter. Our work

provides a consistent method to determine the frequency response of the gain and the terminal impedance matching when compared with previous works [91][92]. The method we proposed here is a general case solution. Previous works [91][92] have discussed the design equations of the Meyer amplifier using BJT technologies; however, the previous approach has limitations for the CMOS technologies caused by an invalid analytical approximation, as described in the following sections. To the best of our knowledge, the pole and zero analysis of the small signal S-parameters of the Meyer topology is established for the first time in this work. Section 6.1 to Section 6.3 present the detailed design parameters of the Meyer amplifier including gain, input, and output impedances, loop gain, poles and S-parameters. A Meyer amplifier based on the design principles is discussed in Section 6.4. Measurement results are shown in Section 6.6.

6.1 The DC Voltage Gain, the Input Resistance, and the Output Resistance of the Meyer Wideband Amplifier

The Meyer configuration consists of two feedback loops as shown in Fig. 1(b). One of the feedback loops is the shunt-series global feedback consisting of R_{F1} and R_{S2} between the first and second stage common source amplifiers. This feedback loop is a current-sampling shunt-mixing loop [100]; therefore, the feedback loop provides current-current feedback [101]. On the other hand, the global series-shunt feedback is a voltage-sampling series-mixing feedback loop [100] consisting of R_{F2} and R_{S1}, and it provides voltage-voltage feedback [101]. The shunt-series and series-shunt feedback loops are represented by $-\beta_I$ and $-\beta_V$, respectively.

It is a difficult task for the designers to find the A circuit and the β circuit of the dual feedback Meyer amplifier. Because the Meyer configuration contains two feedback loops, the A circuit and β circuits are too complicated to find. However, the Meyer wideband amplifier can be decomposed step by step as followed. Figure 6-2 shows the block diagram of the Meyer amplifier. As shown in Fig. 6-2, the Meyer amplifier can be treated as a voltage amplifier A_V with a voltage-voltage feedback loop β_V. Moreover, the A circuit of the Meyer amplifier actually is a current feedback amplifier. As long as the open loop current gain A_{I0} and the feedback loop β_I is found, the A_V can be determined by:

$$A_V = A_I \times \frac{R_2 // R_L}{R_1} = \frac{A_{I0}}{1 + A_{I0}\beta_I} \times \frac{R_2 // R_L}{R_1} \tag{6.1}$$

Therefore, the total closed-loop gain of the Meyer amplifier is:

$$A_{V\ total} = \frac{V_B}{V_A} = \frac{A_V}{1 + A_V \beta_V} \tag{6.2}$$

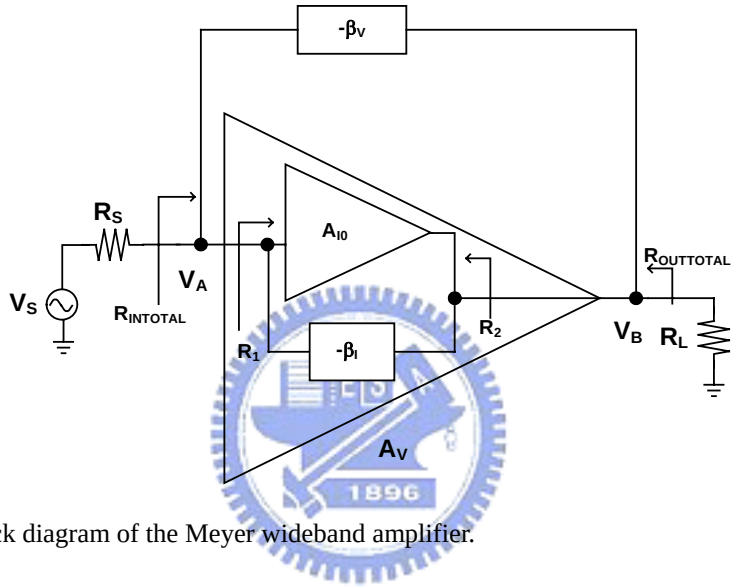


Fig. 6-2. The block diagram of the Meyer wideband amplifier.

Figure 6-3 shows the decomposition sequences of the Meyer amplifier. First, the Meyer topology shown in Fig. 6-1(b) can be decomposed into the circuit show in Fig. 6-3(a). Figure 6-3(a) contains a voltage amplifier and a voltage feedback loop β_V. It is interesting that the A circuit shown in Fig. 6-3(a) actually is a current amplifier with a shunt-series feedback loop. Hence, the A circuit shown in Fig. 6-3(a) can be further decomposed into a current amplifier with a feedback loop β_I as shown in Fig. 6-3(b).

First, the overall open loop voltage gain (V_B/V_A) of the Meyer topology can be described as (6.2). The A_V can be obtained by solving the closed-loop current gain A_I, the input resistance R_{IN}' and the output resistance R_{OUT}' including the loading effect [100] [101] of the wideband amplifier circuit as shown in Fig. 6-3(b). Therefore:

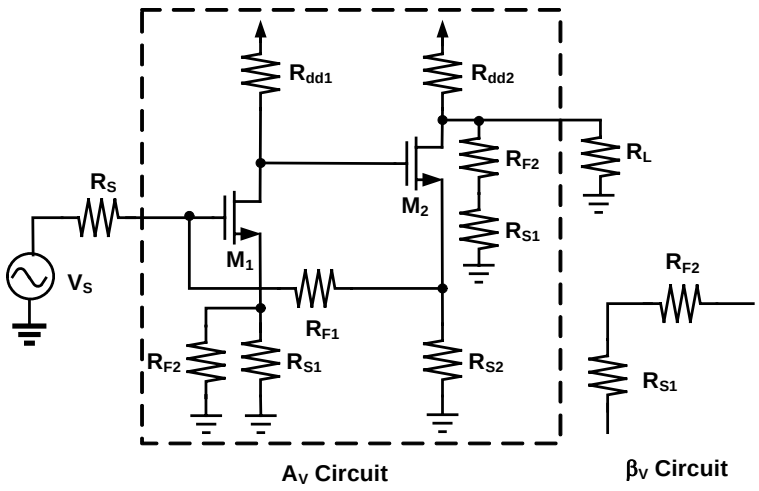
$$A_{V\ total} = \frac{A_I \times \frac{R_{OUT}\ '// R_L}{R_{IN}\ '}}{1 + A_I \times \frac{R_{OUT}\ '// R_L}{R_{IN}\ '} \times \beta_V} = \frac{\frac{A_{I0}}{1 + A_{I0}\beta_I} \times \frac{R_{OUT}\ '// R_L}{R_{IN}\ '}}{1 + \frac{A_{I0}}{1 + A_{I0}\beta_I} \times \frac{R_{OUT}\ '// R_L}{R_{IN}\ '} \times \beta_V} \tag{6.3}$$

Next, we calculate the A_{I0}, R_{IN}' (the input resistance when the shunt-series feedback is taken into consideration) and R_{OUT}' (the output resistance when the series-shunt feedback is taken into consideration) of the current amplifier as shown in Fig. 6-3(b). The A_{I0} is straightforward:

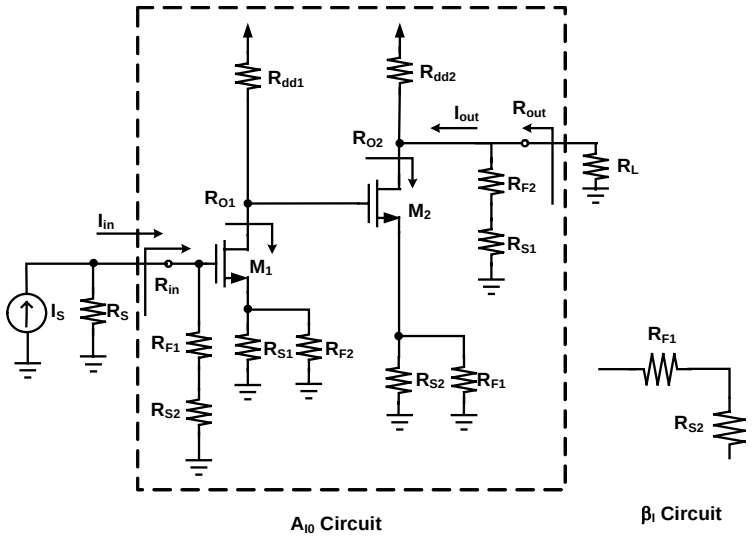
$$\begin{aligned} A_{I0} &= \frac{I_{out}}{I_{in}} \cong (R_{F1} + R_{S2}) \times G_{m1} \times (R_{dd1} // R_{O1}) \times G_{m2} \\ &= (R_{F1} + R_{S2}) \times \frac{g_{m1}}{1 + g_{m1} \times (R_{S1} // R_{F2})} \times (R_{dd1} // R_{O1}) \times \frac{g_{m2}}{1 + g_{m2} \times (R_{S2} // R_{F1})} \end{aligned} \tag{6.4}$$

Where the resistance R_{O1} is the output resistance when looking into the drain node of the transistor M_1. The input resistance of the current amplifier is:

$$R_{IN}{}' = \frac{R_{in}}{1 + A_{I0}\beta_I} = \frac{(R_{F1} + R_{S2})}{1 + A_{I0}\beta_I} \tag{6.5}$$



(a)



(b)

Fig. 6-3. (a) The A circuit and β_V circuit of the Meyer Amplifier after first decomposition, and (b) the A circuit and β_I circuit after second decomposition.

Thus, the total DC input resistance of the Meyer amplifier can be determined by:

$$R_{INTOTAL} = \frac{(R_{F1} + R_{S2}) \times (1 + A_V \beta_V)}{(1 + A_{I0} \beta_I)} \tag{6.6}$$

With the feedback factors:

$$\beta_I = -\frac{R_{S2}}{R_{S2} + R_{F1}} \text{ and } \beta_V = -\frac{R_{S1}}{R_{S1} + R_{F2}} \tag{6.7}$$

Similarly, The output resistance can be obtained by:

$$R_{out}' = R_{O2} // (R_{F2} + R_{S1}) // R_{dd2} \cong (R_{F2} + R_{S1}) // R_{dd2} \tag{6.8}$$

Where the resistance R_{O2} is the output resistance when looking into the drain node of the transistor M_2. The resistance R_{O2} is greatly increased because the source node of the transistor M_2 is in series with a large series-shunt feedback resistance [100]. Therefore, the R_{O2} is very large [100] and the value of R_{O2} can be neglected when R_{O2}, $(R_{F2}+R_{S1})$, and R_{dd2} are in parallel. Thus, the DC total output impedance of the Meyer amplifier is equal to:

$$R_{OUTTOTAL} = \frac{R_{out}'}{(1+A_{V0}\beta_V)} \cong \frac{(R_{F2}+R_{S1}) // R_{dd2}}{(1+A_{V0}\beta_V)} \tag{6.9}$$

As shown in Fig. 6-5, the A_V now can be described as follows:

$$\begin{aligned} A_V &= \frac{A_{I0}}{1+A_{I0}\times\beta_I} \times \frac{R_{OUT}' // R_L}{R_{IN}'} \\ &= \frac{A_{I0}}{1+A_{I0}\times\beta_I} \times \frac{(R_{F2}+R_{S1}) // R_{dd2} // R_L}{\frac{(R_{F1}+R_{S2})}{1+A_{I0}\times\beta_I}} \\ &= A_{I0} \times \frac{(R_{F2}+R_{S1}) // R_{dd2} // R_L}{(R_{F1}+R_{S2})} \end{aligned} \tag{6.10}$$

The total DC voltage gain of the Meyer amplifier is:

$$\begin{aligned} A_{V\ total} &= \frac{A_V}{1+A_V\times\beta_V} \\ &= \frac{A_{I0} \times \frac{(R_{F2}+R_{S1}) // R_{dd2} // R_L}{(R_{F1}+R_{S2})}}{1+A_{I0} \times \frac{(R_{F2}+R_{S1}) // R_{dd2} // R_L}{(R_{F1}+R_{S2})} \times \beta_V} \end{aligned} \tag{6.11}$$

Consequently, as shown in Fig. 6-1 and 6-2, the DC voltage gain from the voltage source, V_S to the load, R_L can be described as:

$$A_{VDC} = \frac{V_B}{V_S} = \frac{R_S}{R_S + R_{\text{int}otal}} \times \frac{A_V}{1+A_V\times\beta_V} \tag{6.12}$$

The DC values of the voltage gain, the input resistance and the output resistance of the Meyer wideband amplifier are determined by (6.6), (6.9), and (6.12).

6.2 The System Transfer Function

In order to determine the frequency response of the small signal power gain S_{21}, we have to find out the system transfer function of the Meyer amplifier. From (6.11), the system transfer function must be:

$$A_{V\ total}(S)=\frac{A_V(S)}{1+A_V(S)\times\beta_V}=\frac{A_{I0}(S)\times K}{1+A_{I0}(S)\times K\times\beta_V}$$
$$=\frac{A_{I0}\times K}{(1+\frac{S}{\omega_1})(1+\frac{S}{\omega_2})+A_{I0}\times K\times\beta_V} \quad (6.13)$$

Where $A_{I0}K$ is the voltage gain and K is a ratio of resistances:

$$K=\frac{(R_{F2}+R_{S1})//R_{dd2}//R_L}{(R_{F1}+R_{S2})} \quad (6.14)$$

Therefore, the loop gain T of the Meyer amplifier can be described as:

$$T=A_{I0}K\beta_V=-(R_{F1}+R_{S2})\times\frac{g_{m1}}{1+g_{m1}\cdot(R_{S1}//R_{F2})}\times(R_{dd1}//R_{O1})$$
$$\times\frac{g_{m2}}{1+g_{m2}\cdot(R_{S2}//R_{F1})}\times\frac{(R_{F2}+R_{S1})//R_{dd2}//R_L}{(R_{F1}+R_{S2})}\times\frac{R_{S1}}{R_{S1}+R_{F2}} \quad (6.15)$$ (15)

The denominator in (6.13) can be expressed as:

$$S^2+S(\omega_1+\omega_2)+(1+T)\omega_1\omega_2 \quad (6.16)$$

Next, as long as the ω_1 and ω_2 are determined, the frequency response of the system transfer function can be obtained. The original two poles (ω_1 and ω_2) will change to two complex poles (P_1 and P_2) caused by the voltage feedback loop. The feedback poles P_1, and P_2 can be calculated by:

$$P_1,P_2=-\frac{1}{2}(\omega_1+\omega_2)$$
$$\pm\frac{1}{2}\times\sqrt{(\omega_1+\omega_2)^2-4\times(1+T)\times\omega_1\times\omega_2} \quad (6.17)$$

The characteristic equation (6.16) can be changed to the following standard form:

$$S^2+S\frac{\omega_0}{Q}+{\omega_0}^2=0 \quad (6.18)$$

Where ω_0 is the natural frequency, and it can be described as:

$$\omega_0 = \sqrt{(1+T)(\omega_1\omega_2)} \tag{6.19}$$

And Q is the quality factor:

$$Q = \frac{\sqrt{(1+T)(\omega_1\omega_2)}}{(\omega_1+\omega_2)} \tag{6.20}$$

In order to let the transfer function (6.18) has the maximum flat response, the Q has to be 0.707. Therefore, the designer can force the pole locations ω_1 same as ω_2 and design the loop gain $(A_{I0}K\beta_V)=1$ to achieve the maximum flat response.

6.3 The Pole Locations of the Meyer Amplifier

Different from Kukielka amplifier, the Meyer topology does not use the Cherry-Hopper structure for the basic amplifier. A simple common source amplifier definitely suffers from its poor frequency response; therefore, the speed of the second stage must be improved. In practical applications, the Darlington configuration can be used for the second stage in the Meyer amplifier. Figure 4 shows a typical topology of the Meyer wideband amplifier including the source impedance R_S and the loading impedance R_L. As shown in Fig. 6-4, the Meyer amplifier consists of two source degenerative stages; first stage is a common-source amplifier, and the second stage is a Darlington frequency doubler.

Assume the Meyer amplifier is a two-pole system, and the first pole is the dominant pole of the first stage common source amplifier and the second pole is the dominant pole of the second stage Darlington amplifier. The equivalent small signal model used for solving the first pole of amplifier A_{I0} is shown in Fig. 6-5(a). Neglecting the biasing resistors R_1 and R_2, the first pole can be obtained by the open-circuit time constant method [102]:

$$\omega_1 = \frac{1}{C_{gs1}R_{gs1} + C_{gd1}R_{gd1}} \tag{6.21}$$

Where the R_{gs1} is approximated:

$$\frac{\left[R_S \,//(R_{F1} + R_{S2})\right] + (R_{S1} \,//\, R_{F2})}{1 + g_{m1}(R_{S1} \,//\, R_{F2})} \tag{6.22}$$

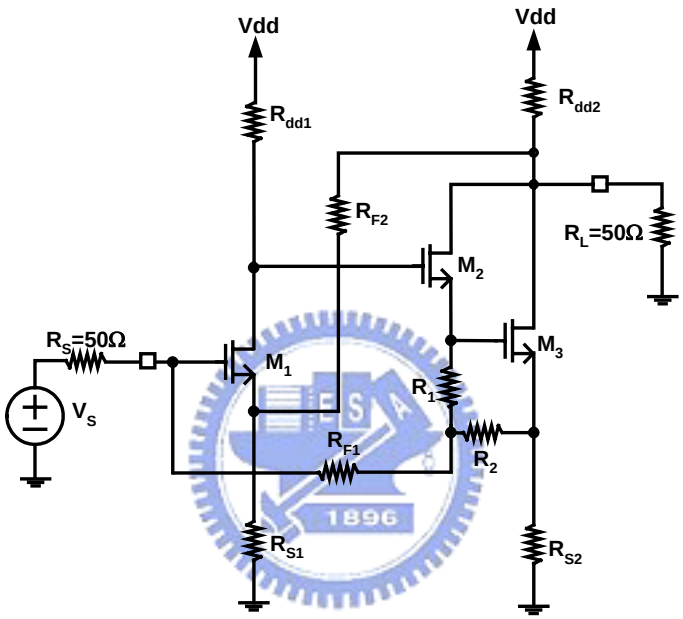


Fig. 6-4. The final topology of modified Meyer wideband amplifier.

The resistor R_S (the source impedance) is 50 ohms. And R_{gd1} equals:

$$R_{gd1} = R_1^{'} + R_{L1}^{'} + \frac{g_{m1}}{1 + g_{m1}(R_{S1} \,//\, R_{F2})} R_1^{'} R_L^{'}$$

where (6.23)

$R_1^{'} = R_S \,//(R_{F1} + R_{S2})$ and $R_{L1}^{'} \cong R_{dd1}$

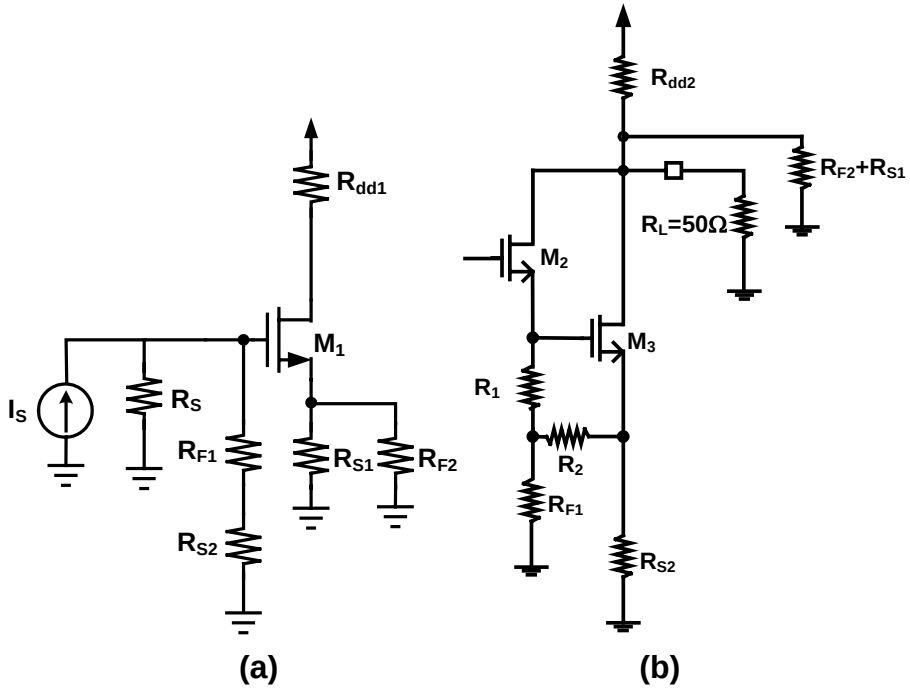


Fig. 6-5. The small signal model for solving (a) the first pole and (b) the second pole.

The second pole can be obtained by the small signal model shown in Fig. 6-5(b). Although the second stage is a Darlington pair, the dominant pole can be approximated by [100]:

$$\omega_2 \cong \frac{1}{C_T \times R_T + C_{gd3} \times \left[R_L \,//\, R_{dd2} \,//(R_{F2} + R_{S1}) \right]} \tag{6.24}$$

The transconductance g_{m2} of the common-drain transistor M_2 is normally much smaller than that of the transistor M_3 in the Darlington configuration. Consequently, the capacitance C_{gd2} and C_{gs2} can be neglected and only the capacitance C_{gs3} is taken into consideration. Therefore, the dominant pole of the Darlington stage is approximated by calculating the pole of the transistor M_3. The capacitance C_T is the Miller capacitance [100]:

$$\begin{aligned} C_T &\cong C_{gs3} + C_{gd3} \\ &\times \{1 + G_{m3} \cdot [R_{dd2} \,//\, R_L \,//(R_{F2} + R_{S1})]\} \end{aligned} \tag{6.25}$$

Assuming the resistor R_{S2} is small enough, which is usually valid for the CMOS amplifiers because the CMOS transistor gm naturally is much smaller, the resistor R_T

can be determined using the small signal model illustrated in the Fig. 6-6. The resistor R_{eq} is the output resistance of the source node of the transistor M_2, and it is approximated to:

$$R_{eq} \cong \frac{1}{g_{m2}} \tag{6.26}$$

As shown in Fig. 6-6, the resistance R_T can be calculated by changing the T-network (R_1, R_2 and R_{F1}) into Π-network (R_a, R_b and R_c) as shown in Fig. 6-6 [102]. Thus, the resistance R_T is:

$$R_T = \left[\left(R_{eq} \,//\, R_b\right) + \left(R_c \,//\, R_{S2}\right)\right] // \mathrm{R_a} \tag{6.27}$$

With

$$\begin{cases} R_a = \dfrac{R_1R_2 + R_1R_{F1} + R_2R_{F1}}{R_{F1}} \\ R_b = \dfrac{R_1R_2 + R_1R_{F1} + R_2R_{F1}}{R_1} \\ R_c = \dfrac{R_1R_2 + R_1R_{F1} + R_2R_{F1}}{R_2} \end{cases} \tag{6.28}$$

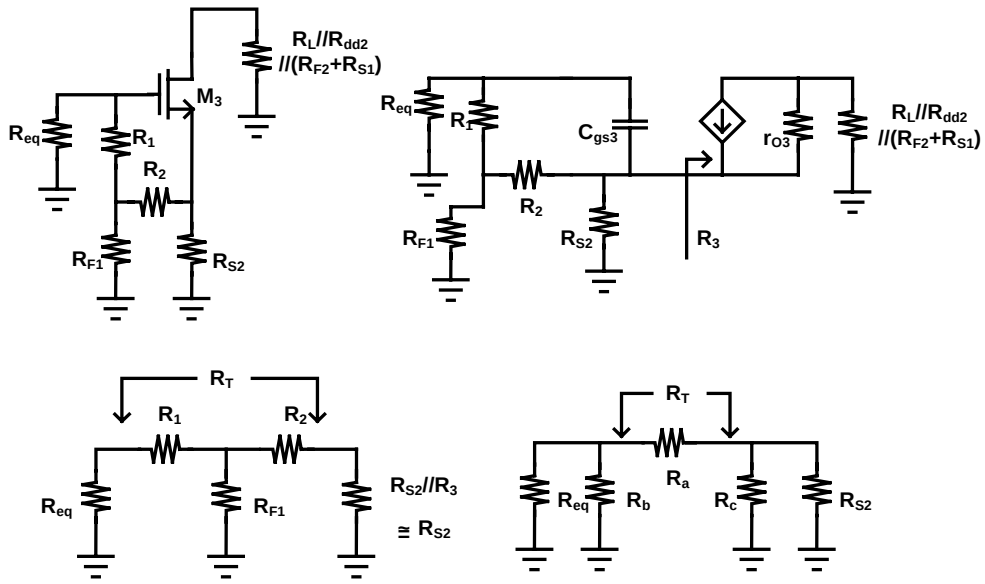


Fig. 6-6. The small signal model of the Darlington stage used to solve the frequency response.

According to (6.21), and (6.24), now the S_{21} can be determined once the A_{I0} and K are obtained by (6.4) and (6.14):

$$S_{21}(S) = 2 \times \frac{V_B}{V_S} = \frac{2 \times A_{VDC}}{(1+\frac{S}{P_1})(1+\frac{S}{P_2})} \tag{6.29}$$

According to (6.6), (6.7), (6.9), we intentional assume that all the S-parameters have the same poles (P_1, and P_2); therefore, the S-parameters can be obtained by following equations:

$$S_{11}(S) = \frac{R_{\text{int}otal} - 50}{R_{\text{int}otal} + 50} \times \frac{(1+\frac{S}{Z_1})(1+\frac{S}{Z_2})}{(1+\frac{S}{P_1})(1+\frac{S}{P_2})} \tag{6.30}$$

$$S_{22}(S) = \frac{R_{outtotal} - 50}{R_{outtotal} + 50} \times \frac{(1+\frac{S}{Z_3})(1+\frac{S}{Z_4})}{(1+\frac{S}{P_1})(1+\frac{S}{P_2})} \tag{6.31}$$

The zeros Z_1 and Z_2 can be obtained by solving the root of the dominator in (6.17) by changing the R_S into $-R_S$ [96], [97], [100]. Similarly, the zeros Z_3 and Z_4 are the root of the dominator in (6.17) by changing the R_L into $-R_L$.

6.4 The Simplified Design Equations and Design Methodology

Although the design equations of the DC values and pole locations are found in the previous sections, it is still difficult to give the designer an instinct to arrange the values of resistors in order to optimize the gain, the input/output resistances, and the bandwidth. However, the first-order design methodology of the Meyer amplifier is very clear based on some practical assumptions. As shown in (6.19), if the designer wants the largest bandwidth, the ω_1 must equal ω_2, and $A_{I0}K\beta_V$ has to be equal one. If the loop gain ($A_{I0}K\beta_V$) is equal to one, then:

$$
\begin{aligned}
&A_{I0}K\beta_V = 1 \\
&\cong (R_{F1}+R_{S2})\times G_{m1}\times R_{dd1}\times G_{m2} \\
&\times \frac{(R_{F2}+R_{S1}) // R_{dd2} // R_L}{(R_{F1}+R_{S2})} \times \frac{R_{S1}}{(R_{F2}+R_{S1})} \\
&\therefore G_{m1}R_{dd1}G_{m2} = \frac{(R_{F2}+R_{S1})R_{dd2}+(R_{F2}+R_{S1})R_L+R_{dd2}R_L}{R_{S1}R_{dd2}R_L}
\end{aligned}
\tag{6.32}
$$

Therefore, The input and output resistance can be simplified to the following equations:

$$
\begin{aligned}
R_{INTOTAL} &= \frac{(R_{F1}+R_{S2})\times 2}{(1+A_{I0}\beta_I)} \\
&= \frac{2(R_{F1}+R_{S2})}{1+(R_{F1}+R_{S2})G_{m1}R_{dd1}G_{m2}\dfrac{R_{S2}}{R_{F1}+R_{S2}}} \\
&= \frac{2R_L\times R_{S1}\times R_{dd2}(R_{F1}+R_{S2})}{R_{S1}R_{dd2}R_L+R_{S2}[(R_{F2}+R_{S1})R_L+(R_{F2}+R_{S1})R_{dd2}+R_LR_{dd2}]}
\end{aligned}
\tag{6.33}
$$

and:

$$
R_{OUTTOTAL} = \frac{(R_{F2}+R_{S1}) // R_{dd2}}{2} = \frac{(R_{F2}+R_{S1})R_{dd2}}{2(R_{F2}+R_{S1}+R_{dd2})} \tag{6.34}
$$

As we can see, these equations are helpful for the designers to determine the values of the resistors when the gain-bandwidth product is maximized. In order to obtain the first-order design equation, some extra but reasonable assumptions must be made. Assuming the β_I and β_V are very small to achieve the unity loop gain, thus the term $R_{F1}+R_{S2}$ and the term $R_{F2}+R_{S1}$ has to be large enough. For the output impedance matching, the resistance R_{dd2} in (6.34) can be described as:

$$
2\times 50 = R_{dd2} \tag{6.35}
$$

Therefore, the resistance of the loading resistor R_{dd2} must be near 100 ohms for the perfect impedance matching. Under the same assumptions, the equation (6.33) can be simplified to

$$50 = \frac{2R_L R_{S1} R_{dd2} (R_{F1} + R_{S2})}{(R_{F2} + R_{S1}) R_{S2} R_L + (R_{F2} + R_{S1}) R_{S2} R_{dd2}} \tag{6.36}$$

Using the results in (6.14) and (6.35), the voltage gain of the A circuit as shown in Fig. 6-3(a) is:

$$A_{I0} \cdot K = 33 G_{m1} R_{dd1} G_{m2} \tag{6.37}$$

Consequently, the first-order design flow for the maximum gain-bandwidth product is summarized as follows:

1) Assuming $A_{I0}K\beta_V = 1$ and thus R_{dd2} approximates 100 ohms for the output impedance matching.

2) Design the pole locations by (6.21) and (6.24). The first pole must be equal to the second pole.

3) The values determined in design flow 2) have to be checked by equation (6.36) to perform the input impedance matching.

4) Recursively repeat process 1) to 3) until the optimize values of the S-parameters are found.

6.5 Comparisons of the Small Signal Parameters Among Our Work and Previous Works

Compared with the previous works [91], [92], the derived circuit parameters in this paper such as total terminal impedances, and the gain in this work are more general because the transconductanceof the transistor has not to be very large in our assumption. According to the work [92], there is a major assumption that the transconductance of the transistor is large enough (which is true for the bipolar transistors) and thus both current and voltage feedback loops have equal feedback loop gain to the closed-loop voltage gain [92]. This assumption is employed to obtain the input and output impedance in [92]. However, the gm of the CMOS transistor is usually much smaller than that of the BJT transistor, and this assumption is not suitable for the CMOS Meyer wideband amplifier. In addition, as described in [91],

[92], the derived S_{21} is approximated to:

$$S_{21} \cong \frac{1}{2}\frac{R_{F2}+R_{E1}}{R_{E1}} \tag{6.38}$$

The emitter degenerative resistor R_{E1} in (6.38) equals the source degeneration resistor R_{S1} in our work. As shown in (6.38), the term S_{21} is proportional to $1/\beta_V$, which is based on very huge loop gain of the voltage feedback path, and only the voltage feedback loop (consisting of resistors R_{F2} and R_{S1}) is taken into consideration in this special case. Under this circumstance, the loop gain is greatly larger than one; therefore, the bandwidth is not optimized. The result of S_{21} in (6.38) implies that only the voltage feedback loop dominates the dual feedback system; however, it is not true to analyze the terminal impedance matching, especially for CMOS technologies.

Consequently, the approaches of determining the terminal impedances and the gain in reference [91][92] are based on the conflict assumptions in a single circuit. Our work has provided much general formula to determine the gain, and input/output impedance.

6.6 Circuit Design

In this section, a shunt-series series-shunt dual feedback wideband amplifier is demonstrated using 0.13 um CMOS technology. The advanced 0.13 um CMOS technology is suitable to implement the high performance RFICs. The circuit schematic and the designed values of resistors are shown in Fig. 6-7. This Meyer amplifier is design and implemented with the CMOS technology to verify our theory because of its excellent cut-off frequency provided by the technology. This Meyer amplifier is designed without the source capacitive peaking technique in order to simplify the prediction of the pole locations

As shown in Fig. 6-7, a Darlington pair is employed in the second stage of the demonstrated Meyer amplifier. The effective transconductance g_{meff} of the Darlington pair can be determined by using (6.39). In the most cases, the g_{meff} can be simply

approximated to g_{m3}.

$$g_{meff} = \frac{g_{m2} + g_{m2} \cdot g_{m3} \cdot (R_1 + R_2)}{1 + g_{m2} \cdot (R_1 + R_2)} \tag{6.39}$$

In this section, a shunt-series series-shunt dual feedback wideband amplifier is demonstrated using 0.13 um CMOS technology. The circuit schematic and the designed values of resistors are shown in Fig. 6-7. This Meyer amplifier is design and implemented with the CMOS technology to verify our theory because of its excellent cut-off frequency provided by the technology. The maximum cutoff frequency f_T is around 80- GHz.

The die photo of the 0.13 μm CMOS wideband amplifier is shown in Fig. 6-8. The input RF GSG pads are on the left while the output RF GSG pads are on the right. There are two DC bias pads on the top. As shown in Fig. 6-8, the chip consumes area of 800 X 800 μm^2. The wideband amplifier only needs chip area of 150X150 μm^2, and the probing pads, metal dummies and poly dummies occupy the rest 96 % chip area. It is because the 0.13 μm process requires dummies to perform the CMP (Chemical Mechanical Polishing) process. The DC supply is 2.5 V and the current consumption is 24 mA.

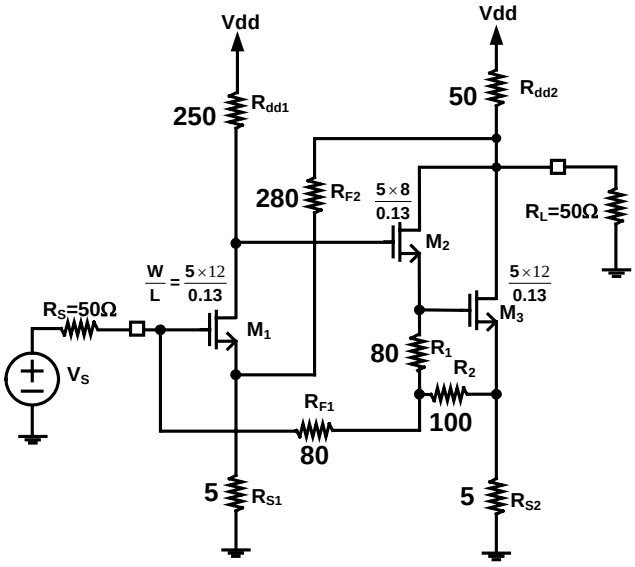


Fig. 6-7. The demonstrated 0.13 μm CMOS Meyer wideband amplifier with its component values.

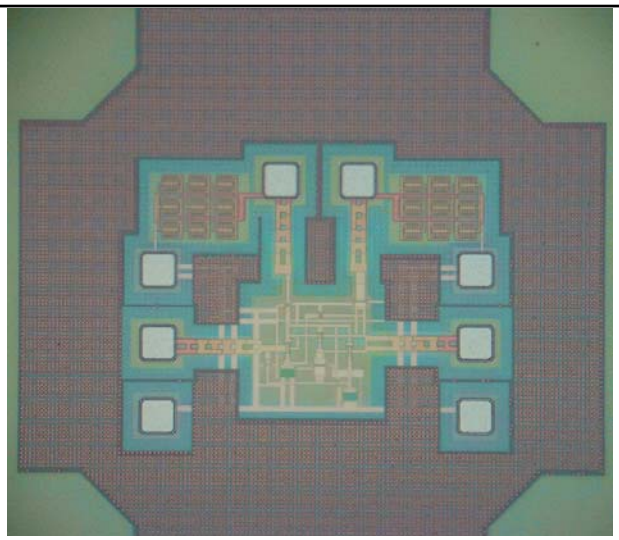


Fig. 6-8. The die photograph of the 0.13 μm CMOS shunt-series series-shunt double feedback amplifier.

An HP8510 network analyzer in conjunction with the Cascade on-wafer probe station is used to measure the S parameter performances. Figure 6-9 shows the measured power gain S_{21} of the fabricated wideband amplifier. In addition, the predicted S_{21} by our theory is drawn in the same figure for comparison. The Meyer amplifier has 17 dB gain with 10-GHz bandwidth.

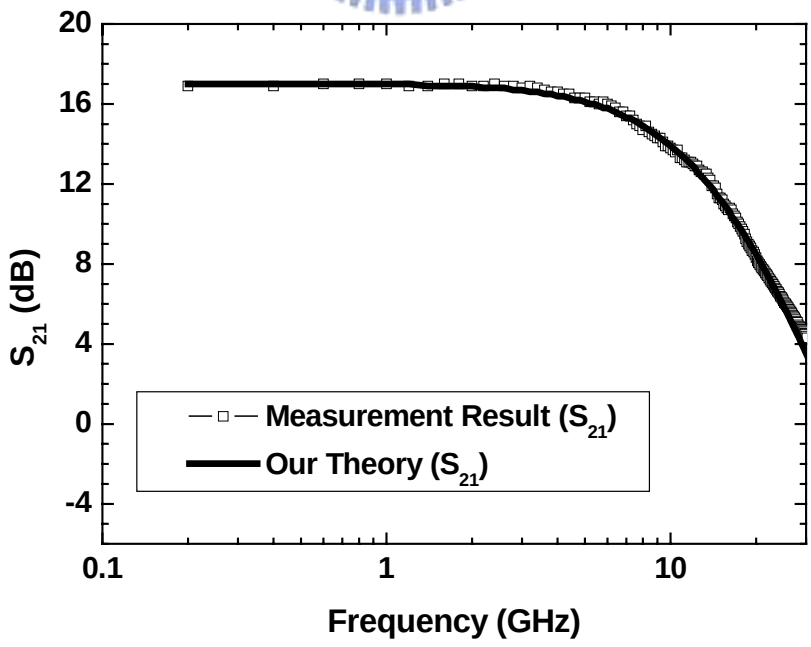


Fig. 6-9. The measured S_{21}, and the S_{21} predicted by our theory of the 0.13 μm CMOS Meyer wideband amplifier.

Figure 6-10 shows the measured S_{11}, and the predicted S_{11} by our theory. On the other hand, the measured S_{22}, and the predicted S_{22} by our theory are shown in Fig. 6-11. The measured input and output return loss are less than –10 dB in the 3-dB gain-bandwidth, respectively. Consequently, our theory is highly agreed with the experimental S-parameters results. The measured noise figure of the Meyer wideband amplifier is shown in Fig. 6-12. The demonstrated wideband amplifier exhibits a flat-gain bandwidth of 7GHz as shown in Fig. 6-9. The measured noise figure is better than 6.5 dB within the flat-gain bandwidth.

Figure 6-13 shows the measured OP_{1dB} and OIP_3 of the demonstrated Meyer wideband amplifier. The power performances degrade as the operating frequency getting higher. The OP_{1dB} and the OIP_3 within the flat gain bandwidth is better than –11dBm and 0 dBm, respectively.

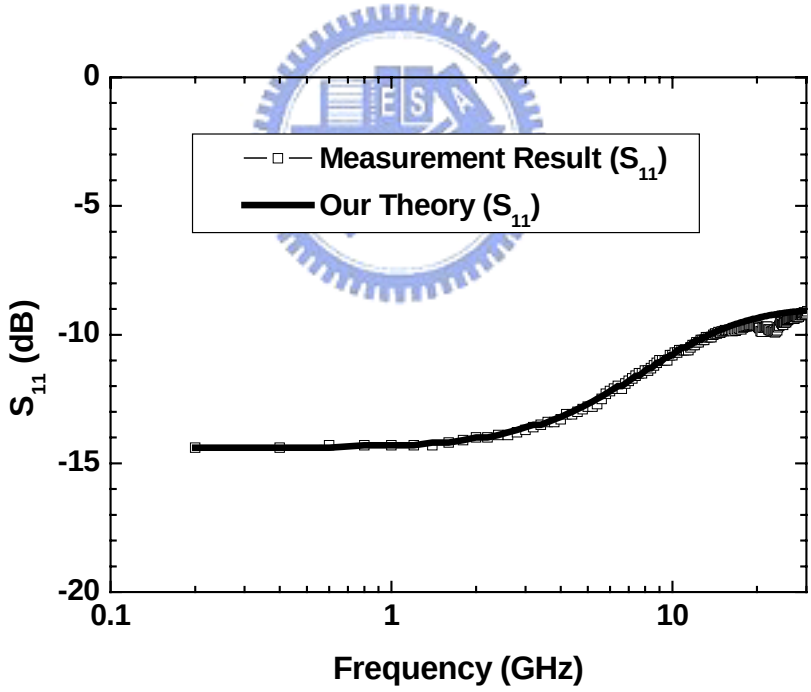


Fig. 6-10. The measured S_{11}, and the S_{11} predicted by our theory of the 0.13 μm CMOS Meyer wideband amplifier.

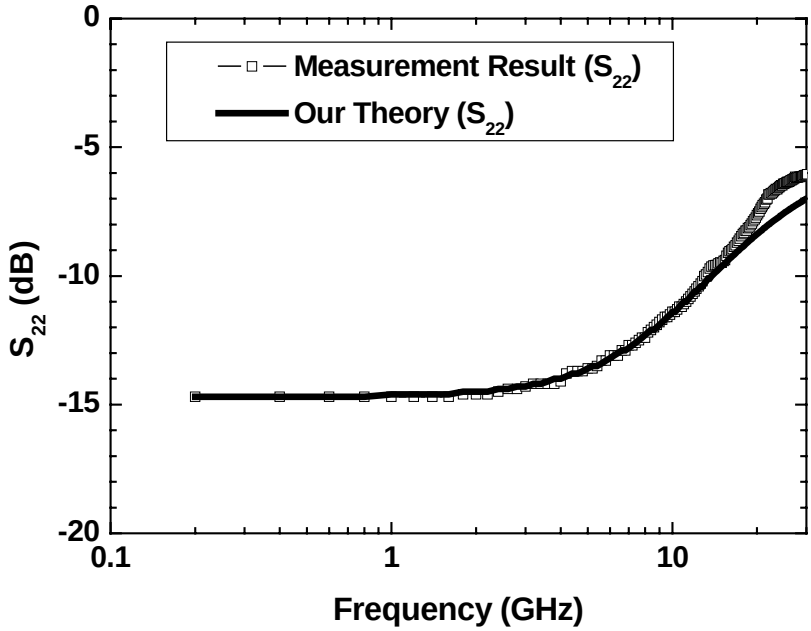


Fig. 6-11. The measured S_{22}, and the S_{22} predicted by our theory of the 0.13 μm CMOS Meyer wideband amplifier.

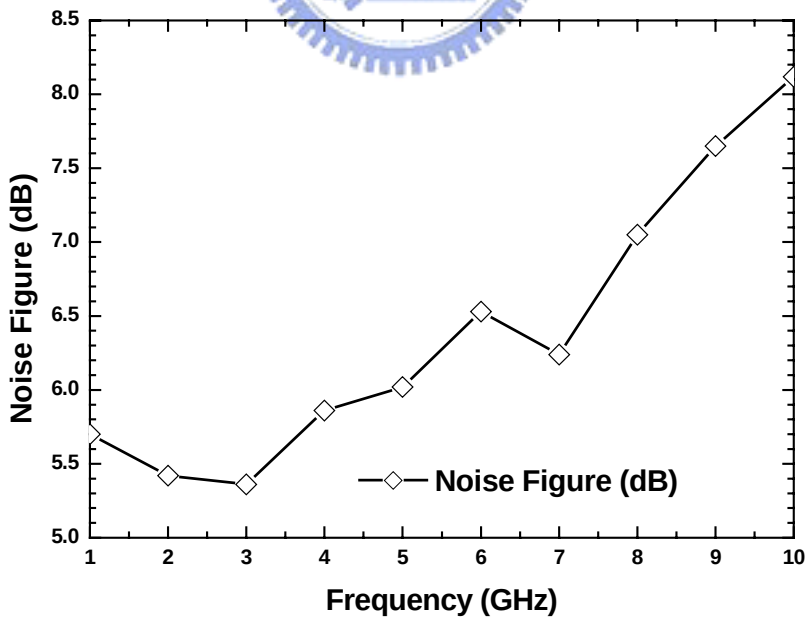


Fig. 6-12. The measured noise figure of the 0.13 μm CMOS Meyer wideband amplifier.

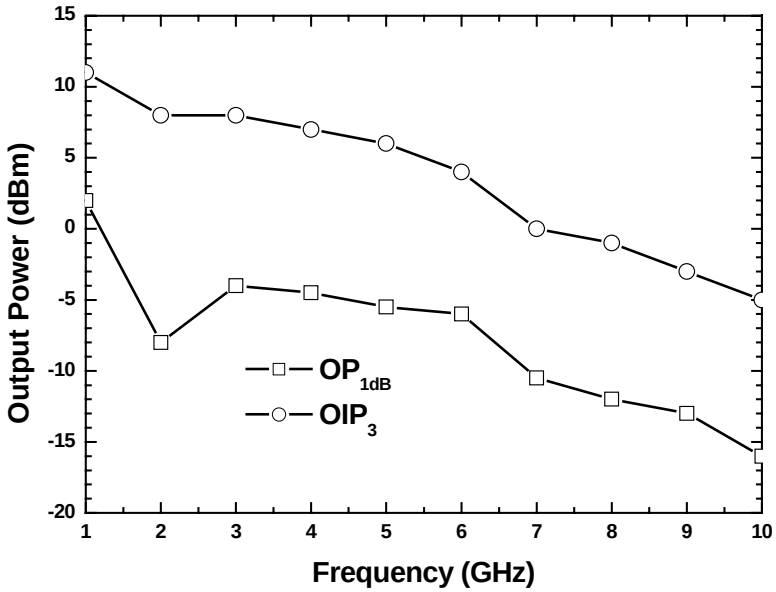


Fig. 6-13. The measured power performance of the 0.13 um CMOS Meyer wideband amplifier.

The first-order design methodology of the shunt-series series-shunt double feedback Meyer wideband amplifier is developed. A 10-GHz wideband amplifier is demonstrated using 0.13 μm CMOS technology. The experimental results are highly agreed with our theory, and the design trade-offs are discussed. The small signal S-parameters are obtained by the approach of pole and zero analysis; therefore, it gives the insight of the Meyer wideband amplifier to the RF designers. The fabricated 0.13 μm CMOS wideband amplifier has 17 dB gain, -10 dB input return loss, and -10 dB output return loss with 10-GHz bandwidth. The noise figure of the demonstrated amplifier is lower than 8.2 dB while the OP_{1dB} and OIP_3 is better than –16 dBm and -5 dBm, respectively in the bandwidth.

Chapter 7

Conclusion and Future Work

High performance direct-conversion mixers are investigated. The design trade-offs of the stacked-LO, top-leveled-LO, and bottom-leveled-LO sub-harmonic Gilbert mixers are obtained. The stacked-LO sub-harmonic mixer can operate with the smallest LO pumping power at the cost of a higher DC voltage supply. On the other hand, the leveled-LO sub-harmonic mixers including the top-LO-configured and the bottom-LO-configured mixers can operate in higher frequencies. In addition, there are still some design trade-offs in the two leveled-LO mixer topologies. The top-LO-configuration mixer has higher conversion gain and 2LO-to-RF isolation but the bottom-LO-configuration mixer has advantage in terms of the power consumption, the linearity and the RF-to-IF isolation. A novel LO compensated sub-harmonic topology is proposed, and the 10 GHz novel sub-harmonic mixer presents excellent IIP_2 and 2LO-to-RF isolation. Because the LO is truly balanced, the IIP_2 is as high as 33 dBm when the RF frequency is 10 GHz.

Another important building block is the up-conversion mixer. Several high performance up-conversion Gilbert mixer are demonstrated. The L-C current combiner and the lumped-element rat-race hybrid used in the conversion mixer are analyzed. The design methodology and the analysis of the LC current mirror including the parasitic resistors are developed in this work. The design consideration of the rat-race hybrid is also obtained. In this work, up-conversion mixers using the LC current mirror and the lumped rat-race hybrid are demonstrated using 0.35 um SiGe HBT technology and GaInP/GaAs HBT technology. In addition to the passive inductors used in the LC current mirror, the active inductor formed by the conventional common-collector output buffer is also employed. A compact up-onversion Gilbert mixer using the active inductor for the LC current mirror is demonstrated, and the chip area is effectively saved.

High performance receiver architecture have been demonstrated and analyzed in the thesis. The conventional image rejection Hartley and Weaver systems are

demonstrated. Both of them present excellent image rejection ratio. Moreover, a novel Weaver-Hartley system is proposed. This novel system combines the advantages of the Hartley and Weaver architectures and presents high image rejection ratios. The proposed novel architecture can be used to implement a dual band system and two 5.7/2.4 GHz down-converter are demonstrated.

There are still other types of the dual-conversion image rejection architectures. These topologies shall be summarized for the future work. The first category is the Weaver-Hartley system as shown in Fig. 7-1 (a) and (b).

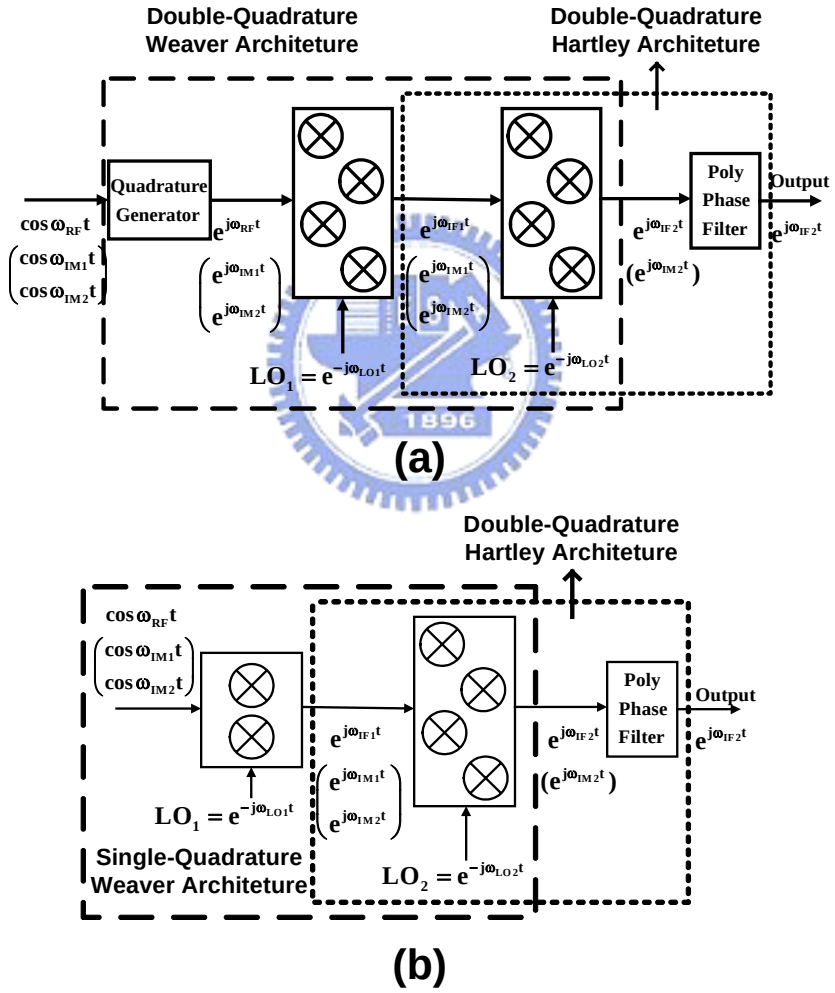


Fig. 7-1. The block diagram of (a) the double-quadrature Weaver with double-quadrature Hartley architecture, and (b) the single-quadrature Weaver with double-quadrature Hartley architecture.

Figure 7-1(a) is a double-quadrature Weaver with double-quadrature Hartley architecture, and this kind of configuration can provide the pest performance of the

first image signal rejection as well as the secondary image signal rejection because the dual double quadrature structures minimize signal mismatches. Figure 7-1(b) is a single-quadrature Weaver with double-quadrature Hartley architecture. This topology is less complicated at the cost of worse first image signal rejection.

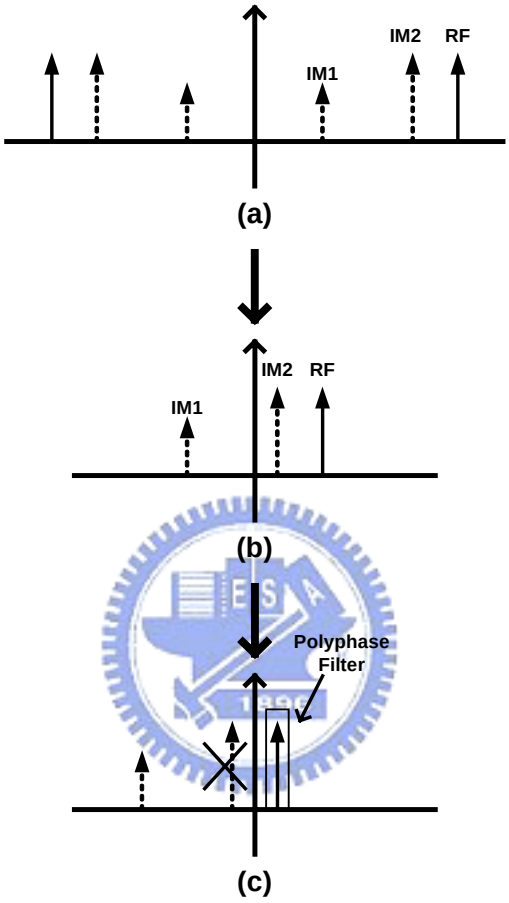


Fig. 7-2. The illustration of the frequency shifting (down-converting) of the single quadrature Weaver-Hartley system.

Figure 7-2 shows the frequency shifting (down-converting) of the single quadrature Weaver-Hartley system. The first image signal, secondary image signal, and the RF signal before mixing are illustrated in Fig. 7-2(a). When these signals pass through or are mixed down by the first stage of the Weaver-Hartley system, the spectrum should be Fig. 7-2(b). Finally, the resulting signal is shown in Fig. 7-3(c) when the signals pass through the second stage mixers. The down-conversion sequence is the same as that described in Chapter 4 and 5. The double quadrature Weaver-Hartley system frequency shifting is similar to the case of single quadrature Weaver-Hartley system, and the only difference is that the signals in the negative

spectrum as shown in Fig. 7-2(a) is absence.

The second category is the Hartley-Hartley system as shown in Fig. 7-3 (a) and (b). The first stage of this kind of dual-conversion system is a Hartley structure, and it consists of mixers and polyphase filters. Compared with the Weaver-Hartley system, the Hartley-Hartley system requires additional polyphase filters as shown in Fig. 7-3 (a) and (b). The extra polyphase filter is used to reject the first image signal and extend the dynamic range of the second stage mixers. However, this structure obviously is more complicated and area-wasted. Besides, additional polyphase filter means that the phase accuracy of the polyphase filters become very critical to achieve the image rejection successfully.

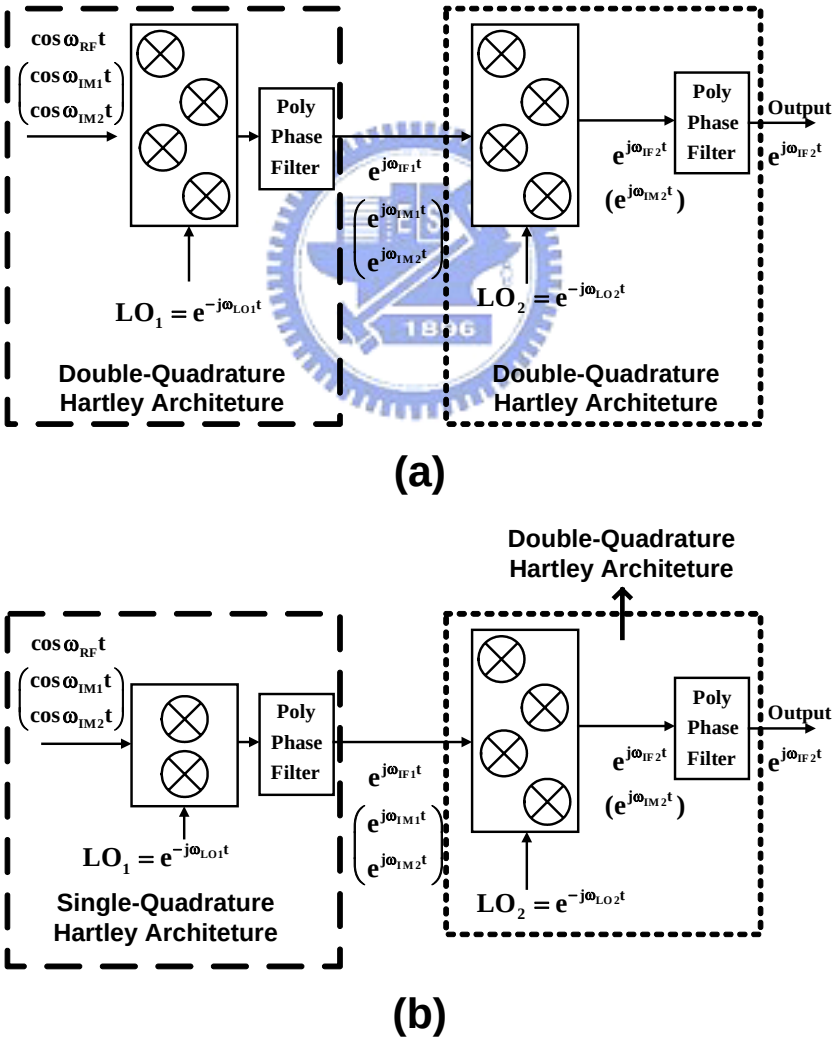


Fig. 7-3. The block diagram of (a) the double-quadrature Hartley with double-quadrature Hartley architecture, and (b) the single-quadrature Hartley with double-quadrature Hartley architecture.

Figure 7-4 shows the frequency shifting (down-converting) of the single quadrature Hartley-Hartley system and the case of double-quadrature system is neglected because they are quite similar. The first image signal, secondary image signal, and the RF signal before mixing are illustrated in Fig. 7-4(a). When these signals pass through by the first stage mixers and the polyphase filter of the Weaver-Hartley system, the spectrum should be like Fig. 7-4(b). Finally, the resulting signal is shown in Fig. 7-4(c) when the signals pass through the second stage mixers and the polyphase filter. The first and secondary image signals are basically rejected by the polyphase filter.

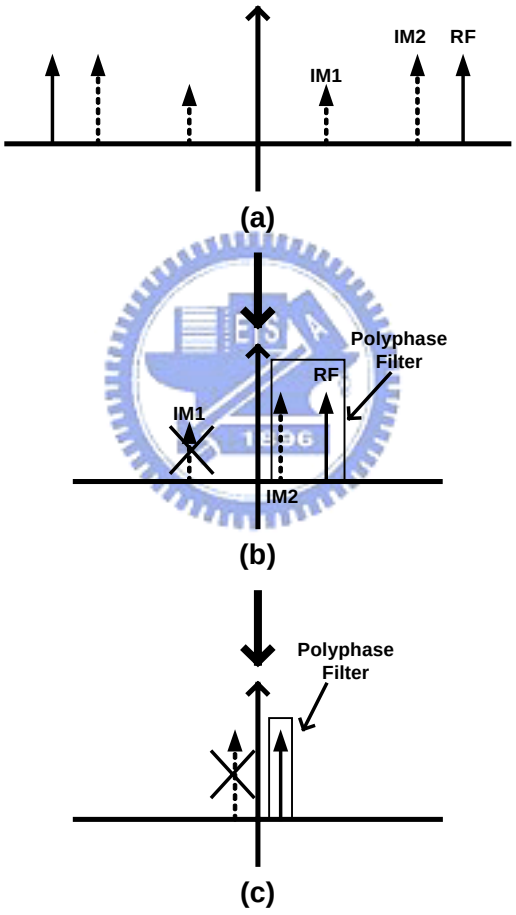


Fig. 7-4. The illustration of the frequency shifting (down-converting) of the single quadrature Hartley-Hartley system.

Next, the third category is the Weaver system combined with the double quadrature direct-conversion system as shown in Fig. 7-5 (a) and (b). The first stage of this kind of dual-conversion system is a Weaver structure, and it consists of four mixers in the first stage and four sub-harmonic mixers in the second stage. Because

the frequency of the IF_2 signal is set to be zero, there is no secondary image signal in this topology. This zero-IF topology doesn't require the polyphase filter; however, the design of the second-stage sub-harmonic mixer is quite challenging for CMOS technology because the CMOS transistor has poor 1/f noise performance. In addition, an accurate octet-phase LO signal generator is also very difficult to be achieved.

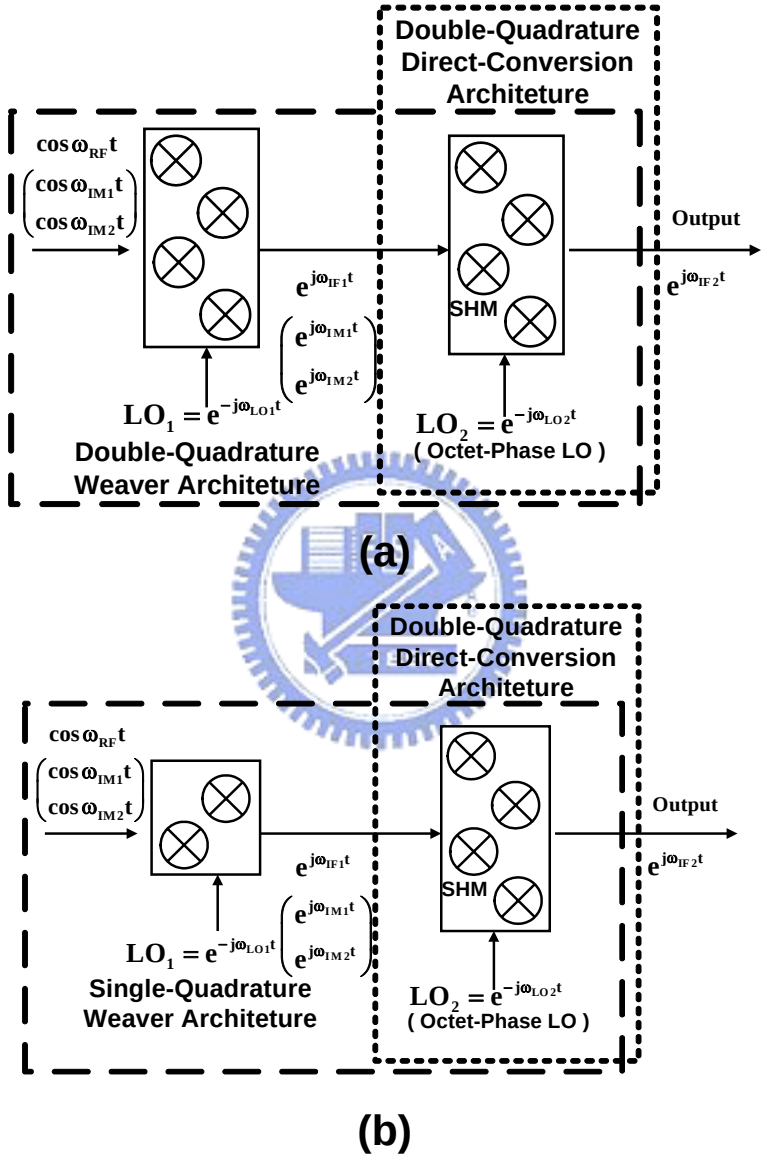


Fig. 7-5. The block diagram of (a) the double-quadrature Weaver with direct-conversion architecture, and (b) the single-quadrature Weaver with direct-conversion architecture.

The spectrum shifting of the single quadrature Weaver with direct-conversion system is shown in Fig. 7-6. Because the second stage is a direct-conversion system, there is no secondary image problem. Figure 7-6(a) shows the spectrum of the RF signal and the first image signal before mixing. Figure 7-6(b) shows the spectrum

after the signals passing through the first stage mixers. The resulting signals is shown in Fig. 7-6(c). The image signal can be filtered out by the IF circuits since the first image signal is shifted to high frequency.

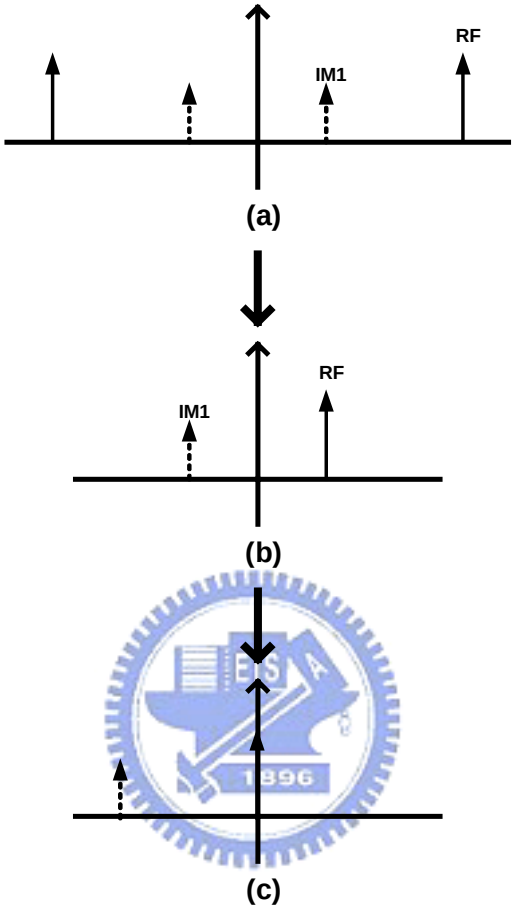


Fig. 7-6. The illustration of the frequency shifting (down-converting) of the single quadrature Weaver with direct-conversion system.

Finally, the final group of the dual-conversion system is the Hartley system combined with the double quadrature direct-conversion system as shown in Fig. 7-7 (a) and (b). Similarly, the second stage is a double quadrature direct-conversion system, and thus there is no secondary image problem. This structure is the most complicated and it contains all the drawbacks of the previous architecture such as 1/f noise problem, the phase accuracy of the polyphase filter, and the complicated octet-phase LO generator.

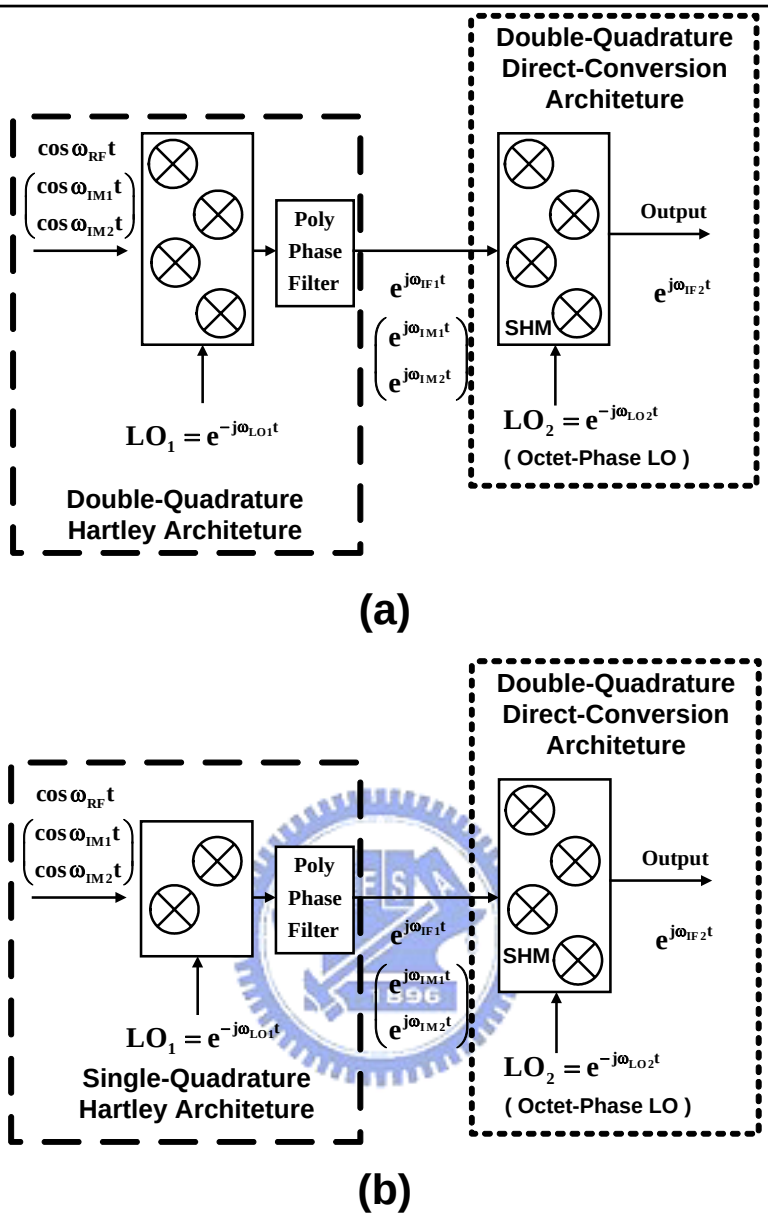


Fig. 7-7. The block diagram of (a) the double-quadrature Hartley with double-quadrature direct-conversion architecture, and (b) the single-quadrature Hartley with double-quadrature direct-conversion architecture.

The frequency shifting of the Hartley with direct-conversion system is shown in Fig. 7-8. As mentioned, there is no secondary image signal problem in this system. The spectrum of the signals after mixed down by the first stage mixers is shown in Fig. 7-8(b). As shown here, the polyphase filter filters out the image signal. The resulting down-converted RF signal is shown in Fig. 7-8(c).

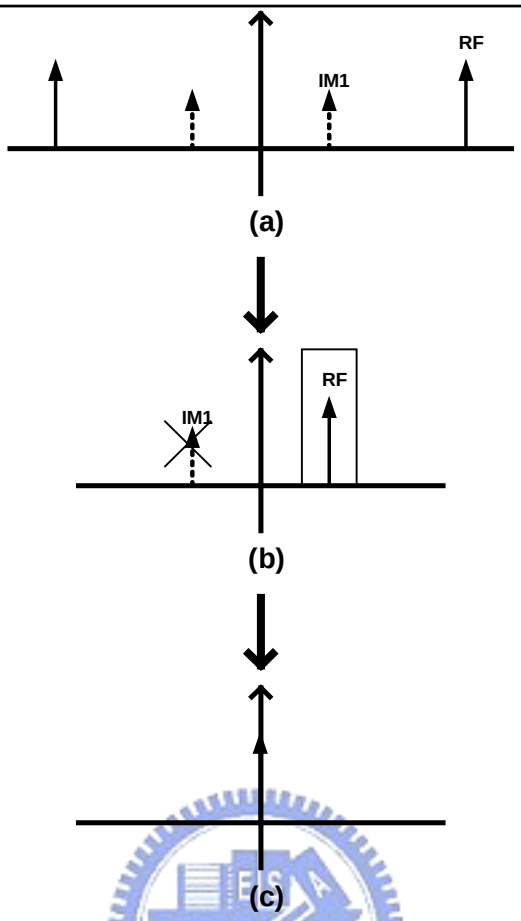


Fig. 7-8. The illustration of the frequency shifting (down-converting) of the single quadrature Hartley with direct-conversion system.

Finally, a shunt-series series-shunt wideband amplifier in 0.13 um CMOS technology is presented in this dissertation. The small signal design equations of the wideband amplifier is established in this thesis, and the experimental results are highly agreed with our design theory. The small signal S-parameters are obtained by the approach of pole and zero analysis; therefore, it gives the insight of the Meyer wideband amplifier to the RF designers. The fabricated 0.13 μm CMOS wideband amplifier has 17 dB gain, -10 dB input return loss, and -10 dB output return loss with 10-GHz bandwidth. The noise figure of the demonstrated amplifier is lower than 8.2 dB while the OP_{1dB} and OIP_3 is better than –16 dBm and -5 dBm, respectively in the bandwidth.

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Appendix A

The Mathematical Derivation of Image Rejection Ratio of Weaver and Hartley Architectures

In this section, the detailed derivation of the image rejection ratio is developed. As shown in Fig. A-1(a), a Weaver down-converter is illustrated. The desired input signal is defined as:

$$D(t) = \cos \omega_{RF} t \tag{A.1}$$

And the image signal is:

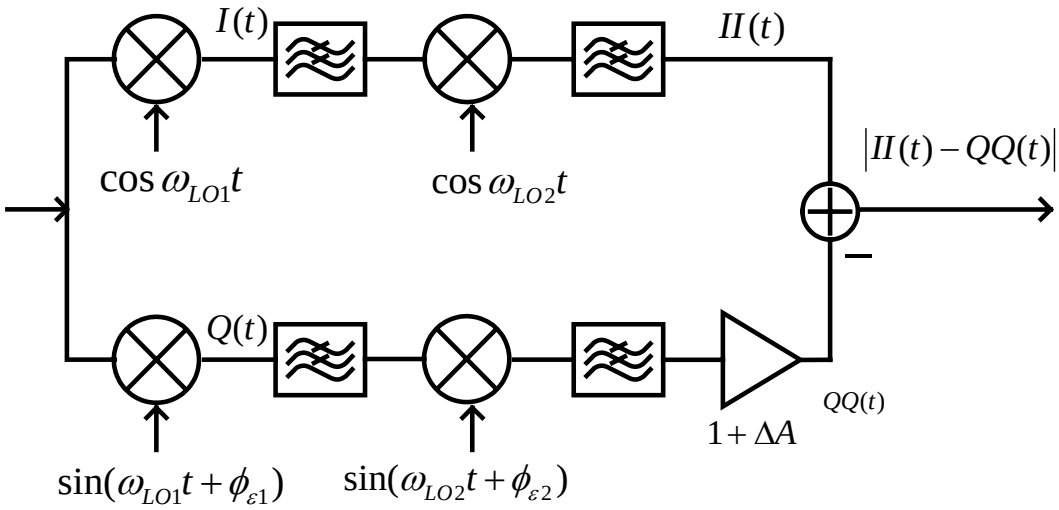
$$IM(t) = \cos \omega_{IM} t \tag{A.2}$$

The $\phi_{\varepsilon 1}$ and $\phi_{\varepsilon 2}$ represent the phase error of LO_1 and LO_2 signals, respectively. Therefore, the down-converted signals after the first stage mixer are:

$$\begin{aligned}
I_D(t) &= \frac{1}{2}\left[\cos\left(\omega_{RF} - \omega_{LO1}\right)t + \cos\left(\omega_{RF} + \omega_{LO1}\right)t\right] \\
I_{IM}(t) &= \frac{1}{2}\left[\cos\left(\omega_{IM} - \omega_{LO1}\right)t + \cos\left(\omega_{IM} + \omega_{LO1}\right)t\right] \\
Q_D(t) &= \frac{1}{2}\left\{\sin\left[\left(\omega_{RF} + \omega_{LO1}\right)t + \phi_{\varepsilon 1}\right] - \sin\left[\left(\omega_{RF} - \omega_{LO1}\right)t - \phi_{\varepsilon 1}\right]\right\} \\
Q_{IM}(t) &= \frac{1}{2}\left\{\sin\left[\left(\omega_{IM} + \omega_{LO1}\right)t + \phi_{\varepsilon 1}\right] - \sin\left[\left(\omega_{IM} - \omega_{LO1}\right)t - \phi_{\varepsilon 1}\right]\right\}
\end{aligned} \tag{A.3}$$

Furthermore, these signals after the second stage mixer become:

$$\begin{aligned}
II_D(t) &= \frac{1}{4}\cos \omega_{IF2} t \\
II_{IM}(t) &= \frac{1}{4}\cos \omega_{IF2} t \\
QQ_D(t) &= -\frac{1}{4}(1+\Delta A)\left[\cos\left(\phi_{\varepsilon 1} + \phi_{\varepsilon 2}\right)\cos \omega_{IF2} t + \sin\left(\phi_{\varepsilon 1} + \phi_{\varepsilon 2}\right)\sin \omega_{IF2} t\right] \\
QQ_{IM}(t) &= \frac{1}{4}(1+\Delta A)\left[\cos\left(\phi_{\varepsilon 1} - \phi_{\varepsilon 2}\right)\cos \omega_{IF2} t - \sin\left(\phi_{\varepsilon 1} - \phi_{\varepsilon 2}\right)\sin \omega_{IF2} t\right]
\end{aligned} \tag{A.4}$$



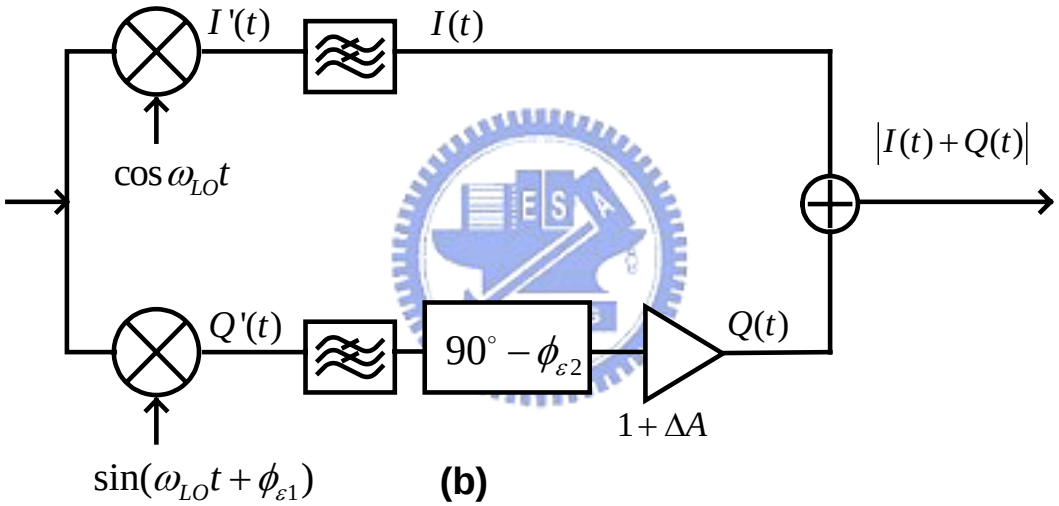


Fig. A-1. The block diagram of (a) the Weaver architecture, and (b) the Hartley architecture.

Where ΔA represents the gain mismatch. Consequently, the image rejection ratio of the Weaver down-converter can be determined as:

$$IRR(dB) = 10\log\frac{\left|II_D(t) - QQ_D(t)\right|^2}{\left|II_{IM}(t) - QQ_{IM}(t)\right|^2} = 10\log\left[\frac{1+(1+\Delta A)^2 + 2(1+\Delta A)\cos(\phi_{\varepsilon 1}+\phi_{\varepsilon 2})}{1+(1+\Delta A)^2 - 2(1+\Delta A)\cos(\phi_{\varepsilon 1}-\phi_{\varepsilon 2})}\right] \quad \text{(A.5)}$$

On the other hand, the image rejection ratio of the Hartley down-converter also

can be obtained. As shown in Fig. A-1(b), it is the block diagram of a Hartley down-converter. If the $\phi_{\varepsilon 1}$ represents the phase mismatch of the LO signal, and $\phi_{\varepsilon 2}$ identifies the phase error of the 90^o phase shifter (or the polypahse filter used in the Hartley low-IF systems [6][17]), the image rejection ratio can be obtained by flowing derivations. The output signals mixed by the first stage mixer are:

$$\begin{aligned}
I_D'(t) &= \frac{1}{2}\left[\cos(\omega_D - \omega_{LO})t + \cos(\omega_D + \omega_{LO})t\right] \\
I_{IM}'(t) &= \frac{1}{2}\left[\cos(\omega_{IM} - \omega_{LO})t + \cos(\omega_{IM} + \omega_{LO})t\right] \\
Q'_D(t) &= \frac{1}{2}\left\{\sin\left[(\omega_D + \omega_{LO})t + \phi_{\varepsilon 1}\right] - \sin\left[(\omega_D - \omega_{LO})t - \phi_{\varepsilon 1}\right]\right\} \\
Q'_{IM}(t) &= \frac{1}{2}\left\{\sin\left[(\omega_{IM} + \omega_{LO})t + \phi_{\varepsilon 1}\right] - \sin\left[(\omega_{IM} - \omega_{LO})t - \phi_{\varepsilon 1}\right]\right\}
\end{aligned} \tag{A.6}$$

After the 90^o phase shifter:

$$\begin{aligned}
I_D(t) &= \frac{1}{2}\cos\omega_{IF}t \\
I_{IM}(t) &= \frac{1}{2}\cos\omega_{IF}t \\
Q_D(t) &= \frac{1}{2}(1+\Delta A)\left[\cos(\phi_{\varepsilon 1} + \phi_{\varepsilon 2})\cos\omega_{IF}t + \sin(\phi_{\varepsilon 1} + \phi_{\varepsilon 2})\sin\omega_{IF}t\right] \\
Q_{IM}(t) &= -\frac{1}{2}(1+\Delta A)\left[\cos(\phi_{\varepsilon 1} - \phi_{\varepsilon 2})\cos\omega_{IF}t - \sin(\phi_{\varepsilon 1} - \phi_{\varepsilon 2})\sin\omega_{IF}t\right]
\end{aligned} \tag{A.7}$$

Where $\omega_{IF} = \omega_D - \omega_{LO} = \omega_{LO} - \omega_{IM}$ and ΔA represents the gain mismatches. Therefore, the image rejection ratio of the Hartley architecture is:

$$\begin{aligned}
IRR(dB) &= 10\log\frac{\left|I_D(t) + Q_D(t)\right|^2}{\left|I_{IM}(t) + Q_{IM}(t)\right|^2} \\
&= 10\log\left[\frac{1 + (1+\Delta A)^2 + 2(1+\Delta A)\cos(\phi_{\varepsilon 1} + \phi_{\varepsilon 2})}{1 + (1+\Delta A)^2 - 2(1+\Delta A)\cos(\phi_{\varepsilon 1} - \phi_{\varepsilon 2})}\right]
\end{aligned} \tag{A.8}$$

The image rejection ratio of the Hartley architecture is identical to that of the Weaver architecture as shown in (A.5) and (A.8). Furthermore, the image rejection ratio derived in (A.8) is identical to the result in [73] when the phase shifter or the

polypahse filter is assumed to be fully balanced. From the above derivation, it is clear that eliminating the phase errors or making the phase errors of LO_1 and LO_2 equal can optimize the image rejection ratio of the Weaver down-converter. This property is directly caused by the frequency shifting as discussed previously. However, the image signal caused by the LO signal and the polypahse filter mismatches cannot be set to be equal in the Hartley system. The phase error of polypahse filter obviously is independent from the LO signal of the first stage mixer in Hartley down-converters. As a result, the image rejection performance of the Weaver architecture has a chance to be further improved by making these individual phase errors coherent.

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Publication List

Journal Paper：

[1] **Tzung-Han Wu**, Sheng-Che Tseng, Chinchun Meng, and Guo-Wei Huang, "GaInP/GaAs HBT Sub-Harmonic Gilbert Mixers Using Stacked-LO and Leveled-LO Topologies", ***IEEE Transactions on Microwave Theory and Techniques***, vol. 55, no. 5, pp. 880-889, May 2007. (SCI)

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