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博 士 論 文

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Abstract (Chinese)

國立交通大學

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摘　　要

在本論文中，是以 0.15 微毫米砷化鎵(GaAs)假晶格高速電子遷移電晶體（pHEMT）及變形晶格高速電子遷移電晶體(mHEMT)來設計毫米波頻段的類比積體電路與單晶微波積體電路。這些砷化鎵的技術具有高崩潰電壓，截止頻率，低雜訊，高輸出功率和半絕緣基板的優點。除此，高頻電路的封裝技術也很重要，在此採用覆晶封裝技術來驗證 V 頻段的放大器在封裝前後有一樣的特性。

在第二章中，使用 0.15 微毫米砷化鎵 pHEMT 來提出設計在 Ku 跟 Ka 頻帶的三種吉伯特混頻器。由於半絕緣的砷化鎵基版，微波被動元件具低損耗而且多重相位濾波器可以操作在較高的頻段。利用高精確的氮化鉭薄膜式電阻可設計多重相位濾波器而產生完美的正交相位。因此，我們所提出的 15 GHz 單頻帶升頻器具有 63 dB 的單邊頻帶消除比率，另一個 34 GHz 次諧波正交輸出的降頻器可達到小於 0.4 dB 的振幅與 1°相位的誤差，且超過 50 dB 的本端振盪源（LO）洩漏壓制。再者，提出 40 GHz 次諧波堆疊式-LO 電路使用補償式技術來解決延遲時間的問題而且比較我們之前所發表論文可以減少電晶體數量。

在第三章比較 Q 頻帶 0.15 微毫米 PHEMT 及 mHEMT 的次諧波堆疊式-LO 升頻器在增益，隔絕度及線性度上的差異。一般來說，0.15 微毫米 mHEMT 的元件比 pHEMT 具有較高的轉導和截止頻率。所以在設計主動吉伯特混頻器，使用 mHEMT 製程的轉換增益應該會比 pHEMT 來的大。利用 pHEMT 及 mHEMT

製程來設計 Q 頻帶的次諧波堆疊式-LO 升頻器，經量測分別有-7.1 dB 及-0.2 dB 的轉換增益。pHEMT 的升頻器有-12 dBm 的輸出三階截止點和-24 dBm 的輸出 1dB 壓縮點，此時 mHEMT 線性度改善有 4 dB 在於輸出 1dB 壓縮點與輸出三階截止點的差值。

在第四章節展現 V 頻帶的共平面波導-微帶線-共平面波導兩級放大器結合覆晶封裝技術。為了配合覆晶封裝的結構，輸入與輸出端則設計共平面波導，而中間級則採用微帶傳輸線來減少晶片面積。在這兩級放大器著重是在第一級利用電晶體當作共平面波導轉換成微帶線，及在第二級利用電晶體將微帶線轉換成共平面波導。共平面波導-微帶線-共平面波導轉換的兩級放大器在 53 GHz 有 14.8 dB 的增益，10 dB 及 22 dB 的輸入及輸出反射係數。經過覆晶封裝後的量測放大器特性也跟沒有覆晶封裝前幾乎差不多。

在第 5 章節說明使用 mHEMT 製程設計一個 60 GHz 單晶微波積體電路接收機。接收機包括一個 LO 倍頻串，60 GHz 鏡像消除二極體混頻器及一個 60GHz 的三級低雜訊放大器。LO 倍頻串的形成是採用一個乘三器及一個三級的回授放大器。而 60GHz 的鏡像消除混頻器則採用對稱式的次諧波二極體混頻器且結合了 IF 及三倍 LO 頻率的正交分合波器。這 60 GHz mHEMT 接收機有 5 dB 的轉換增益，7 dB 的雜訊指數和 22 dB 的鏡像消除比率。且有-24 dBm 的輸入 1dB 壓縮點和-16 dBm 的輸入三階截止點。

第六章節報告用 pHEMT 製程設計在 Ka 頻帶正交輸出除二的米勒除頻器。架構是基於一個正向回授的迴路，包含了一個馬爾尚巴倫，兩個乘法器和 LC 槽濾波器。除頻器使用單邊頻帶升頻器來驗證正交輸出的精確度。可達到 35 dB 的旁波帶消除比率。最小的輸入靈敏度是 2.7 dBm，可除的頻寬從 32 到 36 GHz 比率是 12%。

關鍵字：補償、降頻器、多重相位濾波器、假晶格高速電子遷移率電晶體、正交、

單邊頻帶、次諧波、升頻器、變形晶格高速電子遷移率電晶體、共平面波導管、覆晶封裝、微帶線、60 GHz、單晶片、砷化鎵、完全整合、鏡像消除、接收機、單晶微波積體電路、混頻器、除二、馬爾尚巴倫、米勒除頻器、乘法器。


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Millimeter-Wave HEMT Transceiver With Analog Circuit Design Approach and Flip-Chip Technology

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Abstract (English)

In this dissertation, all analog integrated circuits and monolithic microwave integrated circuits (MMICs) are demonstrated using 0.15-μm pseudomorphic high electron mobility transistor (pHEMT) and metamorphic high electron mobility transistor (mHEMT) technologies. These GaAs-based technologies have the advantages of a high breakdown voltage, cutoff frequency, low noise figure, higher output power, and semi-insulating substrate. Furthermore, a package technique is an important key for high-frequency circuits. The flip-chip technique is demonstrated that the performances of V-band amplifiers with and without flip-chip are almost the same.

In Chapter 2, three kinds of Ka/Ku-band Gilbert mixers are demonstrated using pHEMT technology. Thanks to the semi-insulating GaAs substrate, microwave passive components have a low-loss feature, and polyphase filters work up to higher frequencies. Highly accurate Tantalum Nitride (TaN) thin film resistors utilized in polyphase filters result in perfect quadrature operation. Therefore, our proposed single-sideband up-converter operates at 15 GHz with a 63-dB sideband rejection ratio, and another 34-GHz I/Q subharmonic down-converter reaches < 0.4-dB

magnitude and < 1° phase errors. More than 50-dB LO leakage suppression is achieved in the I/Q subharmonic mixer. On the other hand, a 40-GHz stacked-LO subharmonic mixer with a novel compensation technique is also proposed and demonstrated to improve LO speed and reduce the amount of transistors as compared to the previous work.

Chapter 3 makes a comparison between Q-band 0.15 μm pHEMT and mHEMT stacked-LO subharmonic upconversion mixers in terms of gain, isolation and linearity. In general, a 0.15 μm mHEMT device has a higher transconductance and cutoff frequency than a 0.15 μm pHEMT does. Thus, the conversion gain of the mHEMT is higher than that of the pHEMT in the active Gilbert mixer design. The Q-band stacked-LO subharmonic upconversion mixers using the pHEMT and mHEMT technologies have conversion gain of -7.1 dB and -0.2 dB, respectively. The pHEMT upconversion mixer has an OIP_3 of -12 dBm and an OP_{1dB} of -24 dBm, while the mHEMT one shows a 4 dB improvement on linearity for the difference between the OIP_3 and OP_{1dB}.

In Chapter 4, the V-band coplanar waveguide (CPW)-microstrip line (MS)-CPW two-stage amplifier with the flip-chip bonding technique is demonstrated. The CPW is used at input and output ports for flip-chip assemblies and the MS transmission line is employed in the interstage to reduce chip size. This two-stage amplifier employs transistors as the CPW-MS transition and the MS-CPW transition in the first stage and the second stage, respectively. The CPW-MS-CPW two-stage amplifier has a gain of 14.8 dB, input return loss of 10 dB and output return loss of 22 dB at 53.5 GHz. After the flip-chip bonding, the measured performances have almost the same value.

A 60 GHz single-chip receiver MMIC using 0.15-μm mHEMT technology is demonstrated in Chapter 5. The receiver consists of an LO multiplier chain, a 60 GHz

three-stage low noise amplifier, and 60 GHz image rejection diode mixer. The LO chain is formed with a tripler and a 28 GHz three-stage feedback amplifier. Furthermore, the 60 GHz image rejection mixer is a symmetrical subharmonic diode mixer and integrated with IF and 3 × LO quadrature hybrids. The mHEMT receiver has the conversion gain of 4 dB, the noise figure of 7.0 dB, and the image rejection ratio of 22 dB at 60 GHz. The -24 dBm IP_{1dB} and -16 dBm IIP_3 are measured.

Chapter 6 reports a Ka-band quadrature-output divide-by-two Miller divider using the 0.15-μm pHEMT technology. The circuit topology consists of one Marchand balun, two active multipliers and LC-tank filters with a positive feedback loop. The divider includes a single side-band (SSB) up-converter to verify the quadrature accuracy of the divider's outputs. A 35-dB side-band rejection ratio is achieved. The minimum input sensitivity equals 2.7 dBm. The stable division from 32 to 36 GHz in a bandwidth of 12 % can be obtained.

Keywords: Compensation, down-converter, polyphase filter, pseudomorphic high electron mobility transistor (pHEMT), quadrature, single sideband (SSB), subharmonic, up-converter, metamorphic high electron mobility transistor (mHEMT), coplanar waveguide (CPW), flip-chip, microstrip line (MS), 60 GHz, single-chip, GaAs, fully integrated, image rejection, receiver (RX), MMIC, mixer, divide-by-two, Marchand balun, Miller divider, multiplier.


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List of Abbreviations and Symbols

Abbreviations

CPW	Coplanar Waveguides
CG	Conversion Gain
EM	Electromagnetic
FGCPW	Finite-Ground Coplanar Waveguide
GSGSG	Ground–Signal–Ground–Signal–Ground
I/OP_{1dB}	Input/Output 1-dB Gain Compression Point
I/OIP_3	Input/Output Third-Order Intercept Point
I/Q	In-Phase/Quadrature
IC	Integrated Circuit
LO	Local Oscillator
LNA	Low Noise Amplifier
MS	Microstrip Line
MMIC	Monolithic Microwave Integrated Circuit
MIM	Metal-insulator-metal
NF	Noise Figure
mHEMT	metamorphic High Electron Mobility Transistor
pHEMT	pseudomorphic High Electron Mobility Transistor
RFD	Regenerative Frequency Divider
RX	Receiver
SSB	Single Side-Band
SOC	System-on-Chip
TX	Transmitter
TaN	Tantalum Nitride

Symbols

λ	Wavelength
ω_0	Operating frequency, resonant frequency
f_T	Cut-off frequency
*f*max	Maximum Oscillator Frequency
gm	Transconductance of a transistor
k	Coupling factor
Q	Quality factor

Z_0	Terminal impedance
Z_{0e}	Even-mode characteristic impedance
Z_{0o}	Odd-mode characteristic impedance


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Chapter 1 Introduction

1.1 ADVANTAGES OF HEMT TECHNOLOGY

Until now, high electron mobility transistor (HEMT) technology has played a chief role in microwave and millimeter-wave circuits [1], [2]. The advantages of HEMT transistors, such as large transconductance, great power density, low noise figure, and high breakdown voltage, as well as a semi-insulating GaAs substrate are favorable for circuits operating at high frequencies. Today, the HEMT technology retains the world record for the cut-off frequency and maximum operation frequency (about 500-GHz ft and about 400-GHz fmax) [3]. Obviously, HEMT-based low-noise amplifiers (LNAs) and power amplifiers (PAs) are superior to silicon-based circuits at microwave and millimeter-wave regimes in terms of gain, noise figure and power performances [4]-[6]. Much effort has been expended to integrate silicon-based front-end circuits with CMOS analog and logic circuits. However, HEMT-based LNAs and PAs are not yet replaceable for better performance especially at much higher frequencies. Connections between individual LNAs, PAs, and mixers using different technologies in a module suffer from large loss. It is preferable to implement the front-end circuits with the same process and on the same chip to reduce chip connections at high frequencies. Here, the HEMT technology is the best choice at high-frequency regimes [7]. Figure 1-1 shows the profile of a GaAs-based HEMT structure [8]. The process includes the metal-insulating-metal (MIM) capacitors (C_{plate}=0.39 fF/μm^2), thin-film resistors (50 Ω/□), mesa resistors (150 Ω/□ for pHEMT and 180 Ω/□ for mHEMT), backside processing, via-hole etching, air-bridge and two metal layers.

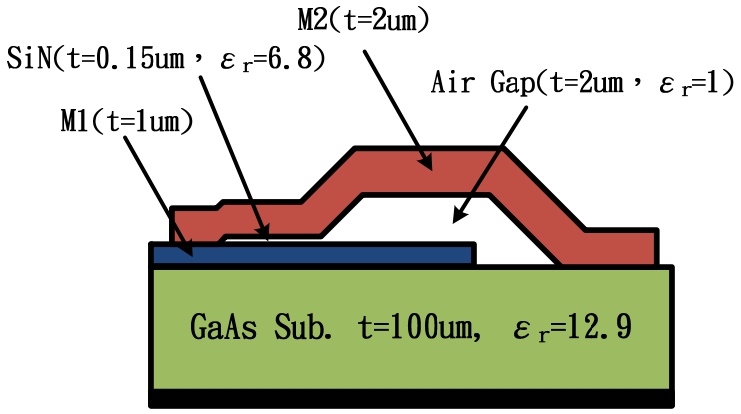


Fig. 1-1 Profile of a GaAs-based HEMT structure.

A metamorphic HEMT (mHEMT) on a GaAs substrate has a lower noise figure, a higher transconductance and a higher cutoff frequency (f_T) as compared with a pseudomorphic HEMT (pHEMT). Fully integrated 60 GHz single-chip front-end MMICs show that the mHEMT, contrasted with the pHEMT, has higher gain, higher output power and lower power consumption [7]. The advantage of the technology appears obviously in the amplifiers, which is a conclusive outcome. In the past, different kinds of passive mixers, such as diode mixers and FET resistive mixers, were discussed using the HEMT technology [9]-[11]. However, the diode passive mixers, using the pHEMT and mHEMT technologies, show comparable performances because the potential barriers associated with pHEMT and mHEMT diodes are almost equivalent. Identical resistive mixers using the 0.15 μm mHEMT and pHEMT technologies nearly have the same conversion loss, even though the mHEMT technology has a higher ft of 110 GHz, while the 0.15 μm pHEMT technology employed has an 85 GHz f_T [10]. TABLE 1.1 shows the comparison between pHEMT and mHEMT technologies.

TABLE 1-1 Typical data of pHEMT and mHEMT technologies [Herbert, MTT 2006].

Parameter	pHEMT	mHEMT	Unit
Gate length	0.15	0.15	μm
In mole fraction	15~30	40	%
f_t	88	110	GHz
f_{max}	183	200	GHz
Gm_{peak}	495	730	mS/mm
$V_{breakdown}$(gate-drain)	10	12	volt
I_{DSmax}(Vgs=0.5V)	650	530	mA/mm

The diode and passive mixers have good linearity but a larger conversion loss [12]-[14], whereas the traditional microwave passive components based on quarter-wavelength design concepts are not compact and consume the real estate in the IC technology [15], [16]. Therefore, analog circuit design, where a high f_T is important, concepts are adopted in this dissertation rather than implementing impedance matching design approaches. The double balanced Gilbert mixer is a popular topology for designing an active mixer due to the benefits of high conversion gain, compact size, and good isolation. Many Gilbert complex mixers have been realized using CMOS and SiGe HBT technologies, mostly at low frequencies. Lately, advancements in silicon device scaling have made Gilbert mixers possible even at millimeter-wave frequencies [10], [17].

1.2 Current State of development for Millimeter-Wave Front-End in GaAs

In the wireless communications, the combination package provides voice, video, and data service. This type of service requires the high data-rate and board bandwidth. The millimeter-wave regime can be used to satisfy these requirements. In recent years, researchers have paid significant attention to the 60 GHz front-end monolithic

microwave integrated circuits (MMICs) in the millimeter-wave regime. 57 GHz ~ 64 GHz bands in the U.S. and 57 GHz ~ 66 GHz bands in Europe are the best solutions due to unlicensed bands and oxygen resonance. Figure 1-2 shows that oxygen absorption in the air reaches its maximum value of 10~15 dB/km in the 60 GHz band. The advantages of the millimeter-wave band include greater high-speed bandwidth, higher resolution radar, smaller antenna, less crowded bandwidth, less jamming and less interference. Furthermore, the chip in the band is light, small, and highly integrated. On the other hand, it also comes with certain disadvantages – expensive parts, higher air loss, lower power device, and difficulty in design and manufacture.

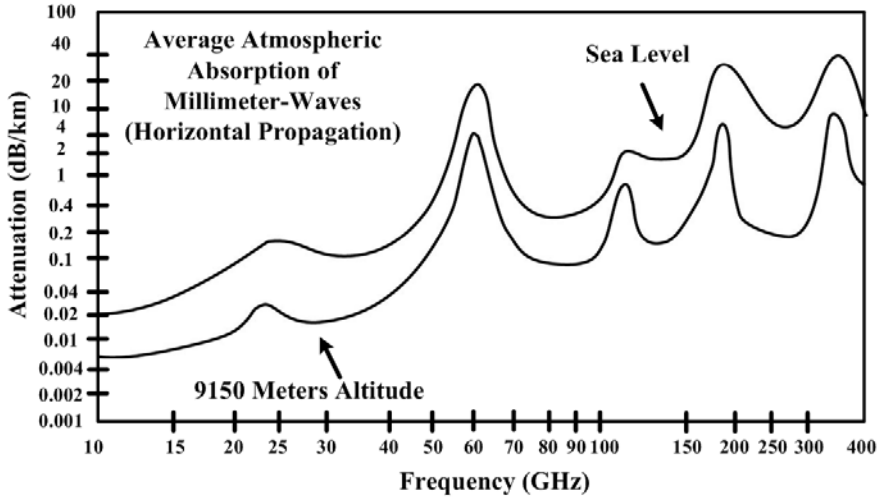
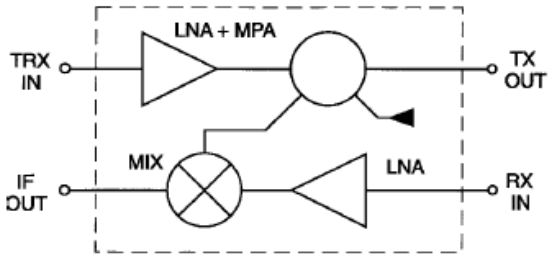
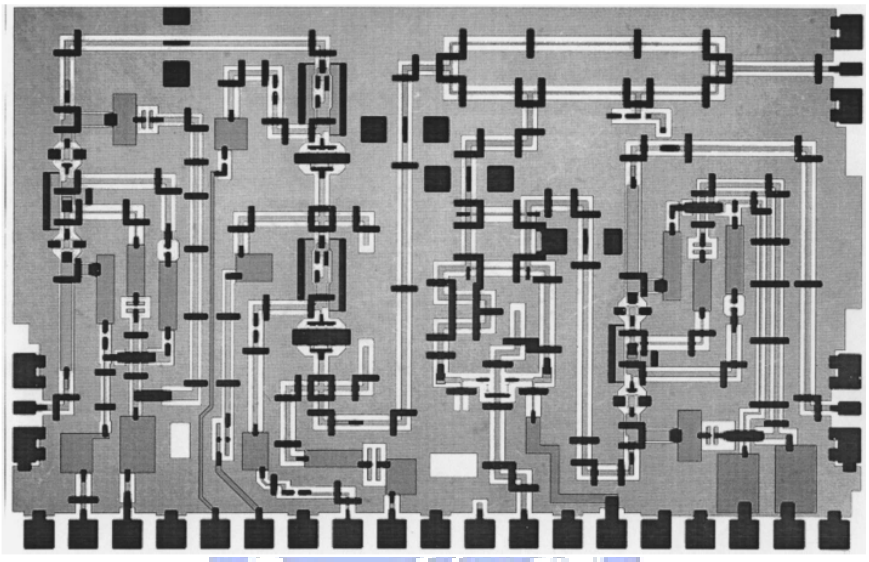


Fig. 1-2 Millimeter-wave atmosphere absorption.

Previous research has developed GaAs-based single-chip front-end circuits in the millimeter-wave regime [18], [1], [7]. Figure 1-3, 1-4 and 1-5 illustrate these circuits. Figure 1-3 depicts the coplanar monolithic microwave integrated circuits for 77 GHz millimeter-wave sensor applications designed by Siemens Semiconductor Group. Part (a) and (b) of this figure depict the block diagram and photograph of this highly integrated transceiver, respectively. Siemens Semiconductor developed this 0.12 μm pHEMT technology in-house.



(a)

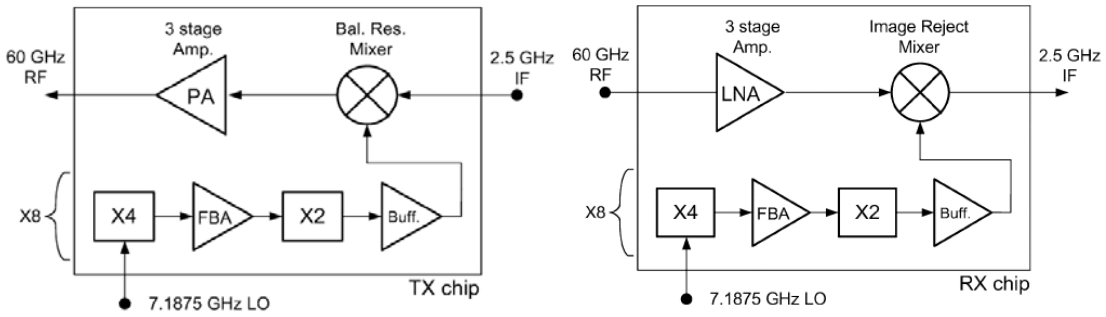


(b)

Fig. 1-3 (a) Block diagram and (b) chip photograph of the 77-GHz transceiver MMIC (2.0mm × 3.0mm) [Siemens, MTT 1998].

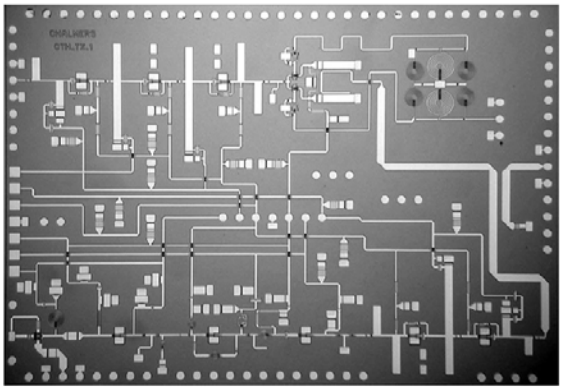
Herbert recently proposed a V-band single-chip transmitter and receiver using 0.15 μm pHEMT and mHEMT technologies. Figure 1-4 (a) and (b) shows the block diagrams of the V-band transmitter (Tx) and receiver (Rx), respectively. Figure 1-5 (a) and (b) shows the Tx and Rx photographs of the fabricated chip using pHEMT technology. Figure 1-6 (a) and (b) corresponds with Fig. 1-4 (a) and (b), respectively, for mHEMT technology. The performances of HEMT V-band transmitters and receivers usually perform than those of CMOS. These results prove the feasibility of a GaAs single MMIC chip in the millimeter-wave front-end circuits. Furthermore, a package technique is necessary in the manufacture IC products, especially in

microwave and millimeter-wave regimes.

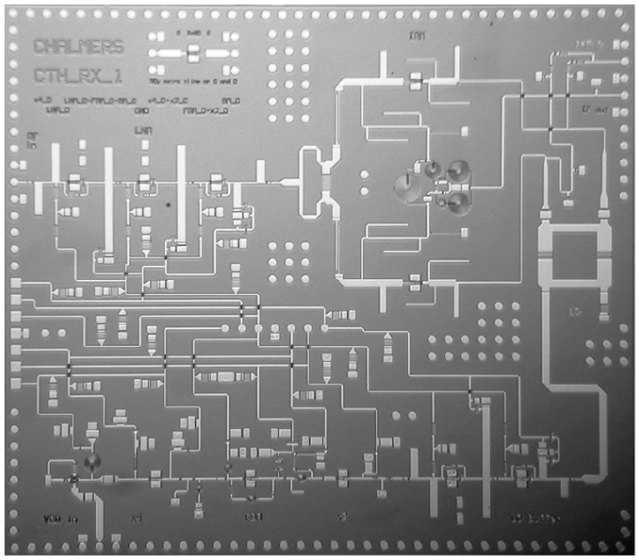


(a) Tx (b) Rx

Fig. 1-4 Circuit block diagrams of (a) Tx and (b) Rx chips at 60 GHz [Herbert, JSSC 2005, 2007].

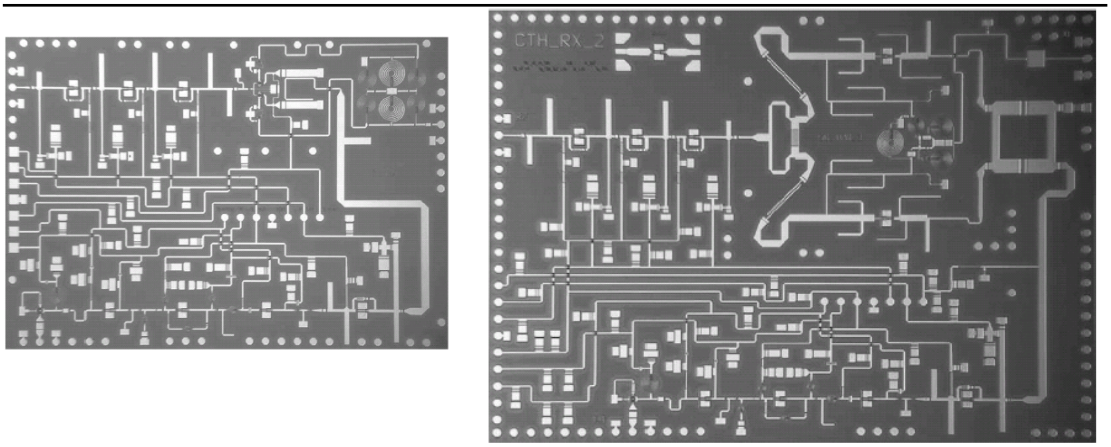


(a) pHEMT transmitter chip



(b) pHEMT receiver chip

Fig. 1-5 (a)The pHEMT transmitter chip measures 5.0 mm × 3.5 mm and (b) the pHEMT receiver chip is 5.7 mm × 5.0 mm [Herbert, JSSC 2005].



(a) mHEMT Tx photo (b) mHEMT Rx photo

Fig. 1-6 Sizes of (a) the mHEMT transmitter chip and (b) the mHEMT receiver chip are 4.0 mm × 3.0 mm and 5.5 mm× 3.0 mm, respectively [Herbert, JSSC 2007].

1.3 PACKAGE IN MICROWAVE AND MILLIMETER-WAVE REGIMES – FLIP-CHIP TECHNOLOGY

Generally, bonding is needed for interconnection of integrated circuit packages. Especially at higher frequencies, conventional wire bonding has larger parasitic effects and poor reliability. Thus, the resulting circuit performances degrade. The flip-chip bonding technology [19]-[22] in development plays a more and more important role in the monolithic microwave integrated circuit (MMIC) packages. The flip-chip bonding offers great benefits of negligible parasitic effects and higher reliability thanks to shorter interconnected lines and superior mechanical stability [19]-[21]. Up to present, a microstrip (MS) line is still a classic type utilized in MMICs because of less time consumption in electro-magnetic (EM) simulations and flexible layout in designs. However, the MS is not compatible to the flip-chip technology [7]. Figure 1-7 shows the profile of a MMIC chip mounted on a carrier using flip-chip bonding. For the flip-chip bonding, coplanar waveguide (CPW) or finite-ground coplanar waveguide (FG-CPW) structures are more suitable than an MS because they can offer the smooth transition interface in nature.

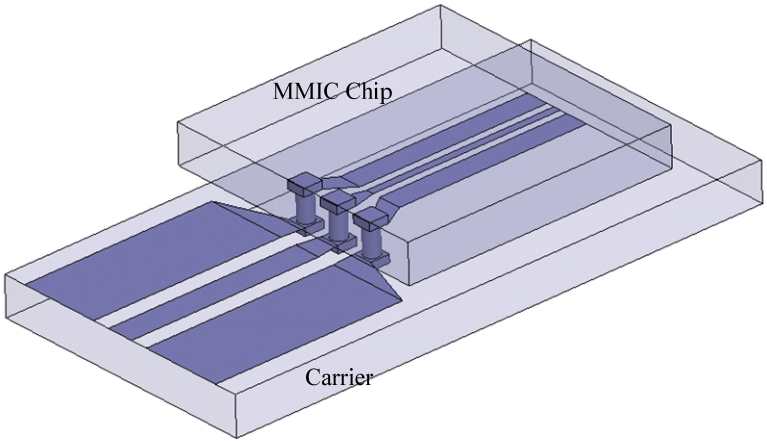


Fig. 1-7 Flip-chip bonding profile of MMIC chip on a carrier.

In a fully integrated MMIC transceiver, the CPW's size is intolerable in the low frequency application while the MS is suitable for the MMIC integration and can be designed with compact size, flexibilities on routing and wafer dicing easily [7]. The process with backside ground can support the MS and CPW designs at the same time. The CPWG type has wide uniplanar ground planes that, along with a back conductor, excite the parallel-plate mode easily [23]-[26]. The parallel-plate mode inducing parasitic resonance can be suppressed by the finite ground or via holes connecting front side ground with backside ground for an electric short. Besides, by adequately using via holes, the CPW mode can transfer easily to the MS mode [27]. Under these considerations, the FG-CPWG type is adopted in Chapter 4. The FG-CPWG in possession of narrow ground planes can eliminate surface wave and leakage effect [24]-[26]. However, the extremely small ground width causes large loss and higher impedance. So, the best design for flip-chip bonding is to optimize ground planes of the FG-CPWG and to overcome drawbacks of the CPW. The FG-CPWG type is hence becoming more and more popular in compact integrated circuits.

1.4 ORGANIZATIONS

Chapter 2 analyzes the accuracy of RC-CR polyphase filters based on GaAs and CMOS technologies and designs pHEMT Gilbert mixers with polyphase filters, which are fundamental, leveled-LO and stacked-LO subharmonic Gilbert mixers. Chapter 3 compares the performances between the pHEMT and mHEMT Q-band subharmonic Gilbert up-conversion mixers. The V-band CPW-MS-CPW two-stage amplifier with flip-chip technology is demonstrated in Chapter 4. Chapter 5 designs and measures the V-band fully integrated mHEMT MMIC receiver. In Chapter 6, the Ka-band divide-by-2 Miller divider with quadrature outputs using pHEMT technology is depicted.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Chapter 2 Ka/Ku-Band PHEMT Gilbert Mixers With Polyphase and Coupled-Line Quadrature Generators

2.1 INTRODUCTION

Recently, increased attention has been paid to complex mixers in modern wireless systems. Complex mixers with both in-phase and quadrature-phase mixing are employed to image rejection mixers and single-sideband (SSB) up-converters. The RC-CR polyphase filters [28]-[32] are used to generate the differential quadrature signals needed by complex mixers and subharmonic mixers. However, the RC-CR polyphase filters in CMOS and SiGe HBT technologies were realized below 2 GHz because it is difficult to fabricate accurate, small resistors and capacitors at high frequencies due to the Si substrate parasitic effect [30]. Even with electronic tuning, the complex Gilbert mixers based on the silicon technology can function at up to 6 GHz and the uncalibrated sideband rejection of the SSB Gilbert mixer at 6 GHz is 48.2 dB [31], [32]. On the contrary, the GaAs-based technology has accurate thin film resistors, metal-insulator-metal (MIM) capacitors and no parasitic substrate effect. Thus, the resistors and capacitors required for the polyphase filter can be implemented in a precise way. The high accuracy in GaAs-based thin film resistors comes from the in-situ film thickness monitor during processing. A 5 GHz complex mixer with accurate RC-CR polyphase filters has been realized in GaInP/GaAs HBT technology, but the performance is limited by the GaInP/GaAs HBT device due to its low ft [33]. At high operating frequencies, a quadrature coupler is another good choice for complex mixers. Nevertheless, the silicon-based coupler has a poor quality factor and bad magnitude balance at high frequencies. The 5.9 GHz CMOS I/Q subharmonic

mixer with a quadrature coupler and transformers at the RF path reveals a large magnitude mismatch in the output waveforms [34].

The subharmonic Gilbert mixer also plays an important role because the LO frequency of a subharmonic mixer is only half of the fundamental mixer's LO frequency. This can solve the problem associated with generating LO signals at high frequencies. However, at high LO frequencies, the transistor time delay destroys the frequency doubling mechanism in the LO stage, so that the LO speed and the RF-to-IF isolation degrade [35]. Thus, a time-delay compensator is proposed at the stacked-LO stage to improve the performances of the subharmonic Gilbert mixer in this Chapter. This time-delay compensated subharmonic Gilbert mixer is reformed based on the previous work [35] to reduce the amount of transistors and to balance the current density of the transistors at the current commutating stages.

The low breakdown voltage in the advanced silicon technology makes the analog circuit design approach difficult. Thus, GaAs-based pHEMT technology with a high cut-off frequency, high breakdown voltage and semi-insulating substrate becomes the technological choice for high-frequency complex Gilbert mixers and subharmonic Gilbert mixers. So far, very few papers on Gilbert mixers incorporating HEMT technology have been published [36]-[39]. The 0.15-μm pHEMT technology employed has an 85-GHz ft and 10-V breakdown voltage. The high-performance active devices and precise passive components are utilized to realize several typical pHEMT Gilbert up- and down-converters, which are fundamental, leveled-LO and stacked-LO subharmonic Gilbert mixers. In Section 2 part 1, Monte Carlo simulations are employed to verify that the polyphase filter on the GaAs substrate has better accuracy than that on the silicon substrate. In Section 2 part 2, the S-matrices of the two types of differential quadrature coupled-line generators are analyzed for our Gilbert mixer at an

RF port. In Section 2 part 3, the novel time-delay compensator, which cancels the phase error, is explained. From the experimental results, polyphase filters and 90˚/180˚ passive couplers used at the LO and RF stages are suitable for applications in the microwave and millimeter-wave regimes. A 15-GHz Ku-band pHEMT SSB complex Gilbert up-converter of 63-dB sideband rejection is realized in Section 3 part 1. A 34-GHz quadrature RF subharmonic down-converter with I/Q outputs is successfully demonstrated in Section 3 part 2 and a 40-GHz stacked-LO subharmonic mixer with a novel compensation technique is represented in Section 3 part 3.

2.2 Component Design of Millimeter- Wave Gilbert Mixer With Quadrature Features

2.2.1 Polyphase Filter Design Using Monte Carlo Simulation for GaAs and CMOS Technologies

There are two common methods to design a quadrature generator—one is a polyphase filter and the other is a coupler. A polyphase filter is composed of sequential resistor-capacitor (R-C) and C-R components. The one-stage RC-CR polyphase filter is only designed at a center frequency and usually many stages are cascaded to tolerate mismatch errors. A two-section polyphase filter is shown in Fig. 2-1. This topology can generate balanced quadrature signals with equal amplitude at 0°, 90°, 180°, and 270° when R and C values are designed at the desired frequency $\omega=1/(RC)$. The two-stage polyphase filter has lower sensitivity to process variations than a one-stage. Thus, the two-stage polyphase filter is adopted in our mixer design to achieve optimum trade-offs in terms of magnitude balance, phase error, loss, and layout size.

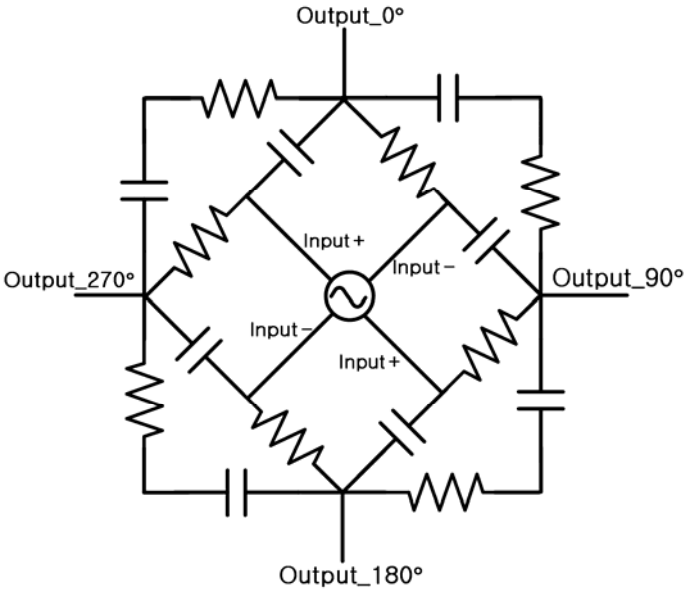


Fig. 2-1 Two-section RC-CR polyphase filter structure.

In the GaAs pHEMT technology, the Tantalum Nitride (TaN) thin film resistors and metal-insulator-metal (MIM) capacitors possess a sheet resistance of 50 Ω/sq ± 2 % and a unit capacitance of 0.4 fF/μm2 ± 10 % [7], respectively. On the other hand, the

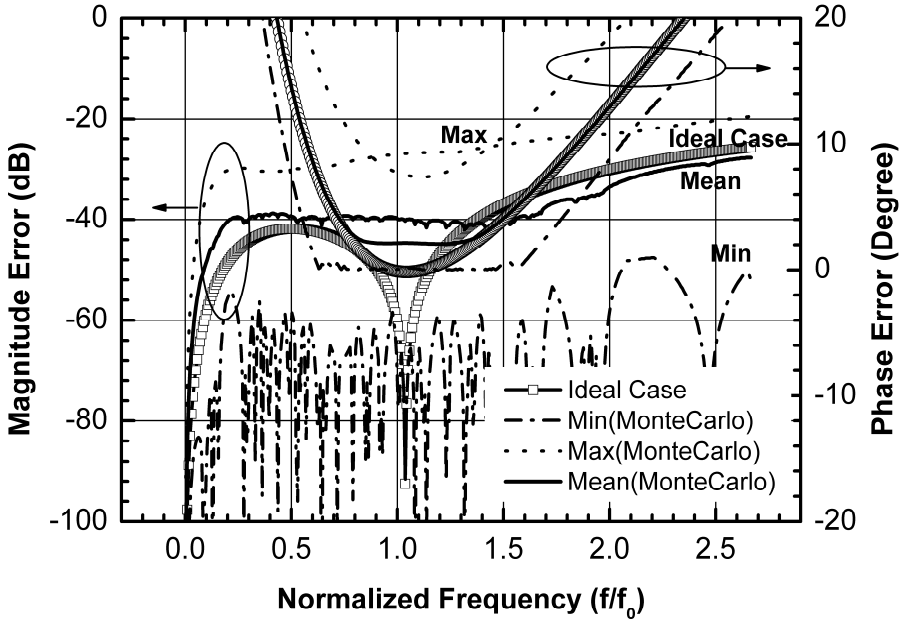


Fig. 2-2 Magnitude and phase errors of the two-section polyphase filter by Monte Carlo simulations with resistance and capacitance variations.

poly resistors and MIM capacitors in the TSMC 1P6M 0.18-μm CMOS technology have 7.58 Ω/sq ± 25 % and 1 fF/μm2 ± 15 %, respectively. Compared with the silicon-based technology, the semi-insulating GaAs-based HEMT process has better accuracy for passive components. The in-situ film thickness monitor in the thin-film resistor fabrication enhances resistance accuracy. According to Monte Carlo simulations with process variations, the maximum phase mismatch of 7° and magnitude error of -28 dB in a two-section GaAs-based polyphase filter for the worst case are shown at the desired frequency, f_0, in Fig. 2-2. Figure 2-3 describes the rejection ratio of the two-stage polyphase filters between the silicon-based and GaAs-based technologies using Monte Carlo simulations with resistance and capacitance variations. The formula for the sideband and image rejection ratios is expressed as

$$\text{Rejection ratio (dB)} = 10\log\left\{\frac{(1+\chi)^2+2(1+\chi)\cos\theta+1)}{(1+\chi)^2-2(1+\chi)\cos\theta+1}\right\} \quad (1)$$

with the function of amplitude (χ %) and phase (θ degree) errors [7]. The mean rejection ratio of the GaAs-based polyphase filter reaches 34 dB, but there is only a 24-dB rejection ratio for the silicon-based counterpart. A 60-dB rejection ratio can be achieved in the ideal case.

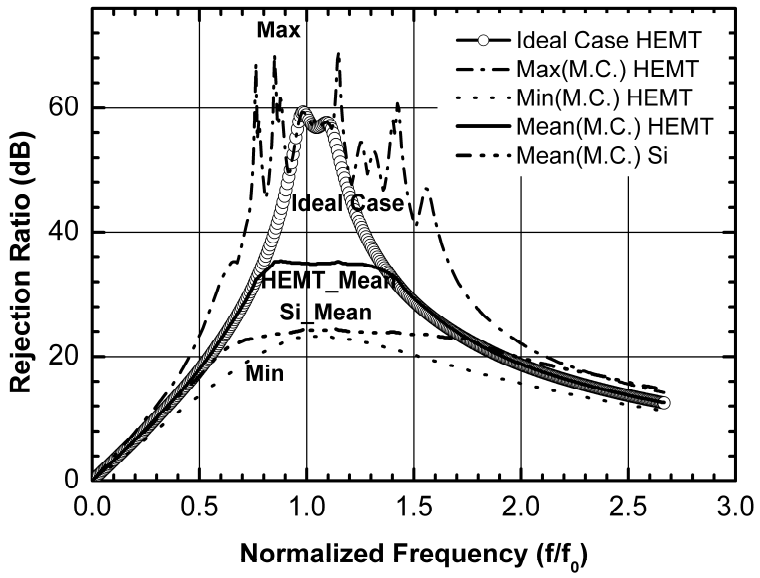


Fig. 2-3 Rejection ratio of Si- and GaAs-based polyphase filters by Monte Carlo simulations.

2.2.2 Performance Analysis of Differential Quadrature Coupled-Line Generator

The passive RC-CR polyphase filter is more suitable for applications below 30 GHz while a quadrature coupler consumes formidably large sizes at lower frequencies. However, as the operating frequency becomes higher and higher, the polyphase filters are not easily realized due to process limitations, interconnection delays and high driven power requirements, so that a quadrature coupler becomes a preferable alternative. At 30 GHz, a quarter-wavelength coupled line is about 1000 μm. The layout size of a coupler can be further reduced by the spiral shape, and thus a coupler can be easily implemented in the integrated circuits above 30 GHz.

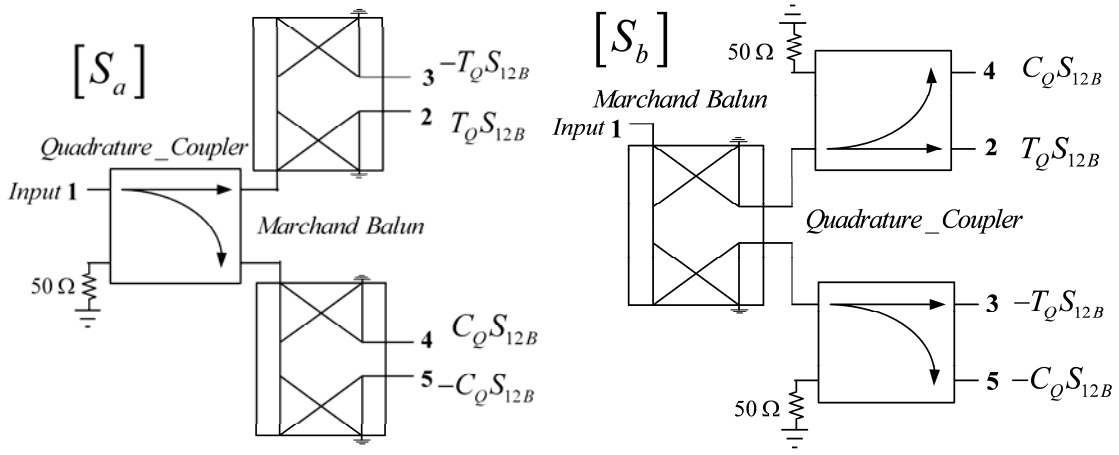
There are two methods to generate differential quadrature signals based on microwave components. One is a quadrature coupler followed by two Marchand baluns and the other is a Marchand balun before two quadrature couplers, as illustrated in Fig. 2-4(a) and (b), respectively. All quadrature couplers are terminated with a 50-Ω resistor at the isolation port. Since the Marchand balun is composed of two

back-to-back quadrature couplers, the first topology has five couplers while the second counterpart has four couplers. As derived in Appendix A, the scattering parameter matrix for each differential quadrature generator is

$$[S_a]=\begin{bmatrix} S_{11B}\left(T_Q{}^2+C_Q{}^2\right) & T_QS_{12B} & -T_QS_{12B} & C_QS_{12B} & -C_QS_{12B} \\ T_QS_{12B} & S_{22B} & S_{23B} & 0 & 0 \\ -T_QS_{12B} & S_{23B} & S_{22B} & 0 & 0 \\ C_QS_{12B} & 0 & 0 & S_{22B} & S_{23B} \\ -C_QS_{12B} & 0 & 0 & S_{23B} & S_{22B} \end{bmatrix} \quad (2.2)$$

and

$$[S_b]=\begin{bmatrix} S_{11B} & T_QS_{12B} & -T_QS_{12B} & C_QS_{12B} & -C_QS_{12B} \\ T_QS_{12B} & T_Q{}^2S_{22B} & T_Q{}^2S_{23B} & T_QC_QS_{22B} & T_QC_QS_{23B} \\ -T_QS_{12B} & T_Q{}^2S_{23B} & T_Q{}^2S_{22B} & T_QC_QS_{23B} & T_QC_QS_{22B} \\ C_QS_{12B} & T_QC_QS_{22B} & T_QC_QS_{23B} & C_Q{}^2S_{22B} & C_Q{}^2S_{23B} \\ -C_QS_{12B} & T_QC_QS_{23B} & T_QC_QS_{22B} & C_Q{}^2S_{23B} & C_Q{}^2S_{22B} \end{bmatrix}, \quad (2.3)$$



(a) (b)

Fig. 2-4 Differential quadrature generator consists of (a) one coupler with two baluns or (b) one balun with two couplers.

with the coupling coefficient (C_Q) and through coefficient (T_Q) of the coupler and the S parameters (S_{11B}, S_{12B}, S_{22B} and S_{23B}) of the Marchand balun as defined in the Appendix. Obviously, these two combinations produce the same differential quadrature outputs. The input return loss of the first type is improved by the factor of ($T_Q^2+C_Q^2$) in comparison with the second counterpart because the reflected power caused by the impedance mismatch between the coupler and balun can be absorbed totally at the isolation port of the coupler. This design approach is commonly used in balanced amplifiers. In the first structure, the two Marchand baluns do not interfere with each other since $S_{24(42)}$, $S_{25(52)}$, $S_{34(43)}$ and $S_{35(53)}$ are equal to zero.

In this Chapter, the structure of the coupler followed by two Marchand baluns is employed at the RF input stage and connected with common-gate-configured transistors with 50-Ω input impedance. The ac grounded terminals in the Marchand balun can be used as the dc grounds for the common-gate-configured transistors [37]. Thus, this structure does not need to add an auxiliary ac choke and an auxiliary dc blocking capacitor to separate the ac signal and dc bias of the mixers. The layout size can also be reduced by the first topology because of no extra biasing components

2.2.3 Stacked-LO Subharmonic Gilbert Cell With Time-Delay Compensation

A transistor has a finite time delay between the output drain current and input gate voltage. The I-V transfer function of a transistor can be expressed by the gate-source voltage, the drain-source voltage, and the time delay τ. When the gate-source port of a transistor is fed by a step voltage function, the output drain shows up after the phenomenological time delay τ, which is generally one-third of the transistor transit-time delay. Thus, the adiabatic approximation for I-V characteristics is used when the operating frequency is much slower than the inversion of the time delay τ

($\omega \ll \frac{1}{\tau}$) [28]. However, the time delay problem can not be ignored when a mixer operates at higher frequency.

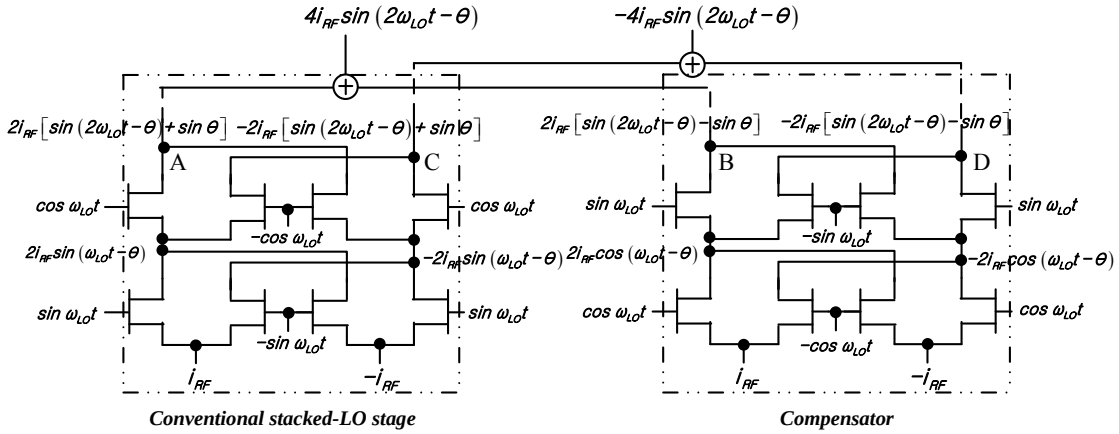


Fig. 2-5 Time-delay (θ) compensation analysis for the compensated stacked-LO subharmonic mixer.

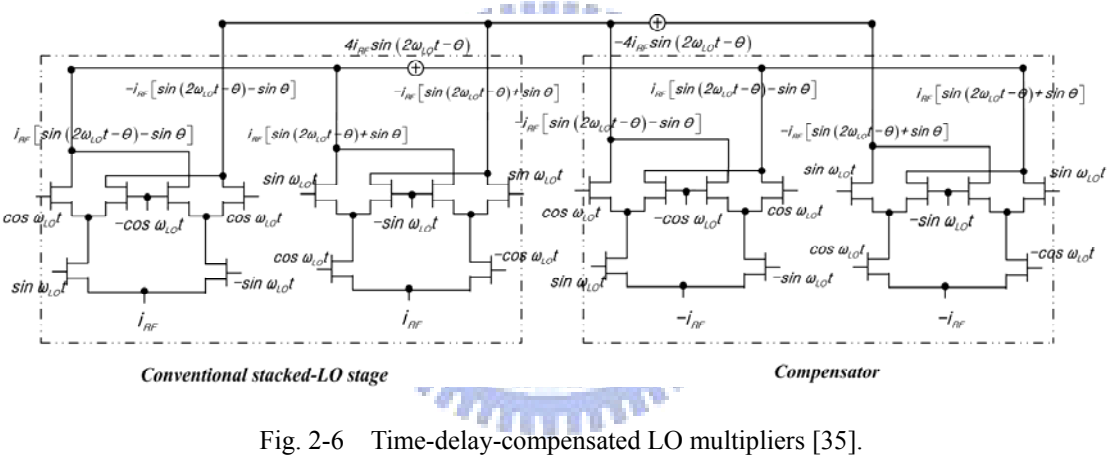


Fig. 2-6 Time-delay-compensated LO multipliers [35].

A conventional stacked-LO subharmonic Gilbert mixer is shown in Fig. 2-5. The stacked-LO stage provides a frequency doubling mechanism when differential quadrature LO signals are applied. Thus, the mixer outputs are $2sin(2\omega_{LO}t)i_{RF}$ and $-2sin(2\omega_{LO}t)i_{RF}$ at nodes A and C, respectively. However, the finite transistor delay, $\theta = \omega\tau$, which is pronounced at high frequencies, introduces the extra dc term, $sin(\theta)$ at nodes A and C. This dc offset problem makes the LO speed of a conventional stacked-LO subharmonic Gilbert mixer slow and degrades the RF-to-IF isolation. A novel time-delay compensated subharmonic Gilbert mixer is proposed and analyzed in

Fig. 2-5. The time-delay compensator is employed at the stacked-LO stage to improve the LO speed and isolation of the subharmonic Gilbert mixer. The upper/lower LO stages of the conventional stacked-LO stage and compensator are fed with (I+,I-)/(Q+,Q-) and (Q+,Q-)/(I+,I-) signals, respectively. The nodes A and C of the conventional stacked-LO stage connect with the nodes B and D of the compensator, respectively, and as a consequence the component ($\pm 2 i_{RF} sin(\theta)$) is cancelled. Only the $\pm 4 sin(2\omega_{LO}t-\theta) i_{RF}$ signal is available at the outputs. Further, for the purpose of enhancing the LO speed, the upper and lower LO stages can use the smallest transistors with a width of 2×15 μm, which is limited by air-bridge fabrication, to obtain the same high current density.

The time-delay compensated LO multiplier shown in Fig. 2-5 is an improved version of the first proposed one as shown in Fig. 2-6 [35]. It is evident that both time-delay-compensated mixers have the identical mathematical functions. The mixer intrinsic response depends on the transistor cut-off frequency, which is determined by the current density. On the other hand, the mixer extrinsic response caused by the device capacitance is limited by the device size. The current density and device size are optimized for the improved version because the switching pairs of the lower- and upper-LO are identical as shown in Fig. 2-5. Thus, the improved version has the advantages of higher speed, smaller size and less power consumption.

2.3 MILLIMETER-WAVE UP- AND DOWN-CONVERTER DESIGNS AND MEASURED RESULTS

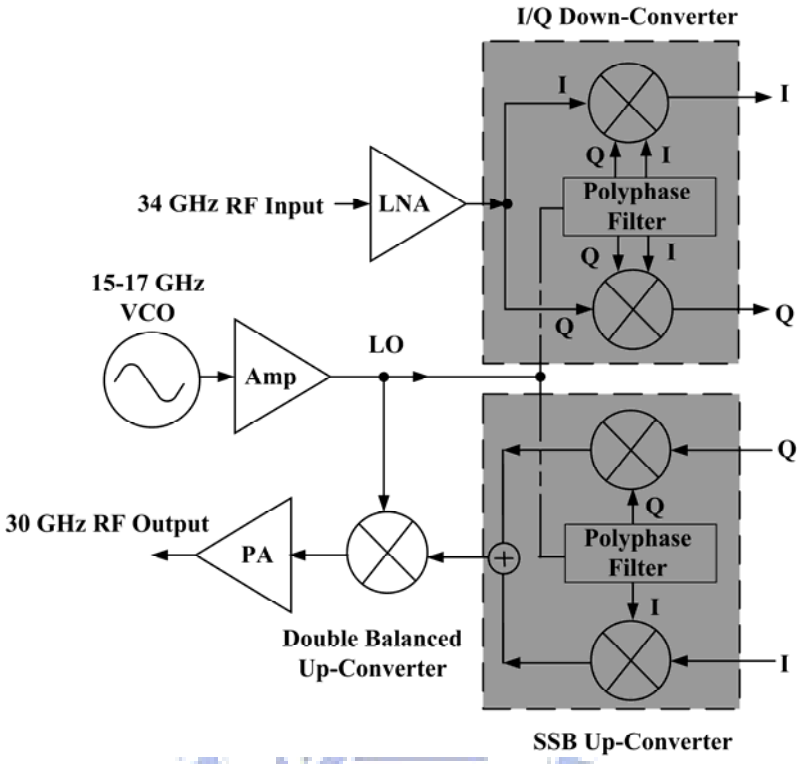


Fig. 2-7 Simple block diagram of a Ka-band system.

Figure 2-7 shows the block diagram and frequency planning of a Ka-band system. The circuits in the shaded area are implemented in this Chapter. The polyphase filters needed for both transmitting and receiving are designed around 15 GHz thanks to the semi-insulating GaAs substrate. The received signal is amplified by an LNA and then sequentially down-converted to 200 MHz by the 34-GHz I/Q subharmonic mixer. The LO frequency works at only half an RF frequency for the subharmonic mixer to reduce the effects of DC offset and self-mixing. Dual conversion is employed in the transmitter chain. A quadrature IF input is first up-converted to 15 GHz by the 15-GHz SSB up-converter and subsequently up-converted to 30-GHz by a double balanced fundamental up-converter. The simple 30-GHz double balanced up-converter has equal

LO and IF frequencies. Thus, the undesired sideband signal is around dc and can be eliminated by the front-end circuits and antenna [40]. The proposed frequency planning has its merit because all the mixers in Fig. 2-7 share the same voltage control oscillator (VCO) of 15 - 17 GHz to reduce the complexity. In addition, the VCO operated at low frequency consumes less power than the one operated at high frequency.

As mentioned above in Section 2, the polyphase filter, quadrature coupler, and compensation technique have their own advantages in the up- and down-conversion mixers. In this section, all the implemented mixers adopt the two-section polyphase filter at the LO stages. The predictions of the RF output return loss of the up-converter and the input RF return loss of the down-converter by simulations are accurate because precise passive components can be built on the semi-insulting GaAs substrate. A pHEMT device reaches the maximum transconductance when the fully transfer of electrons from the low mobility donor layer to the high mobility channel layer occurs. The gate terminal controls the two-dimensional electron gas (2-DEG) channel at the hetero-junction interface when a more negative gate voltage is applied. The abrupt charge transfer renders the pHEMT device characteristics sensitive to the process variation and thus makes the circuit prediction from the given active device model inaccurate. Passive components and all of the high-frequency routings are simulated by an EM simulator. The distance between high-frequency routings is kept at least 25 μm to avoid line-to-line coupling effects. The symmetry in the circuit is well preserved in layouts by keeping the symmetrical paths equal length to suppress the phase mismatch. The sideband rejection in the SSB up-converter and I/Q IF waveforms in the I/Q down-converter are the best vehicles to verify the overall quadrature accuracy. 63-dB single sideband rejection is achieved for the 15-GHz SSB up-converter. The

leveled-LO subharmonic I/Q down-converter at 34 GHz has < 0.4-dB magnitude and < 1° phase errors in the output waveform. The advantage of combination of analog and microwave circuit design methodology in HEMT technology is evident. The fabricated pHEMT mixers for high-frequency applications are measured by on-wafer testing.

2.3.1 15-GHz Up-Conversion Mixer With 63-dB Sideband Rejection

Figure 2-8 shows the functional block diagram of a double-quadrature single-sideband (SSB) up-converter. The SSB output expression, i.e. $cos(\omega_{LO}t+\omega_{IF}t)$, is derived and explained straightforwardly in Fig. 2-8. Quadrature IF signals and quadrature LO signals are needed in the SSB up-converter. The SSB up-converter in Fig. 2-9 includes an LO polyphase filter, two fundamental analog multipliers, IF active baluns, and a current combiner with the matching network for the RF output. The two analog multipliers are two double balanced Gilbert mixers, which are composed of Gilbert cells (M_5~M_8 and M_9~M_{12}), IF input stages (M_{13}~M_{16}) and current sources (M_{17} and M_{18}). The source resistors are used for self-biasing the current sources because only the depletion mode pHEMT devices are available. The self-biasing technique had been utilized in amplifiers [41]. The differential quadrature signals needed by the Gilbert cells are generated by applying the differential signals to the two-stage polyphase filter.

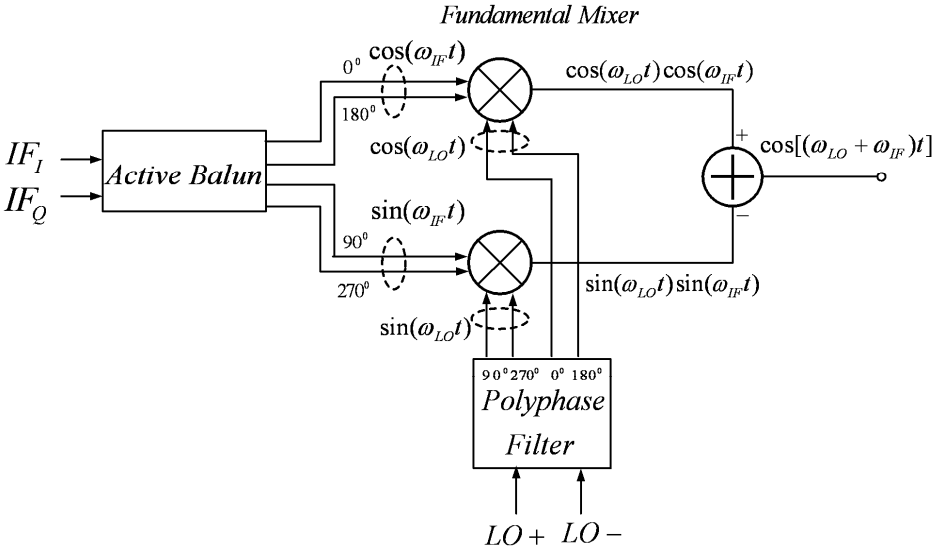


Fig. 2-8 Block diagram of an SSB up-converter.

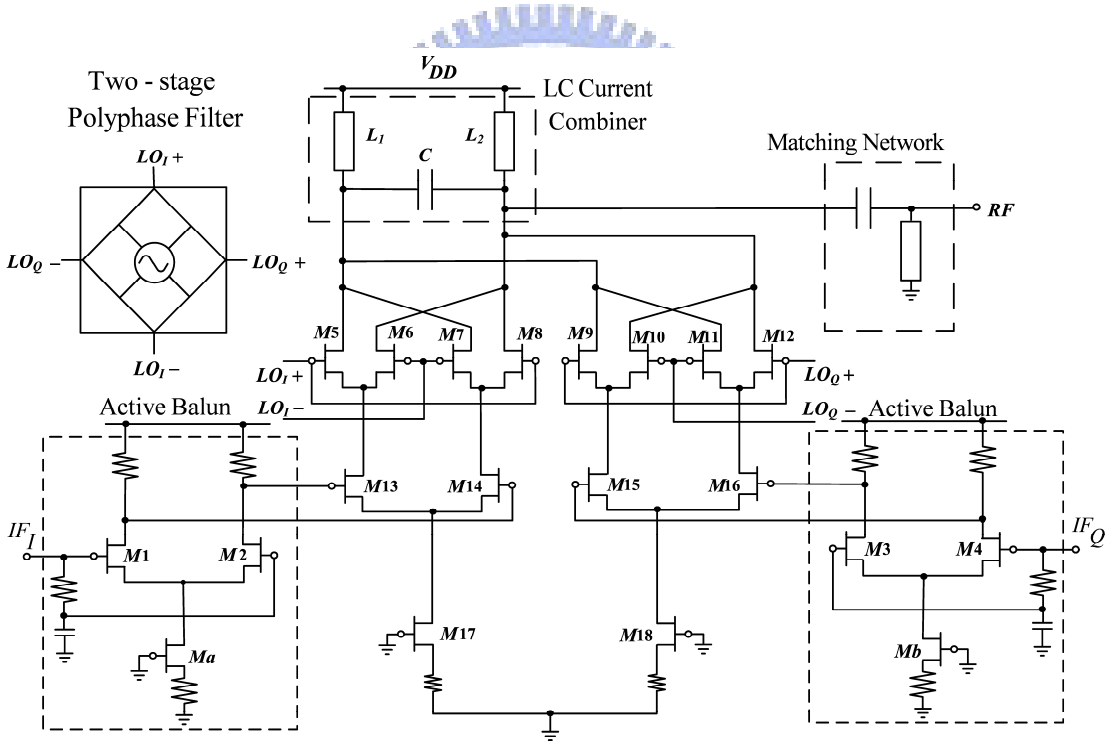


Fig. 2-9 Circuit topology of a 15-GHz SSB up-conversion mixer using depletion mode AlGaAs/InGaAs pHEMT technology.

The input quadrature IF signals are transformed to the differential quadrature signals via the IF active baluns. These active baluns are employed to generate two IF

signals with balanced magnitude and opposite phase. The IF active balun is intentionally designed with low gain in order to not limit the gain compression point. In addition, when compared with the passive baluns, the active baluns can save much valuable real estate in the IC technology at low IF frequencies.

Two inductors, L_1 and L_2, and a capacitor, C, form an LC passive current combiner designed at $\omega = \sqrt{1/(2L_{1,2}C)}$. The purpose of the LC current combiner is to transform the differential output of the Gilbert mixer into the single-ended output while doubling the current gain [42]. In general, the performance of a passive LC current combiner at higher frequencies is superior to an active current mirror load because an active current mirror has a limited output voltage swing and cannot respond rapidly at higher frequencies. Furthermore, a passive LC current combiner possesses higher linearity. The microstrip line inductor has a good quality factor because the GaAs-based technology owns the backside ground plane and semi-insulating substrate. On the other hand, the high quality microstrip line inductor cannot be realized in the Si-based technology due to the lack of the backside ground plane and the lossy silicon substrate.

Figure 2-10 displays the micrograph of the fabricated chip in Fig. 2-9. The layout is kept as symmetric as possible and the IF_I and IF_Q inputs are located on opposite sides for the sake of symmetrical considerations. A ground-signal-ground (GSG) IF_I input is on the right-hand side, a GSGSG LO pad is on the top, and an IF_Q input and RF output GSGSG pad is on the left-hand side. The chip size is 1.4 × 0.9 mm^2 including pads. The supply voltage and current for the mixer cores are 4.8 V and 18 mA, respectively.

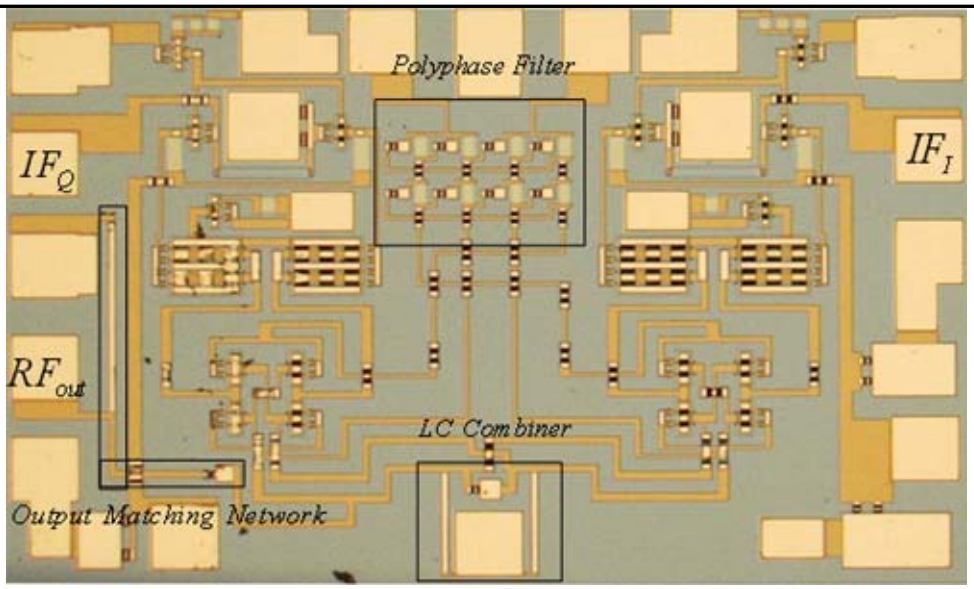


Fig. 2-10 Micrograph of a 15-GHz pHEMT SSB Gilbert up-converter.

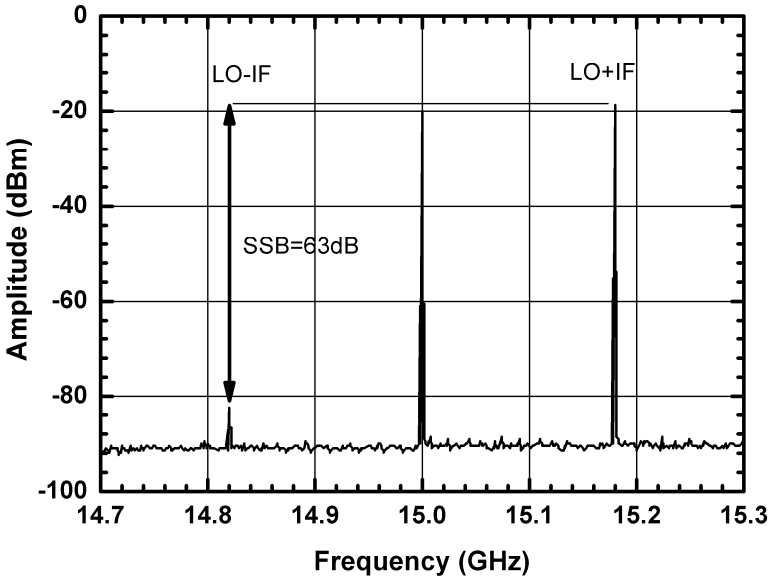


Fig. 2-11 SSB suppression performance of the pHEMT SSB Gilbert up-converter. 63-dB sideband rejection is achieved.

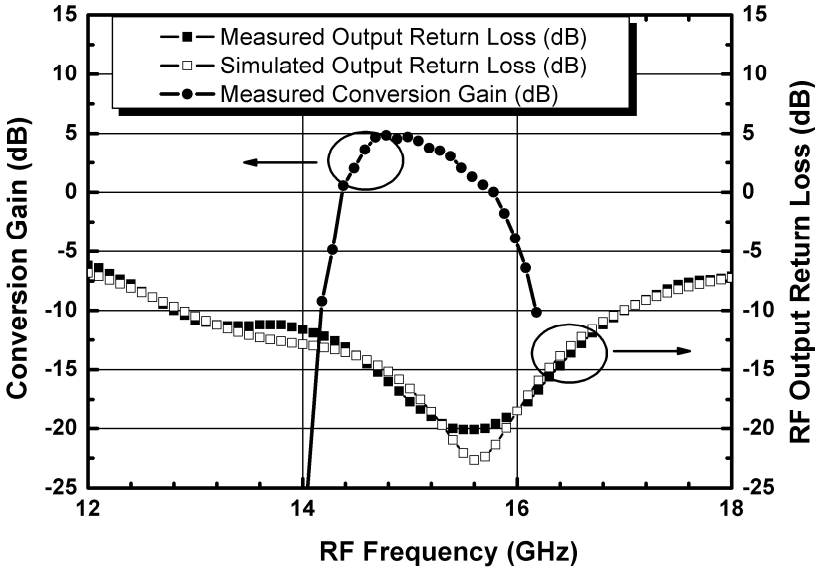


Fig. 2-12 Measured and simulated RF output return loss and measured conversion gain of the pHEMT SSB Gilbert up-converter.

When IF_1 = 0.18 GHz and LO = 15 GHz, the conversion gain keeps a constant of 5 dB for LO input power from 10 dBm to 20 dBm. The sideband rejection ratio of the SSB up-converter is shown in Fig. 2-11. The sideband rejection ratio is defined as the power ratio between the wanted and unwanted signals. We have achieved a 63-dB sideband rejection ratio in this study.

The simulation and measurement of the RF output return loss are shown in Fig. 2-12. The output return loss is determined by the LC current combiner and the output matching network because the impedance looking into the output of the commutating Gilbert mixer cell is high. The simulated curve of the RF output return loss is close to the measured curve. The RF output return loss is better than 10 dB from 12.8 GHz to 17 GHz and 20 dB between 15.4 GHz and 15.8 GHz. The measured conversion gain versus RF frequencies is also illustrated in Fig. 2-12. The experimental RF 3-dB bandwidth is about 1 GHz in the RF frequency range of 14.4 GHz to 15.4 GHz and is limited by the LC current combiner and the associated output matching network. Meanwhile, the LO-to-RF isolation is better than 31 dB for 14.7~15.2-GHz LO

frequencies and the IF-to-RF isolation is above 50 dB for 0.1~0.4-GHz IF frequencies. The output power performances of an SSB up-converter are displayed in Fig. 2-13. The measured OP_{1dB} equals -6 dBm and OIP_3 equals 8 dBm while IF_1=0.18 GHz and IF_2=0.28 GHz. The measured data reveal that the SSB up-converter has good linearity because the band-pass LC current combiner is utilized instead of an active low-pass current mirror.

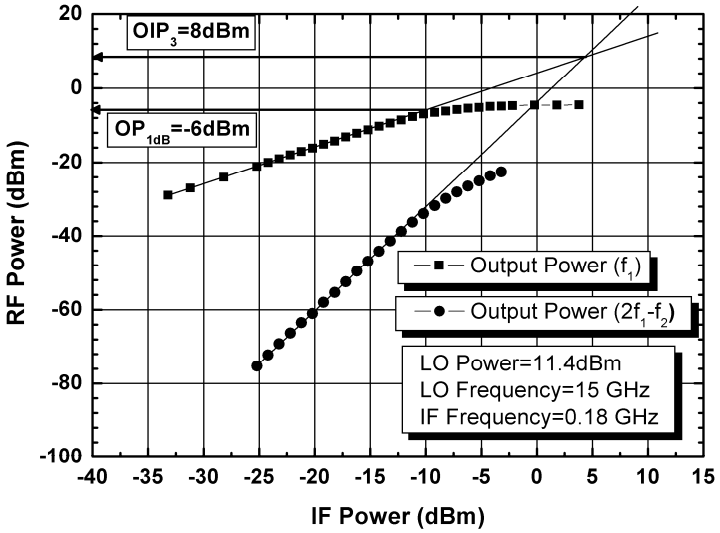


Fig. 2-13 Power performance of the pHEMT SSB Gilbert up-converter when IF_1=0.18 GHz and IF_2=0.28 GHz.

2.3.2 34-GHz Double-Quadrature I/Q Subharmonic Down-Conversion Mixer

The micrograph of a 34-GHz double-quadrature I/Q subharmonic down-converter is shown in Fig. 2-14. The mixer utilizes an area of 2.35 × 1.85 mm^2. This proposed circuit of the leveled-LO I/Q subharmonic down-conversion mixer is employed with the quadrature LO and RF inputs. The quadrature LO signals and differential quadrature RF signals are generated by a two-section polyphase filter and one coupler followed by two Marchand baluns, respectively. The mixer core consists of a leveled-LO subharmonic Gilbert mixer to perform frequency translation, as shown in Fig. 2-15 [28]. The mixer core has 12 mA and the supply voltage is 8V.

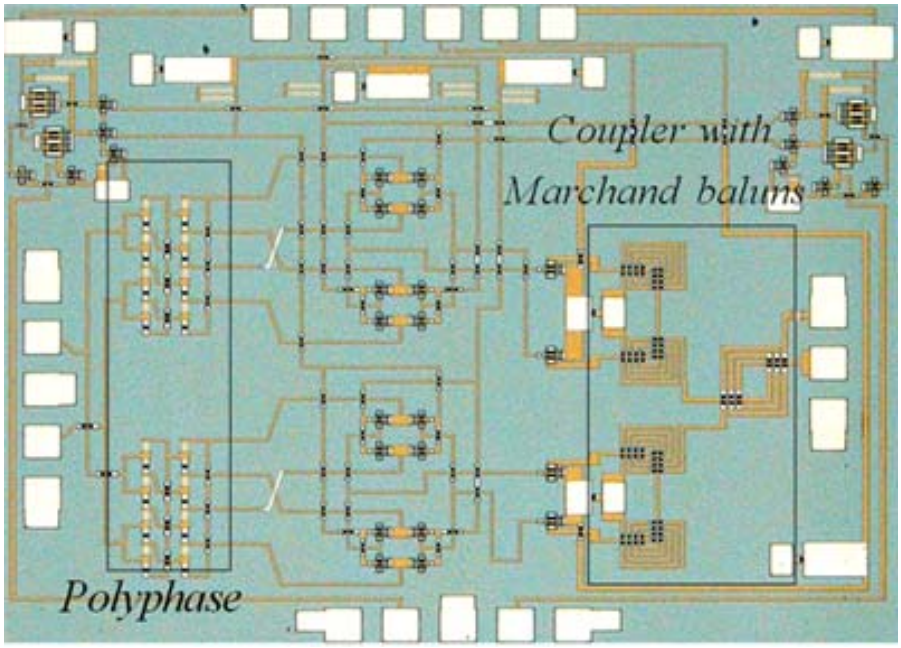


Fig. 2-14 Micrograph of the 34-GHz pHEMT double-quadrature subharmonic Gilbert mixer.

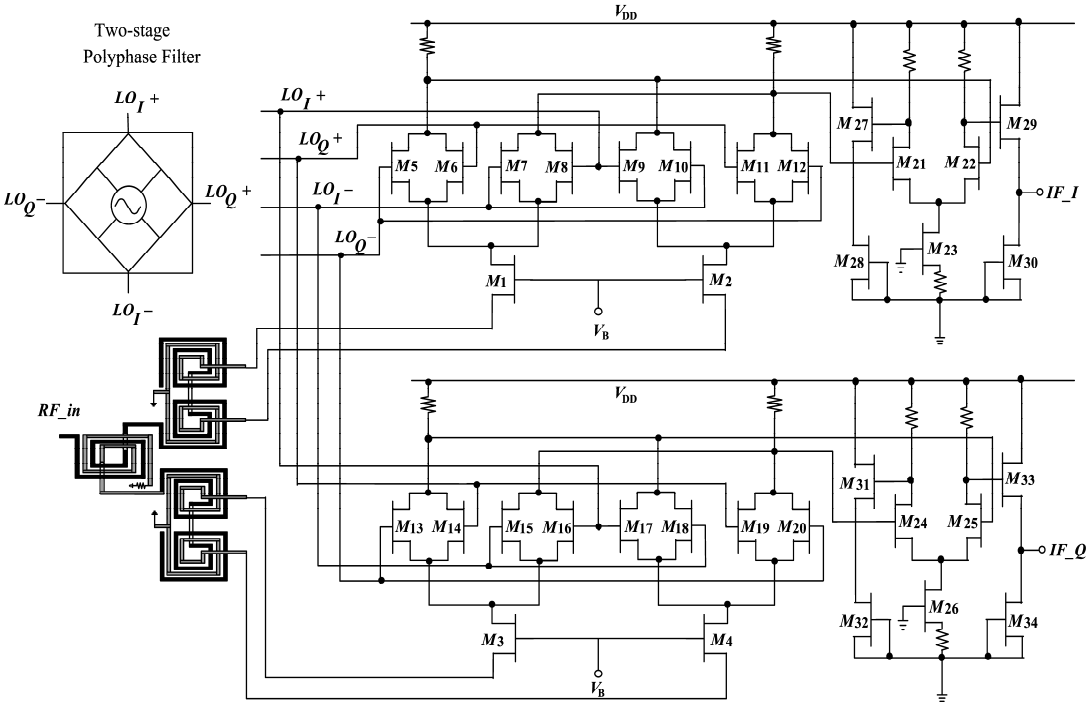


Fig. 2-15 Schematic of the 34-GHz I/Q subharmonic down-conversion mixer.

Figure 2-16 displays the 200-MHz IF_I and IF_Q output waveforms when RF and LO input frequencies are 34.2 GHz and 17 GHz, respectively. The measured performances

have smaller than 1° phase error and 0.4-dB amplitude error limited by the measurement accuracy of ±0.5° phase and ±0.1-dB amplitude errors. Figure 2-17 shows the phase and magnitude errors as a function of frequencies and the I/Q phase error and the output mismatch from 32.5 GHz to 34 GHz are less than 1° and 0.5 dB, respectively. The excellent I/Q performance reveals that the LO R-C polyphase filter as well as the RF coupler and baluns can be implemented precisely on the semi-insulating GaAs substrate and operates well at high frequencies. The two-stage polyphase filter at the LO port has a wider balanced magnitude-and-phase bandwidth than the coupled-line components at the RF port. The differential quadrature signal for feeding the RF port of the mixer is produced by the composite network, which consists of one quadrature coupler and two Marchand baluns. Because the Marchand balun has a wider balanced bandwidth than that of the coupler, the I/Q output difference in conversion gain is mainly affected by the quadrature coupler. The peak conversion gain reaches 4.5 dB for 14~15 dBm LO input power.

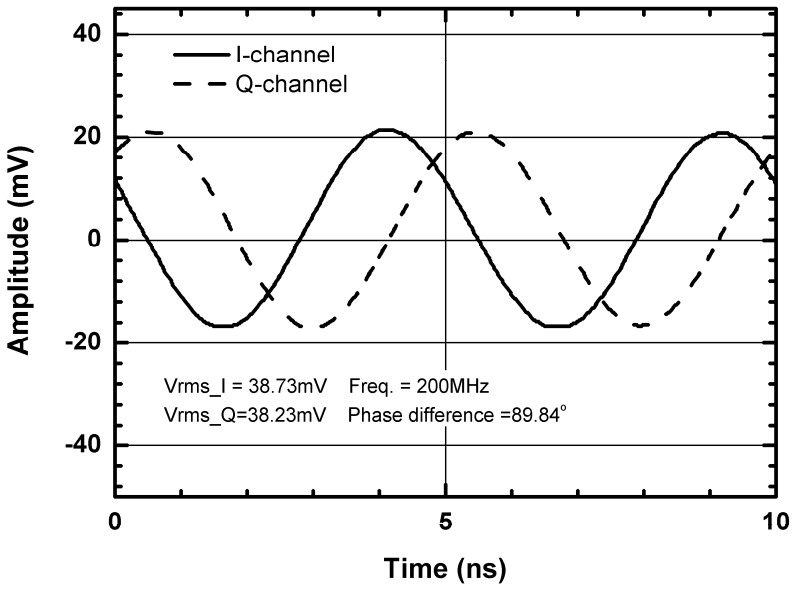


Fig. 2-16 IF output waveforms of the 34-GHz I/Q subharmonic down-converter.

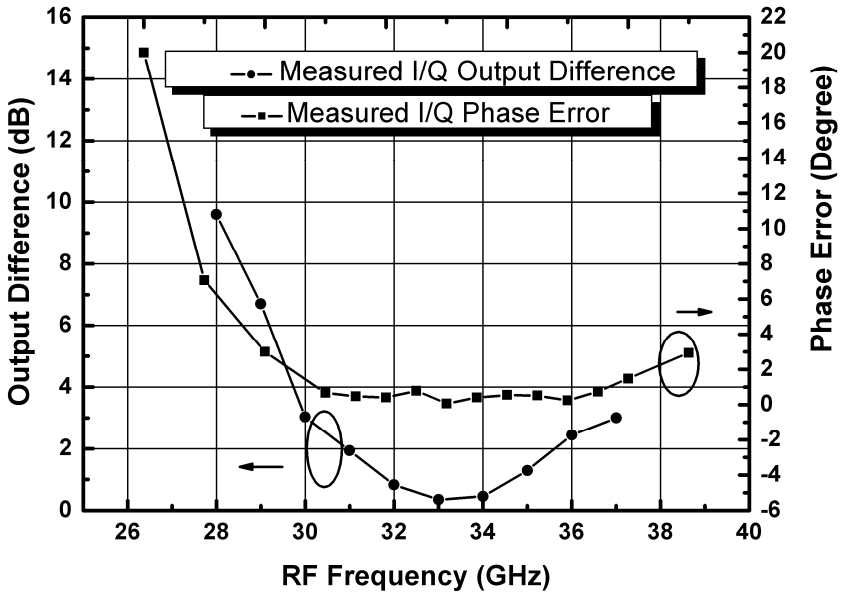


Fig. 2-17 Measured phase error and output difference of the 34-GHz I/Q subharmonic down-converter.

The RF input return loss is simulated and measured in Fig. 2-18 and the RF input return loss is better than 10 dB from 20 GHz to 39.2 GHz. The input matching network of the subharmonic I/Q down-converter shown in Fig. 2-15 consists of a differential quadrature coupled-line coupler and source-port input impedance of the common-gate configuration. The common-gate input impedance is simply a reciprocal of the transconductance for the frequency up to the transistor cut-off frequency, 85-GHz in the employed pHEMT transistor. Thus, the simulated and measured data of the input return loss in the down-converter is very consistent. From 200 MHz to 300 MHz, the measured noise figure (N.F.) is about 24.5 dB, as shown in Fig. 2-18. The 3-dB IF bandwidth is 500 MHz.

Figure 2-19 depicts that the input 1-dB compression point, IP_{1dB}, of the RF signal is -8 dBm while the input third-order intercept point, IIP_3, is 3-dBm. All port-to-port isolations regarding LO leakage are more than 50 dB for 15-GHz to 18-GHz LO frequencies. Meanwhile, LO-to-RF and 2LO-to-RF [43] isolations exceed 60 dB. The

outstanding isolations of the I/Q subharmonic down-converter prevent the self-mixing problem.

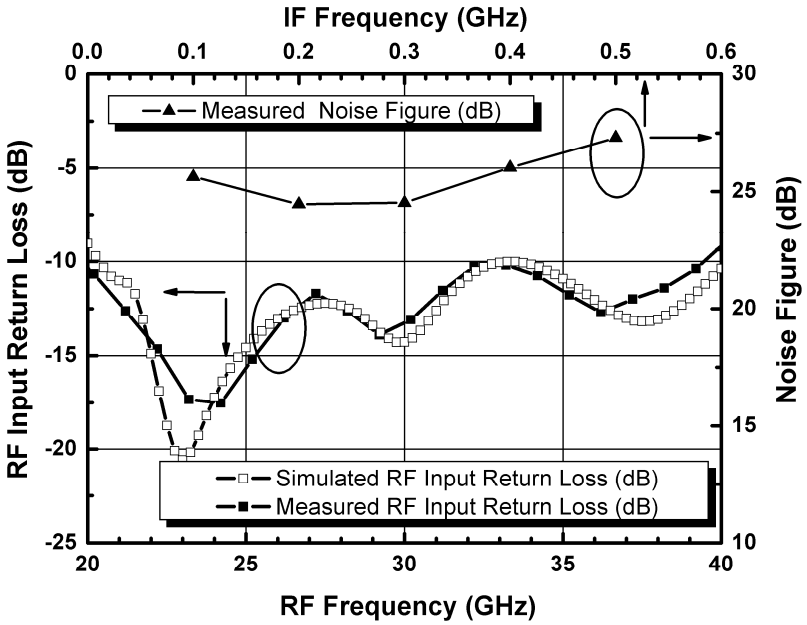


Fig. 2-18 Measured and simulated RF input return loss and measured noise figure of the 34-GHz pHEMT leveled-LO subharmonic Gilbert down-converter.

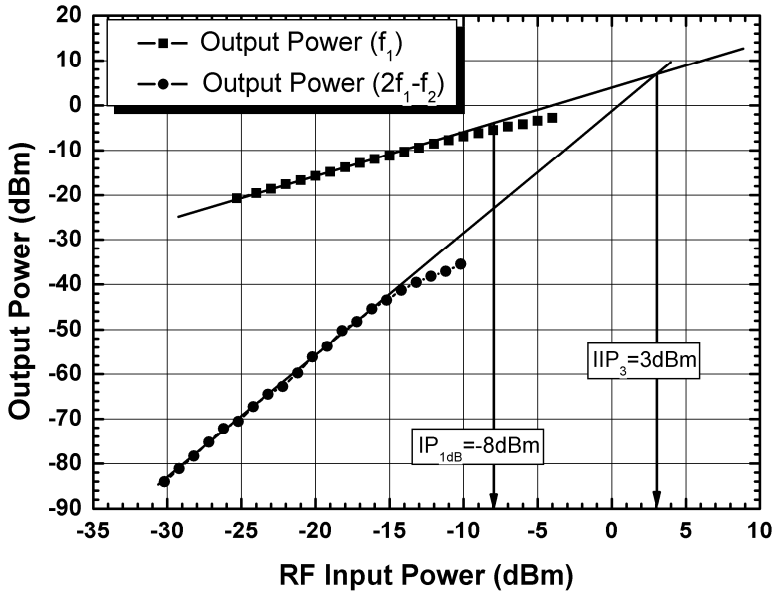


Fig. 2-19 Power performance of the I/Q subharmonic Gilbert down-converter when RF_1=34.1 GHz and RF_2=34.16 GHz.

2.3.3 40-GHz pHEMT Stacked-LO Subharmonic Gilbert Down-Conversion Mixer With Time-Delay Compensation

In order to cancel the dc offset resulting from the transistor delay, the highly symmetrical stacked-LO subharmonic Gilbert mixer is designed with a time-delay compensation technique. This structure not only improves the LO speed but also largely reduces the amount of transistors required as compared with previous work [35].

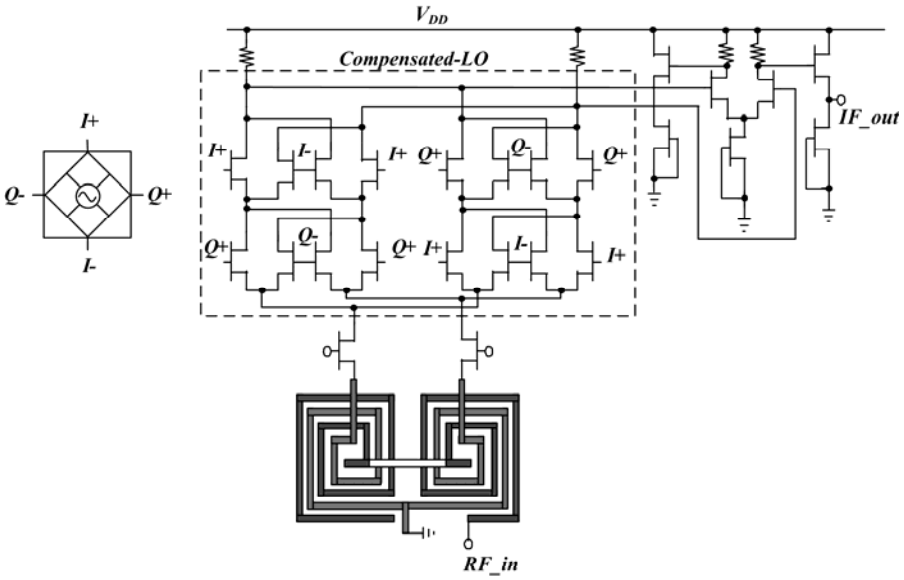


Fig. 2-20 Schematic of the 40-GHz pHEMT stacked-LO subharmonic Gilbert down-conversion mixer with a time-delay compensation technique.

As shown in Fig. 2-20, the 20-GHz R-C polyphase filter is employed at the LO stage when the RF input stage is a common-gate-configured amplifier with a Marchand balun. Here, the common-gate-configured transistors provide an input impedance of 50-Ω for the Marchand balun and hence facilitate the input matching. The fabricated

chip is shown in Fig. 2-21. The chip size is 2.4 mm × 1.9 mm. The microstrip lines connecting a polyphase filter with stacked-LO Gilbert cells are a critical issue, and these microstrip lines are meandered so as to remain equal in length for the phase error reduction of the differential quadrature LO signals. The current consumption of the mixer core is 11 mA at the supply voltage of 8V.

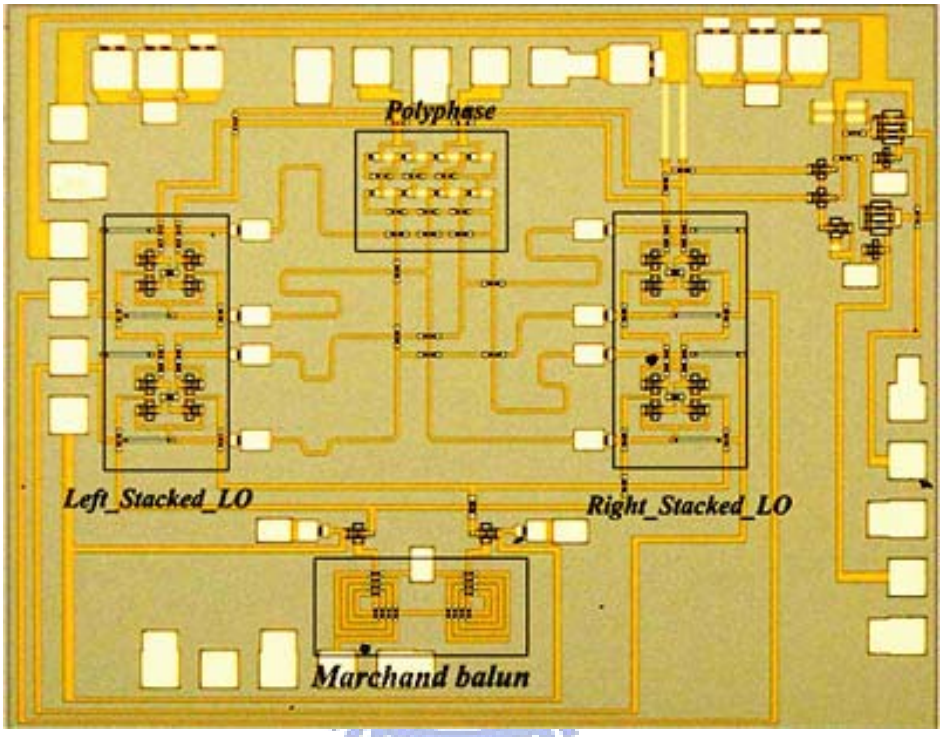


Fig. 2-21 Micrograph of the 40-GHz pHEMT compensated stacked-LO subharmonic Gilbert down-conversion mixer.

The maximum conversion gain of 3.1 dB is obtained from a single-ended IF output at the LO power of 10 dBm, as shown in Fig. 2-22. At the same time, the 3-dB RF bandwidth is about 4 GHz from 37 GHz to 41 GHz. The measured N.F. of the 40-GHz stacked-LO subharmonic down-converter with the time-delay compensation is also shown in Fig. 2-22. The N.F. almost keeps a constant of 18 dB. The 3-dB IF bandwidth is 550 MHz. The LO-to-IF, 2LO-to-IF, LO-to-RF, and 2LO-to-RF [43] isolations are better than 30 dB, 45 dB, 40 dB and 50 dB, respectively. Further, the RF-to-IF

isolation is better than 30 dB. The 1-dB gain compression occurs when the input RF power equals -4.5 dBm and the IIP3 of 10 dBm is achieved, as shown in Fig. 2-23.

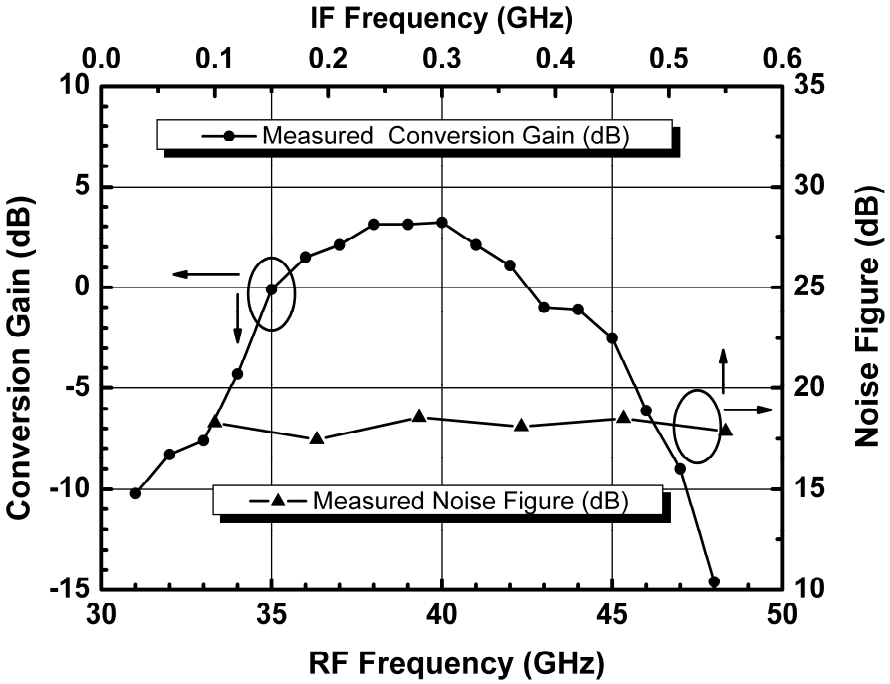


Fig. 2-22 Measured conversion gain and noise figure of the 40-GHz pHEMT stacked-LO subharmonic down-converter.

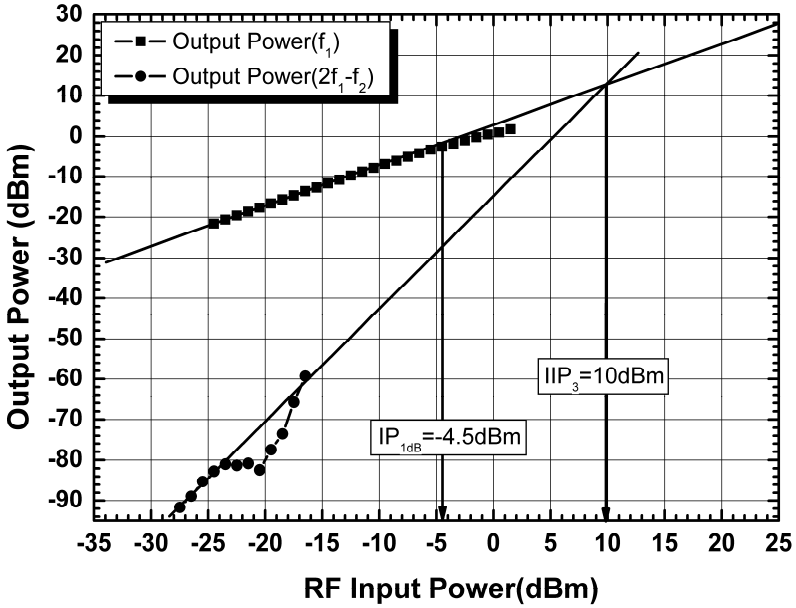


Fig. 2-23 Power performance of the 40-GHz compensated stacked-LO Gilbert down-converter when RF_1=40.101 GHz and RF_2=40.201 GHz.

2.4 SUMMARY

The combination of analog and microwave circuit design approaches has been successfully demonstrated with Ka/Ku-band mixers using 0.15-μm AlGaAs/InGaAs pHEMT technology. The quadrature coupler based on the microwave design methodology is formidably large for operation frequencies below 30 GHz. Thus, the complex mixer can be feasible using the RC-CR polyphase differential quadrature generator. The excellent 63-dB sideband rejection ratio of the 15-GHz SSB up-conversion mixer, and the < 0.4-dB magnitude and < 1° phase errors of the 34-GHz I/Q down-conversion mixer reveal that not only does the LO polyphase filter work accurately, but also the quadrature coupler has good quality on the semi-insulating GaAs-based substrate. Further, the novel time-delay compensator is employed at the stacked-LO subharmonic Gilbert cell to improve the current commutation speed and RF-to-IF isolation. The analog Gilbert mixer design can be further improved by employing mHEMT technology. The 0.15-μm mHEMT has an ft of 110 GHz. On the other hand, passive mixers using the mHEMT and pHEMT technologies have the same conversion loss [10]. The results shed light on the HEMT analog circuit design approach in the millimeter-wave regime.

Chapter 3 Comparison Between Q-Band pHEMT and mHEMT Subharmonic Gilbert Upconversion Mixers

3.1 INTRODUCTION

In this Chapter, two Q-band subharmonic Gilbert upconverters are demonstrated for the first time, to the best of our knowledge, using the mHEMT and pHEMT processes. The experimental results show that the conversion gain of the mHEMT Gilbert mixer is higher than that of the pHEMT mixer and the linearity of the mHEMT mixer is better. Both pHEMT and mHEMT Gilbert mixers possess high port-to-port isolations. The performance comparison between the Q-band subharmonic mHEMT and pHEMT Gilbert upconversion mixers is established in this Chapter. Using the mHEMT technology in the millimeter-wave transceiver, the performance of the amplifier is improved and the active Gilbert mixer also works better. The outcomes offer another choice — the mHEMT analog circuit design approach in the fully integrated millimeter-wave regime.

3.2 MEASURED PHEMT AND MHEMT DC CHARACTERISTICS

The indium mole fraction of 15 - 30% and 40% is held for pHEMT and mHEMT devices provided by the standard foundry process [44]. In Fig. 3-1, the measured dc transconductance (g_m) and drain current (I_{ds}) are plotted as a function of gate voltage with V_{ds}=1.5V for the 0.15 μm pHEMT and mHEMT, respectively. The gm peaks around V_{gs}= -0.4 V with a value of 467 mS/mm for the pHMET transistor and the mHEMT has a maximum g_m of 616 mS/mm at V_{gs}= -0.1 V, respectively. At V_{gs}= 1.0 V, the pHEMT and the mHEMT have a maximum drain current of 691 mA/mm and

660 mA/mm, respectively.

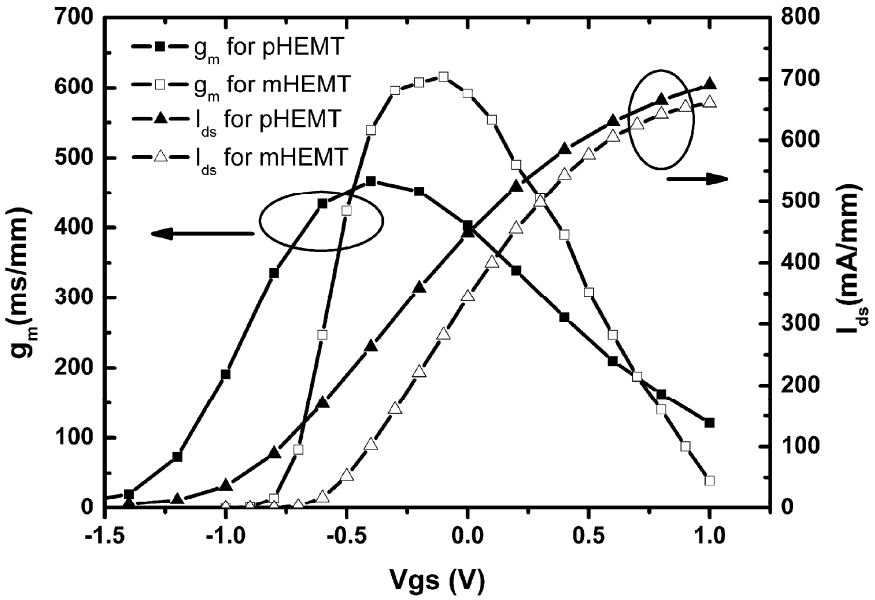


Fig. 3-1 Measured drain-to-source current (I_{ds}) and tranconductance (g_m) with respect to gate-to-source voltage for both pHEMT and mHEMT.

3.3 CIRCUIT DESIGN

The Q-band stacked-LO subharmonic Gilbert upconversion mixer structure is shown in Fig. 3-2. The stacked-LO subharmonic mixer is composed of the switching-pairs (M_1-M_2, …, M_7-M_8), the transconductance-pair (M_9-M_{10}) and the current source (M_{11}). The RF output port uses a LC current combiner with a matching network [42]. Short high impedance transmission lines are used as inductors at high frequencies in the LC current combiner. The LO input port adopts a two-section RC-CR polyphase filter. The quadrature LO generated by a polyphase filter for the subharmonic mixer is needed. The cascade stages of a polyphase filter can reduce phase and magnitude errors while accurate implementations of resistance and capacitance on semi-insulating GaAs substrate result in the high precise quadrature outputs of the polyphase filter [28]. The output ports of the two-section polyphase filter connect with dc-blocking capacitors and large rf-choking resistors in order to

isolate ac signals and dc biases. The device size of the current source (M_{11}) is 2 × 15 μm and a resistor connects the M_{11} source port for the self-biasing technique.

We employ 0.15-μm mHEMT and pHEMT technologies to demonstrate Q-band subharmonic Gilbert mixers. For both mixers, the size of the transistors remains almost the same and the input transistors are biased at the maximum transconductance condition. Moreover, the two layouts of the pHEMT and mHEMT mixers remain nearly alike. The effect of complicated layout must be considered as a part of the mixer design and the line-to-line coupling effects have to be greatly alleviated.

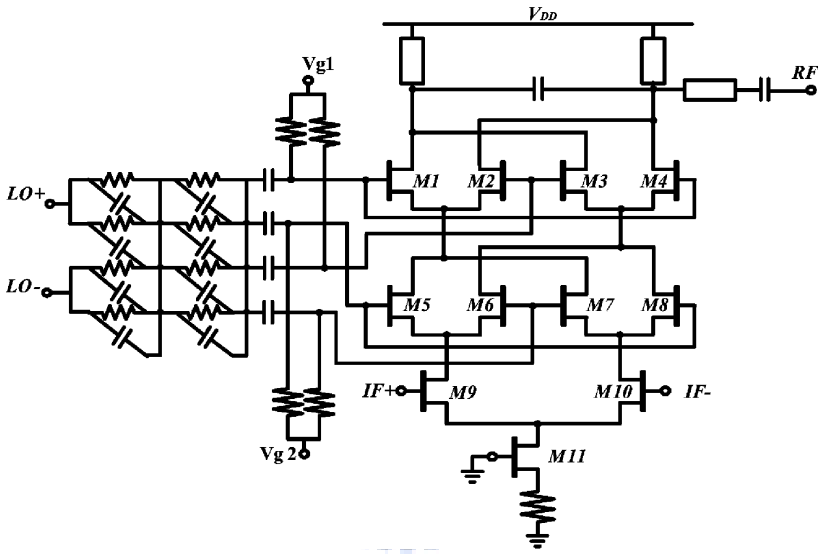
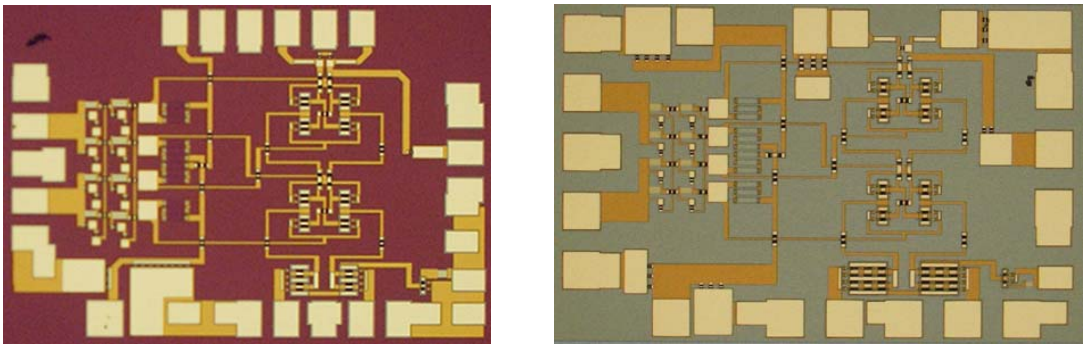


Fig. 3-2 The stacked-LO subharmonic Gilbert upconverter.

3.4 Measured Results of pHEMT and mHEMT Mixers

Figure 3-3 displays the fabricated chip micrographs with the same area of 1.3 mm × 0.9 mm including pads. Fig. 3-3 (a) and (b) are mHEMT and pHEMT stacked-LO subharmonic Gilbert upconversion mixers, respectively. The left and bottom sides are LO and IF differential input ground-signal-ground-signal-ground (GSGSG) pads, respectively. The RF output GSG pad is on the right side. The supply voltage and current are 4.6 V and 7 mA for the mHEMT mixer, while the pHEMT mixer needs 5 V supply voltage and draws a 10 mA current.



(a) mHEMT mixer (b) pHEMT mixer

Fig. 3-3 Micrographs of (a) mHEMT and (b) pHEMT Gilbert upconverters.

The measured conversion gain with respect to LO power is shown in Fig. 3-4. When LO=19/20 GHz and IF=0.1 GHz, the mHEMT and pHEMT stacked-LO subharmonic Gilbert mixers have a peak gain of -0.2 dB and -7.1 dB, respectively. High LO driving power is needed to compensate for the loss of the two-section polyphase filter. The higher cut-off frequency of mHEMT devices renders a higher conversion gain for the active Gilbert mixer. The linearity of the mHEMT and pHEMT upconverters is displayed in Fig. 3-5. The pHEMT upconverter has a measured OP_{1dB} of -24 dBm and OIP_3 of -12 dBm, while the other mHEMT subharmonic mixer possesses -26 dBm OP_{1dB} and -10 dBm OIP_3. The mHEMT mixer is better by 4-dB on linearity measured as the difference between the OIP_3 and OP_{1dB}. As shown in Fig. 3-6, LO-to-RF and 2LO-to-RF [43] isolations are about 40 dB for the pHEMT mixer, and 30 dB and 40 dB for the mHEMT mixer, respectively. The 45 dB and 50 dB IF-to-RF isolations are measured as IF=100 MHz ~ 500 MHz for the mHEMT and pHEMT upconverters, respectively. The 3-dB RF bandwidth of pHEMT and mHEMT mixers are 5 GHz (37.5 ~ 42.5 GHz) and 7 GHz (35 ~ 42GHz), respectively. The pHEMT mixer has an RF output return loss of 9.6 dB at 40 GHz and the best matching point of 11 dB at 39 GHz. The output return loss of the mHEMT mixer is 7 dB at 38 GHz and better than 10 dB from 42 GHz to 47 GHz.

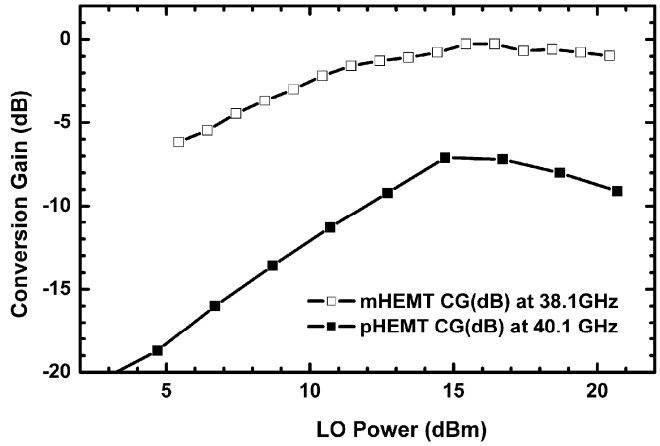


Fig. 3-4 Measured conversion gain of the pHEMT and mHEMT Gilbert upconverters when the LO frequency is fixed at 20/19 GHz, respectively.

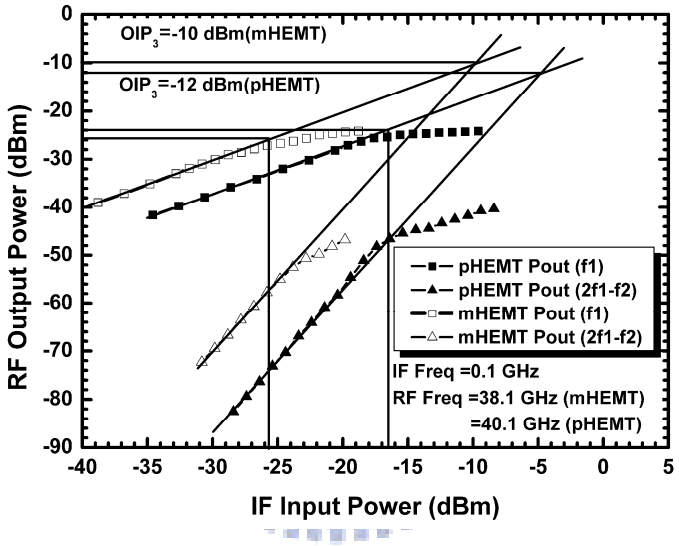


Fig. 3-5 Measured output performances of pHEMT and mHEMT upconverters when IF_1=100 MHz and IF_2=150 MHz .

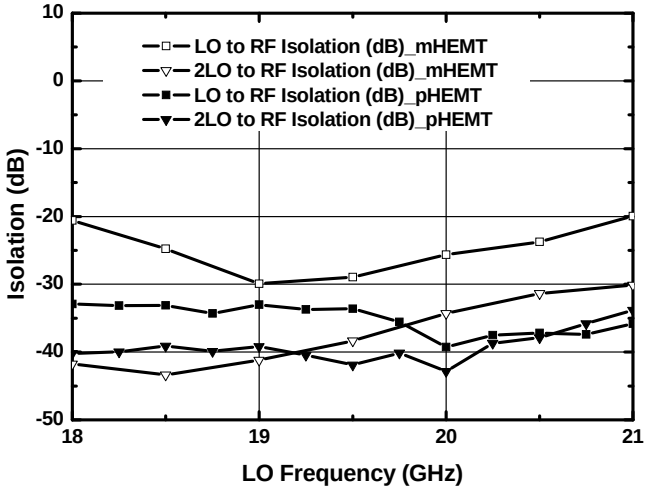


Fig. 3-6 Measured LO-to-RF and 2LO-to-RF isolations of pHEMT and mHEMT upconverters.

3.5 SUMMARY

In this Chapter, the Q-band stacked-LO subharmonic upconversion mixers are designed and compared using both 0.15 μm mHEMT and pHEMT technologies. In the upconversion mixers, the performance comparisons of the previously published papers are shown in Table 3.1 at the similar frequency bands using pHEMT, mHEMT [9], [11], SiGe BiCMOS [45], and CMOS technologies [46]-[47]. The mHEMT upconversion mixer has better conversion gain. The conversion gain of the mHEMT Gilbert mixer is improved by 7 dB in Q-band frequencies because the 0.15 μm mHEMT technology has higher g_m and f_t than the 0.15 μm pHEMT. A comparison of V-band mHEMT and pHEMT FET-based image reject mixers was published and their performances are almost the same [10]. It is of no use increasing the conversion gain in passive mixers by technological advances. In Table 3.1, the experimental outcome shows that the active Gilbert mixer with good isolations can be implemented using HEMT in the millimeter-wave regime, and we can select the advanced mHEMT technology to improve conversion gain and linearity.

TABLE 3-1 Performance comparisons of up-conversion mixers.

Up-conversion mixer	Type	RF Freq. (GHz)	LO Power (dBm)	Conversion Gain(dB)
0.18 μm pHEMT [9]	SH SB diode	43 ~ 46	+12	-11
0.14 μm pHEMT [11]	FET resistive	30 ~ 50	+2	-6
0.14 μm mHEMT [11]	FET resistive	30 ~ 50	+2	< -6
0.18 μm SiGe BiCMOS [45]	DB Gilbert-cell	35 ~ 65	+5	-7
0.13 μm CMOS [46]	DB Gilbert-cell	18 ~ 28	+3	-2 ~ 0.7
65 nm CMOS [47]	FET resistive	60	+8.7	-13.5
This work (mHEMT)	SH Gilbert-cell	37.5 ~ 42.5	+15	-0.2
This work (pHEMT)	SH Gilbert-cell	35 ~ 42	+15	-7.1

3.5 Summary

Up-conversion mixer	Type	LO-RF Isolation(dB)	2LO-RF Isolation(dB)	OP_{1dB} (dBm)	OIP_3 (dBm)
0.18 μm pHEMT [9]	SH SB diode	NA	8 ~ 20	-16	NA
0.14 μm pHEMT [11]	FET resistive	>30	NA	NA	3
0.14 μm mHEMT [11]	FET resistive	>30	NA	NA	< 6
0.18μm SiGe BiCMOS[45]	DB Gilbert-cell	> 40	NA	-25	-16
0.13 μm CMOS [46]	DB Gilbert-cell	> 30	NA	-7 ~ -5.2	3 ~ 5.8
65 nm CMOS [47]	FET resistive	34	NA	-19	NA
This work (mHEMT)	SH Gilbert-cell	20 ~ 30	30 ~ 45	-26	-10
This work (pHEMT)	SH Gilbert-cell	33 ~ 40	> 40	-24	-12

NA = not available, SH = subharmonic, SB=Schottky barrier, DB = double-balanced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Chapter 4 Compact CPW-MS-CPW Two-Stage pHEMT Amplifier Compatible With Flip Chip Technique in V-Band Frequencies

4.1 INTRODUCTION

Recently, the flip-chip bonding technique is necessary for packages of millimeter-wave monolithic microwave integrated circuits (MMICs) [7], [19]-[22]. The flip-chip bonding technique has advantages over traditional wire bonding technique because of the shorter interconnect path, better mechanical stability, higher reliability and less parasitic effects [19]-[21]. CPW topology [19][20][48] is widely employed in the millimeter-wave flip-chip MMICs to provide a smooth electric transition interface between the chip and the substrate carrier while the MS topology after flip-chip assemblies shows a strong gain degradation for the frequencies above 50 GHz [7] even though the layout of an MS-type topology can save much real estate in the IC technology. The CPW MMIC has less complicated processing steps by eliminating via hole etching, wafer thinning, and backside processing in the MS-type process [19][7]. Although the CPW circuit has the advantage of simple process, the lower effective dielectric constant and the difficulties in meandering the layout make the CPW MMIC size formidably large. CPW two-stage amplifiers were demonstrated at W-band frequencies, but consumed the large size of 1.9 mm × 1.25 mm and 2.4 mm × 1.1 mm, respectively [19], [48]. The compact size of the MS topology results from the higher effective dielectric constant and flexibilities on routing. The cost of the MMIC largely depends on the MMIC size rather than on the processing steps. For a two-stage power amplifier, the highest impedance transformation ratio occurs in the interstage because the input of the power stage has the lowest impedance while the

output of the driver stage has the highest impedance. Transistors can function as a transition between MS and CPW circuits. Thus, it is imperative that for a two-stage amplifier the interstage matching circuit should be implemented in MS topology while the CPW topology should be employed in the input and output port to be a good compromise between flip-chip bonding compatibility and chip size.

The purpose of this work is to employ transistors as the area-saving CPW-MS transition. Many CPW-MS passive transitions were investigated [24]-[27]. In order to reduce the mismatch between the CPW and MS lines, a passive transition normally requires a large area and becomes impractical in the MMIC design. Figure 4-1 shows the concept of the CPW-MS (MS-CPW) transition by the transistor. The gate (drain) port of the pHEMT is fed by the CPW line and source ports are symmetrically connected to the front side ground of the CPW line. The same via holes are also employed to connect the backside ground of the MS line at the drain (gate) port.

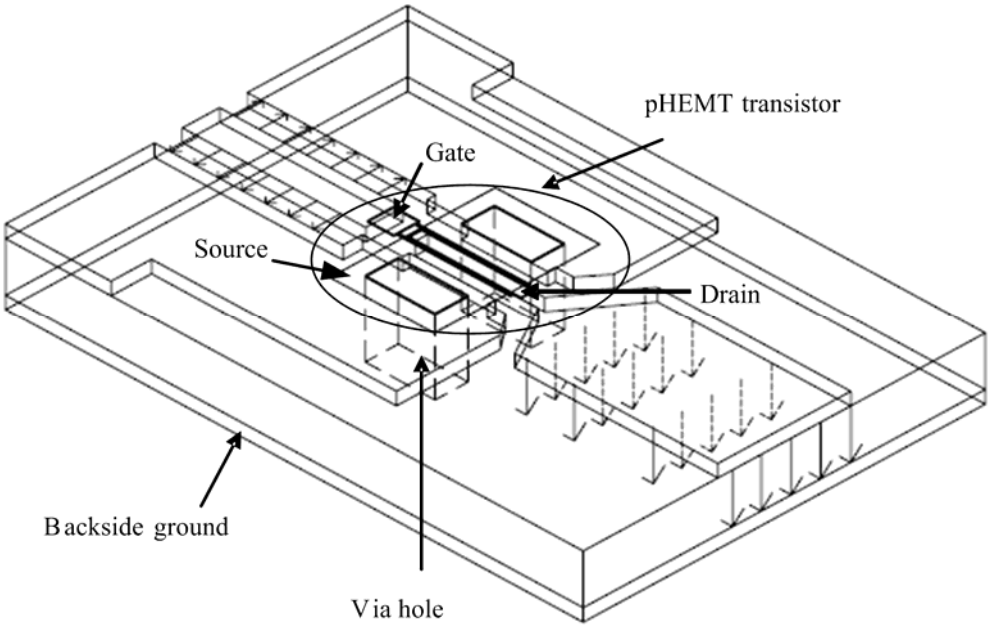


Fig. 4-1 The CPW-MS transition by pHEMT with via holes at the source terminals.

4.2 THE OPTIMAL GROUND PLANE DESIGN FOR FG-CPWG WITH FLIP-CHIP TECHNOLOGY

The simulated analyses of loss and characteristic impedance for different ground widths are shown in Fig. 4-2 and 4-3, respectively. CPWG's signal width, slot spacing and transmission line length are 20 um, 17 um and 200 um, respectively. As shown in Fig. 2 and 3, the loss rapidly increases with the ground width decrease at high frequencies. In addition, the shrinking ground width causes impedance of transmission line higher gradually. The loss is reduced and characteristic impedance approximately keeps 50 Ω when the ground width is at least four times the signal width. Taking into consideration of loss, impedance, modes, and chip size, we choose 80-μm ground width for the optimal design. This transmission line dimension also conforms to the pHEMT transistor layout.

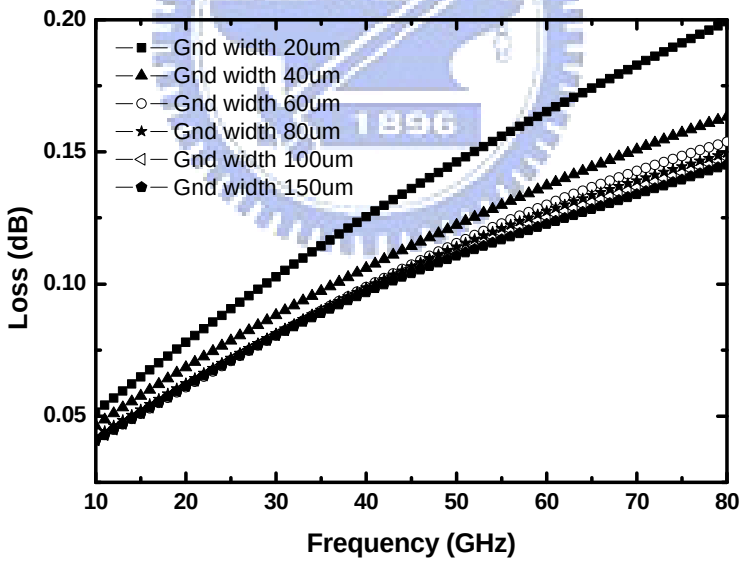


Fig. 4-2 Loss versus frequency for various ground widths with signal width of 20 um, length of 200 um and slot spacing of 17 um.

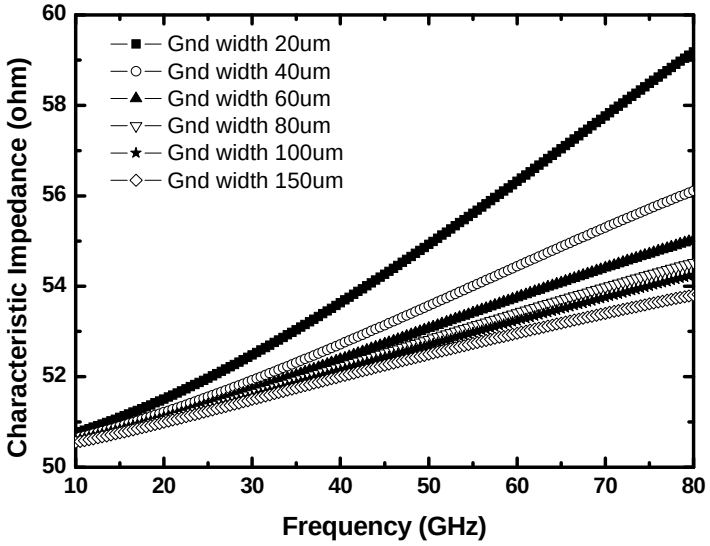


Fig. 4-3 Characteristic impedance versus frequency for various ground widths with signal width of 20 um, length of 200 um and slot spacing of 17 um.

4.3 GAIN COMPARISON OF FOUR TYPES – MS-MS, CPW-MS, MS-CPW, CPW-CPW

MS-MS, MS-CPW, CPW-MS and CPW-CPW one-stage pHEMT amplifiers designed at 60 GHz are employed to study the effect of using device as a transition. Figure 4-4 shows the simulation results for these four designs. All of the four designs have the same impedance matching as shown in Fig. 4-4. The input/output return loss is better than 10 dB for frequencies from 58.5 to 61.5 GHz for these four designs. Thus, the effect of loss is more pronounced at the resonant matching frequencies as shown in Fig. 4-4. It is well known that a CPW transmission line suffers more metal loss because the electric field is more concentrated at the metal edge in a CPW transmission line. Thus, the MS-MS one-stage amplifier has the highest peak gain of 9.4 dB while the CPW-CPW one-stage amplifier has the lowest peak gain of 8.0 dB. The metal loss causes 1.4 dB peak gain degradation for the CPW-CPW configuration and 0.7 dB for both CPW-MS/MS-CPW configurations when the MS-MS one-stage

amplifier is compared. The loss occurring mostly at the resonant matching frequency band also affects the bandwidth. The 3 dB gain bandwidth is 7.7 GHz, 8.4 GHz and 9.2 GHz for MS-MS, MS-CPW/CPW-MS and CPW-CPW configurations, respectively. Consequently, the CPW-MS-CPW two-stage amplifier is a good topology for V-band flip-chip amplifiers in terms of gain, bandwidth, and chip size. In this work, a CPW-MS-CPW two-stage amplifier is demonstrated at V-Band frequencies and the resulting amplifier shows no electric performance degradation after flip-chip mounting.

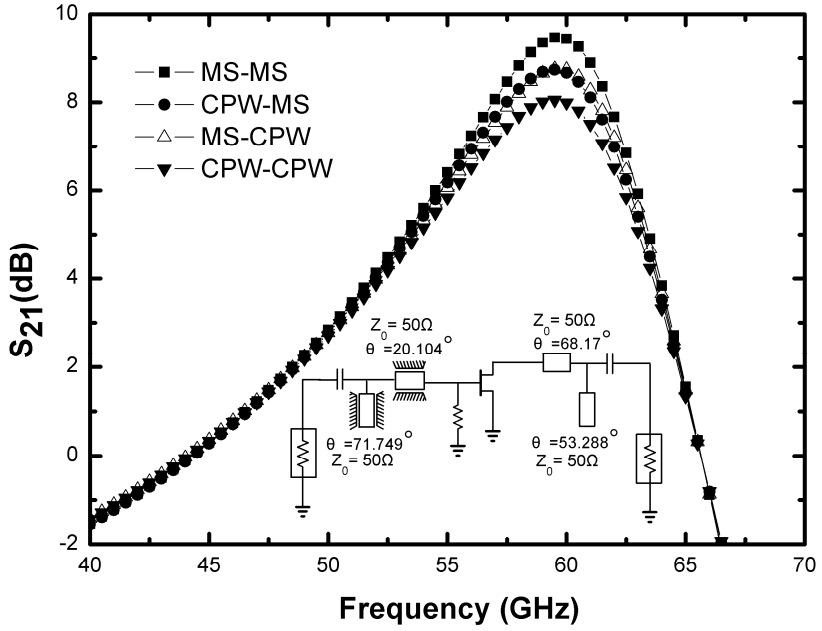


Fig. 4-4 Gain curves of the MS-MS, CPW-MS, MS-CPW and CPW-CPW one-stage amplifiers with the same impedance matching.

4.4 CIRCUIT DESIGN

The schematic of the CPW-MS-CPW two-stage amplifier is shown in Fig. 4-5 and the die photo is shown in Fig. 4-6. The size of the chip is 1.75 × 0.85 mm^2. This size is much smaller than the chip sizes of published references [19], [24]. S

parameters for both the passive elements and transistors are needed in the amplifier design. The S parameters of the passive elements are obtained through the EM simulator for better accuracy while the measured S parameters of the pHEMT transistors are used. The CPW-MS-CPW two-stage amplifier is designed for the maximum gain because the devices are unconditionally stable at 50 GHz when the voltages of V_{DS} and V_{GS} are 2.0 V and 0 V, respectively. The width of two pHEMTs in the amplifier is 2 × 50 μm. In Fig. 4-5, several the R-C series elements and C elements at drain and gate ports are designed to avoid the low-frequency oscillation and to enhance the out-band stability, respectively [24]. As shown in Fig. 4-5, the quarter-wavelength transmission lines with a characteristic impedance of 90 Ω are applied to the biasing networks at gate and drain terminals of the transistors. This transmission line design aims to isolate the RF signal through dc paths. The matching networks at both input and output of the two-stage amplifier are designed and realized using CPW-type transmission lines for flip-chip assembly. Additionally, the MS transmission line, which has a higher effective dielectric constant than CPW line has, is applied to realize the matching network between two transistors for miniaturizing the size of the amplifier.

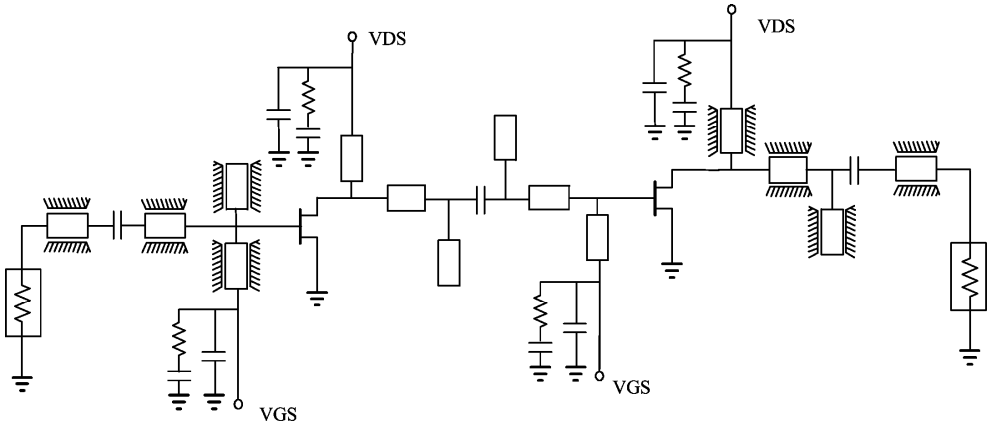


Fig. 4-5 The V-band CPW-MS-CPW two-stage pHEMT amplifier.

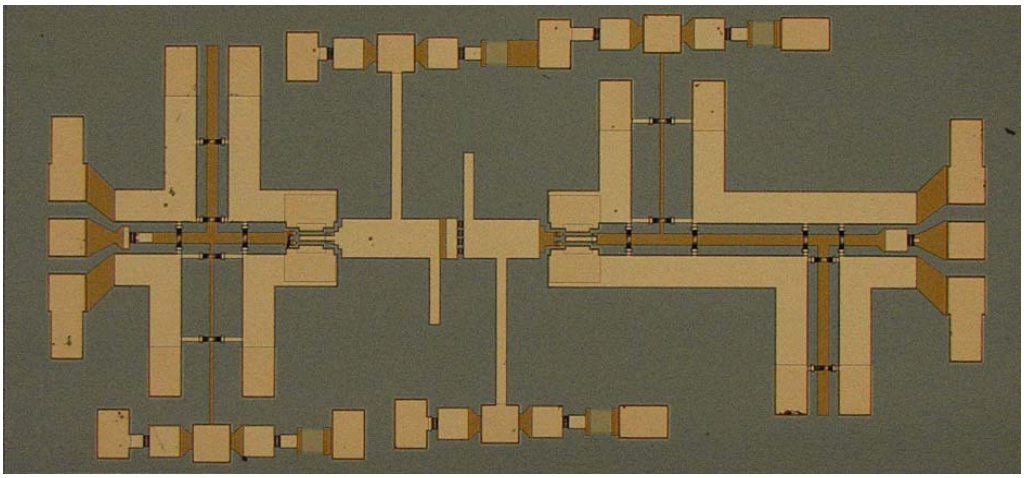


Fig. 4-6 Die photo of the CPW-MS-CPW two-stage pHEMT amplifier.

4.5 FLIP-CHIP MEASURED RESULTS

The S-parameter was measured from 2 GHz to 110 GHz by HP Network Analyzer 8510XF. Figure 4-7 shows a flip-chip micrograph of the V-band CPW-MS-CPW two-stage amplifier. The substrate carrier is made of alumina. The carrier has the feedline patterns including DC bias lines and 50 Ω CPW transmission lines in Fig. 4-7. The feedline patterns and chip pads are connected by the flip-chip bonding bumps. The flip-chip bonding bump sizes are 50 μm in diameter and 30 μm in height. The Au bumps have good conductance, malleability and stability.

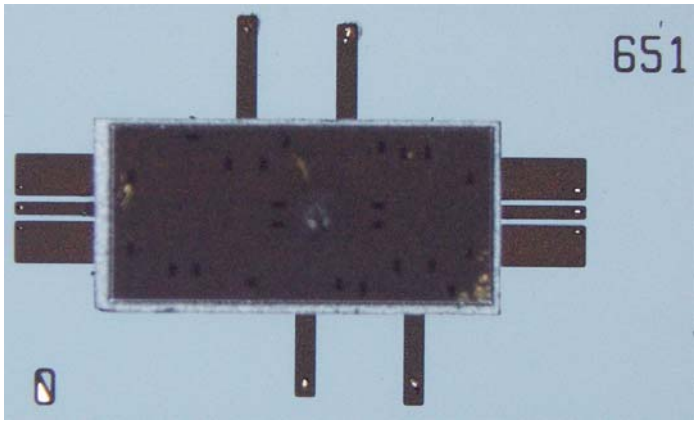
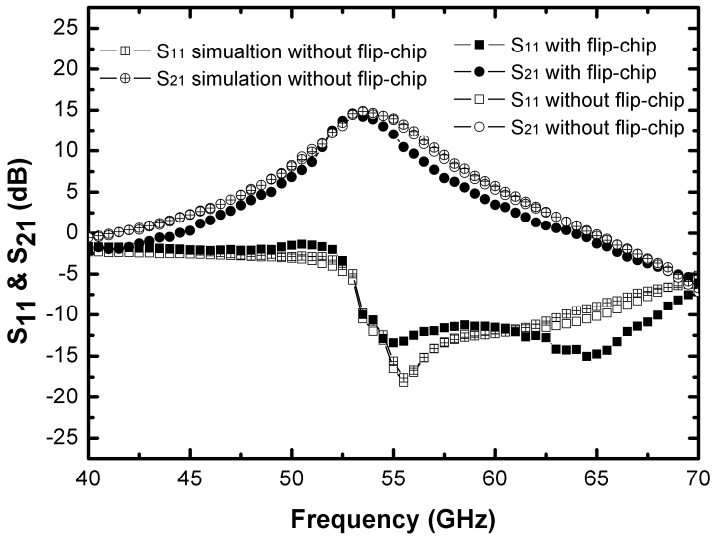
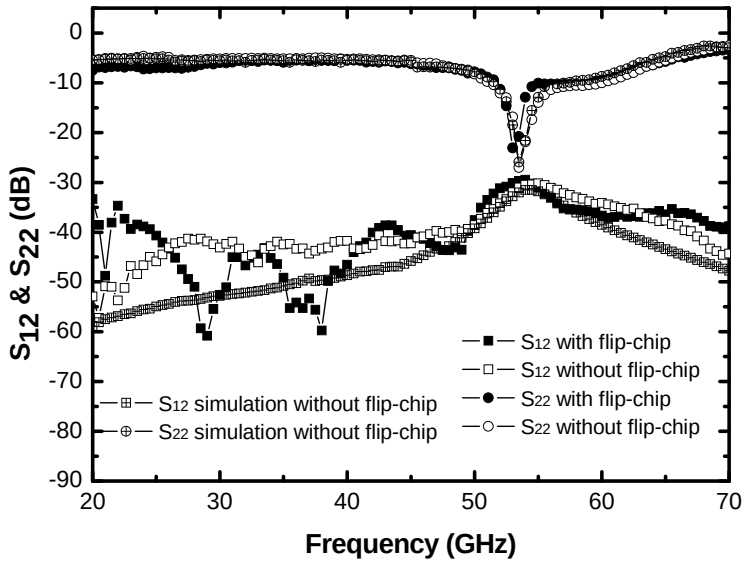


Fig. 4-7 Flip-chip photograph of the CPW-MS-CPW two-stage pHEMT amplifier.

As shown in Fig 4-8 (a) and (b), the measured S-parameters of the V-band two-stage amplifier with and without flip-chip bonding are very similar. The S_{21} peak of the amplifier without flip-chip bonding is 14.81 dB at 53.5 GHz. After using the flip-chip bonding technique, the amplitude and frequency of the S_{21} peak are slightly reduced and shifted to 14.52 dB and 53 GHz, respectively. The S_{11} with and without flip-chip bonding are -13.3dB and -18.1dB near the operating frequency of 55GHz, and the S_{12} of them are lower than -30 dB anywhere. Obviously, the reverse isolation (S_{12}) of the flip-chip technique is insignificant to the performance of the bare-chip. S_{22} of two curves are almost kept the same. The deepest S_{22} without flip-chip bonding is -27dB at 53.5GHz, and the lowest S_{22} with flip-chip bonding is -23dB at 53.0 GHz. The measured results show the feasibilities of this design approach utilizing the CPW-MS-CPW topology for flip-chip bonding techniques. Besides, the simulation results and measured results without flip-chip bonding are also shown in Fig. 4-8(a) and (b) for comparison. The simulation results agree well with the measured results. Thus, the CPW-MS/MS-CPW transitions by transistor device are wideband in nature.



(a) S_{11} and S_{21}



(b) S_{12} and S_{22}

Fig. 4-8 (a)S_{11} & S_{21} (b) S_{12} & S_{22} of the simulation (without flip-chip bonding) and measurement (with and without flip-chip bonding) CPW-MS-CPW two-stage pHEMT amplifiers.

4.6 SUMMARY

The V-band CPW-MS-CPW two-stage amplifier compatible with flip-chip bonding techniques is proposed and demonstrated. The input and output networks of the proposed amplifier are constructed by the CPW-based transmission lines, forming the smooth electric interfaces for the flip-chip bonding package. Additionally, the proposed compact CPW-MS-CPW transition, which effectively integrates the pHEMT transistors, successfully converts the electromagnetic energy from CPW mode to the MS mode. Such transition provides a wide degree of freedom to design the pHEMT amplifier with both CPW and microstrip elements. The prototype is fabricated using AlGaAs/InGaAs 0.15 μm pHEMT technology. After the prototype is packaged through the flip-chip bonding technology, there is negligible change on the electric characteristics. The measured results demonstrate the feasibility of the proposed CPW-MS-CPW two-stage pHEMT amplifier design for flip-chip bonding techniques.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Chapter 5 60 GHz mHEMT Single-Chip Receiver

5.1 INTRODUCTION

In recent years, researchers have paid significant attention to the 60 GHz front-end MMICs in high data wireless communication systems. These MMICs must satisfy the requirements of broad frequency bands. During the last few years, many authors have presented 60 GHz MMIC chip-set applications on Si-based and GaAs-based substrates [1], [7], [49]-[51]. A 0.13-μm CMOS 60 GHz frond-end receiver (RX) with an IF buffer amplifier provides a conversion gain of 11.8-dB, input-referred 1-dB compression point (P_{1dB}) of -15 dB, and a noise figure (NF) of 10.4-dB at a 1.2-V supply voltage [49]. Two 90nm CMOS 60GHz RXs with IF amplifiers exhibit a power gain of 32 dB/ -8.5 dB ~ 55.5 dB, P_{1dB} of -30 dBm/ -26 dBm, and NF of 8 dB/6.2 dB (double sideband), respectively [50], [51]. Although many attempts have been made to develop a CMOS-based system-on-chip (SOC) including the front-end and based-band circuits, III-V semiconductor technology is still much better suited to high frequency circuits than Si-based technology. III-V semiconductors offer the advantages of low noise, better power density, and higher breakdown voltage. 0.15-μm GaAs pHEMT and mHEMT RXs have 8.5-dB and 12.9-dB conversion gain, 9.8-dB and 7.2-dB NF, 27.6-dB and 14.6-dB image rejection ration, and 990-mW and 450-mW power consumption, respectively [1], [7]. HEMT GaAs-based front-end circuits surpass Si-based ones in performances such as a power amplifier and low noise amplifier, especially at microwave and millimeter-wave regions [4]-[6]. As a result, the silicon-based power amplifier and low noise amplifier cannot substitute for these GaAs-based circuits. Furthermore, high integration is needed in module to

reduce the cost and mismatch losses. Fully integrated GaAs-based HEMT single-chips are also a good choice in millimeter-wave regimes.

This Chapter demonstrates 60 GHz fully integrated receiver MMIC using 0.15-μm mHEMT technology. mHEMT technology has a cutoff frequency (f_t) of 110 GHz and a maximum oscillation frequency (f_{max}) of more than 200 GHz. Figure 5-1 shows the circuit block diagrams of a 60 GHz RX. The RF input path is a 60 GHz three-stage low noise amplifier (LNA) and the LO input contains a diode tripler and a three-stage feedback amplifier. When the RF signal mixes with the LO signal, the IF output signal is obtained through a multiplier which is an image rejection mixer.

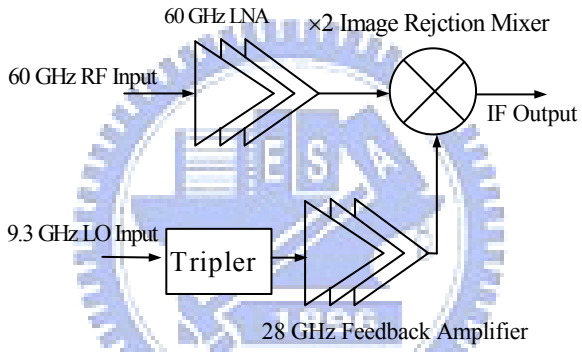

Fig. 5-1 Fully integrated 60 GHz receiver.

5.2 CIRCUIT DESIGN

This section explains three parts of the V-band fully integrated receiver—5.2.1 LO multiplier chain, 5.2.2 image rejection mixer and 5.2.3 60 GHz low noise amplifier.

5.2.1 LO Multiplier Chain

Figure 5-2 shows that an LO multiplier chain is composed of the tripler [52] and a three-stage amplifier, as shown in Fig. 5-2. The tripler uses an anti-parallel Schottky diode pair to generate the third harmonic of a design frequency as the even harmonic is suppressed. In this design, a diode is the 2 finger with a 10-μm width and two

diodes form the anti-parallel diode pair. The fundamental signal of the diode pair is attenuated when the signal is transmitted to the next stage which is a three-stage amplifier. A three-stage amplifier based on the microstrip line topology for a low frequency design includes input, interstage, and output matching. A resistor and a capacitance (R-C) feedback networks at every stage, connected between the gate and drain ports, help achieve the flat broadband gain. The first and second stages of the amplifier use an active device of two gate fingers with a 50-μm width, while the third stage uses 4 × 50 μm active device for more output power. To enhance the circuit stability, the 12-Ω resistor is located on the gate ports. The total power consumption of the amplifier is 80 mA with Vd＝3.6V.

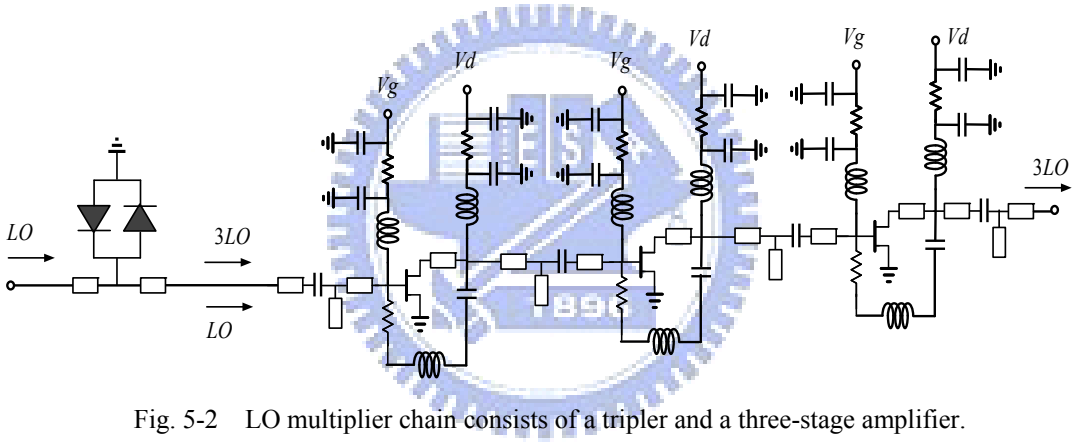

Fig. 5-2　LO multiplier chain consists of a tripler and a three-stage amplifier.

5.2.2 Image Rejection Mixer

The image rejection mixer includes two symmetrical anti-parallel subharmonic diode mixers with RF band-pass filters, a Wilkinson power divider, a 3 × f_{LO} quadrature hybrid and an IF quadrature hybrid [53]. The RF band-pass filters in the image rejection mixer based on the conventional quarter-wavelength coupler line at an RF frequency to design. This filter isolates the LO to RF ports leakage and reduces the LO power for a conversion gain. Figure 5-3 shows that the quadrature hybrid is formed with high-pass and low-pass LC elements. The symmetric hybrid can be

analyzed and derived by the odd- and even-mode half structure [53]. When port 4 is terminated with 50 Ω and an input power injects the port 1, ports 2 and 3 can be obtained with the equal magnitude and quadrature phase.

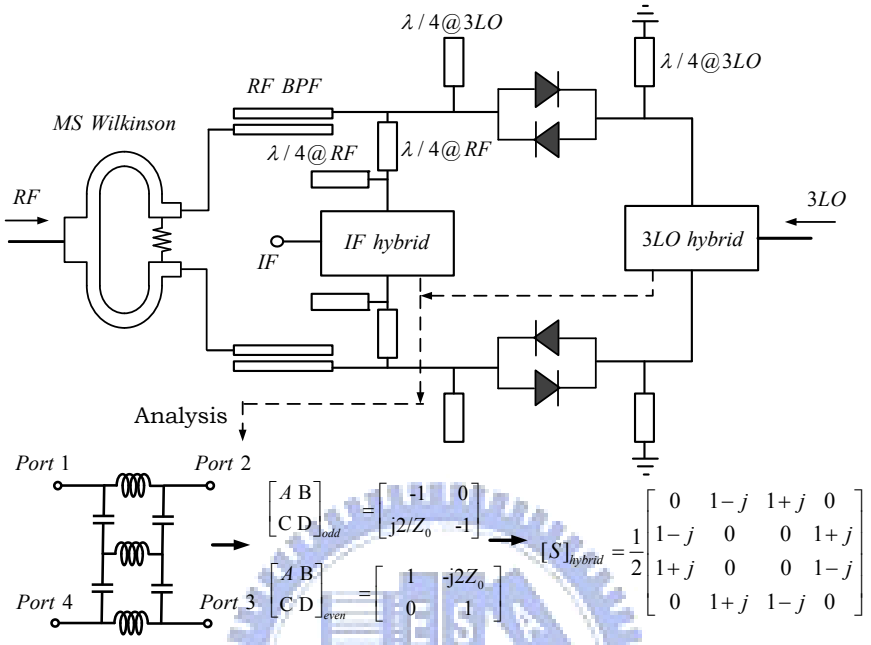

Fig. 5-3 Schematic of an image rejection mixer and analysis of a quadrature hybrid.

5.2.3 60 GHz Low Noise Amplifier

This receiver has a 60 GHz three-stage low noise amplifier (LNA) to compensate for conversion loss and suppress noise figure for the image rejection mixer. In Fig. 5-4, the LNA adopts the source degeneration to minimize noise figure and expand the bandwidth in the first and second stages. Each stage of the three-stage amplifier comprises a 2 finger active device with a 50-μm width. The gate and drain biases connect the short stubs of the quarter-wavelength transmission line to open the in-band signal when a capacitor with a via hole is placed in the end of the quarter-wavelength transmission line. Furthermore, the resistor-capacitor series enhances the stability on the gate and drain bias networks. The total current

consumption of the three-stage LNA is 96 mA at Vd= 2.4 V.

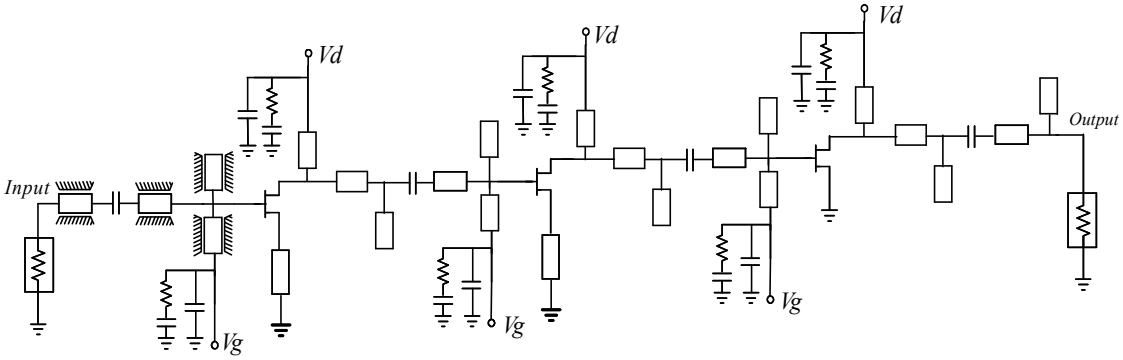

Fig. 5-4 60 GHz three-stage low noise amplifier with finite-ground coplanar waveguide (FGCPW) input matching network.

5.3 MEASUREMENT RESULTS

Figure 5-5 shows a photograph of the 60 GHz fully integrated receiver using 0.15 μm mHEMT GaAs technology. The measured results in this figure are based on the waveguide probes and on-wafer tests. The chip size measures 4.3 mm × 2.4 mm including pads. The left and bottom sides of Fig. 5-5 represent the RF input and LO input, respectively. The IF output is on the top side and the 8-pin DC pad is on the right side. The performance of the receiver can be enhanced by properly arranging the DC bias in the LO amplifier and RF LNA. Figure 5-6 shows the flip-chip micrograph of Fig. 5-5.

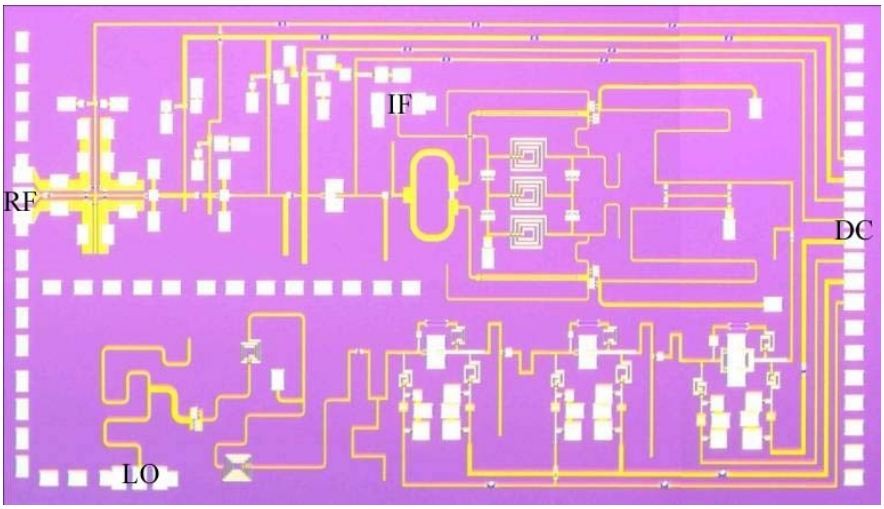

Fig. 5-5 Micrograph of the 60 GHz mHEMT receiver.

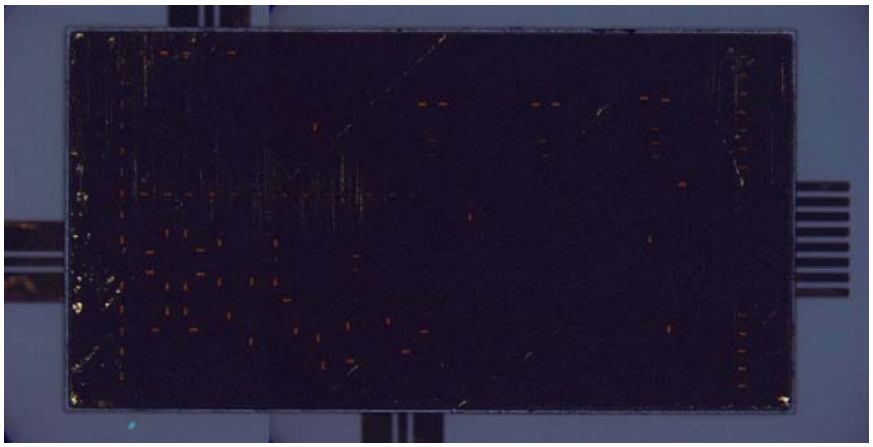

Fig. 5-6 Flip-chip photo of the 60 GHz mHEMT receiver.

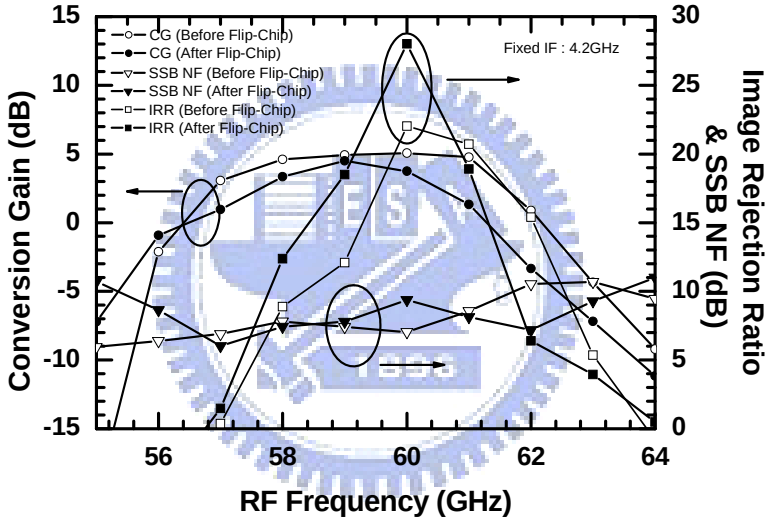

Fig. 5-7 Measured conversion gain, noise figure and image rejection ratio versus RF frequencies when IF = 4.2 GHz before and after flip-chip bonding.

Before and after flip-chip technology, Fig. 5-7 plots a conversion gain, an image rejection ratio (IRR), and a single-side band (SSB) noise figure (NF) versus RF frequencies are plotted at a fixed IF frequency of 4.2 GHz. Before flip-chip, the maximum conversion gain of 4 dB is measured at 60 GHz and the 1 dB RF bandwidth is about 3.6 GHz, spanning from 57.6 GHz to 61.2 GHz. The SSB NF of 7.0 dB and the IRR of 22 dB are achieved at 60 GHz. From 58 GHz to 63 GHz, the image

rejection ratio is more than 10 dB. After flip-chip, the maximum conversion gain is 4.5 dB and the noise figure is 7.7 dB at 59GHz. The best point of the IRR is 28 dB at 60GHz.

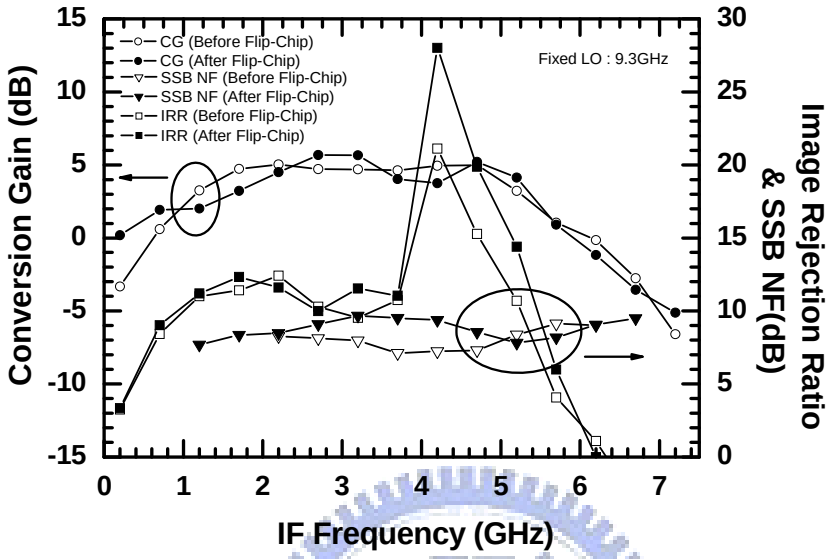

Fig. 5-8 Measured conversion gain and image rejection ratio versus IF frequencies when LO = 9.3 GHz before and after flip-chip bonding.

Figure 5-8 shows the conversion gain and IRR related to IF frequencies before and after flip-chip. Before flip-chip, when the fixed LO frequency equals 9.3 GHz, the 3-dB IF bandwidth is about 4.9 GHz, spanning from 0.8 GHz to 5.7 GHz,. Furthermore, the IRR is above 10 dB from 1 GHz to 5.6 GHz. The measured NF is better than 8 dB in the IF frequency ranges of 2.2 GHz to 5.2 GHz. After flip-chip, the noise figure increases a little from 2.4 GHz to 4.4 GHz. The Linearity performances of the mHEMT RX can be measured by the input 1 dB compression point (IP_{1dB}) and the input third-order intercept point (IIP_3). In Fig. 5-9, the IP_{1dB} and IIP_3 are -23.7 dBm and -15 dBm before flip-chip, and -19.7 dBm and -9.6 dBm after flip-chip,

respectively. Before flip-chip, the LO-IF and 3LO-IF isolations are better than 65 dB and 30 dB, respectively, as shown in Fig. 5-10. In particular, the best point of 75 dB is pronounced for the LO-IF isolation when LO=9.3 GHz. After flip-chip, 3LO-IF and LO-IF isolations are above 57 dB and 13 dB, respectively.

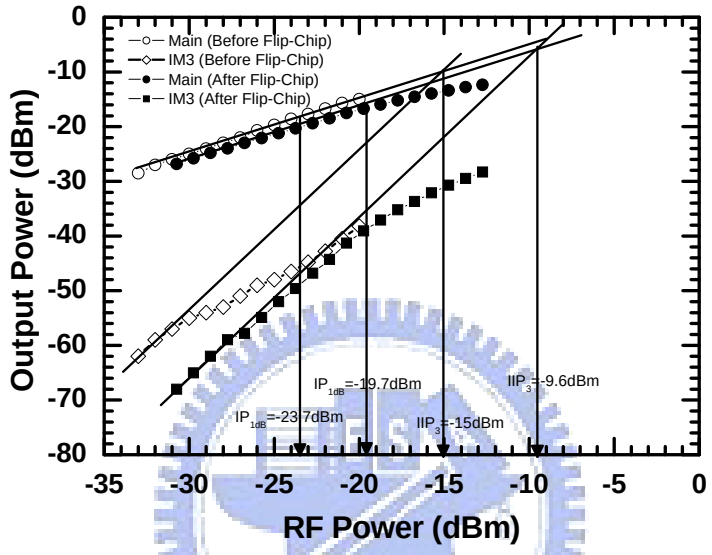

Fig. 5-9 Linearity performances of the 60GHz mHEMT receiver with and without flip-chip while the RF_1=60 GHz and RF_2=60.01GHz.

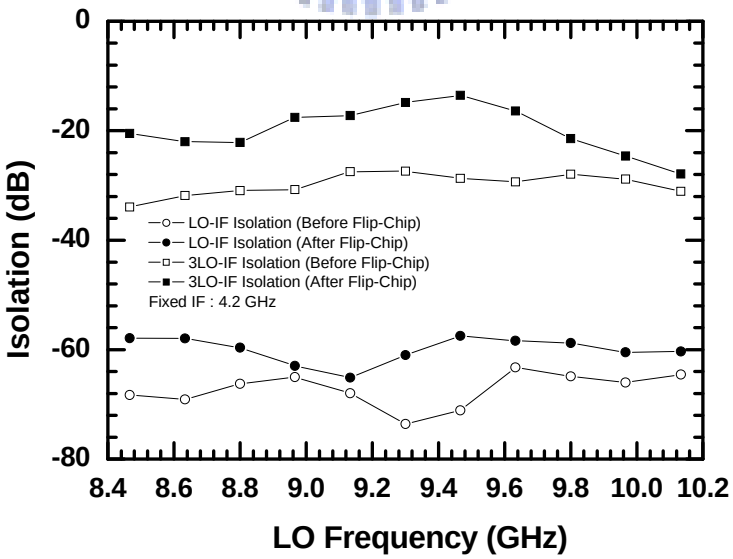

Fig. 5-10 LO-IF and 3LO-IF isolations before and after flip-chip bonding.

5.4 SUMMARY

This 60 GHz fully integrated single-chip RX is designed, fabricated and demonstrated using 0.15 μm GaAs-based mHEMT technology. The RF and LO design frequencies are 60 GHz and 9.3 GHz, respectively, and the IF output frequency is fixed at 4.2 GHz. The DC biases of the V-band low noise amplifier are optimized for the conversion gain and noise figure, which are trade-offs. Previous studies on 60 GHz pHEMT and mHEMT receivers and transmitters are few, but many studies regarding advanced CMOS technologies at 60 GHz have been presented. Table 5-1 shows the measured performance of 60 GHz RXs using 0.13 μm CMOS [54], 90nm CMOS [50]-[51], [55], 0.15 μm pHEMT [1], and 0.15 μm mHEMT [7] technologies, respectively. The noise figure on a mHEMT GaAs substrate is better than that on 0.13 μm and 90nm CMOS substrates [50], [54]-[55], and the chip size in this study is smaller than previously reported [1], [7]. The power performance and noise figure of the proposed GaAs-based HEMT amplifier are better than those of a CMOS-based amplifier at high frequencies. This is because the HEMT amplifier naturally has a higher current density, higher transconductance, and lower noise figure. The optimal design solution of a V-band fully integrated front-end transceiver might therefore use the mHEMT technology instead of CMOS technology in the millimeter-wave regimes.

TABLE 5-1 Performance comparisons of the state-of-the-art 60 GHz receivers

Ref.	Technology	Operation Frequency (GHz)	CG (dB)	IF Amp	NF (dB)	IRR (dB)
[54]	0.13 μm CMOS	60	27.5	X	12.5	--
[50]	90nm CMOS	60	32	X	8	--
[51]	90nm CMOS	60	-8.5~ +55.5	X	6.2	--
[55]	90nm CMOS	60	11.8	X	10.4	--
[1]	0.15 μm pHEMT	60	8.5	--	9.8	27.6
[7]	0.15 μm mHEMT	60	12.9	--	7.2	14.6
	This work (mHEMT) -before flip-chip	60	5	--	7.0	22
	This work (mHEMT) -after flip-chip	60	4	--	9.3	28

Ref.	Technology	Operation Frequency (GHz)	IP_{1dB} (dBm)	IIP_3 (dBm)	DC Power (mW)	Chip Size (mm^2)
[54]	0.13μm CMOS	60	-22.5	--	9	--
[50]	90nm CMOS	60	-30	--	70	--
[51]	90nm CMOS	60	-26	--	24	1.53
[55]	90nm CMOS	60	-15.8	--	76.8	3.8
[1]	0.15μm pHEMT	60	-19	-11	990	28.5
[7]	0.15μm mHEMT	60	-17	-10	450	16.5
	This work (mHEMT) -before flip-chip	60	-23.7	-15	518	10.32
	This work (mHEMT) -after flip-chip	60	-19.7	-9.6	518	10.32

Chapter 6 Regenerative Frequency Divider With Quadrature Outputs

6.1 INTRODUCTION

As a system of higher operating frequency, high-speed frequency dividers (FDs) play an important role in the modern wireless communication system. System architectures, such as homodyne and heterodyne, are used in RF integrated circuits to eliminate the bulky image-reject and IF filters. FDs with the quadrature outputs are required in direct-conversion architectures. Until now, several kinds of quadrature-output FDs have been reported at low frequencies. A divide-by-4 injection-locked LC divider based on a 0.18-μm CMOS technology was driven by anti-phase signals at 8 GHz and has a 0.8° phase error measured by an oscilloscope [56]. A 5~6 GHz quadrature regenerative divider was designed using a 0.18-μm SiGe BiCMOS technology [57]. The dividers, in the GaAs-based HEMTs technology, work up to high frequencies but most of them were designed with a single-ended output or differential outputs [58]-[61]. The maximum operating frequency of the original RFD, proposed by Miller in 1939 [62], is inherently higher than that of a conventional Master-Slave D-flip-flop (MS D-FF). The Miller divider based on a positive feedback loop is composed of a multiplier, an amplifier and a filter. This topology achieves a wideband division range and functions up to high frequencies. The conventional microwave design approach for regenerative frequency dividers (RFDs) takes a large valuable estate in the IC technology. The microwave monolithic integrated circuits (MMICs) of 94/47 GHz and 28/14 GHz RFDs consume a large size of 1 mm × 2 mm and 1.5 mm × 3 mm, respectively [58], [59]. In this Chapter, analog design concepts are adopted in the divider, so that the divider size becomes acceptable.

Consequently, higher cut-off frequency, high breakdown voltage and a semi-insulating substrate are the advantages of the GaAs-based pHEMT process, and this technology is a good option to design a high-frequency RFD when compared with the Si-based technologies. There are fewer papers published on analog cascode dividers implemented using the pHEMT technology [60]. To the best of our knowledge, the Ka-band Miller analog FD with quadrature outputs is realized for the first time in this Chapter using the AlGaAs/InGaAs pHEMT technology. The quadrature-output divider's size is small as 1.37 × 1.6 mm^2.

6.2 CIRCUIT DESIGN

Two multiplier-with-feedback dividers are injected with 0° and 180° signals, respectively, as shown in Fig.6-1, which results in quadrature outputs. The timing diagram of the quadrature-output divide-by-two divider is also shown in Fig. 6-1.

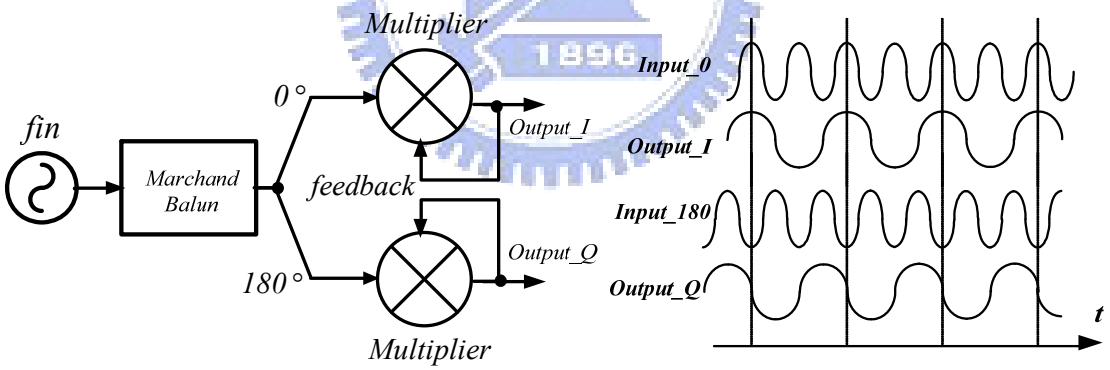

Fig. 6-1 Block diagram of the quadrature-output regenerative frequency divider and its input and output waveforms.

As shown in Fig. 6-2, active multipliers are composed of switching-pairs (M_1~M_8), transconductance-pairs (M_9~M_{12}) and current sources (M_{13}~M_{14}). All circuits operate in a differential mode. The differential output signals are fed into the transconductance stages and then commutated by the switching-pairs, which constructs a positive loop

gain. The frequency response of the feedback loop is like band-pass filter behavior due to LC tanks. The LC tanks at the multipliers, as band-pass filters, are designed at a half of the input frequency. The output signals of the Marchand balun, which are equal in magnitude but opposite in phase, are fed into the switching-pairs of the two multipliers. The planar Marchand balun uses two back-to-back quarter-wavelength coupled lines as a single-to-differential converter [63], [64]. The Marchand balun can be accurately implemented on a GaAs semi-insulating substrate based on a precise electromagnetic (EM) simulation. Additionally, all signal paths must be symmetrically arranged and avoid coupling effects to keep phase and magnitude balanced. Thus, the truly quadrature outputs of the divider are obtained.

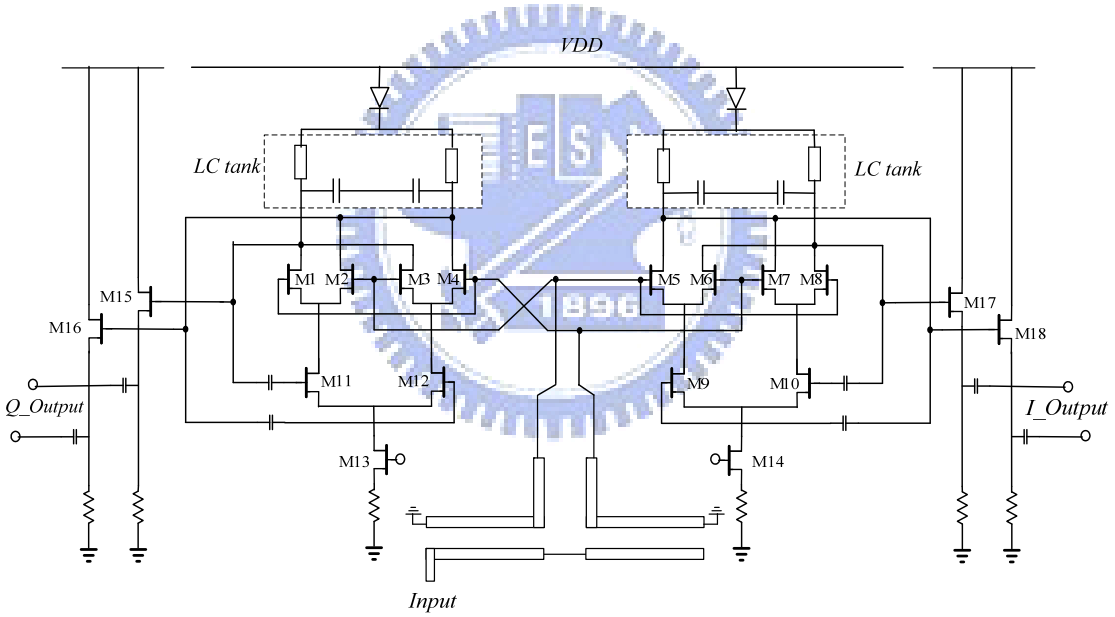

Fig. 6-2 Circuit topology of the quadrature-output regenerative frequency divider using a depletion mode AlGaAs/InGaAs pHEMT technology.

The depletion mode pHEMT transistor needs negative gate bias (V_{gs}) for operation. The sources of M_{13} and M_{14} are connected with thin film resistors to form self-biasing. In this circuit design, all supply voltages are positive. On the contrary, many reported

pHEMT dividers still adopted negative biasing [58], [59]. Then, diodes (D_1 and D_2) are inserted between V_{DD} and LC tanks and provide a voltage drop in order to easily bias the source followers (M_{15}~M_{18}) as output buffers.

6.3 MEASURED RESULTS

The die photo of the Ka-band quadrature-output Miller divider with a passive single side-band (SSB) up-converter test is shown in Fig. 6-3. The paths for high-frequency signal propagation must be minimized to avoid inductive parasitics, and the coupling effects among all paths also should be taken into consideration carefully. The chip size is 2.4 × 1.9 mm^2 including the SSB test architecture. The real size of the quadrature divider as well as the Marchand balun is about 1.37 × 1.6 mm^2. The supply voltage and current consumption of the divider's core are 6 V and 17.6 mA, respectively.

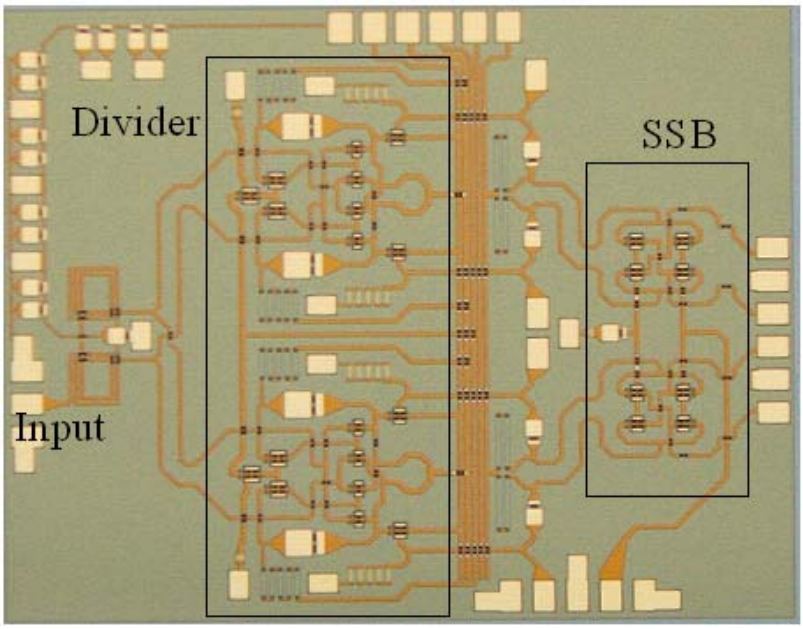

Fig. 6-3 Micrograph of the 32~36 GHz pHEMT analog cascode regenerative frequency divider with the single side-band up-converter test.

Figure 6-4 shows the relationship between the input sensitivity and the input frequency. The division range is from 32 to 36 GHz and the division bandwidth is 12 %. The curve gradually falls down to the minimum point from 32 to 35 GHz. The lowest input sensitivity of 2.7 dBm occurs at 35 GHz. The input source must simultaneously drive two multipliers' switching-pairs so more power is needed. Moreover, there is a rapid increase in input power from 35 to 36 GHz. The spectrum of the divider output with a 35-GHz input signal is displayed in Fig. 6-5. The output power is better than -10 dBm. In Fig. 6-6, a 35-dB side-band rejection ratio is achieved when the 60-MHz input IF quadrature signals are provided by an external quadrature component. This data reveals that the Marchand balun works well on a GaAs semi-insulating substrate at high frequencies and offers truly differential outputs for the multipliers. The measured phase noise performances of the divider's output at 17.5 GHz and the input source at 35 GHz are shown in Fig. 6-7. In general, the phase noise of the divider's output is better 6 dB than that of the driving source.

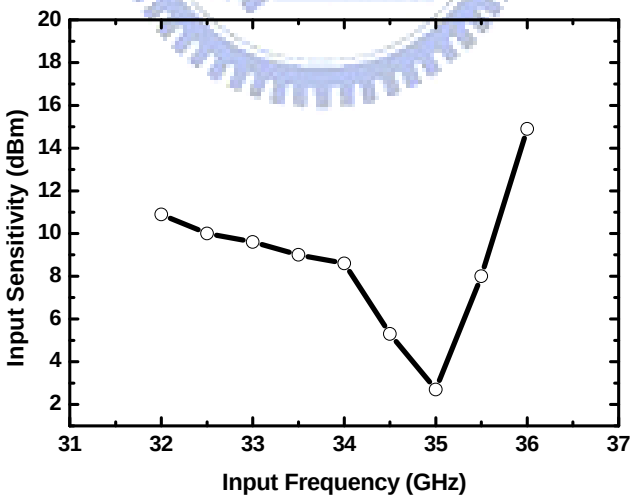

Fig. 6-4 Input sensitivity of the Miller frequency divider.

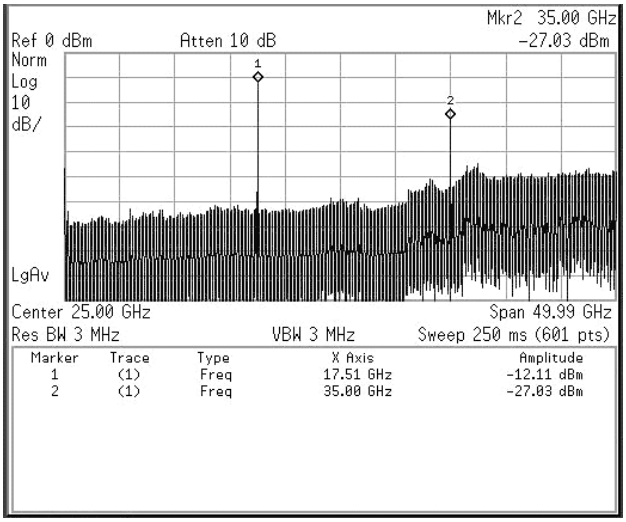

Fig. 6-5 Output spectrum of the divide-by-two Miller frequency divider.

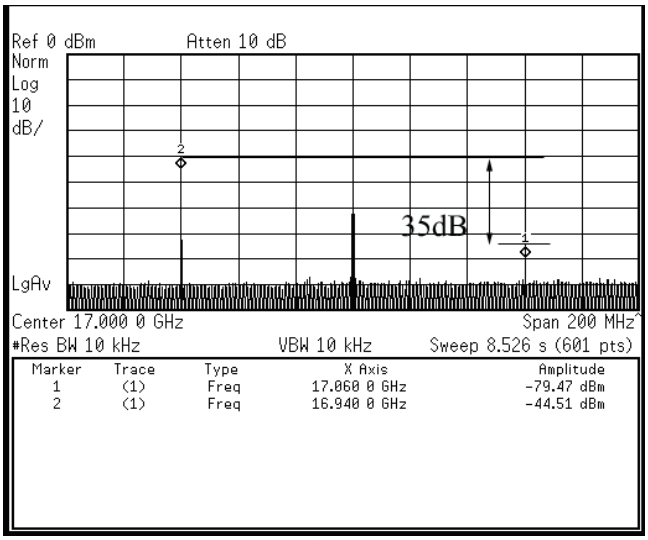

Fig. 6-6 Measured side-band rejection ratio of the 32~36 GHz pHEMT quadrature-output divider.

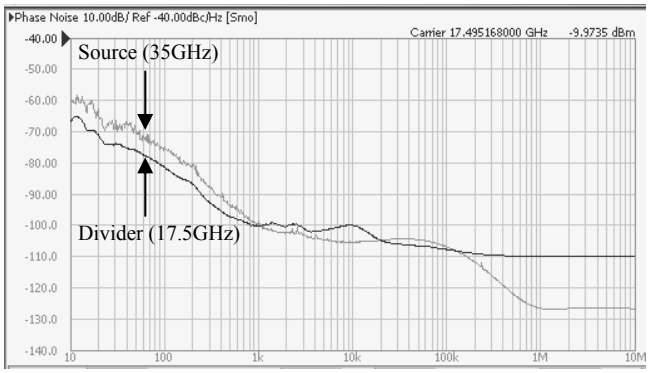

Fig. 6-7 Phase noise performance of the Ka-band pHEMT divider with a 35-GHz source input.

6.4 SUMMARY

The Ka-band quadrature-output analog Miller divider MMIC with the on-wafer SSB up-converter test is proposed and successfully demonstrated using the 0.15-μm AlGaAs/InGaAs pHEMT technology. This side-band rejection ratio defining the quadrature accuracy of the divider's outputs is 35 dB, since the process variation and uncertain path delay influence the circuit performance such as quadrature precision, especially in a higher frequency region. Dense path lines have been carefully considered in the layout to reduce parasitic effects and to keep balanced while the standard GaAs process has only two metal layers for path routing. A bandwidth of 12 % in the stable division has been obtained. The bandwidth can be improved by the lower quality-factor LC resonator. The chip size without the SSB up-converter test is compact thanks to the analog design methodology. The measured outcome agrees that the analog cascade 0.15-μm pHEMT Miller frequency divider with the quadrature outputs is a good opportunity for high-frequency quadrature applications.


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Chapter 7 Conclusion

Chapter 2 and 3 of this dissertation successfully proposed the several high-frequency Gilbert cell mixers combined with highly accuracy passive components, such as polyphase filters, couplers, and baluns. The semi-insulting substrate of GaAs is a very important contribution to passive elements. The image rejection ratio of a two-stage RC-CR polyphase filter based on a GaAs technology is better than that of a CMOS technology. Using HEMT technology, the experiments in this dissertation show that passive mixers in a transceiver below 40 GHz might be able to be replaced by Gilbert mixers. Passive mixers have a larger loss and size and require an amplifier to compensate for the mixer's loss. However, Gilbert cell mixers based on a 0.15 μm pHEMT technology supply the conversion gain and compact the size below 40 GHz. Furthermore, a pHEMT RFD works well for quadrature accuracy outputs at high frequencies. Results demonstrate that the proposed analog divider is also a good choice in high-frequency applications. With advanced technology that offers a high f_T, such as mHEMT, the performance of a Gilbert cell mixer can be improved in terms of a gain, power consumption, and operation frequency. These outcomes show that HEMT analog circuit design is applicable in the millimeter-wave regime.

Packaging is also an important factor in the microwave and millimeter-wave regimes. Therefore, this dissertation also demonstrates a flip-chip assembly test in the V-band CPW-MS-CPW amplifier. Just like the on-chip amplifier, the mounted CPW-MS-CPW amplifier performs excellently, and this flip-chip bonding produces only negligible change in the electric characteristics of the amplifier. To maintain performance, and minimize chip size, this dissertation uses the CPW design at the input and output ports and the MS inside. This flip-chip technology successfully

provides the packaging required for millimeter-wave regimes.

This dissertation also demonstrates a 60 GHz single-chip receiver MMIC with high complexity using 0.15-μm mHEMT technology. The 60 GHz RF input is fed with the CPW line because of compatible for flip-chip technology. The first stage of the 60 GHz low noise amplifier utilizes the CPW-MS transition, while the MS line is used in low frequencies at the LO and IF ports. Using the MS line in low frequencies, a lot of layout areas are saved for easy routing. The receiver is composed of an LO multiplier chain, a V-band three-stage low noise amplifier, and a V-band image rejection diode mixer. A tripler and three-stage feedback amplifier form the LO multiplier chain. The 60 GHz image rejection mixer, which is based on the subharmonic diode mixer, is integrated with the IF and 3 × f_{LO} quadrature hybrids. The resulting mHEMT receiver without flip-chip technology produces the conversion gain of 5 dB, the noise figure of 7.0 dB, and the image rejection ratio of 22 dB at 60 GHz. The receiver with flip-chip technology has the maximum conversion gain of 4.5 dB and the better noise figure of 7.7 dB at 59 GHz, and the best image rejection ratio of 28 dB at 60 GHz, respectively.

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Appendix A Derivation of Scattering Parameters of Coupled-Line Quadrature Generators

The coupling coefficient (C) and through coefficient (T) for the coupled-line coupler are expressed as

$$C = \frac{jk\sin\theta}{\sqrt{1-k^2}\cos\theta + j\sin\theta}, \tag{A.1}$$

and

$$T = \frac{\sqrt{1-k^2}}{\sqrt{1-k^2}\cos\theta + j\sin\theta}, \tag{A.2}$$

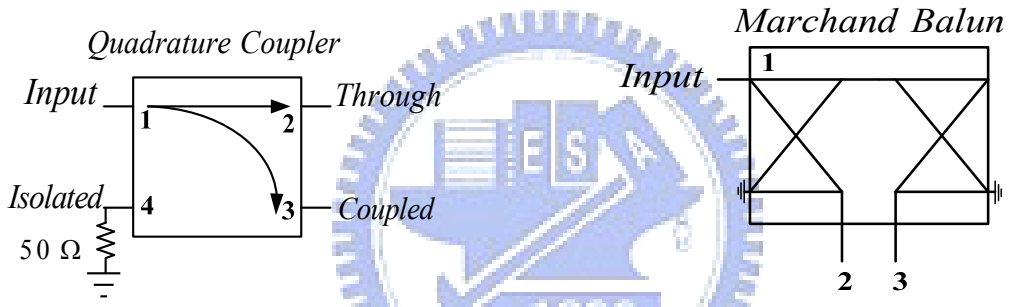
respectively, with electric length, θ, and coupling factor, $k = (Z_{0e} - Z_{0o})/(Z_{0e} + Z_{0o})$. Z_0 is the termination impedance, while Z_{0e} and Z_{0o} are the even-mode and odd-mode characteristic impedance of the coupled lines, respectively. For simplicity, the analysis is done under the lossless condition and $Z_0=(Z_{0e}Z_{0o})^{1/2}$. The scattering parameter matrices of the quarter-wavelength coupled-line coupler (Q) and Marchand balun (B) are shown by

$$\begin{bmatrix} V_1^{m-} \\ V_2^{m-} \\ V_3^{m-} \\ V_4^{m-} \end{bmatrix} = \begin{bmatrix} 0 & T_Q & C_Q & 0 \\ T_Q & 0 & 0 & C_Q \\ C_Q & 0 & 0 & T_Q \\ 0 & C_Q & T_Q & 0 \end{bmatrix} \begin{bmatrix} V_1^{m+} \\ V_2^{m+} \\ V_3^{m+} \\ V_4^{m+} \end{bmatrix} \tag{A.3}$$

and

$$\begin{bmatrix} V_1^{m-} \\ V_2^{m-} \\ V_3^{m-} \end{bmatrix} = \begin{bmatrix} -C_B^{\,2} + \dfrac{T_B^{\,4}}{1+C_B^{\,2}} & -C_B T_B + \dfrac{C_B T_B^{\,3}}{1+C_B^{\,2}} & C_B T_B - \dfrac{C_B T_B^{\,3}}{1+C_B^{\,2}} \\ -C_B T_B + \dfrac{C_B T_B^{\,3}}{1+C_B^{\,2}} & -T_B^{\,2} + \dfrac{C_B^{\,2} T_B^{\,2}}{1+C_B^{\,2}} & C_B^{\,2} - \dfrac{C_B^{\,2} T_B^{\,2}}{1+C_B^{\,2}} \\ C_B T_B - \dfrac{C_B T_B^{\,3}}{1+C_B^{\,2}} & C_B^{\,2} - \dfrac{C_B^{\,2} T_B^{\,2}}{1+C_B^{\,2}} & -T_B^{\,2} + \dfrac{C_B^{\,2} T_B^{\,2}}{1+C_B^{\,2}} \end{bmatrix} \begin{bmatrix} V_1^{m+} \\ V_2^{m+} \\ V_3^{m+} \end{bmatrix}, \quad \text{(A.4)}$$

$$= \begin{bmatrix} S_{11B} & S_{12B} & -S_{12B} \\ S_{12B} & S_{22B} & S_{23B} \\ -S_{12B} & S_{23B} & S_{22B} \end{bmatrix} \begin{bmatrix} V_1^{m+} \\ V_2^{m+} \\ V_3^{m+} \end{bmatrix}$$



(a) Coupler (b) Marchand balun

Fig. A-1 Symbols for (a) quadrature coupler and (b) back-to back coupled-line Marchand balun.

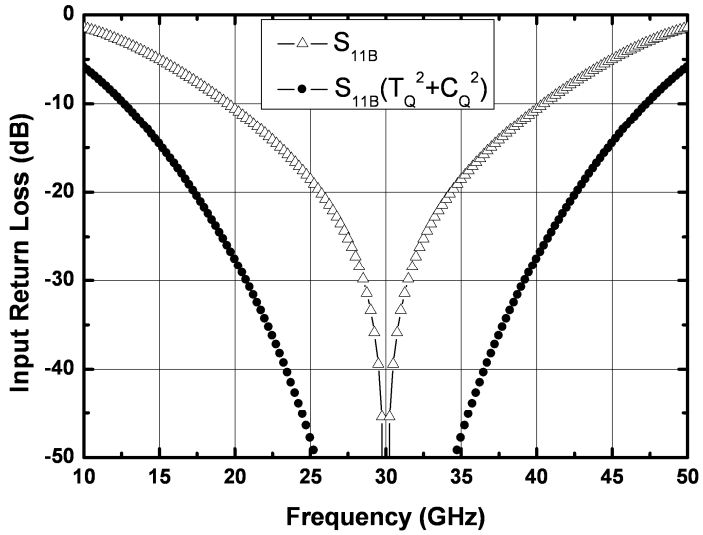


Fig. A-2 Simulated input return loss of the two differential quadrature generators in Fig. 2-4.

respectively, where V_n^{m+} and V_n^{m-} are the incident and reflected voltage waves at the n-th port of the m-th passive component, respectively, as shown in Fig. 2-4 and Fig. A-1 [64]. When the Marchand balun is designed with the coupling factor of $\sqrt{1/3}$, perfect matching is achieved at the center frequency [64]. The coupler with a $\sqrt{1/2}$ coupling factor results in balanced quadrature outputs. As shown in Fig.2-4, the input return coefficients of (a) a quadrature coupled-line coupler followed by two Marchand baluns and (b) a Marchand balun accompanied by two quadrature coupled-line couplers are derived as

$$\begin{aligned} V_{1,a}^{-} &= V_1^{1-} = T_Q V_2^{1+} + C_Q V_3^{1+} = T_Q V_1^{2-} + C_Q V_1^{3-} \\ &= T_Q \left(S_{11B} V_2^{1-} + S_{12B} V_2^{2+} - S_{12B} V_3^{2+} \right) + C_Q \left(S_{11B} V_3^{1-} + S_{12B} V_2^{3+} - S_{12B} V_3^{3+} \right) \\ &= T_Q{}^2 S_{11B} V_1^{1+} + T_Q S_{12B} V_2^{2+} - T_Q S_{12B} V_3^{2+} + C_Q{}^2 S_{11B} V_1^{1+} + C_Q S_{12B} V_2^{3+} - C_Q S_{12B} V_3^{3+} \\ &= S_{11B} \left(T_Q{}^2 + C_Q{}^2 \right) V_{1,a}^{+} + T_Q S_{12B} V_{2,a}^{+} - T_Q S_{12B} V_{3,a}^{+} + C_Q S_{12B} V_{4,a}^{+} - C_Q S_{12B} V_{5,a}^{+} \end{aligned} \quad \text{(A.5)}$$

and

$$\begin{aligned} V_{1,b}^{-} &= V_1^{4-} = S_{11B} V_1^{4+} + S_{12B} V_2^{4+} - S_{12B} V_3^{4+} \\ &= S_{11B} V_1^{4+} + S_{12B} \left(T_Q V_2^{5+} + C_Q V_3^{5+} \right) - S_{12B} \left(T_Q V_2^{6+} + C_Q V_3^{6+} \right), \\ &= S_{11B} V_{1,b}^{+} + T_Q S_{12B} V_{2,b}^{+} + C_Q S_{12B} V_{4,b}^{+} - T_Q S_{12B} V_{3,b}^{+} - C_Q S_{12B} V_{5,b}^{+} \end{aligned} \quad \text{(A.6)}$$

respectively, and the 5-port scattering parameter matrices are completely shown in Eq. (2.2) and (2.3) of Chapter 2. These 5-port scattering parameter matrices can also be obtained by heuristic derivation as developed in reference [64]. Figure A-2 shows the input return loss of the two topologies of the differential quadrature generators with $k_Q = \sqrt{1/2}$ and $k_B = \sqrt{1/3}$. The input return loss of the first type is improved by the factor of ($T_Q{}^2$+$C_Q{}^2$) in comparison with the second counterpart. There is more than 75% bandwidth expansion of 10-dB input return loss in the first structure.

Appendix B Single-Quadrature Image Rejection Gilbert Down-Conversion Mixer

A schematic of the 0.15-μm pHEMT single-quadrature image rejection Gilbert down-converter is shown in Fig. B-1. The single-quadrature Gilbert down-converter is composed of two Gilbert cell mixers, a two-stage polyphase filter at the LO stage, a four-stage polyphase filter at the IF stage and an IF buffer amplifier. As shown in Fig.B-1, (I+, I-) and (Q+, Q-) signals are applied to the left and right LO Gilbert cells of both mixers, respectively. At the same time, differential RF signals are injected into the RF stages of mixers. External baluns are used to generate the required RF and LO signals. The two-stage polyphase filter is adopted at the LO stage to generate quadrature-phase (0˚, 90˚, 180˚ and 270˚) and balanced-magnitude signals. The polyphase filter can be cascaded to improve quadrature accuracy and expand the bandwidth. Furthermore, the wanted signal can be obtained through the IF polyphase filter while the image-band unwanted signal is suppressed. The IF differential quadrature output signals are properly connected to form the differential signal as shown in Fig. B-1. The IF buffer amplifier provides a little gain to compensate the loss of the four-stage IF polyphase filter. Additionally, the transmission line at high frequencies must be considered as a portion of the mixer design and the layout is kept symmetrically for better performances.

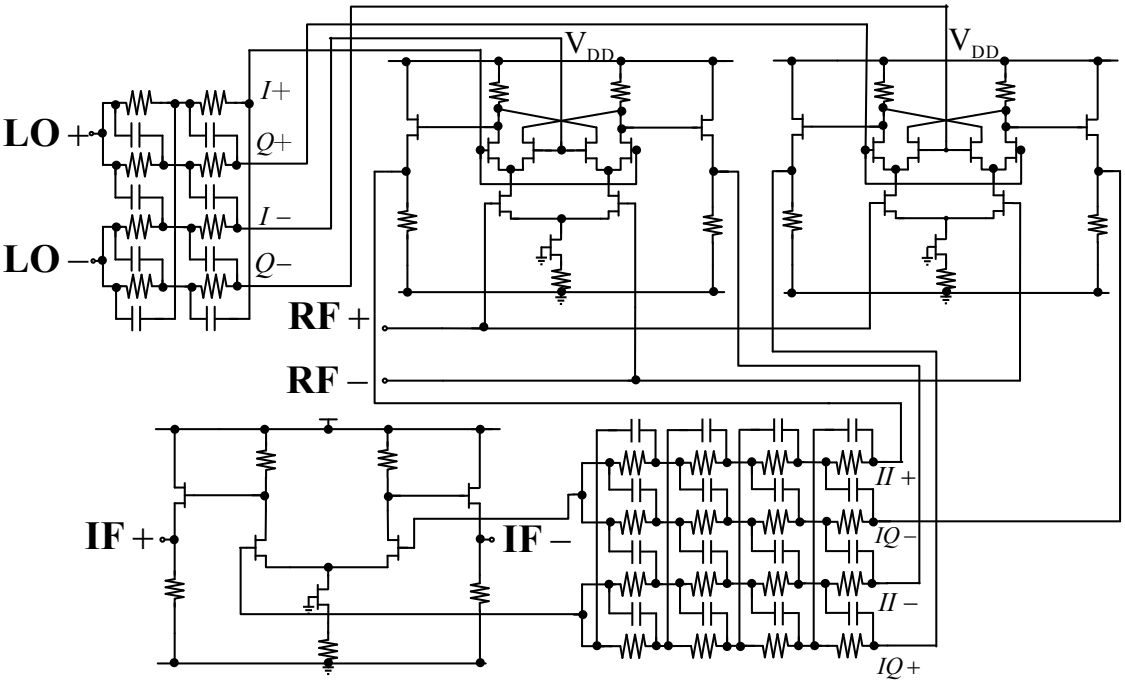


Fig. B-1 Schematic of the pHEMT single-quadrature Gilbert down-conversion mixer.

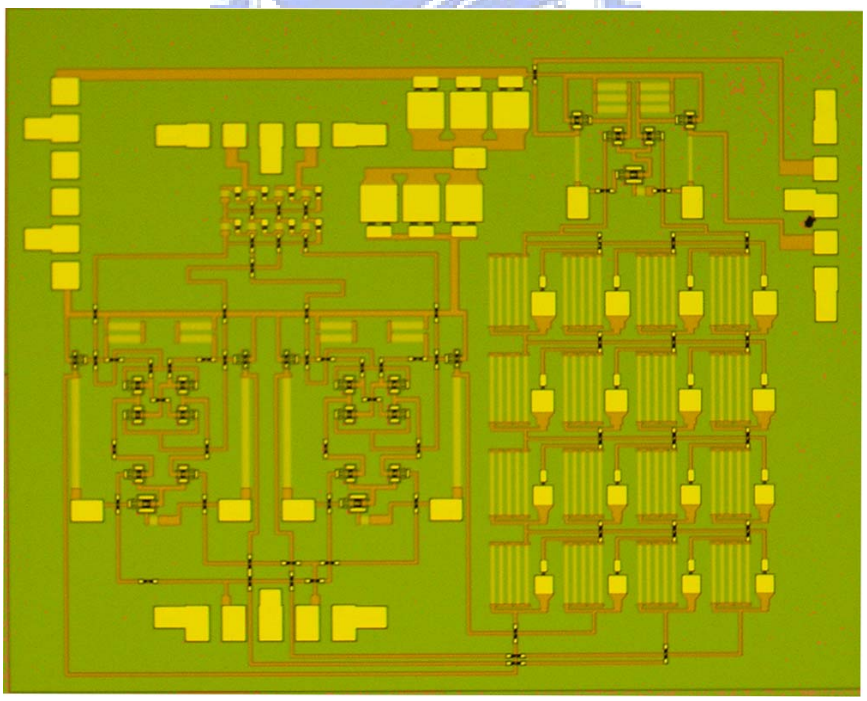


Fig. B-2 Photograph of the single-quadrature Gilbert down-conversion mixer using depletion mode pHEMT technology.

The microphoto of the pHEMT single-quadrature Gilbert down-conversion mixer with the IF polyphase filter is shown in Fig. B-2, and the die size is 2.3 mm × 1.6 mm. The layout just has two metal layers for routings in GaAs technology. The top and bottom sides are LO and RF differential input ground-signal-ground-signal-ground (GSGSG) pads, respectively. The right pad is the IF differential outputs, and the left pad is dc supply. The measured results are based on 50 Ω systems and on-wafer probes. The high-frequency LO and RF signal paths must be kept equal, respectively. The equal-path signal can reduce phase mismatch. The current consumption of mixer cores is 39 mA at the supply voltage V_{DD} of 5.5 V. All performances are measured at one port of differential outputs, and the other port is terminated by a 50 Ω load. When LO input power equals 6.7 dBm at 17.5 GHz, the maximum conversion gain of the image rejection down-converter is about 5.5 dB. The power ratio between the wanted IF signal and the unwanted IF signal defines the image rejection ratio. The image rejection ratio is better than 30 dB from 10 MHz to 90 MHz and 37 dB is achieved at 15 MHz and 80 MHz in Fig. B-3. Furthermore, the down-converter has 32-dB LO-to-RF, 40-dB LO-to-IF and 21-dB RF-to-IF isolations. Figure B-4 depicts the linearity performances of the input 1 dB compression point (IP_{1dB}) and the input third-order intercept point (IIP_3). IP_{1dB} and IIP_3 of the pHEMT Gilbert mixer equal 0 dBm and 16 dBm, respectively.

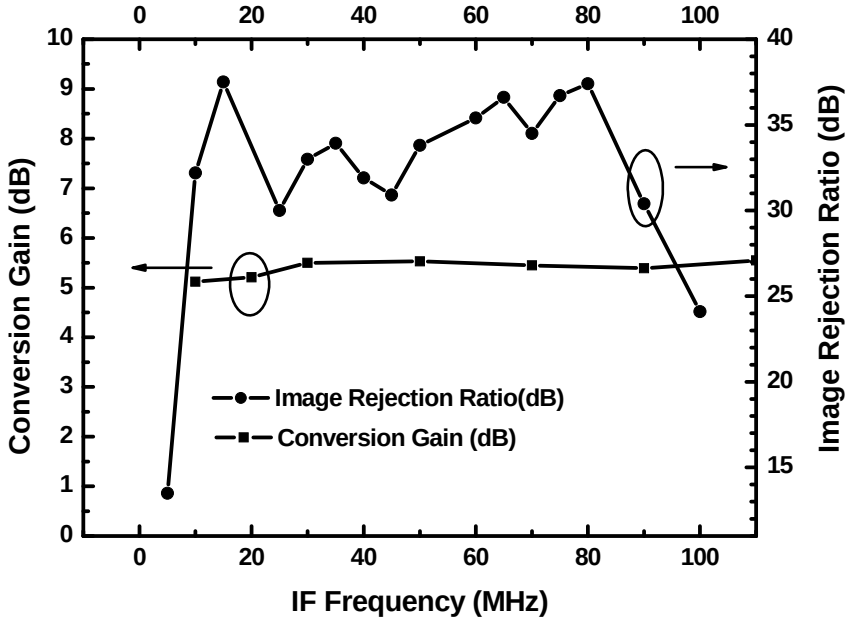


Fig. B-3 37-dB image rejection ratio and 5.5-dB conversion gain are measured in the pHEMT single-quadrature Gilbert down-conversion mixer.

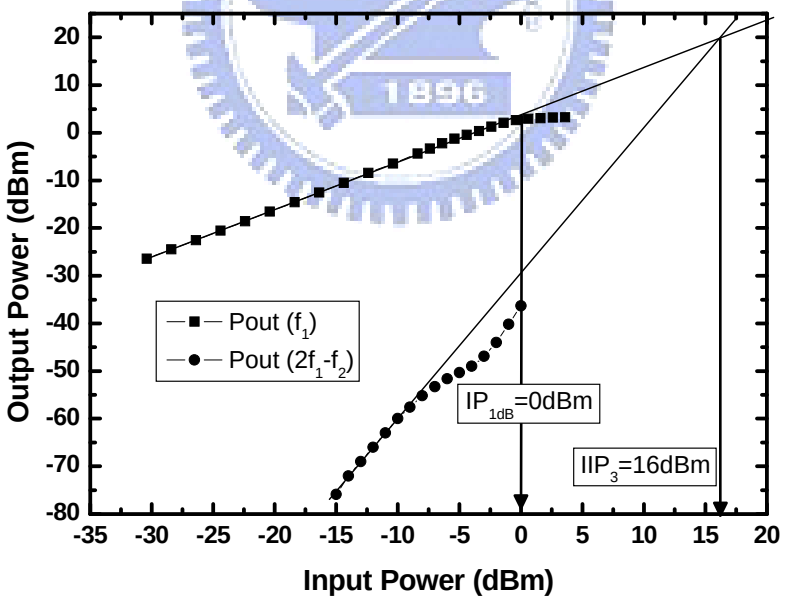


Fig. B-4 Measured linearity performances of IP_{1dB} and IIP_3.

Appendix C 60 GHz Balanced Amplifier With CPW Lange Coupler

,The balanced amplifier is commonly used in the microwave and millimeter-wave applications in order to enhance the output power. The directional coupler, such as a Lange coupler, is to divide or combine power in the amplifier. When an incoming signal supplies to port 1 and port 4 is terminated with 50 ohm, the two outputs in through and coupled ports can be ideally obtained with 3-dB insertion lass and 90˚ related phase difference. The CPW-type Lange coupler design is required for flip-chip technology. The optimal design dimension of the CPW-type Lange coupler is shown in Fig. C-1. The signal width (W) and spacing (S) are 9 μm and 13μm as the distance between the signal lines to ground plane fixes 94 μm at 60 GHz using Sonnet EM simulation. The S-parameters and phase difference of the V-band Lange coupler are simulated in Fig. C-2. The simulated insertion loss for through (S21) and coupled (S31) ports equals about 3.7 ± 0.1 dB and 3.5 ± 0.1 dB, respectively. The input return loss (S11) and the isolation (S41) port are 13 dB and 14.5 dB, respectively. The phase difference of the through (S21) and coupled (S31) ports keeps 90 ± 0.5 degree in the frequency ranges of 55 to 65 GHz.

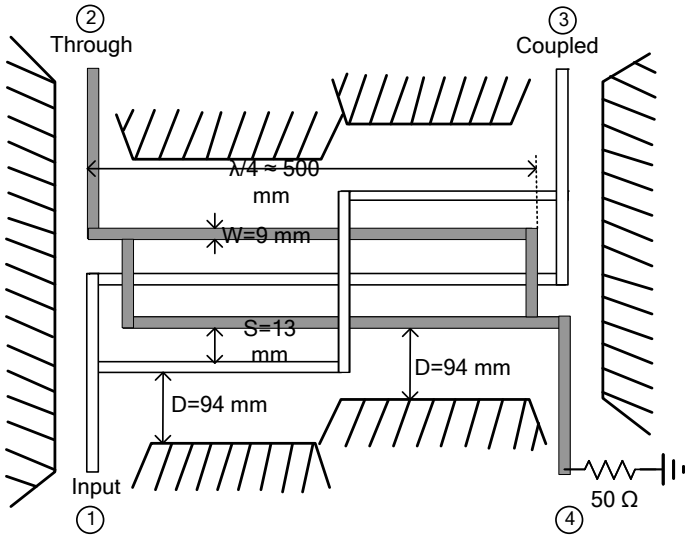


Fig. C-1 Design dimension of the V-band CPW Lange coupler.

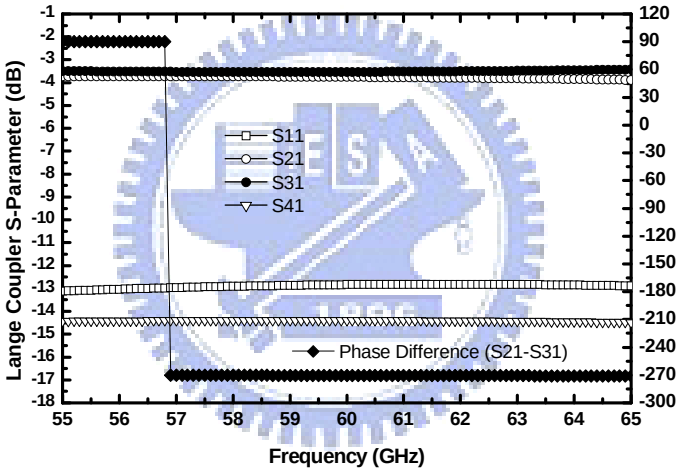


Fig.C-2 Simulation of the CPW Lange coupler.

This balanced amplifier consists of the CPW Lange couplers for an input and output and the two individual power amplifiers of the middle section, as shown in Fig. C-3. The individual amplifier uses the 0.15-μm pHEMT transistor sizes of 2-finger with a 50-um width and 4-finger with a 75-um width in the first and second stages, respectively. The fist stage amplifier has 89 mA under supply voltage of 3.4 V and the

second stage amplifier consumes 230 mA from 2.5 V power supply. The amplifiers also base on the CPW-MS-CPW design by via hole of the transistor.

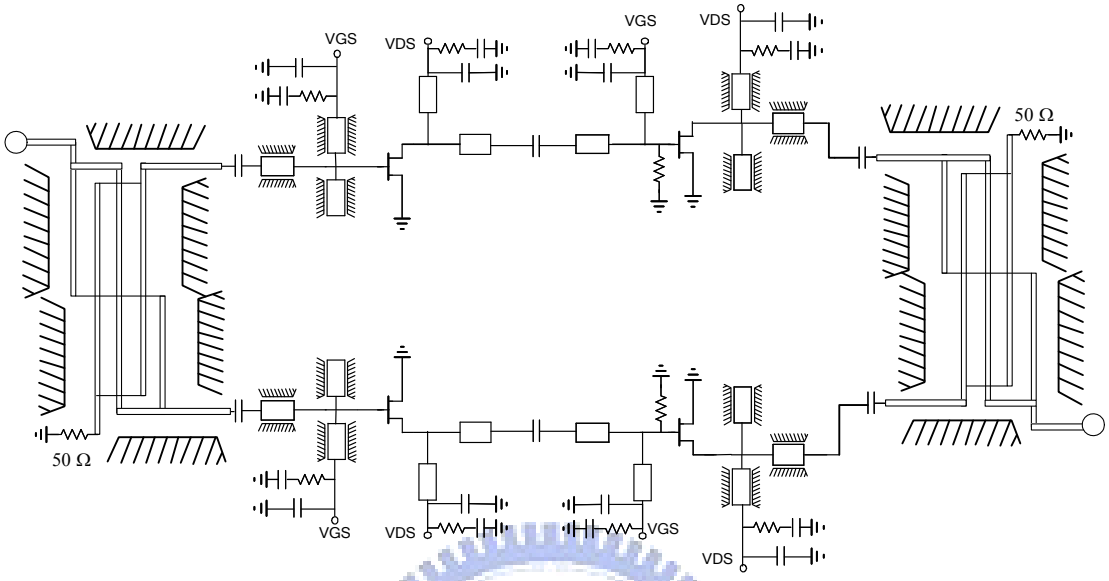


Fig.C-3 Circuit schematic of the balanced amplifier with CPW Lange couplers.

The die and flip-chip photos of the balanced amplifier with the Lange coupler are shown in Fig. C-4 (a) and (b). The chip area is 2.2×1.8 mm^2. The size of the CPW Lange coupler, which is 500 μm by 800 μm including pads, is compact in Fig. C-4 (a).

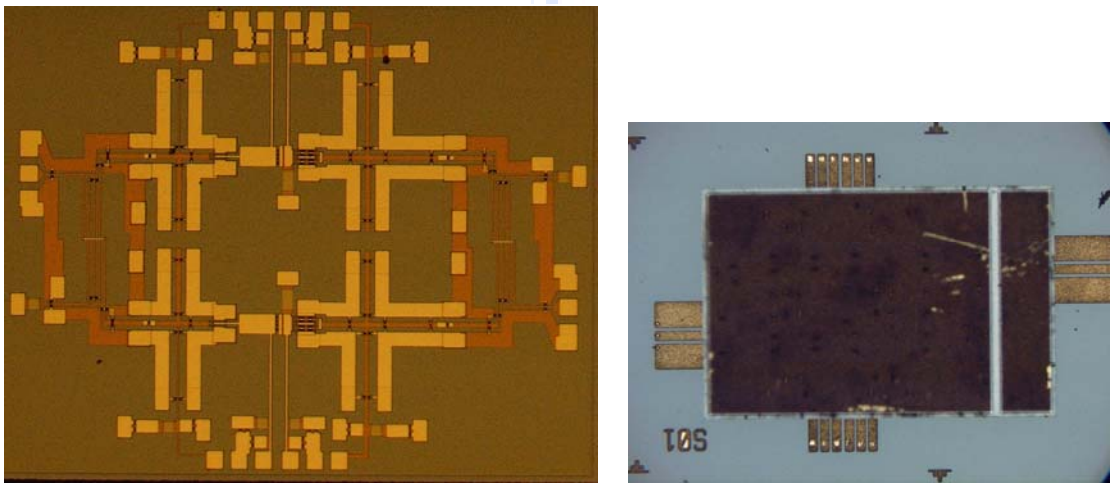
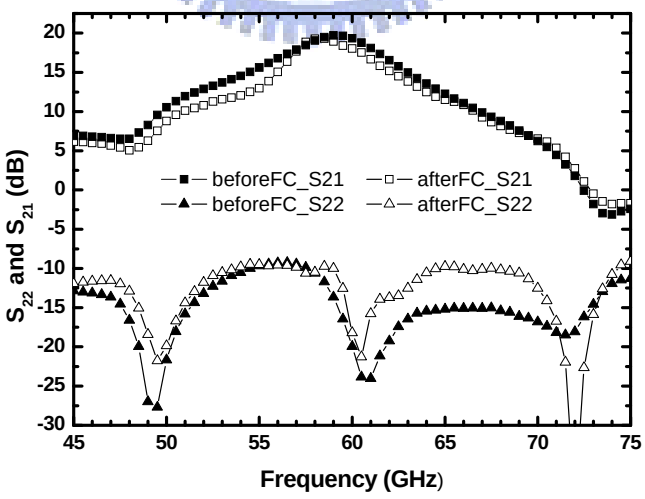
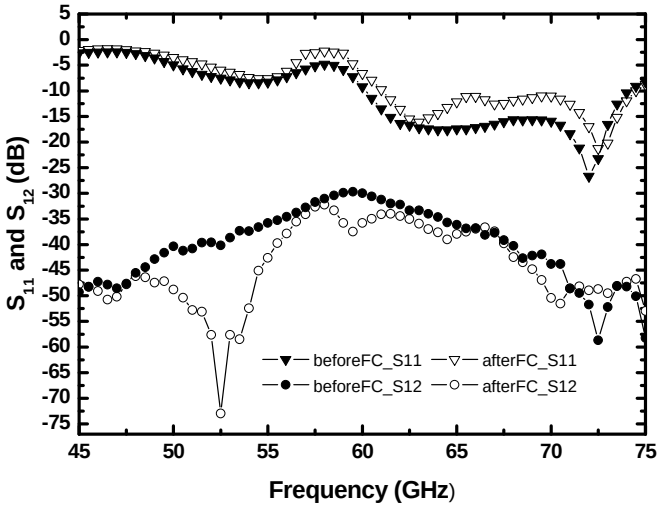


Fig.C-4 (a) Die photograph of the balanced amplifier with the CPW Lange coupler and (b) a photo of the V-band balanced amplifier with flip-chip technology.

Figure C-5 shows that measured S parameters of the balanced amplifiers with/without the flip-chip bonding. The S_{21} are 19.32 dB and 18.0 dB at 60 GHz and the minimum S_{22} are -20.0 and -18.2 dB at 60 GHz without and with the flip-chip technology, respectively. The S_{21} curve of the bonded amplifier agrees well with that of the bare one. All S_{22} values are almost better than 10 dB. The lower input return loss (S_{11}) is 16 dB after flip-chip and 17 dB before flip-chip at 63 GHz. S_{12} curves are below -30 dB anywhere. Fig. C-6 shows the output power of the amplifier. The OP_{1dB} equals 13.5 dBm and 12 dBm, and saturation output power is 17 dBm and 15 dBm at 60 GHz before and after flip-chip technology, respectively. Apparently, the flip-chip bonding has a little effect on the CPW input/output amplifier. Hence, the CPW design is more suitable for the flip-chip bonding than the MS design does.



(a) S_{21} and S_{22}



(b) S_{11} and S_{12}

Fig.C-5 Measured S-parameters of the V-band balanced amplifier.

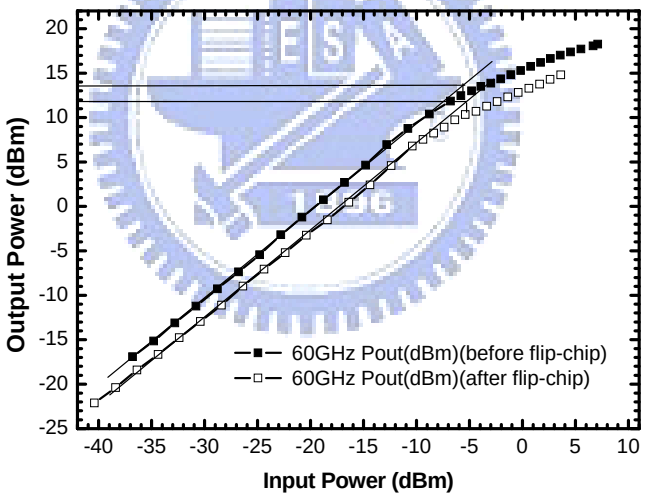


Fig.C-6 Measured power performance of the balanced amplifier.

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籍　貫：彰化

學　歷：私立逢甲大學電子工程系學士 (86年9月 ~ 90年6月)
國立中央大學電機研究所碩士 (90年9月 ~ 92年6月)
國立交通大學電信研究所博士 (92年9月 ~ 98年6月)

論文題目：應用類比電路設計及覆晶封裝技術於毫米波高速電子遷移率電晶體之收發機


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Publication List

（A）Significant Journals

[1] **Jen-Yi Su**, Sheng-Che Tseng, Chinchun Meng, Po-Yi Wu, Yueh-Ting Lee and Guo-Wei Huang, "Ka/Ku-band PHEMT Gilbert mixers with polyphase and coupled-line quadrature generator," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 5, pp. 1063-1073, May 2009.

[2] **Jen-Yi Su**, Chinchun Meng, and Po-Yi Wu, "Q-band pHEMT and mHEMT subharmonic Gilbert upconversion mixers," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 2, pp. 392-394, Jun. 2009.

[3] **Jen-Yi Su**, Chinchun Meng, Yueh-Ting Lee and Guo-Wei Huang, "Compact CPW-MS-CPW two-stage pHEMT amplifier compatible with flip chip technique in V-Band frequencies," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 6, pp. 112-114, Feb. 2008.

（B）International Journals

[1] **Jen-Yi Su**, Chinchun Meng, Po-Yi Wu and Guo-Wei Huang "0.13-μm CMOS Q-Band Leveled-LO Subharmonic Mixer with Injection-Locked Frequency-Divider Quadrature Generator," *MICROWAVE AND OPTICAL TECHNOLOGY LETTERS*, to be published, 2009.

[2] C. C. Meng, S. C. Tseng, Y. W. Chang, **J. Y. Su**, and G. W. Huang, "Low-phase-noise transformer-based top-series QVCO using GaInP/GaAs HBT technology," *MICROWAVE AND OPTICAL TECHNOLOGY LETTERS*, vol. 49, no. 1, pp. 215-218, Jan. 2007.

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[4] Sheng-Che Tseng, Chinchun Meng, Shao-Yu Li, **Jen-Yi Su** and Guo-Wei Huang, "Single-ended frequency divider with moduli of 256~271," *MICROWAVE AND OPTICAL TECHNOLOGY LETTERS*, vol. 48, no. 10, pp. 2096-2100, Oct. 2006.

[5] C. C. Meng, **J. Y. Su,** B.C. Tsou, and G.-W. Huang, "The effect of selectively and fully ion-implanted collector on RF characteristics of BJT devices," *IEICE Tran. Electron.*, vol. E89-C, no. 4, pp. 520-523, Apr. 2006.

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[7] C. C. Meng, **J. Y. Su** and S. M. Yang, "Analysis of dc characteristics and small signal equivalent circuit parameters of GaAs metal－semiconductor field effect

transistors with different gate lengths and different gate contours by two-dimensional device simulations," *Japanese J. of Appl. Phys*, vol. 44, no. 9A, pp. 6389-6394, Sept. 2005.

（C）Significant Conferences

[1] **Jen-Yi Su**, Chinchun Meng, Po-Yi Wu and Guo-Wei Huang," 40-GHz CMOS subharmonic Gilbert mixer with quadrature injection-locked frequency divider," *APMC'2008*, 2008.

[2] C. C. Meng, S. C. Tseng, Y. W. Chang, **J. Y. Su** and G. W. Huang, "4-GHz low-phase-noise transformer-based top-series GaInP/GaAs HBT QVCO," *IEEE MTT-S 2006*, pp. 1809-1812, Jun. 11-16, 2006.

[3] **Jen-Yi Su**, Chinchun Meng, Yang-Han Li, Sheng-Che Tseng and Guo-Wei Huang," 2.4 GHz 0.35 um CMOS single-ended LNA and Mixer with gain enhancement techniques," *APMC'2005*, vol. 3, pp. 1550-1553, Dec. 2005.

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