CHPATER 5

PROCESSING AND DEVICE CHRACTERIZATION OF ALGAN/GAN HIEH ELECTRON MOBILITY TRANSISTORS

GaN based High Electron Mobility Transistors (HEMTs) have emerged as a promising candidate for microwave (f > 1GHz) power amplification [1-3], with applications ranging from satellite links to wireless communication. In late 1990s, AlGaN/GaN, AlGaInN/GaN, AlGaInN/InGaN power HFETs grown on sapphire, the insulating 4H-SiC, conducting SiC, and even bulk GaN have demonstrated much larger output powers and have become promising contenders for a variety of high power amplification and switching applications. Moreover, the using of wide bandgap semiconductors in power amplifiers increase not only the output power, but also extends the temperature tolerance and the radiation hardness of the circuits. The latter is corroborated by demonstrated operation of GaN-based HFET at 750℃ [4]. In terms of power density, GaN HEMT's on sapphire substrates have achieved 3.3 W/mm at 18 GHz [5]. In previous chapters, we developed the etch techniques (PEC wet etch and ICP dry etch) and metallization techniques (Ohmic and Schottky contacts) which will be further applied to the device fabrication in this chapter. The goal is not to fabricate a super device for power output or high-frequency operation. In stead, we intended to demonstrate the feasibility of high temperature operation of GaN-based devices by using the techniques developed here. Finally, room temperature to 330℃ DC characteristics of GaN HEMT fabricated using the PEC etch and WN T-gate will be demonstrated and discussed in the last section.

5.1 Processing for AlGaN/GaN HEMT

Cleaning is very important step for device fabrication. All the process study here used the following cleaning procedure.

(1) ACE 5min.

(2) IPA 4 min.

(3) D.I. water rinse 1 min.

(4) N2 dry.

(5) HCl: H2O=1:10 5 min.

(6) D. I. rinse 10 min.

(7) N2 dry.

Except for the WN_x T-gate, the photoresist and developer used for lithography were AZ6112 and PFD0005, respectively. For WNx T-gate, the PMMA/MMA bilayer was used which will be described in later section. In the following sections, we will describe the processing procedures in details and also discuss the results of the device fabricated.

5.1-1 Isolation

Isolation serves a serial of purposes: (1) in actives devices, it restricts the current flowing to the desired path that is under the gate in FETs; (2) electrically isolates separated devices from each other; (3) reduces parasitic capacitance and resistance; (4) provide a good electrical isolation between discrete devices by etching away portions

of the electrically active surface layer, leaving the mesas of the active layer in the desired location. Two kinds of isolation method were used, one is mesa isolation by etching method, and the other is isolation by implantation. The device structure used in isolation study is 100Å n-GaN/500Å followed by $Al_{0.1}GaN_{0.9}N$/2μm u-GaN, the structure has a 2DEG mobility of 800 cm^2/Vs.

For mesa isolation, the etching depth target was 2500 Å. The device was etched to the upper region of the intrinsic GaN buffer layer, which is under unintentional doped (UID) AlGaN layers in our structure. After photolithography, 1500 Å of Ni mask was deposited for the purpose of serving as hard mask. An etching solution composed of HNO_3 and H_2O in D.I. water with proportional ratio 1:3 was employed to define the mesa area. The etching profile was calibrated by an surface profiler, α-step. The leakage current measured on the Iso-key is well under $1x10^{-10}$ amperes below 10 volts and $2x10^{-6}$ amperes at 20 volts. Even after thermal annealing high to 900℃, there was no big difference in the leakage current.

For ion-implantation isolation, O^+ was implanted with an ion energy 150 KeV and $5x10^{13}cm^{-3}$ of dosage. The intended implantation depth was 1800Å. A 2μm of photoresist was deposited as a mask to prevent the ions from damaging the undesired (active) region. The leakage current was measured on the isolation key. The Ohmic contact used here, for simplicity, is Ti/Al/Ni/Au. Thermal annealing was performed on this contact to check its high temperature tolerance from 430℃ to 900℃ which was basically the range of annealing temperature for Ohmic contact.

Figure 5-1(a) is measured on the Iso-key. The distance between the pads is 150 μm. No mater what kinds of isolation techniques we used; the leakage currents were almost the same. At low bias (under 10V), the leakage current was less than $1x10^{-10}$ amperes, even at 20 volts the leakage current is still less than $1x10^{-6}$ amperes. This implied that the isolation is very good at R.T. for both techniques we used. Figure 5-1

(b) is the leakage current between two adjacent devices. It showed the same result. However, as shown in Fig. 5-2, after thermal annealing, the implantation isolation seemed to be getting worse as the temperature was increased. This should be due to the recrystallization of the lattice. This suggests that either the implantation isolation needs to be further optimized or the devices could not endure high temperature processing after implantation.

5.1-2 Ohmic Contact

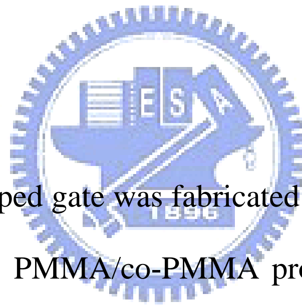
The metallization process is as described in chapter 4. After isolation, we applied the metallization techniques developed in chapter 4 onto the HEMT structure. For high temperature applications, Ti/Al/Pt/Au was used as the Ohmic contact to test the thermal tolerance. For un-capped HEMT (**without** n-GaN on top of AlGaN/GaN HEMT) study, Ti/Al/Pt/Pt was used as Ohmic contact. As shown in Fig. 5-3, the device structure was 500Å $Al_{0.1}Ga_{0.9}N$/ 2 μmGaN, the saturation current without gate was about 27 mA/mm in this case.

5.1-3 N-GaN Cap Etch

Some of the HEMT structures used here were capped by n-GaN on the top layer, as 100Å n-GaN/500Å u-$Al_{0.1}Ga_{0.9}N$/2 μm u-GaN. The top n-GaN layer is used for Ohmic contact formation as well as to diminish the surface states near the active region. However, it is not able to form good Schottky contact because it's highly doped. The Schottky contact was made with the contact Schottky metal contact to u-AlGaN, the top n-GaN should be removed for gate formation. PEC etch it was used for this purpose. Since we have discussed the etching damages caused by ICP in

chapter 3. The PEC wet etch condition was 0.05 M of KOH $_{(aq)}$, 300 mW/cm^2 of Hg-Arc lamp. If the cap is not removed, there would be a parallel conduction along the top n-GaN layer. Figure 5-4 (a) and (b) show the difference of the saturation current before and after n-cap removal. Before cap removal, the saturation current was about 200 mA/mm, this was due to the parallel conduction in the cap layer. After cap was removed, the saturation current is about 60 mA/mm, as shown in Fig. 5-4 (b), and decrease with the thickness removed. This is an application of PEC wet etch on the GaN HEMT fabrication. Gate-recessing was very common in AlGaAs/GaAs PHEMT fabrication, especially in enhanced mode HEMT. With proper etch at the gate region the source resistance of the device can be reduced.

5.1-4 T-Gate Formation



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The Ni/Au or WN_x T-shaped gate was fabricated by using the PMMA/co-PMMA bi-layer resist technique. The PMMA/co-PMMA profile defined the T-shaped gate and gate recess. Gate metal deposition was performed with this bi-layer resist. For the Ni/Au T-gate, an E-beam evaporation system was used for gate metal deposition. In the other hand, the WN_x was deposited by reactive sputtering system as described in chapter 4. It's straightforward to obtain a 0.7μm T-shaped Ni/Au gate after lift-off. Figure 5-5 shows the Ni/Au T-gate formed after lift-off. However, for the WN_x T-gate, it's very different. Due to the characteristic of superior step coverage of the sputtering process, it is difficult to lift-off the WN_x as E-beam evaporation process. Because the residuals on the side wall of photoresist made it difficult in precisely defining the gate length and width. To remove the WN_x residuals on the side wall of the photoresis, thin Ti/Au films were deposited by e-beam evaporation system as a metal mask and subsequent etch by RIE was employed to remove the WN_x on the side-wall. RIE

played an eraser for cleaning the residual films through controlling the atmosphere in RIE chamber. The RF power was 50W and the chamber pressure was 70 mtorrs. CF_4 and O_2 gases were used as the plasma sources to etch WN_x films. Due to the chemical stability of Au in the plasma, it is very suitable to serve as a hard mask in this process. Collocating with WN_x sputtering and Ti/Au hard mask fully utilized different lithography properties in the WN_x gate. RIE etchant conditions such as etchant percentage, chamber pressure, RF power should be seriously emphasized. As two points described above were done, WN_x gate would be well formed.

In contrast, to form Ni/Au T-gate needs less process that WN_x T-gate does. Figure 5-5 shows the Ni/Au T-gate by lift-off process. Due to evaporation of Ni/Au by E-beam has worse step coverage, there was no residuals on the side wall of the photoresist. Consequently, there is no necessary of Ti/Au mask and RIE process for Ni/Au T-gate.

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5.1-5 Passivation

GaN surface is very sensitive and contains many many surface states. Long-term degradation under high temperature can occur through processes such as oxidation or particulate contamination. After formation of source, drain, and gate electrodes, a dielectric film passivated the device. Dielectric films are typically used in GaAs process for environmental encapsulation. The dielectric film keeps humidity, chemicals, gases, and particles away from sensitive areas of the device. This also protects the surface of the device from environmental contamination and mechanical damage. Silicon nitride (Si_3N_4) was used for passivation in the study, obtained by using plasma-enhanced chemical vapor deposition (PECVD). The film thickness is about 1000Å and the reflective index is about 2.0. Then, contact via hole was formed

by photolithography and reactive ion etching (RIE) [6] was performed to etch the silicon nitride film.

5.2 DC Characteristics of AlGaN/GaN HEMTs at High Temperature

Figure 5-7 (a) shows the I-V curves of an AlGaN/GaN HEMT with incomplete removal of the n-GaN cap layer. A normal transistor should have I-V curves as shown in Fig. 5-7 (b), though the current is low for this transistor. Better I-V curves could be found as in Fig. 5-8. It's a WNx T-gate AlGaN/GaN HEMT with a periphery of 125 μ m. The pinch off voltage was well below 1.5V, and the saturation current at room temperature was about 40 mA/mm. Figure 5-9 (a) shows the transconductances of the device at various gate biases. In comparison with the literatures, the application current density is very low. On the other hand, the breakdown voltage is very high as shown in Fig. 5-9 (b). This implies that the processing technology is good. So, the low transconductance should be mainly related to the quality issues of epitaxy.

The high temperature performance of the WN_x T-gate HEMT would be emphasized here. The DC characteristics of the WN_x T-gate $Al_{0.1}Ga_{0.9}N$/GaN were measured at different ambient temperatures from 25℃ to 330℃. Figure 5-10 shows the test results. As expected, the saturation currents at zero bias decrease with the increase of the test temperature. This is obviously due to the thermal scattering effect. In addition, there are negative resistance phenomena at moderate high temperatures. Two possible reasons can explain the phenomena, one is Gunn Effect, and the other is the D_0X center trapping effect. If it was Gunn Effect, the negative conductivity (resistance) should happen at any gate bias. To verify this, we compared the I-V curves that measured with and without light exposures. The current collapse phenomenon was much more obvious without light exposure. The current collapse

phenomena before pinch-off were very obvious at 100℃ and 200℃. This could be due to the deep level trapping effect. Current collapse (CC) is a trap-related phenomenon that severely limits the output power of FETs, and has been observed in Si metal-oxide-semiconductor FETs [7], $Al_xGa_{1-x}As$/GaAs modulation-doped FETs [8-9], in nitride-based $Al_xGa_{1-}N$/GaN heterostructure insulated gate FETs [10], and in GaN metal-semiconductor field-effect transistors (MESFET) [11]. The effect results from the trapping of hot carriers by deep centers located in regions of the device structure outside the conducting channel. The excess charge associated with the trapped carriers produces a depletion region in the conducting channel, which results in a partial pinch-off of the device and a severe degradation of the drain current characteristics. The effect could be reverses by liberating trapped carriers either thermally by emission at elevated temperatures or optically by photoinozation. In $Al_xGa_{1-}N$/GaN heterostructures it was suggested, by analogy with work done in $Al_xGa_{1-}As$/GaAs MODFETs, that the traps responsible were located in the $Al_xGa_{1-}N$ barrier layer [11]. In the GaN MESFETs, it was assurmed that the high-resistivity (HR) GaN insulating layer was the source of the trapping centers [11]. There have been several studies of the effect of light on CC. For example, Kastalsky and Kieh [8] measured the spectral dependence of the conductance in an $Al_xGa_{1-}As$/GaAs heterjunction test structure, and concluded that the collapse resulted from processes in the $Al_xGa_{1-}As$ layer. Khan *et al.* observed increases in the drain current of an $Al_xGa_{1-}N$/GaN HIGFET near 360 nm, corresponding to the AlGaN band edge, and near 650 nm, which was associated with an unidentified deep trap. Similarly in GaN MESFETs, Binari *et al.* observed an optically induced restoration of the drain current that decreased dramatically in effectiveness with the increasing wavelength. Figure 5-13 shows the DC characteristics measured with exposure to light that depicts the deep level defects existing in the devices.

In summary, we demonstrated the high temperature durable WN_x T-gate AlGaN/GaN HEMTs with operation temperatures up to 330℃. The WN_x T-gate was fabricated by sputtering and etch-lift-off process and the WN_x-T Gated HEMT was proven to work well at high temperatures. The gate recessing by PEC wet etch was also demonstrated and showed that it's a promising method for fabricating damage-free gate recess process. The DC characteristics for various recessed-gate showed that PEC wet etch was a very practical technique in AlGaN/GaN HEMT fabrication. The Ti/Al/Pt/Au Ohmic metal used also worked well at high temperatures. The low transconductance and current collapse phenomena showed that there were still a lot to improve in AlGaN/GaN epitaxial film quality, especially in AlGaN material. Although the DC properties of the WN_x-gate HEMT needs further improvement, the etch techniques developed here, the metallization schemes of the Ohmic and the Schottky contacts were proven promising for the fabrication for high temperature operating AlGaN/GaN HEMTs.

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