# Test Structure on SCR Device in Waffle Layout for RF ESD Protection

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***Abstract*—With the highest ESD level in a smallest layout area, SCR device was used as effective on-chip ESD protection device in CMOS technology. In this paper, a waffle layout test structure of SCR is proposed to investigate the current spreading efficiency for ESD protection. The SCR in waffle layout structure has smaller parasitic capacitance under the same ESD robustness. With smaller parasitic capacitance, the degradation on RF circuit performance due to on-chip ESD protection device can be reduced. The proposed waffle SCR is suitable for on-chip ESD protection in RF applications.**

***Index Terms* — Electrostatic discharges (ESD), radio-frequency integrated circuit (RF IC), silicon-controlled rectifier (SCR).**

## I. INTRODUCTION

Electrostatic discharge (ESD) is the major reliability issue for integrated circuits (ICs), including radio-frequency integrated circuits (RF ICs). Against ESD damages, ESD protection device must be included in RF ICs, as shown in Fig. 1. However, the parasitic capacitance ($C_{ESD}$) of ESD protection device introduces negative impacts to RF circuits [1], [2]. The parasitic capacitance will disturb the high frequency signals and induces RC delay in the signal path. For a 5-GHz low-noise amplifier (LNA) in an RF receiver, a typical specification on the total input loading capacitance is in the order of 100 fF, including the ESD protection device and the bond pad. Therefore, the parasitic capacitance of ESD protection device must be minimized. Namely, device with large ratio of ESD robustness to parasitic capacitance is desired. The figure of merit (FOM) used in this work is $V_{MM}/C_{ESD}$, where $V_{MM}$ is the machine-model (MM) ESD level and $C_{ESD}$ is the parasitic capacitance of ESD protection device.

Silicon-controlled rectifier (SCR) device had been reported as useful RF ESD protection element [3]. The equivalent circuit schematic and the I-V characteristics of SCR device are shown in Fig. 2. The SCR device has a much higher ESD robustness within a smaller device size than other ESD protection devices, such as diode, MOS, BJT, or field-oxide device, because of the low holding voltage ($V_{hold}$, about ~1.5 V in general bulk CMOS processes) of the SCR device [4]. With the smaller device size, using SCR as ESD protection device will cause less parasitic capacitance. Thus, implementing RF ESD protection by using SCR device can achieve the better FOM of $V_{MM}/C_{ESD}$.

As the SCR device under ESD stresses, ESD current primarily flows through the edges of SCR device. So the ESD level will depend on the perimeter of SCR device. However, the parasitic capacitance primarily exists on the bottom plate of SCR device, i.e., the area of SCR device. Therefore, the FOM of $V_{MM}/C_{ESD}$ is in proportion to the ratio of perimeter to area of the SCR device. The ratio of perimeter to area of the SCR device is

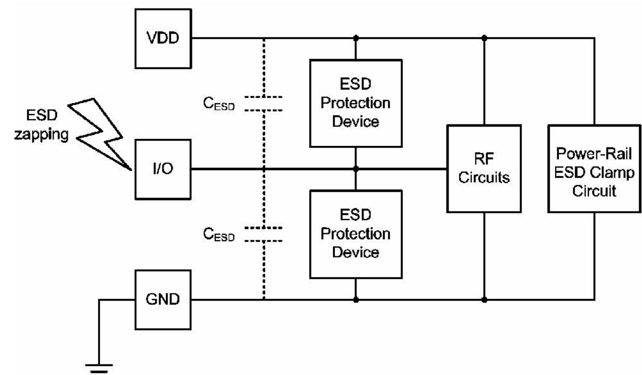
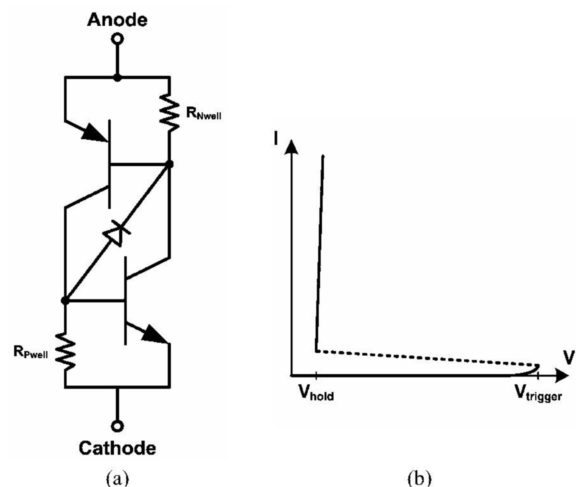



Fig. 1. A general concept of on-chip ESD protection in RF ICs.




(a) (b)

Fig. 2. (a) Equivalent circuit schematic, and (b) I-V characteristics, of a SCR device.

$$\frac{Perimeter}{Area} = \frac{2(W+L)}{W \cdot L} = \frac{2}{L} + \frac{2}{W}. \tag{1}$$

where W and L are the width and the length of SCR device, respectively. The maximized ratio of perimeter to area will be achieved as the width and the length are both minimum. If a slightly larger ESD level is desired, the width or the length of SCR device should be increased to extend the perimeter. The better method is to increase both width and length with the same ratio than with the different ratio. Therefore, the waffle SCR, which is with the same width and length, has the better FOM.

The MOS transistors in waffle layout structures had been studied [5]. The waffle layout structures for diodes had also been proposed to reduce its parasitic capacitance for ESD protection in high-speed I/O [6]. In this paper, SCR realized in the waffle structure is investigated in a 0.18-µm CMOS process. With the comparison between the traditional stripe SCRs and the waffle SCRs, the improvements from the new proposed waffle SCRs has been confirmed in silicon.

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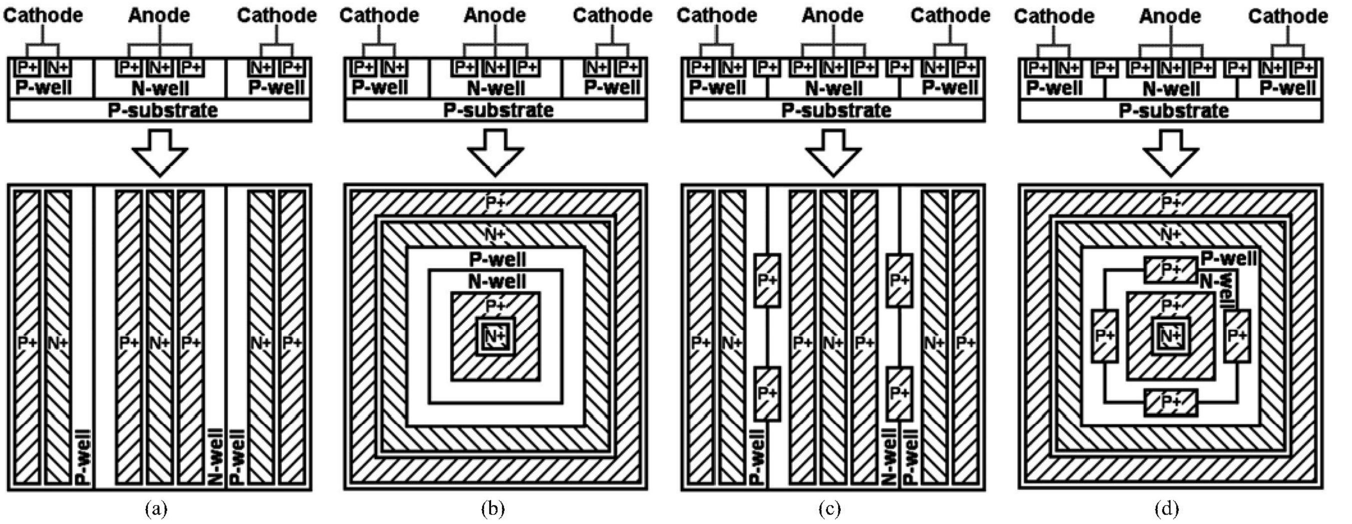


Fig. 3. Device cross-sectional view and layout top view of (a) stripe SCR (SSCR), (b) waffle SCR (WSCR), (c) stripe modified SCR (SMSCR), and (d) waffle modified SCR (WMSCR).

## II. SCR Structures

### *A. SCR in Stripe Layout*

Fig. 3(a) shows the traditional stripe layout for SCR (SSCR). The SCR is composed of four layers of P+/N-well/P-well/N+. The ESD currents primarily flow through two edges of the N-well of the stripe SCR.

### *B. SCR in Waffle Layout*

In Fig. 3(b), the waffle layout for SCR (WSCR) is proposed to discharge ESD current in four edges of the N-well. By using the waffle SCR, the parasitic capacitance, which primarily exists on the N-well/P-substrate junction, can be decreased and the FOM can be increased.

### *C. Modified SCR in Stripe Layout*

In Fig. 3(a) or 3(b), the trigger voltage ($V_{trigger}$) of SSCR or WSCR is the breakdown voltage of the N-well/P-well junction, which is often greater than the MOSFET breakdown voltage of internal circuits. In order to improve the turn-on efficiency and reduce the trigger voltage, the trigger diffusion is added across the N-well/P-well junction in the stripe modified SCR (SMSCR), as shown in Fig. 3(c), to reduce the junction breakdown voltage. Since the lager trigger diffusion may increase the parasitic capacitance, the SMSCR was implemented with different trigger diffusion areas to evaluate ESD performance and the device parasitic effects.

### *D. Modified SCR in Waffle Layout*

With the trigger diffusion across the N-well/P-well junction, the waffle modified SCR (WMSCR) is shown in Fig. 3(d). The WMSCR was also implemented with different trigger diffusion areas for silicon verification.

## III. Measurement Setup

The trigger voltage ($V_{trigger}$), the secondary breakdown current ($It_2$), and the turn-on resistance ($R_{on}$) in the holding region of the fabricated SCR devices were characterized by the transmission line pulsing (TLP) system. The human-body-model (HBM) and machine-model (MM) ESD robustness were evaluated by the ESD simulator.

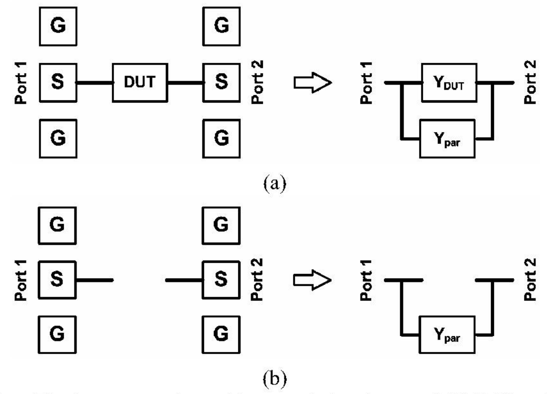


Fig. 4. The layout top view with ground-signal-ground (G-S-G) pads and the equivalent model of (a) including-DUT pattern and (b) excluding-DUT pattern.

The high-frequency S-parameters were measured under the bias of 0.9 V ($V_{DD}/2$ in a 0.18-µm CMOS process) by using vector network analyzer HP 8510C, then the Y-parameters were obtained from the measured S-parameters. Because the SCR devices were arranged with ground-signal-ground (G-S-G) pads to facilitate on-wafer measurement, the intrinsic characteristics of the SCR device in high frequency are embedded within the parasitic effects of metal interconnects and bond pads. To de-embed the intrinsic characteristics of the SCR device, the test patterns shown in Fig. 4, one including the device under test (DUT) while the other excluding the device under test, were fabricated in the same chip. Then, the intrinsic device behaviors ($Y_{DUT}$) can be obtained by subtracting $Y_{par}$ from $Y_{meas}$, where $Y_{meas}$ is the Y-parameter of the including-DUT pattern and $Y_{par}$ is the Y-parameter of the excluding-DUT pattern. Finally, the parasitic capacitance of SCR device can be extracted from the $Y_{DUT}$ by using

$$C_{ESD} = \frac{Im(Y_{11})}{2\pi f}. \qquad (2)$$

## IV. Experimental Results

The measured results on the characteristics of the fabricated SCRs are listed in Table I. The TLP I-V curves and leakage currents for SSCR and WSCR are shown in Fig. 5(a) and 5(b), respectively. Excluding the difference in trigger

voltages, the similar I-V curves and leakage currents are found in the other SCR patterns. The trigger voltages among the SCR devices under different layout structures are compared in Fig. 6. Both SSCR and WSCR are triggered at about 16-17 V. With the trigger diffusion added into the modified SCRs in the stripe and waffle structures, the trigger voltages were reduced to 12-13 V. The TLP-measured turn-on resistances of the stripe and the waffle SCRs in high-current holding region are as low as ~1 Ω. The secondary breakdown currents of all SCR devices exceed 6 A. The HBM ESD levels of all SCR devices exceed 8 kV, and MM ESD levels are within the range of 1.5-1.8 kV, as listed in Table I.

The S-parameters between 2.4 GHz and 5 GHz of the stand-alone pad, SSCR, and WSCR are shown in Fig. 7. The parasitic capacitance of each SCR is extracted from the measured S-parameter by using aforementioned method. Fig. 8 shows the extracted capacitances from 2.4 GHz to 5 GHz of the SSCR and WSCR.

The FOM ($V_{MM}/C_{ESD}$) between the SCR devices under different layout structures are compared at 2.4 GHz and 5 GHz (for wireless LAN applications) in Fig. 9(a) and 9(b), respectively. Each FOM of waffle structure devices has an increase of about 25%, as compared with the traditional stripe SCRs. Although the FOM is decreased with the increase of the trigger diffusion area, the trigger voltage can be reduced to effectively protect the internal circuits. The SCRs with waffle structures have the better FOM in high frequency.

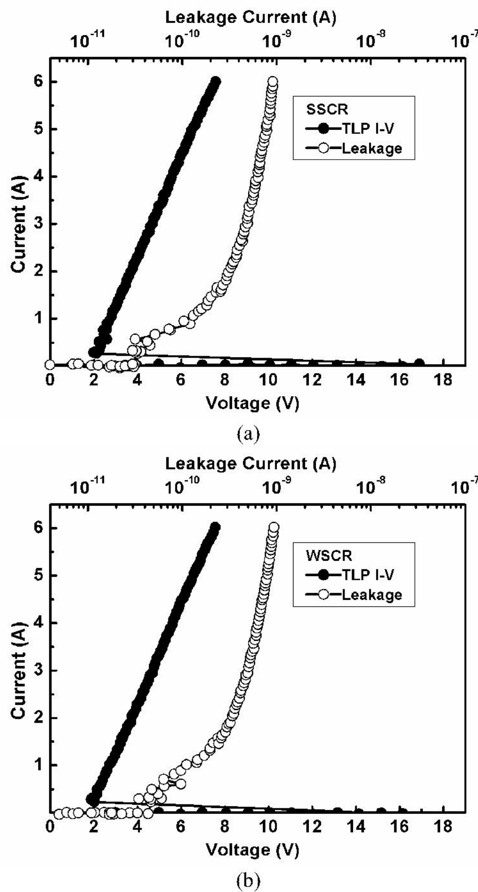


Fig. 5. The I-V characteristics and the leakage current of (a) SSCR and (b) WSCR.

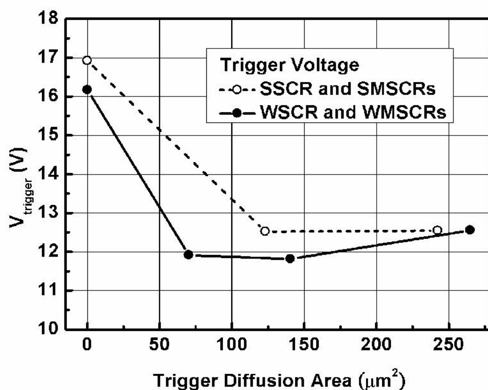


Fig. 6. The dependence of trigger voltages ($V_{trigger}$) on the trigger diffusion area of SCR devices under different layout structures.

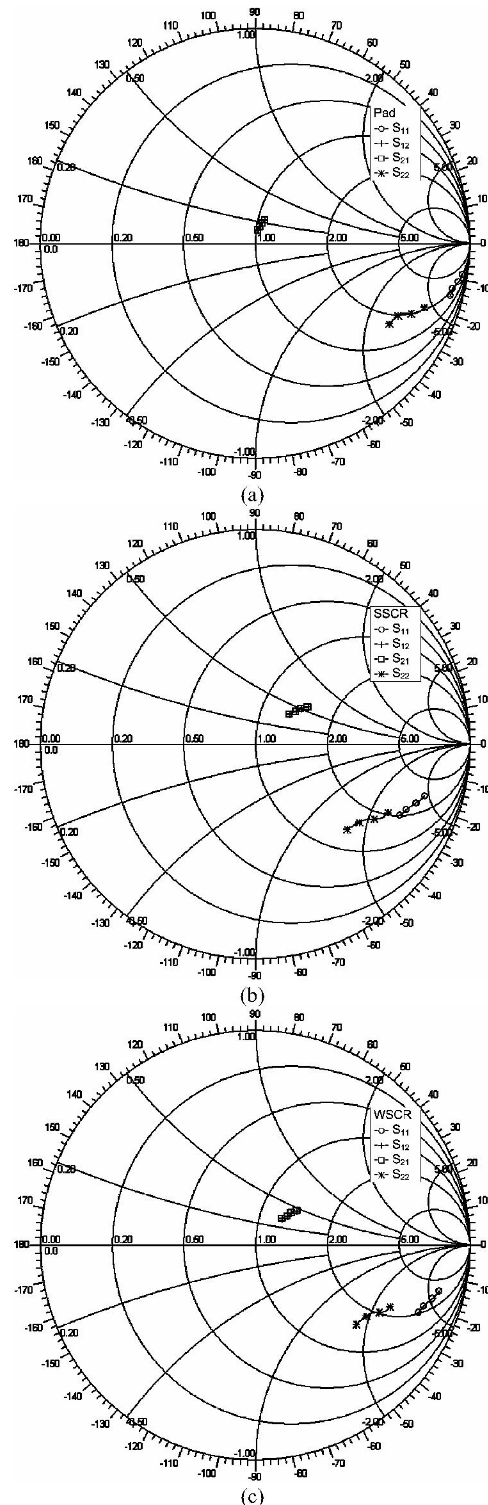


Fig. 7. The S-parameters between 2.4 GHz and 5 GHz of (a) stand-alone pad, (b) SSCR, and (c) WSCR.

TABLE I

COMPARISONS ON THE MEASURED DEVICE CHARACTERISTICS OF SCR UNDER DIFFERENT TEST STRUCTURES

| Structure | Name | Device Size ($\mu m^2$) | Trigger Diffusion Area ($\mu m^2$) | $V_{trigger}$ (V) | $R_{on}$* ($\Omega$) | $It_2$* (A) | $V_{HBM}$ (kV) | $V_{MM}$ (kV) | $C_{ESD}$@2.4 GHz (fF) | $C_{ESD}$@5 GHz (fF) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Stripe** | **SSCR** | **60.62×60.62** | **0** | **16.92** | **0.95** | **> 6** | **> 8** | **1.80** | **118.51** | **87.01** |
| **Stripe** | **$SMSCR_1$** | **60.62×60.62** | **123.2** | **12.52** | **1.09** | **> 6** | **> 8** | **1.63** | **178.47** | **132.92** |
| **Stripe** | **$SMSCR_2$** | **60.62×60.62** | **242.48** | **12.54** | **1.02** | **> 6** | **> 8** | **1.68** | **212.81** | **154.07** |
| **Waffle** | **WSCR** | **60.62×60.62** | **0** | **16.17** | **0.96** | **> 6** | **> 8** | **1.53** | **77.17** | **57.22** |
| **Waffle** | **$WMSCR_1$** | **60.62×60.62** | **70.24** | **11.91** | **1.08** | **> 6** | **> 8** | **1.52** | **115.39** | **87.94** |
| **Waffle** | **$WMSCR_2$** | **60.62×60.62** | **140.48** | **11.81** | **1.10** | **> 6** | **> 8** | **1.59** | **139.63** | **103.62** |
| **Waffle** | **$WMSCR_3$** | **60.62×60.62** | **264.96** | **12.55** | **1.22** | **> 6** | **> 8** | **1.56** | **165.25** | **119.05** |

*** measured by TLP (transmission line pulsing) system.**

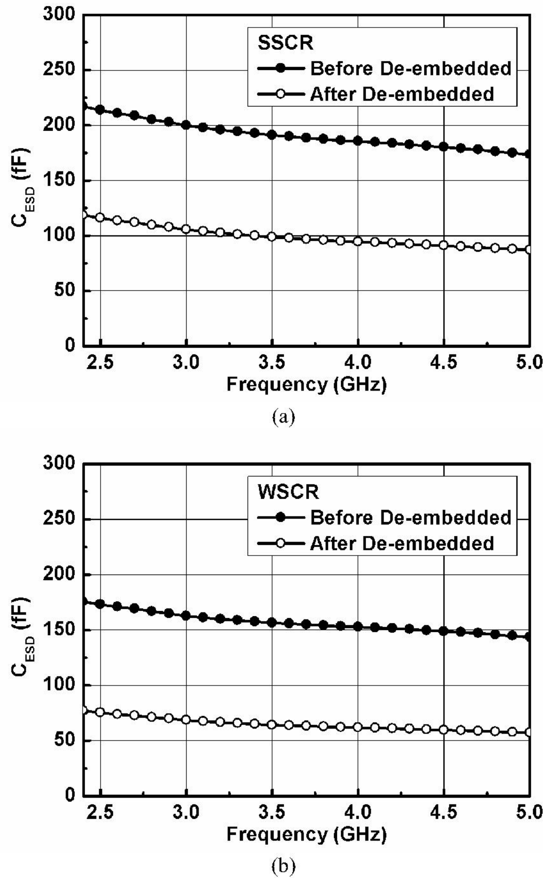


Fig. 8. The extracted capacitances of (a) SSCR and (b) WSCR from 2.4 GHz to 5 GHz.

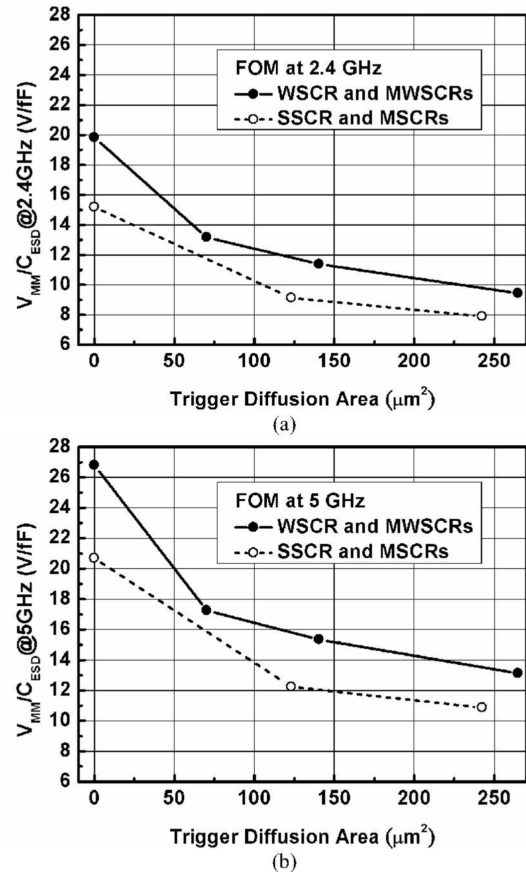


Fig. 9. The dependence of FOM ($V_{MM}/C_{ESD}$) on trigger diffusion area of SCR devices under different layout structures at (a) 2.4 GHz and (b) 5 GHz.

## V. CONCLUSIONS

The waffle layout structure has been demonstrated to improve ESD robustness with small parasitic capacitance. The SCR devices with waffle structures have also been verified to have better FOM ($V_{MM}/C_{ESD}$) ratio. Thus, the SCR realized in the proposed waffle layout structure is more suitable for RF ESD protection than the SCR realized in the traditional stripe layout.

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