Low-capacitance ESD protection design for high-speed I/O interfaces in a 130-nm CMOS process

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ABSTRACT

Electrostatic discharge (ESD) protection design for high-speed input/output (I/O) interface circuits in a 130-nm CMOS process is presented in this paper. First, the ESD protection diodes with different dimensions were designed and fabricated to evaluate their ESD levels and parasitic effects in gigahertz frequency band. With the knowledge of the dependence of device dimensions on ESD robustness and the parasitic capacitance, whole-chip ESD protection scheme were designed for the general receiver and transmitter interface circuits. Besides, an ESD protection scheme is proposed to improve the ESD robustness under the positive-to-V_{SS} (PS-mode) ESD test, which is the most critical ESD-test pin combination. With a silicon-controlled rectifier (SCR) between the I/O pad and V_{SS}, the clamping voltage along the PS-mode ESD current path can be reduced, so the PS-mode ESD level can be improved. Besides, the parasitic P-well/N-well diode in the SCR can provide the NS-mode ESD current path. Thus, SCR is the most promising ESD protection device in ESD protection design with low-capacitance consideration. The ESD protection scheme presented in this paper has been practically applied to an IC product with 2.5-Gb/s high-speed front-end interface.

1. Introduction

With the advantage of low cost and high integration capability, more and more integrated circuits (ICs) have been fabricated in CMOS processes, including the high-speed input/output (I/O) interface circuits. Electrostatic discharge (ESD), which has been one of the most important reliability issues for CMOS ICs, must be taken into consideration during the design phase [1]. To achieve satisfactory high-speed circuit performance, high-speed I/O interface circuits have been fabricated in nanoscale CMOS processes due to the advantage of superior high-frequency device characteristics. With the reduced gate-oxide thickness and lower gate-oxide breakdown voltage, nanoscale MOS transistors are very vulnerable to ESD, because ESD does not shrink with CMOS processes. Recently, several ESD protection designs for high-speed I/O applications have been reported [2–6], and the negative impacts of ESD protection circuits on high-speed I/O interfaces have been studied [7,8]. Diodes have been used to protect the dual-channel optical transceiver array [2]. To lower the overall capacitive load at the I/O pad, the ESD protection scheme with the T-coil and negative impedance converter has been reported [3]. In the silicon-controlled rectifier (SCR)-based ESD protection scheme, an RC-based ESD detection circuit and an NMOS have been used to draw the trigger current from the base terminal of the PNP BJT in the SCR un-

der ESD stresses [4]. Besides, a modified SCR with a low trigger voltage has been used to protect the DRAM with DDR3 interface [5]. Another design with the darlington-based SCR structure has been proposed to reduce the first breakdown voltage of SCR [6].

There are two major considerations in ESD protection design for high-speed I/O interfaces. First, ESD protection circuits for high-speed I/O interfaces must sustain high enough ESD robustness to effectively protect the thin gate oxide of the MOS transistor in the internal circuits against ESD stresses. Second, the high-speed circuit performance degradation due to the parasitic effects of the ESD protection devices needs to be minimized [9].

Traditional ESD protection devices with large dimensions, which have large parasitic capacitance, would significantly degrade the high-speed circuit performance. Therefore, traditional ESD protection designs with large ESD protection devices are no longer suitable for high-speed I/O applications because of the intolerable large parasitic effects. With proper design, the double-diode ESD protection scheme in cooperation with the active power-rail ESD clamp circuit can be used to realize the whole-chip ESD protection scheme for high-speed I/O applications with minimum degradation on the circuit performance.

In order to minimize the parasitic capacitance caused by the ESD protection devices and to achieve satisfactory ESD robustness, the high-frequency characteristics and the ESD levels of the ESD protection diodes in a 130-nm CMOS process were evaluated in this work to obtain the dependence of device size on ESD

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robustness and parasitic capacitance. After determining the dimensions of ESD protection diodes, whole-chip ESD protection scheme can be realized with the active power-rail ESD clamp circuit [10]. To investigate the ESD robustness of the general receiver and transmitter interface circuits with the proposed whole-chip ESD protection scheme, the receiver NMOS emulator and transmitter NMOS emulator were fabricated in a 130-nm CMOS process. In the receiver NMOS emulator and transmitter NMOS emulator, the I/O pad is connected to the gate terminal and drain terminal of the NMOS transistor, respectively. After investigating the ESD robustness of the receiver NMOS emulator and transmitter NMOS emulator, the positive-to-V_{SS} (PS-mode) ESD test was found to be the most critical ESD-test pin combination. Another ESD protection scheme using the substrate-triggered SCR between the I/O pad and V_{SS} is proposed in this work to improve the PS-mode ESD robustness. The proposed ESD protection schemes have been applied to a 2.5-Gb/s high-speed I/O interface circuit in a 130-nm CMOS process. Experimental results have shown that good high-speed circuit performance and high ESD robustness can be achieved simultaneously.

2. ESD protection diodes

The most popular ESD protection devices at the I/O pad are the shallow-trench-isolation (STI) diodes [11,12]. The device characteristics of the STI diodes in a 0.18-μm CMOS process have been investigated [13]. There are three diodes available in the 130-nm CMOS process, which are the P+/N-well diode, N+/P-well diode, and N-well/P-substrate diode. The P+/N-well diode is placed between the I/O pad and V_{DD}, because the N-well is often connected to V_{DD}. The layout top view and cross-sectional view of P+/N-well diode are shown in Fig. 1a and b, respectively. In a P+/N-well diode, the P+ diffusion is connected to the I/O pad, and the parasitic effects between the P+/N-well junction is contributed to the I/O pad. The size of the P+/N-well diode is referred to the size of the P+ diffusion. On the contrary, the N+/P-well diode is connected between the I/O pad and V_{SS}, because the P-well must be connected to V_{SS}. The layout top view and cross-sectional view of N+/P-well diode are shown in Fig. 2a and b, respectively. Since the N+ diffusion is connected to the I/O pad, the size of an N+/P-well diode is referred to the size of the N+ diffusion. Another ESD protection diode which can be used between the I/O pad and V_{SS} is the N-well/P-substrate diode, whose layout top view and cross-sectional view are shown in Fig. 3a and b, respectively. In the N-well/P-substrate diode, the N-well is connected to the I/O pad through the N+ diffusion. Thus, the size of the N-well region is the design parameter of the N-well/P-substrate diode. The dependence of ESD robustness on parasitic capacitance in a 130-nm CMOS process was investigated in this work to solve the trade-off between the ESD protection capability and the high-speed performance degradation. These three kinds of diodes with junction perimeters of 20, 40, and 80 μm have been designed and fabricated in a 130-nm CMOS process.
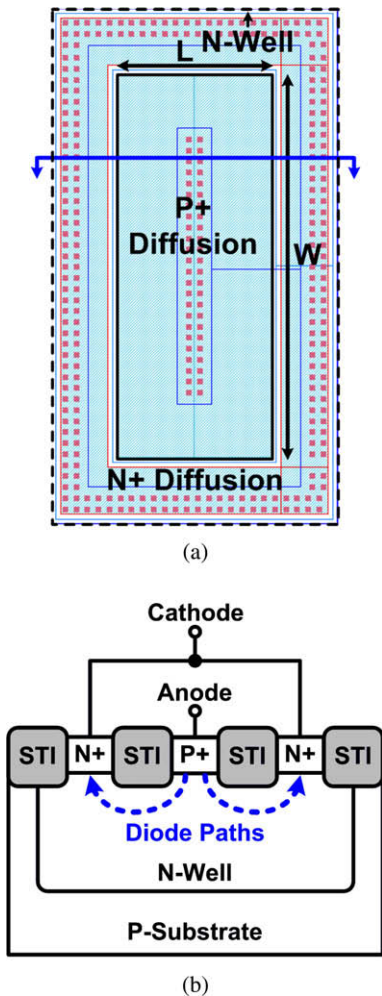

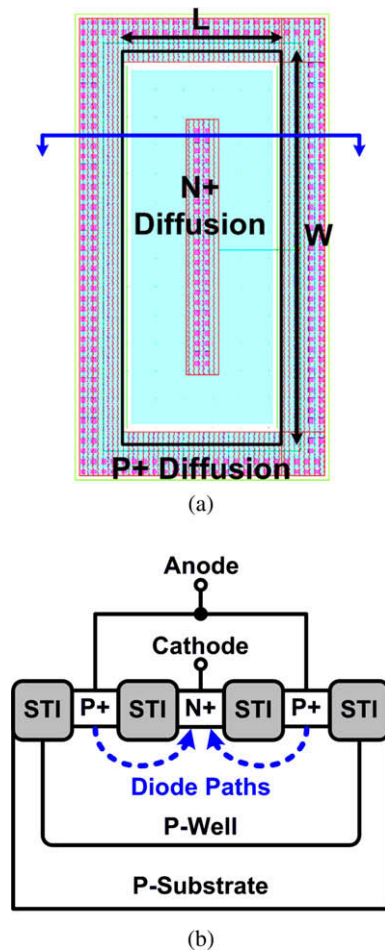**Fig. 1.** (a) Layout top view and (b) cross-sectional view of P+/N-well diode.

Fig. 2. (a) Layout top view and (b) cross-sectional view of N+/P-well diode.
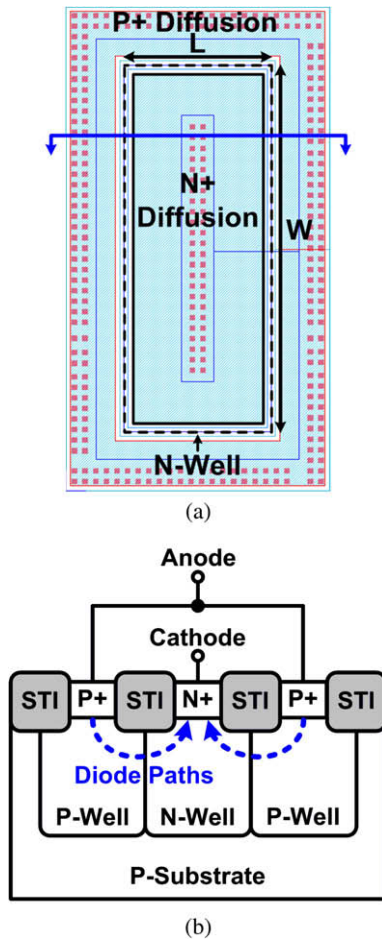
Fig. 3. (a) Layout top view and (b) cross-sectional view of N-well/P-substrate diode.

For high-speed I/O applications, the parasitic capacitance of the ESD protection diode is a key factor because it directly affects the high-speed circuit performance. To evaluate the parasitic capacitance of the ESD protection diodes, the two-port S-parameters of the fabricated ESD protection diodes were measured with the network analyzer. In the S-parameter measurement, port 1 and port 2 of the network analyzer were connected to the two terminals of the diode. Port 1 is connected to the terminal which is connected to the I/O pad when the ESD protection diode is applied to the high-speed I/O interface circuits. Port 2 is connected to the terminal which is connected to the AC ground node (V_{DD} or V_{SS}) when the ESD protection diode is applied to the high-speed I/O interface circuits. With the measured two-port S-parameters, the Y_{11}-parameter can be obtained with the conversions between two-port S-parameters and two-port Y-parameters, which is given by [14]

$$Y_{11} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{Z_0[(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}]} \quad (1)$$

where Z_0 is the termination resistance and is 50 Ω in this work. After obtaining the Y_{11}-parameter, the parasitic capacitance (C_{diode}) of the ESD protection diode was extracted by

$$C_{diode} = \frac{Im(Y_{11})}{\omega} = \frac{Im(Y_{11})}{2\pi f} \quad (2)$$

where Y_{11}-parameter is the admittance seen from port 1 with port 2 grounded, $Im(Y_{11})$ denotes the imaginary part of the Y_{11}-parameter, and f is the operating frequency. The extracted parasitic capacitances of the P+/N-well ESD protection diodes at 2.5 GHz are listed in Table 1. At 2.5 GHz, the extracted parasitic capacitances of P+/N-well diode with 20-, 40-, and 80-μm junction perimeters are 27.9, 51.1, and 77.7 fF, respectively. Tables 2 and 3 list the parameters of the N+/P-well and N-well/P-substrate ESD protection diodes, respectively. For the N+/P-well diode (N-well/P-substrate) diode, the extracted parasitic capacitances at 2.5 GHz under 20-, 40-, and 80-μm junction perimeters are 37.9 (40.5), 66.3 (69.3), and 89.7 fF (81.9 fF), respectively. The parasitic capacitance of the ESD protec-

Table 1
Characteristics of P+/N-well ESD protection diodes in a 130-nm CMOS process.

Junction perimeter (μm)	Junction area (μm²)	C_{diode} at DC (fF)	C_{diode} at 2.5 GHz (fF)	It2 (A)	HBM ESD level (kV)
P+/N-well diode					
20	25	25.9	27.9	0.62	1
40	75	75.7	51.1	1.47	3
80	150	151.4	77.7	4.18	6

Table 2
Characteristics of N+/P-well ESD protection diodes in a 130-nm CMOS process.

Junction perimeter (μm)	Junction area (μm²)	C_{diode} at DC (fF)	C_{diode} at 2.5 GHz (fF)	It2 (A)	HBM ESD level (kV)
N+/P-well diode					
20	25	20	37.9	0.55	1
40	75	58.1	66.3	1.56	3
80	150	116.2	89.7	3.75	6

Table 3
Characteristics of N-well/P-substrate ESD protection diodes in a 130-nm CMOS process.

Junction perimeter (μm)	Junction area (μm²)	C_{diode} at DC (fF)	C_{diode} at 2.5 GHz (fF)	It2 (A)	HBM ESD level (kV)
N-well/P-sub diode					
20	25	24.1	40.5	0.61	1
40	75	52.1	69.3	1.84	3
80	150	104.2	81.9	3.9	6

tion diode becomes larger when the diode size increases. Larger junction area and larger junction perimeter in the diode lead to larger junction capacitance. Besides, the zero-bias DC junction capacitance (C_{diode_DC}) can be calculated by using the SPICE model provided by the foundry, which is given by

$$C_{diode\_DC} = (Total\ Junction\ Area) \times C_j$$
$$+ (Total\ Junction\ Perimeter) \times C_{jsw} \qquad (3)$$

where C_j and C_{jsw} are the zero-bias bottom-plate capacitance per unit junction area and the zero-bias side-wall capacitance per unit junction perimeter, respectively. The values of C_j and C_{jsw} are provided in the SPICE model. As listed in Table 1, the calculated DC junction capacitances of the P+/N-well diode with 20-, 40-, and 80-μm junction perimeters are 25.9, 75.7, and 151.4 fF, respectively. From Tables 2 and 3, the calculated DC junction capacitances of N+/P-well (N-well/P-substrate) diodes under 20-, 40-, and 80-μm junction perimeters are 20 (24.1), 58.1 (52.1), and 116.2 fF (104.2 fF), respectively. Since C_j and C_{jsw} are different in N+/P-well and N-well/P-substrate diodes, the relationships between their DC junction capacitances under different dimensions are different. The difference between the extracted parasitic capacitance and the calculated junction capacitance is attributed to the parasitic series resistance in the well or substrate region, and the parasitic effects of metal routing.

Tables 1–3 also list the ESD levels of the P+/N-well, N+/P-well, and N-well/P-substrate ESD protection diodes, respectively. The characteristics of the fabricated ESD protection diodes in high-current regions were characterized by the transmission line pulsing (TLP) system with 10-ns rise time and 100-ns pulse width [15]. Moreover, the secondary breakdown current (It2) can be obtained in the TLP-measured I–V curve. It2 is the highest current that the device can handle under ESD stresses, which denotes the current at the failure point. The TLP-measured I–V curves of the stand-alone P+/N-well, N+/P-well, and N-well/P-substrate diodes with different dimensions under forward-biased condition are shown in Fig. 4. The It2 values of the P+/N-well diodes with 20-, 40-, and 80-μm junction perimeters are 0.62, 1.47, and 4.18 A, respectively. The It2 of the N+/P-well diodes with the junction perimeters of 20-, 40-, and 80-μm are 0.55, 1.56, and 3.75 A, respectively. As compared with the N+/P-well diodes, the N-well/P-substrate diodes have slightly higher It2 values. The It2 values of the N-well/P-substrate diodes with 20-, 40-, and 80-μm junction perimeters are 0.61, 1.84, and 3.9, respectively. Fig. 5 compares the It2 values of the ESD protection diodes with different device dimensions. As shown in Fig. 6, these three kinds of diodes exhibit identical human-body-model (HBM) [16] ESD levels under the same device. The HBM ESD levels are 1, 3, and 6 kV with the junction perimeters of 20, 40, and 80 μm, respectively. The measured HBM ESD levels are proportional to the device size, which demonstrates that good turn-on uniformity is achieved. Experimental results have shown that diodes with larger dimensions have higher ESD robustness, but larger diodes exhibit larger parasitic capacitance.

3. Whole-chip ESD protection design

To investigate ESD robustness of the typical receiver and transmitter interface with the ESD protection diodes and the power-rail ESD clamp circuit, the test circuits with the receiver NMOS emulator and transmitter NMOS emulator were implemented in a 130-nm CMOS process. In the receiver NMOS emulator and transmitter NMOS emulator, the I/O pad is connected to the gate terminal and drain terminal of the NMOS transistor, respectively. With the typical connection between the I/O pad and the MOS transistor, the ESD robustness of the ESD-protected receiver and transmitter
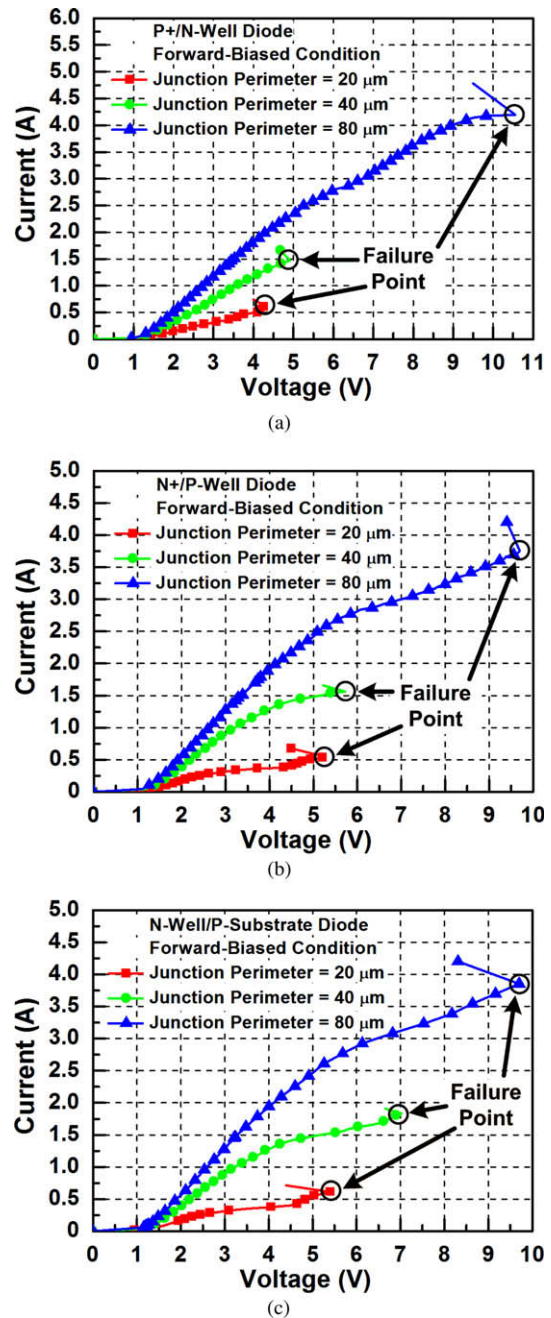

Fig. 4. TLP-measured I–V curves of (a) P+/N-well diodes, (b) N+/P-well diodes, and (c) N-well/P-substrate diodes with different dimensions.

interface circuits can be estimated by the ESD robustness of the receiver NMOS emulator and transmitter NMOS emulator, respectively.

3.1. Power-rail ESD clamp circuit

The power-rail ESD clamp circuit is an essential block in the whole-chip ESD protection design [17]. With the ESD current path between V_{DD} and V_{SS} provided by the power-rail ESD clamp circuit, the ESD protection diodes at the I/O pad can be ensured to be operated in the forward-biased condition under all ESD-test pin combinations to achieve high ESD robustness.

In this work, the ESD clamp device in the power-rail ESD clamp circuit is realized by the P-type substrate-triggered SCR (P-STSCR),
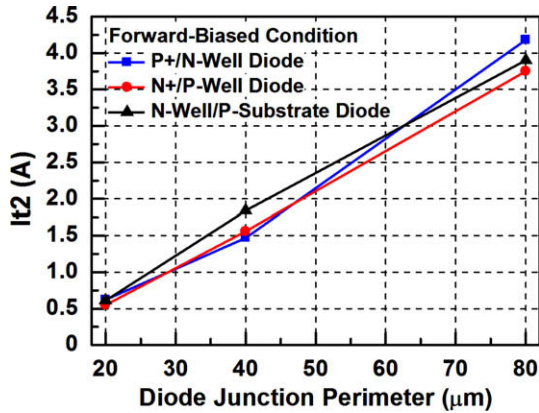
Fig. 5. TLP-measured It2 values of ESD protection diodes under different dimensions in a 130-nm CMOS process.
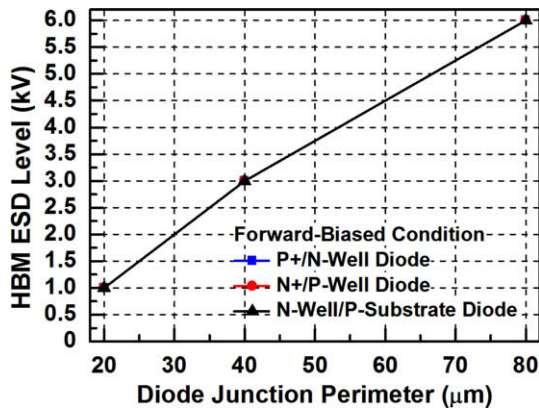

Fig. 6. HBM ESD levels of ESD protection diodes under different dimensions in a 130-nm CMOS process. The ESD protection diodes have identical HBM ESD robustness under the same size.

because SCR has been demonstrated to have high ESD robustness under a small layout area [18,19]. The cross-sectional view and equivalent circuit of the P-STSCR are shown in Fig. 7. The SCR path exists among the P+ diffusion (anode), N-well, P-well, and N+ diffusion (cathode). The equivalent circuit of the P-STSCR consists of a parasitic vertical PNP BJT and a parasitic lateral NPN BJT. The PNP BJT Q_{PNP} is formed by the P+ diffusion (anode), N-well, and P-well. The NPN BJT Q_{NPN} is formed by the N-well, P-well, and N+ diffusion (cathode). In the power-rail ESD clamp circuit, the anode and N-well of the P-STSCR are connected to V_{DD}, while the cathode
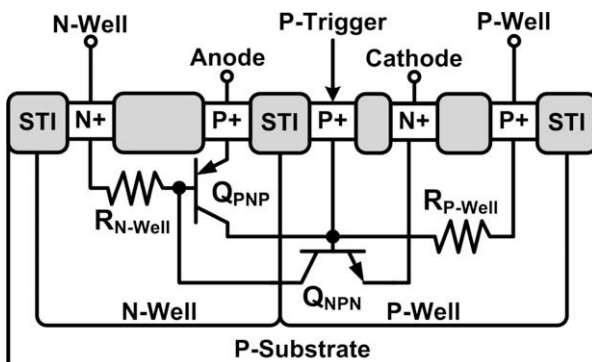
and P-well of the P-STSCR are connected to V_{SS}. To quickly turn on the P-STSCR under ESD stresses, the P+ trigger diffusion (in the P-well region) was added between the anode and cathode. An extra ESD detection circuit was designed to inject trigger current to the P-trigger node under ESD stresses. After the voltage drop across the P-well resistance (R_{P-well}) is larger than the cut-in voltage of the base-emitter junction of Q_{NPN}, Q_{NPN} is turned on to conduct it collector current, which leads to voltage drop across the N-well resistance (R_{N-well}). When the voltage drop across R_{N-well} is larger than the cut-in voltage of the base-emitter junction of Q_{PNP}, Q_{PNP} is also turned on to conduct ESD current, which causes more collector current of Q_{NPN} due to the current gain of BJT. The regenerative positive-feedback mechanism [20] results in the great current handing capability of SCR, and makes SCR very robust against ESD stresses.

The power-rail ESD clamp circuit is shown in Fig. 8, which includes the P-STSCR and the ESD detection circuit. The ESD detection circuit consists of an RC timer and an inverter. The RC timer is designed to distinguish the ESD transients from the normal circuit operating conditions. Under normal circuit operating conditions, the node between R and C is charged to high potential (V_{DD}). Since NMOS M_N is turned on and PMOS M_P is turned off, the P-trigger node is tied to V_{SS} and no trigger current is injected. Consequently, the P-STSCR is kept off under normal circuit operating conditions. Under ESD stresses, the ESD energy is coupled to V_{DD} quickly. With the RC delay provided by the resistor R and the capacitor C, the gate voltages of M_P and M_N are initially biased at low potential (∼0 V). Therefore, M_P is turned on to inject trigger current into the P-trigger node. As a result, the P-STSCR is turned on to provide ESD current path between V_{DD} and V_{SS} under ESD stresses.

Since the power-rail ESD clamp circuit is placed between V_{DD} and V_{SS}, it does not contribute any parasitic capacitance to the input nor output pads of the high-speed I/O interface circuits. Thus, the size of the P-STSCR in the power-rail ESD clamp circuit is not limited by the specification of parasitic capacitance at the high-speed I/O pad.

3.2. ESD protection design with receiver NMOS emulator

Fig. 9 shows the schematic of the receiver NMOS emulator. In the receiver NMOS emulator, the gate terminal of the NMOS M_{RX} was connected to the I/O pad, whereas the drain, source, and bulk terminals are grounded. The ESD protection diode (D_P) between the I/O pad and V_{DD} was realized by the P+/N-well diode, whereas the ESD protection diode (D_N) between the I/O pad and V_{SS} was realized by the N-well/P-substrate diode. According to the measured results in Section 2, the stand-alone ESD protection diodes with more than 40-μm junction perimeter can sustain over 2-kV
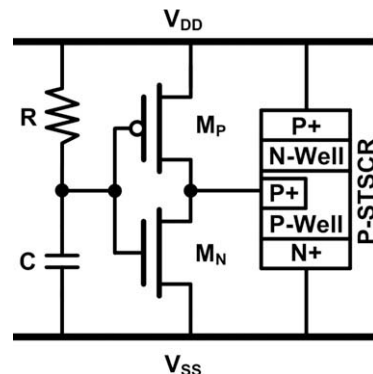

Fig. 7. Cross-sectional view and equivalent circuit of P-STSCR.

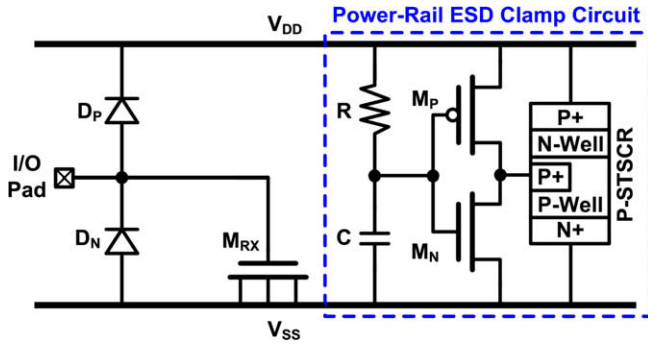**Fig. 8.** Power-rail ESD clamp circuit realized with P-STSCR.

Fig. 9. Receiver NMOS emulator used as a test circuit to verify the effectiveness of the proposed ESD protection scheme in a receiver (double diodes and active power-rail ESD clamp circuit).
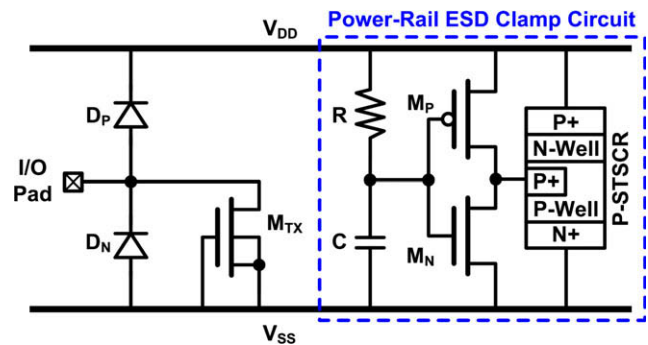

Fig. 10. Transmitter NMOS emulator used as a test circuit to verify the effectiveness of the proposed ESD protection scheme in a transmitter (double diodes and active power-rail ESD clamp circuit).

HBM ESD level, which is the specification for general commercial IC products. To increase the margin of ESD robustness, namely, to reduce the voltage drop across the internal circuits under ESD stresses and to lower the turn-on resistance of the ESD protection devices, the ESD protection diodes were realized with 45- and 55-µm junction perimeters to compare their ESD levels. The P-STSCR in the power-rail ESD clamp circuit was implemented with 59.6-µm width. When the I/O pad of receiver NMOS emulator is stressed by ESD, the voltage across the I/O pad and V_{SS} is across the gate oxide, which is the worst case for the gate oxide of NMOS under ESD stresses. Since the gate terminal of the MOS transistor is often

connected to the input pad of the receiver, the ESD robustness of receiver NMOS emulator can be used to estimate the ESD robustness of the practical receiver interface circuit with this ESD protection scheme.

3.3. ESD protection design with transmitter NMOS emulator

Fig. 10 shows the schematic of the transmitter NMOS emulator. In the transmitter NMOS emulator, the drain terminal of the NMOS M_{TX} was connected to the I/O pad, whereas the gate, source, and bulk terminals are grounded. Similarly, the ESD protection diode (D_P) between the I/O pad and V_{DD} was realized by the P+/N-well diode, and the ESD protection diode (D_N) between the I/O pad and V_{SS} was realized by N-well/P-substrate diode. D_P and D_N with 45- and 55-µm junction perimeters were used in the ESD protection scheme for the transmitter NMOS emulator. The P-STSCR in the power-rail ESD clamp circuit was implemented with 59.6-µm width. When the I/O pad is stressed by ESD, the voltage between the I/O pad and V_{SS} is across the drain terminal and the other three terminals of the NMOS transistor. Since the drain terminal of the MOS transistor is often connected to the output pad of the transmitter, the ESD robustness of the transmitter NMOS emulator can be used to estimate the ESD robustness of the practical transmitter interface circuit protected by this ESD protection scheme.

3.4. ESD levels of receiver NMOS emulator and transmitter NMOS emulator

The calculated DC junction capacitances of D_P with 45- and 55-µm junction perimeters are 88.1 and 118 fF, whereas the calculated DC junction capacitances of D_N with 45- and 55-µm junction perimeters are 59.1 and 73.1 fF. The HBM and machine-model (MM) [21] ESD levels of the receiver NMOS emulator and transmitter NMOS emulator with different diode junction perimeters are listed in Tables 4 and 5, respectively. The step voltages in the HBM and MM ESD tests are 500 V and 50 V, respectively. With the active power-rail ESD clamp circuit, the ESD protection diodes are assured to be operated in the forward-biased condition rather than the reverse-biased condition under all ESD-test pin combinations. Therefore, high enough ESD robustness can be achieved in the receiver NMOS emulator and transmitter NMOS emulator. The receiver NMOS emulator with 45-µm diode junction perimeter has 2.5-kV HBM and 100-V MM ESD robustness. By using the ESD protection diodes with 55-µm junction perimeter in the receiver NMOS emulator, the HBM and MM ESD levels are improved to 3 kV and 150 V, respectively. In the transmitter NMOS emulator

Table 4
ESD Robustness of receiver NMOS emulator with different dimensions of ESD protection diodes.

Junction area (µm²)		Junction perimeter (µm)		PS-mode		NS-mode		PD-mode		ND-mode	
D_P	D_N	D_P	D_N	HBM (kV)	MM (V)	HBM (kV)	MM (V)	HBM (kV)	MM (V)	HBM (kV)	MM (V)
Receiver NMOS emulator											
87.5	87.5	45	45	2.5	100	3	200	3	150	3.5	200
112.5	112.5	55	55	3	150	4	200	4	200	4	250

Table 5
ESD robustness of transmitter NMOS emulator with different dimensions of ESD protection diodes.

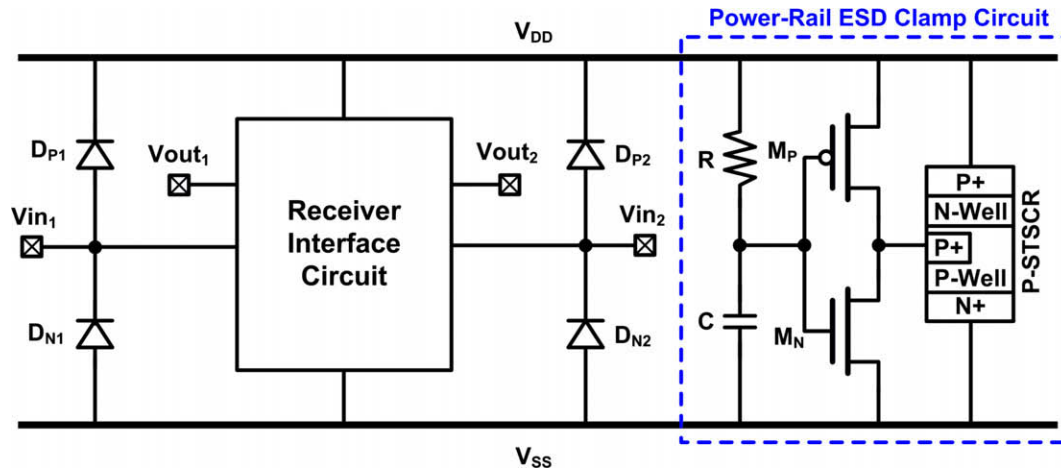| Junction area (µm²)		Junction perimeter (µm)		PS-mode		NS-mode		PD-mode		ND-mode	
D_P	D_N	D_P	D_N	HBM (kV)	MM (V)	HBM (kV)	MM (V)	HBM (kV)	MM (V)	HBM (kV)	MM (V)
Transmitter NMOS emulator											
87.5	87.5	45	45	3	300	6	450	3.5	400	5	300
112.5	112.5	55	55	3.5	300	6.5	450	4.5	450	5.5	350

Fig. 11. The first whole-chip ESD protection scheme for 2.5-Gb/s high-speed receiver interface circuit (Receiver_1–Receiver_2).

Table 6
Dimensions of ESD Protection Devices in High-speed receiver interface circuits without and with double-diode ESD protection scheme.

	ESD protection device between I/O pad and V_{DD}		ESD protection device between I/O pad and V_{SS}		Total C_{ESD}
	Device	C_{ESO} (fF)	Device	C_{ESO} (fF)	
Receiver_0	None	0	None	0	0
Receiver_1	D_P (PJ = 35 μm)	63.2	D_N (PJ = 35 μm)	45.1	108.3
Receiver_2	D_P (PJ = 55 μm)	117.9	D_N (PJ = 55 μm)	73.1	191

with 45-μm diode junction perimeter, the HBM and MM ESD levels are 3 kV and 300 V, respectively. With 55-μm diode junction perimeter, the HBM ESD level is improved to 3.5 kV with the MM ESD level unchanged. The transmitter NMOS emulator has higher negative-to-V_{SS} (NS-mode) and negative-to-V_{DD} (ND-mode) ESD levels as compared with those of the receiver NMOS emulator, because the parasitic P-well/N+ junction diode between the bulk and drain of the transmitter NMOS emulator discharges some ESD current. Moreover, it is found that the PS-mode ESD test is the most critical ESD-test pin combination for both receiver NMOS emulator and transmitter NMOS emulator. Under the PS-mode ESD stress, the ESD current path consists of the diode D_P and the power-rail ESD clamp circuit. In this situation, the voltage drop along the whole ESD current path is across the gate oxide of the receiver

NMOS emulator and transmitter NMOS emulator. Under the ND-mode ESD stress, the ESD current path consists of the power-rail ESD clamp circuit and the diode D_N. However, the voltage across the gate oxide of the receiver NMOS emulator and transmitter NMOS emulator is only the voltage across D_N. With the highest voltage across the gate oxide, the PS-mode ESD test becomes the most critical ESD-test pin combination. In the following section, a modified design to improve the PS-mode ESD level is proposed.

4. ESD-protected high-speed I/O interface circuit

After investigating the ESD robustness of receiver NMOS emulator and transmitter NMOS emulator, this whole-chip ESD protection scheme was applied to a 2.5-Gb/s high-speed receiver
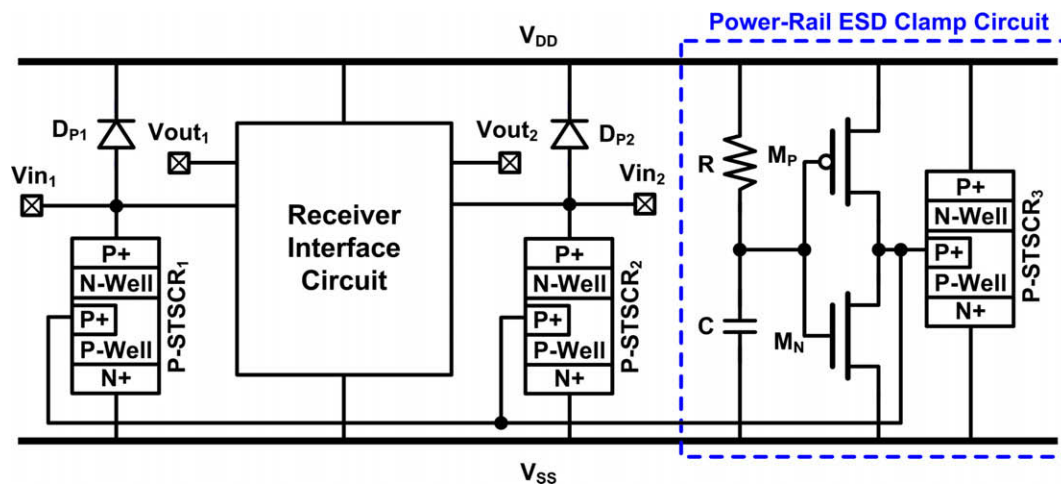

Fig. 12. The second whole-chip ESD protection scheme for 2.5-Gb/s high-speed receiver interface circuit (Receiver_3–Receiver_8).

interface circuit in a 130-nm CMOS process. Fig. 11 shows the ESD protection scheme for a 2.5-Gb/s high-speed receiver interface circuit. The receiver interface circuit has the differential input stage realized by PMOS transistors. In the power-rail ESD clamp circuit, the ESD clamp device of P-STSCR was realized with 59.6-μm width. Two diode junction perimeters of 35 and 55 μm were implemented in the ESD protection scheme shown in Fig. 11. According to Table 4, the ESD protection diodes with 45-μm junction perimeter can sustain 2.5-kV HBM ESD robustness. In this high-speed receiver interface circuit, the ESD protection diodes with 35-μm junction perimeter are implemented to investigate its ESD robustness because lower parasitic capacitance from the ESD protection devices is preferred. Table 6 lists the dimensions of the ESD protection devices and the corresponding DC junction capacitance (by calculation) in the high-speed receiver interface circuit without and with the double-diode ESD protection scheme. In Receiver_1 (Receiver_2) with the diode junction perimeter of 35 μm (55 μm), the calculated capacitance from the ESD protection devices at the I/O pad is 108.3 fF (191 fF).

It was mentioned that the PS-mode ESD test is the most critical ESD-test pin combination for the ESD protection scheme shown in Fig. 11. A modified design is proposed to improve the PS-mode ESD robustness, as shown in Fig. 12. In the proposed ESD protection scheme, the ESD protection diode between the I/O pad and V_{SS} is replaced with the P-STSCR. The device dimensions in the power-rail ESD clamp circuit in Fig. 12 are identical to those in Fig. 11. Since the P-STSCR is already used in the power-rail ESD clamp circuit, the ESD detection circuit in the power-rail ESD clamp circuit can also be used to inject trigger current into the P-STSCRs (P-STSCR$_1$ and P-STSCR$_2$) at the I/O pads under ESD stresses. Under PS-mode ESD stresses, the ESD voltage is coupled from the I/O pad to V_{DD} through D_P, and the P-STSCR devices can be turned on by the ESD detection circuit. When the P-STSCR at the I/O pad is turned on, it provides an ESD current path directly from the I/O pad to V_{SS}. As a result, ESD current will flow through only the P-STSCR at the I/O pad instead of through D_P and the power-rail ESD clamp circuit. With fewer ESD protection devices and lower voltage drop along the ESD current path under PS-mode ESD tests, higher ESD robustness can be achieved. In the proposed design, the P-STSCR at the I/O pad was implemented with 20-, 30-, and 50-μm widths to investigate the ESD levels with different parasitic capacitances at the I/O pad. The dimensions of the ESD protection devices in the proposed ESD protection scheme and the corresponding DC junction capacitances (by calculation) are listed in Table 7. In Receiver_3 (Receiver_4) with 20-μm wide P-STSCR between the I/O pad and V_{SS}, the calculated parasitic capacitance at each I/O pad is 127.9 fF (182.6 fF) when D_P is realized with 35-μm (55-μm) junction perimeter. When the width of the P-STSCR between the I/O pad and V_{SS} is increased to 30 μm, the calculated parasitic capacitances at each I/O pad is 153.3 fF (208 fF) in Receiver_5 (Receiver_6) with 35-μm (55-μm) D_P perimeter. With 50-μm wide P-STSCR between the I/O pad and V_{SS}, Receiver_7 (Receiver_8) with 35-μm (55-μm) D_P perimeter has the parasitic capacitance of 204.1 fF (258.8 fF) at each I/O pad. To verify the effectiveness of the
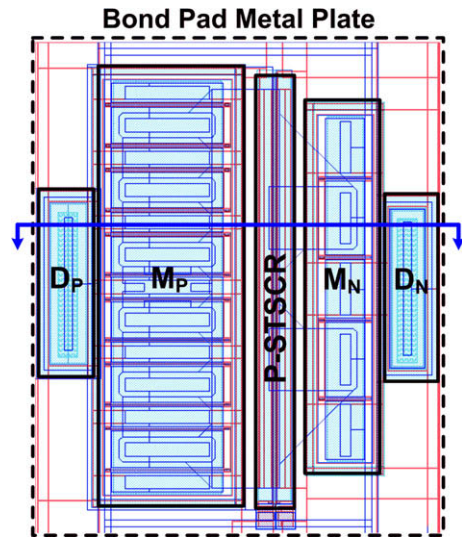

Fig. 13. Layout top view of the ESD protection devices under the bond pad.

ESD protection schemes, the high-speed receiver interface circuit (Receiver_0) without ESD protection was also fabricated in the same process.

To save the chip area of the ESD-protected high-speed receiver interface circuit, the ESD protection devices at the input node, M_P, M_N, and the P-STSCR in the power-rail ESD clamp circuit were placed under the I/O pad [22]. Fig. 13 shows the layout top view of the ESD protection devices under the bond pad in Receiver_1 and Receiver_2. The cross-sectional view of the ESD protection devices under the bond pad is shown in Fig. 14. By putting D_P and M_P together, only an N-well is needed. D_N and M_N are put together in the layout. The P-STSCR in the power-rail ESD clamp circuit is realized between the N-well and P-well regions. In Receiver_3 to Receiver_8, the P-STSCR between the I/O pad and V_{SS} is also placed under the I/O pad. Besides saving the chip area, placing the ESD protection devices under the I/O pad reduces some parasitic capacitance at the I/O pad because the bond-pad capacitance and the parasitic capacitance of the ESD protection devices are series connected between the I/O pad and the substrate.

The nine high-speed receiver interface circuits were fabricated in a 130-nm CMOS process. The HBM ESD levels of the high-speed receiver interface circuits without and with the double-diode ESD protection scheme are listed in Table 8. Without ESD protection, Reveiver_0 is very vulnerable to ESD, which fails at 0.5-kV HBM ESD test. With the double-diode ESD protection scheme, Receiver_1 and Receiver_2 have 2- and 3-kV HBM ESD levels, respectively. Table 9 lists the HBM ESD levels of the high-speed receiver interface circuits with the proposed ESD protection scheme. By using the P-STSCR between the I/O pad and V_{SS}, the PS-mode ESD robustness is improved. With 20-, 30-, and 50-μm wide P-STSCR between the I/O pad and V_{SS}, the PS-mode HBM

Table 7
Dimensions of ESD protection devices in High-speed receiver interface circuits with proposed ESD protection scheme.

,	ESD protection device between I/O pad and V_{DD}		ESD protection device between I/O pad and V_{SS}		Total C_{ESD} (fF)
	Device	C_{ESD} (fF)	Device	C_{ESD} (fF)	
Receiver_3	D_P (PJ = 35 μm)	63.2	P-STSCR(W = 20 μm)	64.7	127.9
Receiver_4	D_P (PJ = 55 μm)	117.9	P-STSCR(W = 20 μm)	64.7	182.6
Receiver_5	D_P (PJ = 35 μm)	63.2	P-STSCR(W = 30 μm)	90.1	153.3
Receiver_6	D_P (PJ = 55 μm)	117.9	P-STSCR(W = 30 μm)	90.1	208
Receiver_7	D_P (PJ = 35 μm)	63.2	P-STSCR(W = 50 μm)	140.9	204.1
Receiver_8	D_P (PJ = 55 μm)	117.9	P-STSCR(W = 50 μm)	140.9	258.8

Fig. 14. Cross-sectional view of the ESD protection devices under the bond pad.

Table 8
HBM ESD robustness of the high-speed receiver interface circuits without and with double-diode ESD protection scheme.

	PS-mode (kV)	NS-mode (kV)	PD-mode (kV)	ND-mode (kV)
Receive r_0	<0.5	<0.5	<0.5	<0.5
Receive r_1	2.5	2	2.5	2.5
Receive r_2	3	3	3.5	3

Table 9
HBM ESD robustness of the High-speed receiver interface circuits with proposed ESD protection scheme.

	PS-mode (kV)	NS-mode (kV)	PD-mode (kV)	ND-mode (kV)
Receiver_3	2.5	2.5	2.5	1.5
Receive r_4	4	2	4.5	2
Receive r_5	4	2.5	2.5	2.5
Receive r_6	5	3.5	4.5	2.5
Receive r_7	6	3.5	2.5	3
Receive r_8	6.5	3.5	4.5	3.5

ESD level is improved to 4, 5, and 6.5 kV, respectively. Since the ESD protection device between the I/O pad and V_{DD} is not changed in the proposed ESD protection scheme, the positive-to-V_{DD} (PD-mode) ESD level does not have significant difference under the same D_P size. In the interface circuit with the PMOS input stage, the ND-mode may become another critical ESD-test pin combination. The concept of using SCR to improve the PS-mode ESD robustness can be used to improve the ND-mode ESD robustness. The ESD protection diode between V_{DD} and the input pad can be replaced by the SCR. In such an ESD protection scheme, the ND-mode ESD current path consists of only the SCR between V_{DD} and the I/O pad. Thus, the ND-mode ESD robustness is expected to be improved because the voltage drop along the ND-mode ESD current path is reduced.

The double-diode ESD protection scheme has been applied to an IC product with a 2.5-Gb/s high-speed front-end interface fabricated in a 130-nm CMOS process. In this high-speed front-end chip, two P+/N-well diodes with 24.36-µm width and 2.74-µm length were used between the I/O pad and V_{DD}, whereas two N+/P-well diodes with 26.46-µm width and 4.84-µm length were used between the I/O pad and V_{SS}. The total calculated parasitic capacitance of the ESD protection diodes is 336 fF. This 2.5-Gb/s high-speed front-end interface passes 2-kV HBM and 200-V MM ESD tests, respectively. The measured eye diagram of this 2.5-Gb/s high-speed front-end interface circuit is shown in Fig. 15. After the ESD protection devices are applied at the I/O pad, the measured eye diagram can be still satisfactory if the parasitic capacitance from the ESD protection devices is within the design budget.

Fig. 15. Measured eye diagram of the 2.5-Gb/s high-speed I/O interface circuit fabricated in a 130-nm CMOS process.

5. Conclusion

In this work, the ESD protection design for high-speed I/O interface circuits in a 130-nm CMOS process is presented in detail. The parasitic capacitances and the ESD levels of the stand-alone ESD protection diodes were investigated in the beginning. To estimate the ESD robustness of general receiver and transmitter interface circuits with ESD protection, the receiver NMOS emulator and transmitter NMOS emulator with different ESD protection device dimensions were fabricated and their ESD levels were measured. Then, the double-diode ESD protection scheme was applied to a high-speed receiver interface circuit. To improve the ESD robustness under PS-mode ESD test, which is the most critical ESD-test pin combination for the double-diode ESD protection scheme, the ESD protection diode between the I/O pad and V_{SS} was replaced by the P-STSCR in the proposed design to reduce the clamping voltage along the PS-mode ESD current path can be reduced, so the PS-mode ESD level can be improved. Besides, the parasitic P-well/N-well diode in the SCR can provide the NS-mode ESD current path. Thus, SCR is the most promising ESD protection device in ESD protection design with low-capacitance consideration. ESD test results have shown that the PS-mode ESD level is improved by using the proposed ESD protection scheme. With the ESD protection design methodology proposed in this work, the two most important requirements of ESD protection design for high-speed I/O interface circuits, which are high ESD robustness and low parasitic capacitance, can be met simultaneously.

Acknowledgments

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