Performance Enhancement in Double-Gated Poly-Si Nanowire Transistors With Reduced Nanowire Channel Thickness

Horng-Chih Lin, *Senior Member, IEEE*, Wei-Chen Chen, Chuan-Ding Lin, and Tiao-Yuan Huang, *Fellow, IEEE*

***Abstract*—A new method is proposed and successfully demonstrated for the fabrication of polycrystalline silicon (poly-Si) nanowire (NW) transistors with rectangular-shaped NW channels and two independent gates. The two independently controllable gates allow higher flexibility in device operation and provide a unique insight into the conduction mechanism of the NW device. Our results indicate that dramatic performance enhancement is feasible when the thickness of the NW channel is sufficiently thin, and the two conduction channels in the NW structure are operating simultaneously.**

***Index Terms*—Double gate, nanowire (NW), polycrystalline silicon (poly-Si).**

RECENTLY, poly-Si nanowire (NW) field-effect transistors have received considerable attention owing to their potential applications to advanced logic and memory devices [1]–[5]. Although it is well known that defects contained in the granular poly-Si films would aggravate the device characteristics, the adoption of NW structure could help alleviate the effects. For example, subthreshold swing better than 100 mV/dec, comparable to that of modern CMOS devices, has been demonstrated for poly-Si NW devices [1], [5]. The improvement is ascribed to the small amount of defects contained in the tiny channel volume of the NW structure. An alternative remedy is to adopt multiple-gated configuration, thereby increases the gate controllability over the device channel [6], [7]. Recently, we have proposed a novel poly-Si NW transistor with the NW channels formed by the sidewall spacer etching technique, and the channels were surrounded by both an inverse-T-shaped gate and a top gate [5]. The independently controllable double-gate scheme effectively enhanced the flexibility in device operation. However, in our previous device structure, the cross section of the NW channels was irregular in shape, causing nonuniform distribution of channel carriers and complicating the device analysis. To gain insight into the conduction mechanism of the NW devices, we propose and characterize a new type of poly-Si NW device which features rectangular-shaped NW channels and two independently controllable gates.

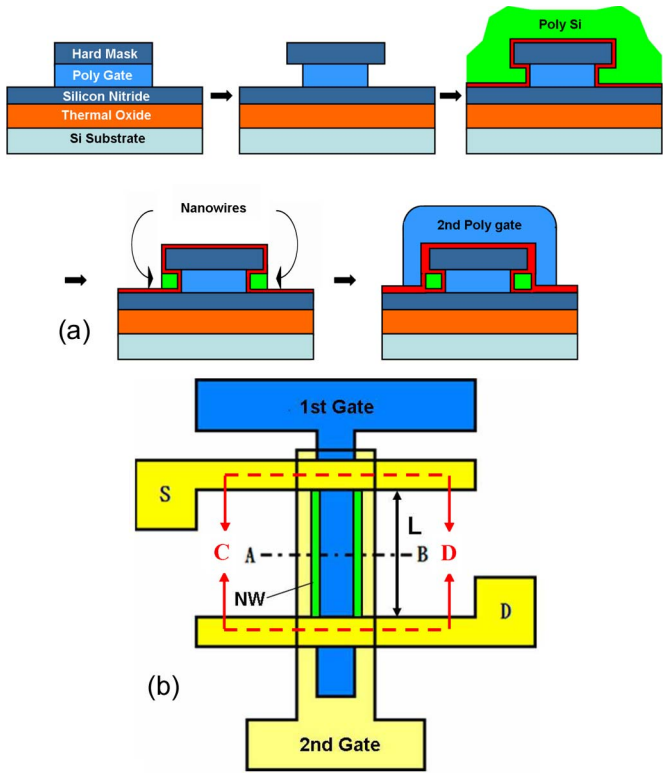

Fig. 1. (a) Fabrication flow and (b) top view of the proposed poly-Si NW device.

The fabrication flow and top view of the new structure are shown in Fig. 1(a) and (b), respectively. The cross-sectional views at different steps shown in Fig. 1(a) are along the A–B dashed line shown in Fig. 1(b). From the completed structure, it can be seen that the poly-Si NW channel is rectangular in shape. Below, we briefly describe the key process flow. First, silicon wafers which were capped with 200-nm-thick thermal oxide and 50-nm-thick SiN layer were used as the starting substrates. Next, a first gate structure consisting of 100-nm-thick *in situ* doped n^+ poly-Si capped with 50-nm-thick SiN was formed. Then, cavities underneath the nitride hardmask were formed by encroaching both sides of the gate structure. This was

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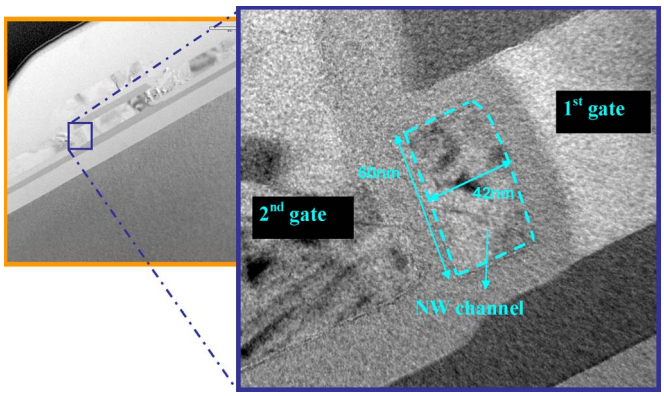

Fig. 2. TEM image of a fabricated device.

performed in a plasma reactor with SF_6/Cl_2 chemistry which allows the selective etching of n^+ poly-Si with high selectivity to the nitride capping layers. Afterward, a 20-nm-thick TEOS oxide layer was formed to serve as the gate dielectric of the first gate, followed by the deposition of a 100-nm-thick undoped amorphous-Si layer serving as the channel material, both by low-pressure chemical vapor deposition (LPCVD). Owing to the excellent conformability of the CVD process, the cavities are completely refilled with the deposited materials. An annealing step was then performed at 600 °C in N_2 ambient for 24 h to transform the amorphous-Si into poly-Si. Subsequently, source/drain (S/D) implantation was performed. After S/D photoresist patterns were formed, an anisotropic plasma etching step was employed to form the S/D regions. In this step, the portions of Si layer residing in the cavities were retained and formed the NW channels. It should be noted that the horizontal width of the NW is defined as the channel thickness in this letter. Another LPCVD TEOS oxide layer with thickness of 20 nm was deposited to serve as the second gate oxide. Moreover, a 100-nm-thick *in situ* doped n^+ poly-Si was deposited and patterned to serve as the second gate electrode. All devices were then covered with a 200-nm-thick oxide passivation layer. The fabrication steps were completed after the formation of test pads using standard metallization steps. Finally, all devices received a NH_3 plasma treatment at 300 °C for 3 h before characterization in order to improve the device performance as well as to reduce the fluctuation in device characteristics [8].

The cross-sectional transmission electron microscopic (TEM) image of a fabricated device showing the NW channel and the gates is shown in Fig. 2. It can be seen that the cross section of the NW channels is rectangular in shape, and the channel thickness is around 42 nm. Fig. 3 shows and compares the transfer characteristics of devices with NW channel thickness of 53 and 42 nm, operating in both single-gated (SG) and double-gated (DG) modes. The channel length of the devices is 1 μm. Table I summarizes major measured characteristics shown in Fig. 3. In DG mode of operation, both gate electrodes are applied with the sweeping bias. In SG modes, varying bias is applied to one of the two gate electrodes with the other one grounded. In the figures, SG-1 and SG-2 modes denote the schemes with sweeping voltage applied to the first gate and the second gate, respectively. From the figures, we can see that the operation under SG-1 mode exhibits lower on-current than

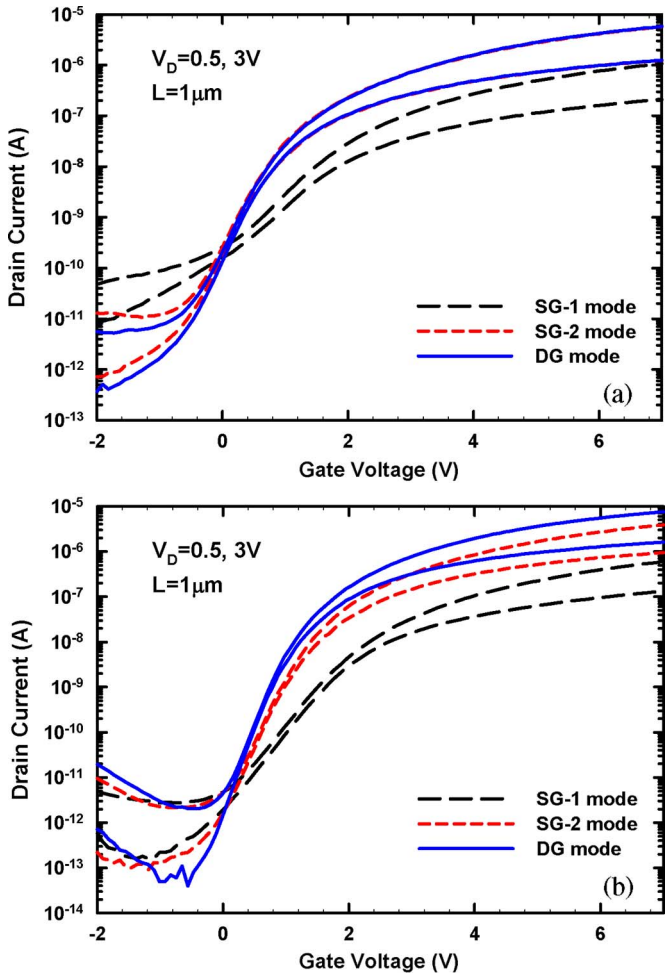

Fig. 3. Transfer characteristics of fabricated devices with NW channel thickness of (a) 53 nm and (b) 42 nm.

TABLE I
SUMMARY OF THE DEVICE CHARACTERISTICS SHOWN IN FIG. 3

	Swing (mV/dec)			I_{on} (μA)			I_{min} (pA)		
	SG-1	SG-2	DG	SG-1	SG-2	DG	SG-1	SG-2	DG
42nm NW	560	317	254	0.13	0.94	1.61	0.16	0.09	0.04
53nm NW	851	393	372	0.21	1.24	1.25	7.77	0.72	0.37

* swing and I_{min} is extracted @ V_D=0.5V
I_{on} is extracted @ V_G=7V, V_D=0.5V

that under the SG-2 mode. This is attributed to the larger S/D series resistance under SG-1 mode of operation, as the conduction occurs mainly at the inner channel interface of the NWs. To make it clear, in Fig. 4, we plot the cross-sectional view of the device along the C–D lines shown in Fig. 1(b). During SG-1 mode of operation, the conduction electrons have to transport across the offset (i.e., ungated) regions between the S/D and the inner conduction channel, therefore the S/D series resistance is larger. For the DG mode of operation, it is thus expected that the current conduction is mainly through the outer channel gated by the second gate. This is particularly true for the device characterized in Fig. 3(a) where we can see the current–voltage (I–V) curve of DG mode coincides with that of the SG-2 mode as the device is switched on.

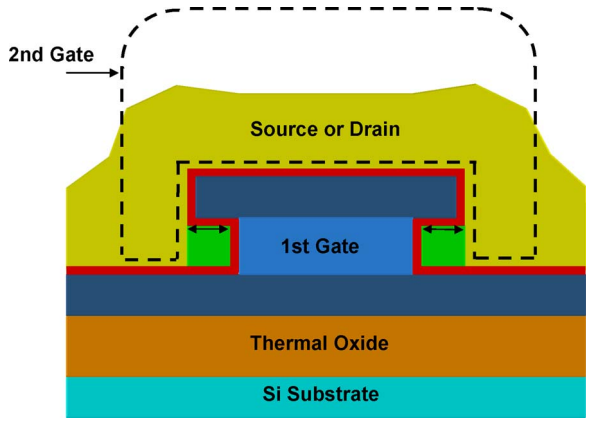

Fig. 4. Cross-sectional view of the device along the C–D lines shown in Fig. 1(b). Projection of the second gate (shaped by the dashed lines) is also shown. From the figure, it can be seen that ungated regions (indicated by the double-head arrows) exist between the inner conduction channel (gated by the first gate) and S/D.

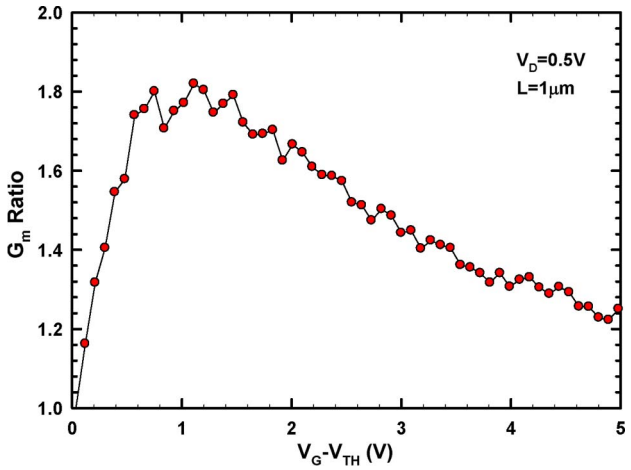

Fig. 5. Ratio of transconductance (G_m) under DG mode of operation to the sum of G_m of the two SG modes for the device characterized in Fig. 3(b).

When the thickness of the NW channel is reduced to 42 nm, as shown in Fig. 3(b), we can see that the performance *is improved* in terms of steeper subthreshold slope and higher on-current. Specifically, the subthreshold slope under DG mode of operation is 372 mV/dec in Fig. 3(a) and is greatly improved to 254 mV/dec in Fig. 3(b). In Fig. 3(b), we can also see that the on-current is dramatically increased with the DG mode of operation. This is postulated to be due to the volume inversion effect which occurs when the two conduction channels are sufficiently close to each other [9]. Such phenomenon is known to increase the conduction carrier concentration and mobility, and therefore the on-current. In Fig. 5, we plot the ratio of transconductance (G_m) under DG mode of operation to the sum of G_m of the two SG modes for the device characterized in Fig. 3(b). The ratio is much larger than unity, a major signature for the occurrence of volume inversion [10]. When this happens, the S/D series resistance is also reduced due to the increase in conduction carrier concentration, further improving the device drivability. Additional improvement is expected by further shrinking of the NW thickness.

In summary, a novel poly-Si NW device featuring rectangular-shaped NW channels and two independently controllable gates is proposed and characterized. The fabrication process is simple without resorting to advanced and costly lithography tools. Enhanced performance has also been demonstrated with reduced NW channel thickness, including higher on-current, larger on/off current ratio and steeper subthreshold swing. Volume inversion effect which occurs when the NW is sufficiently thin is postulated as one of the major causes for the performance enhancement.

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