Impact of Uniaxial Strain on Low-Frequency Noise in Nanoscale PMOSFETs

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***Abstract*—This letter investigates the low-frequency noise characteristics and reports a new mechanism for uniaxial strained PMOSFETs. Through a comparison of the input-referred noise and the trap density of the gate dielectric/semiconductor interface between co-processed strained and unstrained devices, it is found that the tunneling attenuation length for channel carriers penetrating into the gate dielectric is reduced by uniaxial strain. The reduced tunneling attenuation length may result in smaller input-referred noise, which represents an intrinsic advantage of low-frequency noise performance stemming from process-induced strain.**

***Index Terms*—Interface state, low-frequency noise, process-induced strain, trap density, tunneling attenuation length, uniaxial strained PMOSFET.**

I. Introduction

Low-frequency noise is becoming a concern for continuously down-scaled CMOS devices because increased low-frequency noise in these nanoscale transistors may limit the functionality of analog, mixed-signal, and RF circuits. As strained silicon is widely used in state-of-the-art CMOS technologies to enable the mobility scaling [1], [2], the low-frequency noise performance for strained devices is particularly important. Several studies regarding this topic have been carried out in the past [4], [5]. For example, Giusi *et al.* [3] have reported that the low-frequency noise of strained PMOSFETs with HfO_2 gate dielectric could be degraded due to worse gate dielectric quality when processing the SiGe source/drain. The work of Simoen *et al.* [4] and Ueno *et al.* [5] revealed that the low-frequency noise performance of strained devices with SiON gate dielectric may be preserved. While the low-frequency noise performance is determined by the device fabrication processes [3]–[6], whether there exists any other intrinsic stress effect on low-frequency noise is still not clear and merits further investigation. In this letter, through an in-depth comparison between co-processed strained and unstrained devices regarding the low-frequency noise characteristics, we report a new mechanism for uniaxial strained PMOSFETs.

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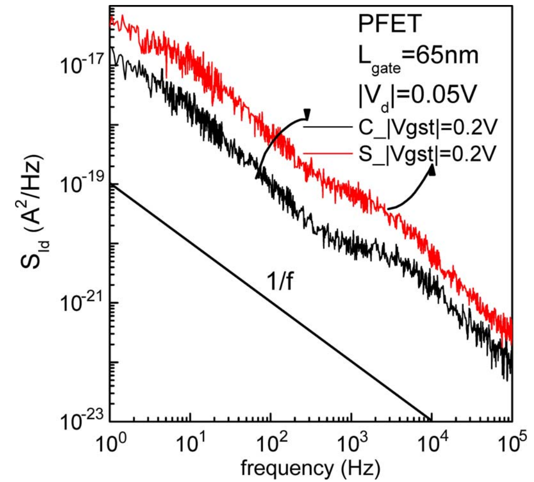

Fig. 1. Drain current noise spectral density $S_{\rm Id}$ for devices with $L_{\rm gate} =$ 65 nm at $|V_d| = 0.05$ V and $|V_{\rm gst}| = 0.2$ V showing typical $1/f^r$ noise type with r close to one.

II. Devices

Co-processed uniaxial strained and unstrained PMOSFETs are investigated in this letter [7], [8]. Strained and unstrained devices with channel direction $\langle 110 \rangle$ and poly/SiO_2 gate stack were fabricated on (100) silicon substrate. The strained device features compressive uniaxial Contact Etch Stop Layer (CESL) and SiGe source/drain. For the transistors with gate length $L_{\rm gate} = 65$ nm, the saturation drain current $(I_{\rm dsat})$ of the strained device is improved by more than 100% as compared with its control counterpart. The low-frequency noise measurements were carried out using the BTA9812 [3], [9] measurement system.

III. Results and Discussion

The drain current noise spectral densities $(S_{\rm Id})$ for strained and unstrained devices biased at gate overdrive $|V_{\rm gst}| = 0.2$ V are shown in Fig. 1. The spectra show typical $1/{\rm f}^r$ noise type with the frequency index γ close to one. Fig. 2 shows the normalized noise spectral density, $S_{\rm Id}/I_d^2$, as well as $(g_m/I_d)^2$ versus drain current I_d for strained and unstrained devices at frequency $f = 10$ Hz. It can be seen that the $S_{\rm Id}/I_d^2$ shows a fairly good proportionality with $(g_m/I_d)^2$, indicating a carrier-number-fluctuation origin [10], [11].

Fig. 3 shows the input-referred voltage spectral density $(S_{\rm Vg} = S_{\rm Id}/g_m^2)$ as a function of $V_{\rm gst}$ taken from the average of ten devices. It can be seen that the $S_{\rm Vg}$ for strained and

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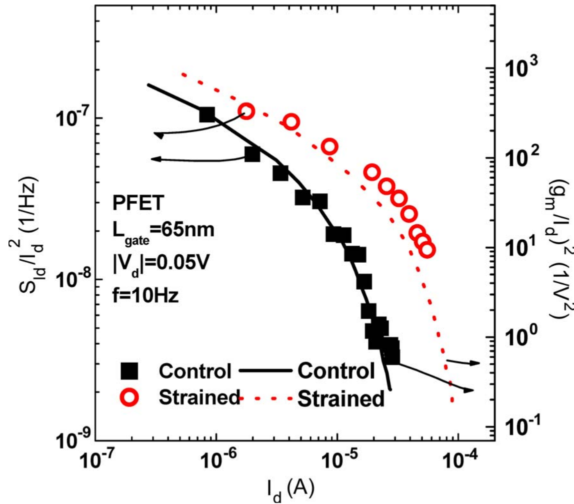

Fig. 2. Normalized current noise spectral density S_{Id}/I_d^2 and $(g_m/I_d)^2$ versus I_d for devices with $L_{\text{gate}} = 65$ nm and $|V_d| = 0.05$ V.

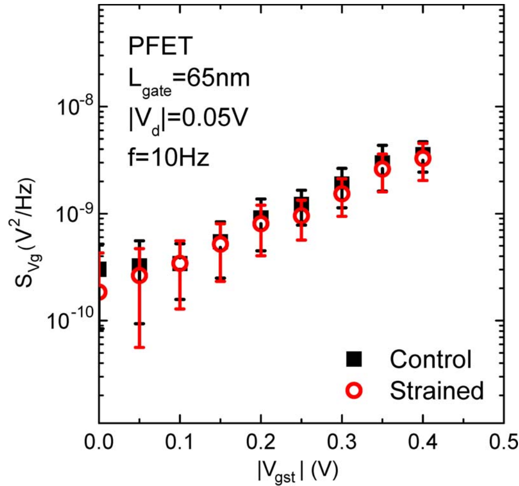

Fig. 3. Input-referred noise spectral density S_{Vg} versus $|V_{\text{gst}}|$ for devices with $L_{\text{gate}} = 65$ nm at $f = 10$ Hz and $|V_d| = 0.05$ V.

unstrained devices are nearly the same. The S_{Vg} stems from oxide traps and can be expressed as [12]

$$S_{\text{Vg}} = \frac{kTq^2}{fWL_{\text{gate}}C_{\text{OX}}^2}\lambda \times N_t \tag{1}$$

where λ, N_t, kT, W, and C_{OX} are the tunneling attenuation length for channel carriers penetrating into the gate dielectric, the occupied trap density, the thermal energy, the gate width, and the gate capacitance per unit area, respectively. The nearly identical S_{Vg} implies that the $\lambda \times N_t$ products of the strained and unstrained devices are almost the same.

To further analyze the impact of uniaxial strain, we have measured the N_t by the incremental frequency charge pumping method [13] under the following conditions: source/drain reverse voltage $V_{\text{rev}} = -0.1$ V, amplitude of gate pulse $V_a = 1.2$ V, frequencies of gate pulse are 20 and 25 MHz, duty cycle $= 50\%$, rise time of gate pulse $t_{\text{rise}} = 2$ ns, and fall time of gate pulse $t_{\text{fall}} = 2$ ns. According to the incremental frequency charge pumping method [13], the difference of

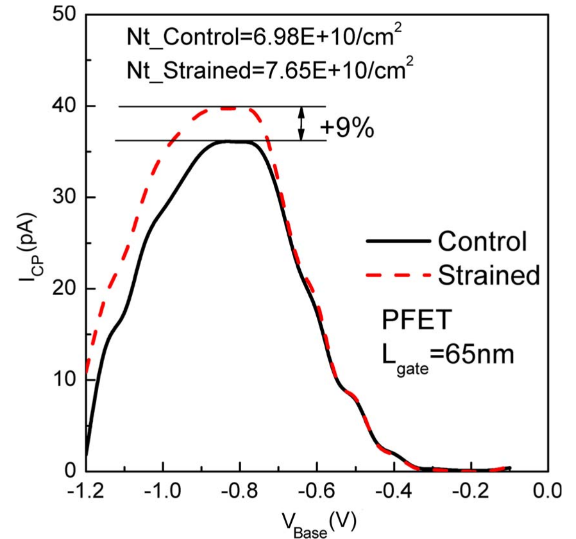

Fig. 4. Measurement results of charge pumping for strained and unstrained devices with $L_{\text{gate}} = 65$ nm. N_t is proportional to the maximum of I_{CP}.

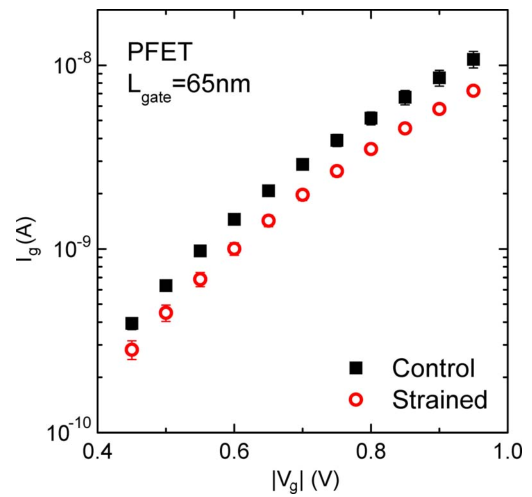

Fig. 5. I_g versus $|V_g|$ showing smaller gate tunneling current for the strained device.

charge pumping current (I_{CP}) between 20 and 25 MHz can be regarded as the I_{CP} at 5 MHz. The I_{CP} at 5 MHz versus base level of gate pulses (V_{Base}) is shown in Fig. 4. Since the N_t is proportional to the maximum of I_{CP}, it can be seen that the occupied trap density N_t of the strained device is 9% larger than its control counterpart. More importantly, the increased N_t means that the tunneling attenuation length (λ) of the strained device is reduced.

The reduced λ in the strained device can be attributed to the increased out-of-plane effective mass (m_z^*) and tunneling barrier height (φ_B). Thompson *et al.* [14] have reported that when the uniaxially compressive strain is applied, the valence bands split, and more holes populate in the top band. Moreover, the m_z^* and φ_B of the top band are larger for the strained device as compared with that of the unstrained ones. The strain-increased m_z^* and φ_B are also responsible for the smaller gate tunneling current (I_g) in the strained device, as shown in Fig. 5, which is consistent with the results in [15]–[17].

Since λ is related to m_z^* and φ_B by [12]

$$\lambda = \sqrt{\hbar^2/2m_z^*\varphi_B} \quad (2)$$

with $\hbar$ being the reduced Planck's constant, the strain-increased m_z^* and φ_B result in a smaller λ in the strained device. In other words, while the gate dielectric quality may be degraded by the strain process, the tunneling attenuation length of carriers can actually be reduced by strain. It indicates that the carrier-number-fluctuation origin of low-frequency noise can be improved intrinsically for nanoscale strained PFETs.

IV. Conclusion

We have investigated the low-frequency noise characteristics of uniaxial strained PMOSFETs. Based on the extracted N_t, it is found that the tunneling attenuation length λ is reduced in the strained device. The reduced λ can be attributed to the increased out-of-plane effective mass m_z^* and tunneling barrier height φ_B by uniaxially compressive strain. This reduced λ may result in smaller S_{Vg}, which represents an intrinsic advantage of low-frequency noise performance stemming from process-induced strain.

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