J Electron Test (2009) 25:145–156
DOI 10.1007/s10836-008-5095-x

A Built-in-Self-Test Σ-Δ ADC Prototype

Hao-Chiao Hong · Sheng-Chuan Liang · Hong-Chin Song

Received: 19 June 2008 / Accepted: 3 November 2008 / Published online: 31 January 2009

Abstract This paper presents a built-in-self-test (BIST) Σ-Δ ADC prototype. The BIST circuity uses the proposed modified controlled sine wave fitting (CSWF) procedure to calculate the signal power and the total-harmonic-distortion-and-noise power in time domain separately. Compared with conventional Fast Fourier Transform (FFT) analysis, neither complex CPU/DSP nor bulky memory is required. The added BIST circuitry is purely digital and the hardware overhead is as low as 11.9 K gates. A prototype comprising the second-order design-for-digital-testability Σ-Δ modulator chip and an FPGA board which implements the digital functions is used to demonstrate the effectiveness of the BIST design. Measurement results show that the SNDR difference between conventional FFT analysis and the proposed BIST design of the standard −6 dBFS, 1 KHz tone test is only 0.3 dB. Furthermore, the tested dynamic range values by both methods are the same. The proposed BIST implementation achieves the advantages of compact hardware, high test accuracy, and the flexibility of adjusting the stimuli which are important features for BIST applications.

Keywords BIST · Σ-Δ ADC · Controlled sine wave fitting · Output response analyzer

Responsible Editor: A. Ivanov

H.-C. Hong (✉) · S.-C. Liang · H.-C. Song
Department of Electrical and Control Engineering,
National Chiao Tung University, Hsinchu, Taiwan,
Republic of China
e-mail: hchong@cn.nctu.edu.tw

1 Introduction

Testing high resolution ADCs such as Σ-Δ modulators is very costly because of the requirements of high-end mixed-signal automatic test equipment (ATE) and a long test time. Besides, the test setup is very bothersome since the cost of an ultra-low noise testing environment is substantial [5]. In addition, the testability becomes worse when the high resolution ADC is embedded in a complex system-on-chip (SoC) device. To address these issues, build-in-self-test (BIST) techniques are drawing more and more attention [1–3, 7–9, 12, 16, 18, 20–25].

In [10], we proposed a design-for-digital-testability (DfDT) structure for Σ-Δ modulators which simultaneously achieves a low analog circuit overhead, high measurement accuracy, high fault observability, and the capability to perform at-speed tests. The DfDT structure allows the high-resolution Σ-Δ modulator to be tested with digital stimuli. The large noise margins of digital signals greatly alleviate the difficulty of setting up a low-noise test environment. Since the digital tests are like functional tests, a fully BIST Σ-Δ ADC can be realized by adding a cost effective digital stimulus generator (DSG) and an embedded output response analyzer (ORA).

Conventional functional tests analyze the output responses in frequency domain [4, 5, 13, 16]. By deriving the output spectra of the circuit under test (CUT), various test data can be obtained. However, at least a CPU or DSP as well as bulky memory are usually necessary for the ORA to conduct the complex Fast Fourier transform (FFT). Its applicability depends on the availability of such resources.

Instead of using frequency domain analysis, a controlled sine wave fitting (CSWF) method that performs the SNDR analysis in time domain has been proposed [15]. The idea is that the signal and the total-harmonic-distortion-and-noise (THD+N) powers can be calculated separately. In practice, the output response of an ADC consists of the stimulus tone, the offset, and the THD+N parts. If we can generate an error-free digital reference signal which is identical to the stimulus tone part of the output response, then the THD+N signal can be obtained by subtracting the error-free digital reference signal and the offset parts from the output response in time domain. By calculating the power of the residue THD+N signal and comparing it with the designated threshold value, a pass or fail decision can be made.

The CSWF BIST design in [15] is for testing general ADCs. The stimulus generation is achieved by controlling a digital pulse density modulated (PDM) signal following a RC low-pass filter. To provide high SNDR stimuli, the corner frequency of the RC low-pass filter should be as low as possible. As a consequence, the required values of the resistance and capacitance may be too large to be realized on-chip. The scheme also demands for some multiplication during estimating the amplitude of the stimulus tone at the output response. A BIST function that needs multiplication is not preferable since it usually results in a higher hardware overhead.

Rolindez et al. proposed a BIST design based on the CSWF method for the Σ-Δ ADC [21]. Similar to the DfDT design in [10], their analog core also eliminates the need of the bulky RC low-pass filter. Yet the hardware overhead of the digital circuits could be improved.

This paper presents a BIST Σ-Δ ADC prototype that uses the modified CSWF procedure for testing the specified parameters of a Σ-Δ ADC including the dynamic range, the SNDR, the offset, and the gain error. It would be useful for the applications in which other test parameters are not a concern such as testing some consumer audio products.

The BIST design benefits from the single-bit input/output (I/O) characteristics of the Σ-Δ modulator under test (MUT) as well as the simple hardware implementation of the CSWF ORA. In addition, we adopted the area-efficient oscillator circuit in [14] for generating the BIST stimuli. It is more flexible and low cost. The remainder of this paper is organized as follows. Section 2 describes the design of the ADC under test (AUT). Sections 3 and 4 discuss the design of the BIST system and detailed circuit implementation, respectively. A prototype has been built in which the DfDT second-order Σ-Δ modulator test chip in [10] was used as the MUT. The decimation filter and the rest of the BIST circuitry were realized by an FPGA. Measurement results will be shown in Section 5. Finally, Section 6 draws our conclusions.

2 Description of the Σ-Δ ADC Under Test

2.1 Modulator Under Test

Figure 1 shows the schematic of the DfDT MUT [10]. It's a conventional second-order Σ-Δ modulator design except for the DfDT structure indicated by the shaded area. A test mode control signal T is used to select the operation mode of the MUT. If $T = 0$ and $D_{BSG} = 1$, the MUT operates as a normal second-order Σ-Δ modulator does. In the normal mode, D_{MUT} is the PDM output of the analog input V_{ASG}. When T is set to 1, the MUT enters the test mode in which it accepts the Σ-Δ modulated bit-stream, D_{BSG}, as its test stimulus. In fact, the DfDT structure is reconfigured as a digital-to-charge converter which converts the digital stimulus into a two-level analog stimulus in the test mode.

Let A_S and f_{in} respectively represent the amplitude and the frequency of the desired sinusoidal stimulus tone, f_{CLK} be the sampling frequency of the MUT, and $X_{BIST}(z)$ be the z-transform of the sinusoidal stimulus tone whose amplitude is normalized to be 1. A digital Σ-Δ modulator is first used to modulate the nominal test stimulus, $A_S X_{BIST}(z)$, for generating the required D_{BSG}. Without loss of generality, the digital Σ-Δ modulator can be characterized by its I/O relationship which is expressed as

$$Y_{BSG}(z) = STF_{SDM}(z)A_S X_{BIST}(z) + NTF_{SDM}(z)E_{SDM}(z). \quad (1)$$

Above $STF_{SDM}(z)$, $NTF_{SDM}(z)$, and $E_{SDM}(z)$ represent the signal transfer function (STF), the noise transfer function (NTF), and the normalized quantization noise of the digital Σ-Δ modulator, respectively. For convenience, we define $Y_{BSG}(z) \equiv 2D_{BSG}(z) - 1$ which is the normalized bit-stream output. The normalized bit-stream, $y_{BSG}(n)$, has a value of either 1 or −1.

Similarly, the normalized I/O relationship of the test mode enabled MUT can be shown to be [10]

$$\begin{aligned} Y_{MUT}(z) = {} & STF_{MUT}(z)STF_{SDM}(z)A_S X_{BIST}(z) \\ & + STF_{MUT}(z)NTF_{SDM}(z)E_{SDM}(z) \\ & + NTF_{MUT}(z)E_{MUT}(z) \\ & + THDN_{MUT}(z) + OS_{MUT}, \end{aligned} \quad (2)$$

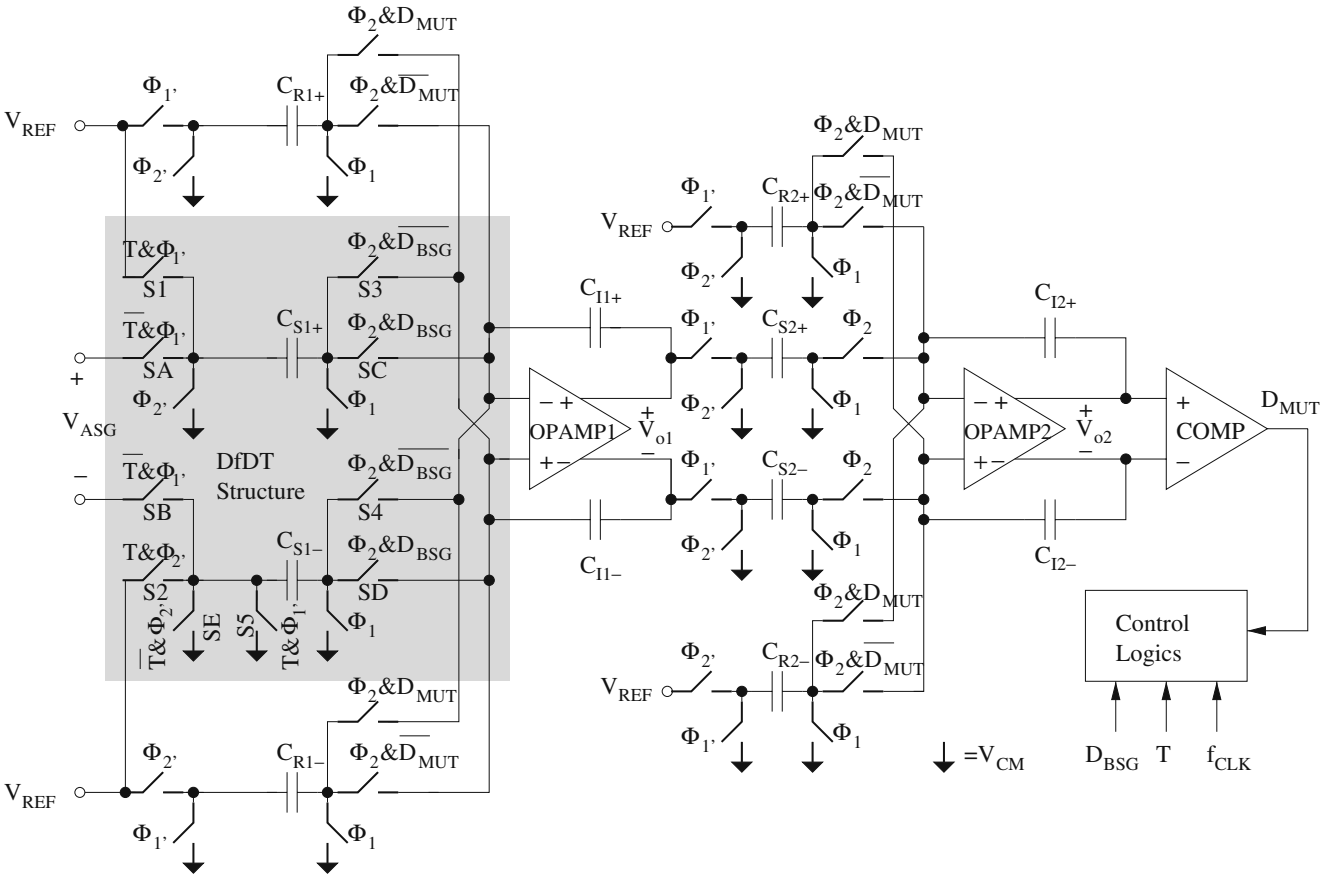

Fig. 1 Schematic of the DfDT second-order Σ-Δ modulator [10]

where $Y_{MUT}(z) \equiv 2D_{MUT}(z) - 1$ symbolizes the normalized digital output of the MUT. The terms $STF_{MUT}(z)$ and $NTF_{MUT}(z)$ are the STF and NTF of the MUT. $E_{MUT}(z)$, $THDN_{MUT}(z)$, and OS_{MUT} correspond to the quantization noise, the THD+N signal, and the offset generated by the MUT, respectively.

2.2 Decimation Filter

Note that the terms $STF_{MUT}(z)NTF_{SDM}(z)E_{SDM}(z)$ and $NTF_{MUT}(z)E_{MUT}(z)$ in Eq. 2 are high-pass shaped quantization noises. A complete Σ-Δ ADC needs a decimation filter to remove the out-of-passband noise and to down-sample its final output to the Nyquist rate. A simple implementation of the decimation filter uses a comb filter [6] whose transfer function is

$$H_{COMB}(z) = \left(\frac{2}{OSR}\frac{1 - z^{-OSR/2}}{1 - z^{-1}}\right)^{k+1}. \quad (3)$$

OSR and k above stand for the over-sampling ratio (OSR) and the order of the MUT. In our design, an additional finite-impulse-response (FIR) compensation filter is added to compensate the droop of the comb filter's frequency response around the passband edge such that the transfer function of the decimation filter, $H_{DEC}(z)$, has an amplitude response approximating to 1 within the passband.

Most of the out-of-passband noises in Eq. 2 will be removed after $Y_{MUT}(z)$ passing through the decimation filter. As a result, the decimated output of the Σ-Δ AUT, $Y_{DEC}(z')$, can be approximately expressed by

$$Y_{DEC}(z') \simeq STF_{MUT}(z')H_{DEC}(z')A_S X_{BIST}(z') + THDN_{MUT}(z')H_{DEC}(z') + OS_{MUT}. \quad (4)$$

Here, we use the notation $z' \equiv e^{j2\pi f \cdot OSR/f_{CLK}}$ to indicate that the output of the decimation filter has been down-sampled by a factor of OSR.

3 BIST Design

3.1 Block Diagram

Figure 2 shows the block diagram of the proposed BIST Σ-Δ ADC. It consists of the AUT, the DSG, and the

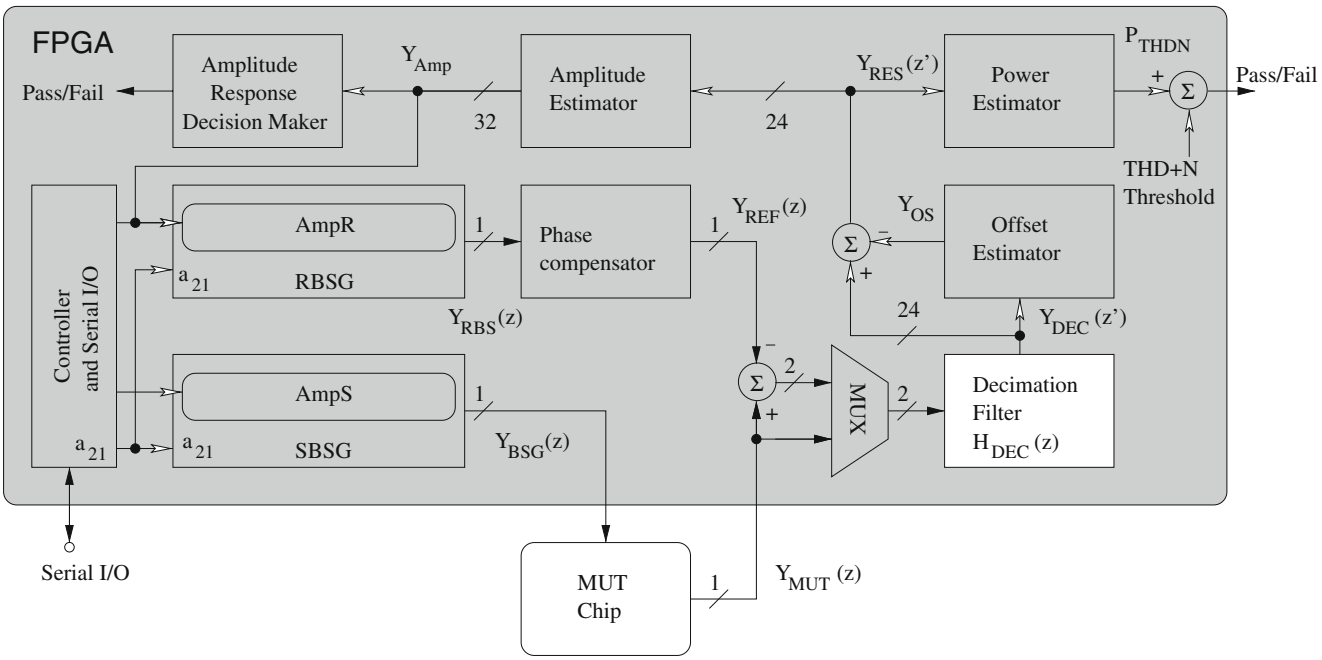

Fig. 2 Block diagram of the proposed Σ-Δ ADC prototype

ORA. The AUT is composed of the DfDT second-order Σ-Δ modulator chip proposed in [10] and the digital decimation filter.

The DSG comprises two bit-stream generators (BSGs): the stimulus bit-stream generator (SBSG) for generating the stimuli for the AUT, and the reference bit-stream generator (RBSG) for generating the digital reference signals. The amplitudes of the generated stimulus tones can be well controlled. In particular, we use *AmpS* to represent the amplitude of the stimulus tone generated by the SBSG, and *AmpR* for that of the RBSG. The input a_{21} sets the frequency of the generated stimulus tone. The rest of the block diagram belongs to the ORA.

Equations 2 and 4 reveal an important feature of the AUT: the single-bit output of the MUT contains similar in-band information to the decimated output of the AUT. In other words, the necessary BIST computations can be moved from the multi-bit side to the single-bit side without significant impact on the BIST results. Therefore, the phase compensator and the subtractor for removing the stimulus tone part of the output response are moved to the single-bit side to save the hardware cost.

3.2 The Modfied Controlled Sine Wave Fitting BIST Procedure

The BIST design operates based on the CSWF procedure [15] but with some modification. There are three BIST steps to complete a test. They are used to obtain the offset, the amplitude response, and the THD+N power, respectively. Figures 3, 4, and 5 show the

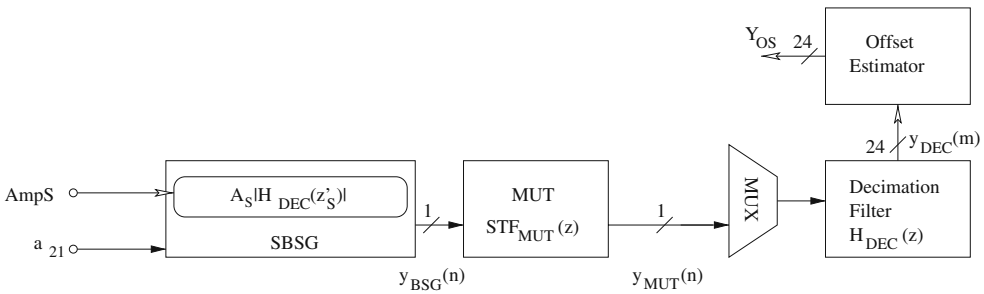

Fig. 3 First BIST step: calculating the offset of the MUT

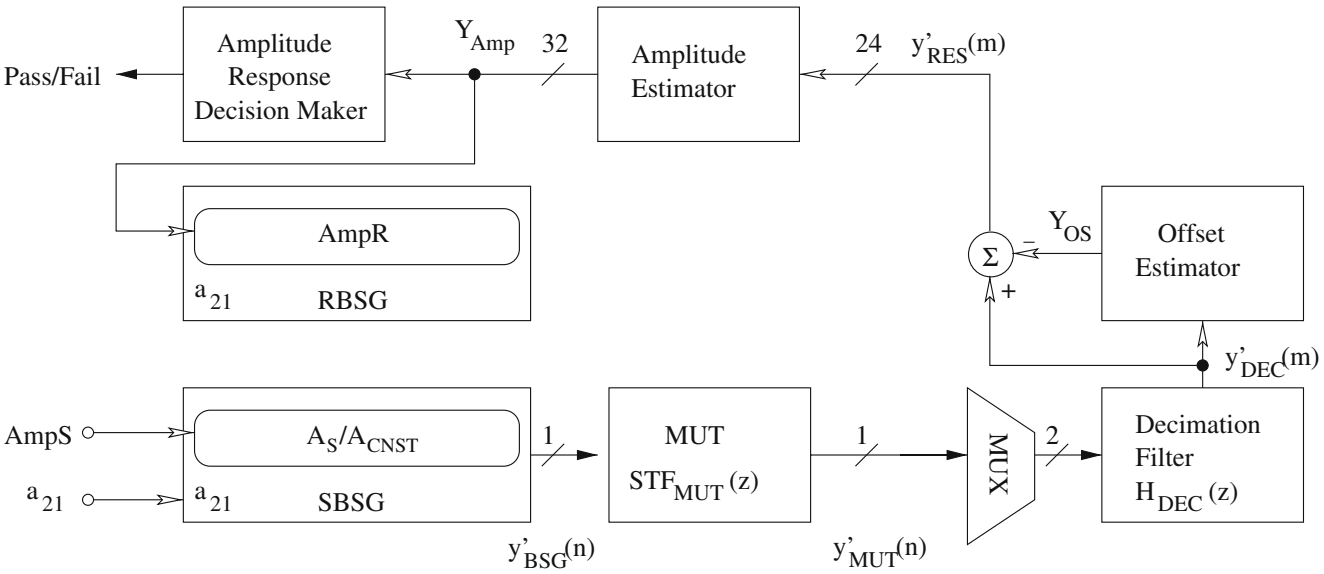

Fig. 4 Second BIST step: estimating the amplitude of the stimulus tone in the output response

operation in each BIST step. Every BIST step acquires N decimated output samples for analysis where N is selected to be a power of two to simplify the hardware implementation. In addition, each BIST step conducts a coherent analysis. That is, a_{21} is carefully designed such that the N decimated output samples contain integer cycles of the stimulus tone.

In the following, we use the symbols with a prime to indicate they are the signals in the second BIST step. $y'_{RES}(m)$ is an example. While the symbols with a double prime such as $y''_{RES}(m)$ and $Y''_{MUT}(z)$ belong to the third BIST step. The symbols without additional prime notation indicate that they are generated within the first BIST step.

3.2.1 Calculating the Offset

The offset estimator whose function is

$$Y_{OS} = \frac{1}{N}\sum_{m=1}^{N} y_{DEC}(m) \tag{5}$$

accepts the decimated output of the AUT, $y_{DEC}(m)$, for estimating the offset [15]. Due to the coherent

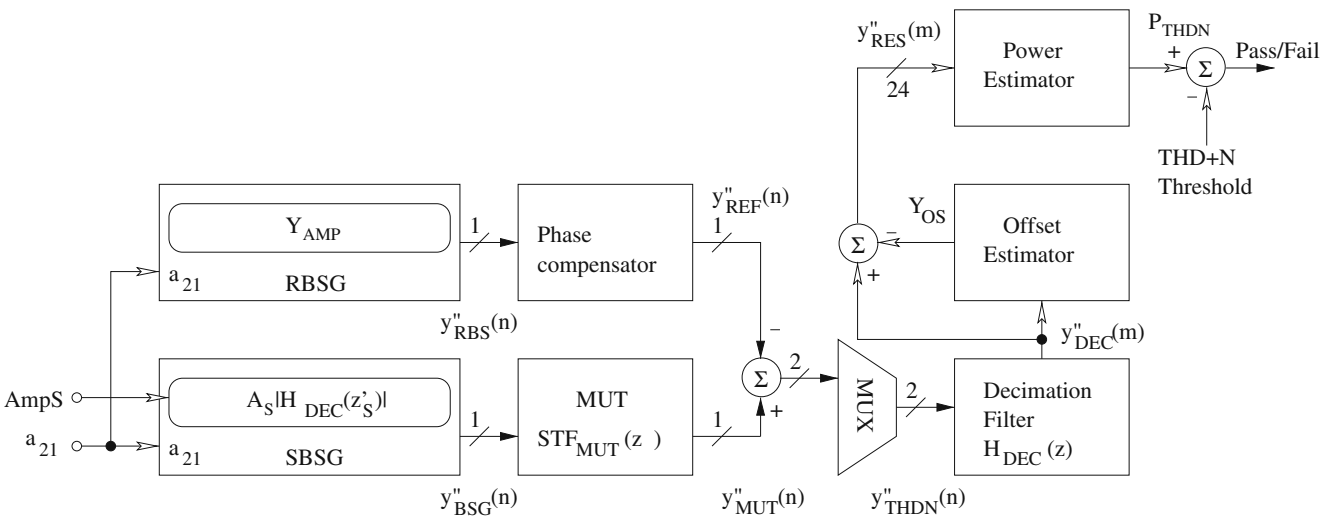

Fig. 5 Third BIST step: calculating the THD+N power

characteristic of the analysis, the stimulus tone part in Eq. 4 will be vanished no matter what value $AmpS$ is set to. To reduce the necessary parameters that need to be stored for a given test, we set $AmpS$ to be $A_S|H_{DEC}(z'_S)|$ which is the same value that will be used in the BIST step 3. As a result, the output of the offset estimator is

$$Y_{OS} = OS_{MUT} + \frac{1}{N}\sum_{m=1}^{N} thdn_{MUT}(m) \tag{6}$$

according to Eqs. 4 and 5. Since $thdn_{MUT}(m)$ approximates to a random process whose average is zero, Y_{OS} gives a good estimation for OS_{MUT}.

3.2.2 Calculating the Amplitude of the Stimulus Tone at the Output Response

In the second BIST step, the SBSG generates the bitstream containing the sinusoidal tone as the stimulus. The offset part of the decimated output of the AUT is removed first. Then, the amplitude estimator accepts the offset-free response $y'_{RES}(m)$ and calculates the amplitude.

Mattes et al. suggested that the function of the amplitude estimator can be [15]

$$Y_{Amp} = \frac{1}{A_{CNST}}\frac{1}{N}\sum_{m=1}^{N}|y'_{RES}(m)|, \tag{7}$$

where

$$A_{CNST} = \frac{1}{N}\sum_{m=1}^{N}|\sin(2\pi f_{in} OSR \cdot m/f_{CLK})| = \frac{2}{\pi}. \tag{8}$$

However, Eq. 7 requires an undesirable multiplication which needs more complex hardware to implement. Hence, we modified the CSWF procedure and the following simpler function is used for the amplitude estimator:

$$Y_{Amp} = \frac{1}{N}\sum_{m=1}^{N}|y'_{RES}(m)|. \tag{9}$$

To avoid affecting the accuracy of the BIST result, the amplitude of the generated stimulus tone in this step is set to A_S/A_{CNST} instead of A_S. This setup value can be calculated in advance and stored in some embedded memory.

According to Eqs. 4 and 9, the output of the amplitude estimator is

$$Y_{Amp} = A_S|STF_{MUT}(z'_S)||H_{DEC}(z'_S)|, \tag{10}$$

where $|STF_{MUT}(z'_S)|$ and $|H_{DEC}(z'_S)|$ represent the amplitude responses of the MUT's STF and the transfer function of the decimation filter at the stimulus frequency, respectively. An amplitude response decision maker is followed to check if the estimated output amplitude is within the specification.

3.2.3 Calculating the THD+N Power

The obtained Y_{Amp} in the second BIST step is used to set the stimulus tone's amplitude generated by the RBSG in the third BIST step. Meanwhile, the SBSG generates the stimulus tone whose amplitude is set to $A_S|H_{DEC}(z'_S)|$. Because $|H_{DEC}(z'_S)|$ is a deterministic value, the setup value can be computed in advance and loaded. Thus, no multiplication is required. In practice, we used the circuit simulations to derive the values so that the effects of the finite resolution of the digital signals can be taken into account.

According to Eq. 2, the test setup leads to

$$\begin{aligned} Y''_{MUT}(z) = {} & STF_{MUT}(z_S)z^{-1}A_S|H_{DEC}(z'_S)|X_{BIST}(z) \\ & + STF_{MUT}(z)NTF_{SDM}(z)E_{SDM1}(z) \\ & + NTF_{MUT}(z)E_{MUT}(z) \\ & + THDN_{MUT}(z) + OS_{MUT}. \end{aligned} \tag{11}$$

From Eqs. 1 and 10, we have

$$\begin{aligned} & Y''_{REF}(z) \\ & = z^{-1}A_S|STF_{MUT}(z'_S)||H_{DEC}(z'_S)|X_{BIST}(z)H_{FC}(z) \\ & \quad + NTF_{SDM}(z)E_{SDM2}(z). \end{aligned} \tag{12}$$

The term $H_{FC}(z)$ represents the transfer function of the phase compensator. Original CSWF procedure requires several cycles to calibrate the phase shift [15]. Yet the phase calibration loop is saved in our implementation. The reason is that the phase shift is almost a constant for our Σ-Δ modulator core due to its over-sampling nature. Since the phase response of $STF_{MUT}(z)$ approximates to z^{-2} for the MUT, we set

$$H_{FC}(z) = z^{-2} \tag{13}$$

such that the stimulus tone parts of Eqs. 11 and 12 are approximately equal.

By subtracting Eq. 12 from Eq. 11, we have

$$\begin{aligned} Y''_{THDN}(z) \simeq {} & NTF_{MUT}(z)E_{MUT}(z) \\ & + NTF_{SDM}(z) \\ & \times (STF_{MUT}(z)E_{SDM1}(z) - E_{SDM2}(z)) \\ & + THDN_{MUT}(z) + OS_{MUT}. \end{aligned} \tag{14}$$

The shaped quantization noise related terms in Eq. 14, $NTF_{SDM}(z)\left(STF_{MUT}(z)\,E_{SDM1}(z) - E_{SDM2}(z)\right)$ and $NTF_{MUT}(z)E_{MUT}(z)$, will be suppressed by the deci-

mation filter. Therefore, the decimated output of the AUT in the third BIST step approximates to

$$Y''_{DEC}(z') \simeq THDN_{MUT}(z') + OS_{MUT}. \quad (15)$$

By removing the offset from $Y''_{DEC}(z')$, the power estimator whose function is

$$P_{THDN} = \frac{1}{N}\sum_{m=1}^{N} y''_{RES}(m)^2 \quad (16)$$

will output the total THD+N power in the passband. Pass/Fail decision is made by comparing P_{THDN} with the predetermined threshold of the THD+N power.

For each test, only three 32-bit parameters including a_{21}, A_S/A_{CNST}, and $A_S|H_{DEC}(z'_S)|$ have to be stored or loaded.

4 Circuit Design

All the necessary BIST functions are digital. It means that the BIST circuitry will benefit from the robustness, scalability, and lower power features of advanced CMOS technology.

4.1 Bit-stream Generator

As has been discussed in Section 3, the BIST design requires two identical BSGs whose generated stimuli should be well controlled. We adopted the area-efficient oscillator proposed by Lu et al. for the design of the BSGs [14]. Figure 6 shows the schematic.

The BSG is a digital resonator embedded with a single-bit digital Σ-Δ modulator. The single-bit characteristic of the Σ-Δ modulator avoids the necessity of any multiplier for implementation. In fact, this embedded digital Σ-Δ modulator plays the same role as that we have mentioned in Section 2. Equation 1 actually describes the I/O relationship of it.

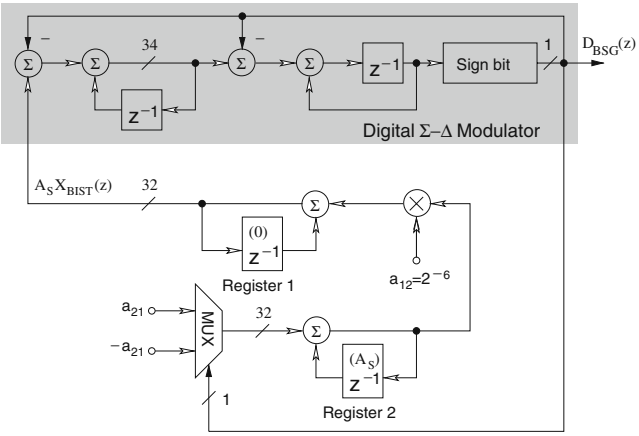

Fig. 6 Schematic of the BSG using oversampling technique [14]

To sustain stable oscillation, detailed analysis showed that the STF of the digital Σ-Δ modulator should be exactly equal to z^{-1} [14]. A second-order Σ-Δ modulator having such an STF can be found in [14] and was adopted in our design.

The frequency of the stimulus tone is determined by the parameters a_{21} and a_{12} [14] with respect to

$$f_{in} = f_{CLK}\frac{\cos^{-1}(1 - a_{12}a_{21}/2)}{2\pi}, 0 < a_{12}a_{21} < 2;$$
$$f_{in} = f_{CLK}\left(\frac{1}{2} - \frac{\cos^{-1}(1 - a_{12}a_{21}/2)}{2\pi}\right), 2 < a_{12}a_{21} < 4. \quad (17)$$

We fixed the value of a_{12} at 2^{-6} to save the hardware cost. Therefore, only the frequency parameter a_{21} has to be stored or loaded per test. On the other hand, the stimulus amplitude can be well controlled by the initial value of Register 2 while keeping the initial value of Register 1 at zero. That is, $AmpS$ and $AmpR$ mentioned in Section 3 are the initial values of the Register 2 in the corresponding BSGs.

4.2 Output Response Analyzer

The functions of the offset, amplitude, and power estimators are listed in Eqs. 5, 9, and 16, respectively. Their implementations are shown in Fig. 7. Thanks to these simple functions, the circuits mainly comprise adders and registers.

Although Eq. 16 requires the only multiplication, a much simpler serial multiplier was used to implement it since the input of the power estimator has been downsampled by a factor of 128.

4.3 Hardware Overhead

We synthesized the digital design including the DSG, the ORA, and the decimation filter with a 0.18 μm standard cell library. Table 1 lists the synthesis results.

The total hardware overhead is less than 12 K gates. It is much less than the similar BIST design proposed by Rolindez et al. which is also based on the same CSWF method [21]. They used a 2252-bit shift register to store the binary stimulus. In one of their design examples, a 563 by 19-bit memory and a 563 by 16-bit memory were used to store the reference signal and the output response for calculating the SNDR value. In addition, their ORA is more complex than ours since they adopted the original CSWF design in [15]. Put the

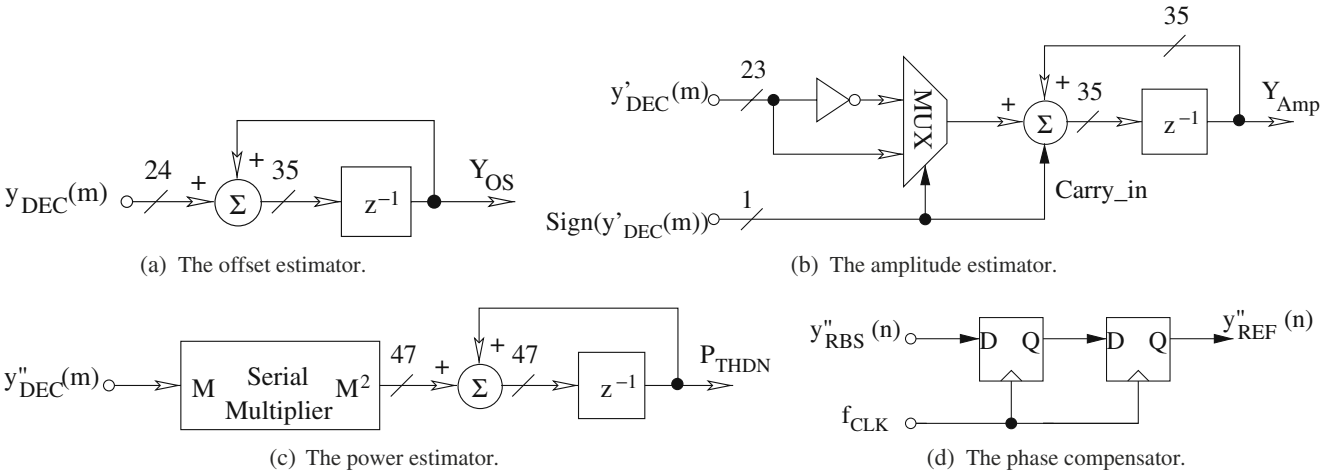

Fig. 7 Hardware implementation of the ORA (**a**–**d**)

ORA and the memory aside, the shift register along is already larger than 13 K gates. Besides, our design is more flexible and compact when multiple tests (with the stimuli of various frequencies and amplitudes) are required.

5 Experimental Results

To verify the BIST design, the DfDT second-order Σ-Δ modulator chip proposed in [10] was used as the MUT. All the digital circuits including the decimation filter, the DSG, and the ORA were implemented with an FPGA.

In the following measurements, the sampling clock frequency of the MUT was set to 6.144 MHz and the OSR was set to 128. It corresponds to an output rate of 48KS/s. The minimum-four-term window was applied to derive all spectra. The sample numbers taken for each analysis of the $y''_{MUT}(n)$ and $y''_{RES}(m)$ were 2^{18} and 2048, respectively. Meanwhile, the stimulus frequency was set to $43/2^{18}$ times the sampling clock frequency which is around 1KHz, and the stimulus amplitudes of the tests (A_S) were set to −6 dBFS unless otherwise noticed.

Table 1 Summary of the BIST circuitry

Block	Gate counts
DSG	2.35 K × 2
ORA[a]	5.6 K
Controller and Serial I/O	1.6 K
Total BIST circuitry	11.9 K
Decimation Filter	15 K

[a]Including the offset, amplitude, and power estimators as well as other auxiliary circuits

5.1 The −6 dBFS, 1KHz Tone Test

Figure 8 depicts the output spectra of the MUT's output bit-stream $Y''_{MUT}(z)$ and the decimated residue signal $Y''_{RES}(z')$ of the standard 1-KHz test for audio applications [17]. The original offset component of $Y''_{MUT}(z)$ is −55.7 dBFS. It has been successfully eliminated to be less than −106 dBFS which is already on the noise floor. On the other hand, the residue stimulus tone in $Y''_{RES}(z')$ is less than −107.5 dBFS which also lies on the noise floor. The spectra show that the in-band noise floors of both signals are almost identical. It verifies that the BIST functions work properly.

The proposed BIST implementation gave a peak SNDR of 74.3 dB while the conventional FFT analysis resulted in a 74.6 dB SNDR of the same test. A part of the subtle difference is due to that the FFT analysis

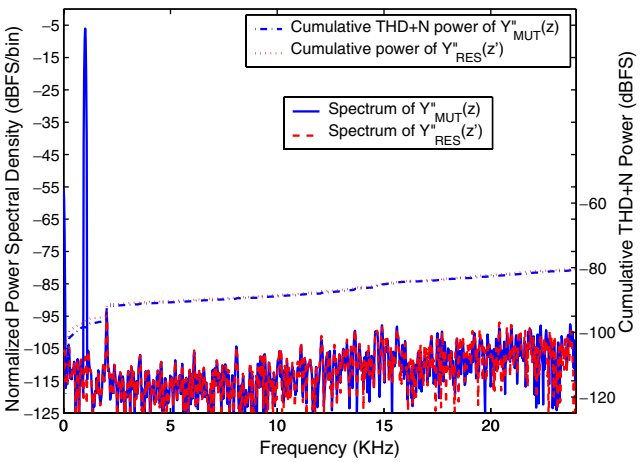

Fig. 8 Measured spectra of the raw output $Y''_{MUT}(z)$ and the decimated $Y''_{RES}(z')$ of the same test with the −6 dBFS stimulus

does not count in the spectral bins of the stimulus tone and the offset as shown by the cumulative THD+N power plots in Fig. 8. This will degrade the BIST results by −0.1 dB. The finite resolution of the digital circuits which induces truncation errors may be another reason for the SNDR difference. Yet, the subtle difference is already within the measurement uncertainty.

5.2 Dynamic Range Tests

Figure 9 shows and compares the corresponding measured SNDR results using FFT and BIST methods of the dynamic range tests. The stimulus amplitude was swept from −60 to −4 dBFS. The BIST results are very close to those of FFT analysis. The dynamic ranges measured by both methods are the same 82.3 dB. The SNDR differences between them have a maximum value of 1.45 dB at −56 dBFS and a minimum value of −5.7 dB at −4 dBFS. To understand the root causes of the deviation, Figs. 10 and 11 depict their spectra as well as the cumulative THD+N power of $Y''_{MUT}(z)$ and the cumulative power of $Y''_{RES}(z')$.

In the low frequency range (< 20 KHz) of Fig. 10, the noise floors of $Y''_{MUT}(z)$ and $Y''_{RES}(z')$ are almost identical. The 1.45 dB SNDR difference comes from the high frequency range in which the noise floor of $Y''_{MUT}(z)$ is somewhat higher than that in Fig. 8. It is because the term $NTF_{SDM}(z)(STF_{MUT}(z)E_{SDM1}(z) - E_{SDM2}(z))$ in Eq. 14 is stimulus dependent. For this particular test, the term $STF_{MUT}(z)E_{SDM1}(z)$ is correlated to the term $E_{SDM2}(z)$ more closely. Consequently, more shaped quantization noise power is left in the passband. Since $Y''_{RES}(z')$ is low-pass filtered

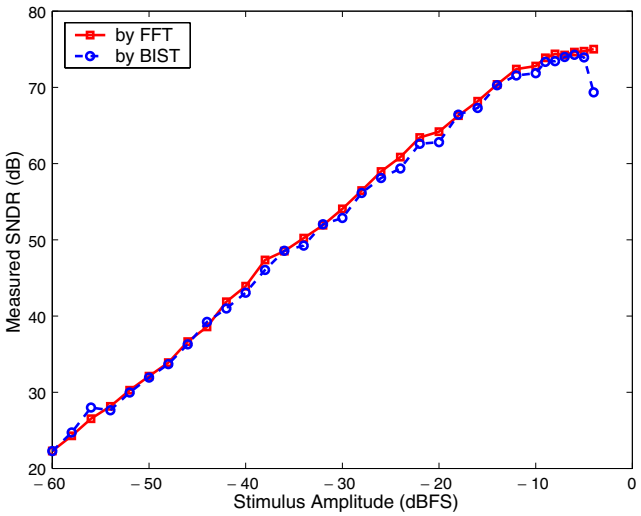

Fig. 9 Measured SNDR results of the dynamic range tests

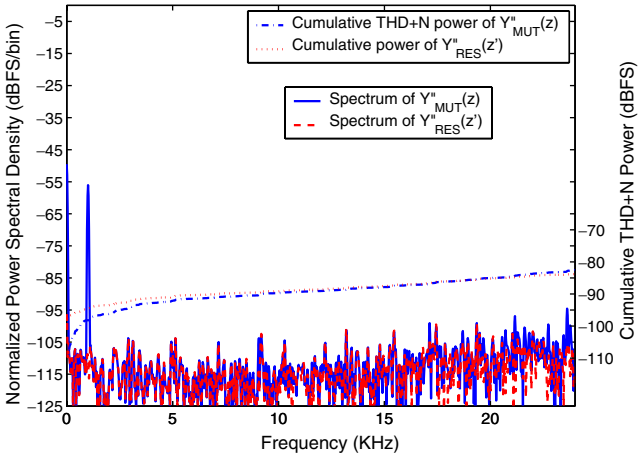

Fig. 10 Spectra of the raw output $Y''_{MUT}(z)$ and the decimated $Y''_{RES}(z')$ of the same test with the −56 dBFS stimulus

while $Y''_{MUT}(z)$ is not, $Y''_{RES}(z')$ has less in-band noise power. It explains the random variation of the SNDR differences measured by both methods.

On the other hand, the mechanism that leads to the −5.67 dB SNDR difference with the −4 dBFS stimulus is different. According to Fig. 11, the root cause is the too high residue tone in $Y''_{RES}(z')$. Recall that the modified CSWF procedure requests the SBSG to generate the stimulus whose amplitude is 3.92 dB higher than the designated A_S in the second BIST step. However, the digital second-order Σ-Δ modulator in the SBSG will be overloaded if the setup value of the stimulus amplitude is too high [19]. Take $A_S = -4$ dBFS as an example, the SBSG has to generate a −0.08 dBFS stimulus which indeed saturates the digital Σ-Δ modulator. Once the digital Σ-Δ modulator is overloaded, the

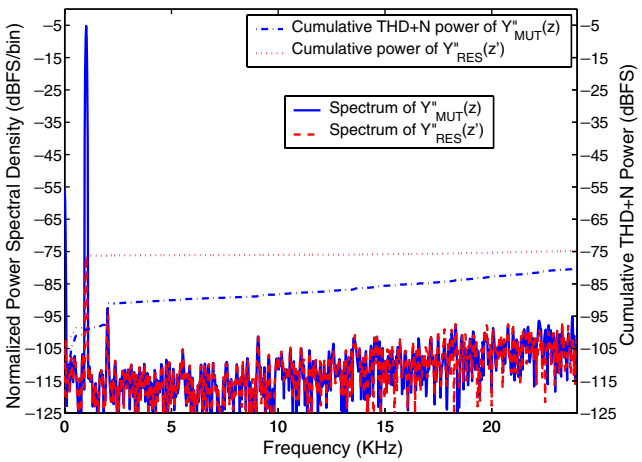

Fig. 11 Spectra of the raw output $Y''_{MUT}(z)$ and the decimated $Y''_{RES}(z')$ of the same test with the −4 dBFS stimulus

generated stimulus can not be well controlled any more. As a consequence, the BIST results are less accurate for the stimulus amplitudes higher than −5 dBFS.

5.3 Test Bandwidth

Figure 12 shows the measured SNDRs by applying the stimuli with different frequencies. The BIST results and the corresponding FFT results are within 1.5 dB when the stimulus frequency is not higher than 8 KHz. If the stimulus frequency increases further, the SNDR degradation becomes more significant for both methods. The major reason is that the in-band SNDR of the bit-stream $y''_{BSG}(n)$ generated by the SBSG is getting worse as shown by Fig. 12. Since the bit-stream is our stimulus, the functional test nature of the BIST design restricts the highest tested SNDR value of the AUT to be less than that of the stimulus. As a result, even the FFT results follow the decreasing trend of the SBSG's in-band SNDR. In practice, a poor in-band SNDR of the stimulus implies the oscillation of the BSG is less stable. That is, the amplitude of the generated stimulus tone no longer can be well controlled. The deviation between the setup value and generated value results in incomplete cancellation of the stimulus tone in the third BIST step. Consequently, the residue tone power is getting higher as the stimulus frequency is increasing. The residue tone power plot in Fig. 13 illustrates this phenomenon.

Table 2 summarizes the performance of the proposed BIST Σ-Δ ADC.

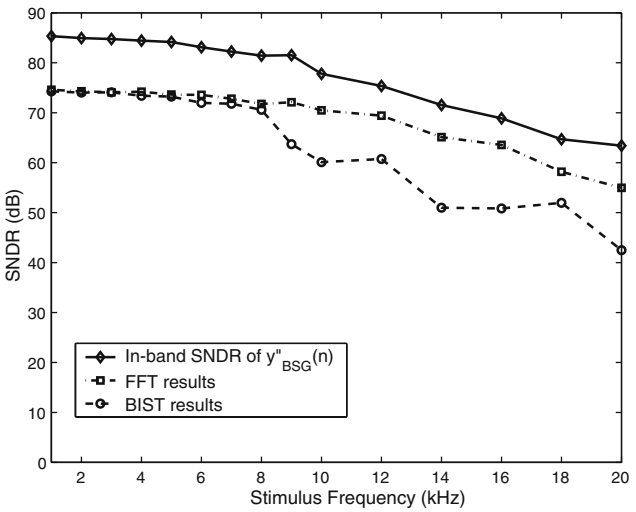

Fig. 12 Measured SNDR vs. stimulus frequency by the BIST circuitry and by FFT analysis

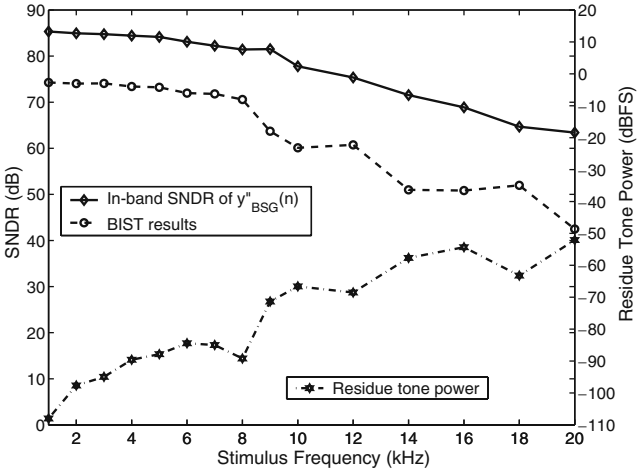

Fig. 13 Measured SNDR vs. stimulus frequency of the BIST and FFT analysis and the corresponding residue tone power

5.4 Comparison with the Original CSWF Design

It is worth to note that the original CSWF design proposed by Mattes et al. is for testing general ADCs. Consequently, no optimization was performed in their work in order to cover wide applications. On the other hand, we focused on the optimal BIST design for the specified Σ-Δ AUT. That's the main reason why our BIST showed good performance both in testing cost and accuracy. In the following, we discuss the major differences between the original CSWF design and ours.

The CSWF method consists of the stimulus and reference generation and the output response analysis. For generating the stimulus, Mattes et al. proposed feeding a simple RC low-pass filter with a Σ-Δ modulated bit-stream [15]. The bit-stream was generated by a digital Σ-Δ modulator operating at an OSR of 958 to obtain a theoretical SNDR as high as 147 dB. However, their experimental results showed that the peak SNDR of the analog test stimulus is less than 56 dB [15]. The major issue is on the digital-to-analog interface where a

Table 2 Performance summary

Test items	Analysis method	
	FFT	BIST
OSR	128	128
Offset	−55.7 dBFS	−55.7 dBFS
Dynamic range[a]	82.3 dB	82.3 dB
SNDR @ −6 dBFS	74.6 dB	74.3 dB
Peak SNDR	75.0 dB	74.3 dB
Test bandwidth	10 KHz	8 KHz

[a]Dynamic range = SNDR @−60 dBFS (in dB) + 60 dB [17]

discrete-time signal is converted into a continuous-time one. Practical circuit impairments keep the SNDR of the test stimulus far from the theoretical one.

For our AUT, the DfDT structure avoids the necessity of converting a discrete-time signal to a continuous-time signal but to a synchronized discrete-time analog signal. As a result, our design is more robust than that in [15]. In addition, we adopted the area-efficient oscillator [14] for generating the digital stimuli to save area, whereas Mattes et al. used a software Σ-Δ modulator which may require bulky CPU and memory in embedded applications.

For the ORA part, we made efforts to reduce the hardware cost without degrading the test accuracy. The benefits are the results of that our BIST design is for the particular Σ-Δ AUT. The Σ-Δ AUT has an important characteristic: the in-band signals of the bit-stream output and the decimated output are very similar. Therefore, we can move the necessary BIST computations from the multi-bit side to the single-bit side to save more area without impact on the testing accuracy. We also modified the CSWF procedure such that no parallel multiplier is required in the implementation.

The testing accuracy of the CSWF method mainly relies on if the stimulus response and the offset can be accurately removed in the final BIST step. In other words, it depends on how accurate the offset, response amplitude, and response phase are estimated and compensated. For the offset and response amplitude parts, our BIST design is similar to the original CSWF design, and thus there is no significant difference. Calibrating the phase may be the major difference. The original CSWF design tried to adjust the phase of the reference signal such that the amplitude of the residue signal is minimized. If it treats the AUT as a black box, the phase calibration loop in it may be able to adjust integer output cycles only. Since the Σ-Δ modulator is an oversampling type ADC, the output period is 128 times the clock period in our case. As a result, the resulted phase error will be around 2 clock cycles after the phase calibration is done. Unfortunately, it has been shown that a phase error as small as one clock cycle will make the cancellation of the stimulus tones in the last BIST step very poor and severely degrades the test accuracy [15].

Even with the assumption that the phase calibration loop can adjust the reference signal by integer fine clock cycles, the results will be the same as ours. As shown in Fig. 8, the residue tone of our test is already below −106 dBFS. It indicates that there is no headroom for improvement.

6 Conclusion

A cost effective BIST Σ-Δ ADC prototype based on the proposed modified CSWF procedure is presented. The BIST design can test the dynamic range, the SNDR, the offset, and the gain error of the AUT. It eliminates the need of any complex circuitry such as CPU, DSP, and parallel multiplier and thus saves a lot of hardware overhead. The measurement results of our prototype show that the SNDR difference between the proposed BIST and the conventional FFT analysis of the standard 1KHz, −6 dBFS test is only −0.3 dB. In addition, the measured dynamic range by our BIST design is the same as that from conventional FFT analysis. The proposed BIST implementation achieves the advantages of compact hardware, high accuracy, and the flexibility of adjusting the stimuli which are important features for BIST applications. The BIST design can be applied to the Σ-Δ ADC equipped with the decorrelating design-for-digital-testability (D^3T) structure. For such ADCs, the digital tests can have higher amplitude stimuli and higher test accuracy [11].

Acknowledgments This work was supported by the Ministry of Economic Affairs and National Science Council of Taiwan, R.O.C. under Grants 94-EC-17-A-01-S1-002, 95-EC-17-A-01-S1-002 and NSC93-2215-E-009-050, respectively.

References

1. Arabi K, Kaminska B (1997) Efficient and accurate testing of analog-to-digital converters using oscillation-test method. In: Proc European design and test conference, Paris, 17–20 March 1997, pp 348–352
2. Arabi K, Kaminska B (1998) On chip testing data converters using static parameters. IEEE Trans Very Large Scale Integr (VLSI) Syst 6(3):409–419
3. Azais F, Bernard S, Bertrand Y, Renovell M (2001) Implementation of a linear histogram BIST for ADCs. In: Proc design, automation and test in Europe (DATE), Munich, 13–16 March 2001, pp 590–595
4. Bernard S, Comte M, Azais F, Bertrand Y, Renovell M (2004) Efficiency of spectral-based ADC test flows to detect static errors. J Electron Test Theory Appl (JETTA) 20(3):257–267
5. Burns M, Roberts GW (2001) An introduction to mixed-signal IC test and measurement. Oxford University Press, Oxford
6. Candy JC (1986) Decimation for sigma delta modulation. IEEE Trans Commun 34(1):72
7. Chen H-K, Wang C-H, Su C-C (2002) A self calibrated ADC BIST methodology. In: Proc IEEE VLSI test symp (VTS), Monterey, April 2002, pp 117–122
8. Flores MDG, Negreiros M, Carro L, Susin AA, Clayton FR, Benevento C (2005) Low cost BIST for static and dynamic testing of ADCs. J Electron Test Theory Appl (JETTA) 21(3):205–219

9. Goyal S, Chatterjee A, Purtell M (2007) A low-cost test methodology for dynamic specification testing of high-speed data converters. J Electron Test Theory Appl (JETTA) 23(1):95–106
10. Hong H-C (2007) A design-for-digital-testability circuit structure for Σ-Δ modulators. IEEE Trans Very Large Scale Integr (VLSI) Systems 15(12):1341–1350
11. Hong H-C, Liang S-C (2008) A decorrelating design-for-digital-testability scheme for Σ-Δ modulators. IEEE Trans Circuit Syst I Regular papers (in press)
12. Hong H-C, Huang J-L, Cheng K-T, Wu C-W, Kwai D-M (2003) Practical considerations in applying sigma-delta modulation based analog BIST to sampled-data systems. IEEE Trans Circuits Syst 2 Analog Digit Signal Process 50(9): 553–566
13. IEEE Std 1241-2000 (2001) IEEE standard for teminology and test methods for analog-to-digital converters. IEEE-SA Standards Board, New York
14. Lu AK, Roberts GW (1994) A High-quality analog oscillator using oversampling D/A conversion techniques. IEEE Trans Circuits Syst 2 Analog Digit Signal Process 41(7):437–444
15. Mattes H, Sattler S, Dworski C (2004) Controlled sine wave fitting for ADC test. In: Proc IEEE int test conf (ITC), Charlotte, 26–28 October 2004, pp 963–971
16. Mendez-Rivera MG, Valdes-Garcia A, Silva-Martinez J, Sanchez-Sinencio E (2005) An on-chip spectrum analyzer for analog built-in testing. J Electron Test Theory Appl (JETTA) 21(3):205–219
17. Metzler B (1993) The audio measurement handbook. Audio Precision, Beaverton
18. Negreiros M, Carro L, Susin A (2003) Ultra low cost analog BIST using spectral analysis. In: Proc IEEE VLSI test symp (VTS), pp 77–82
19. Norsworthy SR, Schreier R, Temes GC (1997) Delta-sigma data converters: theory, design, and simulation. IEEE, Piscataway
20. Parthasarathy KL, Jin L, Kuyel T, Price D, Chen D, Geiger R (2003) Experimental evaluation and validation of a BIST algorithm for characterization of A/D converter performance. In: Proc IEEE int symp circuits and systems (ISCAS), pp 537–540
21. Rolindez L, Mir S, Bounceur A, Carbonero J-L (2006) A BIST scheme for sndr testing of Σ-Δ ADCs using sine-wave fitting. J Electron Test Theory Appl (JETTA) 22(4–6): 325–335
22. Ting H-W, Liu B-D, Chang S-J (2008) Histogram based testing method for estimating A/D converter performance. IEEE Trans Instrum Meas 57(2):420–427
23. Toner MF, Roberts GW (1996) A frequency response, harmonic distortion, and intermodulation distortion test for BIST of a sigma-delta modulator. IEEE Trans Circuits Syst 2 Analog Digit Signal Process 43(8):608–613
24. Wen Y-C, Lee K-J (2000) An on chip ADC test structure. In: Proc design, automation and test in Europe (DATE), pp 221–225
25. Wibbenmeyer J, Chen C-IH (2007) Built-in self-test for low-voltage high-speed analog-to-digital converters. IEEE Trans Instrum Meas 56(6):2748–2756

Hao-Chiao Hong received the BS, MS, and Ph.D. degrees in Electrical Engineering from National Tsing-Hua University, Taiwan, in 1990, 1992, and 2003, respectively. From 1997 to 2001, he was with Taiwan Semiconductor Manufacturing Company (TSMC) where he developed mixed-signal IPs for customers and process vehicles. He joined Intellectual Property Library Company, HsinChu, Taiwan, as the senior manager of the Analog IP Department in Aug., 2001. He has been with the Department of Electrical and Control Engineering, National Chiao Tung University, Hsinchu, Taiwan since Feb., 2004 where he is currently an assistant professor. His main research interests include the design-for-testability (DFT) and built-in self-test (BIST) techniques for mixed-signal systems and high performance mixed-signal circuit design.

Dr. Hong served as the executive secretary for Mixed-signal and RF Consortium, Taiwan from 2006 to Feb., 2008. He is currently the executive secretary of Heterogeneous Integration Consortium, Taiwan. Dr. Hong is a member of IEEE, a life member of Taiwan IC Design Society, and a member of VLSI Testing Technology Forum (VTTF).

Sheng-Chuan Liang received the BS and MS degrees in Electrical Engineering from National Cheng-Kung University, Taiwan, in 1993 and 1995, respectively. From 1997 to 2001, he was with Taiwan Semiconductor Manufacturing Company (TSMC), designing Analog circuits and process vehicles. He joined UBIG Electronics Company, HsinChu, Taiwan, working on Analog IPs from Nov., 2001. He is currently working toward his Ph.D. degree in National Chiao Tung University.

His research interests include the design of high performance ADC, DAC, PLL, and power management circuits, as well as the design-for-testability (DfT) and built-in-self-test (BIST) techniques for mixed-signal circuits.

Hong-Chin Song received the BS and MS degrees in Electrical and Control Engineering from National Chiao Tung University, Taiwan, in 2004 and 2007, respectively.

His major research interest is the built-in-self-test (BIST) design for ADCs.